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Publication Date

2023-11-02

DOI

10.1109/ecce53617.2023.10362157

Proceedings of the 15th IEEE Energy Conversion Congress and Exposition (ECCE 2023), Nashville, TN, USA, October 29 – November 2, 2023

Comparative Performance Analysis of Regulated Hybrid Switched-Capacitor Topologies for Direct 48 V to Point-of-Load Conversion

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***Abstract*—Multiple regulated hybrid switched-capacitor (SC) topologies have been proposed in previous literature for direct 48 V to point-of-load (PoL) conversion. To compare their theoretical potential, this paper establishes an analytical framework for topological characterization and performance comparison using two metrics: a) a normalized switch stress as an indicator for efficiency and b) a normalized passive component volume as an indicator for power density. Based on the proposed analytical framework, a comparative analysis of state-of-the-art 48-V-to-1-V regulated hybrid SC converters reveals that increasing the SC stage conversion ratio can reduce both metrics and thus improve both efficiency and power density at the same time.**

I. Introduction

High-performance microprocessors (e.g., CPUs, GPUs, ASICs, etc.) serve as the engine of data center platforms and the foundation for technical progress in areas such as artificial intelligence, deep learning, computer vision, speech recognition, big data mining, and countless other applications. In recent years, the electric power consumption of microprocessors has increased dramatically and is approaching 1000 W, due to the fast-growing demand of greater computational power. As power levels increase, the 48 $\mathrm{V_{dc}}$ bus architecture is gradually replacing the legacy 12 $\mathrm{V_{dc}}$ bus in modern data centers since the power distribution losses (i^2R losses) decrease by sixteen-fold with the quadrupling of the bus voltage. This makes the design of the voltage regulation modules (VRMs) responsible for the 48 V to Point-of-Load (PoL) power conversion more challenging with a quadrupled voltage conversion burden. In particular, the continued increase in power levels with maintained or even reduced space for power conversion leads to an ever-increasing demand for higher power density. Moreover, higher power conversion efficiency is required to ease the load on the thermal management system and to reduce the electricity consumption of data centers which can bring corresponding economic and environmental benefits.

To address the above challenges, multiple regulated hybrid switched-capacitor (SC) topologies have been proposed in previous literature for direct 48-V-to-PoL conversion in data centers [1]–[14]. As an emerging family of topologies, hybrid SC converters can leverage both the greatly superior energy density of capacitors compared to magnetic components [15], [16] and the better figure-of-merit (FOM) of low-voltage switching devices compared to high-voltage devices [17].

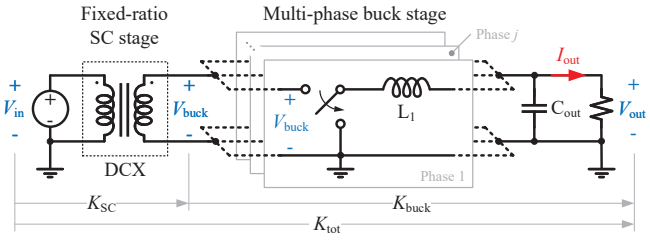

Fig. 1: General representation of a regulated hybrid SC topology consisting of a fixed-ratio SC stage and a multi-phase buck stage. The SC stage is modeled as an ideal DC transformer as presented in [18]. The input voltage V_{in} is first stepped down to V_{buck} by the SC stage. The buck stage then performs the remaining voltage conversion from V_{buck} to V_{out} and output voltage regulation. The total conversion ratio K_{tot} is allocated between the SC stage and the buck stage.

A regulated hybrid SC topology can be captured by the general representation in Fig. 1. In general, it consists of two stages: 1) a fixed-ratio SC stage for efficient and compact voltage conversion, and 2) a multi-phase buck stage for the remainder of the voltage conversion task, output voltage regulation, and soft-charging operation. Note that a distinction of high performance hybrid SC topologies is that the two stages are not independent, but rather have their operation merged [19], [20] to achieve increased performance. The input voltage V_{in} is first stepped down to V_{buck} by the SC stage, where

$$V_{\mathrm{buck}} = \frac{V_{\mathrm{in}}}{K_{\mathrm{SC}}}, \tag{1}$$

and K_{SC} is the SC stage conversion ratio. The buck stage then performs the remaining voltage conversion from V_{buck} to V_{out} and output voltage regulation.

Since the total conversion ratio K_{tot} ($K_{\mathrm{tot}} = V_{\mathrm{in}}/V_{\mathrm{out}}$) is allocated between the SC stage and the buck stage, if the SC stage achieves a larger conversion ratio (K_{SC}), the conversion burden on the buck stage (K_{buck}) can be reduced. At the same output voltage, buck converters with smaller conversion ratios typically require smaller inductors and achieve higher efficiency. Given that magnetic components typically dominate the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden so that the inductor volume of the buck stage can be reduced.

Although it is clear that a larger SC stage conversion ratio

is favorable to the buck stage, there is still a concern that increasing the SC stage conversion ratio can impair overall efficiency since achieving a larger SC stage conversion ratio requires more switching devices and thus can induce higher conduction losses and switching losses. Moreover, higher order SC networks require more flying capacitors, potentially offsetting the inductor volume reduction seen in the buck stage.

This paper aims to establish an analytical framework to analyze and compare the performance of regulated hybrid SC converters for 48-V-to-PoL conversion using two metrics: a) a normalized switch stress as an indicator for efficiency and b) a normalized passive component volume as an indicator for power density. Through a comparative analysis, it is revealed that both metrics decrease as the SC stage conversion ratio increases, which indicates that increasing the SC stage conversion ratio can help achieve both higher efficiency and higher power density.

II. Analytical Framework for Topological Characterization and Comparison

The proposed analytical framework focuses on two metrics of regulated hybrid SC topologies: a) a normalized switch stress M_{S} as an indicator for efficiency and b) a normalized passive component volume M_{P} as an indicator for power density. This section first discusses the key assumptions of this framework, then provides the definitions and derivations of the two metrics, and finally introduces a formalized analytical procedure using topology-dependent characteristic vectors.

A. Key Assumptions

The proposed analytical framework is based on the following assumptions:

- *Small-ripple approximation:* In the analysis of normalized switch stress, capacitor voltage ripples and inductor current ripples are assumed to be negligible.
- *Lossless energy transfer:* Duty ratio is calculated based on the assumption that the converter is lossless.
- *Linear-ripple approximation:* In the analysis of normalized passive component volume, capacitor voltage ripples and inductor current ripples are assumed to be piecewise linear. In other words, capacitor voltage ripples are assumed to be negligible in inductor volume analysis, and inductor current ripples are assumed to be negligible in capacitor volume analysis.
- *Uniform-ripple approximation:* In the analysis of normalized passive component volume, all inductors are assumed to experience the same percentage current ripple (α_{I}), and all flying capacitors are assumed to experience the same percentage voltage ripple (α_{V}).
- *Uniform energy density:* All inductors are assumed to have the same volumetric energy density ($\rho_{\mathrm{E,L}}$). All capacitors are assumed to have the same volumetric energy density ($\rho_{\mathrm{E,C}}$).

The symbols used in this framework are defined in Table I. The symbols with the hat notation $\hat{(\cdot)}$ are normalized values with respect to their base values listed in Table II.

TABLE I: Symbol definitions

Symbol	Definition
N_{S}	Total number of switching devices
N_{L}	Total number of inductors
N_{C}	Total number of flying capacitors
V_{in}	Input voltage (base value for voltage)
V_{buck}	Buck stage input voltage (illustrated in Fig. 1)
V_{out}	Output voltage
I_{out}	Total output current (base value for current)
K_{tot}	Total conversion ratio ($K_{\mathrm{tot}} = V_{\mathrm{in}}/V_{\mathrm{out}}$)
K_{SC}	SC stage conversion ratio ($K_{\mathrm{SC}} = V_{\mathrm{in}}/V_{\mathrm{buck}}$)
K_{buck}	Buck stage conversion ratio ($K_{\mathrm{buck}} = V_{\mathrm{buck}}/V_{\mathrm{out}}$)
$V_{\mathrm{ds},i}$	Peak blocking voltage across switch i
$I_{\mathrm{d(rms)},i}$	RMS value of the current through switch i
$\mathrm{Vol}_{\mathrm{tot}}$	Total passive component volume
$\mathrm{Vol}_{\mathrm{L},j}$	Volume of inductor j
$\mathrm{Vol}_{\mathrm{C},k}$	Volume of capacitor k
L_j	Value of inductor j
$I_{\mathrm{L},j}$	Average current of inductor j
$\Delta i_{\mathrm{L},j,\mathrm{ap}}$	Average-to-peak current ripple of inductor j
$\Delta i_{\mathrm{L},j,\mathrm{pp}}$	Peak-to-peak current ripple of inductor j
T	Switching period of the buck stage
D	Duty ratio of the buck stage
$E_{\mathrm{L},j,\mathrm{peak}}$	Peak energy stored in inductor j
C_k	Value of capacitor k
$V_{\mathrm{C},k}$	Average voltage of capacitor k
$\Delta v_{\mathrm{C},k,\mathrm{ap}}$	Average-to-peak voltage ripple of capacitor k
$\Delta v_{\mathrm{C},k,\mathrm{pp}}$	Peak-to-peak voltage ripple of capacitor k
$q_{\mathrm{C},k}$	Total charge flowing into capacitor k before it is discharged
$E_{\mathrm{C},k,\mathrm{peak}}$	Peak energy stored in capacitor k
α_{I}	Inductor current ripple factor ($\alpha_{\mathrm{I}} = \Delta i_{\mathrm{L},j,\mathrm{ap}}/I_{\mathrm{L},j}$)
α_{V}	Capacitor voltage ripple factor ($\alpha_{\mathrm{V}} = \Delta v_{\mathrm{C},k,\mathrm{ap}}/V_{\mathrm{C},k}$)
$\rho_{\mathrm{E,L}}$	Volumetric energy density of inductors
$\rho_{\mathrm{E,C}}$	Volumetric energy density of flying capacitors
β	Energy density ratio of capacitors to inductors ($\beta = \rho_{\mathrm{E,C}}/\rho_{\mathrm{E,L}}$)

TABLE II: Base values for normalization

Quantity	Voltage	Current	Charge	Volume
Base value	V_{in}	I_{out}	$I_{\mathrm{out}}T$	$\dfrac{V_{\mathrm{out}}I_{\mathrm{out}}T}{\rho_{\mathrm{E,L}}}$

B. Normalized Switch Stress M_{S}

The normalized switch stress M_{S} is defined as the total switch stress normalized to the output power

$$M_{\mathrm{S}} = \frac{\sum\limits_{\text{switches}} V_{\mathrm{ds},i} I_{\mathrm{d(rms)},i}}{V_{\mathrm{out}} I_{\mathrm{out}}} = \underbrace{\frac{V_{\mathrm{in}}}{V_{\mathrm{out}}}}_{K_{\mathrm{tot}}} \cdot \sum_{i=1}^{N_{\mathrm{S}}} \underbrace{\frac{V_{\mathrm{ds},i}}{V_{\mathrm{in}}}}_{\widehat{V}_{\mathrm{ds},i}} \cdot \underbrace{\frac{I_{\mathrm{d(rms)},i}}{I_{\mathrm{out}}}}_{\widehat{I}_{\mathrm{d(rms)},i}}$$

$$= K_{\mathrm{tot}} \sum_{i=1}^{N_{\mathrm{S}}} \widehat{V}_{\mathrm{ds},i} \widehat{I}_{\mathrm{d(rms)},i}. \tag{2}$$

where $V_{\mathrm{ds},i}$ is the peak blocking voltage across switch i when assuming no capacitor voltage ripple, and $I_{\mathrm{d(rms)},i}$ is the RMS value of the current through switch i when assuming no inductor current ripple.

The normalized switch stress M_{S} indicates how much volt-

ampere (VA) stress that the switches in a topology experience when transferring one per-unit watt of power from the input to the output. A lower M_{S} is desirable, as it indicates lower switching losses and lower conduction losses and thus higher efficiency. A lower M_{S} also indicates smaller switch size, which is favorable to higher power density.

C. Normalized Passive Component Volume M_{P}

The normalized passive component volume M_{P} is defined as the total passive component volume normalized to the base volume and is the sum of the normalized inductor volume and the normalized capacitor volume

$$\begin{aligned} M_{\mathrm{P}} &= \frac{\mathrm{Vol}_{\mathrm{tot}}}{\mathrm{Vol}_{\mathrm{base}}} = \frac{\sum\limits_{\text{inductors}} \mathrm{Vol}_{\mathrm{L},j} + \sum\limits_{\text{capacitors}} \mathrm{Vol}_{\mathrm{C},k}}{\mathrm{Vol}_{\mathrm{base}}} \\ &= \sum_{j=1}^{N_{\mathrm{L}}} \widehat{\mathrm{Vol}}_{\mathrm{L},j} + \sum_{k=1}^{N_{\mathrm{C}}} \widehat{\mathrm{Vol}}_{\mathrm{C},k}, \end{aligned} \tag{3}$$

where the base value for volume is

$$\mathrm{Vol}_{\mathrm{base}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}} T}{\rho_{\mathrm{E,L}}}. \tag{4}$$

Parameter $\rho_{\mathrm{E,L}}$ is the volumetric energy density of inductors, and T is the converter switching period. The normalized passive component volume M_{P} indicates the total passive component volume needed to meet the given ripple requirements on the inductor currents and flying capacitor voltages when transferring one per-unit watt of power from the input to the output. A smaller normalized passive component volume is desirable, as it indicates higher power density.

This work adopts an energy-based approach to passive component volume assessment by analyzing the peak energy stored in each passive component [16]. To determine the total passive component volume that a topology requires, this section first finds the minimum inductor and capacitor values that can meet chosen current and voltage ripple requirements and then calculates the peak energy stored in the passive components.

1) Normalized Inductor Volume $\widehat{\mathrm{Vol}}_{\mathrm{L},j}$: Define the average-to-peak current ripple factor of inductor j as

$$\alpha_{\mathrm{I}} = \frac{\Delta i_{\mathrm{L},j,\mathrm{ap}}}{I_{\mathrm{L},j}} = \frac{\Delta i_{\mathrm{L},j,\mathrm{pp}}}{2 I_{\mathrm{L},j}}, \tag{5}$$

where, as annotated in Fig. 2, $I_{\mathrm{L},j}$ is the average inductor current, and $\Delta i_{\mathrm{L},j,\mathrm{ap}}$ and $\Delta i_{\mathrm{L},j,\mathrm{pp}}$ are the average-to-peak and peak-to-peak inductor current ripples, respectively. According to the uniform-ripple approximation, the current ripple factors (α_{I}) of all inductors are assumed to be the same.

By integrating the inductor's current-voltage relation over $t \in [DT, T]$, we can obtain the peak-to-peak inductor current ripple as

$$\Delta i_{\mathrm{L},j,\mathrm{pp}} = \frac{V_{\mathrm{out}}}{L_j} (1 - D) T, \tag{6}$$

where D is the duty ratio of the buck stage. Based on the assumption of lossless energy transfer, D can be calculated as

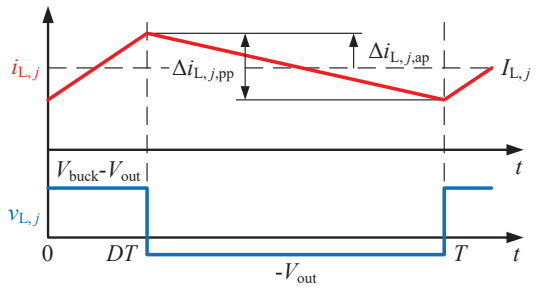

Fig. 2: Current (top, red) and voltage (bottom, blue) waveforms of inductor j (L_j). $I_{\mathrm{L},j}$ is the average current through L_j. $\Delta i_{\mathrm{L},j,\mathrm{ap}}$ and $\Delta i_{\mathrm{L},j,\mathrm{pp}}$ are the average-to-peak and peak-to-peak inductor current ripples, respectively. The inductor voltage jumps between $V_{\mathrm{buck}} - V_{\mathrm{out}}$ and $-V_{\mathrm{out}}$.

$$D = \frac{1}{K_{\mathrm{buck}}} = \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}. \tag{7}$$

We can obtain the minimum inductor value required to meet the chosen current ripple requirement (α_{I}) by substituting (5) and (7) into (6), which yields

$$L_j = \frac{V_{\mathrm{out}} T}{2 \alpha_{\mathrm{I}} I_{\mathrm{L},j}} \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right). \tag{8}$$

Therefore, the peak energy stored in the inductor is

$$\begin{aligned} E_{\mathrm{L},j,\mathrm{peak}} &= \frac{1}{2} L_j (I_{\mathrm{L},j} + \Delta i_{\mathrm{L},j,\mathrm{ap}})^2 \\ &= \frac{1}{2} (1 + \alpha_{\mathrm{I}})^2 L_j {I_{\mathrm{L},j}}^2. \end{aligned} \tag{9}$$

Substituting (8) into (9) yields the required inductor volume

$$\mathrm{Vol}_{\mathrm{L},j} = \frac{E_{\mathrm{L},j,\mathrm{peak}}}{\rho_{\mathrm{E,L}}} = \frac{(1 + \alpha_{\mathrm{I}})^2 V_{\mathrm{out}} I_{\mathrm{L},j} T}{4 \alpha_{\mathrm{I}} \rho_{\mathrm{E,L}}} \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right). \tag{10}$$

Using the base value for volume in (4), we can obtain the normalized inductor volume as

$$\begin{aligned} \widehat{\mathrm{Vol}}_{\mathrm{L},j} &= \frac{\mathrm{Vol}_{\mathrm{L},j}}{\mathrm{Vol}_{\mathrm{base}}} = \frac{(1 + \alpha_{\mathrm{I}})^2}{4 \alpha_{\mathrm{I}}} \cdot \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right) \cdot \underbrace{\frac{I_{\mathrm{L},j}}{I_{\mathrm{out}}}}_{\widehat{I}_{\mathrm{L},j}} \\ &= \frac{(1 + \alpha_{\mathrm{I}})^2}{4 \alpha_{\mathrm{I}}} \left(1 - \frac{K_{\mathrm{SC}}}{K_{\mathrm{tot}}}\right) \widehat{I}_{\mathrm{L},j}. \end{aligned} \tag{11}$$

2) Normalized Capacitor Volume $\widehat{\mathrm{Vol}}_{\mathrm{C},k}$: Define the average-to-peak voltage ripple factor of capacitor k as

$$\alpha_{\mathrm{V}} = \frac{\Delta v_{\mathrm{C},k,\mathrm{ap}}}{V_{\mathrm{C},k}} = \frac{\Delta v_{\mathrm{C},k,\mathrm{pp}}}{2 V_{\mathrm{C},k}}, \tag{12}$$

where, as annotated in Fig. 3, $V_{\mathrm{C},k}$ is the average capacitor voltage, and $\Delta v_{\mathrm{C},k,\mathrm{ap}}$ and $\Delta v_{\mathrm{C},k,\mathrm{pp}}$ are the average-to-peak and peak-to-peak capacitor voltage ripples, respectively. According to the uniform-ripple approximation, the voltage ripple factors (α_{V}) of all capacitors are assumed to be the same.

Illustrated as the shaded area on the capacitor current waveform in Fig. 3, $q_{\mathrm{C},k}$ represents the total charge flowing

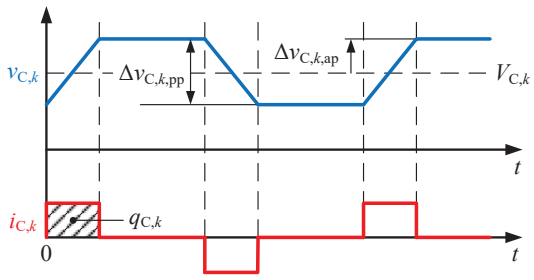

Fig. 3: Voltage (top, blue) and current (bottom, red) waveforms of capacitor k (C_k). $V_{C,k}$ is the average voltage across C_k. $\Delta v_{C,k,ap}$ and $\Delta v_{C,k,pp}$ are the average-to-peak and peak-to-peak capacitor voltage ripples. $q_{C,k}$ is the total charge flowing into capacitor k before it is discharged and is illustrated as the shaded area on the capacitor current waveform. If a capacitor is charged multiple times before discharged, all charges delivered into the capacitor should be added up when calculating $q_{C,k}$.

into capacitor k before it is discharged. The peak-to-peak capacitor voltage ripple can be obtained as

$$\Delta v_{C,k,pp} = \frac{q_{C,k}}{C_k}. \tag{13}$$

We can obtain the minimum capacitor value required to meet the chosen voltage ripple requirement (α_V) by substituting (12) into (13), which yields

$$C_k = \frac{q_{C,k}}{2\alpha_V V_{C,k}}. \tag{14}$$

Thus, the peak energy stored in the capacitor is

$$\begin{aligned} E_{C,k,peak} &= \frac{1}{2} C_k (V_{C,k} + \Delta v_{C,k,ap})^2 \\ &= \frac{1}{2}(1+\alpha_V)^2 C_k {V_{C,k}}^2. \end{aligned} \tag{15}$$

Substituting (14) into (15) yields the capacitor volume

$$\mathrm{Vol}_{C,k} = \frac{E_{C,k,peak}}{\rho_{E,C}} = \frac{(1+\alpha_V)^2 V_{C,k} q_{C,k}}{4\alpha_V \rho_{E,C}}, \tag{16}$$

where $\rho_{E,C}$ is the volumetric energy density of capacitors.

Using the base value for volume in (4), we can obtain the normalized capacitor volume as

$$\begin{aligned} \widehat{\mathrm{Vol}}_{C,k} = \frac{\mathrm{Vol}_{C,k}}{\mathrm{Vol}_{base}} &= \frac{(1+\alpha_V)^2}{4\alpha_V} \cdot \underbrace{\frac{\rho_{E,L}}{\rho_{E,C}}}_{1/\beta} \cdot \underbrace{\frac{V_{in}}{V_{out}}}_{K_{tot}} \cdot \underbrace{\frac{V_{C,k}}{V_{in}}}_{\widehat{V}_{C,k}} \cdot \underbrace{\frac{q_{C,k}}{I_{out}T}}_{\widehat{q}_{C,k}} \\ &= \frac{(1+\alpha_V)^2}{4\alpha_V \beta} K_{tot} \widehat{V}_{C,k} \widehat{q}_{C,k}, \end{aligned} \tag{17}$$

where β is the ratio of the energy density of capacitors to that of inductors

$$\beta = \frac{\rho_{E,C}}{\rho_{E,L}}. \tag{18}$$

3) Normalized Passive Component Volume M_P: Summing the normalized volumes over all inductors and capacitors by substituting (11) and (17) into (3) yields

$$\begin{aligned} M_P = &\sum_{j=1}^{N_L} \frac{(1+\alpha_I)^2}{4\alpha_I} \left(1 - \frac{K_{SC}}{K_{tot}}\right) \widehat{I}_{L,j} \\ &+ \sum_{k=1}^{N_C} \frac{(1+\alpha_V)^2}{4\alpha_V \beta} K_{tot} \widehat{V}_{C,k} \widehat{q}_{C,k}. \end{aligned} \tag{19}$$

Applying Kirchhoff's current law (KCL), we can obtain

$$\sum_{j=1}^{N_L} \widehat{I}_{L,j} = \frac{1}{I_{out}} \sum_{j=1}^{N_L} I_{L,j} = 1, \tag{20}$$

which can be used to simplify (19) as

$$\begin{aligned} M_P = &\frac{(1+\alpha_I)^2}{4\alpha_I} \left(1 - \frac{K_{SC}}{K_{tot}}\right) \\ &+ \frac{(1+\alpha_V)^2}{4\alpha_V \beta} K_{tot} \sum_{k=1}^{N_C} \widehat{V}_{C,k} \widehat{q}_{C,k}. \end{aligned} \tag{21}$$

D. Formalized Analysis Procedure

According to (2) and (21), the following topology-dependent characteristic parameters are needed to calculate the normalized metrics M_S and M_P: $\widehat{V}_{ds,i}$, $\widehat{I}_{d(rms),i}$, $\widehat{V}_{C,k}$, and $\widehat{q}_{C,k}$. To formalize the analytical procedure, we define four topology-dependent characteristic vectors:

- Switch voltage stress vector $\widehat{\mathbf{V}}_{ds} = \left(\widehat{V}_{ds,i}\right)_{1 \leqslant i \leqslant N_S}$
- Switch current stress vector $\widehat{\mathbf{I}}_{d(rms)} = \left(\widehat{I}_{d(rms),i}\right)_{1 \leqslant i \leqslant N_S}$
- Capacitor voltage vector $\widehat{\mathbf{V}}_C = \left(\widehat{V}_C\right)_{1 \leqslant i \leqslant N_C}$
- Capacitor charge vector $\widehat{\mathbf{q}}_C = \left(\widehat{q}_{C,k}\right)_{1 \leqslant i \leqslant N_C}$

with which we can rearrange (2) and (21) as

$$M_S = K_{tot} \widehat{\mathbf{V}}_{ds}^\top \widehat{\mathbf{I}}_{d(rms)}, \tag{22}$$

and

$$M_P = M_{P,L} + M_{P,C}, \tag{23}$$

where $M_{P,L}$ is the normalized inductor volume

$$M_{P,L} = \frac{(1+\alpha_I)^2}{4\alpha_I} \left(1 - \frac{K_{SC}}{K_{tot}}\right), \tag{24}$$

and $M_{P,C}$ is the normalized capacitor volume

$$M_{P,C} = \frac{(1+\alpha_V)^2}{4\alpha_V \beta} K_{tot} \widehat{\mathbf{V}}_C^\top \widehat{\mathbf{q}}_C, \tag{25}$$

in which $\cdot^\top$ denotes the transpose of a vector.

Equations (22) and (23) provide a formalized analytical procedure of M_S and M_P that can be automated. Equations (24) and (25) reveal two properties of $M_{P,L}$ and $M_{P,C}$:

- As the SC stage conversion ratio K_{SC} increases, the normalized inductor volume $M_{P,L}$ decreases and the normalized capacitor volume $M_{P,C}$ increases, which is

TABLE III: Topological comparison of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion

Year	Topology	SC Stage Conversion Ratio (K_{SC})	Buck Stage Conversion Ratio (K_{buck})	Buck Stage Duty Ratio (D)	Normalized Switch Stress (M_{S})	Normalized Passive Component Volume* (M_{P})	Complete Soft-Charging
2005	Series-capacitor buck with multi-phase operation [1]	2:1	24:1	0.042	31.6	2.14	Yes
2011	Series-capacitor buck with two-phase operation [2]	4:1	12:1	0.083	18.7	2.10	Yes
2020	Crossed-coupled QSD buck [3]	4:1	12:1	0.083	24.2	2.08	Yes
2020	DIH** [4]	6:1	8:1	0.125	14.7	2.40	Yes, with split-phase control
2021	CaSP [5]	6:1	8:1	0.125	23.5	2.02	Yes
2022 2023	LEGO† [6] Mini-LEGO† [7]	6:1	8:1	0.125	17.6	2.41	No
2023	SDIH** [8]	6:1	8:1	0.125	14.7	2.40	Yes, with split-phase control
2022	MLB [9]	8:1	6:1	0.167	23.7	2.03	Yes
2022	VIB‡ [10]	8:1	6:1	0.167	14.3	2.07	No
2023	MSC [11]	8:1	6:1	0.167	15.1	1.95	Yes
2022	Dickson^2 [12]	9:1	5.33:1	0.188	14.8	1.90	Yes
2023	16-to-1 switching bus converter (SBC) [13]	16:1	3:1	0.333	10.2	1.69	Yes
2023	20-to-1 switching bus converter (SBC) [14]	20:1	2.4:1	0.417	8.99	1.56	Yes

* The normalized passive component volume M_{P} is calculated under the following conditions: $\alpha_{\mathrm{I}} = 15\%$, $\alpha_{\mathrm{V}} = 5\%$, $\beta = 100$.

** In [4] and [8], all flying capacitor voltage ripples are designed to be the same, which enables simple split-phase control timing. Since the average voltages across different flying capacitors are different, the voltage ripple factors of different flying capacitors in these two works are not uniform. Nevertheless, the normalized passive component volume M_{P} listed in this table assumes uniform voltage ripple factors for all flying capacitors, which requires more complex split-phase control timing.

† Small filter capacitors $\mathrm{C_{filter}}$ are not taken into account in the capacitor volume analysis, although they are used in the hardware prototype in [6] and [7] to filter the high-frequency pulsating current from the buck stage. Additionally, the charge sharing loss between the filter capacitors and the flying capacitors is not captured in this analysis.

‡ In addition to flying capacitors, an intermediate bus capacitor $\mathrm{C_{IB}}$ is included in capacitor volume calculation as well. As mentioned in [10], its value is chosen to be $C_{\mathrm{IB}} = C_{\mathrm{F}}/2.34$, where C_{F} is the charge pump capacitance. The normalized voltage stress on $\mathrm{C_{IB}}$ is $1/2$. The charge sharing loss between the intermediate bus capacitor and the flying capacitors is not captured in this analysis.

intuitive since increasing K_{SC} means shifting more conversion burden from the buck stage to the SC stage.

- Topologies with the same SC stage conversion ratio K_{SC} have the same normalized inductor volume $M_{\mathrm{P,L}}$, since the only topology-independent parameter in (24) is K_{SC}, and K_{tot}, α_{I}, α_{V} and β are all constants. Therefore, the difference in the normalized passive component volume M_{P} among different topologies with the same K_{SC} comes from the difference in the normalized capacitor volume $M_{\mathrm{P,C}}$.

These two properties will be used in the comparative analysis in Section III-C.

III. Comparative Performance Analysis of 48-V-to-1-V Regulated Hybrid SC Topologies

Based on the analytical framework established in Section II, this section performs a comparative analysis of state-of-the-art 48-V-to-1-V hybrid SC topologies to demonstrate the benefits of a larger SC stage conversion ratio.

A. Performance Comparison

Table III summarizes the key characteristics and the two normalized metrics of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. To better visualize the influence of the SC stage conversion ratio on the two normalized metrics, Figs. 4 and 5 plot the normalized switch stress M_{S} and the normalized passive component volume M_{P} of different topologies versus their SC stage conversion ratio K_{SC}. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. Some extendable topologies are plotted with dashed curves connecting different possible implementations at different SC stage conversion ratios. As shown in Figs. 4 and 5, with a larger SC stage conversion ratio K_{SC}, the buck stage duty ratio D can be extended.

B. Analysis of the Normalized Switch Stress M_{S}

The series-capacitor-buck (SCB) topology was first proposed in [1] with multi-phase operation and then extended

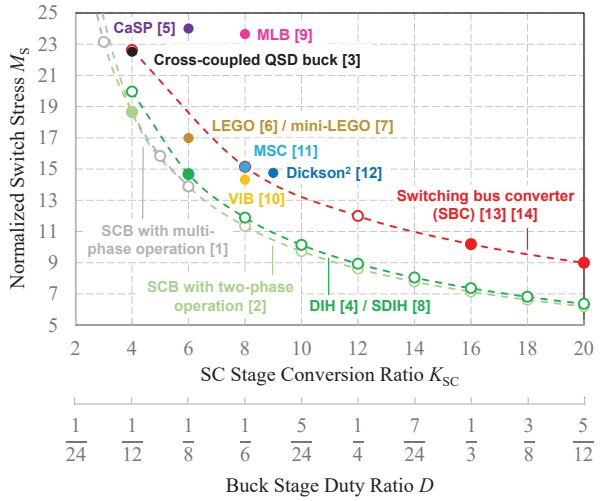

Fig. 4: Normalized switch stress M_S of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A lower normalized switch stress M_S is more desirable.

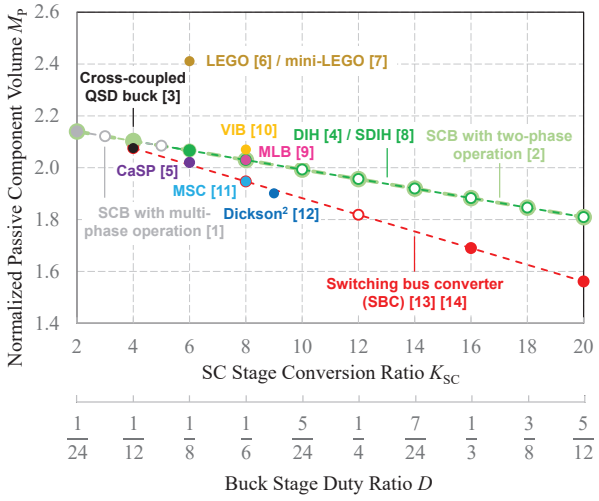

Fig. 5: Normalized passive component volume M_P of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion ($\alpha_I = 15\%$, $\alpha_V = 5\%$, $\beta = 100$). Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A smaller normalized passive component volume M_P is more desirable.

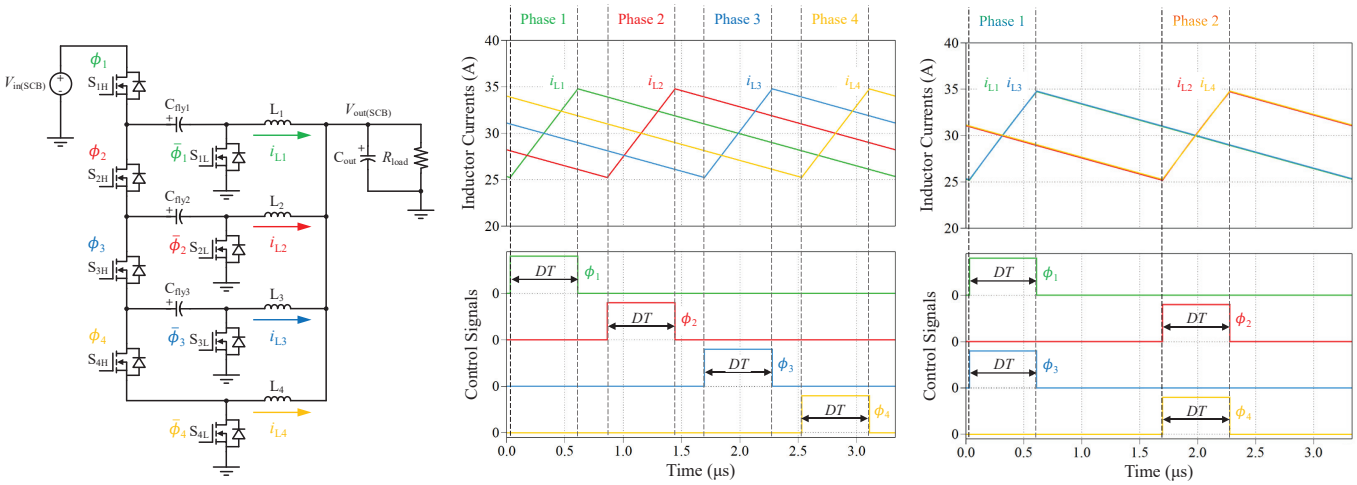

Fig. 6: Four-branch series-capacitor-buck (SCB) converter. (a) Schematic drawing. (b) Multi-phase operation. (c) Two-phase operation.

in [2] with two-phase operation. Fig. 6 shows a four-phase SCB converter as an example. In multi-phase operation illustrated in Fig. 6(b), each inductor operates in an individual phase; in two-phase operation illustrated in Fig. 6(c), the inductors are grouped together into two phases with a 180° phase shift. Compared to two-phase operation, multi-phase operation can achieve a smaller net output current ripple through multi-phase interleaving. However, two-phase operation can extend the maximum duty ratio from $\frac{1}{N}$ to $\frac{1}{2}$, where N is the number of branches in a SCB converter. As a result, the upper limit on the number of branches (N_{m-ph} and N_{2-ph}) can be increased:

$$\text{Multi-phase operation: } N_{m-ph} < \sqrt{\frac{V_{in(SCB)}}{V_{out(SCB)}}} \tag{26}$$

$$\text{Two-phase operation: } N_{2-ph} < \frac{V_{in(SCB)}}{2V_{out(SCB)}}, \tag{27}$$

where $V_{in(SCB)}$ and $V_{out(SCB)}$ are the input and output voltages of the SCB converter, respectively. For 48-V-to-1-V conversion ($V_{in(SCB)} = 48$ V and $V_{out(SCB)} = 1.0$ V), the maximum allowable numbers of SCB branches for multi-phase operation and two-phase operation are $N_{m-ph(max)} = 6$ and $N_{2-ph(max)} = 20$, respectively. Since the SC stage conversion ratio K_{SC} of a SCB converter is equal to its number of branches N, the maximum SC stage conversion ratio for multi-phase operation and two-phase operation are $K_{SC,m-ph(max)} = 6$ and $K_{SC,2-ph(max)} = 20$, respectively. As the SC stage conversion ratio K_{SC} increases, the voltage stress on the switches decreases while the current stress on most of the switches increases. Nevertheless, the increase in

switch current stress is not able to offset the voltage stress reduction. Therefore, as shown in Fig. 4, the net result is that the normalized switch stress of a SCB topology decreases as K_{SC} increases. This means that a SCB converter with a larger SC stage conversion ratio has the theoretical potential of achieving higher efficiency. Compared to multi-phase operation, two-phase operation can extend the upper limit on the number of branches and thus better leverage the benefit of a larger SC stage conversion ratio.

The DIH [4] and SDIH [8] topologies can be viewed as the SCB topology in two-phase operation but with the inductors in the same phase connected in parallel and merged into one inductor. Combining multiple small inductors into one large inductor can typically improve the overall performance of magnetic components [21]. However, shorting the switch nodes in the same phase brings about hard-charging of flying capacitors that can only be overcome by split-phase control [22]. The additional secondary phases inserted by the split-phase control reduces the effective duty ratio, leading to slightly higher normalized switch stress compared to a SCB topology in two-phase operation, which is captured in Fig. 4. Given that the timing of split-phase control is sensitive to component sizing, either capacitors with high stability (e.g., Class I multilayer ceramic capacitors [MLCCs]) or active split-phase control [23] must be used to ensure complete soft-charging.

The switching bus converter (SBC) [13], [14] can be viewed as a 2-to-1 SC front-end merged with two SCB modules through two switching buses with redundant switches removed. Each submodule operates in the two-phase fashion and therefore can extend the maximum duty ratio and enable a larger SC stage duty ratio. As can be seen in Fig. 4, the normalized switch stress of the switching bus converter decreases as the SC stage conversion ratio increases, which shows the benefit of a larger SC stage conversion ratio. As discussed in [13], [14], the switching-bus-based architecture ensures complete soft-charging and therefore split-phase control is not needed. Other switching-bus-based topologies include MLB [9], CaSP [5] and Dickson^2 [12] topologies.

C. Analysis of the Normalized Passive Component Volume M_{P}

Fig. 5 shows the normalized passive component volume M_{P} of different topologies versus their SC stage conversion ratio K_{SC} assuming inductor ripple factor $\alpha_{\mathrm{I}} = 15\%$, capacitor voltage ripple factor $\alpha_{\mathrm{V}} = 5\%$, and energy density ratio of capacitors to inductors $\beta = 100$. As can be seen in Fig. 5, in general, the normalized passive component volume M_{P} of these regulated hybrid SC topologies decreases as their SC stage conversion ratio K_{SC} increases. Recall the first property of the normalized inductor volume $M_{\mathrm{P,L}}$ and the normalized capacitor volume $M_{\mathrm{P,C}}$ mentioned at the end of Section II-D: with a larger K_{SC}, $M_{\mathrm{P,L}}$ decreases and $M_{\mathrm{P,C}}$ increases. This is because as K_{SC} increases, more conversion burden is shifted from the buck stage to the SC stage, and therefore the normalized inductor volume decreases and the normalized capacitor volume increases. However, since capacitors have much higher volumetric energy density than inductors [15], the increase in capacitor volume will not be able to offset the inductor volume reduction. As a result, the total passive component volume goes down when the SC stage conversion ratio increases. This is the reason why increasing the SC stage conversion ratio can help reduce the normalize passive component volume and improve power density.

As shown in Fig. 5, the switching bus converter (SBC) requires a smaller passive component volume compared to series-capacitor buck (SCB), DIH, and SDIH topologies at the same SC stage conversion ratio. Recall the second property of $M_{\mathrm{P,L}}$ and $M_{\mathrm{P,C}}$: topologies with the same SC stage conversion ratio have the same normalized inductor volume. Therefore, at the same SC stage conversion ratio, the difference in the normalized passive component volume among different topologies comes from the difference in the normalized capacitor volume. In SCB, DIH, and SDIH topologies, the flying capacitor voltages are $\frac{k}{K_{\mathrm{SC}}}V_{\mathrm{in}}$ $(k = 1, 2, \cdots, K_{\mathrm{SC}}-1)$, with half of the capacitor voltages above $\frac{1}{2}V_{\mathrm{in}}$. In contrast, the flying capacitor voltages in the switching bus converter are $\frac{1}{2}V_{\mathrm{in}}$ and $\frac{k}{K_{\mathrm{SC}}}V_{\mathrm{in}}$ $(k = 1, 2, \cdots, K_{\mathrm{SC}}/2 - 1)$, with all capacitor voltages less than or equal to $\frac{1}{2}V_{\mathrm{in}}$. As a result, the switching bus converter requires less capacitive energy storage, smaller normalized capacitor volume, and thus smaller normalized passive component volume.

In summary, this comparative performance analysis reveals that with a larger SC stage conversion ratio, both the normalized switch stress and the normalized passive component volume of a regulated hybrid SC converter can be reduced. This indicates that increasing the SC stage conversion ratio can improve both the efficiency and power density of a regulated hybrid SC converter.

IV. Conclusion

In this paper, an analytical framework is established for topological characterization and performance comparison among different regulated hybrid SC topologies for direct 48-V-to-PoL conversion. The proposed framework focuses on two metrics: a) a normalized switch stress as an indicator for efficiency and b) a normalized passive component volume as an indicator for power density. Through a comparative analysis of state-of-the-art 48-V-to-1-V regulated hybrid SC topologies, it is revealed that a larger SC stage conversion ratio can help reduce both metrics, indicating both higher efficiency and higher power density can be achieved by increasing the SC stage conversion ratio.

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