UNIVERSITY OF CALIFORNIA SAN DIEGO

140 GHz 8x8 Wafer-Scale On-Grid Transmit-Receive Array in 45RFSOI with 24 Gbps Links and 8-30 GHz High-Linearity Harmonic Rejection Mixers

A dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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The Dissertation of Amr Ahmed is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2023

DEDICATION

To my Grandmother, Mother, Father, Grandfather and Wife

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Chapter 2, in full, has been submitted for publication of the material as it may appear in: A. Ahmed, L. Li, M. Jung, S. Li, D. Baltimas and G. M. Rebeiz, "140 GHz 2D Scalable On Grid 8x8 Element Transmit Receive Phased Arrays with Up/Down Converters Demonstrating 5.2m Link and Beyond," *IEEE Trans. Microw. Theory Techn.* and A. Ahmed, L. Li, M. Jung and G. M. Rebeiz, "A 140 GHz FMCW Imaging System Utilizing 8x8 Transmit-Receive Phased Arrays with Integrated x6 LO Multipliers," *IEEE IMS*. The dissertation author was the primary investigator and author of these materials.

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A. Ahmed, L. Li, M. Jung, S. Li, D. Baltimas and G. M. Rebeiz, "140 GHz 2D Scalable On Grid 8x8 Element Transmit Receive Phased Arrays with Up/Down Converters Demonstrating 5.2m Link and Beyond," *IEEE Trans. Microw. Theory Techn.*, under review .

A. Ahmed and G. M. Rebeiz, "A 8–30 GHz Passive Harmonic Rejection Mixer with 8 GHz Instantaneous IF Bandwidth in 45RFSOI," *IEEE Trans. Microw. Theory Techn.*, under review.

A. Ahmed, L. Li, M. Jung and G. M. Rebeiz, "A 140 GHz FMCW Imaging System Utilizing 8x8 Transmit-Receive Phased Arrays with Integrated x6 LO Multipliers" *IEEE IMS*, in preparation.

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ABSTRACT OF THE DISSERTATION

140 GHz 8x8 Wafer-Scale On-Grid Transmit-Receive Array in 45RFSOI with 24 Gbps Links and 8-30 GHz High-Linearity Harmonic Rejection Mixers

by

Amr Ahmed

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2023

Professor Gabriel M. Rebeiz, Chair

Recent increase in demand for low latency and high data rate wireless links was the drive for the rapid advancement in >100-GHz millimeter-wave systems especially D-band (110-170 GHz) communication links. Thanks to the wide, available, unused, and unallocated spectrum (up to 60 GHz), emerging applications such as virtual/augmented reality (VR/AR), high speed backhaul communication and the Internet of Things (IoT) now have greater opportunities. The first contribution of this thesis is the development of the world's first 140 GHz 64-element fully 2D scalable wafer-scale transmit-receive phased array in CMOS technology.

The 8x8 array grid size is maintained close to (or equal) $\lambda/2$ at 140 GHz in both x- and

y-directions, hence achieving a wide electronic scanning angle of up to 60°. The measured peak effective isotropic radiated power (EIRP) of the TX array is 34-37.5 dBm at 137.5-145 GHz which is the highested reported EIRP so far for silicon technologies. The RX operation input 1-dB compression point (P1dB) of -12 to -9 dBm is measured at 134-143 GHz. Communication link measured for both TX and RX operations supports modulated 16-/64- quadrature amplitude modulation (QAM) signals with up to 24Gb/s data rates with an rms EVM less than 7%/6% respectively.

The second contribution of this thesis is the development of a harmonic rejection mixer (HRM) operating in the frequency range 8-30 GHz. The mixer is an 8-phase mixer rejecting up to the 5th harmonic of the LO with a measured harmonic rejection ratio of 27-45 dBc. The input 1-dB compression point of the mixer is measured to be 4.2-7 dBm across the frequency range with an IF bandwidth of up to 8 GHz.

Chapter 1

Introduction

1.1 140 GHz Wireless Systems

D-band wireless communication systems (110-170 GHz) can be a key to fulfill the increasing demand on low latency and high data rate links; thanks to the wide available unallocated frequency spectrum of up to 60 GHz. Hence, D-band wireless systems have been an emerging topic recently in industry and academia [1]. The potential for high frequency bands (above 95 GHz) is also emphasized by the move of the Federal Communication Commission (FCC) to open spectrum above 95 GHz which might lead to beyond 5G and 6G [1]–[4].

In addition, with increased advancement in technology scaling, wireless systems at 140 GHz can be realized using low cost silicon technologies, such as SiGe and CMOS. Such technologies achieves f_t and f_{max} values of more than 300 GHz, meaning that the transistor pairs can realize some intrinsic gain and reasonable performance at 140 GHz.

However, at such high frequency, free space loss factor (FSLF) is very high. Comparing wireless link at 6 GHz and 140 GHz, the SLF at 140 GHz is around 27 dB higher than that at 6 GHz. Meaning that for the same wireless link distance, bandwidth and radiated power, the 140 GHz link would have much lower SNR for the same modulated signal. This results in the degraded bit error rate performance (higher BER) and limited datarate according to Shannon theory [5].

In order to address the high SLF at 140 GHz, it is mandatory to implement phased-array

systems for both the transmiter (TX) and receiver (RX). With N number of elements at the TX and RX sides, the link budget can be improved by up to 30log(N). This is due to the gain in the total effective isotropic radiated power (EIRP) of the TX by 20log(N) because of the power addition of each elements in addition to the array directivety. In addition, SNR improvement in the RX side of 10log(N) due to the coherent addition of the signal and incoherent addition of the noise.

Such phased-array systems can be implemented using several options (Fig. 1.1). First, digital beamforming architecture (Fig. 1.1 (a)) where each channel has its own ADC / DAC and signal phase shifting and addition is processed in the digital domain. This provides the highest flexibility in terms of beamforming and the ability to generate different beams at the same time. However, for large modulation bandwidth and large array, this implementation would consume huge amount of power due to the need of high performance ADC/DAC at each element.

Second and third options for phased-array architectures would be IF and LO beamformings. The IF beamfroming has the phase shifter and variable gain amplifiers at the IF frequency, hence achieving low rms phase and gain errors and, hence, more accurate beamforming. For both LO and IF beamfroming architectures, a mixer is needed in each channel along with LO distribution to all channels. This results in a higher power consumption for the LO network. Furthermore, and more importantly, the each channel will occupy more areah due to the presence of lower frequency circuits at each channel. At 140 GHz, this would limit the achievable grid size to be more than $\lambda/2$ if one or both X and Y planes. Hence, full 2-D scalability would not be feasible.

The final and most suitable options at D-band is the RF beamforming architecture (Fig. 1.1 (d)). Using this option, since all circuits are at RF frequency, hence, each channel size can be squeezed to be equal (or close to) $\lambda/2$. Therefore, achieving full 2-D scalable arrays in addition to achieving wide scanning angles up to 60^o.

In summary, the challenges for 140 GHz TRX systems are as follows: first, achieving full 2-D scalabity. Second, implement grid size close to or equal $\lambda/2$. Third, achieve wide scan

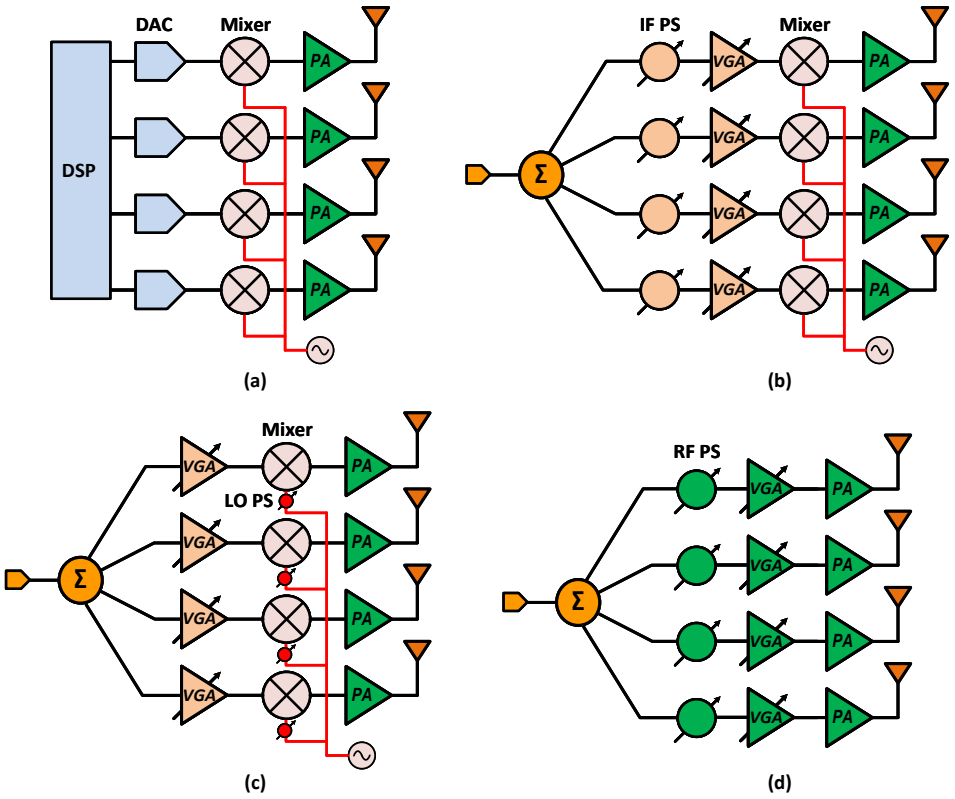


Figure 1.1. Phased-arrays architecture beamforming options (a) Digital, (b) IF, (c) LO and (d) RF.

range both in elevation and azimuthal planes. Fourth, reach high EIRP values and high data rates. Finally, build the system with a low cost (chip technology and packaging). This thesis addresses these challenges.

1.2 Wide-band Harmonic Rejection Mixing

Wideband receiver systems allows for faster time to market products and ease of use in several products. Furthermore, wideband systems can be used in several prototypes, hence, saving development cost and time. Unfortunately, such systems face several challenges. Firstly, in-band and out-of-band blockers will produce intermodulation products that might fall in signal band and degrade the desired signal SNR. Secondly, far-away blockers falling close to the harmonic frequencies of the local oscillator (LO) will mix down on top of the desired signal and,

therefore, corrupting the desired signal.

Therefore, it is mandatory for wide-band systems to have highly linear mixers to reduce any intermodulation products. In addition, LO harmonic operation is mandatory to reject the mixing down of blockers around the LO frequency.

1.3 Thesis Overview

This thesis has two main contribution, first in wide band mixing and second in high data rate D-band arrays.

Chapter 2 presents a scalable wafer-scale transmit-receive phased array at 140 GHz. The chip is composed of 2-D 8x8 140 GHz channels employing radio-frequency (RF) beamforming with 4-bit phase and gain controls at 135-145 GHz. An up/down-converter (UDC) channel with a x6 LO chain and an IF of 9-14 GHz is also integrated on the chip. The on-chip RF distribution network is composed of Wilkinson divider/combiner networks, along with line amplifiers (LAs) to provide signal amplification. The chip is fabricated in GlobalFoundries CMOS 45RFSOI technology with an area of 9.84*8.27 mm2 and is flipped on a low-cost organic RF PCB containing 8x8 patch antenna array placed at 1.07x1.22 mm grid (0.5λ x 0.57λ at 140 GHz). The array can scan $\pm 60^{o}$ for both transmit and receive operations. The measured TX EIRP is 37.5 dBm at 140 GHz. The measured RX array input 1-dB compression point is -11 dBm with an electronic gain of 20 dB at 140 GHz. The array supports 16/64 QAM operation with up to 24 Gb/s for both transmit and receive operations. This work presents the first phased-array at 140 GHz with wide-angle scanning and full scalability in the X and Y directions.

Chapter 3 presents a passive harmonic rejection mixer which employs resistive scaling to maintain high linearity and to achieve 3^{rd} and 5^{th} harmonic rejection. The 8-phase 50% duty-cycle clocks are generated using polyphase filters without any clock dividers, and isolation between the 4 mixers is achieved using a Wilkinson network in the RF path. This enables the mixer to operate at mm-wave frequencies with wide instantaneous bandwidth, and greatly

reduces the LO power consumption due to the much lower operating frequency of the LO network. The mixer is fabricated in the GlobalFoundries CMOS 45RFSOI process and has a measured conversion loss of 12 dB with a 3-dB bandwidth of 8-30 GHz, and an IF instantaneous bandwidth of up to 8 GHz. The measured harmonic rejection ratio (HRR) at the 2^{nd}, 3^{rd} and 5^{th} harmonics is better than 27 dBc across the entire bandwidth. An input P1dB of 4.2-7 dBm is achieved at 8-30 GHz due to the passive architecture. Application areas are in high linearity high-IF mm-wave 5G systems and wideband receivers.

Chapter 4 concludes this thesis, gives a summary of the presented projects, and discusses potential future works.

Chapter 2

140 GHz 2D Scalable On-Grid 8x8-Element Transmit-Receive Phased-Arrays with Up/Down Converters Demonstrating 5.2 Meter Link and Beyond

2.1 Introduction

Recent increase in demand for low latency and high data rate wireless links was the drive for the rapid advancement in >100-GHz millimeter-wave systems [1]–[3], [6]–[25], especially D-band (110-170 GHz) communication links. Thanks to the wide, available, unused, and unallocated spectrum (up to 60 GHz), emerging applications such as virtual/augmented reality (VR/AR), high speed backhaul communication and the Internet of Things (IoT) now have greater opportunities. However, the high space loss factor (SLF) at such high communication frequencies necessitates higher radiated TX power and higher TX and RX antenna gains in order to allow for longer communication distances. In addition, for better system scalability, integration level and cost, advanced CMOS processes are preferred. Furthermore, the communication link needs to be maintained over a wide angular region. This leads to the use and implementation of phased-array systems for both the transmit and receive operations at D-band.

Several phased-array architectures are proposed and used at RF and low mmWave frequencies including IF, RF, LO and digital beamforming architectures. At D-band, especially

with lager bandwidth and large number of elements, digital beamforming would consume very high power due to the high sampling rate and bandwidth of the analog-to-digital converters (ADCs) and the I/Q local-oscillator (LO) paths at each channel. Hence, a full digital beamforming architecture is very challenging for large 2-D arrays. Similarly, LO beamforming consumes large power consumption in the LO path at each channel. On the other side, IF and RF beamforming architectures are suitable for D-band phased arrays. The IF beamforming architecture has been demonstrated in [3], [8], [10] and has the advantage of better phase and gain errors in the phase shifters designed at IF frequency. However, this comes at the cost of necessitating to have IF circuits (amplifier, phase shifter and mixer) present on each channel. Which in turns makes the area occupied by each channel to be large when compared to the very short wavelength of 2mm in the D-band frequency range. Therefore, IF beamforming architectures can be designed with good performance but only scalable in one direction (2xN scalability). This leads to lower electronic scanning range and larger grating lobes. The RF beamforming architecture on the other side has the advantage being able to squeeze the channel area and place all the channels on a 0.5-0.6λ grid size allowing for full 2-D scalability and up to 60^o electronic scanning. In this work, RF-beam forming architecture is adopted as a promising solution for fully scalable 140-GHz phased arrays.

Several chip packaging and antenna solutions have been developed in D-band communication. For example, glass interposer technology is used in [7] but at a relatively high cost. In addition, chip antenna feeding, and quartz superstrate antennas have been demonstrated in [3], [8] showing high efficiency transitions but is limited for scalability. A high efficiency laminate (interposer) antenna is adopted in this work allowing for full scalability and low-cost designs.

This chapter presents an 8x8 2-D scalable 140-GHz transmit-receive phased array based on RF beamforming and using low-cost laminate [6]. Section 2.2 presents the wafer-scale chip block diagram and system architecture. Section 2.3 presents some key circuit implementations for the TRX channel. Section 2.4 presents the UDC channel layout and simulated performance. Section V shows the details of the distribution network. Section 2.6 details the systems analysis

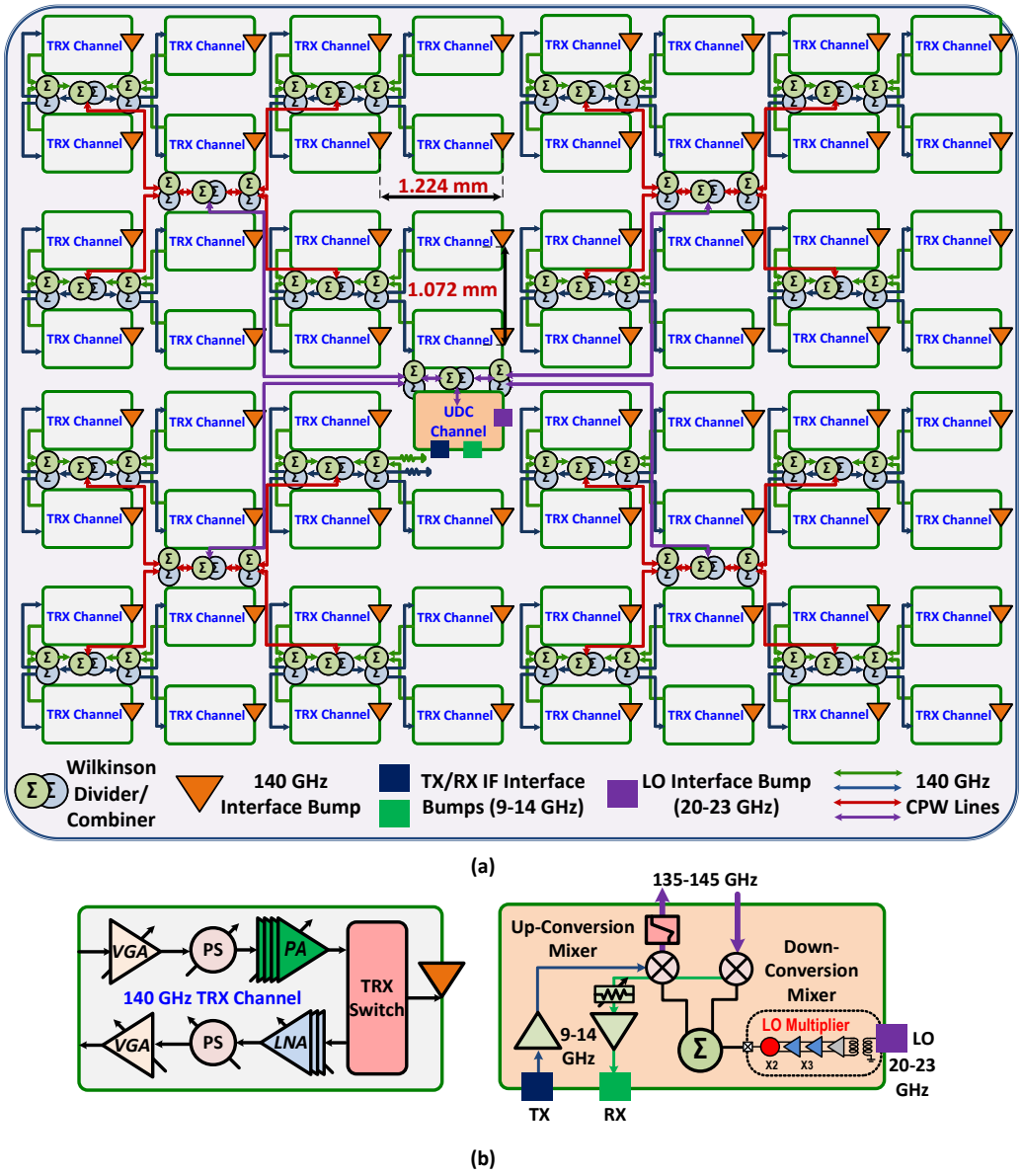


Figure 2.1. (a) Simplified block diagram of the 2D 140 GHz 8x8 transmit-receive array with up/down converter to IF, (b) TRX and UDC channels' details.

for both TX and RX operations. Section 2.7 shows the details of the antennas. Section 2.8 shows the chip micrograph and packaging. Section 2.9 presented the measurement results for each of the TX and RX operations. Section 2.10 shows a demonstration of TX to RX communication link results and analysis. Finally, section 2.12 concludes this work.

2.2 Wafer-Scale RF Beamforming Phased Array Tranmit-Receive Architecture

Wafer-scale phased-arrays incorporate all the RF circuits (front ends, up/down converters, and distribution networks) in a single chip, hence, reducing RF transitions in and out of the chip resulting in a lower power and more efficient systems, especially at frequencies above 100 GHz. This has been demonstrated before at V-band [26], W-band [27], [28] and D-band [3], [8], [10].

Fig. 2.1(a) shows the block diagram of the wafer-scale RF beamforming transmit-receive chip. It is composed of 8x8 RF transmit-receive channels, RF distribution network and a UDC channel. Each RF channel (Fig. 2.1(b)) has a power amplifier (PA), phase shifter (PS) and variable gain amplifier (VGA) in the transmit path and low noise amplifier (LNA), PS and VGA in the receive path. Each path has a total of 4-bit gain and phase controls. A λ/4-based SPDT switch is deigned at the antenna port in order to switch between the TX and RX operations. The UDC channel (Fig. 2.1(b)) is the interface between the off chip IF signals at 9-14 GHz and on chip RF signals at 135-145 GHz. It is composed of IF amplifier, up-conversion (UC) mixer and image rejection (IR) notch filter in the transmit path and down-conversion (DC) mixer, passive attenuator and IF amplifier in the receive path. The LO input to the UDC channel is at 20-23 GHz, this is multiplied by an on-chip x6 frequency multiplier circuit and then split between the UC and DC mixers using Wilkinson divider.

The chip is designed and fabricated in GlobalFoundries 45RFSOI technology. The 40-nm floating body CMOS-SOI transistor is used for all RF/LO/IF circuit design with f_t and f_{max} of 193 and 297 GHz (modeled to the top metal) at bias current density (J_{dc}) of 0.17 mA/μm. The power amplifier transistors are biased in class-A at Jdc of 0.33 mA/μm with f_t and f_{max} of 350 and 270 GHz.

The chip is placed on a grid size of 1.07mm*1.22mm (0.5λ*0.57λ at 140 GHz) and is flipped on a standard commercial organic laminate interposer with ε_r of 3.2 and tanδ of 0.002 (equivalent to Panasonic Megtron 7). This is the same material used at 28 GHz or 60 GHz for

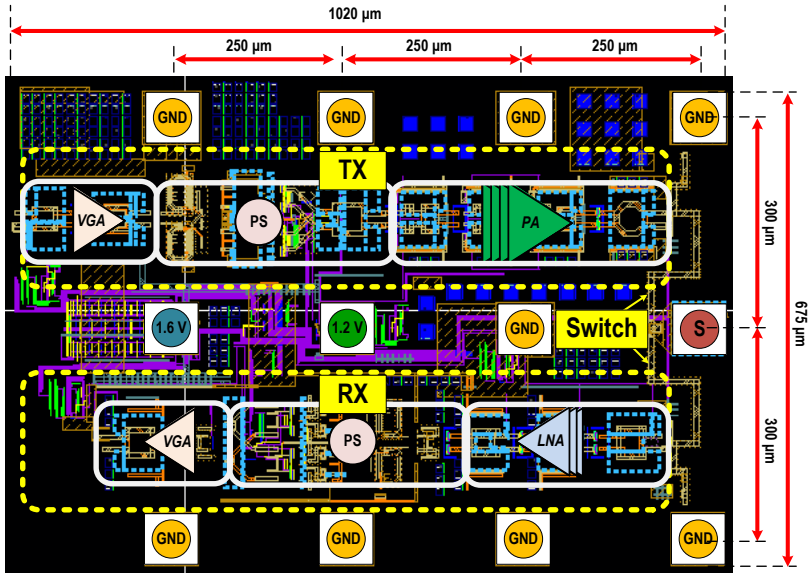


Figure 2.2. TRX channel layout details.

high volume applications and greatly reduces the cost of the D-band phased-array. A stacked probe-fed stub-coupled microstrip antenna array is designed on M10 layer of the PCB with the same grid size as the chip. Details and simulations of the antenna and packaging are shown in section 2.7.

2.3 TRX Channel Building Blocks

The channel layout is presented in Fig. 2.2 showing all RF building blocks. Each channel has several ground pads/bumps (up to 9) in order to reduce the ground (GND) inductance and improve isolation between channels. The 140 GHz signal pad has three surrounding GND pads to improve antenna feed isolation and performance. The spacing between the RF pad and GND pads is 250μm in the x-direction and 300μm in the y-direction. The antenna design considers the GND spacing, pad capacitance and bump inductance as will be shown in section 2.7. The TRX channel has two supply domains; 1.2V supply for PA, LNA and VGAs, and 1.6V supply for the PS. Each channel has one pad per supply in order to reduce the array overall current density per bump.

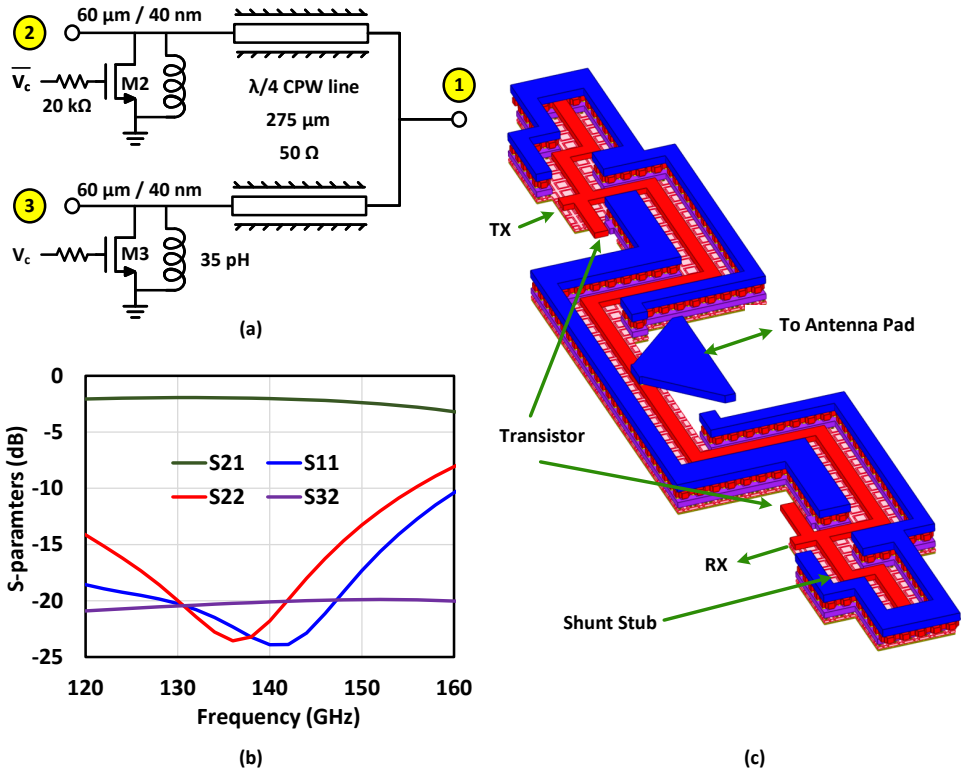


Figure 2.3. TRX Switch (a) single-shunt implementation, (b) layout and (c) simulation results.

2.3.1 TRX Switch

The transmit-receive switch adopts a single-shunt implementation with $\lambda/4$ transmission lines (Fig. 2.3(a)) [29]. A wide transistor size of 60μm is chosen to reduce the switch on resistance and, hence, reduce the overall insertion loss (IL). The switch on resistance is 5Ω (at 1.2V gate voltage) and off capacitance is 40fF. A parallel short-stub inductor of 35 pH is used to resonate out the parasitic capacitances. The $\lambda/4$ CPW lines are used to connect the TX and RX circuits to the antenna port and does not take extra area. The 3D layout of the SPDT switch is shown in Fig. 2.3(c) and the simulated performance is summarized in Fig 2.3(b). The insertion loss of the switch is 2 dB at 140 GHz and increases to 2.4 dB at 150 GHz. The switch is matched at all ports with return loss better than -10 dB from 110 to 155 GHz and the isolation is better than 20 dB across the band from 110 to 170 GHz. The simulated input P1dB looking into port 2

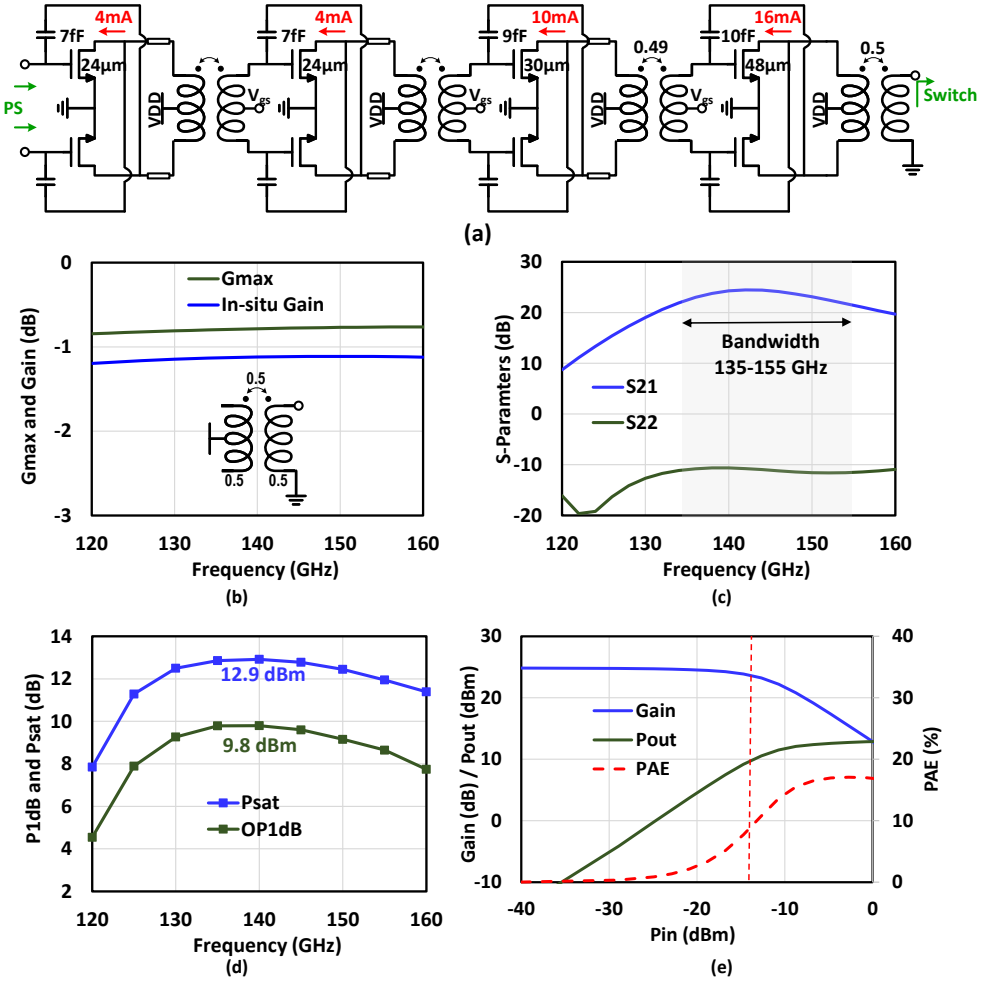


Figure 2.4. 4-Stage PA (a) schematic, (b) output balun Gmax and In-situ gain, (c) gain and output matching, (d) output P1dB and Psat, (e) PAE, gain and Pout versus input power.

(TX port) is 8 dBm when transistor M2 is biased at 0 V and transistor M3 is biased at 1.2 V. In order to further improve the compression point of the switch and make sure it does not degrade the overall P1dB of the TX channel, the transistor M2 is optionally biased at -0.4V, resulting in an input P1dB at port 2 of 14 dBm without affecting the insertion loss.

2.3.2 Power Amplifier

The PA is a four-stage transformer-coupled implementation with neutralization capacitors (Fig. 2.4(a)) [3]. The power stage is designed with transistor size of 48μm, current density of

0.33 mA/μm and 10 fF neutralization capacitors. It is matched close to the optimal load line impedance (Z_opt) of 23+j32Ω using a balun EM structure. The simulated Gmax and in-situ gain of the output balun are -0.8 dB and -1.12 dB respectively at 140 GHz (Fig. 2.4(b)).

The PA drive stage is designed with the same current density as the power stage (0.33 mA/μm), but, with smaller transistor size (30 μm) in order to save power consumption. The wide band interstage matching network between the driver stage and PA has a loaded loss of 2.2-3.2 dB from 120 to 160 GHz. The first two stages are normal gain stages employing 24 μm transistors biased at J_{dc} of 0.17 mA/μm, the interstage matching transformer between the first two stages has a loaded gain of -1.9 dB at 140 GHz. The PA has 4.5 dB of gain control (3 bits) employed by controlling the current density from 0.04 to 0.17 mA/μm in the second amplification stage. The overall gain (Fig. 2.4(c)) of the PA is 24.3 dB at 140 GHz and a 3-dB bandwidth from 135 to 155 GHz. The output matched close to 50Ω while maintaining close to loadpull matching [4]. Fig 2.4(d) shows the output P1dB and Psat across the frequency range 120 to 160 GHz with values of 9.8 and 12.9 dBm at 140 GHz using a 1.2V supply. The simulated peak power added efficiency (PAE) and PAE at P1dB are 17% and 8.5% at 140 GHz (Fig. 2.4(e)).

2.3.3 Low Noise Amplifier

The low noise amplifier is designed as three stage capacitive neutralized common source amplifiers (Fig 2.5(a)) [8]. Fig 2.5(b) shows the simulated S21 and S11 of the amplifier. The peak gain is 18 dB with a 3-dB bandwidth from 135 to 152 GHz. Fig 2.5(c) presents the simulated noise figure from 120 to 160 GHz with a minimum value of 5.9 dB at 140 GHz.

2.3.4 Variable Gain Amplifier

The VGA is a capacitive neutralized common source stage with 4.3 dB gain control (3 bits) (Fig. 2.6(a)). The transistor size is 30 μm and the current density is controlled from 0.03 to 0.14 mA/μm. For TX channel, the input structure is an EM balun to conjugately match the input impedance of the common-source transistors to the 50Ω lines of the distribution network (DN).

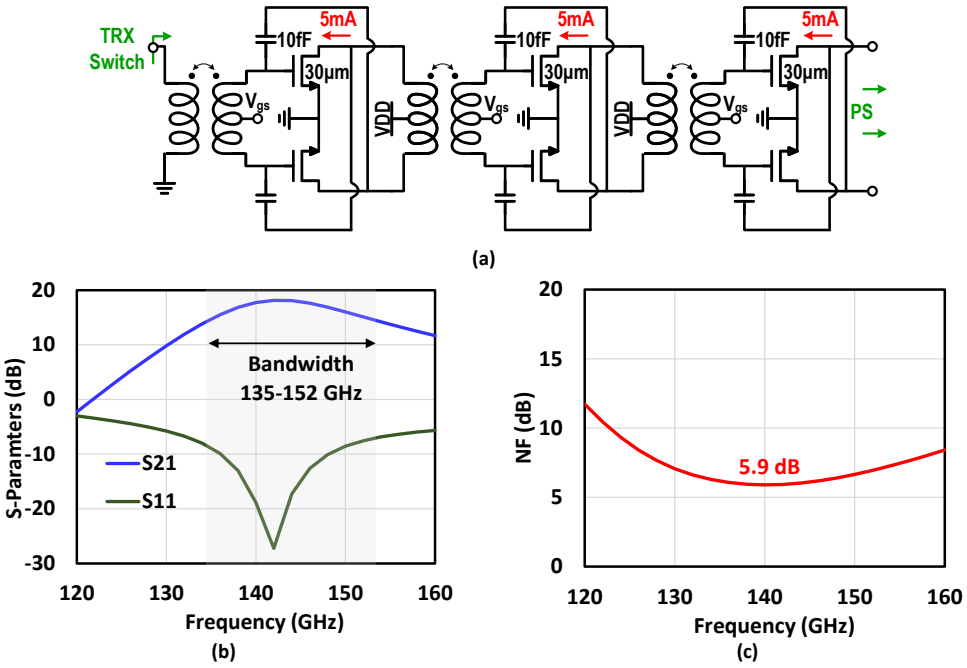


Figure 2.5. LNA (a) Schematic, simulated (b) S-parameters and (c) NF.

The simulated loaded gain of the balun -1.25 dB at 140 GHz. The VGA has a simulated gain of 3.2 to 7.5 dB across gain control at 140 GHz (Fig. 2.6(b)). The S11 performance (Fig. 2.6(c)) is below -10 dB from 135 GHz to 147 GHz and is maintained across gain control. Fig. 2.6(d) shows that the phase variation versus gain control is maintained less than 2^o at 140 GHz. The VGA in the RX channel has similar performance with the exception that the balun is placed at the output of the common source stage to conjugately match to the 50Ω lines of the distribution network.

2.3.5 Phase Shifter

The phase sifter is implemented as a differential quadrature coupled-line-coupler (CLC) followed by a vector modulator and matched with transformers to the input and output stages (Fig 2.7(a)). All differential impedance levels are labeled in Fig 2.7(a). The full EM structure of the phase shifter is shown in Fig 2.7(b).

Fig. 2.8 shows the CLC layout and simulations. It is designed using copper OA/OB

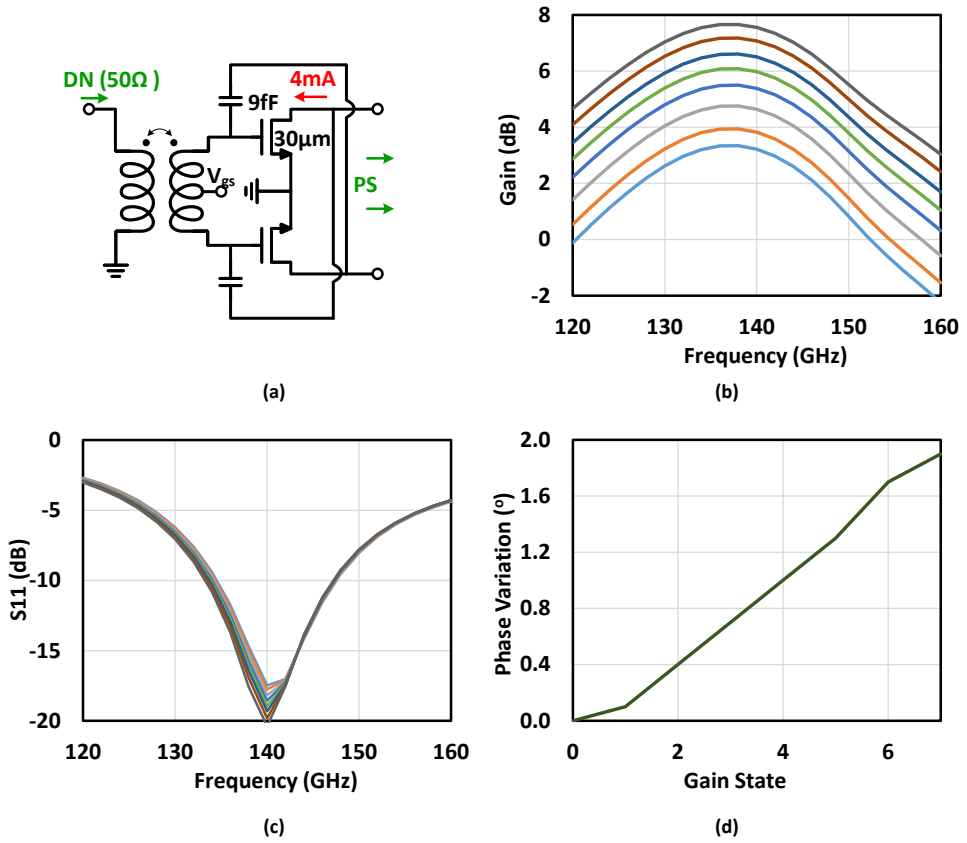


Figure 2.6. VGA (a) schematic simulated (b) gain, (c) S11 and (c) phase variation across gain states.

layers with width and spacing of 2.6μm and 1.2μm respectively. The simulated even and odd impedances are 110Ω and 18Ω respectively. The simulated loss is 0.5dB at 149 GHz and the phase difference between the in-phase (I) and quadrature (Q) outputs is 85^o from 130 to 160 GHz.

The schematic diagram of the vector modulator is presented in Fig. 2.9(a). The tail current mirrors for I and Q are controlled separately in order to choose the desired phase shift as summarized in the table in Fig. 2.9. The digital controls (CI and CQ) are used to choose the quadrant; by switching the polarity of the differential I signal, Q signal or both. The main I and Q differential transistors are sized at 25μm/40nm and are capacitively neutralized with a small 4fF capacitor to improve stability. The controlled current value at each state and the total

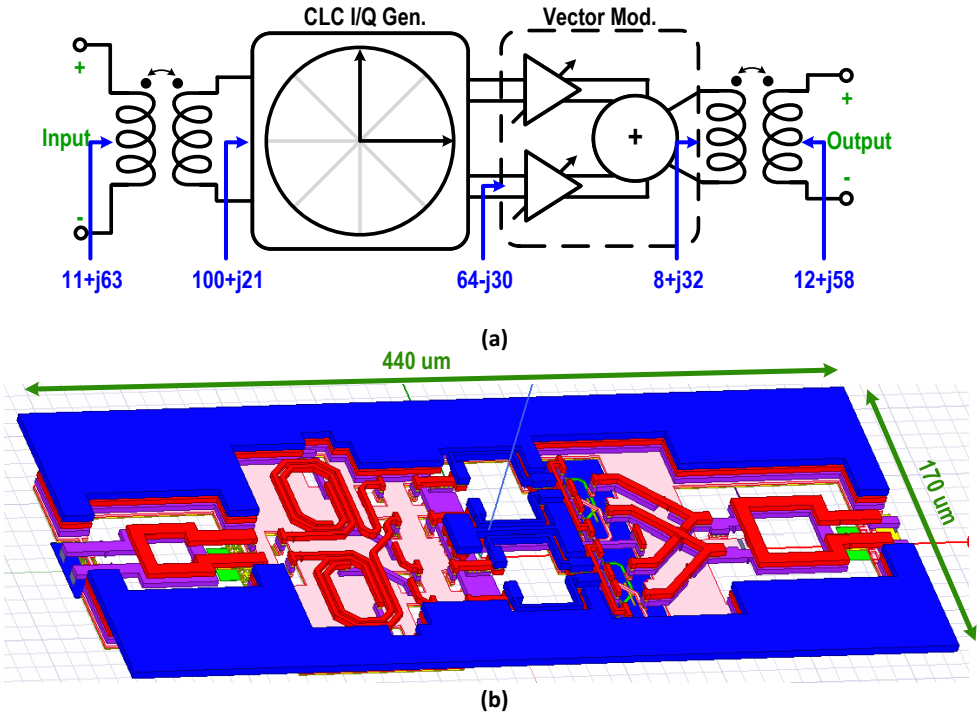


Figure 2.7. Phase shifter (a) block diagram, (b) full EM layout.

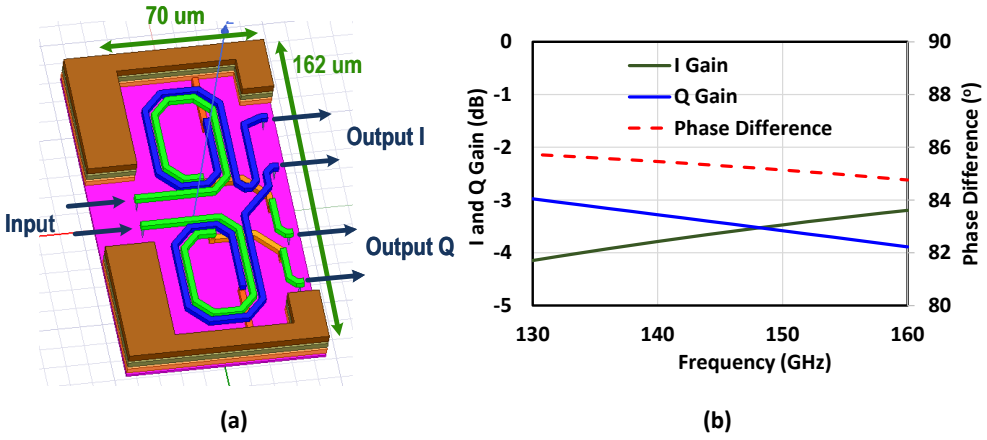
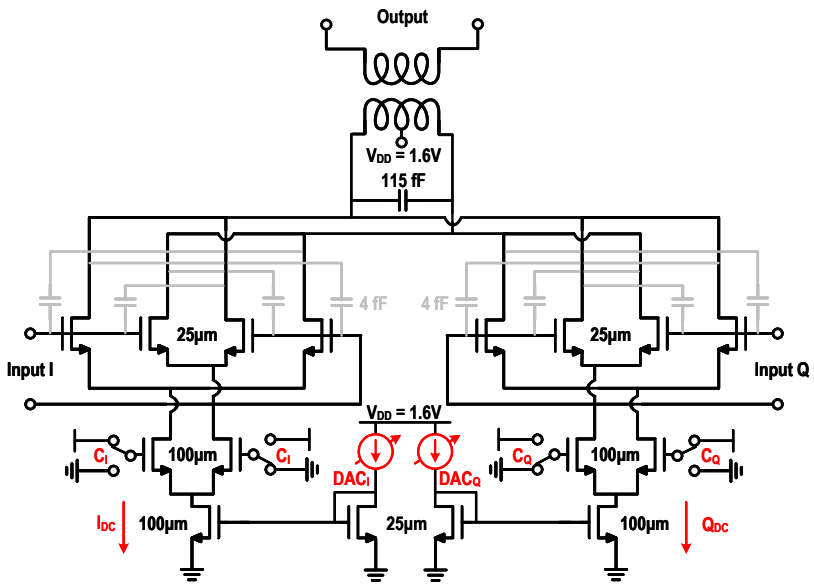


Figure 2.8. CLC (a) EM structure, (b) simulated results.

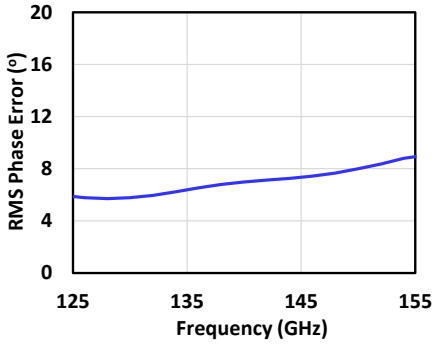
power consumption from 1.6V supply are summarized in Fig. 2.9(b). The simulated gain versus frequency, rms phase and gain errors are presented in Fig. 2.9(c), (d) and (e).



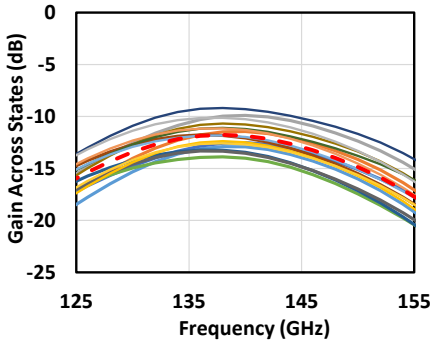
(a)

State	0	1	2	3	4
Phase	0°	22°	45°	67°	90°
I_{DC} (mA)	6.3	6.3	5.4	2	0
Q_{DC} (mA)	0	2	5.4	6.3	6.3
P_{DC} (mW)	15	19	24.5	19	15

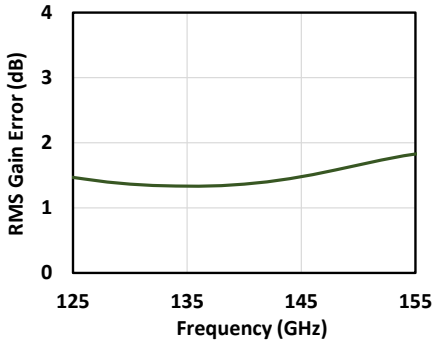
(b)



(c)



(d)



(e)

Figure 2.9. (a) Vector modulator schematic, (b) current control values (c) phase shifter rms phase error, (d) gain for all phase states, (e) rms gain error.

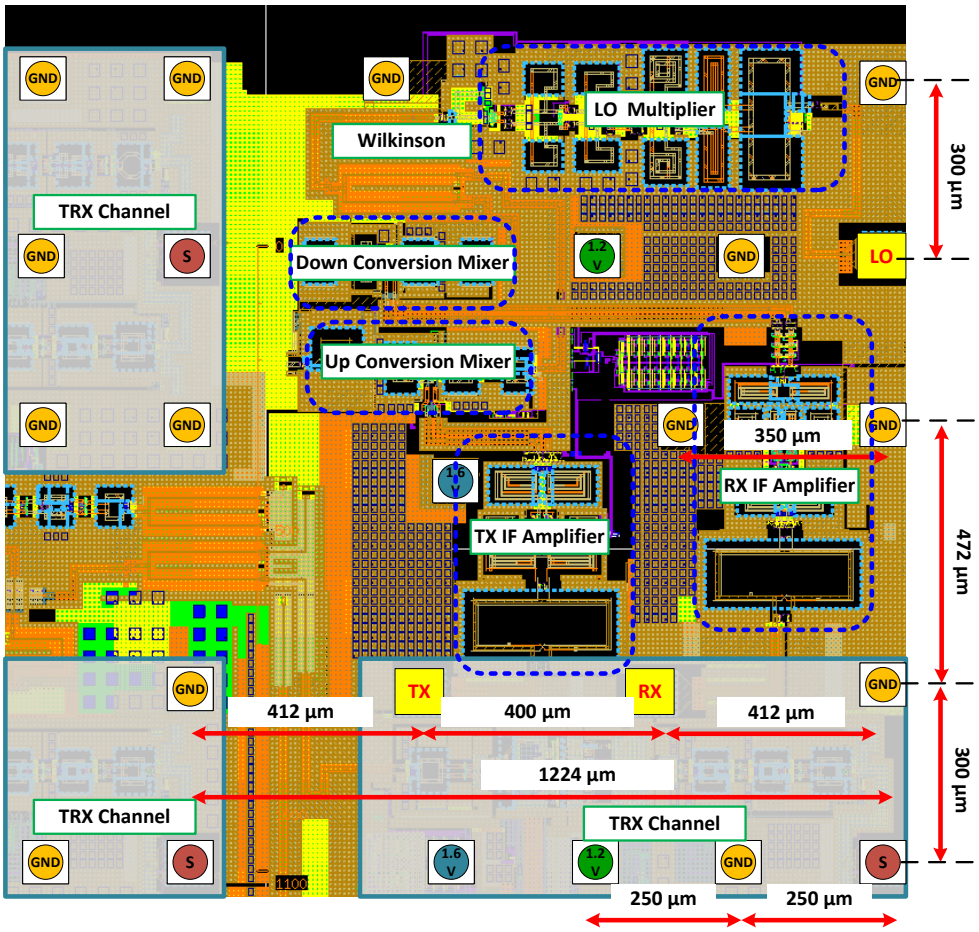


Figure 2.10. UDC channel layout details.

2.4 UDC Channel

The up/down conversion (UDC) channel layout is presented in Fig. 2.10 showing the occupied area and the neighboring RF channels. Unlike the TRX channel, each of the TX and RX IF signals have their own pads. This allows easier interface to the PCB and off-chip RF components, hence, overall simpler system design. Given that either the TX or RX blocks are on at a time, the IF pads are configured as GSSG pads rather than GSGSG in order to reduce the area. The LO pad has similar GND configuration around the signal pad as the TRX channel to improve isolation.

The mixers, LO multiplier and IF amplifiers designs are similar to what is discussed

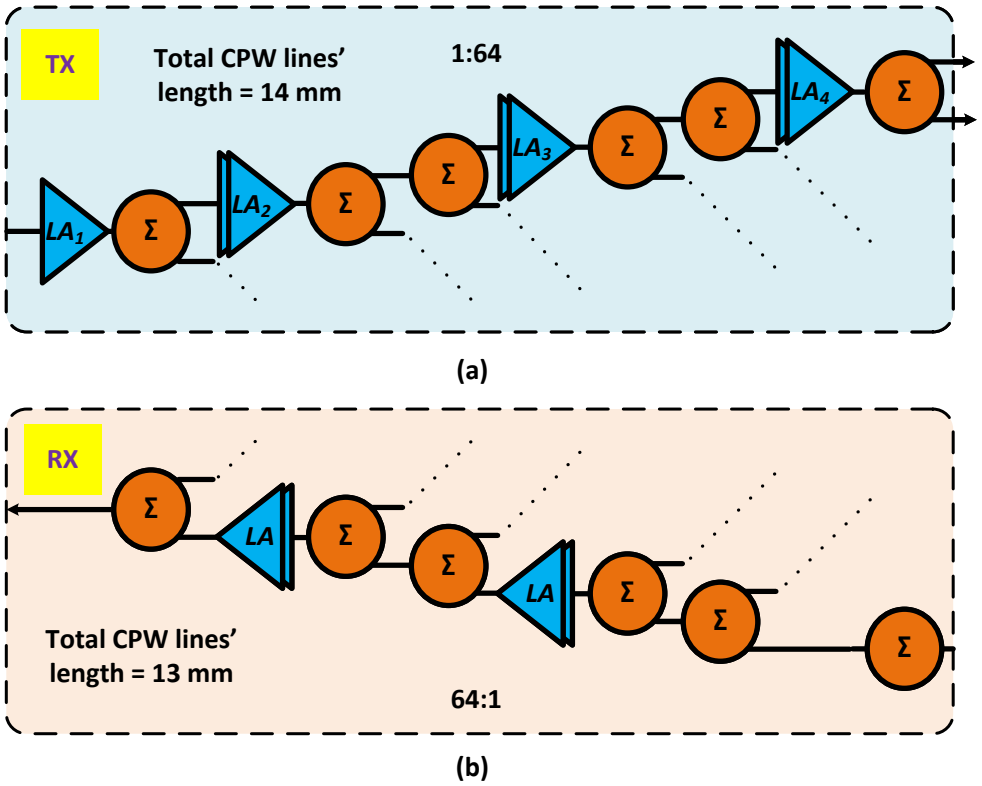


Figure 2.11. Distribution network (DN) block diagram for (a) TX, (b) RX.

in [8] and [3] and are omitted in this article for simplicity. For TX operation, the simulated conversion gain, NF and output P1dB are 5 dB, 7 dB and -14 dBm respectively at RF of 140 GHz and IF of 11 GHz. For RX operation, the simulated conversion, NF and input P1dB are 0.4 dB, 13 dB and -7.4 dBm respectively at RF of 140 GHz and IF of 11 GHz.

2.5 Distribution Network

Fig. 2.11 shows the simplified block diagram for TX and RX distribution networks. Coplanar waveguide (CPW) lines are used for all 140 GHz routings and 6 passive Wilkinson dividers/combiners are used for TX/RX operations. For TX operation, a total of 7 active line amplifier (LA) stages are used in order to compensate for ohmic and division losses. For RX operation, only 4 active LA stages are used to compensate for ohmic losses. Details of each of the building blocks are shown in the next subsections.

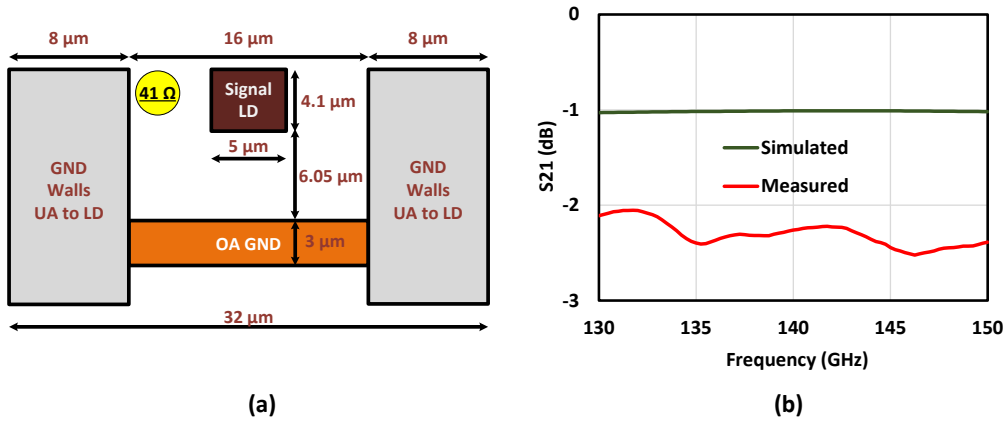


Figure 2.12. CPW (a) structure, (b) simulated and measured loss for 1mm line.

2.5.1 CPW Lines

The stack up of the CPW TL is shown in Fig. 2.12(a), the top metal layer (LD) is used as the signal line and the OB (third top) layer is used as the reference ground. Ground walls up to LD layers are also incorporated with all the dimensions and spacing shown in Fig. 2.12(a). The simulated characteristic impedance of the line is 41Ω which still maintain good matching (S11 ¡ -20dB) across the frequency range 130 to 150 GHz.

The simulated line loss is 1 dB/mm, while the measured loss is 2.2 dB/mm at 140 GHz (Fig. 2.11(b)). This added loss affected the overall performance of the distribution network (hence the array), especially because the total CPW line lengths are 14 and 12 mm for the TX and RX DN respectively. Mainly that led to degradation of the measured EIRP and NF when compared to the simulated values. The overall array system analysis will be discussed in section 2.6.

2.5.2 Wilkinson Divider/Combiner

The EM structure and results of the λ/4 line-based Wilkinson divider are shown in Fig. 2.13. The simulated and measured ohmic losses are 0.32 dB and 0.45 dB respectively at 140 GHz.

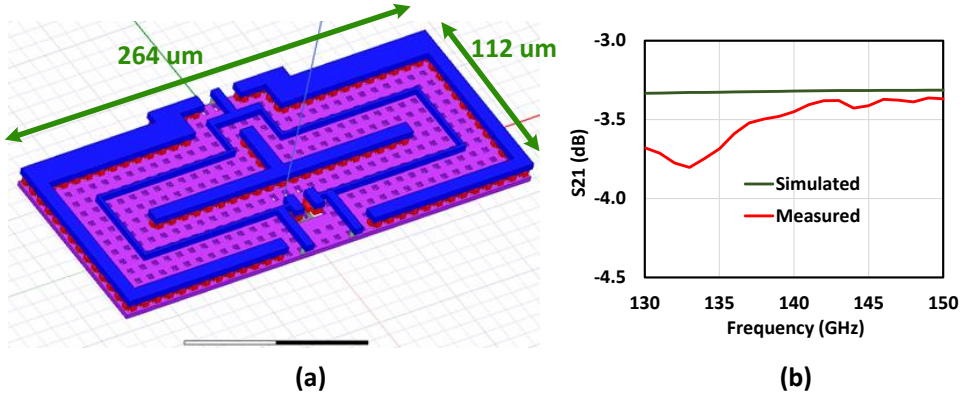


Figure 2.13. Wilkinson divider (a) EM structure, (b) simulated and measured S21.

2.5.3 Line Amplifier

Line amplifiers are implemented very similar to VGAs except they are matched to 50Ω at the input and output. All the LAs are not centered at the same frequency in order to stagger the gain and widen the overall bandwidth of the distribution network. The schematic of the two-stage LA and the simulated gain of all LA variants are shown in Fig. 2.14.

2.5.4 Overall Distribution Network Simulations

The distribution networks for both TX and RX are simulated including all CPW line, Wilkinson dividers/combiners and line amplifiers. For TX DN simulation, the input port is excited and the gain and P1dB are measured at different output ports. For the RX DN, the electronic gain is simulated, which is defined as the output power divided by the total input power at all 64 ports. This is done by using an ideal 1:64 divider to excite all input ports using only one source. The same setup is used for NF and P1dB simulations.

The simulated TX DN gain for different channels is shown in Fig. 2.15(a). The average gain is -5.8 dB at 140 GHz and the variation between the 64 outputs is maintained less than ±0.6 dB across the bandwidth from 135 to 145 GHz. TX DN NF and input P1dB are simulated to be 23.4 dB and 1.3 dBm at 140 GHz respectively (Fig. 2.15(c) and (e)). The RX DN electronic

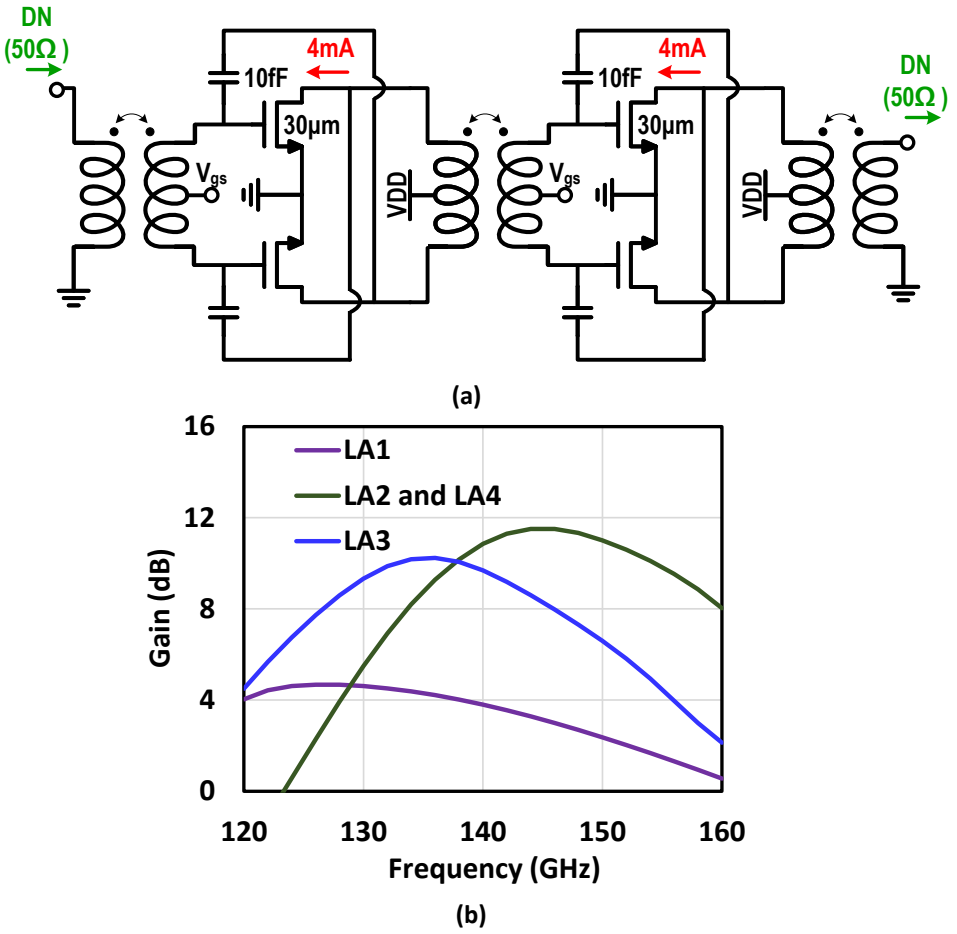


Figure 2.14. Line amplifier (a) schematic, (b) simulated gain.

gain, NF and output P1dB are -2.6 dB, 19 dB and 0 dBm respectively at 140 GHz (Fig. 2.15). Note that all simulation results shown consider the fact that the measured transmission line loss is 2.2 dB/mm rather than 1 dB/mm. The original design target was intended to have better gain and lower noise figure for the distribution networks.

2.6 Array System Analysis

The array system-level noise, power and gain are analyzed for both TX and RX operations. Noting that, all gain, NF and P1dB values used are based on the measured 2.2 dB/mm transmission line loss rather than 1 dB/mm simulated value.

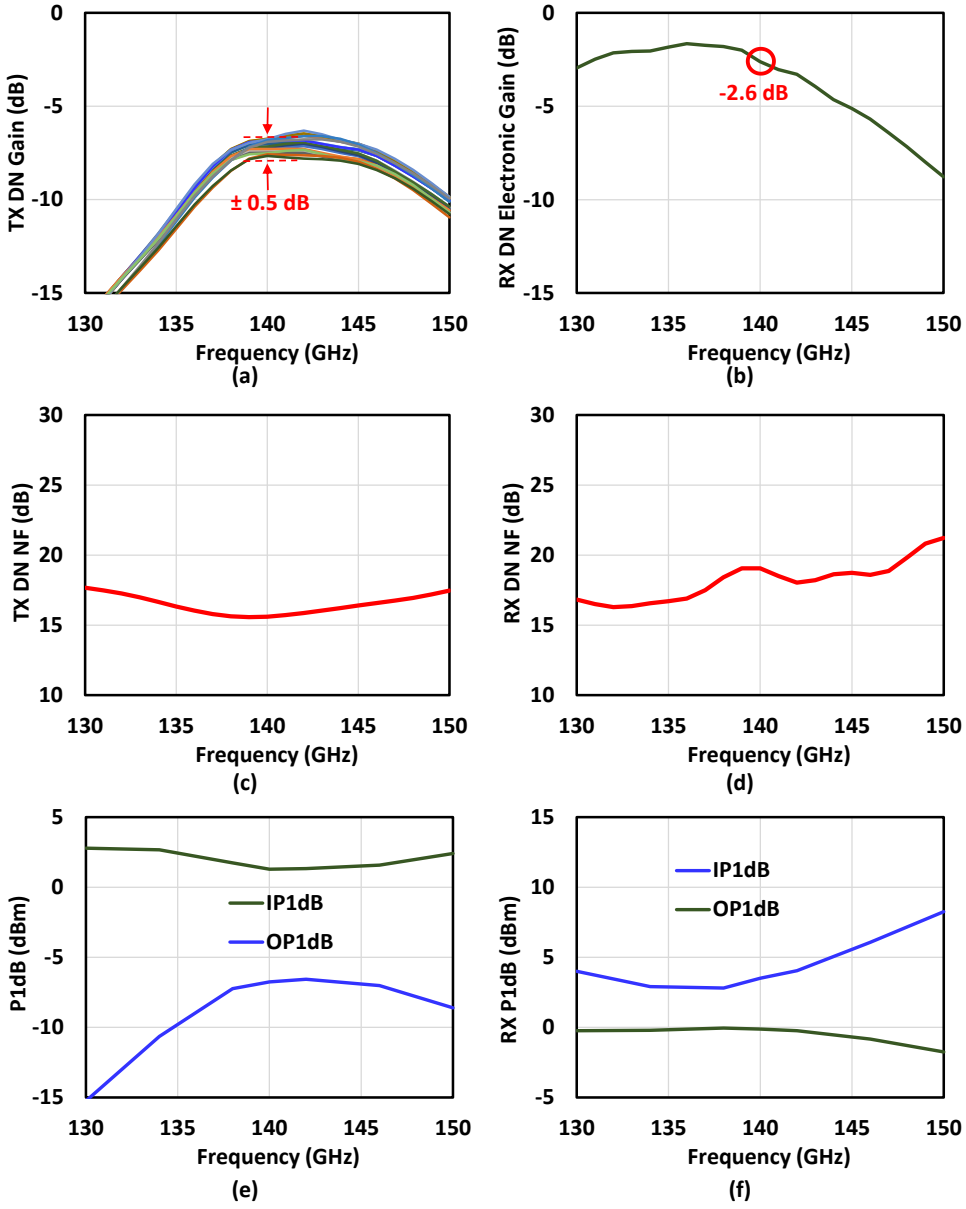
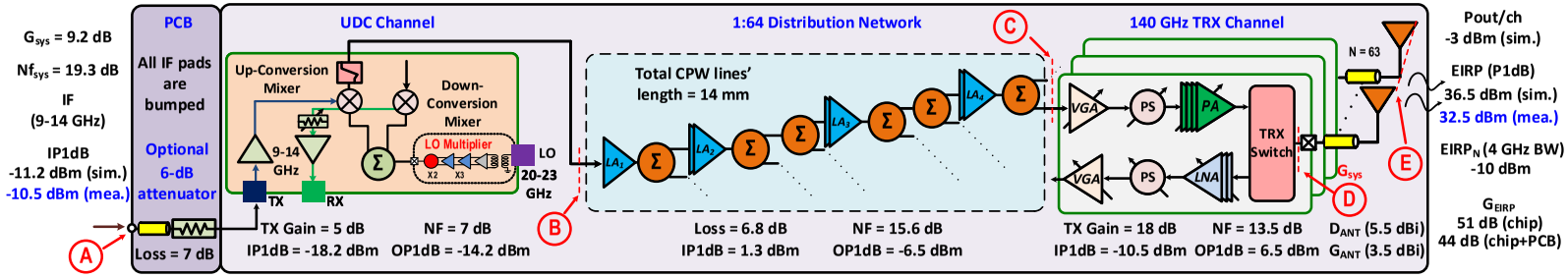


Figure 2.15. DN simulations (a) TX gain, (b) RX electronic gain, (c) TX NF, (d) RX NF, (e) TX P1dB, (f) RX P1dB.

2.6.1 TX System Analysis

Fig. 2.16 shows the system level analysis for the TX operation of the array. Two different gain definitions are used, first is the EIRP gain (G_{EIRP}) and second is the electronic (or system)



	A	B	C	D	E
EIRP Gain (dB)	G_{EIRP} = -7 + 5 - 6.8 + 18 + 3.5 + 20log(63) = 48.7 dB (Meas = 44 dB)				
1-dB Signal Power (dBm)	-12.2	-14.2	-21	-3	36.5 - 4 = 32.5 (EIRP)
Channel Noise (dBm/Hz)			-160.5	-142.5	-121 (incoherent)
UDC Noise (dBm/Hz)	-160	-162	-168.8	-150.8	-111.3 (coherent)
DN Noise (dBm/Hz)		-158.4	-165.2	-147.2	-107.7 (coherent)
Total EIRP Noise	Total transmitted EIRP noise spectral density = -106 dBm/Hz = -16 dBm in 1GHz BW				

Figure 2.16. System-level calculation for the 8x8 TRX array (TX operation).

gain (G_{sys}) as follows:

$$G_{EIRP} = \frac{EIRP}{P_{in-IF}} \tag{2.1}$$

$$G_{sys} = \frac{P_{el}}{P_{in-IF}} \tag{2.2}$$

Where P_{in-IF} is the system input IF power at the PCB SMA, EIRP is the effective isotropic radiated power and P_{el} is the output power per TRX channel. The relation between EIRP and Pel is:

$$EIRP = P_{el} + 20log(N) + G_{ANT} \tag{2.3}$$

Where N is the number of elements (63 elements) and GANT is the antenna gain and is given by:

$$G_{ANT} = D_{ANT} - L_{ANT} \tag{2.4}$$

D_{ANT} is the unit antenna directivity and L_{ANT} is the antenna losses (including ohmic and mismatch losses). For an array with a unit area of A_{unit} = 0.5λ x 0.57λ, the unit patch directivity is given by:

$$D_{ANT} = \frac{4\pi A_{unit}}{\lambda^2} \tag{2.5}$$

The simulated antenna loss is 1 dB (section 2.7), however, in this analysis we used 2 dB of antenna loss to account for part of the excepted extra excess passive losses after fabrication (we used L_{ANT} = -2 dB) leading to G_{ANT} = 3.5 dBi.

The simulated channel gain (G_{TX-ch}) in the TX mode is 18 dB with output and input compression points of 6.5 dBm and -10.5 dBm. The 64:1 distribution network has a total loss (L_{TX-DN}) of 6.8 dB, the UDC channel has 5 dB of gain (G_{UC}), and the PCB has a T-attenuator with an overall 7 dB of loss (G_{TX-PCB}). Leading to simulated TX system gain of:

$$G_{sys} = G_{TX-ch} - G_{TX-DN} + G_{UC} + G_{TX-PCB} = 9.2\ dB \tag{2.6}$$

The simulated EIRP gain is then calculated using 2.3 and 2.6:

$$G_{EIRO} = G_{sys} + 20log(63) + G_{ANT} = 48.7\ dB \tag{2.7}$$

The simulated array input IF P1dB is -11.2 dBm at the SMA connector input, hence, giving a simulated EIRP of 36.5 dBm. However, the measured array input IF P1dB and EIRP are -10.5 dBm and 32.5 dBm respectively. The 4 dB difference between simulated and measured EIRP can be due to four reasons. First, extra passive losses in the chip/PCB after fabrication when compared to simulation even after considering the 2.2 dB/mm TL measured loss. Second, output P1dB of the UDC channel is reduced after fabrication. Third, measurement errors of ±1dB. Fourth, the vector addition of output power of each channel (P_{cl}) is less than 20log(63) (36 dB) due to gain and phase mismatches between each channel, hence, leading to a non-perfect vector addition. In measurements, we observe that the addition factor is 34 dB rather than 36 dB. This observation is done by measuring the output power and phase of each channel by itself and then measuring the overall EIRP and calculating the vector addition error.

The simulated TRX channel NF is 13.5 dB and the calculated output noise power density from each channel (Fig 13(a)) is:

$$P_{TXch-N/ch} = -174 + NF + G_{TX-ch} = -142.5\ dBm/Hz \tag{2.8}$$

The radiated output from each channel adds incoherently summing to a total noise $EIRP_{chN}$ of:

$$EIRP_{chN} = -142.5 + 10log(N) + G_{ANT} = -121\ dBm/Hz \tag{2.9}$$

The noise radiating from the UDC channel on the other side will add coherently (factor of 20log(N)) summing to a total noise $EIRP_{UDC}$ of -111.3 dBm/Hz (Fig. 2.16). The noise from the line amplifiers in part will add coherently and in part incoherently depending on how close the amplifier is to the channel. The total effective noise figure is simulated to be 15.6 dB for

coherent addition. Leading to a total noise $EIRP_{DN}$ of -107.7 dBm/Hz.

In total, the array noise $EIRP_N$ is -106 dBm/Hz and in a 1 GHz BW is equal to -16 dBm. Therefore, the TX system radiated signal-to-noise ratio (SNR_{TX-sys}) at 32.5 dBm EIRP (measured P1dB) and 1 GHz BW is 48.5 dB. At 25 dBm EIRP, this translates to an SNR of 41 dB. Note that, the radiated noise EIRP in measurement is even lower for the calculation for same reasons discussed for the TX ERIP.

2.6.2 RX System Analysis

Fig. 2.17 shows the system level analysis for the RX operation of the array. The RX array electronic gain (G_{RX}) is defined as:

$$G_{RX} = \frac{P_{out-IF}}{P_{inc}} \tag{2.10}$$

Where P_{out-IF} is the output power at the PCB SMA connector and P_{inc} is the total incidence power on the array aperture and is given by:

$$P_{inc} = SA_{ph} \tag{2.11}$$

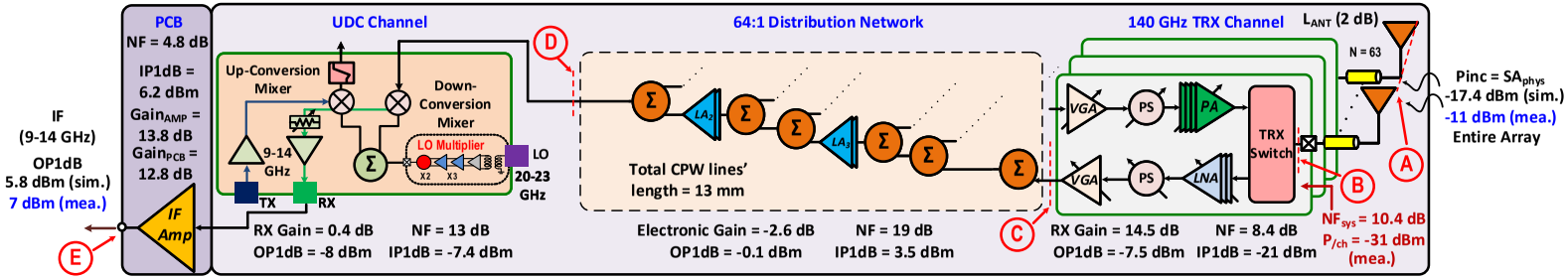
Where A_{ph} is the physical area of the 8x8 array and is given by 64*Aunit = $8.35x10^{-5}$ m^2 (Aunit = 0.5λ x 0.57λ at 140 GHz). S is the incident power density from the transmitting antenna and is given by S=$P_T G_T/(4\pi R^2)$, P_T and G_T are the transmitted power and gain of the transmitting antenna, and R is the distance between the transmitting antenna and the array.

An alternative method to calculate the incidence power is using the SLF equation as follows:

$$P_{inc} = P_T G_T * SLF * D_R \tag{2.12}$$

$$D_R = \frac{4\pi A_{ph}}{\lambda^2} = 23.6\ dB\ at\ 140\ GHz \tag{2.13}$$

Where D_R is the RX array directivity. Note that antenna directivity is used rather than gain since



	A	B	C	D	E
Electronic Gain	G_{RX} = -2 + 14.5 - 2.6 + 0.4 + 12.8 = 23.2 dB (Meas = 20 dB)				
Signal Power (dBm)	-30	-50	-35.5	-20.1	-6.9 (Meas = -10)
Noise (dBm/Hz)	Total Input referred	-163.6	-149.1	-151.7	-138.5
Noise Power (dBm) BW = 1 GHz		-73.6	-59.1	-61.7	-48.5

Figure 2.17. System-level calculation for the 8x8 TRX array (RX operation).

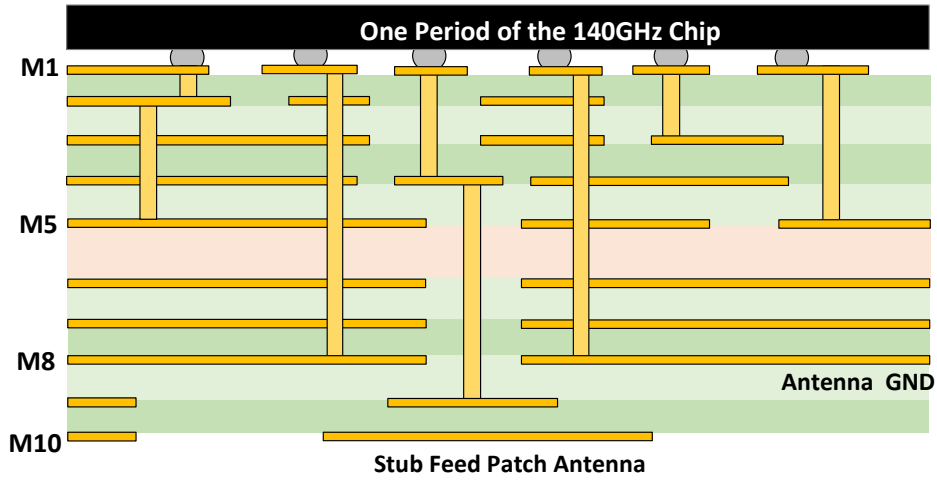


Figure 2.18. Stack of 10-layer low-cost PCB.

the antenna loss (L_{ant}) is already part of the RX electronic gain.

The RX system electronic gain is simulated to be 23.2 dB. The measured value is 20 dB and the discrepancy is due to the same reasons discussed in the TX analysis section. The measured P_{inc}-1dB at 140 GHz is -11 dBm meaning the input P1dB ($P_{inc/ch}$) at the input of each channel is -11 -10log(63) - L_{ANT} = -31 dBm. The system's simulated noise figure is 10.4 dB resulting in an output SNR of 38.5 dB when the P_{inc} is -30 dBm with 1 GHz noise BW (Fig. 2.17).

2.7 Antenna Design

The TRX array chip is flipped on a standard commercial organic laminate interposer with an ε_r of 3.2 and loss tan of 0.002 (equivalent to Panasonic Megtron 7) is used. The stack-up shown in Fig. 2.18 features 10 metal layers (M1–M10). The beamformer is mounted on layer M1, while M2-M4 layers are primarily used for distributing the DC supply lines. Layer M3 functions as the 1.2V VDD layer, as the current in is large and wider supply lines are necessary to avoid excessive IR drop and temperature rise. The transmission lines for the TX and RX IF signals (at 9-14 GHz), and LO signal (at 21 to 23 GHz) are located on M5 layer. M6 and M7

layers are utilized as GND planes to separate analog and digital signals. The stacked probe-fed stub-coupled microstrip antenna is situated on M9 (stub) and M10 (patch), with M8 serving as the antenna group plane.

The simulated antenna S_{11} and S_{21} when scanning in the E and H planes and a -10 dB bandwidth of 130-150 GHz (14.3%) is achieved. At around 140 GHz, the co-simulate model has a return loss of ¡ -15 dB. The simulated S_{21} contains the antenna radiation efficiency, metal loss and ohmic loss up to the reference port in the chip layout, with an average S_{21} of 0.9 dB in most scanning directions. Note that in E-plane scanning, it is hard to get the good matching and high S_{21} over 40^o since the TM0 scan blindness limits it.

2.8 Chip and Packaging

The 8x8 chip is fabricated in GlobalFoundries 45RFSOI CMOS technology occupying a total area of 9.84*8.27mm2 and is flipped on the RF PCB (Fig. 2.19). Figure 2.20(a) and (b) show the top and bottom sides of the fabricated and assembled RF PCB. The top side has the 8x8 chip, external RX IF amplifier, temperature sensor IC, SMA connectors for TX, RX and LO, and QSE connector for supply, bias and digital controls. The bottom side has the antenna array.

A DC board is designed with several DC-DC converters, LDOs and an Arduino board to provide the RF board with all the required supply voltages, bias and SPI controls while using only one external voltage supply of 8-12V (Fig. 2.20(c)). A cooling system is also attached to the RF/DC boards with a mounting box and lid (Fig. 2.20(c), (d) and (e)). A thermal pad (part number A17752-04) is used to attach the TRX chip to a heat pipe (121726), which extends across the DC board and three heat sinks (ATS-56001-C3-R0) are attached to it to reduce the thermal resistance (Fig. 2.20(e)). A lid is used to cover the box and three heat fans (FFB0412VHN-TP03) are attached to it for further cooling (Fig. 2.20(d)). The box (with the lid) is then attached to an antenna positioner (GMI03) and used for all OTA measurements. Fig. 2.20(f) shows the mounted box and the measurement setup.

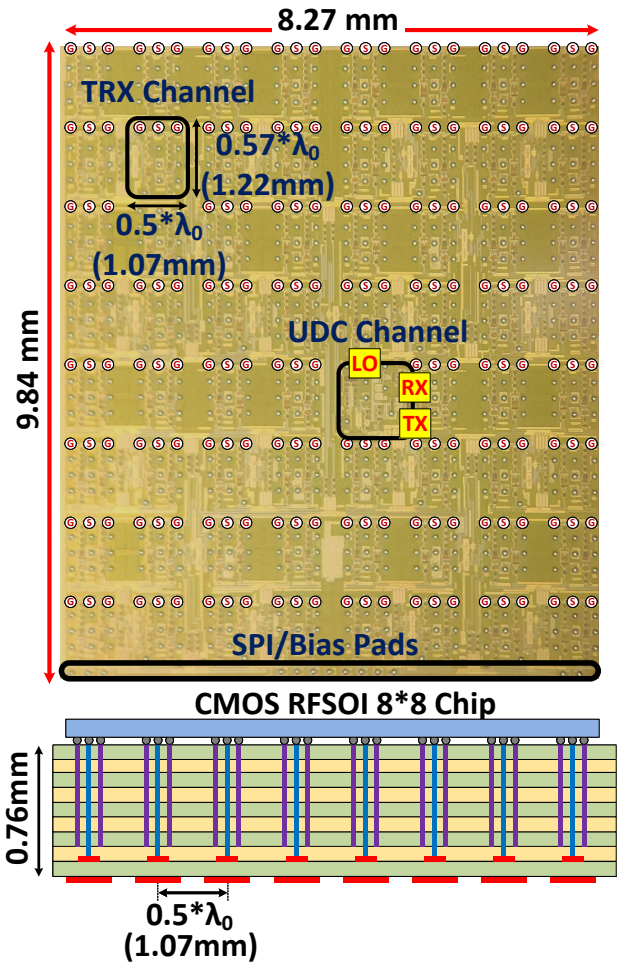


Figure 2.19. Chip die photo and cross section of the RF board.

2.9 Over-The-Air (OTA) Measurements

2.9.1 TX CW Measurements

TX CW signal measurement setup is shown in Fig. 2.21(a). The array (in TX operation) is fed with an IF signal (9-14 GHz) using Keysight N5340C PNA. The radiated signal from the array (at 130-150 GHz) is received with a standard WR-6 horn antenna placed at a 0.74m distance from the array (Fig. 21(f)). The RF signal is then down-converted back to IF using a WR6.5 VDI down-converter unit and fed back to the PNA. After de-embedding all the setup gains and losses, the gain and EIRP of the array are measured. The pattern is also measured

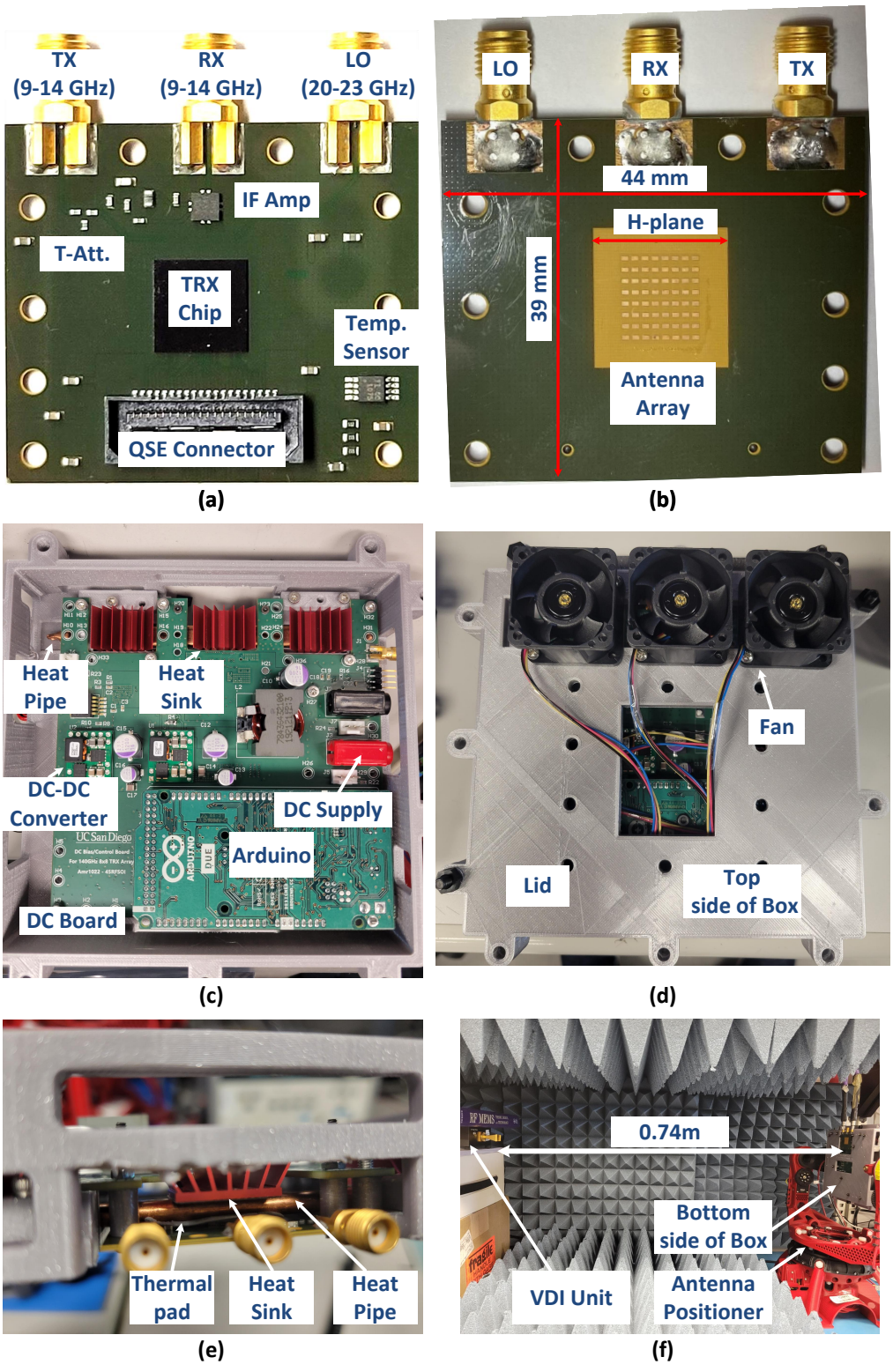


Figure 2.20. Chip die photo and cross section of the RF board.

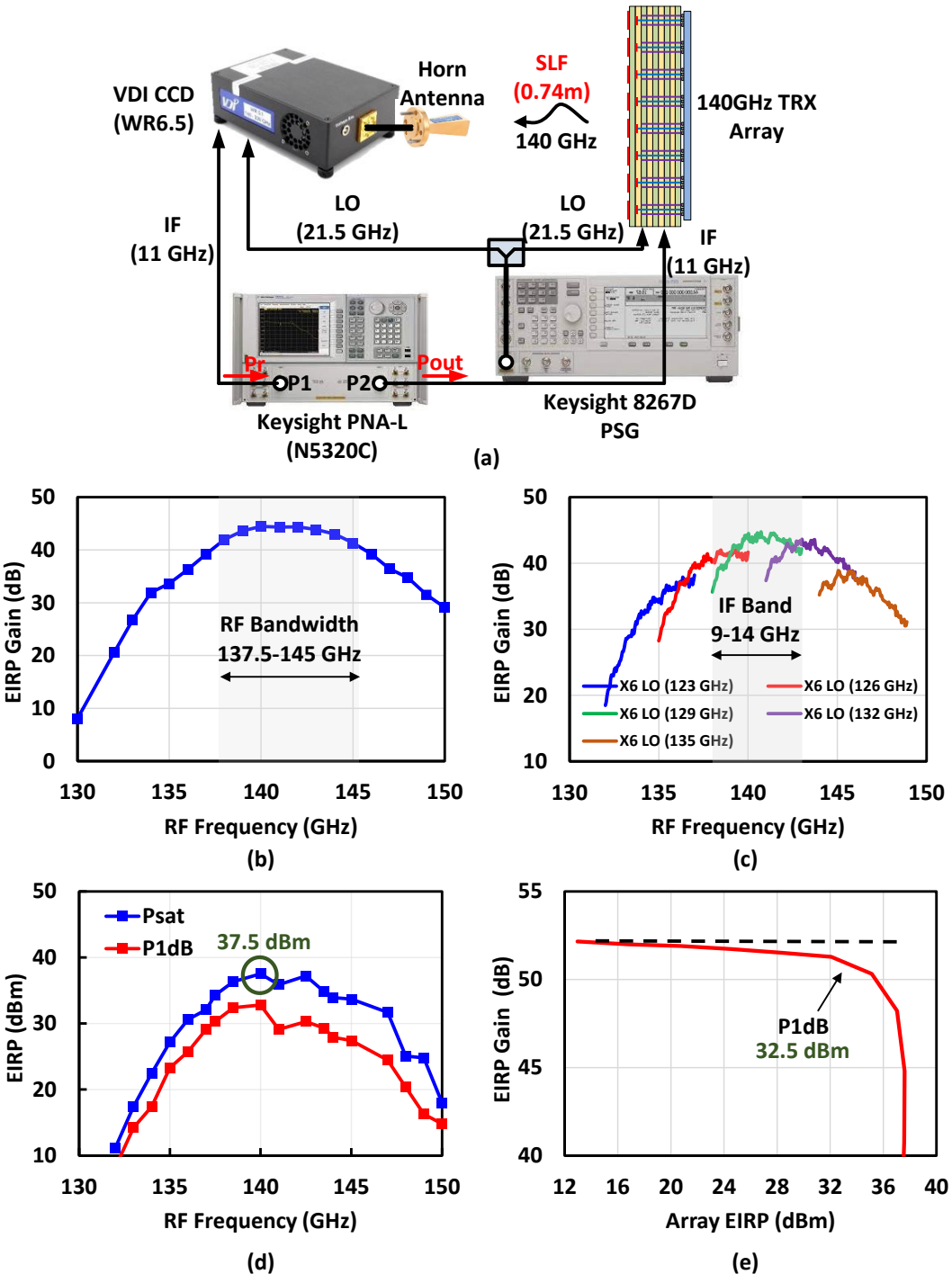


Figure 2.21. (a) CW measurement setup, (b) GEIRP at fixed IF frequency, (b) GEIRP at swept IF frequency and different LO frequencies, (c) EIRP at saturation and at P1dB, (d) array AM-AM response.

using the same setup by rotating the antenna positioner.

Fig. 2.21(b) shows the measured EIRP gain (G_{EIRP}) of the system (chip + PCB) with fixed IF frequency (11 GHz) and swept LO and RF frequencies. The peak measured gain is 44 dB with an RF bandwidth of 137.5-145 GHz (limited by distribution network and TX channel).

Fig. 2.21(c) presents the instantaneous bandwidth of the array by measuring the EIRP gain versus swept IF frequency (9-14 GHz) at different LO frequencies.

The measured EIRP at saturation and at P1dB are presented in Fig. 2.21 across RF frequency. The measured peak $EIRP_{sat}$ is 37.5 dBm. To our knowledge, this is the highest demonstrated EIRP at 140 GHz from a wafer-scale phased array in silicon technology to-date. In this array, the UDC (rather than TRX) channel is the limiting factor for EIRP. This is due to the extra losses we experienced because of the higher transmission line losses (as explained in Section 2.5).

The TX array scanning patterns at 140 GHz for both H- (x-direction) and E- (y-direction) planes are shown in Fig. 2.22. The array is electronically scanned from -60^o to 60^o in the H-plane with a pattern gain drop of 5.3 dB at ±60^o scan angles. In the E-plane, the array is scanned from -38^o to 38^o with a pattern gain drop of 6.5dB at 38o scan angle. The 3-D pattern (array is scanned to broadside) is shown in Fig. 2.22(c) with a side lobe level (SLL) of better than 12.5 dB across all angles.

2.9.2 RX CW Measurements

The RX operation measurement setup is very similar to the TX setup (Fig. 2.21(a)) but using a WR-6 VDI up-converter unit. The measured scanning patterns are shown Fig. 2.22. The RX can also scan to ±60^o and ±38^o in the H- and E-planes respectively. The 3-D pattern at broadside also shows SLL performance of better than 12.5dB.

The measured RX array electronic gain (G_{RX}) is shown in Fig. 2.23(a)(b). The peak gain of 20 dB with an RF 3-dB bandwidth of 135-142.5 GHz are measured.

The measurement setup for P_{inc} 1-dB compression point is shown in Fig. 2.23(c). Here

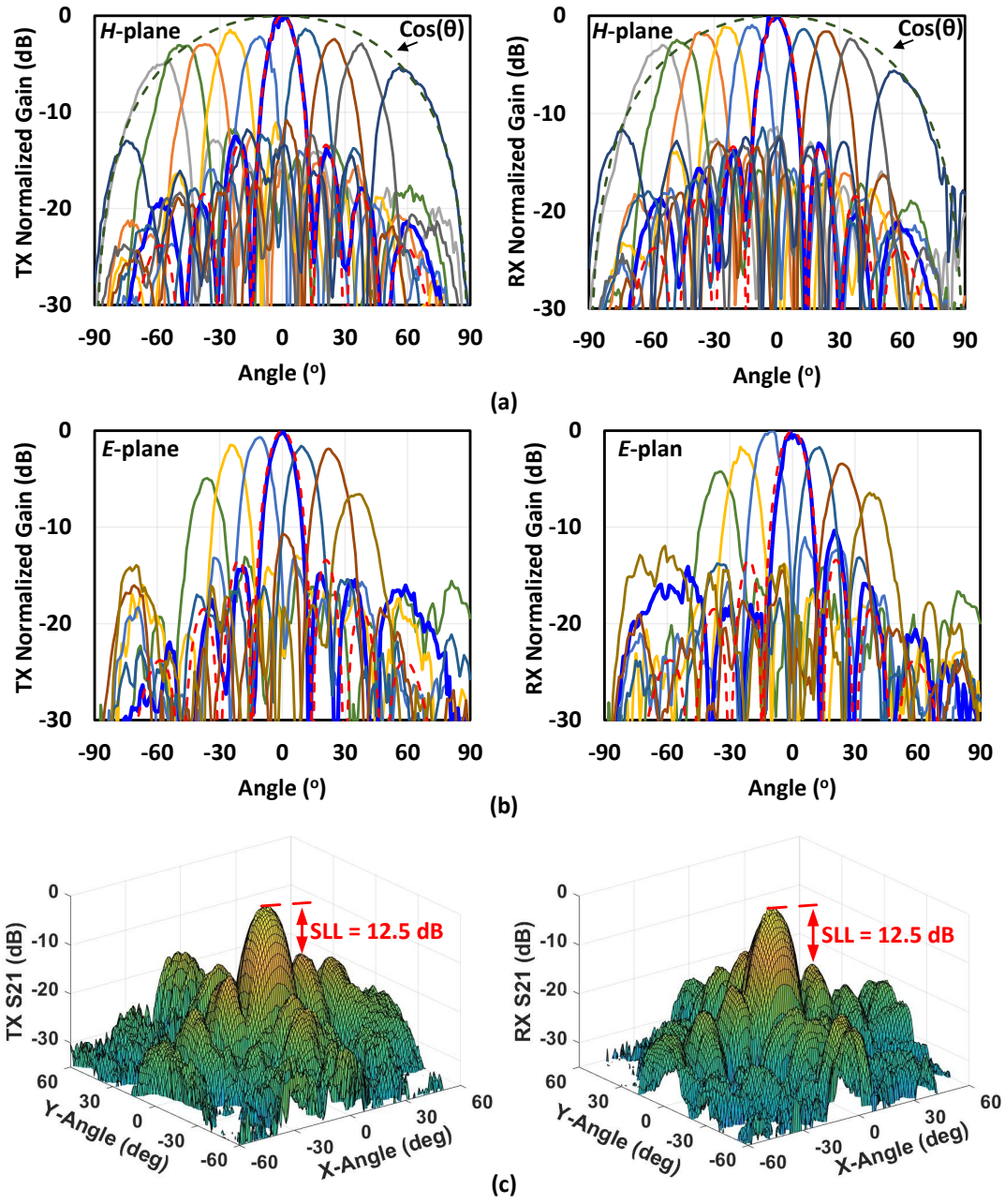


Figure 2.22. (a) CW measurement setup, (b) GEIRP at fixed IF frequency, (b) GEIRP at swept IF frequency and different LO frequencies, (c) EIRP at saturation and at P1dB, (d) array AM-AM response.

the VDI up-converter unit is replaced with a VDI AMC-333 module (OP1dB of 18dBm at 140 GHz) to be able to compress the RX array when considering all the high space loss factor at

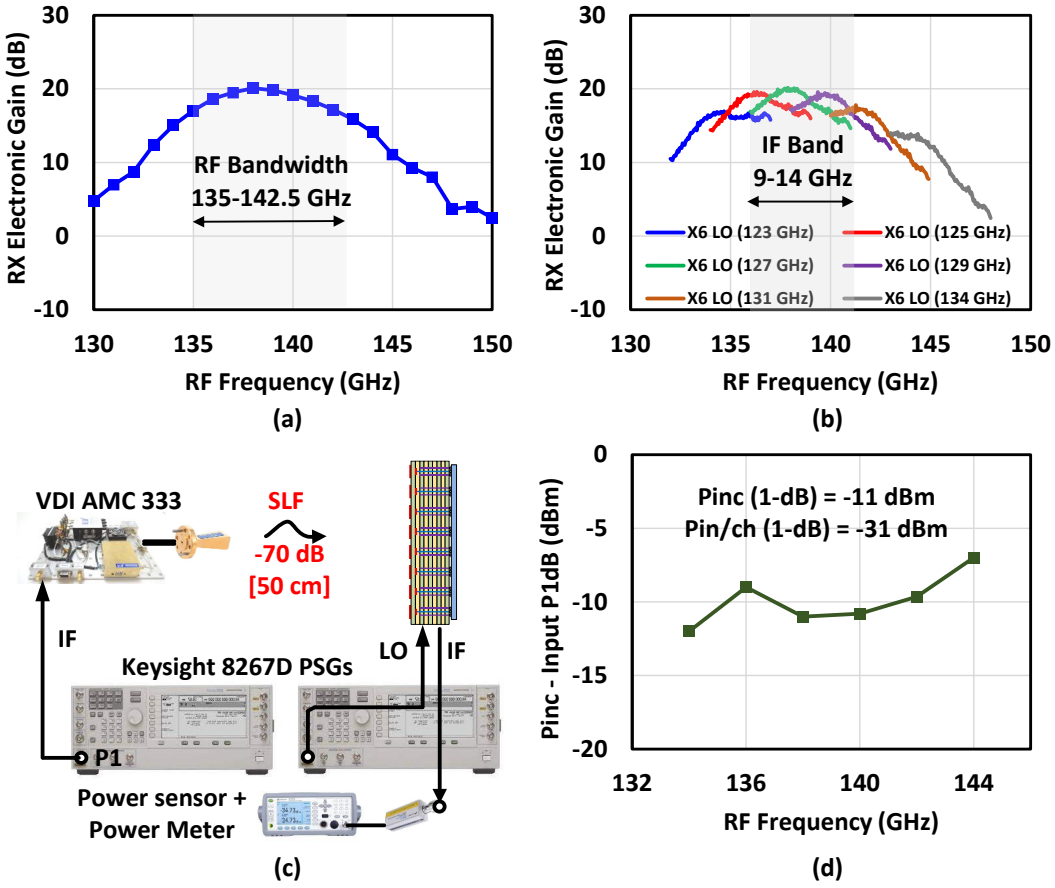


Figure 2.23. (a) G_{RX} at fixed IF frequency, (b) G_{RX} at swept IF frequency and different LO frequencies, (c) P_{inc}-1dB measurement setup, (d) measured RX operation Pinc-1dB.

140GHz. The measured P_{inc} 1-dB compression point is -11 dBm at 140 GHz (Fig. 2.23(b)). This translates to input power at each channel of -30.5 dBm (see section 2.6).

2.9.3 TX Modulation Measurements

The measurement setup for modulation measurement is shown in Fig. 2.24(a). Keysight AWG (M8195A) is used to generate all modulation waveforms at 11 GHz (IF frequency). The TX array is directly fed with the generated waveforms. The radiated signal at 140 GHz is down converted by the VDI unit (at 0.3m distance) and fed to Keysight oscilloscope (DSOZ6632A) for demodulation and EVM measurements.

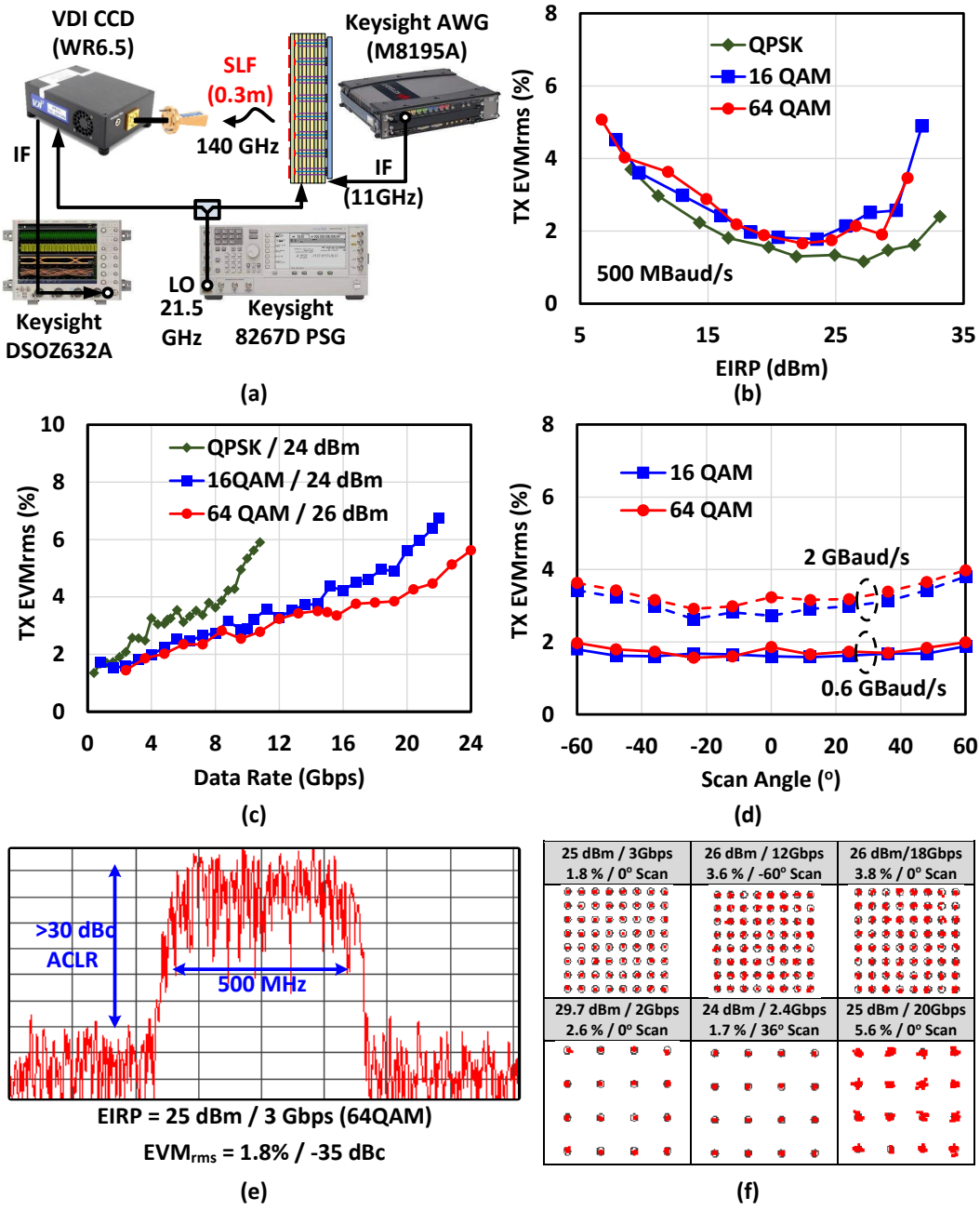


Figure 2.24. TX OTA (a) modulation measurement setup, (b) EVM versus array EIRP, (c) EVM versus data rate, (d) EVM versus beam scan angle, (e) array output spectrum (after down-conversion with CCD unit), (f) output constellation for different EIRP values, scan angles and modulation types.

Fig. 2.24(b) presents the measured EVM versus array EIRP for QPSK, 16QAM and 64QAM modulated signals at 500 MHz bandwidth. At 25 dBm radiated power, the measured rms EVM is around 2% for 16- and 64-QAM signals. Fig. 2.24(c) shows the EVM versus data-rate, with a peak data rate of 22 Gbps and 24 Gbps for 16- and 64-QAM signals and rms EVM of 6.8% and 5.6% respectively. This is measured at an EIRP of 24 dBm and 26 dBm for 16- and 64-QAM signals respectively.

The EVM_{rms} is maintained less than 4% across all scan angles from -60^o to 60^o (Fig 2.24(d)) for 2GBaud/s modulated signals. Fig. 2.24(e) shows the TX array output spectrum (after down conversion by the VDI unit) for EIRP of 25 dBm and modulation bandwidth of 500 MHz and 640QAM signal. The measured EVMrms is 1.8% (35 dB SNR) with an adjacent channel leakage ratio (ACLR) better than 30 dBc. The table in Fig. 2.24(f) shows some demodulated constellations at different EIRP values, scan angles and modulation types.

2.9.4 RX Modulation Measurements

The modulation measurement setup for RX operation is similar to the one presented in Fig. 2.24(a) but replacing the VDI CCD unit with a CCU unit and connecting the array output to the Keysight oscilloscope. Fig. 2.25(a) shows the measured EVM versus the array incident power (P_{inc}), the VDI CCU unit has an output 1-dB compression point of -10 dBm, and with a communication distance of 0.3m, this translates to an incidence power to the array (P_{inc}) of around -28 dBm. Hence, the EVM performance dynamic range is limited by the CCU unit, and we could not measure EVM close to the array P_{inc} 1-dB (-11 dBm) using this setup. Fig. 2.25(b) shows a peak data rate for the RX mode of up to 22 and 24 Gbps for 16- and 64-QAM with an EVMrms of 6.4% and 5.75% respectively.

Modulation performance across scan angles from -60^o to 60^o is presented in Fig. 2.25(c). Finally. Fig. 2.25(d) shows the output constellations for different scan angles and modulation types (16- and 640QAM).

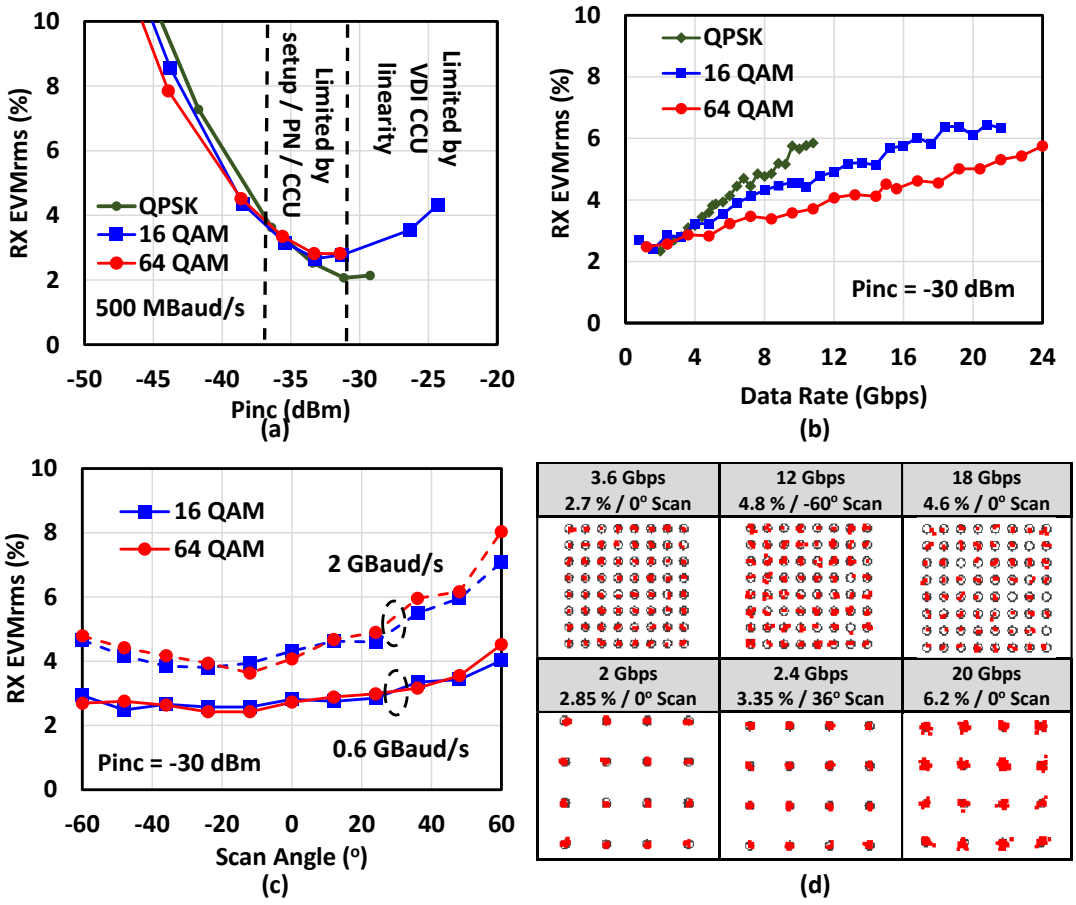


Figure 2.25. RX OTA (a) EVM versus array P_{inc}, (b) EVM versus data rate, (c) EVM versus beam scan angle, (d) output constellation at different scan angles and modulation types (P_{inc}=-30 dBm).

2.10 TX-RX Wireless Link

Fig. 2.26 shows the measurement setups when pointing two arrays at each other, one configured as TX operation and the second as RX operation. The communication link is demonstrated in 1.45m and 4.2 link distances. Keysight M8195A AWG and DSO Oscilloscope are used to generate and demodulate the modulated signals at 11 GHz (IF frequency) respectively. The DSO scope is running with VSA89600 demodulation software with equalization. The use of the same LO source reduces the phase noise contribution of the LO and allows for better EVM.

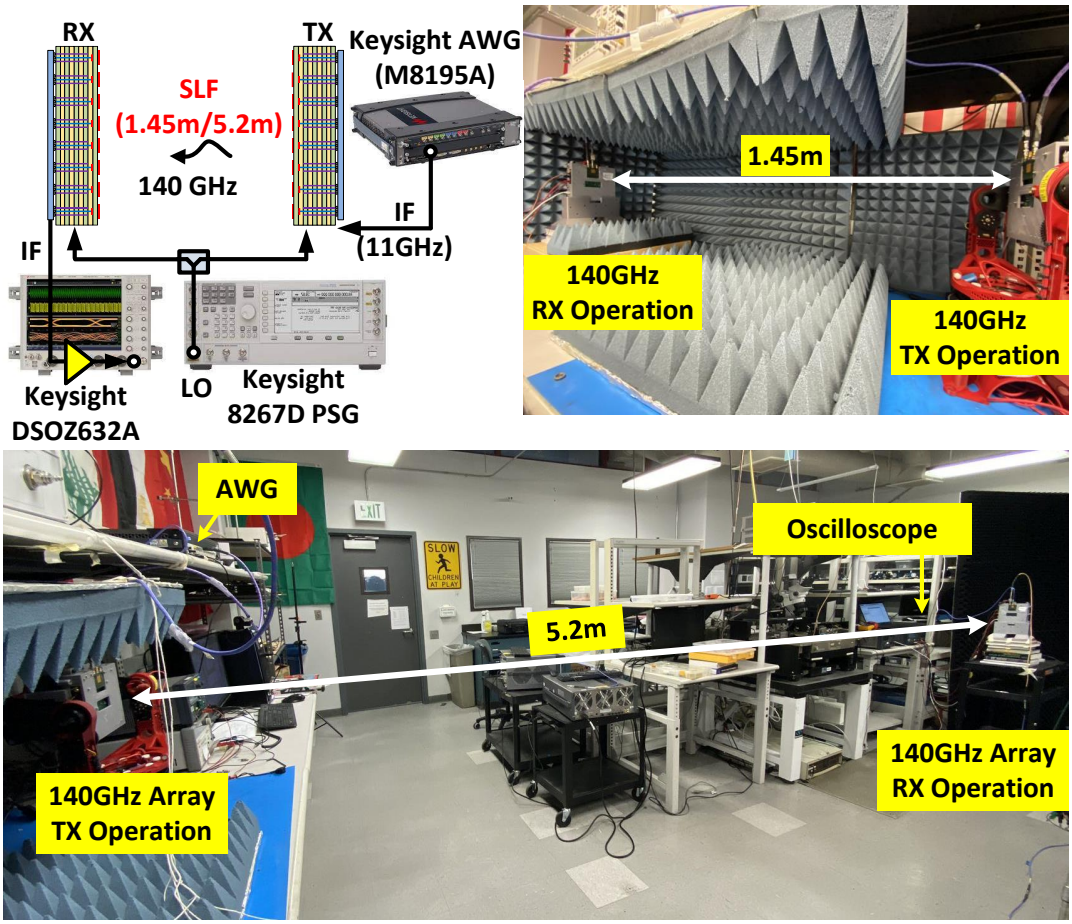


Figure 2.26. TX-RX communication link measurement setups.

An external IF amplifier is placed before the DSO to further amplify the signal and reduce noise contribution of the DSO to the total EVM.

2.10.1 TX-RX link EVM versus TX EIRP

Fig. 2.27 presents the measured rms EVM versus TX EIRP for QPSK, 16- and 64-QAM modulated signals for both communication link distances. The signal level reaching the RX array when switching the distance from 1.45m to 4.2m decreases by a factor of 20 log (5.2/1.45) =11.1 dB. Therefore, we can see a shift in the EVM plots (Fig. 2.27) of around 11 to 12 dB due to reduction in SNR because of the RX array thermal noise at low EIRP values. At higher EIRP,

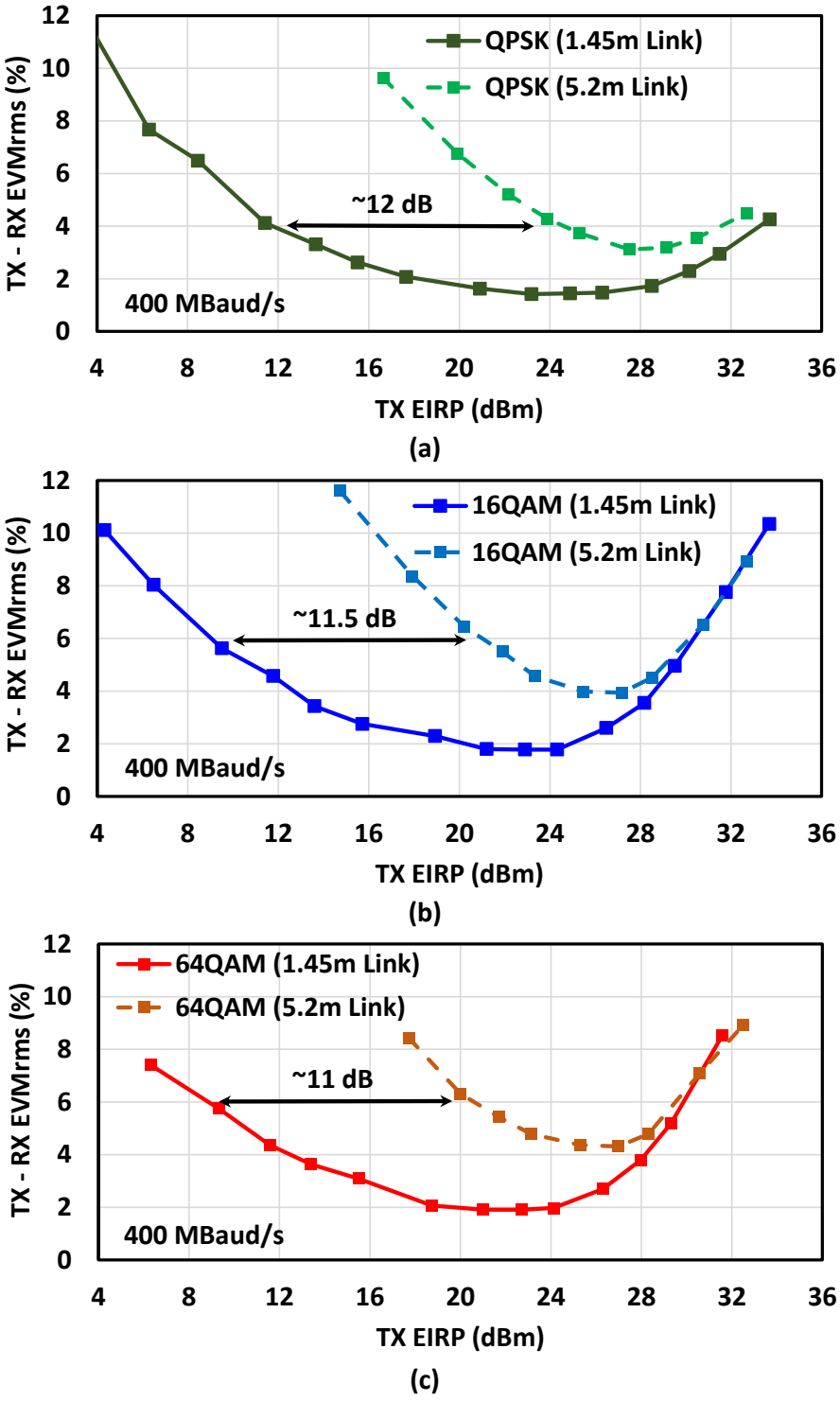


Figure 2.27. TX-to-RX Communication link EVM results versus TX EIRP for (a) QPSK, (b) 16QAM, (c) 64QAM signals.

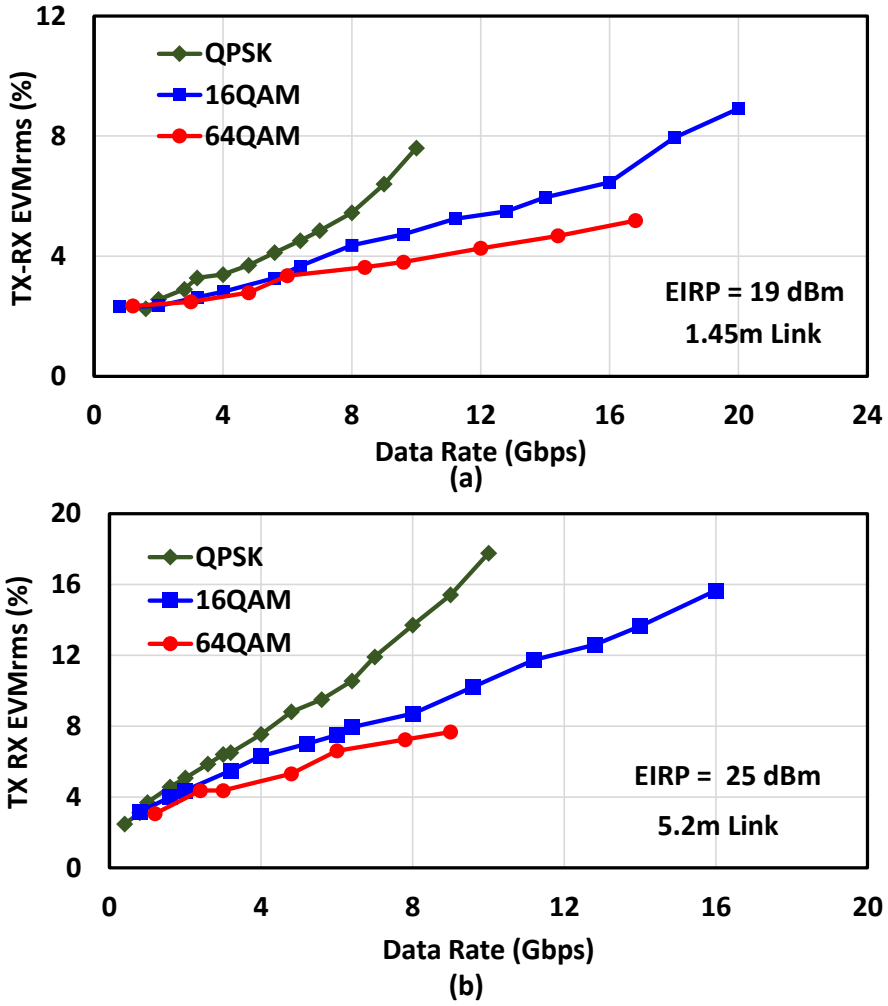


Figure 2.28. TX-to-RX Communication link EVM results versus data rate for (a) 1.45m link with 19 dBm EIRP, (b) 5.2m link and 26 dBm EIRP.

the EVM is limited by the TX array linearity, hence, both links have similar performance. A minimum EVM of ¡2% and 4% is achieved for the 1.45m and 5.2m communication distances for all modulations data types (QPSK, 16- and 64-QAM) at EIRP of 22 dBm (1.45m link) and 26 dBm (5.2m link).

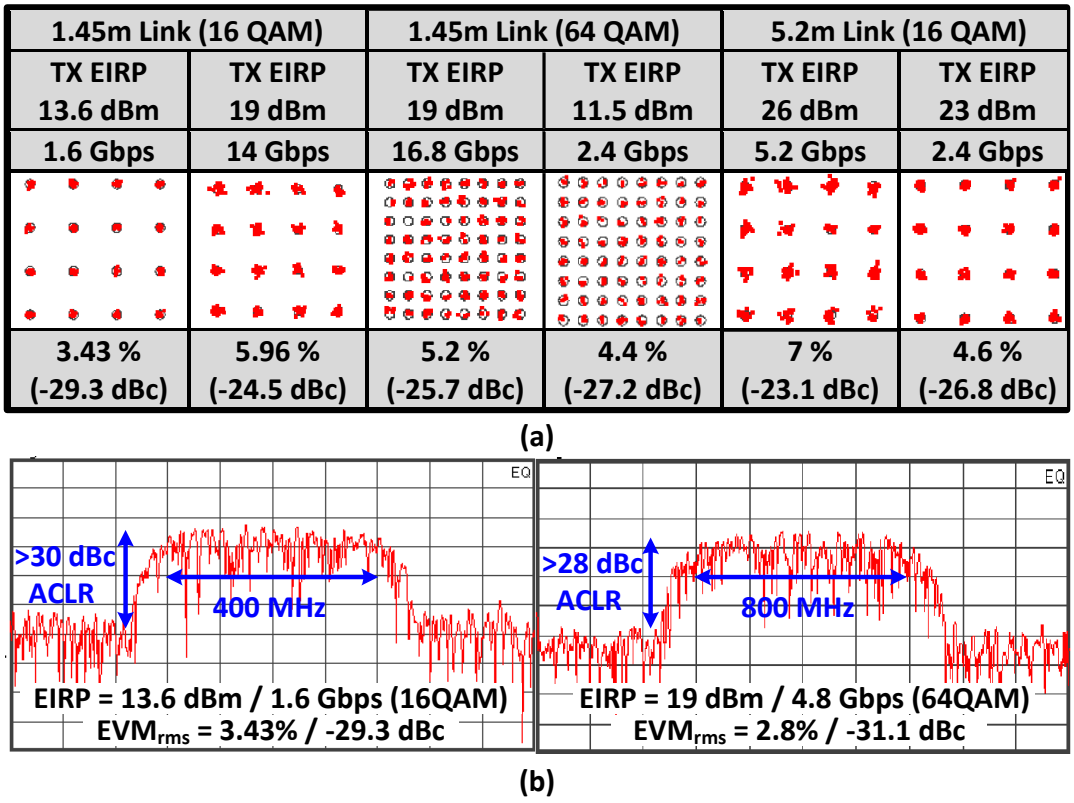


Figure 2.29. TX-to-RX Communication link EVM results versus data rate for (a) 1.45m link with 19 dBm EIRP, (b) 5.2m link and 26 dBm EIRP.

2.10.2 TX-RX link EVM versus datarate

The measured rms EVM versus data rate for the TX-RX links is summarized in Fig. 2.28. A maximum data rate of 20 Gbps (16QAM) and 16 Gbps (16QAM) for the 1.45m and 5.2m respectively is achieved with an EVM of 10% and 16%.

2.10.3 TX-RX link constellations and spectrum

The measured TX-RX link output demodulated constellations and spectrum are presented in Fig. 2.29 for different TX EIRP values, link distanced (1.45m and 5.2m) and modulation schemes (16- and 64-QAM). An ACLR of more than 28 dBc is maintained for 64-QAM modulated signal with 4.8 Gbps and 19 dBm EIRP.

2.10.4 TX-RX link analysis at 25 dBm

The detailed EVM analysis of the TX-RX communication links at 25 dBm EIRP and 0.4Gbauds/s rate is presented in Table 2.1. With a measured TX EIRP gain of 44 dB and cable loss of 4 dB, the output signal power from the AWG is -15 dBm. The SLF is 78.6 dB and 89.7 dB at 1.45m and 5m links respectively. The receiver directivity, measured RX electronic gain, and external amplifier gain (including cable loss) are 23.6 dB, 20 dB and 16 dB respectively. Therefore, the signal power at the DSO input port is 6 dBm and -5.1 dBm for both links respectively. The total noise power spectral density levels at the DSO port are -118.6 and -120.8 dBm/Hz for 1.45m and 5m links. This includes the noise from the AWG (-147 dBm/Hz), TX EIRP noise, RX noise, and DSO noise (NF of 30 dB). Therefore, the total SNR (EVM) due to thermal noise at the DSO is 39.4 dB (1.07%) and 31 dB (2.81%) for both links respectively.

Note that, for all power level calculations, the measured TX and RX gains are used, except for the TX and RX noise contributions. Their noise values used are based on the simulated TX and RX array gains (Fig. 16). This calculates the upper limit of the TX and RX arrays thermal noise contribution. Each of their noise contributions would be at best around 4 dB lower if the measured gains are used (Fig. 16).

The phase noise contribution of the LO signal is calculated to be 1.9% for 0.4GBaud/s signal. This includes the effect of the LO x6 multiplier and the fact we are adding PN twice (at TX and at RX). Therefore, the total EVM for both links can be calculated using:

$$EVM_{tot} = \sqrt{EVM_{SNR}^2 + EVM_{LO}^2} = 2.18\% \; and \; 3.39\% \tag{2.14}$$

The corresponding measured EVM values are 2.2% and 4% for 1.45m and 5.2m links respectively. This slightly higher EVM can be due to misalignment between TX and RX array leading to less power reaching the RX array and hence lower SNR.

The array can operate at further away communication distances based on the measurement

Table 2.1. TX-TO-RX LINK SYSTEM ANALYSIS

TX-RX Link Distance (m)	**1.45**	**5.2**
Modulated signal Level		
AWG average signal power (dBm)	-15	
Cable loss (dB)	4	
TX Array input IF power (dBm)	-19	
TX array EIRP Gain (dB)	44	
TX peak signal EIRP (dBm)	37.5/32.5 at Psat/P1dB	
TX signal EIRP (dBm)	25	
SLF @140 GHz (dB)	78.6	89.7
RX array antenna directivity (dB)	23.6	
RX array Pinc (dBm)	-30	-41.1
RX electronic gain (dB)	20	
Cable + external LNA gain (dB)	16	
Signal power at DSO (dBm)	6	-5.1
AWG Noise Level		
At AWG output (dBm/Hz)	-147	
At DSO input (dBm/Hz)	-126	-137.1
TX Array Noise		
Radiated Noise EIRP (dBm/Hz)	-106	
At DSO input (dBm/Hz)	-125	-136.1
RX Array Noise		
At PCB IF output (dBm/Hz)	-138.5	
At DSO input (dBm/Hz)	-122.5	
DSO Noise		
DSO NF (dB)	30	
DSO noise floor (dBm/Hz)	-144	
Total Noise		
Total noise floor at DSO (dBm/Hz)	-118.6	-120.8
Total noise over 0.4GHz BW (dBm)	-32.6	-34.7
Wireless Link SNR and EVM		
SNR/EVM at DSO (dB)	39.4	31
SNR/EVM at DSO (%)	1.07	2.81
EVM due to LO PN (%)	1.9	
Total EVM for 16-QAM 0.4Gbaud/s (%)	2.18	3.39
Mea. EVM for 16-QAM 0.4Gbaud/s (%)	2.2	4

above (EIRP of 25 dBm, 0.4 GHz BW, 16-QAM, 5.2m distance and EVM/SNR of 4%/28dB). If the EIRP is increased by 4 dB (29 dBm and 3.5 dB back-off) and the EVM spec is taken to be 10% (20 dB SNR) for 16-QAM signal. Then, noting that the EVM will be mainly limited by the receive array SNR, the SLF can be increased by a factor of 12 dB. Hence, the 64-element phased-array TX-RX system can operate at 21-m link with data rate of 1.6 Gbps using 16-QAM signal. Alternatively, at a higher data rate of 12 Gbps, the system can operate at around 7-7.7-m link.

Table 2.2 shows the performance comparison with the state-of-the-art arrays at D-band. This demonstrates the largest wafer-scale array at D-band with full 2-D scalability. The reported TX EIRP (37.5 dBm) is the highest reported for silicon technologies to-date. The scanning range achievable by this work is the widest reported in both H- and E-planes ($\pm 60^o$ in the H-plane and $\pm 38^o$ in E-plane. The array consumes 170mW/element and 105mW/element for TX and RX operations respectively.

2.11 TX-RX Radar Measurements

The array is used in a frequency modulated continuous wave (FMCW) imaging systems at 140GHz. The FMCW system block diagram is shown in Fig. 2.30. Two TRX arrays are used in this system configuration (one as TX and one as RX). A Keysight AWG is used to feed the LO port of each array with an FMCW signal having a frequency span Δf_{in} in a time interval T_b. The on-chip x6 LO frequency multiplier then translates the output frequency span to $\Delta f_{RF} (= 6 * \Delta f_{in})$. The IF port of the TX array is fed with a CW tone at 11GHz using Kesight PSG. The transmitted signal reflects from a metal sphere at a distance R (Fig. 2.30), then, is detected by the RX array and mixed with the transmitted signal. The round-trip delay of the signal causes a constant frequency shift between the transmitted and received signals. Hence, when both signals are mixed, the output frequency at the IF port of the RX array will be 11GHz$\pm f_b$, where f_b is the beat frequency and, for a stationary target, is given by [30]:

Table 2.2. Comparison With the State-of-the-Art D-band Phased Arrays

	This Work		**[3]JSSC 2022**	**[8]JSSCC 2022**	**[7]RFIC 2020**		**[1]TMTT 2022**
Technology	45nm RFSOI		45nm RFSOI	45nm RFSOI	130-nm SiGe		22FDX + InP
# of Elements	63 (8x8)		8 (4x2)	8 (4x2)	8	8	8 (8x1)
Transmit/Receive	TX+RX		TX Only	RX Only	TX Only	RX Only	TX only
Beamforming Arch.	RF		IF	IF	RF	RF	Digital
Frequency (GHz)	137.5-145	135-142.5	136-147	139-155	130-170	130-170	135
TX EIRPsat (dBm)	37.5	N/A	32	N/A	N/A	N/A	38.5
TX Peak Gain (dB)	44	N/A	21	N/A	16	N/A	N/R
RX Peal Gain (dB)	N/A	20	N/A	27.5	N/A	22	N/A
PDC/element (mW)	170	105	230	145	330	165	760
Scan plane 1(^{o})	±60		±30	±35	Not Specified		±7
Scan plane 2(^{o})	±38		Not Specified	Not Specified	Not Specified		N/A
Chip-Antenna Package	Antenna In Package		Quartz Superstrate		Radio-on-glass		LTCC Interposer
OTA Communication (Data Rate (Gb/s))	22 (16-QAM) 24 (64-QAM)		16 (16/64-QAM)	10 (16-QAM) 9 (64-QAM)	N/A		3 (16-QAM)

$$f_b = \frac{2R}{c} * \frac{\Delta f_{RF}}{T_b} \tag{2.15}$$

where c is the speed of light. The range resolution (ΔR) of the radar is given by [30], [31]:

$$\Delta R = \frac{c}{2\Delta f_{RF}} \tag{2.16}$$

For TX EIRP of 32.5dBm, a target range (R) of 130cm and a 5cm diameter metal sphere with a radar cross section (σ) of $0.002m^2$, the space loss factor is calculated as [32]:

$$L = 10log(\frac{\lambda^2 * \sigma}{(4\pi)^3 R^4}) = -118dB \tag{2.17}$$

In this case, the received power at the UXA port is:

$$P_{R130cm} = EIRP + L + D_{RX} + G_{RX} + L_{cable} = -46dBm \tag{2.18}$$

The calculated noise floor at the UXA port including the RX array noise is -95dBm in a 100KHz bandwidth and -105dBm in a 10KHz bandwidth. This yields a calculated SNR¿10dB up to 12.5m and 22m target ranges for integration bandwidth of 100KHz and 10KHz, respectively, as shown in Fig. 2.31. Both of these target ranges are adequate for imaging applications.

2.11.1 Radar Measurements

Fig. 2.32 shows the FMCW radar demonstration setup at 140GHz. First, one sphere, with 5cm diameter, is placed at different range distances (R) and the received power and beat frequencies (f_b) are calculated and measured as shown in Fig. 2.33(a) and (b). In this measurement, the LO chirp signals (20.75-21.25GHz) are generated using Keysight M8195A with ramping speed of 200 MHz/μs ($T_b = 2.5\mu s$). Only one channel of the AWG is used along with a balun to feed both the TX and RX arrays. This ensures LO synchronization between

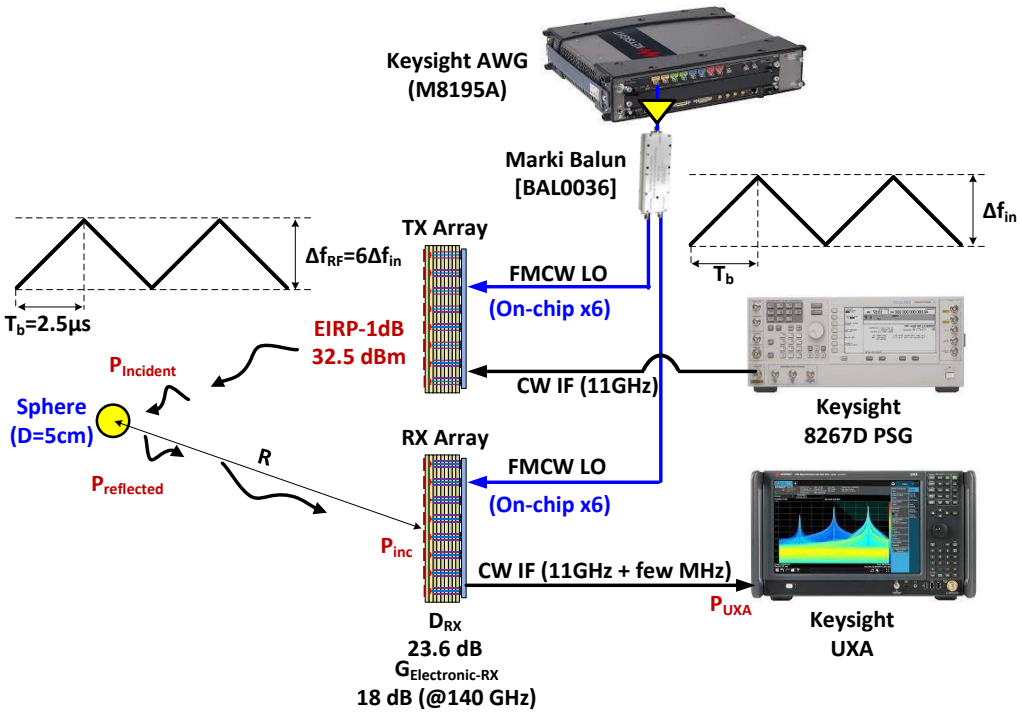


Figure 2.30. (a) 140 GHz array board top view, (b) Array board bottom view showing antenna array, (c) TRX die photo, (d) measured TX EIRP and electronic scanning performance.

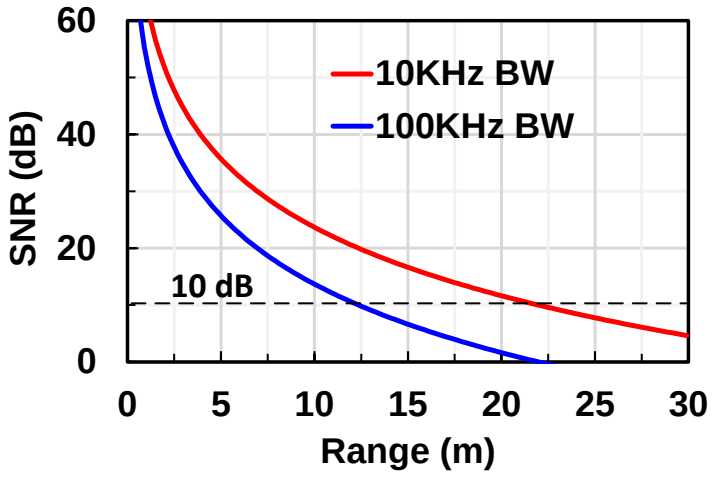


Figure 2.31. Calculated SNR vs. target range at 140GHz.

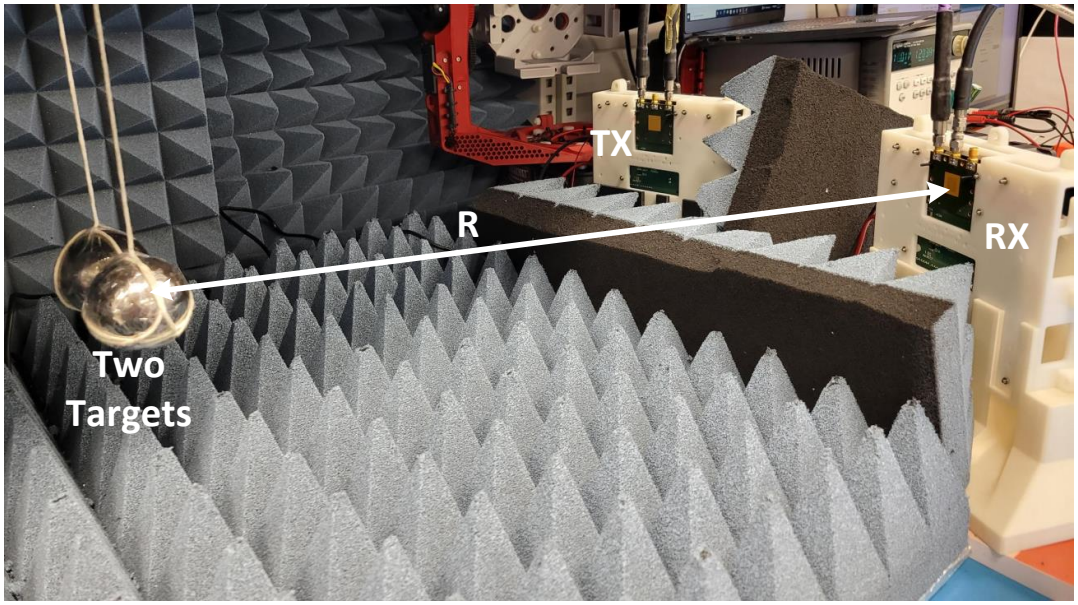


Figure 2.32. Picture of the 140 GHz FMCW radar setup.

both arrays. The measured received power and beat frequency match well the calculated values (Fig. 2.33(a) and (b)). Next, the sphere is placed at R=41cm and the RX array is electronically scanned from -60^o to 60^o and the measured received normalized power is shown in Fig. 2.33(c). This demonstrates that the imaging system can detect object distances as well as angles with respect to the RX array broadside.

Two spheres are then placed at about R=52cm and the separation between both spheres (ΔR) is reduced from 20cm to 5cm. Where 5cm is the minimum allowable for this setup due to the sphere diameter of 5cm. In this setup, the LO chirp signals generated by the AWG is between 20.25-21.75GHz with a ramping speed of 600MHz/μs ($T_b = 2.5\mu s$). This translates to $\Delta f_{RF} = 9GHz$ and range resolution $\Delta R = 1.67cm$. The measured scaled and processed IF spectrum around 11GHz is shown in Fig. 2.34 for both spheres placed as the target. The peaks in the spectrum represents the two spheres. For reference, one measurement is conducted with only one sphere placed in front of the radar. It is clear from the measurements that one peak is always fixed (for the first fixed sphere) and the second peak moves according to the separation of

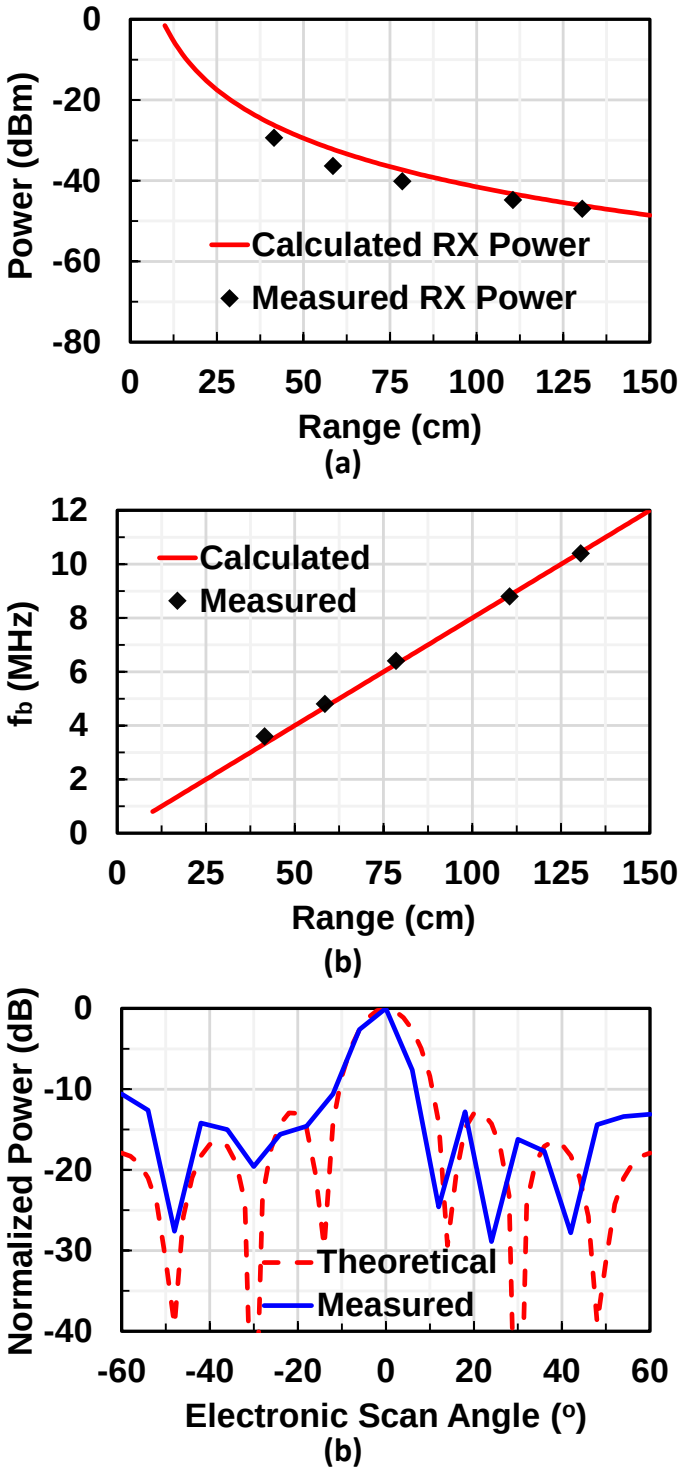


Figure 2.33. Measured and calculated for one sphere target (a) received power versus target range, (b) beat frequency versus target range, (c) normalized received power across RX array electronic scan angles.

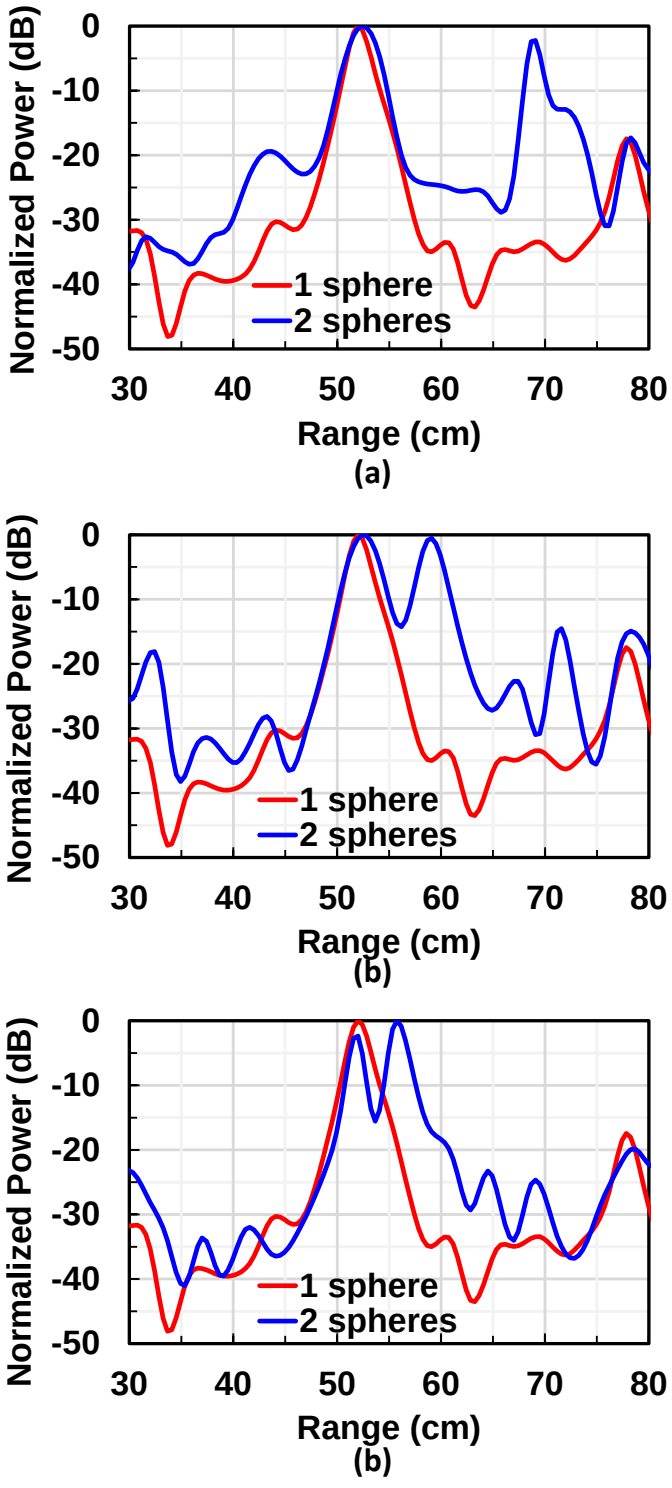


Figure 2.34. Measured normalized and processed IF spectrum for two sphere targets with separation of (a) 17cm, (b) 8cm, (c) 5cm.

the second sphere. At the minimum separation of 5cm, the measurements shows two clear peaks with R=52 and 56.2cm with a 14dB drop inbetween (Fig. 2.34(c)). With a smaller spheres, the imaging system should be a able to detect as small as 1.67cm range resolution.

2.12 Conclusion

This chapter demonstrated a scalable 2-D wafer-scale 8x8 transmit-receive phased array at 140 GHz. The work shows that low-cost silicon and, most important, low-cost packaging, can be used to build scalable phased-arrays at D-band. Also, while this array is built using an 8x8 chip, scalable low-cost topologies could be done using 4x4 or 16x16 chips.

Chapter 2, in full, has been submitted for publication of the material as it may appear in: A. Ahmed, L. Li, M. Jung, S. Li, D. Baltimas and G. M. Rebeiz, "140 GHz 2D Scalable On Grid 8x8 Element Transmit Receive Phased Arrays with Up/Down Converters Demonstrating 5.2m Link and Beyond," *IEEE Trans. Microw. Theory Techn.* and A. Ahmed, L. Li, M. Jung and G. M. Rebeiz, "A 140 GHz FMCW Imaging System Utilizing 8x8 Transmit-Receive Phased Arrays with Integrated x6 LO Multipliers," *IEEE IMS*. The dissertation author was the primary investigator and author of these materials.

Chapter 3

An 8-30 GHz High Linearity Passive Harmonic Rejection Mixer in 45nm CMOS SOI

3.1 Introduction

Wideband and high frequency receivers are being popularly used nowadays because they allow fast time to market products as well as ease of use in several products. In addition, wide-band, high performance circuits save development resources when being used in several products and prototypes. However, such wide-band receivers face several challenges in terms of received signal quality due to the presence of the close-in and harmonic blockers. These blockers cause gain desensitization, harmonic folding and intermodulation products that will eventually degrade the desired signal SNR and, hence, the overall communication link. One way to alleviate this challenge is to use a heterodyne architecture along with channel selection filters. However, unfortunately, this implementation is usually area inefficient and power hungry and, hence, increases the cost of the overall link.

The key block in receiver performance is the mixer because of LO harmonic mixing with the out-of-band blockers resulting in mixing products which fall into the desired signal band (Fig. 3.1). In addition, there are also intermodulation products of the in-band blockers that can fall into the desired band as well. One technique used to enhance the mixer performance is the

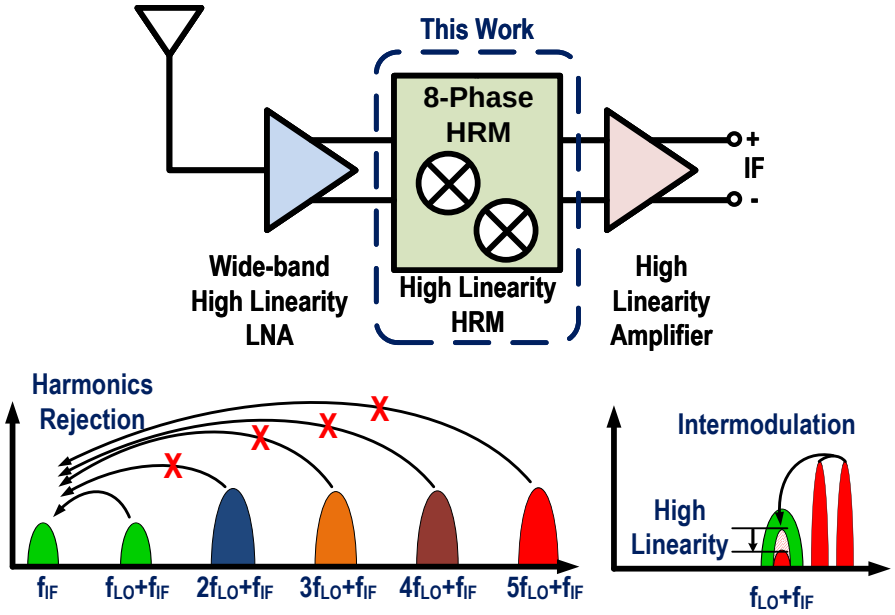


Figure 3.1. Harmonic rejection and high linearity mixer.

harmonic rejection mixing. In this case, the interferers at specific LO harmonics are cancelled. This is done by generating an effective LO waveform with ideally no specific harmonic contents [33]. Typically, an N-phase clock is generated, several mixer cells are used, and the mixer paths are scaled differently for the different LO paths [33]–[35].

Traditionally, the scaling operation in the harmonic rejection mixer (HRM) is done using active amplifiers or transconductance (Gm) cells. This allows for amplification (rather than loss) in the down-conversion operation and, most importantly, provides inherent RF isolation between the different clock-phase paths [34]–[43]. However, using an active implementation greatly reduces the mixer's in-band linearity performance resulting in distortion performance challenges for wide-band operation.

Recently, passive implementations for the harmonic rejection operation have been demonstrated in [44] and [45]. In these implementations, resistive amplitude scaling is used in the different mixer cells (rather than active amplification). Both passive designs achieve significantly enhanced linearity performance when compared to the Gm-cell implementations while maintain-

ing a high harmonic rejection of >35 dBc. In [44], a rejection of the 3^{rd} and 5^{th} harmonics up to 6 GHz is achieved using an 8-phase mixer. In [45], even higher (7^{th} and 6^{th}) harmonics are rejected using a 16-phase mixer with operation up to 3 GHz.

All state-of-the-art active and passive harmonic-rejection mixers have a limited operation frequency of up to 6 GHz. This is mainly due to the N-phase clock division and generation circuits. Typically, to generate N non-overlapping clock phases at f_{LO}, an input frequency of N/2*f_{LO} is required. This N/2*f_{LO} passes through divide-by-N/2 circuits to generate N different overlapping output phases at f_{LO}. Then, digital logic AND gates are used to generate the non-overlapping phases required for the mixer operation. The final duty cycle of the output phases is 100%/N. For example, for 8-phase operation, it is required to use a 4*f_{LO} input, and the final required duty cycle is 12.5% for non-overlapping clocks. The required high LO frequency at the input, and the required sharp edges for the small duty cycle phases at the outputs, make the operation of the clock generation circuits very challenging and results in high power consumption when the frequency (f_{LO}) or the number of phases (N) becomes high. This is the main reason why the above implementations are usually limited to 6 GHz.

One technique presented in [46] employs 4-clock phases (25% duty cycle) to operate an 8-phase N-path mixer (originally 12.5% duty cycle) and hence relaxes the clock dividers and non-overlapping clock generation circuits with operation up to 6.5 GHz. This is achieved by using interleaved inductors in the mixer RF network to provide a certain degree of isolation between the mixer cells, hence, allowing some LO overlapping. This technique can be used at higher frequencies, however, generating 25% duty cycle clocks is still challenging at >10 GHz operation.

An IQ mixer was demonstrated in [47] where non-overlapping 25% clock phases at 20-30 GHz are used. The idea is to use passive quadrature signal generation circuit for the overlapping 4 clock phases, followed by a transmission gate switch driven by the adjacent clock phases, hence, generating non-overlapping clock phases at mm-Wave frequencies. Unfortunately, a harmonic rejection mixer requires 8-phases for the LO (12.5%), and in order to implement this

technique, one needs complex LO routings and a cascade of transmission gates, which is very challenging at 8-30 GHz.

This chapter presents a novel technique to enable mm-wave operation of 8-phase harmonic rejection mixers without the need for N/2* f_{LO} to generate N phases [4], by employing wideband polyphase networks. Furthermore, it enables the use of overlapping 50% square-wave (or sine-wave) clock phases instead of the 12.5% overlapping clocks while still maintaining a high harmonic rejection.

This chapter is divided as follows: Section 3.2 discuses the concept of operation of the harmonic rejection mixers along with some intuitive and mathematical analysis. Section 3.3 shows the block diagram of the proposed circuit as well as detailed circuit and simulation details of the work. Section 3.4 presents the measurement results and Section 3.5 concludes the chapter.

3.2 Harmonic Rejection Concept

3.2.1 Harmonic Rejection

The concept of harmonic rejection is shown in Fig. 3.2(a). Four different vector weightings are applied to the RF signal and the output is the summation of the weighted signals. In addition, the phase shift of the weightings is harmonic dependent. Meaning that, at the fundamental frequency (n=1), the four phases are 0^o, 45^o, 270^o and 315^o whereas at the third harmonic (n=3), the phases are 0^o, 135^o, 90^o and 225^o and so on (Fig. 3.2(a)). In this case, the 3^{rd} and 5^{th} harmonics are vectorially cancelled while the input signal is vectorially added (with a small hit in gain), thus achieving harmonic rejection for the third and fifth harmonics. The phase factor is realized in the mixer cells and the gain factor is realized as resistive attenuation (rather than gain) to allow for a passive implementation. Note that when the mixer is driven by square wave LO signals, the required harmonic dependent 'n' factor in the phase shift is realized naturally. This is because, the square wave will have a harmonic dependent phase shift in its Fourier expansion.

Ideally, one can use a pure LO sinusoidal signal to achieve perfect harmonic rejection.

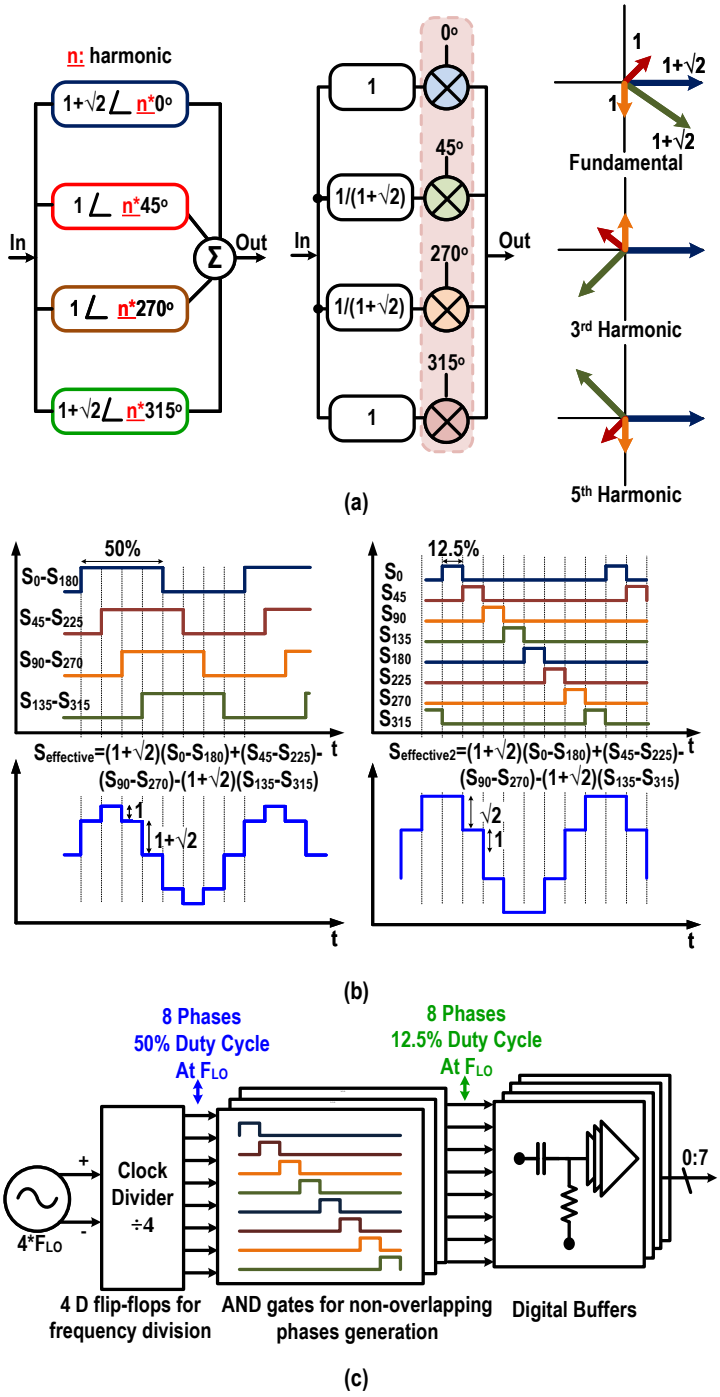


Figure 3.2. (a) Harmonic dependent vector weightings applied to the input using mixer cells and the vector sum at different harmonics, (b) Constructing 3^{rd} and 5^{th} harmonic-free signal using square-waves and 50% and 25% duty cycles, (c) Traditional 8-phase clock generation.

However, the on and off switching characteristics of the mixing transistors will still have a near square-wave shape, and therefore, the harmonic rejection will be similar to the square-wave LO case (-10 dB at 3^{rd} harmonic, -15 dB at 5^{th} harmonic).

Figure 3.2(b) presents the required LO phases for harmonic rejection, where S_0 to S_{315} represent signals of eight different phases of the same frequency ω. If 50% square-wave LO signals are used, the effective constructed LO signal after vector addition of the eight phase-shifted signals is shown in Fig. 3.2(b), $S_{effective}$, and is given by:

$$\begin{aligned} S_{effective} = (1+\sqrt{2})(S_0 - S_{180}) + (S_{45} - S_{225}) - \\ (S_{90} - S_{270}) - (1+\sqrt{2})(S_{135} - S_{315}) \end{aligned} \tag{3.1}$$

The amplitude weightings (1 and 1+$\sqrt{2}$) are used to mathematically get a 3^{rd} and 5^{th} harmonic-free signal $S_{effective}$. Expanding all the square-wave signals S_0 to S_{315} using Fourier series and adding them together, ignoring harmonics above the 5^{th}, we get:

$$S_{effective} = \frac{4}{\pi}[(1+\sqrt{2})sin(\omega t) + cos(\omega t)] \tag{3.2}$$

The effective signal, ideally, has no 3^{rd} and 5^{th} harmonic content, and a perfect 3^{rd} and 5^{th} harmonic rejection can be achieved in the mixer operation. Unfortunately, if 50% duty cycle signals are used for driving passive mixes, several mixer cells will be turned on at the same time, resulting in degraded performance. One way to overcome this is to use non-overlapping clock phases (12.5% duty cycle) to drive the mixers (Fig. 2(b)). In this case, only one switch will be on at a time and switch-to-switch isolation is achieved. In short, the isolation is achieved on the LO side. Note that, with a similar vector sum as in (3.1), addition of 12.5% duty cycle waveforms result in $S_{effective2}$ (see Fig. 3.2(b)) that does not contain 3^{rd} and 5^{th} harmonic signals.

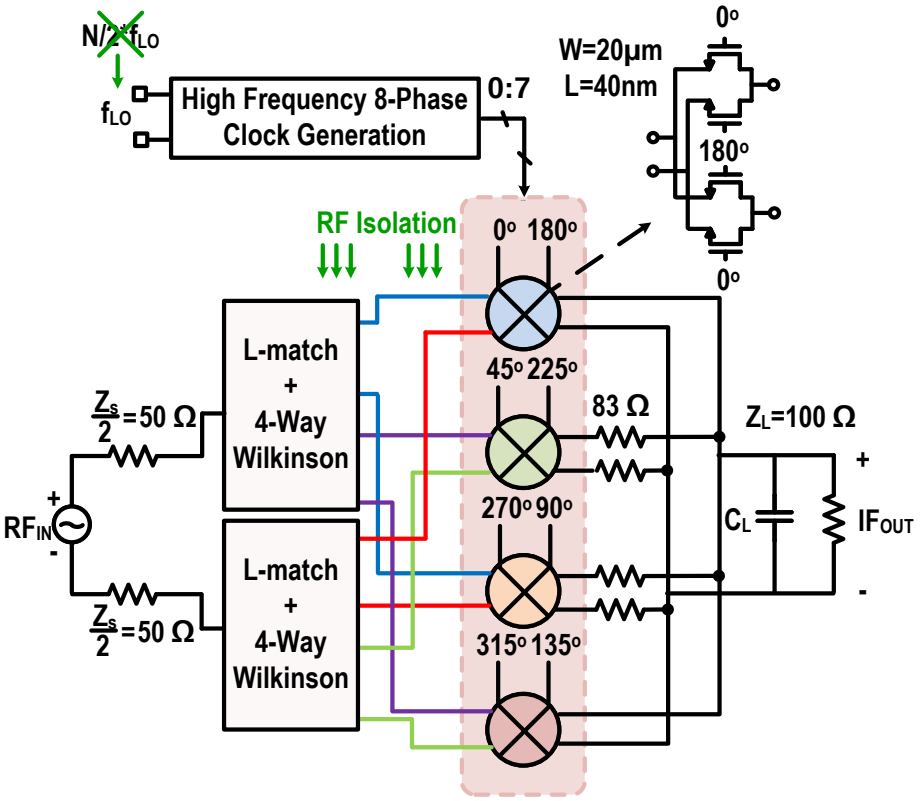


Figure 3.3. Block diagram of high linearity HRM.

3.2.2 Traditional N-Phase Generation

Figure 3.2(c) presents the traditional implementation for generating 8 different clock phases [44], [45]. A 4*f_{LO} is needed, together with /4 flip-flop circuits to generate the outputs at FLO with 50% duty cycle phase. The clock phases are then logic AND gated with the correct combinations and 12.5% 8-phase non-overlapping clocks are achieved. These circuit are not suitable for operation at 30 GHz because, first, the 12.5% duty cycle pulses will be 4.16ps which is comparable to the AND logic cells rise, fall, and hold times. Also, the 12.5% pulses require high frequency switching which is limited by the transistor performance and parasitic capacitances. Second, even for 50% LO phase generation, the clock dividers need to operate at an input frequency of 120 GHz for a /4 operation, and current mode dividers must be used at high power consumption [48].

3.3 Harmonic Rejection Implementation

3.3.1 Block Diagram

The novel mm-wave high-linearity HRM is shown in Fig. 3.3 and incorporates several new concepts [4]. First, the clock phase generation is done using passive polyphase filers to avoid using high frequency input signals and clock dividers. Passive mixer cells are used for high linearity operation. The clock phases are 50% duty cycle instead of 12.5% for low power and mm-wave operation, and isolation between the mixer cells is provided on the RF side using a 4-way Wilkinson network.

3.3.2 8-Phase Clock Generation

Figure 3.4 presents the 8-phase clock generation circuit. The first stage is an inverter with resistitve feedback and 50 Ω resistor to ground for wideband matching. Next, a two-stage polyphase filter (PPF) is used to generate 4 quadrature signals with a voltage loss of 7.3 dB at 20 GHz. Driver amplifiers are then used follwed by a phase interpolator based on a capacitve divider network to genrate 8 signals with 45^o phase difference from the 4 quadrature signals. Finally, 7-stage inverter amplifiers are used to generate square wave LO signals that drive the passive mixer cells.

The first driver stage details and simulation results are shown in Fig. 3.5. The gain is -6 to -8 dB when loaded with the RCCR network and the output voltage waveform is kept sinusoidal across frequency for an input power of 0 dBm.

The two-stage passive RCCR polyphase filter circuit is shown in Fig. 3.6(a) [49]–[52]. Center frequencies of each stage are 9 and 22 GHz, respectively, to widen the bandwidth of the IQ match and achieve the best harmonic rejection possible. Figure 3.6(b) presents the simulated phase and gain mismatches between the I and Q differential output signals and a comparison with a single-stage PPF tuned at 20 GHz. The IQ balance is presented in Fig. 3.6(c) and is given

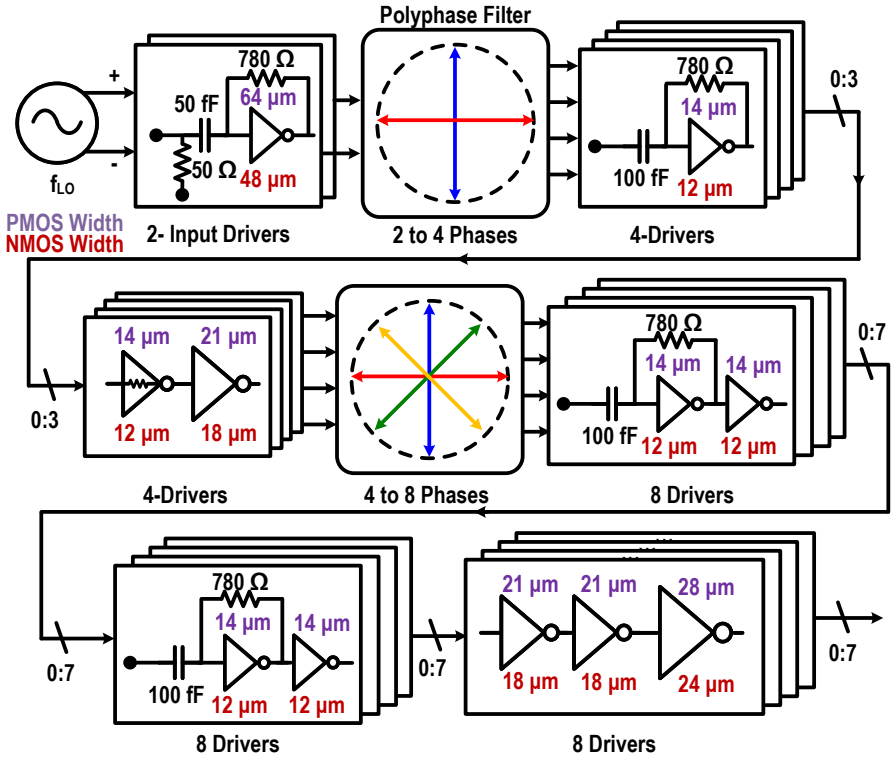


Figure 3.4. LO generation for 8-phase 50% overlap clocks.

by:

$$IQ\ Balance = 10log(\frac{4}{\varepsilon^2 + \Delta\theta^2}) \tag{3.3}$$

where ε represents the amplitude mismatch (linear) and $\Delta\theta$ represents the phase mismatch (radians). The design was optimized such that the IQ balance is better at the lower frequencies within the band of interest (8-30 GHz). This is done since the 3^{rd} harmonic of a signal at 8 GHz is at 24 GHz and will pass by the LNA in the wideband receiver system. In this design, C_1 and C_2 are 50 fF and 70 fF, respectively, while R_1 and R_2 are 136 Ω and 300 Ω, respectively. Note that, values used for the resistors and capacitors take into consideration the loading and parasitic effects.

One key point in the design is the placement of the polyphase filter within the LO chain as the signal driving the polyphase filter should be sinusoidal and not square wave. The reason is that the polyphase filter has a frequency dependent response, and with square-wave inputs, the

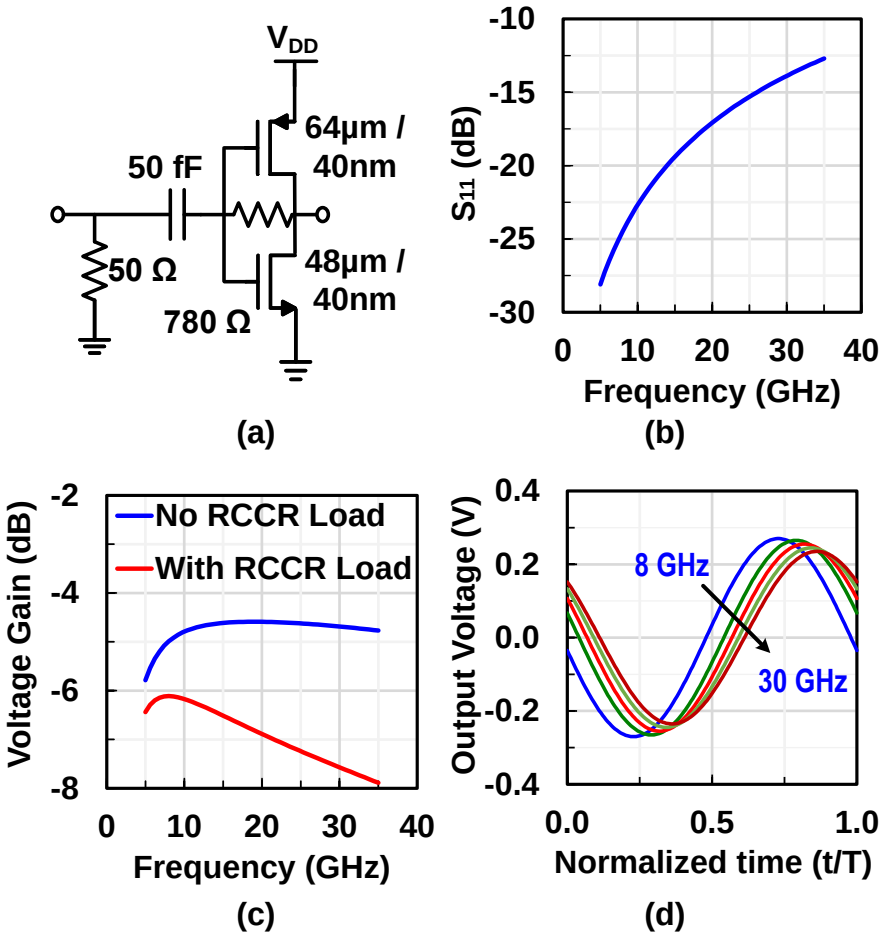


Figure 3.5. First driver stage details and simulations results.

phase and gain at the 3^{rd} and 5^{th} harmonic will be distorted. Therefore, the polyphase filter is placed after the 1st gain stage where the signal is still sinusoidal.

The phase interpolator capacitor divider circuit is used to generate the 8 output phases (Fig. 3.7(a)) [4]. The four inputs have phases of 0^o, 90^o, 180^o, and 270^o (In1 to In4), and for the output port ϕ_2 as an example, the gain and phase are given by:

$$\phi_2 = \frac{C_2}{C_2+C_2}(In1+In2) = \frac{1}{2}(1\angle 0^\circ + 1\angle 90^\circ) = \frac{1}{\sqrt{2}}\angle 45^\circ \tag{3.4}$$

The same applies for ϕ_4, ϕ_6 and ϕ_8.

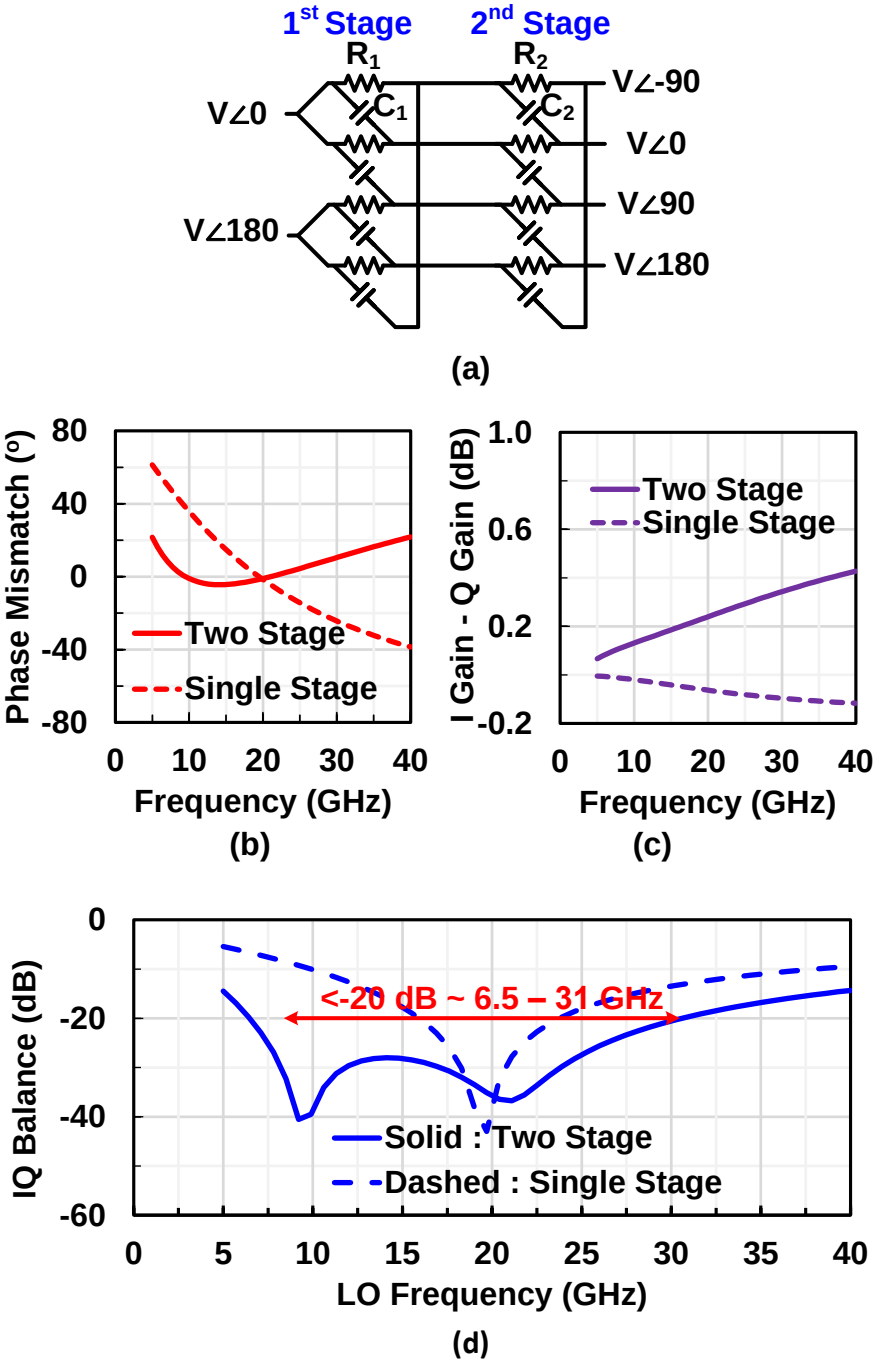


Figure 3.6. (a) Two-stage polyphase filter implementation, (b) phase and gain mismatches, (d) IQ balance.

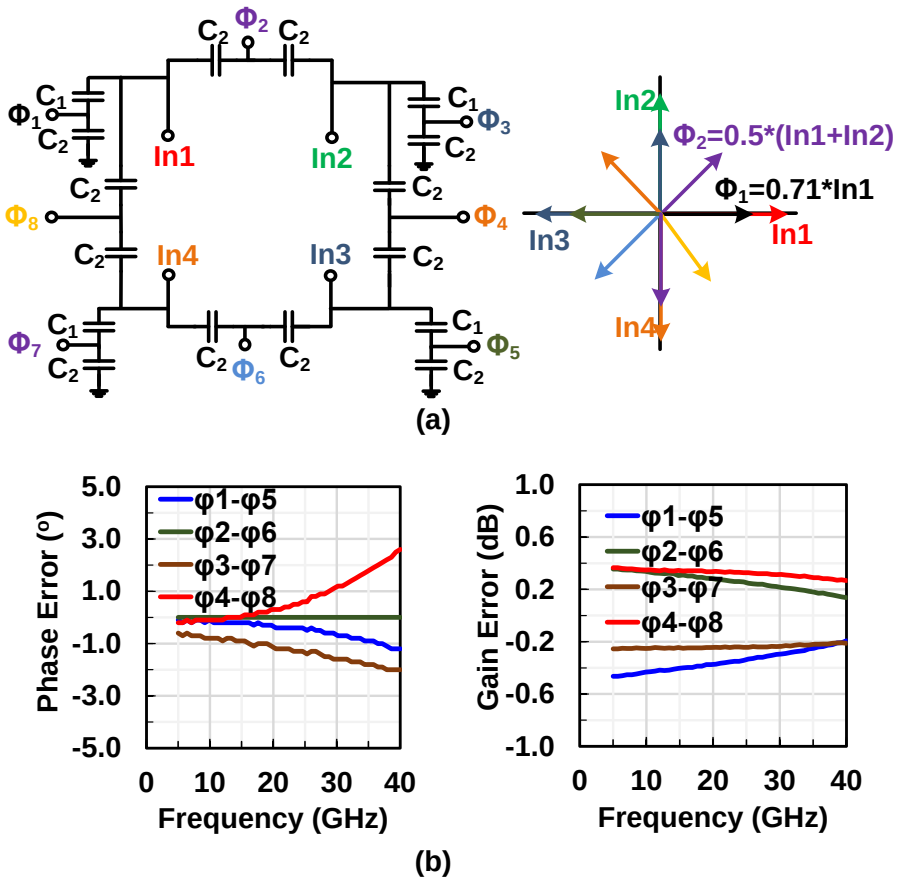


Figure 3.7. Generation of 8 phases from 4 phases (a) circuit implementation, (b) relative gain and phase errors between the outputs.

On the other hand, ϕ_1, ϕ_3, ϕ_5 and ϕ_7 are given by:

$$\phi_1 = \frac{C_1}{C_2 + C_1} In1 \tag{3.5}$$

one can calculate that the voltage divider between C_1 and C_2 should have a gain of $1/\sqrt{2}$. This is achieved by having a $C_1 : C_2$ ratio of 1:($\sqrt{2}$-1).

However, the loading capacitors attached to this capacitor divider network affect the ideal transfer functions, so the used values for C_1 and C_2 are 120 fF and 100 fF respectively, after the driver loading is taken into account. The simulated gain of the capacitor divider from one of the four inputs to one of the eight outputs is -6.5 to -9 dB at 8-90 GHz (third harmonic of 30

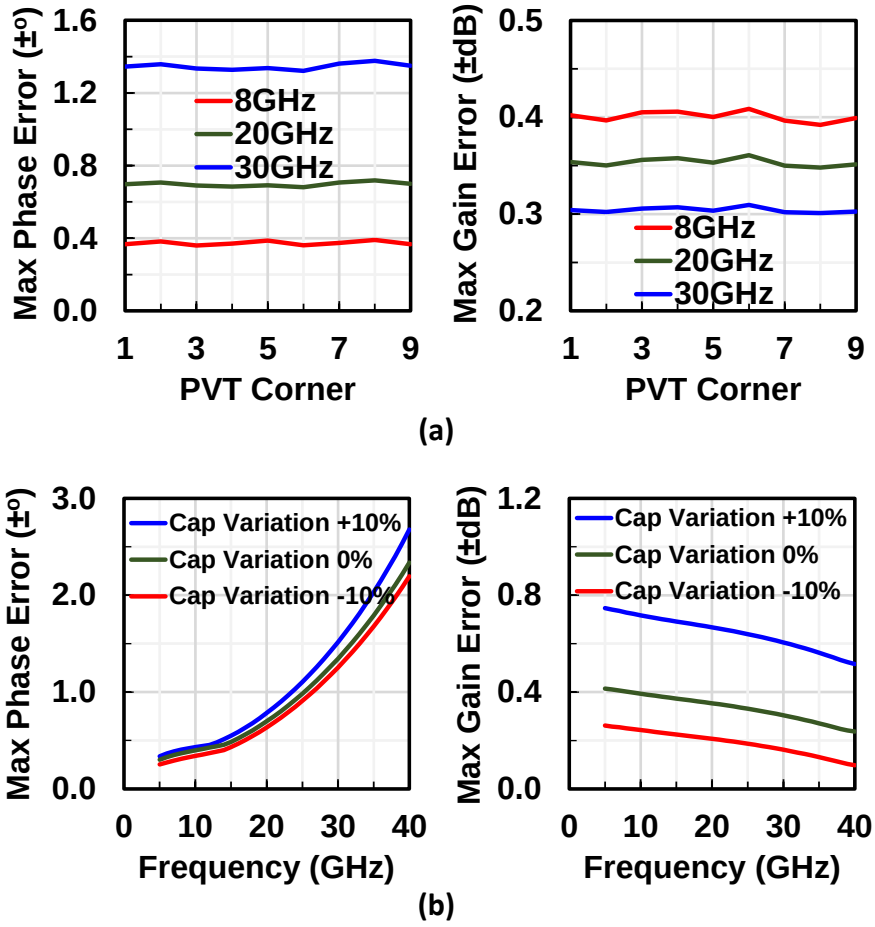


Figure 3.8. Generation of 8 phases from 4 phases (a) Maximum phase and gain variations across corners (TT, FF, SS, -20^o, 27^o and 100^o) (b) Maximum phase and gain variations across capacitor variation (±10%).

GHz). The simulated phase and gain errors are within ±4.2^o and ±0.4 dB, respectively at 8-30 GHz (Fig. 3.7(b)). Figure 3.8(a) shows minimal variation in the maximum phase and gain errors across temperature (-20^{o}C, 27^{o}C and 100^{o}C) and transistor process corners (TT, FF and SS) for the capacitor divider network and load inverters. Figure 3.8(b) presents the maximum gain and phase errors when varying the divider circuit capacitors values by ±10%.

The voltage gain for the LO network from the differential input port to the capacitive divider output ports is 1.8 dB to -16 dB at 8-30 GHz, and the LO signals are therefore amplified using 7-stage inverter-based buffers. The first and second blocks are based on a self-biased

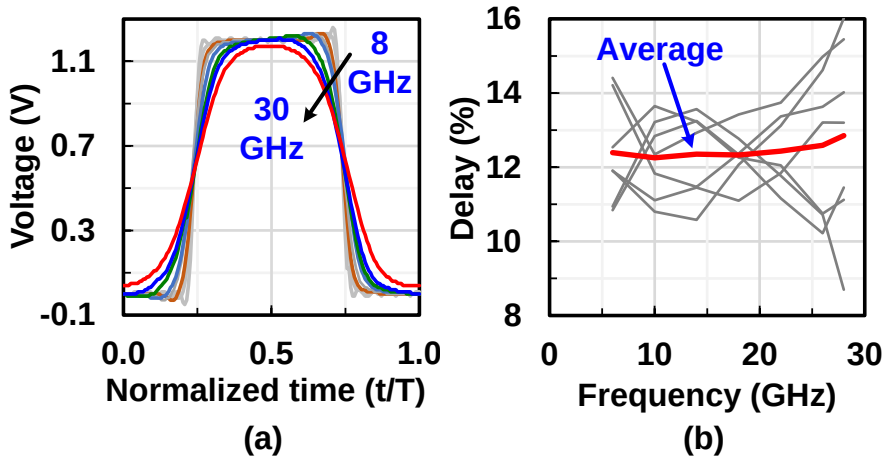


Figure 3.9. (a) LO drivers output waveform from 8 to 30 GHz, (b) delay between adjacent clock phases.

inverter followed by a regular inverter for achhieving highest voltage gain, while setting a stable operating bias point. The last four stages are digital in nature and have increasing buffer sizes for improved capacitive drive capabilities and reduced power consumption.

The simulated LO voltage gain is 50 dB at 8 GHz and decreases to 10 dB at 30 GHz. This insures that with an input LO power of 0 dBm, the mixer switches will be driven by rail-to-rail voltage swing at all frequencies. Note that no inductors are used in the LO network to save chip area, and hence the large gain difference between 8 and 30 GHz due to the RC frequency response of all the amplifier stages (see Fig. 3.4).

The final 8-phase LO waveforms at the mixer nodes are shown in Fig. 3.9(a). Note that only one waveform is shown out of eight in Fig. 3.9(a). At 8-24 GHz, the waveforms are near-ideal square-waves, but at 24-30 GHz the waveforms have less ideal square-wave waveform due to the relatively high rise and fall times (4.5 and 5.6 ps). This is because the 45RFSOI inverter response with a loading capacitor of 22 fF (mixer switches). The rise and fall time combined at 30 GHz are 34% of the LO period of 33ps, hence, the waveform is closer to a sine-wave than a square wave. Figure 3.9(b) presents the relative delay in percentage between

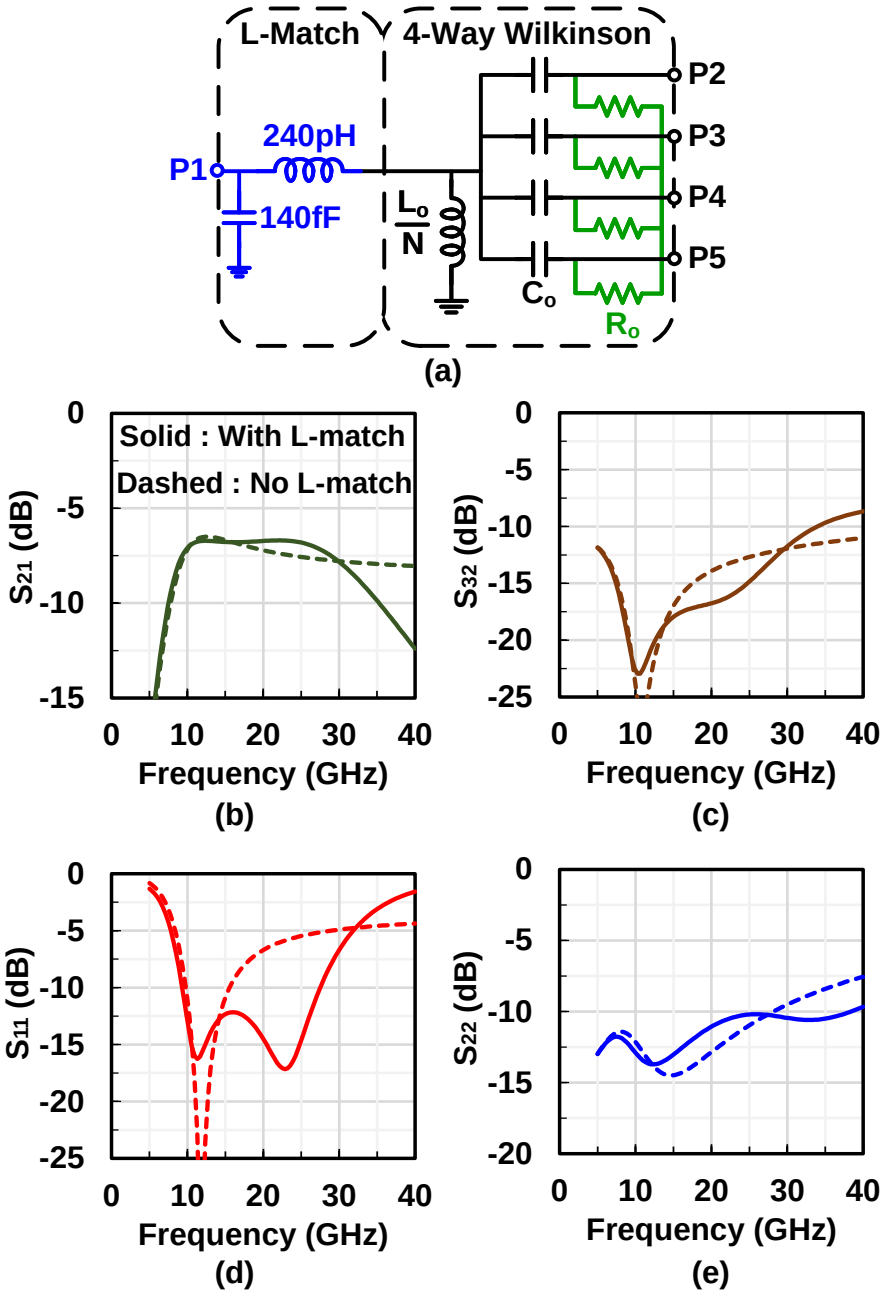


Figure 3.10. Simulated S-parameters for the 4-way Wilkinson network with the L-matching network.

any two adjacent phases as a ratio of the enitre period.. The required value is 12.5% for an 8-phase clock and the average delay is simulated to be 12.5% at 8-30 GHz, but with up to +/-3% of variation due to the IQ error in the polyphase and non-idealities in the capacitive divider

networks.

3.3.3 Input Matching, Wilkinson Dividers and Mixer Cells

A 4:1 Wilkinson network is used between the RF input port and the 4 mixer cells to provide mixer-to-mixer isolation while using 50% LO waveforms. This is implemented using a compact 4-way Wilkinson circuit with one shunt inductor to ground (Fig. 3.10) [53]–[55]. Also, an input L-matching network is added to enhance the input impedance bandwidth. Note that two single-ended Wilkinson networks are used at the input differential port (see Fig. 3.3) as it was found that this is easier to implement than a wideband differential 4:1 Wilkinson network.

The values of the Wilkinson inductor and capacitor are [23]:

$$\frac{L_o}{N} = \frac{1}{N}\left(\frac{\sqrt{N}R_o}{\omega_o}\right) \tag{3.6}$$

$$C_o = \frac{1}{\omega_0\sqrt{N}R_o} \tag{3.7}$$

where N=4 is the number of outputs and ω_o is the center frequency (f_o=12 GHz). In this design, the inductor (L_o/N) is chosen to be 360 pH to avoid self resonance at 30 GHz and the capacitor (C_o) is 160 fF.

The simulated S_{11} bandwidth is 10-15.5 GHz for the 4-way Wilkinson and improves to 9.3-27.5 GHz (3:1 BW) with the L-matching network. The simulated 1-dB bandwidth is 9-30 GHz with L-matching. The network's ohmic loss, not including the 6 dB division loss, is 0.73-1.8 dB at 9-30 GHz (including the L-match loss). The isolation between the Wilkinson output ports is $>$12 dB at 8-30 GHz and $>$15 dB at 9-25 GHz. In summary, with just two inductors and an area of 0.06 mm^2, a 3:1 bandwidth 4-way Wilkinson network can be implemented in RFSOI.

The mixer cells are double balanced passive implementations (Fig. 3.3), with differential inputs and outputs, hence, all even harmonics are rejected. The mixer size is a trade off between the On-resistance and the capacitance (NMOS gate capacitance). The smaller the transistor size, the smaller the LO driver power consumption at the expense of more conversion loss (Fig.

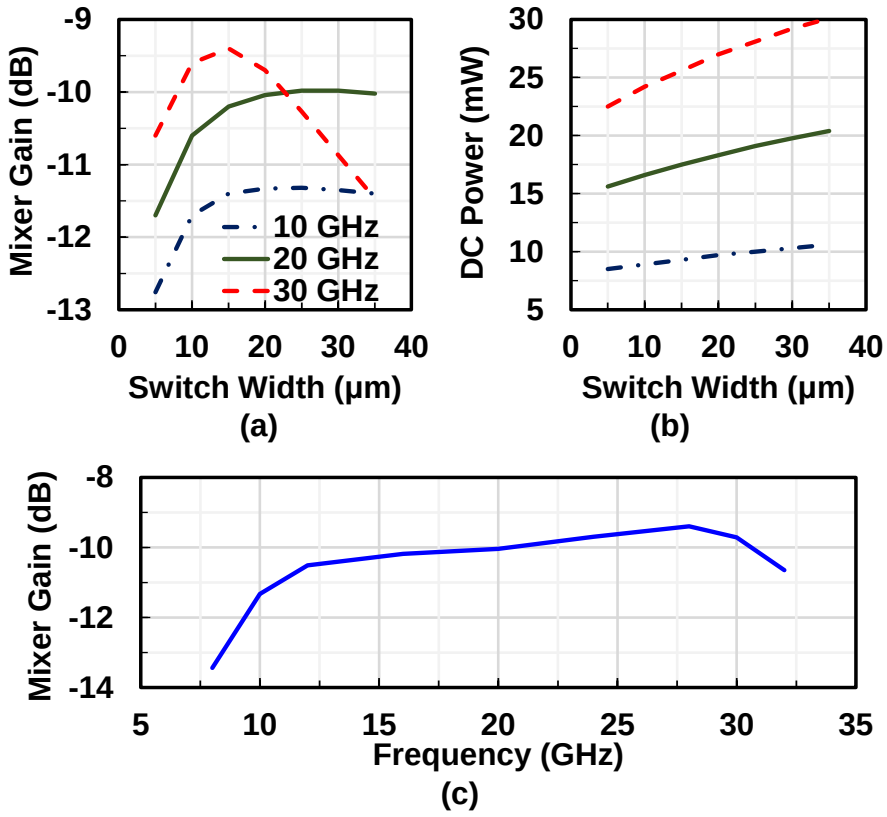


Figure 3.11. Simulated (a) mixer gain, (b) last stage LO drivers DC power for different MOS switch sizes, (c) mixer gain across frequency.

3.11). The switch width is swept from w=5 to 35μm and the mixer gain, and the DC power consumption of the last stage LO drivers (8 drivers, last section with NMOS/PMOS widths of 24/28μm in Fig. 3.3) are analyzed at 10, 20 and 30 GHz. As can be seen from Fig. 3.11, the gain and DC power follow the expected trends, but the gain flattens above $w = 20\mu m$ for 10 and 20 GHz. At 30 GHz, gain drops for large switch sizes because the switch parasitic capacitances are too large and result in a negative effect on the mixer impedance matching and gain. In this design, a w = 20μm is chosen as the optimal design with R_{on} and C_{off} values of 13 Ω and 10 fF, respectively. The simulated mixer voltage conversion gain is shown in Fig. 3.11(c) with increased gain vs. frequency. This is due to the L-matching network which was designed with gain peaking at 24-30 GHz to compensate for extra losses.

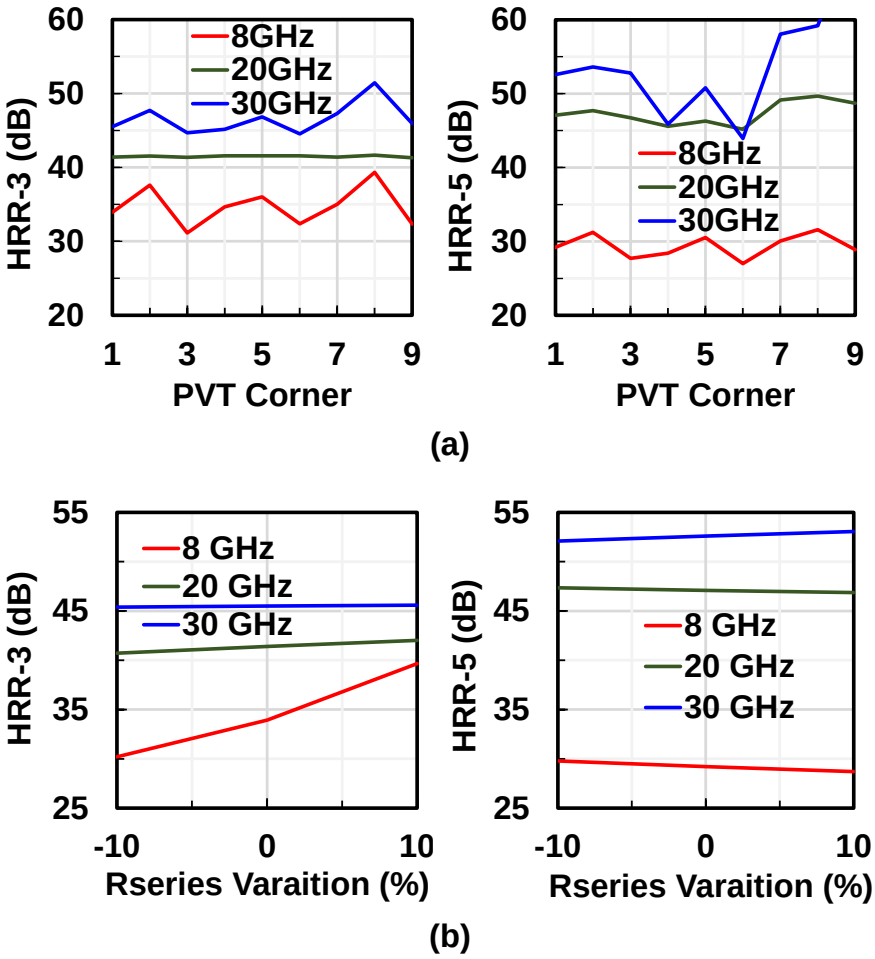


Figure 3.12. Simulated mixer HRR performance across (a) corners (TT, FF, SS, -20^o, 27^o and 100^o), (b) Rseries value variations (±10%).

Finally, the series resistance (R_{series}) used for voltage scaling in the different mixer paths is 83 Ω and has been presented in [44], [45]. The simulated mixer harmonic rejection across temperature (-20^{o}C, 27^{o}C and 100^{o}C) and transistor process corners (TT, FF and SS) is summarized in Fig. 3.12(a). As can be seen, the simulated HRR performance is higher than 27 dBc at 8-30 GHz across PVT variation. Also, the performance for ±10% variation in the resistor value (R_{series}) is shown in Fig. 3.12(b). Again, the simulated HRR is higher than 26-27 dBc at 8 GHz, and much higher at 20 GHz and 30 GHz.

The effectiveness of the RF isolation provided by the Wilkinson network is shown in Fig.

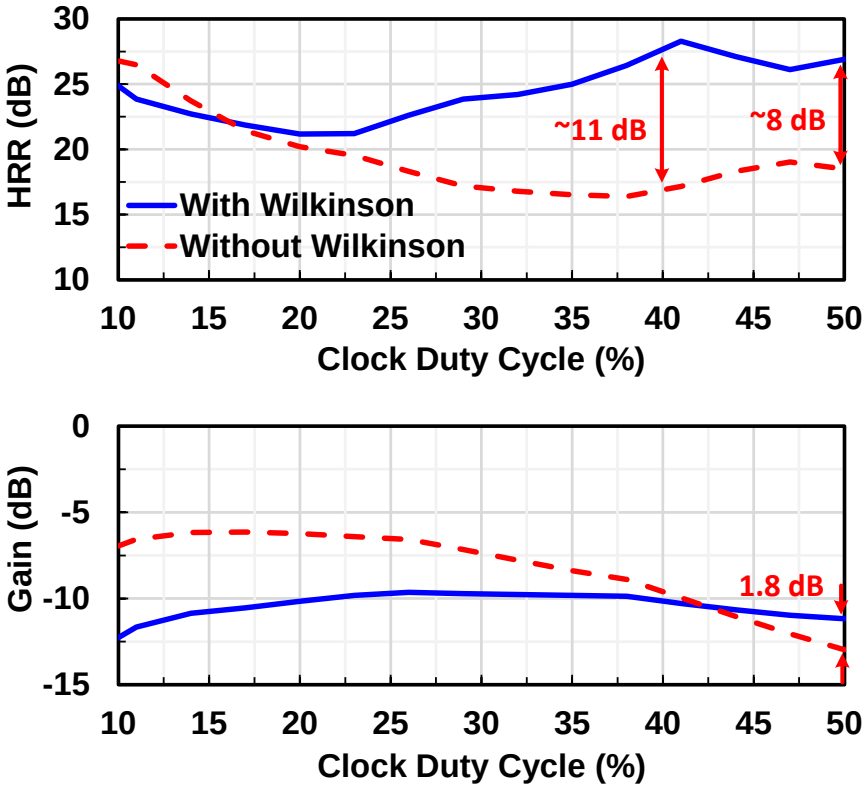


Figure 3.13. Simulated gain and HRR with and without the Wilkinson network.

3.13. Ideal square-wave LO signals are used, and the duty cycle is varied from 10% to 50% (full overlap). The Wilkinson network results in 8-10 dB better harmonic rejection ratio (HRR) and 1.8 dB better gain at high LO duty cycles. Also, as expected, at 12.5% duty cycle, the Wilkinson network is not needed and a traditional non-overlapping design results in the best performance.

3.4 Measurements

Several mixer prototypes were fabricated in the GlobalFoundries 45RFSOI technology. Figure 3.14 presents the 8-30 GHz harmonic rejection mixer with a chip area of 1.1*0.77 mm^2 including all pads. Two more HRM prototypes are fabricated for 2-6 GHz operation: with and without a Wilkinson network at the RF input. The same mixer switch sizes of 20μ/40nm were used in the low frequency prototypes but with an adjusted Wilkinson network and a different

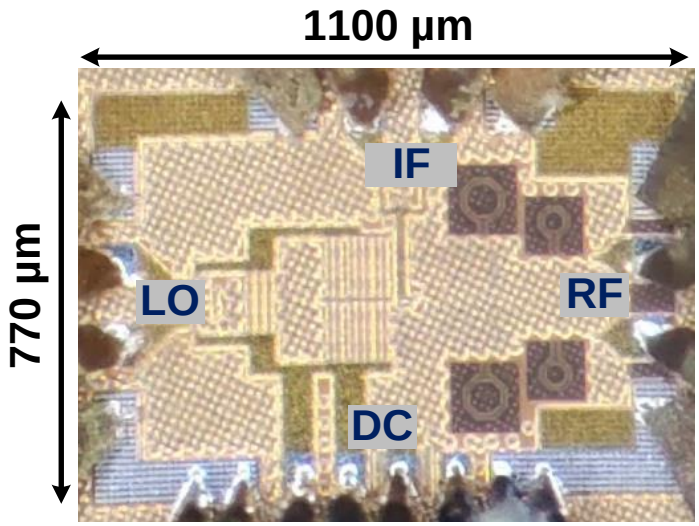


Figure 3.14. Chip micrograph for the 8-30 GHz HRM.

polyphase and capacitive divider network. The same LO drivers are used since the mixer size did not change. An L-matching network was not used in the low frequency HRM due to size constraints (the matching network can also be placed on the PCB if needed).

All measurements are carried out using the Keysight PNA-X (N5247B) with differential input and output measurement options (differential IQ measurement class in the PNA-X). Figure 3.15 presents the measurement setup with the input and output ports connected to the PNA-X using differential GSSG probes. The LO is fed differentially using a Keysight E8267D signal generator and a wideband Marki-Microwave balun (BAL0036). A Keysight power sensor (U8488A) is connected to the PNA-X for power calibration. Calibration is done using a GSSG CS-5 calibration substrate.

First, the two low-frequency mixer prototypes (2-6 GHz) are measured (Fig. 3.16). The Wilkinson and the LO polyphase filters are designed with 3 GHz center frequency and with 50% LO duty cycle, and an L-match is not used. The Wilkinson network provides much better conversion loss and harmonic rejection. At 3 GHz, the 3^{rd}, 5^{th} and 7^{th} harmonic rejection ratios are improved by 9.7 dB, 6 dB and 4.4 dB respectively with the Wilkinson network. The dc power

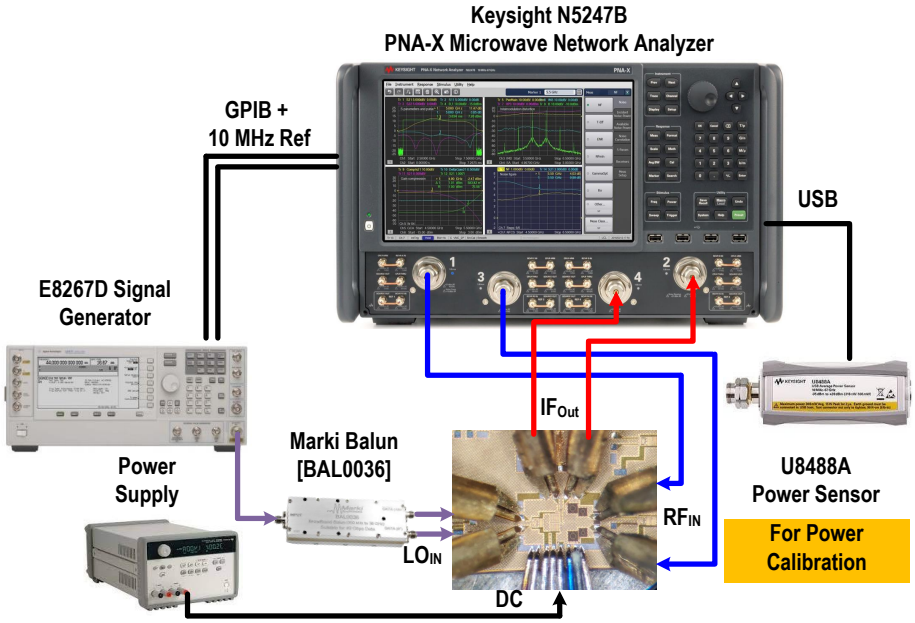


Figure 3.15. HRM measurement setup.

consumption for the low frequency mixer is 160-180 mW at 2-6 GHz, and the simulated IF 3-dB bandwidth is 0.9 GHz. All measurements were done at 50 MHz IF.

Next, the 8-30 GHz HRM is characterized. The measurement is done by applying a differential RF signal at LO+50MHz and then sweeping both RF and LO up to 35 GHz. The power consumption is 200-390 mW at 8-30 GHz. The measured conversion gain of the fundamental and harmonic frequencies is shown in Fig. 3.17(a). The fundamental gain is -12 dB with a 3-dB bandwidth of 8-30 GHz and agrees with simulations of -11.3 dB. The measured gain drops at higher LO frequencies (close to 30 GHz) because of the gain roll off of the Wilkinson divider and the capacitance in the LO path causing the LO to be nearly a sine-wave at 30 GHz.

The measured harmonic rejection ratio (HRR) is >27 dBc at 8-30 GHz. The harmonic gain measurements are done by applying an RF signal at N*f_{LO}+50 MHz, where N is the harmonic number. Due to limitation in the maximum measurable frequency of the setup (67 GHz), the harmonic performance was measured up to 33.5 GHz, 22.3 GHz and 13.4 GHz for the 2^{nd}, 3^{rd} and 5^{th} harmonics, respectively. Figure 3.17(b) presents the normalized gain of the

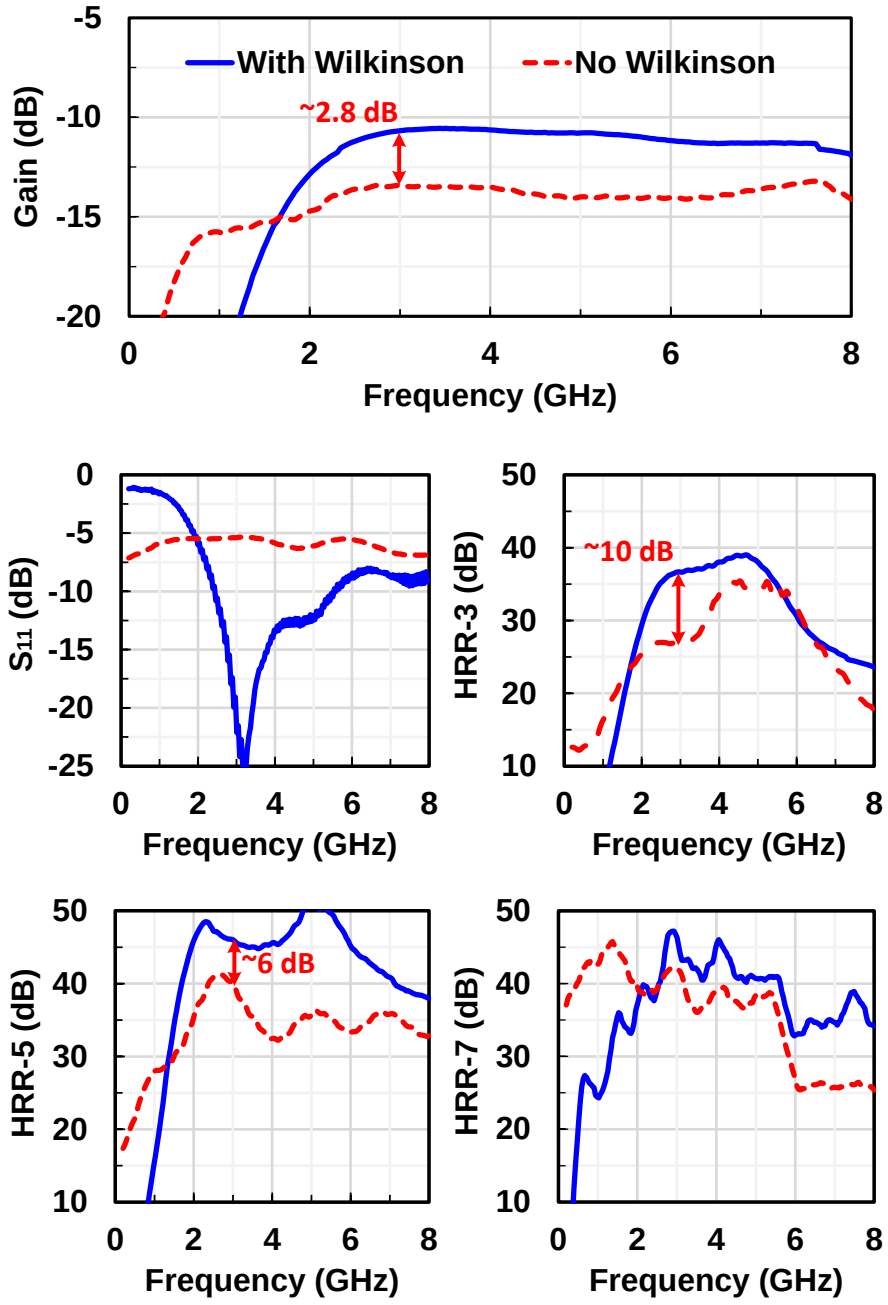


Figure 3.16. Measurement results of a low frequency version of the HRM implemented (2-6 GHz) with and without the Wilkinson network.

fundamental and harmonics at 10 GHz LO while sweeping the IF (and RF 11-20 GHz) signals. This shows that HRR performance is maintained across the IF bandwidth.

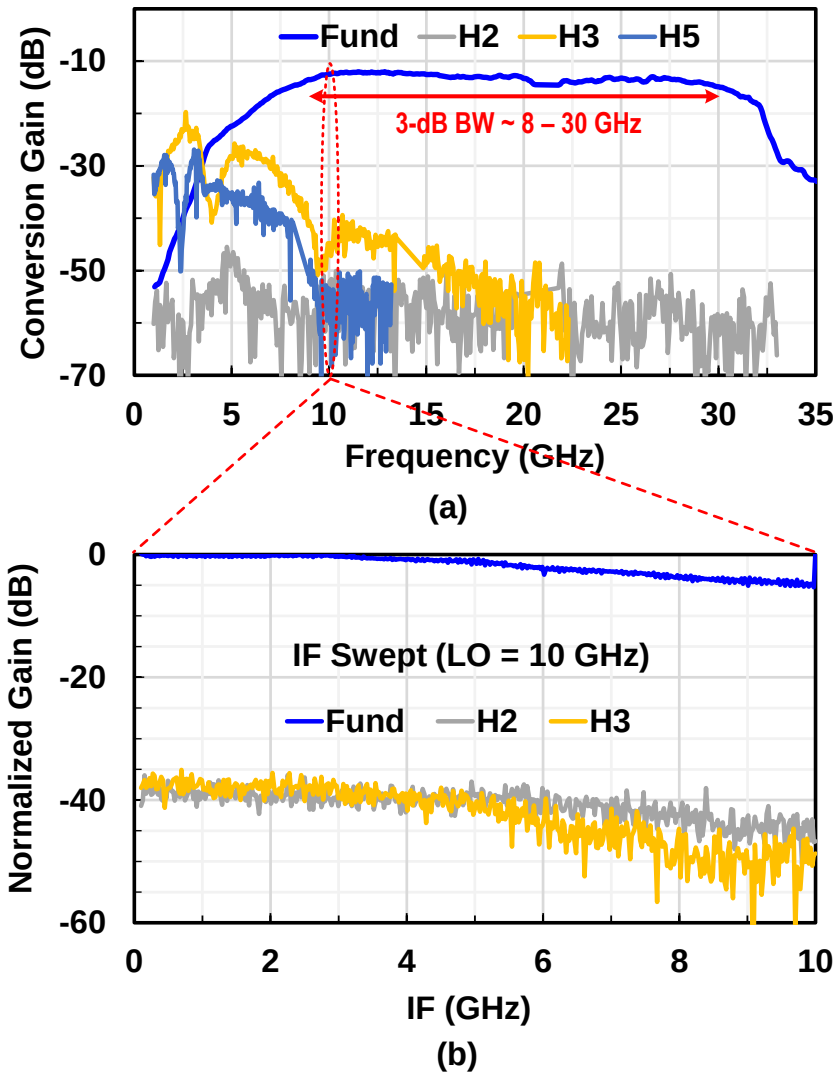


Figure 3.17. Measured conversion gain at fundamental and harmonic frequencies (a) across RF frequency, (b) across IF frequency.

The instantaneous mixer 3-dB IF bandwidth is measured at different LO frequencies (Fig. 3.18(a)). Operation of up to 8 GHz IF bandwidth is possible making the mixer dsign suitable for wideband high-speed receivers. The measured bandwidth is shown for the upper sideband, hence, at high LO frequencies ($f_{LO} \geq 25$ GHz), the IF bandwidth is limited by the RF bandwidth. Still, the full IF bandwidth is expected to be maintained when considering the lower sideband.

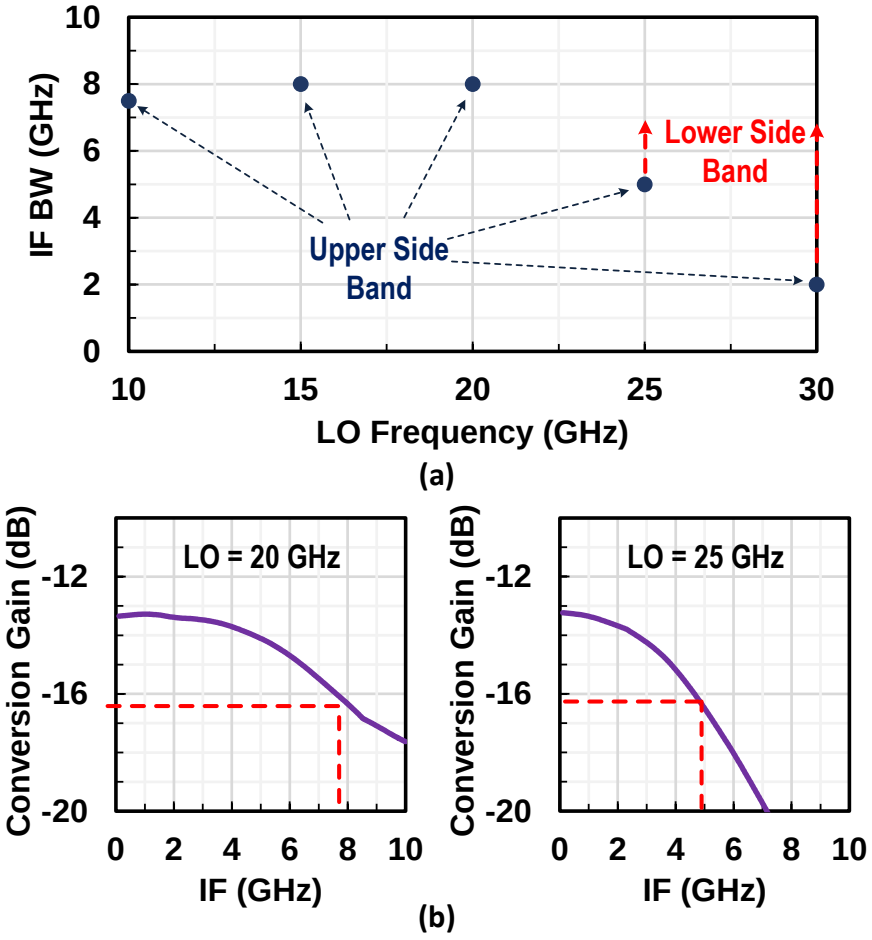


Figure 3.18. Measured (a) instantaneous IF bandwidth at different LO frequencies (b) gain versus IF frequency at two different LO frequencies (20GHz and 25GHz).

Figure 3.18(b) presents the conversion gain and 3-dB instantaneous bandwidth when the LO is fixed at 20 and 25 GHz.

The measured mixer's return loss (S_{11}) agrees well with simulation (Fig. 3.19(a)). The mixer noise figure (NF) is measured using the PNA-X along with two baluns at RF and IF ports to convert the differential signal to single ended (Fig. 3.19(b)). The baluns used in this setup are Krytar (4060265) with up to 26.5 GHz and Marki (BAL-0010) with up to 10 GHz at the RF and IF ports, respectively. The NF measurement is limited to 24 GHz by the input balun.

The mixer's in-band input P1dB is measured to be 4.2-7 dBm at 8-30 GHz and agrees

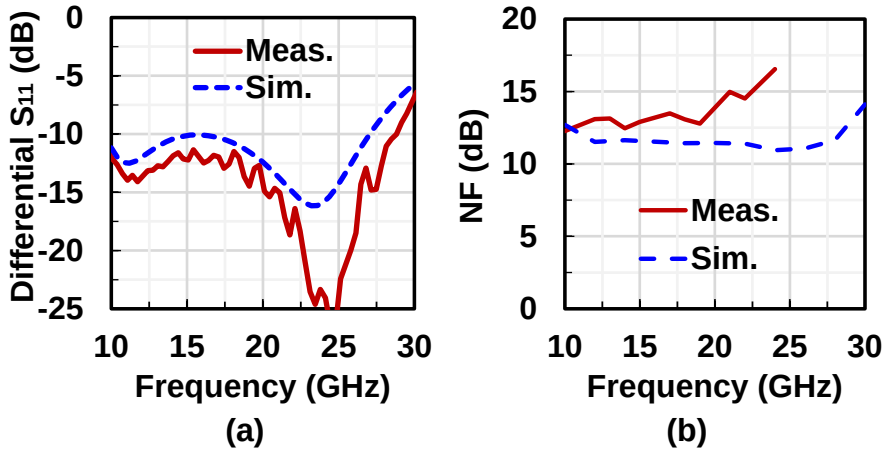


Figure 3.19. (a) Measured and simulated S11 (b) measured noise figure.

well with simulations (Fig. 3.20(a)). This is limited by the gate voltage swing at the mixer gate and is typical for low-voltage devices. Also, the gain compression curve versus input power is shown in Fig. 3.20(b) for f_{LO}=15 GHz.

The measured in-band IIP3 of the mixer is 14.2 to 16.2 dBm across the frequency from 8 to 30 GHz as presented in Fig. 3.21(a). The second order intercept point of the mixer is also measured (Fig. 3.21(b)) and is maintained above 40 dBm across the operation bandwidth.

The mixer spur table was also measured using the following equation relating the LO, RF and IF frequencies:

$$mf_{RF} - nf_{LO} = f_{IF} \tag{3.8}$$

Where m and n represents the harmonic numbers of the RF and LO, respectively.For a fixed LO and output IF frequencies, we can calculate all RF signals that will mix down to the signal bandwidth as follows:

$$f_{RF} = \frac{n}{m} f_{LO} + \frac{1}{m} f_{IF} \tag{3.9}$$

For example, at an LO of 10 GHz and an IF of 0.5 GHz, when m=n=1, RF=10.5 GHz which is the desired signal. For m=n=2, RF=10.25 GHz. The second harmonic of 10.25 GHz (20.5 GHz)

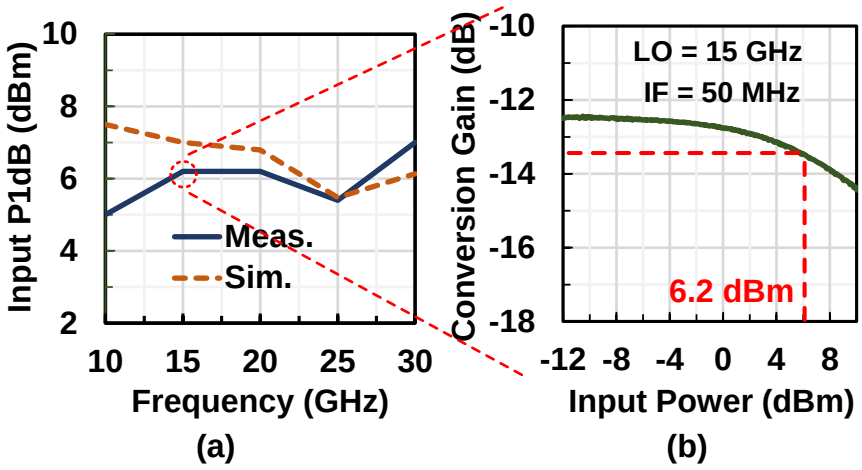


Figure 3.20. Measured input P1dB across LO frequency and detailed gain response versus input power at 15 GHz.

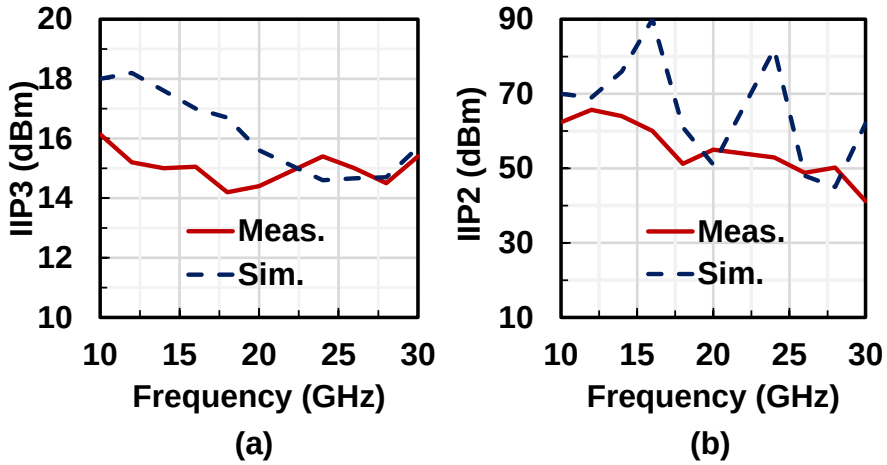


Figure 3.21. Measured and simulated (a) IIP3 (b) IIP2.

will mix with the second harmonic of the LO (20 GHz) generating an output signal at 0.5 GHz (on top of the desired signal). For m=1 and n=3, RF=30.5 GHz signal will mix with the third harmonic of the LO (30 GHz) generating an output signal at 0.5 GHz. Fig. 3.22(a) shows all possible RF signals for (m,n) in the range of 1-5, for an LO=10 GHz and IF=0.5 GHz.

Fig. 3.22(b) shows the measured (blue) and simulated (black) conversion gain when the

mxRF/nxLO	n=1	2	3	4	5
m=1	10.5	20.5	30.5	40.5	50.5
2	5.25	10.25	15.25	20.25	25.25
3	3.5	6.83	10.17	13.5	16.83
4	2.625	5.125	7.625	10.125	12.625
5	2.1	4.1	6.1	8.1	10.1

(a)

mxRF/nxLO	n=1	2	3	4	5
m=1	-11.6 -12	-55 -50	-44 -49	-65 -70	-53 -66
2	-110 -74	-91 -70	-88 -70	-95 -70	-87 -72
3	-110 -80	-100 -80	-70 -60	-89 -80	-71 -70
4	Low -80	Low -80	Low -80	Low -80	Low -80
5	Low -80	Low -80	Low -80	Low -80	Low -80

(b)

mxRF/nxLO	n=1	2	3	4	5
m=1	-11.1 -12.7	-66 -58	-53 -60	-90	-55.57
2	-77 -54	-77 -70	-82 -80	Low -80	Low -80
3	-78 -65	-87 -72	-60 -66	Low -80	-75 -80
4	Low -80	Low -80	Low -80	Low -80	Low -80
5	Low -80	Low -80	Low -80	Low -80	Low -80

(c)

mxRF/nxLO	n=1	2	3	4	5
m=1	-13 -14.9	-94 -70	-60	-75.61	-59.05
2	-65 -62	-80 -73	-88 -75	Low -80	Low
3	-52 -55	-80 -73	-60 -67	Low -80	Low -80
4	Low -80	Low -80	Low -80	Low -80	Low -80
5	Low -80	Low -80	Low -80	Low -80	Low -80

(d)

Figure 3.22. Spur charts of the mixer for IF=0.5 GHz, (a) all input RF frequencies at LO=10GHz, (b) conversion gains at LO=10 GHz, (c) conversion gains at LO=20 GHz and (d) conversion gains at LO=30 GHz. Blue/black represents the measured/simulated values.

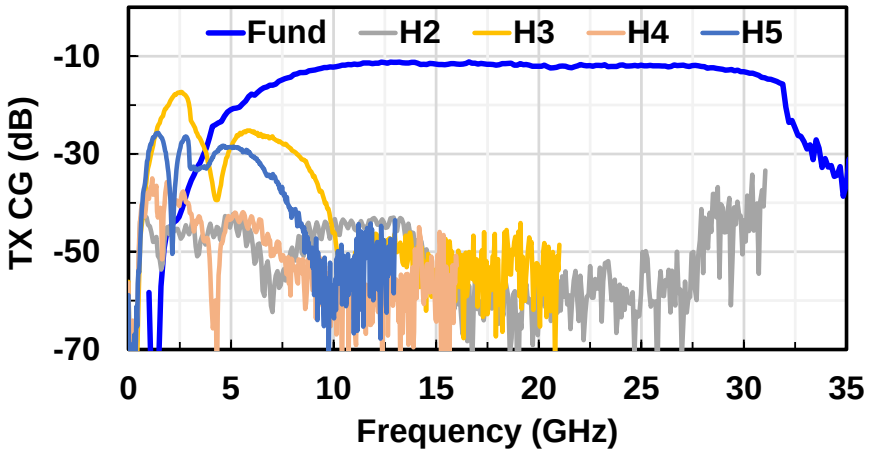


Figure 3.23. Measured TX operation up-conversion gain and harmonic emissions.

input RF frequency is set to the values shown in Fig. 3.22(a). The mixer spur performance is better than 37 dBc across all combinations of the m and n values. The even mixing spurs are naturally low due to the differential signals and double-balanced mixer topology, but note the drastic improvement in the (3,1), (1,3) (3,3), (5,1), (5,3) (5,5) spurs. These are 15-25 dB better than a standard double-balanced mixer due to the elimination of the 3^{rd} and 5^{th} harmonic LO components in the network and the high linearity of the mixer.

Fig. 3.22(c) and (d) shows the conversion gain performances when the LO frequency is set to 20 and 30 GHz, respectively. The input RF frequencies in these case are calculated similar to Fig. 3.22(a). For both charts the performance is maintained better than 40dBc. Note that for all measurements in Fig. 3.22, -80 dBm was the measurements equipment limit, therefore, the mixer spur performance is excepted to be even better when -80 dBc is shown in the table (with 0 dBm input power).

Finally, the mixer is also measured for TX up-conversion operation. The input IF signal is fixed (0.5 GHz) and the LO is swept from 0 to 35 GHz. The measured up-conversion gain versus the LO frequency is presented in Fig. 3.23(a). It is matching well the RX operation conversion gain due to passive and reciprocal operation of the mixer. The measured RF emissions due to

mixing with the harmonics of the LO frequencies are also measured and presented in 3.23. For example, at LO frequency of 10 GHz, H2 represents emissions at 20.5 GHz, H3 represents emissions at 30.5 GHz and H5 represents emissions at 50.5 GHz.

This work also shows a 3.75:1 RF fractional bandwidth which is better than state-of-the-art mixers and mixer-first receivers [56], [57]. Table 3.1 compares this work with the state-of-the-art ([44]–[46], [58], [59]). When comparing harmonic rejection performance, this work shows the highest frequency of operation. Compared with mm-wave mixers/mixer-first receivers, this work also achieves the widest instantaneous (IF) bandwidth. Also, for the low frequency prototype, this work achieves the same harmonic rejection performance when compared with the state-of-the-art, however, with lower power consumption and larger IF bandwidth.

3.5 Conclusion

This chapter presents a mm-wave passive harmonic rejection mixer in GF 45RFSOI with a HRR of 27-45 dBc and 8 GHz of IF bandwidth. The 8-phase LO generation is done using passive polyphase filter implementation, and the isolation between the mixer cells is provided using a 4:1 Wilkinson network in the RF path.

Chapter 3, in full, has been submitted for publication of the material as it may appear in: A. Ahmed and G. M. Rebeiz, "A 8–30 GHz Passive Harmonic Rejection Mixer with 8 GHz Instantaneous IF Bandwidth in 45RFSOI," *IEEE Trans. Microw. Theory Techn.*. The dissertation author was the primary investigator and author of this material.

Table 3.1. Comparison With State-Of-The-Art Mixers and HRMs

Reference	CMOS Node	Freq. (GHz)	Gain (dB)	IF BW (GHz)	HRR (dBc)	Input P1dB (dBm)	Supply (V)	Power (mW)
This Work	**45nm RFSOI**	**8-30** **2-6**	**-12** **-10.5**	**8 GHz** **0.9 GHz[1]**	>27 32	**4.2-7** **7.2-12[1]**	**1.2**	**200-390** **160-180**
[44]	32nm RFSOI	0.05-4	-6.4/-9.2	0.25	35	6-11	1.1/1/5/2.1	98-298
[45]	45nm RFSOI	0.13-3	-8/-10	0.08	35	11-13	1	110-280
[46]	45nm RFSOI	3.7-6.5	N/R	N/R	22-43 (39-72)[2]	5	N/R	89-135
[58]	65nm	21-29	12-14.5 (BB Amp ON) -15 - -12 (BB Amp OFF)	0.5 0.8	N/A	-6 3	1.2	22.8 13.2
[59]	65nm	9-31	40	0.025-0.1	N/A	-	N/R	73 / 162

[1] Simulated [2] With Calibration

Chapter 4

Conclusion and Future Work

4.1 Conclusion

This dissertation presented a 140 GHz 2D scalable wafer-scale transmit-receive (TRX) phased array based on radio frequency (RF) beamforming with 4-bit phase and gain controls. The chip occupies an area of 9.84*8.27 mm^2 and is designed and fabricated in GlobalFoundries (GF) CMOS 45RFSOI technology. The chip is flipped on a low-cost organic RF PCB containing 8x8 patch antenna array placed at 1.07x1.22 mm grid (0.5λ x 0.57λ at 140 GHz). The array electronically scans up to ±60^o in the H-plan and 38^o in the E-plan for both TX and RX operations. Over-the-air (OTA) measured performance of the array demonstrates TX peak effective isotropic radiated power (EIRP) of 34-37.5 dBm at 137.5-145 GHz and RX input 1-dB compression point (P1dB) of -12 to -9 dBm at 134-143 GHz. Communication link measured for both TX and RX operations supports modulated 16-/64- quadrature amplitude modulation (QAM) signals with up to 24Gb/s data rates with an rms EVM less than 7%/6%. In addition, a transmit-receive phased array wireless link at 1.45m and 5.2 meters is demonstrated with data rates up to 20 and 16 Gb/s using 16-QAM modulated signal with an rms EVM less than 9% for the 1.45m link. To the best of our knowledge, this article presents the highest reported EIRP of 37.5 dBm for wafer scale arrays in silicon technologies. This was presented in chapter 2.

A harmonic rejection mixer was also developed and presented in this dissertation in chapter 3. It is a wideband mm-wave harmonic rejection mixer (HRM) operating in the frequency

range from 8 to 30 GHz. Resistive scaling is used to maintain high mixer linearity while rejecting the 3rd and 5th harmonic folding. The clock generation circuit employs a passive two-stage polyphase filter to generate the 8-phases which eliminates clock dividers and results in efficient operation up to 30 GHz. Furthermore, the clocks are designed with overlapping 50% duty cycle, and mixer cell-to-cell isolation is achieved using a Wilkinson network in the RF path. This novel design results in mm-wave operation with wide instantaneous bandwidth and greatly reduced LO power consumption. The HRM is fabricated in GlobalFoundries 45RFSOI CMOS process and has a measured conversion loss of 12 dB at 8-30 GHz with an instantaneous IF bandwidth of up to 8 GHz. A harmonic rejection ratio (HRR) of 27-45 dB is measured across the entire bandwidth for the 2nd, 3rd and 5th harmonics. The measured input P1dB is 4.2-7 dBm across the bandwidth. This mixer is suitable for high linearity mm-wave 5G systems and wideband receivers and can be easily scaled to 20-50 GHz with low power consumption.

4.2 Future Work

4.2.1 140 GHz TRX Array

The array presented in chapter 2 showed the world's first wafer-scale 8x8 phased array at D-band. However, there exist some room for improved performance. First, the mixer and IF amplifiers are limiting the instantaneous bandwidth to 9-14 GHz and, hence, limiting the modulation data rate. For future designs, the IF circuits and mixers needs to be redesigned for higher bandwidth.

Second, as discussed chapter 2, the measured transmission line losses was much higher than simulated losses. This limited the achievable array EIRP for TX operation and Noise Figure for RX operation. For future design, these extra losses needs to be accounted for during the design phase for even higher EIRP and, therefore, larger communication distance.

4.2.2 Harmonic Rejection Mixer

Chapter 3 focused on the discussion of 8-30 GHz harmonic rejection mixer. The achieved linearity is quite good, but, there is room for improvement, especially in a wideband environment. In addition, and extension to this mixer would be designing and IQ or single-side band (SSB) mixer to reject the image as well.

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