Microsc. Microanal., page 1 of 10
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Three-Dimensional Nanoscale Mapping of State-of-the-Art Field-Effect Transistors (FinFETs)

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Abstract: The semiconductor industry has seen tremendous progress over the last few decades with continuous reduction in transistor size to improve device performance. Miniaturization of devices has led to changes in the dopants and dielectric layers incorporated. As the gradual shift from two-dimensional metal-oxide semiconductor field-effect transistor to three-dimensional (3D) field-effect transistors (finFETs) occurred, it has become imperative to understand compositional variability with nanoscale spatial resolution. Compositional changes can affect device performance primarily through fluctuations in threshold voltage and channel current density. Traditional techniques such as scanning electron microscope and focused ion beam no longer provide the required resolution to probe the physical structure and chemical composition of individual fins. Hence advanced multimodal characterization approaches are required to better understand electronic devices. Herein, we report the study of 14 nm commercial finFETs using atom probe tomography (APT) and scanning transmission electron microscopy–energy-dispersive X-ray spectroscopy (STEM-EDS). Complimentary compositional maps were obtained using both techniques with analysis of the gate dielectrics and silicon fin. APT additionally provided 3D information and allowed analysis of the distribution of low atomic number dopant elements (e.g., boron), which are elusive when using STEM-EDS.

Key words: atom probe tomography, finFET, energy-dispersive X-ray spectroscopy, chemical mapping, correlative microscopy

Introduction

In this era of digitalization, the ubiquitous nature of electronic devices such as phones, laptops, and smart home appliances has led to a social and economic revolution. At the core of each device is a transistor, a simple electronic switch that performs logic operations and stores data in memory blocks through intricate connections with other transistors (Mano, 1979). The first transistor was invented in 1947 by Bardeen, Brattain, and Shockley at Bell Labs (Bardeen & Brattain, 1948). Since its invention, there have been numerous changes over the years with the field-effect transistor (FET) taking the forefront (Deal & Early, 1979; Chih-Tang, 1988). The development of complementary metal-oxide semiconductor (CMOS) technology (consisting of PMOS and NMOS; P for p-type and N for n-type, indicating the type of dopants used for the source-drain contacts) with individual FETs as either PMOS or NMOS is the current basis for chipsets used in digital integrated circuits (ICs) (Weste & Eshraghian, 1985).

The FET has seen a relatively steady scaling of size following Moore's Law (Moore, 1965). In effect, as the FET size scaled, parasitic capacitance between the contacts and gate became a major issue which led to new designs and materials to be used (Bohr, 2011). A paradigm shift occurred in 2000 with the introduction of the three-dimensional (3D) finFET technology by Dr. Chenming Hu (Hisamoto et al., 2000). The 3D structure with the fin protruding out and the gate wrapped around three sides allowed better control of the channel current during on/off state and also overcame the problem of drain-induced barrier lowering, which was responsible for large off-state leakage currents due to the small channel size.

The fin brought in the era of nonplanar devices (Thompson & Parthasarathy, 2006; Bohr, 2011). With the current production technology node at 14 nm (based on fin width), identifying and understanding individual finFETs is a burgeoning field. Defects in finFETs are currently identified using electrical, optical, or thermal techniques such as soft defect localization using a scanning optical microscope (Bruce et al., 2003; Phang et al., 2004), infrared (IR)-based techniques, due to Si being transparent to IR wavelengths (Nikawa et al., 1999; Phang et al., 2004) and scanning spread resistance microscopy (Zhang et al., 2007; Hayase et al., 2012). Although these techniques can tell the pass or fail state of each transistor and a localized region where the FETs are good or bad, the relationship between device failure and

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structural or concentration anomalies is still missing. At best these techniques can provide a spatial resolution of ~50 nm (Nikawa et al., 1999; Bruce et al., 2003; Phang et al., 2004; Zhang et al., 2007; Hayase et al., 2012).

Soft defects occurring due to dielectric breakdown, process variations, and resistive interconnects are more often attributed to structural defects at the atomic level. Specifically, line-edge roughness and fin thickness variations can affect the threshold voltage and sub threshold slope (Pei et al., 2002; Baravelli et al., 2008), both important electrical parameters for low power devices. Variations in the oxide layer thickness can give rise to larger tunneling currents (Bernstein et al., 2006), while discrete impurity atoms in the channel can significantly affect the current density in the channel (Wang et al., 2011). Thus, a systematic study of such variability in individual devices is necessary as the device dimensions decrease so that the performance of an IC is not comprised. Both the scanning transmission electron microscopy (STEM) and atom probe tomography (APT) can aid to further this understanding. Although the STEM can provide an atomic scale spatial resolution <1 Å (Batson et al., 2002) and an energy-dispersive X-ray spectroscopy (EDS) system incorporated in the STEM can provide chemical mapping, the ability to observe low atomic number (Z) elements is still lacking. Further the STEM can only provide 2D information on 3D finFETs.

Since the introduction of laser-assisted APT, the semiconductor industry has quickly ensured early adoption of this technique. APT can provide both spatial and compositional information by combining time-of-flight mass spectrometry with a point projection microscope. Samples prepared in the form of a needle are field evaporated under the application of a high-DC voltage and a UV laser to give 3D-nanoscale composition with a spatial resolution of ~0.2 nm at best at best for metals and up to 1–2 nm for complex oxides and nitrides (Lefebvre-Ulrikson et al., 2016), in x, y and z dimensions (Gault et al., 2012; Larson et al., 2013; Miller & Forbes, 2014; Devaraj et al., 2017).

Initial studies on semiconducting devices and structures dealt with arsenic (As) Cottrell spheres in Si (Thompson et al., 2007). Further studies on Si–germanium (Ge) epitaxial layers (Kelly et al., 2007) were followed by reports on planar high-κ dielectrics analyzed using both secondary-ion mass spectrometry and APT to show the reliability of APT (Ulfig et al., 2007; Larson et al., 2008). Subsequent studies on distribution of boron and phosphorus dopants during processing and on boron distribution during ion implantation were also reported (Takamizawa et al., 2012; Han et al., 2015). Individual planar metal-oxide semiconductor field-effect transistor devices have also been analyzed by Inoue et al. (2009) and by Larson et al. (2011). Kambham et al. (2011, 2012, 2013*a*, 2013*b*) dealt with the issue of targeting individual fins. Very recently, correlative microscopy with APT and transmission electron microscopy (TEM) on 30 nm static random access memory (SRAM) planar transistors with Ni–Si contacts has also been shown (Panciera et al., 2013). Boron profiles for 14 nm fins were reported by Hatzistergos et al. (2013) albeit on samples specifically prepared for APT.

Thus, intensive studies have been carried out for transistors using APT, but none of the aforementioned studies have shown the application of correlative microscopy (APT and STEM) to 14 nm commercial finFETs, with analysis of gate dielectric stack and fin region for both PMOS and NMOS; 14 nm finFETs have added complexity of their small size apart from being 3D in nature. Furthermore, previous studies have not dealt with as-fabricated commercial devices, but with devices where fabrication was halted midway to obtain and prepare samples for APT. In this report using STEM-EDS and APT, we analyze in detail finFET regions for both NMOS and PMOS fins in as-fabricated devices. PMOS devices are characterized by the presence of Ge (allows strain-induced mobility enhancement) as opposed to the NMOS. The importance of using two complementary techniques is discussed here along with their advantages and shortcomings. APT being a 3D technique, with the ability to observe all elements with equal probability, shapes the future of nanoscale characterization for finFETs.

Materials and Methods

Scanning electron microscope (SEM) images of individual fins, for both NMOS and PMOS, are shown in Figure 1. This aids in correct identification of the region of interest. The schematic (Fig. 1a) depicts the Si fin and gate dielectrics. Samples prepared for APT are etched using hydrogen peroxide to remove tungsten from the contacts. The removal of the tungsten increases the analysis success rate by reducing sample fracture during field ionization. The planar view of the device at the contact level, after tungsten etching, is shown in Figure 1b. The PMOS is identified by the intermittent nature of the fin (fin ends shown) and the NMOS is the device adjacent to it (left panel of Fig. 1a and Fig. 1b). APT specimens are extracted and sharpened using standard FIB-based cross-section lift-out and annular milling procedures (Larson et al., 1999; Thompson et al., 2007; Lawrence et al., 2008) but the APT lift-out differs from TEM/STEM lift-out since a wedge-shaped section is used for APT whereas the TEM/STEM uses a cuboidal block.

Sample Preparation for STEM

Integrated circuits containing SRAM arrays are removed from the packaging and de-bonded using standard protocols discussed in the literature. The chips are then cleaved to the required size and undergo mechanical polishing to the layer of interest; 14 nm SRAM arrays are identified for the PMOS and NMOS regions, using computer-aided design (CAD) layout, in an FEI Helios NanoLab 650 (FEI, Hillsboro, OR, USA) or 450S FIB/SEM system. The region of interest is protected from Ga damage during ion milling using metallic Pt deposited *in situ* in the FIB using a gas injection system (GIS). The region of interest is then marked down with "X"-type FIB milling patterns to ensure easy identification during subsequent steps. A lift-out section is prepared by milling rectangular patterns on either side followed by a J-cut.

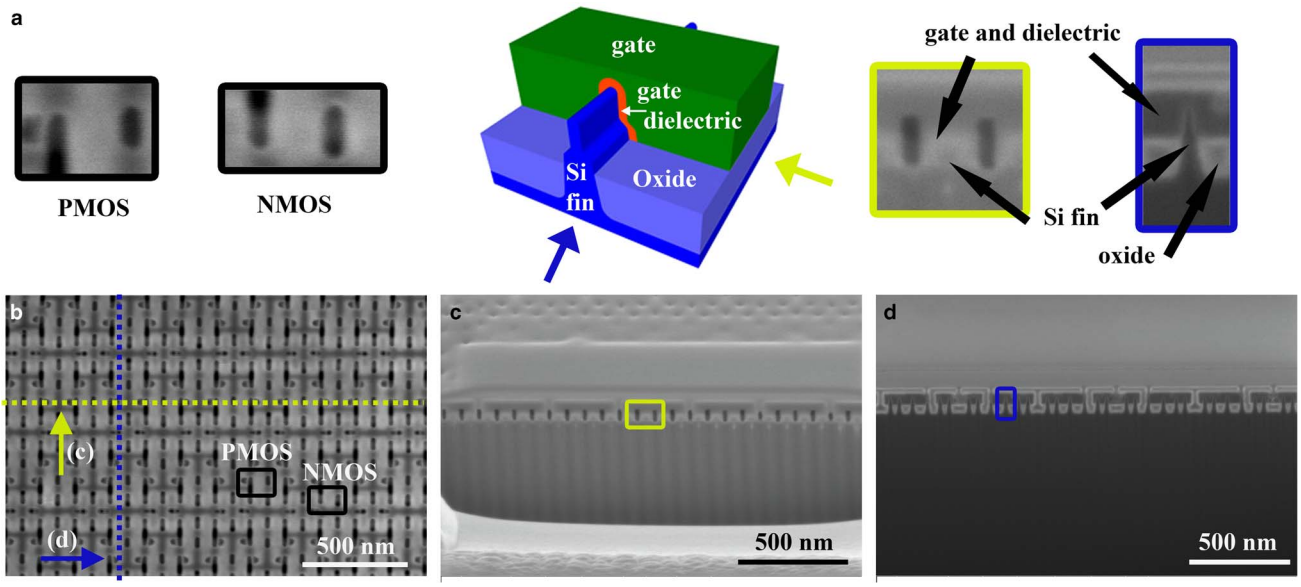

Figure 1. a: Left panel: planar view of individual p-type metal-oxide semiconductor (PMOS) and n-type metal-oxide semiconductor (NMOS) devices that are analyzed using atom probe tomography and scanning transmission electron microscopy. Center panel: schematic of a typical field-effect transistors. The Si fin is shown in blue with a layer of buried oxide, above which the fin protrudes from the substrate. The gate dielectric stack which consists of multiple layers is shown in orange with the gate itself in green (schematic not drawn to scale). Right panel: an individual fin cross-section in two different directions. **b:** Scanning electron microscope (SEM) image of a PMOS and a NMOS transistor with the contacts etched, in planar view. **c:** Cross-section SEM image of the sample along the gate direction (as shown by the yellow dashed line in **b**). **d:** Cross-section SEM image of the sample along the fin direction (as shown by the blue dashed line in **b**). Individual fins are visible as indicated by the blue box.

The thickness of a lift-out section is typically between 2–3 μm. A micromanipulator is then used to detach the prepared section from the substrate and attach it onto an OmniProbe® Cu grid (Ted Pella, Inc., Redding, CA, USA) suitable for use with a TEM/STEM sample holder. The attached section is then milled down to a thickness of ~150 nm at an accelerating voltage of 30 kV and a beam current of ~0.23 nA. A low accelerating voltage of 5 kV or less and a current of ~68 pA are then used for the final polishing step to remove any re-deposition due to the Ga milling and bring the final thickness within 20 nm. The cross-section parallel to the fins, as shown in Figure 1c, and perpendicular to the fins, as shown in Figure 1d, are both used to ensure accurate identification of the region of interest. Additional details and images for the sample preparation are mentioned in Supplementary Section 5.

Supplementary Section 5

Supplementary Section 5 can be found online. Please visit journals.cambridge.org/jid_MAM.

STEM-EDS Measurements

As prepared TEM sections are analyzed using an FEI Tecnai Osiris™ system at 200 kV accelerating voltage. Four windowless silicon drift detectors placed at 90° with respect to each other are used to obtain the chemical maps. A 1 nA beam is used in a ~512 × 512 array with a 25 μs dwell time for ~10 min. The EDS data is then quantified and deconvoluted using the Cliff-Lorimer method.

Sample Preparation for APT

Integrated circuits containing SRAM arrays are removed from the packaging and de-bonded using standard protocols. The chips are then cleaved to the required size and undergo mechanical polishing to the layer of interest. The cleaved chips are then etched to remove tungsten (W) from the contacts; 14 nm SRAM arrays are identified for the PMOS and NMOS regions, using CAD drawings, in a FEI Helios NanoLab 650 or 450S FIB/SEM system. The PMOS is identified by the intermittent nature of the fin (fin ends shown) and the NMOS is the device adjacent to it (Fig. 1b). The region of interest is protected from Ga damage during ion milling using a thin layer (~150 nm) of either metallic (Ni), deposited by sputtering, or insulating (SiO_2) layer, deposited *in situ* in the FIB using a GIS. This is followed by metallic Pt deposition (~100–200 nm). A wedge-shaped slice of the sample section, with the region of interest is then detached from the sample surface using a micromanipulator. The wedge-shaped slice is prepared by milling rectangular patterns at a tilt angle of 22° and ensuring that the fins are perpendicular to the milling direction. The detached section is then placed on an Axial Rotation Manipulator™ (ARM3™) module and the free-hanging edge is cleaned (milled) to view the fins. One of the walls (depending on the direction of rotation for cross-section sample preparation) is milled to bring the transistor of interest right at the edge

(Supplementary Section 4). The lift-out wedge is then physically rotated 90°, such that the fins are facing sideways (with respect to the analysis axis) to prepare cross-section tips. The rotated wedge has the fins facing sideways. On the visible gates on top, another layer of either metallic (Ni) or insulating (SiO_2) layer is deposited (~100 nm) followed by Pt (~200 nm). The wedge (due to the rotation) now has one flat parallel wall (parallel with respect to the analysis axis). Thus a new wedge-shaped section is now prepared out of the existing section where the bottom apex of the wedge is aligned with the top of the fin or the region of interest. The as-prepared wedge is then detached from the ARM3™ module using a micromanipulator; 2 μm long square pieces are cut from the wedge and placed on as-fabricated Si microtip arrays. These are then annularly milled (at 30 kV accelerating voltage and ~0.23 nA followed by ~26 pA when the end diameter is <800 nm) using a donut-shaped milling pattern to obtain a conical tip with an end diameter <150 nm. A final polishing (using 2 kV accelerating voltage and ~34 pA, and subsequently ~24 pA) is used to remove any residual Pt from the tip surface, which might interfere with the APT results. Additional details and images for the sample preparation are mentioned in Supplementary Section 4.

Supplementary Section 4

Supplementary Section 4 can be found online. Please visit journals.cambridge.org/jid_MAM.

APT Measurements

As prepared tips are then quickly transferred to the LEAP system and run in the laser-assisted mode to obtain the 3D atom probe reconstruction. For the PMOS devices, prepared tips are run in a LEAP 4000 XHR (at the Environmental Molecular Sciences Laboratory at Pacific Northwest National Laboratory, Richland, WA, USA) at a base temperature of 50 K and laser energy of 60 pJ with a pulse repetition rate of 125 kHz. A detection rate of 0.005 ions/pulse is used. The NMOS devices are run in the LEAP 5000 XR (Cameca, Gennevilliers, France) at a base temperature of 50 K and laser energy of 60 pJ with the pulse repetition rate of 100 kHz. Obtained data are reconstructed using the Integrated Visualization and Analysis Software (IVAS®) software following the tip profile method.

Results

STEM

Nanoscale chemical composition maps representative of the elements present in the fin and the gate dielectric layer are shown in Figure 2, for both NMOS and PMOS, respectively. The high-angle annular dark field (HAADF) image of the region probed in the EDS is shown at the left in Figure 2. The first row corresponds to a NMOS along the direction of the fin (the direction corresponding to the fins is displayed in Fig. 1d). The HAADF map for the NMOS (Fig. 2a left) demonstrates different contrasts for the Si fin and the gate dielectric layers. The large region of light grainy contrast also seen is tungsten (EDS map shown in Supplementary Section 6), which has been etched only for APT specimens and not for STEM. The EDS maps show that for the silicon (Si) fin and the gate dielectric layers consisting of Hf, O, Ti, N, Al, and C are clearly visible. The HfO_2 high-κ dielectric

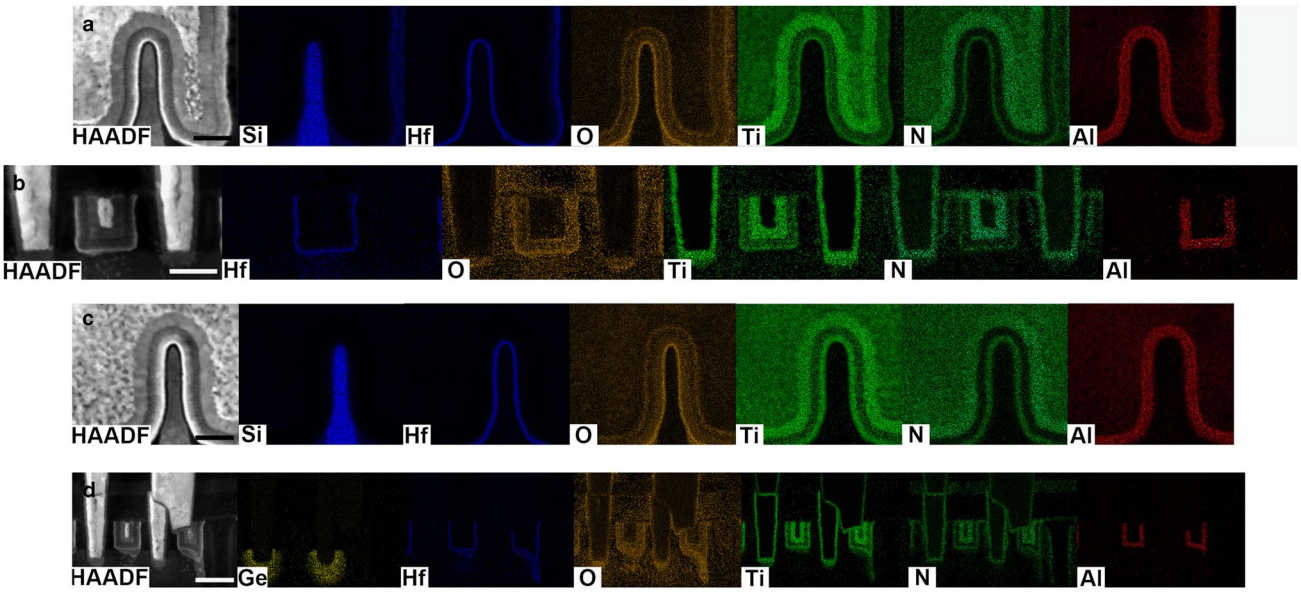

Figure 2. High-angle annular dark field (HAADF) image and energy-dispersive X-ray compositional maps (**a**) for a n-type metal-oxide semiconductor (NMOS) fin, (**b**) for the gate region in an NMOS fin, (**c**) for a p-type metal-oxide semiconductor (PMOS) fin, and (**d**) for the gate region in a PMOS fin. The presence of Ge and the differing fin widths distinguish a PMOS from a NMOS. The Si fin and Hf from the HfO_2 dielectric is shown in blue, O in orange, Ti and N signals from the TiN layer are in green and Al signals from AlC_x are in red. Scale bar: (**a, c**) 20 nm, (**b**) 30 nm, and (**d**) 50 nm.

forms a thin barrier around the Si fin followed by a thin layer of TiN, then AlC_x and subsequently a thicker layer of TiN before the W gate contact. The TiN layer contrast is visible more so from the N maps as opposed to the Ti maps. The Ti map shows a blurry contrast across the Al layer. The HAADF map along the gate direction for the NMOS, displayed in Figure 2b, shows the W (light contrast) present in the contact regions (source and drain) and at the center of the gate region for the 14 nm technology node. The HfO_2 high-κ dielectric is present only in the gate region and the Al signals are also seen only in the gate region. Thus, the source-drain contacts are devoid of any HfO_2 or AlC_x layers. In the gate direction also HfO_2 is the layer closest to the fin. Structural irregularities in the Si fin, as well as the HfO_2 high-κ dielectric, are absent from the EDS maps (Figs. 2a, 2b) indicating a working NMOS device.

Supplementary Section 6

Supplementary Section 6 can be found online. Please visit journals.cambridge.org/jid_MAM.

Figures 2c and 2d display EDS maps for the PMOS devices. The PMOS devices show similar chemical compositions for the gate dielectric stack as the NMOS devices. The Si fin is also visible in Figure 2c. There are two important differences between the PMOS and the NMOS device: (a) the Si fin is thicker for the NMOS device compared with the PMOS device (Figs. 2a, 2c, respectively); (b) the PMOS device is characterized by the presence of Ge in close proximity to the gate region, right under the W contacts. Both these differences, especially the presence or absence of Ge can be used to identify a PMOS from a NMOS device.

Thus, with careful sample preparation and a sensitive EDS detector, a wealth of information on the physical device structure and chemical composition can be obtained from the STEM, however this technique suffers from three shortcomings; (a) with each successive generation of devices, due to reducing sizes the total signal intensity for the EDS will keep decreasing. Low Z elements such as N, O, and Al show a background signal from other regions as well (Fig. 2). This indicates that the available scattering cross-section for reliable EDS signals from finFETs will ultimately reach its limit. (b) The ability to see dopant elements such as boron is not possible using this technique. Both the low concentration of dopants in finFETs ($10^{18}/cm^3$ corresponding to parts per thousand) as well as the low atomic number makes it difficult for EDS to yield any reliable chemical maps of boron in the STEM. (c) Any sort of 3D information is also missing since the STEM provides 2D information averaged over ~100 nm in the third dimension. Obtaining 3D information becomes more important especially for the PMOS devices where the fins are not continuous and the end points at the source/drain cannot be completely understood using 2D maps from the STEM.

APT

The aforementioned shortcomings of STEM motivated the use of APT, which is more suited to characterize the 3D nature of the finFET device (Fig. 1a). APT has equal probability of detecting all elements in the periodic table allowing detection of B, C, N, Al, and O for the FETs. It further allows ~10–100 parts per million (ppm) quantitative sensitivity (upto 1 ppm under conditions of low background counts and large number of atoms collected; Koelling et al., 2017), which is two orders of magnitude higher than that obtained by EDS (Thompson et al., 2007; Miller & Forbes, 2014). Although most techniques provide either compositional or spatial information, APT is unique in its ability to convert time-of-flight mass spectrometry to compositional information (through mass to charge ratio). The sequence of ions and x, y coordinates from a position sensitive detector are converted into 3D spatial information.

The analysis of the Si fin and gate dielectric layers obtained using APT is displayed in Figure 3. The absence of Ge as evidenced by the mass spectrum analysis (Supplementary Section 3, Fig. 3) allowed identification of these maps as part of a NMOS device. As seen from the leftmost map in Figure 3a, the Si fin (in blue) is wrapped on three sides by the gate dielectrics. The HfO_2 layer (shown in orange) and the subsequent TiN and AlC_x layer (in green and red, respectively) are also seen on all three sides of the Si fin. The inset shows the HAADF image of the NMOS fin with the black box marking the region that was analyzed in APT. This conclusion is based on the chemical compositions observed from the NMOS atom probe maps, which were captured using a LEAP 5000 XR at Cameca. The gate dielectric layers are observed in succession in the individual atom maps shown in Figure 3a (additional maps are shown in Supplementary Section 1). The HfO_2 high-κ dielectric layer can be analyzed using the HfO maps and the TiN layer is analyzed using the TiN maps. The Ti maps also show a blurry contrast across the AlC_x layer, similar to the STEM-EDS results. Both Al and C maps are useful for analyzing the AlC_x layer itself.

Supplementary Sections 1 and 3

Supplementary Sections 1and 3 can be found online. Please visit journals.cambridge.org/jid_MAM.

The presence of atoms of different chemical species in regions far apart from the fin cannot be construed as a background signal. As an example, the complete 3D information that could be obtained from the HfO maps is shown in Figure 3b. Each map corresponds to a rotation of 90°. The atom probe maps display regions of HfO perpendicular to the fin (the first and third maps in Fig. 3b). When rotated by 90°, these regions would appear as if they were part of a low count background signal (as seen in the HfO map in Fig. 3a). This can be explained in the following way; during device fabrication, the HfO_2 high-κ dielectric layer is deposited using atomic layer deposition (Lin et al., 2002) in the pits formed after the fins are fabricated, defining the gate area. HfO_2 covers all the pit walls of the gate area and fin walls also. The region of HfO_2 covering the fin (Fig. 3a)

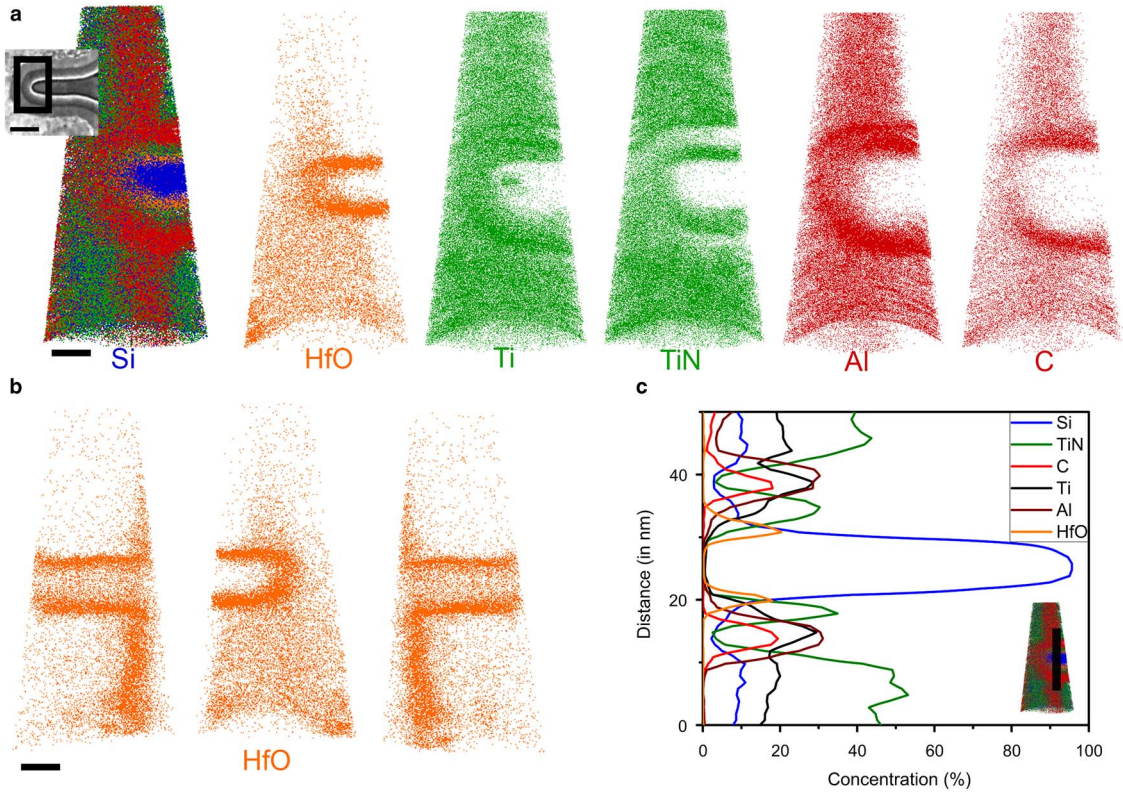

Figure 3. a: Atom probe tomography (APT) maps of a n-type metal-oxide semiconductor fin with inset showing the high-angle annular dark field image for the region of interest captured in APT. The Si fin is covered by the gate dielectric on three sides. **b:** APT maps for HfO each rotated by 90° with respect to the previous. **c:** Concentration profile across the fin and the gate dielectric stack for each of the chemical species. Scale bar is 25 nm in length.

corresponds to that which was deposited over the fin wall while the perpendicular regions, seen in Figure 3b, correspond to part of the pit walls of the gate area. A similar analysis can be carried out for the TiN and AlC_x layers also. Supplementary Movie SM1 shows a video clip of HfO_2 layer as it completes a 360° rotation to allow a full 3D interpretation. Such detailed visualization of the gate dielectric layers, as well as the fin, has been observed for the first time.

Supplementary Movie 1

Supplementary Movie 1 can be found online. Please visit journals.cambridge.org/jid_MAM.

Further detailed analysis of the dielectric layers can be carried out by measuring their concentration profiles as a function of distance (Fig. 3c). The region plotted for the concentration profile is shown in the inset (bottom right). The concentration profile is taken across a cylindrical section by averaging the concentration across a circular area of a given radius (here 5 nm) and plotting it as a function of distance. The physical position of the cylindrical section determines the region where the plot is made, with a bin size of 0.1 nm along the distance axis. From the concentration profile three important inferences can be made; (a) it can be observed that the Si fin (blue curve) is covered by the HfO_2 dielectric on either side (orange curve). This is followed by a thin layer of TiN (green). Subsequently AlC_x (red curves for Al and C) and a thick layer of TiN are present. This is in close agreement with the STEM-EDS maps. The Si fin is devoid of any observable contamination from any of the dielectric stack, as evidenced by the zero concentration of the dielectric layers in the fin region. The concentration of the dielectrics on either side of the fin is also similar indicating uniformity in processing conditions during fabrication. A single peak on each side also hints toward minimal variability in fin wall thickness, which directly affects the device threshold voltage. Such profiles are important in case of failed devices where any anomaly in the concentrations on either side could possibly give rise to device failure. Another observation is that the Si fin concentration also increases after the dielectric stack due to the presence of SiO_2 which is used as the insulating barrier around the fins.

The analysis for a PMOS device is more complicated due to the intermittent nature of the fins and the presence of Ge which strains the region around it. This analysis should be interpreted with caution as the presence of undulating walls or waviness could possibly indicate intermixing or a sporadic evaporation field. APT analysis of a PMOS device is shown in Figure 4. Parts of a Si fin and the gate dielectric layer, albeit on two sides, can be observed in the first map in Figure 4a. This region is toward the right side of the first map. Apart from this, the map also shows a region of Si toward the left of the map and dielectric regions perpendicular to the fin but

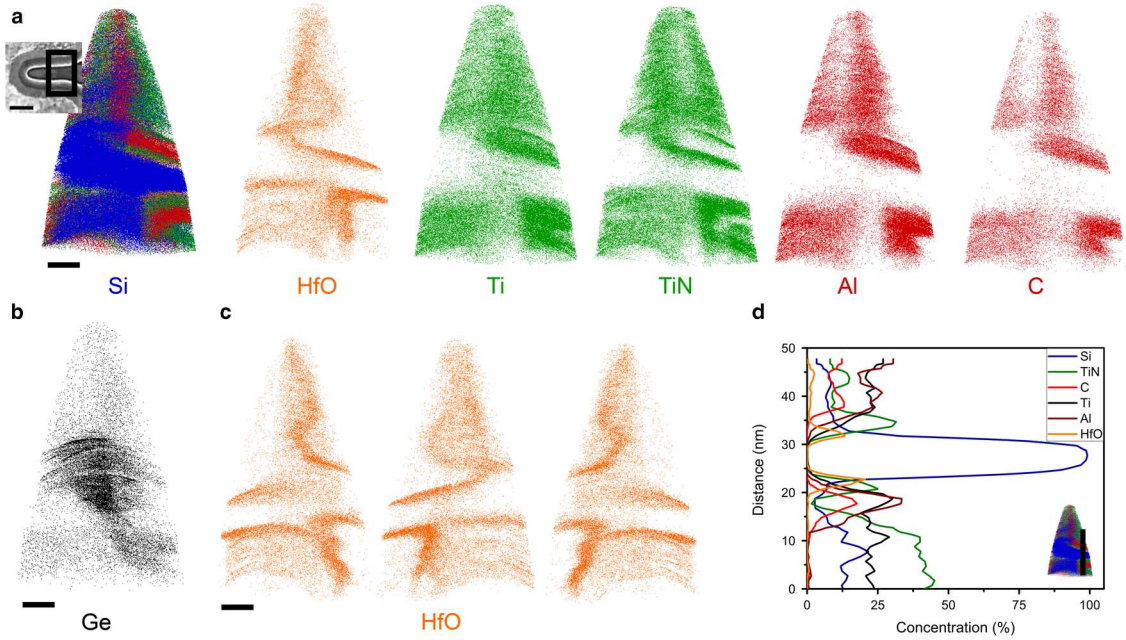

Figure 4. a,b: Atom probe tomography (APT) maps for a p-type metal-oxide semiconductor (PMOS) fin closer to the source/drain contact. Inset: high-angle annular dark field image for the region of interest captured in APT. **c:** APT maps for HfO each rotated by 90° with respect to the previous. **d:** Concentration profile across the fin and the gate dielectric stack for each of the chemical species. Scale bar is 30 nm in length.

with undulating walls unlike the NMOS maps. Such undulating walls are generally observed for contacts (due to less stringent design considerations) or regions near the contacts (Fig. 2d). A clear understanding of these undulations with specific emphasis on the effect of the evaporation field will be the subject of future work. The inset shows the HAADF image of the PMOS fin with the black box marking the region that was analyzed in APT. The PMOS device atom probe maps were captured using the LEAP 4000 XHR at Pacific Northwest National Laboratory. As seen from Figure 4a the PMOS also shows a similar layered structure as present in the NMOS for the gate dielectric stack (additional maps to aid in the interpretation are shown in Supplementary Section 2). Figure 4b shows the Ge maps, which is a signature for PMOS. Ge is present at the base of the fin region in this map (mass spectrum used for the analysis is shown in Supplementary Section 3, Fig. 4).

Supplementary Sections 2 and 3

Supplementary Sections 2 and 3 can be found online. Please visit journals.cambridge.org/jid_MAM.

The HfO maps show a twofold V-shaped region at the base of the atom probe map (first map in Fig. 4c). The left part of this map shows well-defined regions around the fin whereas the right-side shows the perpendicular undulating regions. The same regions can be observed in different views across the other maps in Figure 4c, each rotated by 90° with respect to the previous one. This V-shaped region at the base also contains O and a small amount of B (Supplementary Section 2). Thus, for the PMOS, the 3D visualization along with chemical composition was essential for identifying the region closer to the source/drain contact. The concentration profile shown in Figure 4d follows the same trends as that for a NMOS (Fig. 3c), but provides further information for the PMOS. The slightly different concentrations of the dielectrics on either side of the fin indicate that, closer to the contacts, the control on the layer thickness is less than around the fin-gate intersection, which was seen in the NMOS maps in Figure 3.

Discussion

APT is able to provide detailed spatial (~1 nm for semiconducting heterojunctions) and compositional information (with approximate ppm detection range) for the finFETs which is not possible with STEM. In order to gain confidence in the APT maps, it can be seen that there are similarities between the observed maps. First, the Ti signals in the AlC_x layer is mimicked by both techniques for PMOS and NMOS. Second, the N signal in the STEM maps and the TiN signals from the atom probe maps are useful for understanding the TiN dielectric layer, showing similar features. Third, Al and C signals are consistent across both techniques. Finally, similar distribution for the HfO_2 layer is also observed using both techniques.

A comparison for the thickness of the Si fin and gate dielectric stack, for PMOS and NMOS, by STEM and APT is provided in Table 1. The STEM thickness measurement is obtained from the maps itself while APT values are obtained as full width half maximum of the concentrations

Table 1. Thickness Comparison for the Si Fin and Dielectric Stack for n-Type Metal-Oxide Semiconductor (NMOS) and p-Type Metal-Oxide Semiconductor (PMOS) Using Scanning Transmission Electron Microscopy–Energy-Dispersive X-Ray (STEM-EDS) and Atom Probe Tomography (APT).

	Si Fin	HfO_2	TiN	Al	C
STEM-EDS					
PMOS	–	1.31	3.15	4.58	
NMOS	–	1.25	1.66	3.88	
APT					
PMOS	8.1	1.75	2	4.9	4.2
NMOS	9	2.2	2.35	6.4	3.8

All units are given in nm.

as a first approximation. The values indicate a tighter spread in the thickness using STEM as opposed to APT.

Although the APT can provide true 3D maps of various ionic species, some important shortcomings of this technique are worth mentioning here, specifically with regard to how the contrast (thickness) of different layers can be affected by the instrument itself. The APT uses a mass to charge ratio for identification of chemical species which leads to the issue of overlaps for similar mass to charge ratios for different chemical species (e.g., Ti^{3+} and O^{2+}). Thus, care needs to be taken to ensure that the influence of these overlaps on the interpretation is ruled out. The presence of isotopic abundance and physical regions in the maps are often used to rule out most overlap issues. The field evaporation of ions can also cause significant trajectory aberrations for dissimilar elements, which is severe for regular top-down sample preparation in APT (Gilbert et al., 2011; Koelling et al., 2011; Devaraj et al., 2014; Grenier et al., 2014; Madaan et al., 2015). Further, since the field evaporation process is not uniform due to changes in local electrostatic environment during the evaporation process, the results should be interpreted with caution as the reconstruction algorithms are based on simple hemispherical models (Vurpillot et al., 2011). Therefore, trajectory aberrations due to field evaporation of dissimilar species and spectral overlaps are most likely causing the differences in thickness between STEM-EDS and APT. This brings into focus the role of correlative microscopy used here, whereby two complementary techniques can provide unique information as well as allow greater reliability by supporting the claims based on the other technique.

Such studies, as the one carried out in this paper, are imperative since with each technology node, device to device variability during fabrication can be expected to go up due to the small device size. The tolerance in fin width has been calculated to about 1 nm for industry acceptable variability in electrical parameters for 20 nm finFETs and a tolerance of 10–15% for variations in gate length (Shiying & Bokor, 2003). Further, diffusion of dopants into the Si channel can cause large changes in the electronic density, known as random density fluctuations; these are an important part of current experimental and computational studies (Pei et al., 2002; Bernstein et al., 2006; Baravelli et al., 2008; Wang et al., 2011). A failed device could hence differ from a working device based on small structural or concentration fluctuations. Thorough analyses call for techniques such as APT and STEM, which can observe the structural and compositional variability and correlate it to the device performance.

Summary

In conclusion, the chemical and spatial distribution of finFETs were studied using correlative microscopy by employing APT and STEM. Although STEM is able to provide 2D chemical maps on the fins and dielectrics, its inability to probe low Z dopant atoms or present any 3D maps motivated the use of APT to further our understanding of PMOS and NMOS devices. The APT maps showed the 3D views of the dielectric layers with similarities between both techniques. The TiN signals provide additional information for the finFETs apart from N in the STEM. The thickness measurements show the efficacy of each of these techniques. Although STEM-EDS will ultimately reach its limits due to device scaling and low signal sensitivity in the EDS, the APT with ppm sensitivity and nanoscale spatial resolution will be poised to continue investigations on each new generation of finFETs and other non-Si technologies. In addition, continuous semiconductor process scaling down to 10 and 7 nm aligns well with the APT sample volume, allowing for increased portions of the finFET structure to be analyzed as the transistor geometry scales down. Correlative microscopy will also be important to enhance the reliability in APT results while simultaneously being used for advanced characterization of finFETs. The introduction of 3D integrated circuits and flash memory, such as the VNAND flash technology by Samsung® (Seoul, South Korea), make APT particularly suitable for future applications that require 3D chemical maps.

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Author's Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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