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Materials Sciences Division
Center for Advanced Materials

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M.S. Thesis

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Abstract

Microstructural Coarsening during Thermomechanical Fatigue and Annealing of Micro Flip-Chip Solder Joints

by

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Professor J.W. Morris, Jr., Chair

Microstructural evolution due to thermal effects was studied in micro solder joints (55 ±5μm). The composition of the Sn/Pb solder studied was found to be hypereutectic with a tin content of 65-70 wt %. This was determined by Energy Dispersive X-ray analysis and confirmed with quantitative stereology. The quantitative stereological value of the surface-to-volume ratio was used to characterize and compare the coarsening during thermal cycling from 0–160°C to the coarsening during annealing at 160°C. The initial coarsening of the annealed samples was more rapid than the cycled samples, but tapered off as time to the one-half as expected. Because the substrates to which the solder was bonded have different thermal expansion coefficients, the cycled samples

experienced a mechanical strain with thermal cycling. The low-strain cycled samples had a 2.8% strain imposed on the solder and failed by 1000 cycles, despite undergoing less coarsening than the annealed samples. The high-strain cycled samples experienced a 28% strain and failed between 25 and 250 cycles. No failures were observed in the annealed samples. Failure mechanisms and processing issues unique to small, fine pitch joints are also discussed.

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1. Background

1.1 Flip-Chip Technology

Flip-chip bonding is a method of electrically and mechanically attaching an integrated circuit (IC) to a substrate. In this process, the IC is flipped face down, and the solder on the pads of the IC is bonded to corresponding pads on the substrate.[1] One of the most common low temperature solders used in this application is 62/38 wt% Sn/Pb, which is the eutectic composition for this alloy. In some applications, the IC is packaged in a chip carrier to provide protection from mechanical or chemical damage. The IC is bonded with the solder to the chip carrier, which is often made of a ceramic material (Figure 1.1-1). To further decrease the size of components, some applications demand that the IC be directly bonded to the circuit board. This direct chip mount attachment is called "flip-chip on board".

The chip mount design is the most recent development in the evolution of electronic packaging to ever decreasing size and pitch. A schematic of this progression is shown in Figure 1.1-2. The older technology soldered pins that were attached to the chip carrier to holes drilled in the circuit board. This was called through-hole technology. Decreasing the size of this technology was limited by the size of the pins and the spacing of the holes. There was a lower limit to how small these sizes could be without compromising the mechanical integrity of the part. The next design that quickly gained popularity was a surface mount design that bonded the chip carrier to the board by soldering leads to the surface. No holes were required for this design, and decreasing the size of this technology was only limited by the size and spacing of the leads. New methods were developed that

further decreased these parameters which lead to the development of the fine pitch surface mount technology. Fabrication of these devices became difficult as the size and spacing decreased, because the tolerances required for the proper placing of the leads onto the correct pad on the board became difficult to realize. There was also the increased tendency of cross talk between the leads, compromising the performance of the device. The chip mount design is an attempt to further improve the performance of the device while decreasing the size. This leadless design has the added benefit that the electrical connections can be located anywhere on the surface of the board (array design). The earlier designs only had the capability of peripheral attachment.

Flip-chip technology was first developed by IBM in 1962 in response to this demand for higher density packaging.[2] It has replaced wire bonding in some applications that demand smaller lightweight, higher performance products at lower cost.[3] It provides the shortest possible interconnection with the lowest induction and shortest signal pathway, maximizing operating frequency, which is essential to very high speed logic interconnections.[4] Enhanced performance is seen because shorter electrical pathways reduce propagation delay.[1] The ever increasing demand for higher density packaging and size reduction can be met with the flip-chip design primarily by decreasing the pad size and pitch of the solder joints. Faster switching times are realizable with this design, especially with smaller solder joints and array (rather than peripheral) layouts. Joints of this type are typically an order of magnitude smaller than in conventional surface mount technologies and are termed *microjoints*.[3] Most commonly, they are 100 μm or less.

With the flip-chip technology, a faster operating speed is possible without an increase of the tolerances of alignment that would be required with the fine pitch lead attachment. This is due to the surface tension alignment effect of solder. To bond a component to a substrate, the pads are first aligned optically, typically with a misalignment of 1-10%. During reflow of the solder, the molten alloy spreads over the surface of the pad and initially forms a joint geometry of higher energy (Figure 1.1-3). This geometry profile causes the component to move relative to the substrate until the joint attains the minimum total energy.[5] This is generally assumed to be at zero misalignment.

Flip-chip technologies are found in many applications, from military avionics to personal computers. Telecommunication applications such as pagers and cellular phones benefit from the small size of this interconnect design. The watch market, however is one of the largest users of flip-chip technology in the world, primarily from Citizen Watch Co., Ltd.[1] Automotive and military applications such as automobile navigation systems, missiles, reconnaissance satellites, and ground missile launchers, also benefit from flip-chip technology advantages as well as any of the variety of small consumer products with displays. Table 1.1-1 shows the typical operating temperatures associated with some of the applications discussed. The melting point of eutectic Sn/Pb is 183°C. Therefore, it can be seen that the solder joints in these devices are subjected to very high homologous temperatures during service (Figure 1.1-4). In general, meeting the demand for smaller and

faster devices results in more severe operating conditions for the solder in terms of both strain and temperature.

Application	Product Life (years)	Cycles /Year	Low Temperature (°C)	High Temperature (°C)
Auto (oil)	5-10	1000	-40	175
Auto (under hood)	5-10	1000	-55	125
Military avionics	10-20	365	-55	125
Military marine	5-10	265	-55	95
Space	5-20	9000	-40	85
Commercial aircraft	20	365	-55	95
Telecommunications	7-20	365	-40	85
Industrial	10	185	-55	95
Computers	5	1460	15	60
Consumer	1-3	365	0	60

Table 1.1-1: *Worst Case Operating Conditions of Flip-Chip Solder Joints*[1,6]

1.2 Solder Joint Reliability

The solder in electronic packaging applications is used to join two substrates which usually have much different thermal expansion coefficients. The solder joints in the flip-chip surface-mount design are the sole electrical and mechanical attachments. (Prior methods had either pins or leads to take up the mechanical loading, with the solder joining the pin or lead to the board in a much more compliant configuration.) Therefore, if a device is subjected to thermal fluctuations, the solder joints are subjected to a shear

displacement with every cycle in this leadless design. In most cases, the solder is the most compliant material joining the substrates, and it is assumed that the solder takes up all the strain produced by the thermal cycles.[7] Therefore, the reliability of the solder joints in the newer flip-chip design is much more critical as it is under much greater strain, and, once it fails, all electrical and mechanical connection is lost.

Many different approaches have been used to study thermomechanical fatigue of solder; using methods ranging from experimental to theoretical and computational.[8, 9, 10, 11] There is, however, no industry standard on testing parameters and consequently little consistency in testing conditions or samples from study to study. Extrapolating one result to another can only be done with caution.

Part of reason for the lack of standardization is the complexity of the problem. At such high homologous temperatures, the thermomechanical fatigue conditions described is actually a creep/fatigue problem, further complicated by the microstructure evolution and intermetallic growth that occurs with thermal testing.[12] Thermal fatigue life depends on many parameters such as solder composition and microstructure, void content and morphology, metallization on substrate and chip, intermetallic compounds formed at joined interfaces, as well as joint geometry and layout. The thermally induced displacement results in a complex stress and strain distribution in the joint that is different for different joint geometry and location of the joint between the substrates. The fatigue life of hourglass-shaped joints was found to be three times that of the barrel-shaped joint.[13] This was result was found for 5/95% Sn/Pb joints subjected to a one hour cycle that varied from -50 to 150°C. Finite element studies show that only small changes

in joint geometry of joints within the same sample can substantially change the stress field. It was found that fatigue life improved if many joints were placed at the periphery.[8]

Under some test conditions high Pb solder were found to have better fatigue properties than eutectic solders,[14] while other studies found the opposite result.[15] Keeping composition constant and simply altering the microstructure can also effect fatigue behavior. In prior work, it was found that increasing the cooling rate decreased the phase size and increased fatigue life.[16, 17] The fatigue life is effected by the metallization layers and corresponding intermetallic compounds that form between the solder and the substrate. The solder microstructure is more uniform with nickel metallization than with copper,[19] and this microstructure has been found to have a longer fatigue life than the microstructure with copper metallization.[18] Gold is known to form extremely brittle intermetallic compounds that are detrimental to fatigue life.[20]

There does not appear to be any firm conclusion on the effect of voids on reliability. Different studies indicate that they are detrimental,[21] have no substantial effect,[20] or are advantageous.[22] Others report that it appears that small uniformly dispersed voids may be acceptable, but large voids at the joint interfaces will decrease reliability.[11, 23] One source stated that voids were definite stress risers for surface mount configurations, but they could be stress relievers in others.[11] Some studies show that in other cases, stress and strains increase with void size up to a point and then decrease.[11] It does appear that most work has pointed to the general conclusion that the location of the voids, their size, as well as their distribution is important to the overall effect of voids on

reliability. It is important to observe or measure these parameters to make an informed conclusion as to the effect of voids on reliability. Although the effect of voids on mechanical integrity is not known, they can cause signal deterioration in high frequency applications.[1]

Only a few have undertaken microstructural studies to observe coarsening and its role in failure mechanisms and reliability. The majority of these studies have been performed on relatively large solder joints that have a predominately eutectic microstructure. In these studies,[14, 24] it was determined that upon thermal cycling, an equiaxed shear band of coarser material would form near one of the substrates at a eutectic colony boundary (Figure 1.2-1). A crack would eventually form in this region and would propagate to failure. Although the coarsening was concentrated in the shear band, the rest of the microstructure still coarsened, only to a lesser degree. This failure mode was found in the larger joints even with different cooling rates that generated a degenerate eutectic microstructure.[16] This coarsening needs to be included in reliability models. It was found that, upon accounting for this coarsening,[25] the estimated fatigue life was only 21% of that found without including this parameter.[26]

1.3 Processing Concerns with Smaller Joint Size and Pitch

Issues that were not as significant of a problem with larger joints can become important at the smaller scale. Fine pitch designs suffer from increased solder bridging (the joining of adjacent solder joints).[27] This problem can be improved by decreasing the size of the joints. This constrains joint design such that there is a maximum joint height

for a given pitch. Also, it is difficult or impossible to inspect the joints to insure proper alignment. This is due to both the small size of the joints as well as the limited accessibility of viewing the joints in the array design. The deleterious effect of defects increases as size decreases, especially with voids.[3] Voids can become a significant fraction of the smaller joints and still not be detectable by common nondestructive inspection techniques.

Small variations of the volume of solder on each pad can destroy the possibility of proper z-alignment. With decreasing joint size, the tolerance on variation of solder volume can increase to such an extent that it is very difficult to meet with many methods currently used in production, especially solder paste. With decreasing solder joint size comes a greater concern for the size and corresponding weight of the chip. Once the solder melts, the weight of the chip and the volume of solder determine the final joint height. If the solder volume is small and the chip is large, the weight of the chip can be too great for surface tension of the solder to properly align the chip to the substrate. Therefore optimizing the location and size of the joints as well as the size of the substrate can become critical in applications requiring small solder joints.

Intermetallics take up a much larger fraction of the joints and may play a larger role in the failure mechanisms. As the intermetallic layer grows over time, loss of solderibility is a greater possibility due to the limited amount of solder present.[28] Therefore, these joints have a shorter storage life, and maintaining proper storage temperature is much more critical. Decreasing solderibility leads to incomplete wetting of the solder on the pad. Partial wetting of the pads by the solder can lead to an increase in

the solder height of the individual joint by a significant amount. It was found when the effective wetted area was decreased by 20%, the joint height increased by 4μm.[5] This can exacerbate z-alignment difficulties even with the exact same amount of solder volume present on each pad.

2. Introduction

2.1 Test Samples

Test samples were made to investigate the effect of different thermal treatments on the solder. Each sample consisted of a quartz substrate, metallization layers, hypereutectic 70/30 Sn/Pb solder joints, and either a silicon or an epoxy-fiberglass (FR-4) substrate. A schematic of the cross section of the samples after joining is shown in Figure 2.1-1. Each substrate had the same pattern exposed onto it. A sketch of this is shown in Figure 2.1-2. This pattern consisted of two set of three rows of 21 copper circles, 100μm in diameter, that were surrounded by titanium. There was also one copper circle in the center of the pattern. Solder was deposited on the copper circles on each substrate. Solders in most applications of this type are subjected to variable temperatures, resulting in the application of strain due to the difference in thermal expansion of each of the substrates. The nominal shear strain was calculated using the equation

$$\gamma = (\Delta\alpha * \Delta T * l) / h$$

where γ is the calculated shear strain

$\Delta\alpha$ is the CTE mismatch

ΔT is the change in temperature

l is the distance from the center of the sample to the joint

h is the height of the solder joint

This equation assumes that the strain is only a shear strain, which, especially for the samples containing FR-4, is not the case. Some joints have a large tensile component, depending on where they are located. An average value for the CTE mismatch is used, which assumes isotropic behavior of the solder.

2.2 Solder Deposition Methods

Tolerances on the consistency of the size of the joints become more critical and more difficult to achieve as the joints decrease in size and pitch. Many methods have been used to deposit solder onto discrete locations on a substrate. These include electroplating, stencil printing, physical vapor deposition, the use of pre-made solder balls, and 'ink jet' printing.[29] As the joints decrease in size, new deposition techniques must be employed. Solder paste is not reliable under 300μm pitch.[30] Pre-made solder balls cannot be synthesized with acceptable accuracy under 125μm. To fabricate small solder joints with fine pitch, photolithographic techniques are required. Electroplating worked the best with this type of fabrication and was used to deposit the solder onto the exposed copper pads.

2.3 Microstructure

It is expected that the small amount of solder present in microsolder joints will solidify into a non-equilibrium morphology that will be highly inhomogeneous and vary from joint to joint. This is a result of two effects present in the solidification of small

solder joints. First, the as-cast microstructure of solder joint is primarily dependent on the cooling rate which is inversely related to sample size. As joints and samples decrease in size, the cooling rate increases. Also, the amount of undercooling also plays a large role in determining microstructure. Large undercoolings were found to occur in the fabrication of microsolder joints.[31] Under these conditions, non-lamellar structures of primary Pb-rich dendrites supersaturated with Sn form within a Sn matrix containing randomly dispersed Pb particles. Upon further cooling, Sn precipitates out of the Pb-rich dendrites as the solubility decreases with temperature.

The as-cast microstructure of the microsolder joints no longer displays the lamellar eutectic microstructure found in larger joints (see Figure 2.3-1 and Figure 1.2-1). Therefore, the microstructural evolution and failure mechanisms found for these larger joints cannot be extrapolated to the smaller ones. In prior work on the large joints, it was found that an equiaxed band of coarser phase structure developed as a shear band where a fatigue crack would initiate and propagate to failure. Since the initial microstructure of the small solder joints does not appear to have any colony boundaries and is much different than the bulk eutectic microstructure, it is not known how the it will evolve or whether the eventual failure would be dependent on the microstructure. This study was undertaken in part to produce some initial observations along these lines.

3. Experimental Procedure

3.1 Sample Processing

Three different substrates were used: fused quartz wafers, p-type test silicon wafers, and 1/32" epoxy-fiberglass (FR-4) circuit board material. The quartz and silicon wafers were processed in the exact same fashion, while the FR-4 wafers were made slightly differently due to the thicker size and different metallization layers.

3.1.1 Quartz and silicon

The quartz and silicon wafers were cleaned in a H_2O_2/H_2SO_4 solution prior to processing. They were then rinsed in distilled water and spun dry. Metallization layers were sequentially sputtered onto the wafers using a Perkin-Elmer Randex radio frequency sputter coater. Ti/Cu/Ti (35nm /100nm /50nm) was used on the quartz and silicon. The wafers were primed using a oven set to 120°C containing hexamethyldisilazane (HMDS). OCG 825 (G-line) photoresist was applied automatically using an SVG Photoresist Coater, creating a 1.3μm layer. A pattern was exposed onto the photoresist using UV light in a GCA 6200 wafer stepper with a chrome mask. A schematic drawing of the mask design is shown in Figure 2.1-2 . A post exposure bake of one minute at 120°C was done followed by developing the resist on a SVG Photoresist Development track that automatically dispensed OCG 934 2:1 (G-line) developer. The resist was de-ashed using an oxygen plasma in the Microstripper. The resist was then hard baked for approximately one hour at 120°C. The exposed titanium was then etched in a 1-5% HF

solution until the copper layer was visible. Cu was plated, using a dc source and a copper sulfate and sulfuric acid solution, until the copper layer was 4-7μm above the resist layer. This was measured with an Alphastep 200 Automatic Step (contact) profilometer. Eutectic solder was then plated to the desired height using M&T Chemicals, Inc. TLF Non-Peptone Solder Plating Bath that contained fluoroboric acid with lead and tin fluoroborate. Because of the variability of the resultant composition of the plated metal inherent to this deposition technique, the actual composition of the solder was not precisely eutectic, but slightly Sn-rich (65-70% Sn). This was found by both quantitative stereology as well as with Energy Dispersive X-ray analysis.

3.1.2 FR-4

There were a few differences in the processing of the FR-4 samples. The FR-4 wafers came with a 10μm thick copper layer adhered onto the surface with epoxy. Therefore, only one layer of titanium was sputtered onto the surface to create a passivation layer. The FR-4 wafers were too thick be exposed in the wafers stepper and were exposed in a contact printer with slightly thicker (2μm) photoresist layer. Due to the high surface roughness of the copper (and consequently the titanium) on the FR-4, the plated copper could not be measured on the profilometer accurately. The roughness was not quantified, but was visible to the naked eye. The rest of the procedure was identical to the quartz and silicon.

3.1.3 Final processing

After stripping the resist with PRS-3000 Positive Resist Stripper, each wafer was dipped into glycerol to melt the solder bumps. The glycerol was heated to 215°C, and the wafer was immersed for 15 seconds. Each substrate was then diced into 7mm by 11mm pieces using various types of diamond blades on a Disco Automatic Dicing Saw.

Pieces from different wafer substrates were bonded together by optically aligning the plated solder on each substrate and compression bonding them using a M-8 Series Flip-Chip Bonder made by Research Devices, Inc. Kester's #186 rosin flux, type RMA (rosin, mildly activated), was applied before compression bonding to ensure the removal of the oxide layer during subsequent melting. The high-strain samples were made with one quartz and one FR-4 die while the low-strain samples were made with one quartz and one silicon die. After compression bonding each die from one quartz and one FR-4 or silicon wafer, all samples were put into a programmable reflow furnace to melt the solder together to form a joint. The furnace was purged with nitrogen and preheated to 300°C prior to the introduction of the samples. The profile consisted of a preheat of 170°C for 30 seconds, followed by a reflow step lasting 180 seconds that peaked at 290°C. The joints were cooled under nitrogen until they reached 150°C at a cooling rate of approximately 1°C/second. This was estimated from the description of the different cooling methods described in an earlier work,[17] and from estimations on the time to cool from the maximum temperature and 150°C. They were removed from the furnace and allowed to cool to room temperature in air.

3.2 Testing and Examination

One set of wafers (either quartz/silicon or quartz/FR-4) was used per test to avoid complications with run-to-run variability. Each wafer yielded about 45 die to make an equivalent number of samples per test. Many of the samples failed to align properly (most commonly in the z-direction) after fabrication. The acceptable samples were divided into three groups for examination and testing. The first group of samples was tested in thermal fatigue, the second set was annealed at the maximum temperature of the thermal cycle for equivalent amounts of time, and the last set was not subjected to any thermal treatment

To perform the thermal fatigue test, the first group of samples were placed in a Delta Design #9039 programmable furnace that cycled between 0-160°C with 5 minute hold times. Each cycle was approximately 24 minutes long. One sample was removed from the cycling furnace at 25, 50, 100, 250, 500, and 1000 cycles. Each sample was mounted and polished to examine the microstructure as the test progressed. Failure was first observed at 1000 cycles, and three failed samples were mounted and polished to observe fracture morphology from joint to joint as well as sample to sample. Another failed sample was pried apart to view the void morphology. They were separated by taping the back of each substrate to a piece of steel and pulling the two pieces of steel in tension. Because of the differing amounts of thermal expansion that each substrate undergoes with thermal cycling, a strain is imposed on the solder. The coefficient of thermal expansion (CTE) of each substrate is shown in Table 3.2-1 along with the CTE

mismatches and the corresponding shear strain imposed on the solder during thermal cycling.

Sample Name	Substrate	α ($*10^{-6}$)	$\Delta\alpha$ ($*10^{-6}$)	$\Delta\gamma$ (%)
High-Strain	FR-4	20.0	19.5	28 ± 7
	Quartz	0.5		
Low-Strain	Silicon	2.5	2.0	2.8±0.5
	Quartz	0.5		

Table 3.2-1: *Calculated Shear Strain of Thermally Cycled Samples*

Other thermal cycling conditions and reflow profiles were run for some initial tests to determine the reliability of the final test parameters chosen. The other test condition was not as severe (0-100°C, 10 minute holds) and was performed on larger joints (approximately 100μm) with the low-strain substrates. The quantitative microstructural results of these tests were not included in this study because the initial microstructure was not properly controlled.

The second set of samples were annealed individually in a low temperature furnace at 160°C for equivalent amounts of time as the cycled samples and then mounted in epoxy and polished. An equivalent amount of time was defined as the same amount of time that the cycled samples spent at 160°C. The cycled samples were held at 160°C for 5 minutes per cycle, i.e., $t_{anneal} = 5N$, where N = number of cycles. There is no standard for this type of testing, and other researchers have defined this as the amount of time of

one complete cycle.[24] One sample was annealed and observed per test condition. Test conditions of 50, 100, 500, 1000, and 2100 equivalent cycles were chosen. The third set of samples was mounted and polished in the as-cast condition to determine the morphology and consistency of the initial microstructure. One of these untested samples was pried apart to view the void morphology prior to testing as described previously.

The following steps were taken to reveal the microstructure after mounting each set of samples in epoxy. All polishing supplies used were manufactured by Buehler, except where noted. Samples were first ground to expose the joints using 240 grit silicon carbide paper. This was followed by 400 grit ground 90 degrees from the previous step. For grits 600-800, Microcut brand papers specially made for polishing soft materials were used. One micron cerium oxide (manufactured by Beta Diamond) on Microcloth was used for the first polishing step followed by 0.05μm Micropolish (aluminum oxide) on Microcloth. They were then etched in 5%HCl. The 0.05μm polish and etching steps often had to be performed more than once to remove embedded particles and edge rounding. Once an acceptable polish was achieved, 0.05μm silica was used on Microcloth for 30 seconds to enhance contrast. Photographs were taken on a optical microscope at 1000X (except where noted). A TOPCON 20KeV scanning electron microscope (SEM) was used to observe the fracture surfaces. Fracture surfaces were not coated with any conductive layers, so charging from the nonmetallic substrates and flux residue can be seen in some of the micrographs.

3.3 Quantitative Analysis

Quantitative analysis of the microstructures was performed by using the mean linear intercept method. Large amounts of error can be associated with this method unless statistically large amounts of data are collected. This was not the case in this study, so this method gives only a semi-quantitative measurement. The surface-to-volume ratio was tabulated and used as a parameter to characterize the microstructure and microstructural evolution of each sample. This parameter is an inverse length measurement, so the data produced was plotted in terms of the inverse surface-to-volume ratio. The area fraction of voids was measured using a line per unit length measurement. This was measured to obtain a semi-quantitative value of the void content in the as cycled samples.

4. Results and Discussion

4.1 *Sample Fabrication*

Chromium was the first adhesion metallization layer used to bond the copper layer to the quartz and silicon substrates. The initial thermal cycling tests revealed that the samples failed after 225 cycles through the Cr/Cu interface. Figure 4.1-1 shows the fracture surface of the silicon half of the sample. This fracture surface was found by Energy Dispersive X-ray analysis to be copper (with solder underneath) on the silicon side and chromium on the quartz side. Chromium was replaced by titanium and all failures of samples with this new metallization occurred within the solder. This was concluded to be due to the fact that the binary system of Cr/Cu does not form any intermetallics, while the Ti/Cu system does. Intermetallics, although brittle, are necessary to form a good bond between metal layers. They enhance bonding as long as their growth is not excessive, or the intermetallic is not excessively brittle. It was also found that the adhesive titanium layer had to be thicker than the passivation (top) titanium layer. If this was not the case, etching of the adhesion layer was observed during the passivation layer etch. This was assumed to occur through pinholes in the copper.

It was found that the smaller the volume of solder, the more difficult it was to fabricate joints with proper alignment. It is commonly stated that as the solder volume is increased, its centering force decreases, implying that it should be easier to align smaller joints.[32, 33, 34] However, most plots that show this effect also show that this is only true after a certain solder volume (typically around $0.4mm^3$).[32] Prior to this critical volume, the centering force actually decreases with decreasing volume. All of the joints in this

study were less than the critical value of $0.4mm^3$. This force is also affected by the reflow temperature. It is recommended that reflow temperatures not exceed 215°C and that time above melting stay below 30 seconds to maximize this parameter.[32] The joints in the study were reflowed at higher temperature than this recommendation as an attempt to reduce voiding,[23] so the maximum force was not realized.

The centering force is not the only parameter that effects alignment; it is also affected by other design and processing parameters. The variability of the solder volume per pad is a critical parameter in proper alignment of the joints.[33] The solder height of the joints tested varied from approximately 50-60μm, implying a variability of 5μm. This variation is constant for all joints fabricated in this study (regardless of joint height), and therefore becomes more of a concern as the joint volume decreases. Since all the component substrates were the same size for all samples, the weight of the component was constant. This weight, however, is distributed over a decreasing solder volume and decreasing centering force, making it more difficult to balance the forces and reach proper alignment. Therefore, in applications requiring smaller solder joints, it is critical that the design of the component be optimized for the volume of solder.

Although no precise measurements were made, it was noted that wafer samples had short storage lifetimes. The samples began to have solderability difficulties during the glycerin dip after only one month of room temperature storage. This is most likely due to intermetallic growth, as the presence of even 2-4μm of these compounds was found to reduce solderability.[11]

4.2 Qualitative Microstructural Analysis

4.2.1 Initial microstructure

The initial microstructure of three samples is shown in Figure 4.2.1-1 - 4.2.1-3. Three joints per samples are shown to display the consistency from joint to joint. There appears to be more consistency from joint to joint than from sample to sample, but even the sample to sample variation does not appear to be excessive. They are consistent enough that a general phase morphology can be observed. Each joint consists of large regions of the Pb-rich phase (dark region) surrounded by a background of Sn-rich phase (light region). Each phase also contains precipitates of the other phase within it. The Sn-rich precipitates within the Pb-rich phase appear to be slightly larger than the Pb-rich precipitates within the Sn-rich phase. The size of these precipitates was not quantitatively measured, but the Sn-rich precipitates appear to be approximately 1-5μm, while the Pb-rich precipitates appear to range from 0.5-3μm.

This fine-grained, globular, degenerate eutectic microstructure is observed in the samples used for thermal testing. This microstructure is similar to rapidly cooled larger joint samples whose cooling rate at least two orders of magnitude faster.[17, 35] The large Pb-rich regions in the initial test samples had more of a dendritic morphology rather than globular. One untested sample was made by reflowing on a hot plate at 250°C to observe the effect on microstructure. The hot plate was turned off, and the samples were left on the hot surface until the solder solidified. The microstructure of these joints, although much coarser than that of the samples that were used for testing, did not contain any

lamellar eutectic regions. The lamellar eutectic microstructure never formed in any region of any of the samples in this study. This same microstructure was observed in a prior study (see Figure 2.3-1) that attributed the lack of lamellar morphology to the large undercoolings that were found to occur upon solidification.[31]

Most joints contained voids. Prior work indicates that voids can originate from both evaporating flux and additives from plating baths.[23] Both flux and electroplating were used to fabricate the joints, so the large void content is not surprising. The voids varied greatly in size, percentage of joint area, and location within the joint. Figure 4.2.1-4 shows an SEM micrograph of an initial microstructure sample that was fractured in tension. Void content and morphology was not consistent from samples to sample or joint to joint. The presence of small voids in the cross sectioned samples typically appear as out-of-focus dark regions, often circular in shape. There are also embedded particles from polishing present. They appear darker and in better focus than the voids.

The width of the joints appears to vary, but this is more due to the varying plane of polish than any difference in actual width of the joint. Since the microstructure could possibly vary between the outside of the joint and the inside, microstructural analysis was only performed on the planes of polish where the copper pad was visible. This indicated that the plane observed was at or near the center of the joint.

All initial microstructure pictures shown are taken from the quartz and silicon samples. The initial microstructure of the quartz and FR-4 samples was not analyzed due to polishing difficulties. The reason for the difficulty was not determined definitively. It appeared possible that small pieces from the FR-4 would pull out and scratch the solder

or embed in the Pb-rich phase. Qualitative observation indicates that the as-cast microstructure was coarser as well as possibly containing less lead than that of the quartz and silicon samples. These samples also appeared to be qualitatively consistent from joint to joint as well as from sample to sample.

4.2.2 Cycled microstructural evolution and failure

The microstructure of the low-strain samples is shown in Figures 4.2.2-1 a-f. As the number of cycles increases, the large Pb-rich regions appear to break up and the Sn-rich precipitates within them join the background Sn-rich phase. By 500 cycles, there are large regions within the Pb-rich phase that contain no Sn-rich precipitates. The precipitates that do remain are large and near the edge of the Pb-rich region. It appears that both types of precipitates diffuse toward their parent phase, changing their size distribution from a large number of small particles with a few large particles toward a smaller number of larger precipitates. This is not a surprising results, as this migration reduces the amount of interphase surface area. This general trend was also observed with the initial test samples, even without having a constant initial microstructure.

By 1000 cycles, every joint had failed in the low-strain samples. No cracks were seen in any of the joints observed in the 500 cycle samples. No samples were observed between 500 and 1000 cycles, so a more precise number of cycles to failure cannot be determined. At 25 cycles, all joints in the high-strain samples had failed. In the 50 cycles sample, the approximately 30% of the joints had failed as well. However, the cracks in the 100 cycles samples had not propagated the full length of the joint, but had initiated in

about one-third of them. After 250 cycles, all joints in all samples had failed. Like the low-strain samples, the exact number of cycles to failure is not known. One joint in the 25 cycles high-strain sample was found to be an exception to the polishing difficulties and is shown in Figure 4.2.2-2. Due to the wide variation in test conditions and samples used in earlier works, it is difficult to compare these fatigue lifetimes to other studies. It is interesting to note, however, that the lifetime of the barrel-shaped, low-strain samples is one-third the lifetime time of the hourglass-shaped joints as a prior work predicted.[13]

The fatigue cracks in both the low and high-strain samples occurred almost exclusively through the solder near the solder-intermetallic interface. For this geometry, most finite element models predict the corners of the joint to be the location of highest stress.[3] They conclude that cracks will initiate here as was observed in this study. No coarsened band was observed to form prior to fracture as was observed in the larger joints. This band formed in all of the larger joints, even those that had degenerate microstructures.[16]

Most commonly, the cracks joined voids that were present in the joint. If a void was present in the sample, the cracks invariably followed a path that crossed a void. Since fatigue cracks initiate near the substrate, they have a smaller amount of material to travel through if a void is located near the substrate. The amount of material that crack would have to traverse would be even less if the void were large, so that crack *propagation* would be more rapid. This appears to support the earlier results that indicate that voids near the substrate are the most detrimental to the fatigue life of solder joints.[23] As stated before, voids in surface mount joints are stress risers. However,

thermomechanical fatigue is under strain control, so the voids may not have as much of an effect. Joints with voids may be more compliant and resist crack *initiation* better. Voids may actually act as stress relievers and crack arresters. In one study, a crack initiated and propagated toward a void.[36] The dissipation of the crack energy into the void arrested the crack. Samples between 500 and 1000 cycles would have to be observed to determine if this occurred in this study. However, the effect on lifetime is less than twofold.

The overwhelming majority of the failed joints resembled the one shown in Figure 4.2.2-3. This void morphology was observed from joint to joint as well as sample to sample. It seems intuitive that since the microstructure coarsens with cycling, the void distribution should coarsen as well, which this morphology seems to imply. However, the void make-up varied greatly from sample to sample and joint to joint in the initial samples as well as from joint to joint in the cycled samples prior to failure (see Figure 4.2.1-4 and 4.2.2-4). More samples between 500 and 1000 cycles need to be examined to formulate a definitive conclusion as to the evolution of void size distribution.

It was assumed that the origin of all voids observed was from processing. Therefore, the total void content would not change with time, only the distribution may be effected. However, creep is coupled with fatigue in this type of testing, and creep mechanisms of void formation and coalescence could be occurring. The occurrence of creep microvoid coalescence damage could explain why the fatigue cracks observed were wider than would be expected for fatigue. These voids would be expected to be smaller than those observed, but they could play a role in the failure and could be effecting the void size measurements. The possible effect of creep was not studied in this work.

The location of the fatigue cracks did not appear to be correlated with any particular phase or coarsening feature. However, the relatively large width of the cracks along with the large volume of voids made this difficult to determine with any certainty. Therefore, it appears that the location of greatest stress (which depends on joint geometry) and the location of the voids (if present) dominated any microstructural coarsening feature in determining the location of the fracture.

4.2.3 Annealed microstructural evolution

The microstructures of the annealed samples are show in Figures 4.2.3-1 a-e. A consistent trend is a little more difficult to see in these photographs. This may be due to the variation in the polarization of the light in the optical microscope or in the level of etching. It could also be due to the variation in the initial microstructure. A greater number of samples per test condition and a greater number of tests would need to be performed to determine the exact cause.

Like the cycled samples, the annealed samples also contain large Pb-rich regions surrounded by a background of Sn-rich phase. The Sn-rich precipitates within the Pb-rich region appear to be smaller in these samples. The size distribution of these precipitates appears to shift from a few large particles and several small particles to even fewer medium sized particles and even more small particles. The size distribution of the Pb-rich precipitates within the Sn-rich background appear to follow a similar trend as the thermally cycled samples: shifting from a large number of smaller particles to a smaller number of larger particles. The microstructures of the annealed samples appear to be

more coarse and coarsen more over time. These samples were not expected nor observed to fracture, because no load was placed on them.

4.3 Quantitative Microstructural Analysis

4.3.1 Initial microstructure

A plot of the inverse surface-to-volume ratio of three different samples is shown in Figure 4.3.1-1. The inverse surface-to-volume ratio is tabulated to use in the cycling and annealing data sets. The same trends are seen if the surface-to-volume ratio were used to plot initial microstructure data. Three joints of sample one and three, and five different joints of sample two were examined and measured. Each data point corresponds to the average value of all measurements taken for one joint. The maximum average value per joint calculated was 2.13, and 1.40 was the minimum value. Table 4.3.1-1 shows the average surface-to-volume ratio values for each sample. Combining all initial microstructural data yielded an average value of 1.75, with a standard deviation of 0.63 for all measurements.

Sample	Inverse Surface-to-Volume Ratio (μm)	Standard Deviation (all measurements)	Standard Deviation (averages)
1	2.02	0.61	0.13
2	1.67	0.56	0.31
3	2.13	0.65	0.35

Table 4.3.1-1: *Inverse Surface-to-Volume Ratio of the Initial Microstructure*

This is a rather large standard deviation, so that the initial microstructure does not appear to be consistent on a quantitative basis using this measurement parameter. There also seems to be the same level of consistency from joint to joint as sample to sample, contradicting the qualitative observations. This standard deviation was taken for each surface-to-volume ratio measurement. If the standard deviation of the average surface-to-volume ratio for each joint is taken, it is much lower, but still large. A phase size measurement for each phase would most likely show more consistency than the surface-to-volume ratio, since the later value does not take into account the fact that there are two phases. The surface-to-volume ratio is a point per unit length measurement, and each Sn/Pb intersection was counted; giving more of an average phase size of both phases, rather than each individual phase. However, it was anticipated that the microstructure would be inhomogeneous, and this is what is observed here.

4.3.2 Cycled microstructural evolution and void content

The inverse of the surface-to-volume ratio is plotted verses number of cycles as shown in Figure 4.3.2-1. The curve fit shown is a linear fit, which appear to be a good fit. The lowest value was 1.75 and the highest was 2.20, a difference of less than 0.5. Large amounts of error was associated with the small sample size of data collected. However, all the thermal fatigue data seemed to follow a similar trend.

The area fraction of the voids observed in the cross section of the joint was quantified using a line per unit length measurement to see if there was any trend to indicate void agglomeration. Figure 4.3.2-2 is a plot of the percent void area verses the

number of cycles. Each data point is an average value for one joint in the corresponding sample. No consistent trend could be extracted from this data. A cross section of four joints from the 100 cycles sample is shown in Figure 4.3.2-3. In two of the joints, only the metallization layers are visible in the plane of polish observed, and this leads to a measurement of 100% area fraction of void. While it is possible that the voids do agglomerate into one large void as the number of cycles increases, this cannot be concluded definitely from these measurements. Data between both the 250 and 500 cycles and especially between 500 and 1000 cycles would need to be collected and more measurements taken to determine whether or not a trend exists. The void content values for the 1000 cycled samples are most likely lower than the real content due to the fact that one line of the grid predominately fell very close to the substrate and managed to miss the extremely large void that occupies much of the cross section. Since only five lines were taken per joint, the actual result could be higher than reported here, but more measurements would need to be taken to determine if this is the case. Regardless of whether or not this trend exists, the effect of the voids on fatigue lifetime is less than twofold.

4.3.3 Annealed microstructural evolution

The inverse of the surface-to-volume ratio is plotted verses the square root of time as shown in Figure 4.3.3-1a. Included in the plot is a linear curve fit which does not appear to fit the data very well. It was anticipated that the data would decay as the square root of time according to diffusion trends. A very good linear fit is found if the

initial data points are excluded (Figure 4.3.3-1b). This was done in an earlier work for thermal cycling data with a similar improved fit.[24] The fact that the initial data points do not fit well with the rest could be due to the level of inhomogeneity of the initial microstructure, or could be due to the high level of error associated with the data points. The microstructure could be homogenizing early on, and then coarsening. This would account for the initial data points falling lower than the curve fit. This homogenization could be the size of the Sn-rich precipitates changing with the change in solubility with temperature. This is discussed further in the next section.

4.3.4 Thermal cycling versus annealing

Figure 4.3.4-1a shows the cycled data plotted along with the annealed data. The data is plotted in terms of distance versus time, so the number of cycles was converted to the equivalent amount of time. Since it was expected that the surface-to-volume ratio for the annealing data would decay as the square root of time, a curve fit of time to the one-half is included on this plot. A second fit is shown in Figure 4.3.4-1b with the initial data points excluded, as explained above, yielding a better fit. It appears that the microstructure of the annealed samples coarsens faster than the cycled samples, but tapers off quickly. This coarsening trend observed in this plot is the exact opposite of what has been reported before for larger joints.[24] If just the *shape* of the curves is viewed, some similarities can be seen (see Figures 4.3.4-1b and 4.3.4-2). The shape of the curve of the coarser data (annealing in this study; cycling in the other) was non-linear, and was better fit by excluding the initial points. The more linear plots (cycling in this study;

annealing in the other) fell below the non-linear data. It is not known if this small similarity holds any significance since there are many differences in the two studies. The initial microstructure of the prior work was of the lamellar eutectic variety, so a direct correlation was not necessarily expected. The thermal fatigue tests were operated at different temperatures, 'equivalent' time was defined differently, a different quantitative microstructural parameter was used to measure the coarsening.

The thermally cycled microstructure of this study did not coarsen as quickly as the annealed microstructure. This could not be due to a difference in the amount of time at 160°C, since equivalent time was defined as the high temperature hold time. Recrystallization could play a role. As the temperature drops during the cooling part of the cycle, a force is felt by the solder and a strain is induced. With this strain, there is a driving force upon heating for the grains to recrystallize and then grow. Therefore, the grains would not just be coarsening the entire time at the high temperature hold, but would also be recrystallizing. This dynamic recrystallization would lead to less coarsening over time than annealing, as the grains are refined (during cooling) and then coarsened (during high temperatures) every cycle. Therefore, one would expect an equiaxed microstructure (Figure 4.3.4-3) if recrystallization were the primary phenomenon occurring, but this is not observed. The strain is small and is most likely lower than the critical amount of strain needed to recrystallize at 160°C.

Another possible explanation for this coarsening behavior has to do with precipitation. The solubility of Sn in Pb is higher at elevated temperatures, but drops quickly with temperature. This is common behavior for a dual phase alloy. The phase

diagram for Sn/Pb is shown in Figure 4.3.4-4. As the temperature increases during cycling, the precipitates start to redissolve into the phase in which it is embedded and shrink in size. This occurs until the temperature begins to drop during the second half of the cycle. At the lower temperatures, the parent phase is supersaturated with the minor constituent and a driving force exists to reprecipitate this phase. The Sn reprecipitates and then coarsens. This effect retards the coarsening as a significant part of the microstructure is being refined with each cycle.

The trend for the annealed samples resembles that of the high temperature part of the cycling trend. Following reflow, the Pb-rich region is supersaturated with Sn due to the rapid cooling. Sn precipitates out at room temperature to relatively large size due to low solubility. During annealing, the solubility of Sn in Pb is at a constant value, and the size of the Sn-rich precipitates can more closely reach an equilibrium value; accounting for the trend in size distribution toward smaller precipitates. As this equilibrium value is reached, the size of Sn-rich precipitates decreases as they partially redissolve. At longer annealing times, they migrate toward the parent Sn-rich region. Some also coarsen within the Pb-rich region. This would lead to the annealed samples having a larger coarsening rate.

5. Summary and Conclusions

New fabrication issues must be addressed when manufacturing devices with small joints. Some general conclusions on the fabrication of devices with small, fine pitch joints can be drawn from this study. To maintain proper alignment, it is even more important that 1) the solder volume be optimized for chip design and weight so that the centering force can fully align the substrates, 2) an equal solder volume and composition be present on each pad, 3) storage times be kept to a minimum (less than one month at room temperature), 4) reflow temperatures and times be kept under 215°C for under 30 seconds to optimize the centering force. In general, the smaller, fine pitch joints are more sensitive to many issues that are also important in the fabrication of larger joints

Initial microstructures for smaller joints do not contain any of the lamellar eutectic morphology, even with very slow cooling rates, due to large undercoolings. As an attempt to keep a constant as-cast microstructure, all parts should be reflowed at the same time, because the small solder joints are more sensitive to the inherent run-to-run variability of the same reflow profile. The joints reflowed at the same time had similar microstructural morphology from joint to joint as well as sample to sample. Although there are similarities in this general morphology, the initial microstructure was found to be inhomogeneous. Measuring the average phase size for *each* phase was a better method of checking the consistency from joint to joint when compared to the surface-to-volume ratio. Voids occupied a large percentage of joint volume. Many joints included voids whose diameter were on the order of the height of the joint.

Thermal fatigue experiments showed failures of the 70/30 Sn/Pb joints between 500 and 1000 cycles under 2.8% strain, and between 25 and 250 cycles under 28% strain; with a temperature change from 0-160°C and five minute holds. These are shorter lifetimes than with an equivalent amount of strain on the larger joints. However, the larger joints had a much different geometry, so a direct lifetime comparison is not valid. A geometric factor would need to be used, but the correct parameter for this is not yet known. No consistent trend in void distribution was measured. Voids had less than a twofold effect on the fatigue lifetime.

The microstructural coarsening during cycling appeared to have a linear dependence on time, while the coarsening during annealing roughly followed the expected square root of time dependence. The coarsening during annealing was more rapid than during thermal cycling but tapered off at a faster rate. The curves intersected close to the number of cycles to failure. The difference in coarsening behavior was concluded to be due to the reoccurring dissolution and precipitation that occurs during cycling which retards coarsening when compared to annealing.

Most conclusions on these testing results are somewhat tentative, as this was an initial observation of the thermal behavior of this new technology. In general, more tests need to be run, and more samples need to be observed per test condition to be able to obtain more quantitative results and make more firm conclusions. This is a more realistic undertaking now that the thermal behavior of small solder joints has be observed.

6. References

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FIGURES

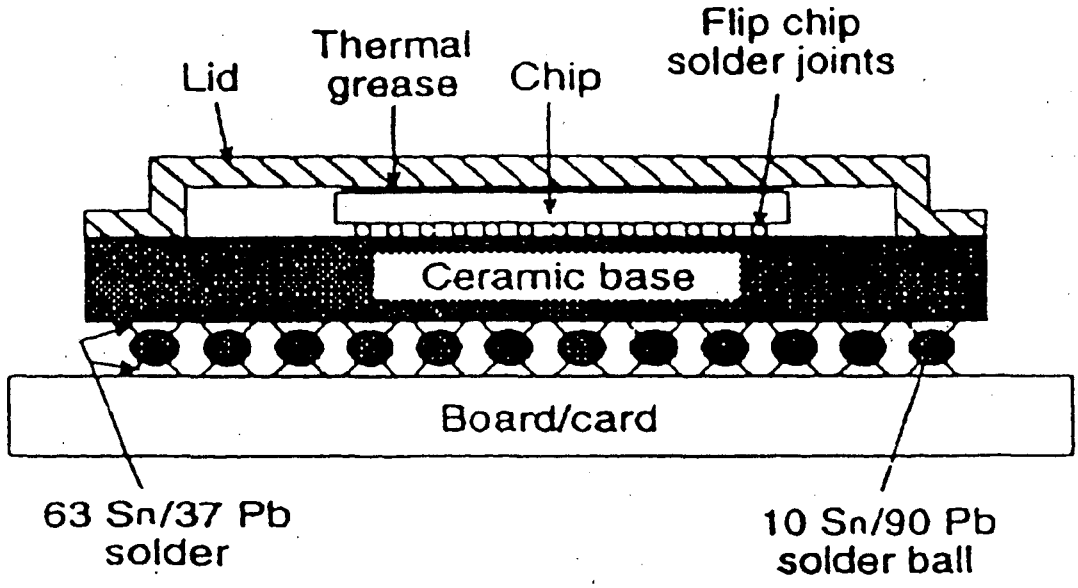

Figure 1.1-1: *Schematic illustration of a common flip-chip joint configuration. Taken from Ball Grid Array and Flip Chip Technologies: Their Histories and Prospects by Bruce M. Romanesco*

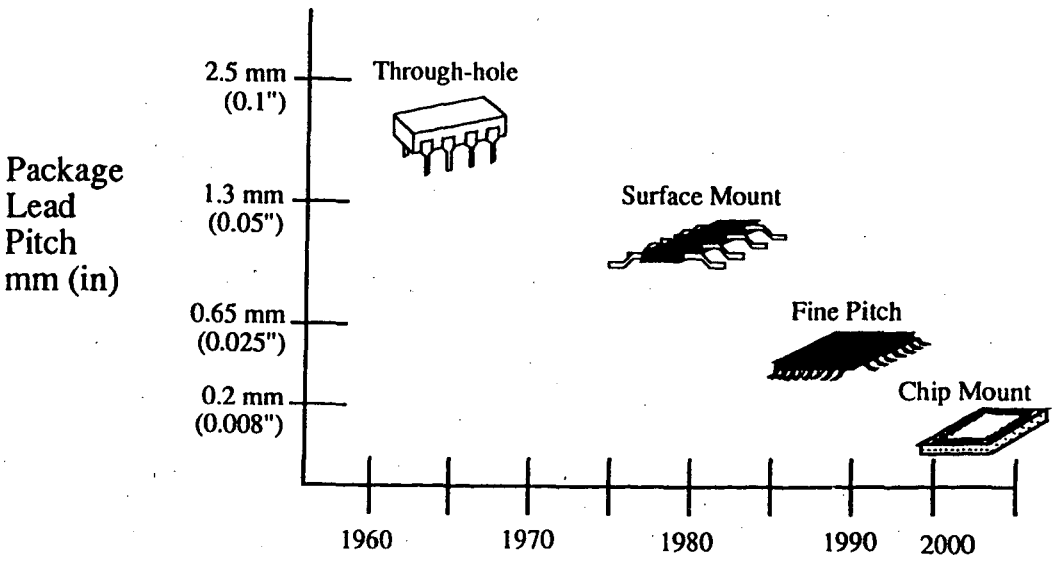

Figure 1.1-2: *Evolution of electronic packaging. Taken from Fine Pitch Surface Mount Technology: Quality, Design, and Manufacturing Techniques by Philip P. Marcoux, Van Nostrand Reinhold, 1992*

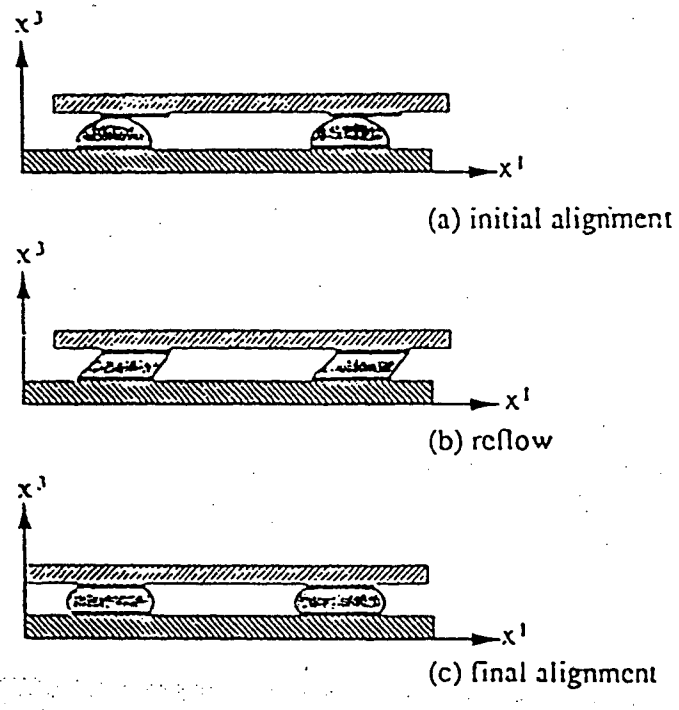

Figure 1.1-3: *Joint configuration during reflow. Taken from S.K. Patra, S.S. Sritharan, and Y.C. Lee, "Quantitative Characterization of a Flip-Chip Solder Joint", Journal of Applied Mechanics, Vol. 62, June 1995*

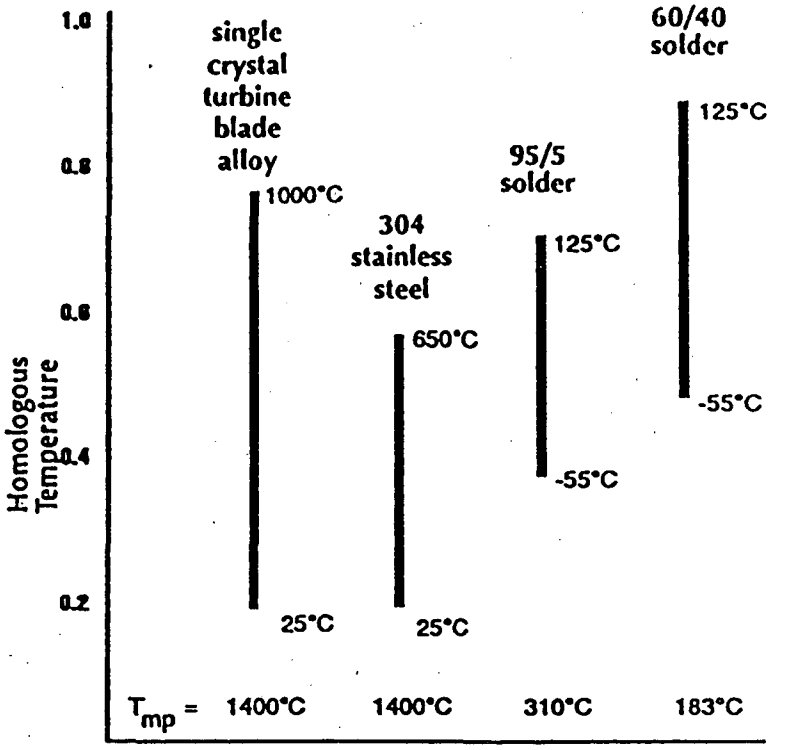

Figure 1.1-4: *Comparison of homologous temperatures in service. Taken from W. Jones, "Fatigue Life Prediction of Solder Joints, The Metal Science of Joining, Ed. M.J. Cieslak, J.H. Perepezko, S. Kang, and M.E. Glicksman, The Minerals, Metals, and Materials Society, 1992*

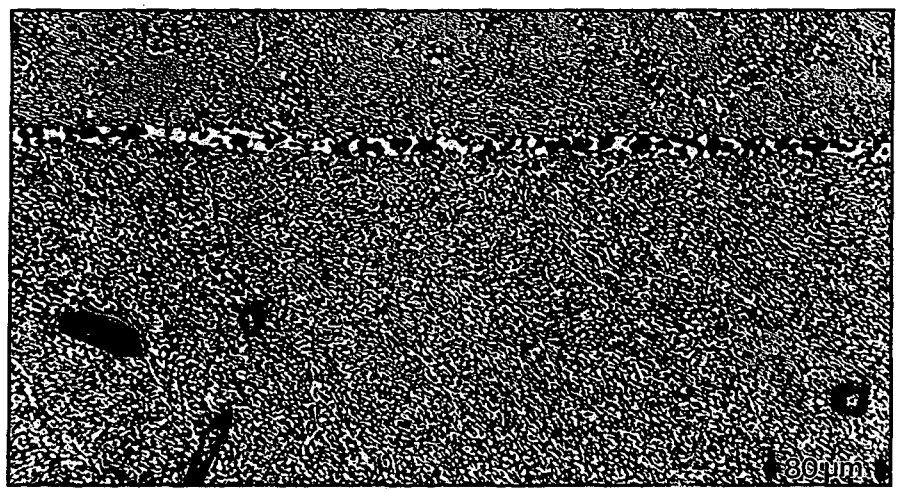

Figure 1.2-1: *Microstructure of a large solder joint with an equiaxed shear band. Taken from D. Tribula, D. Grivas, D.R. Frear, and J.W. Morris, Jr., "Microstructural Observations of Thermomechanically Deformed Solder Joints", Welding Research Supplement, October 1989*

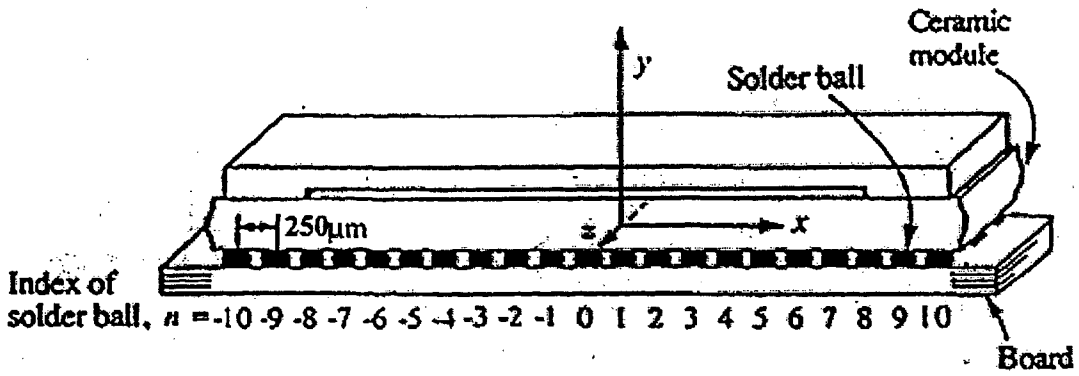

Figure 2.1-1: *Schematic illustration of test samples in cross section. Modified by B.L. Boyce from Y. Guo, C.K. Lim, W.T. Chen, C.G. Woychik, "Solder Ball Connect (SBC) Assemblies under Thermal Loading: I. Deformation Measurement Via Moiré Interferometry, and its Interpretation", IBM Journal of Research and Development, Vol. 37, No. 5, September 1993*

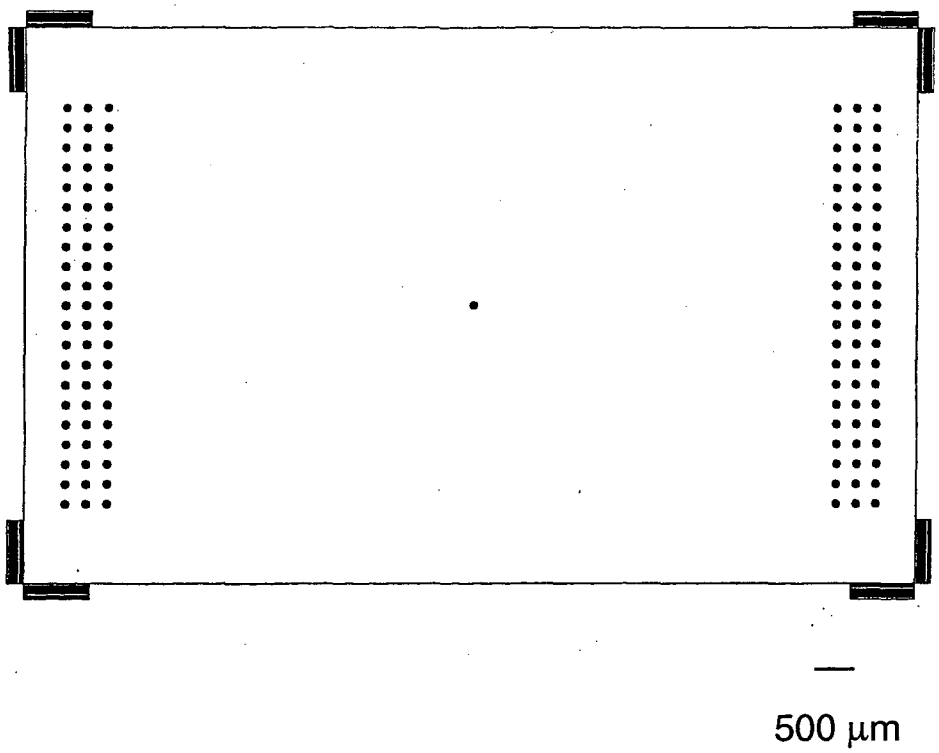

Figure 2.1-2: *Schematic illustration of test sample mask pattern*

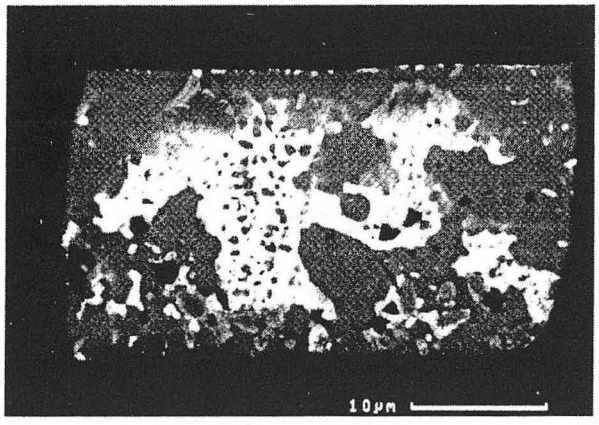

Figure 2.3-1: *Initial microstructure of a microsolder joint. Taken from N.R. Green, J.A. Charles, and G.C. Smith, "Solidification and Microstructure of Eutectic Pb-Sn Microsolder Bonds", Materials Science and Technology, Vol. 10, November 1994*

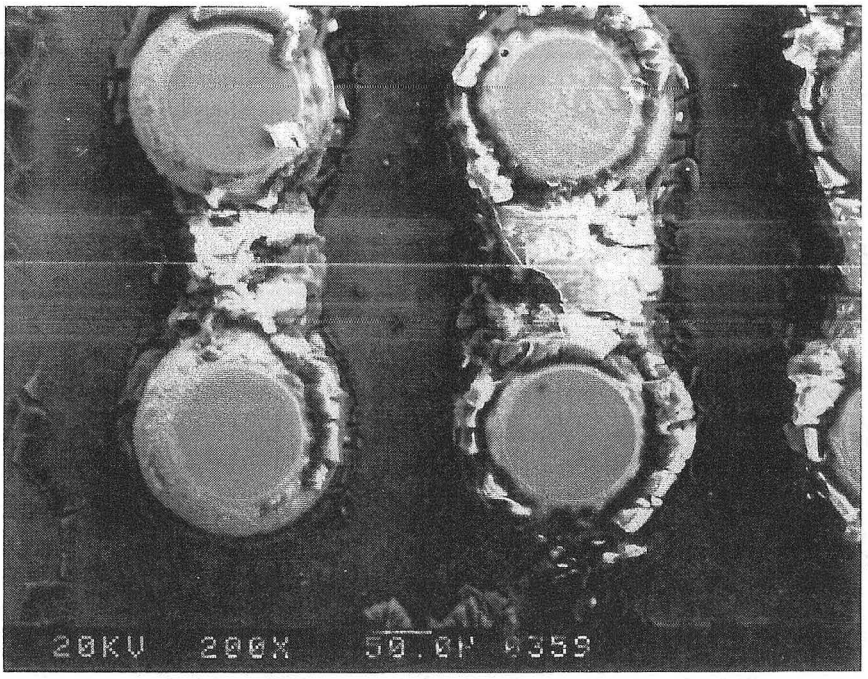

Figure 4.1-1: *Fracture surface of an initial test sample*

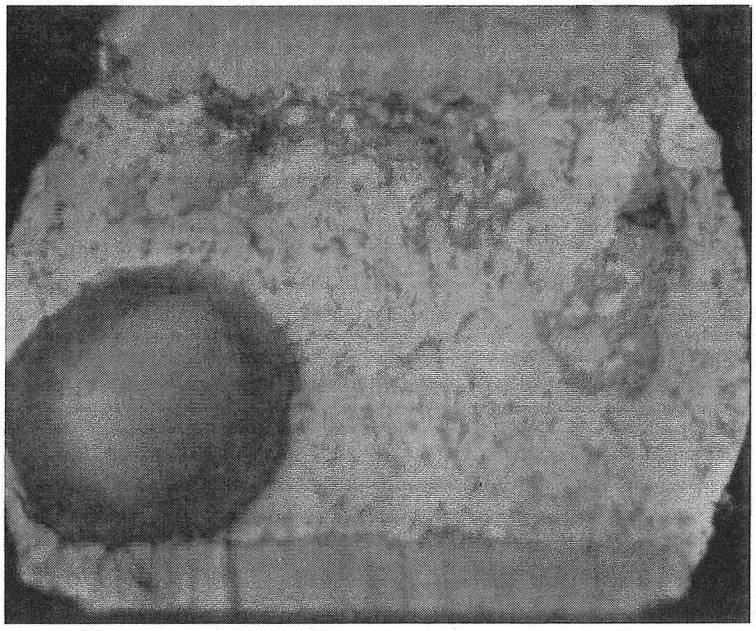

Figure 4.2.1-1 (a): *Initial microstructure of test sample one, Joint 1*

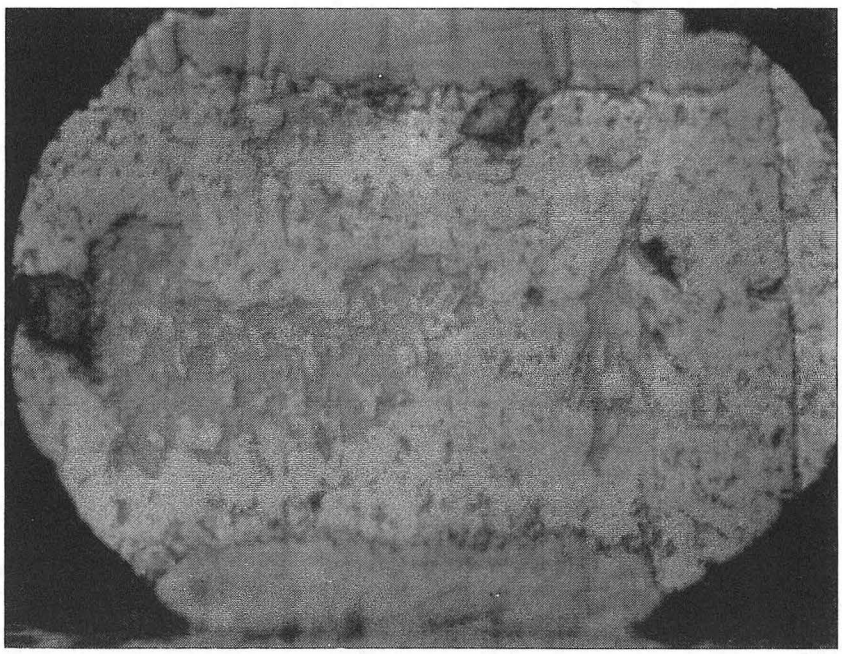

Figure 4.2.1-1 (b): *Initial microstructure of test sample one, Joint 2*

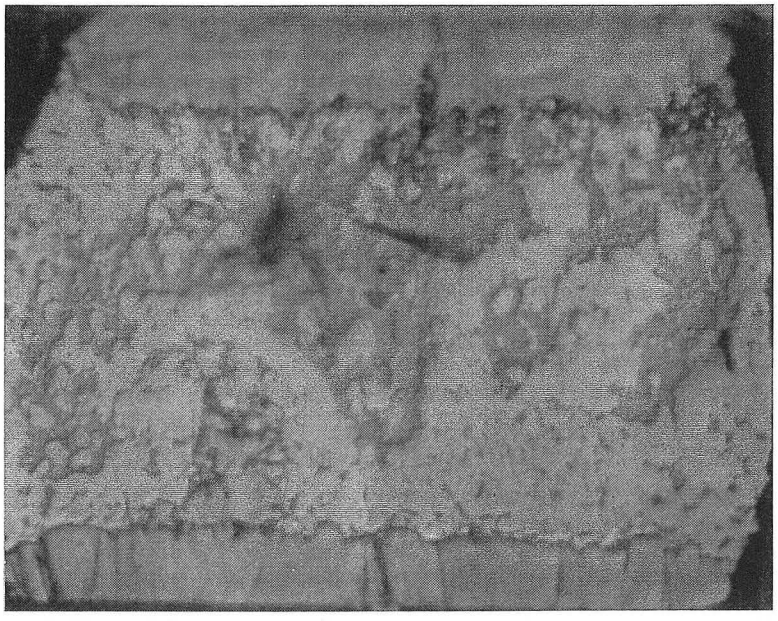

Figure 4.2.1-1 (c): *Initial microstructure of test sample one, Joint 3*

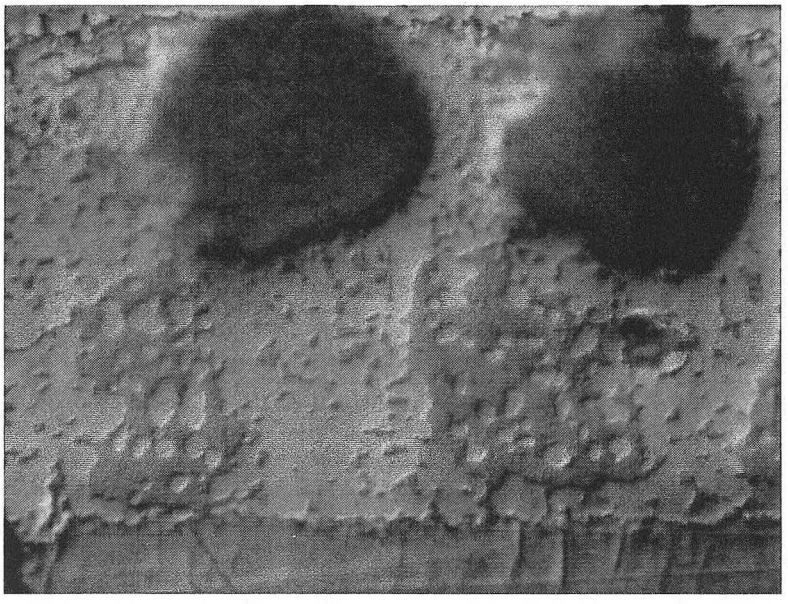

Figure 4.2.1-2 (a): *Initial microstructure of test sample two, Joint 1*

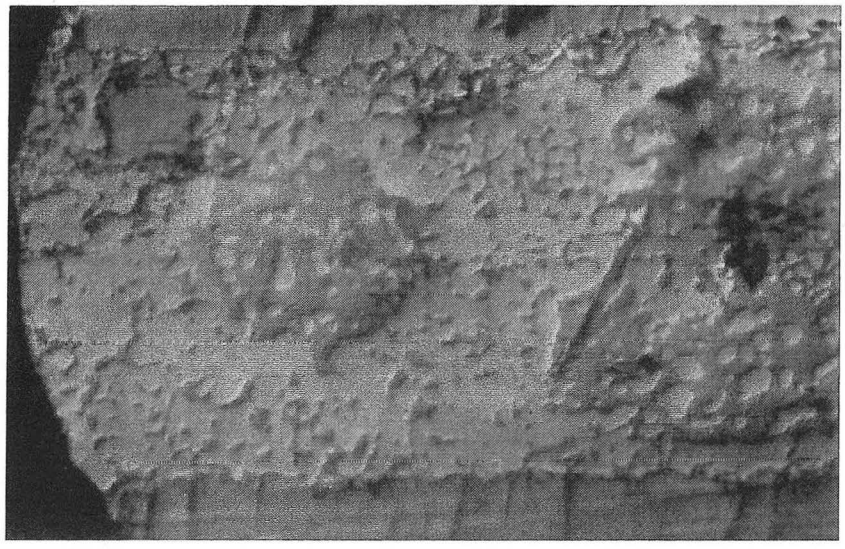

Figure 4.2.1-2 (b): *Initial microstructure of test sample two, Joint 2*

Figure 4.2.1-2 (c): *Initial microstructure of test sample two, Joint 3*

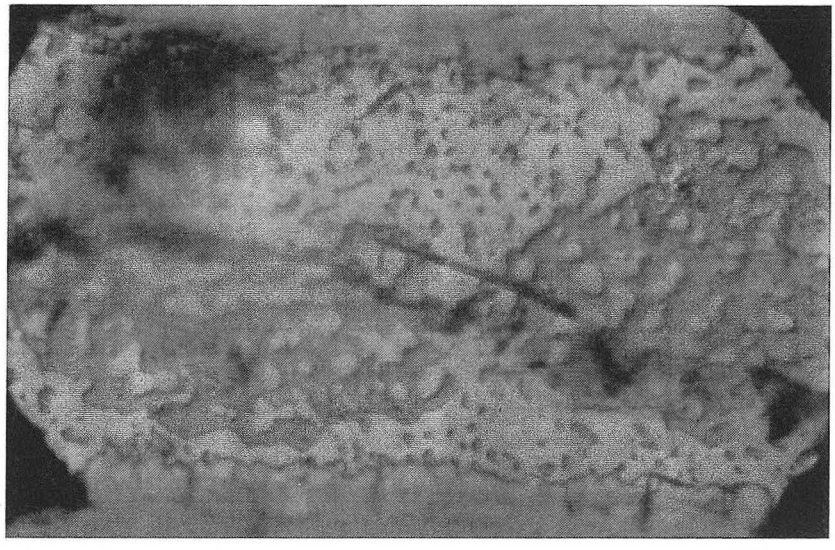

Figure 4.2.1-3 (a): *Initial microstructure of test sample three, Joint 1*

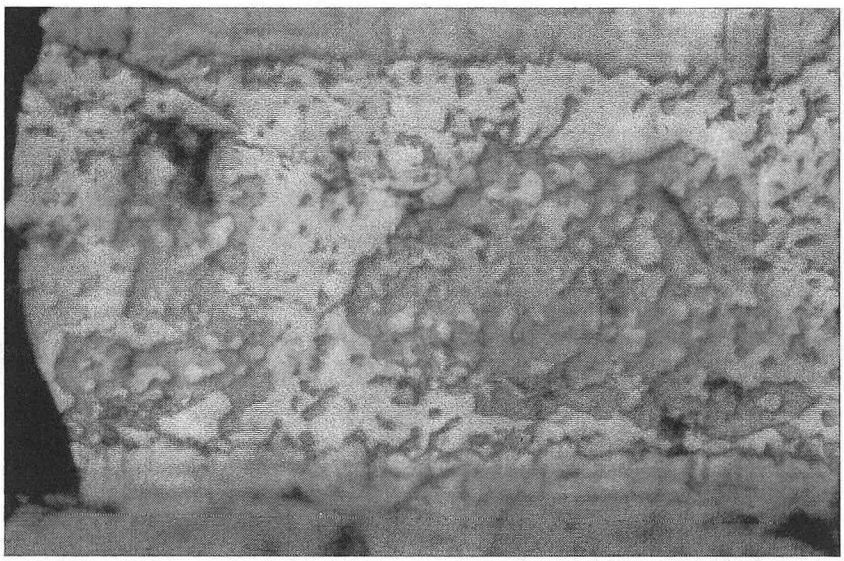

Figure 4.2.1-3(b): *Initial microstructure of test sample three, Joint 2*

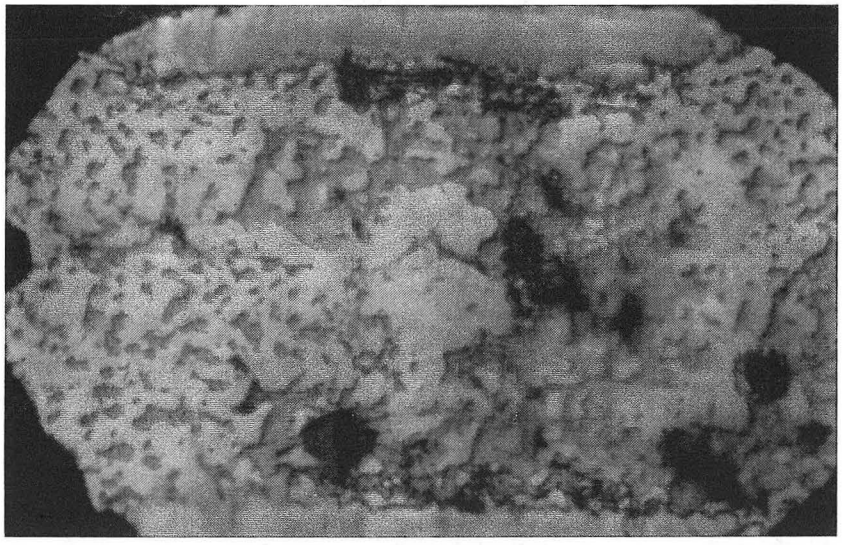

Figure 4.2.1-3 (c): *Initial microstructure of test sample three, Joint 3*

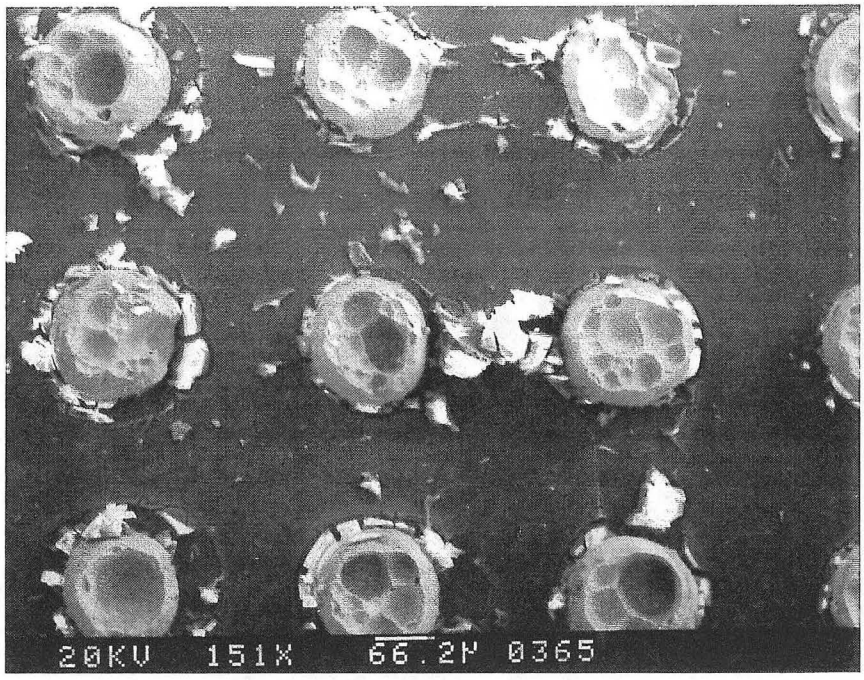

Figure 4.2.1-4: *Fracture surface showing void content of the test samples prior to testing*

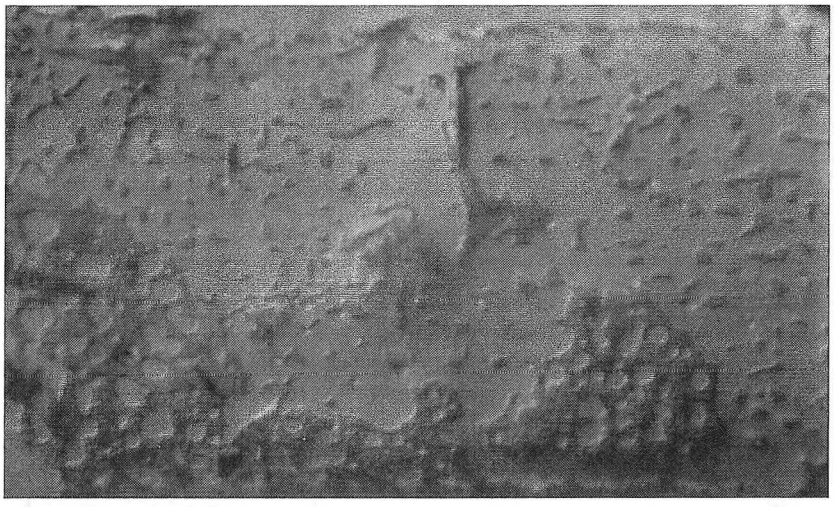

Figure 4.2.2-1 (a) *Microstructure of the thermally cycled low-strain samples, cross section; 25 cycles*

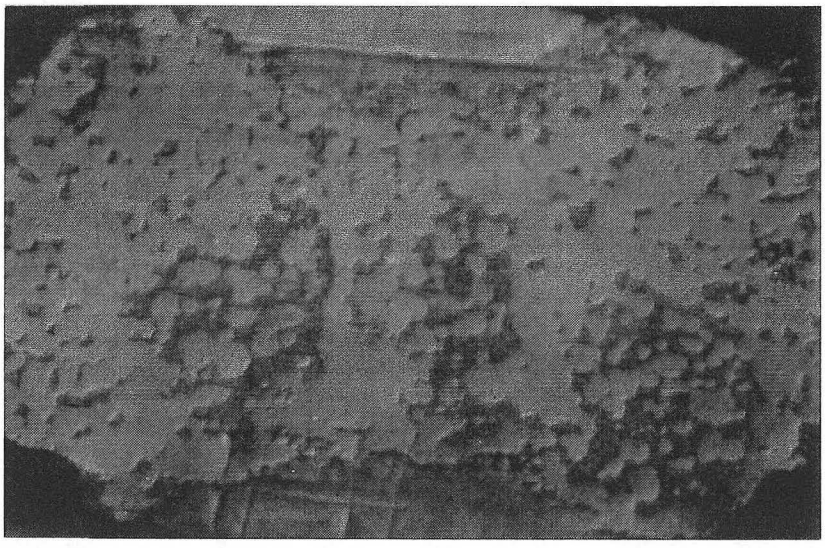

Figure 4.2.2-1 (b) *Microstructure of the thermally cycled low-strain samples, cross section; 50 cycles*

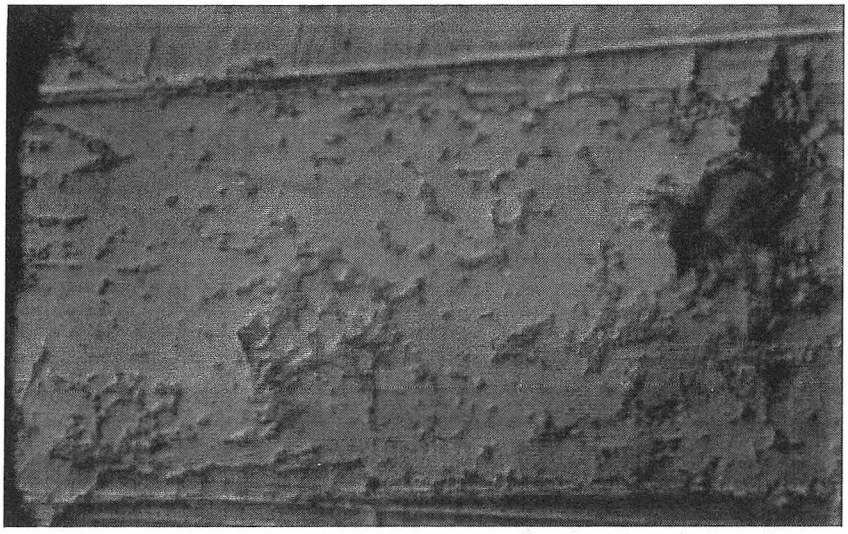

Figure 4.2.2-1 (c) *Microstructure of the thermally cycled low-strain samples, cross section; 100 cycles*

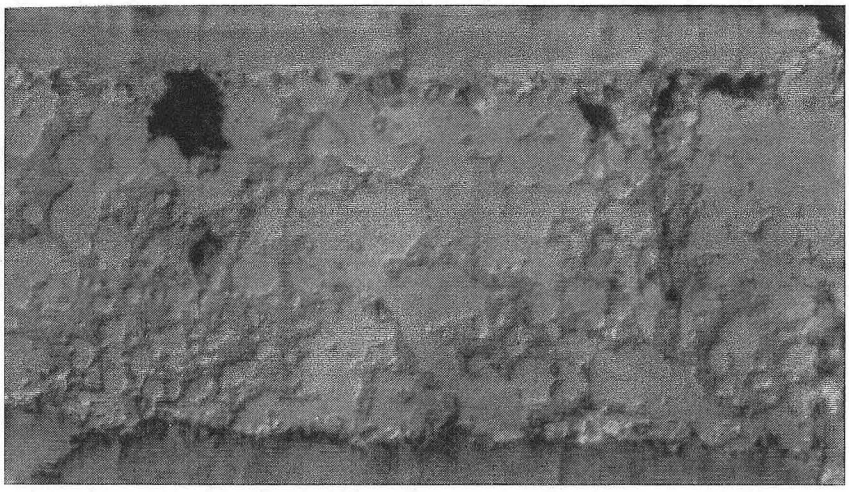

Figure 4.2.2-1 (d) *Microstructure of the thermally cycled low-strain samples, cross section; 250 cycles*

Figure 4.2.2-1 (e) *Microstructure of the thermally cycled low-strain samples, cross section; 500 cycles*

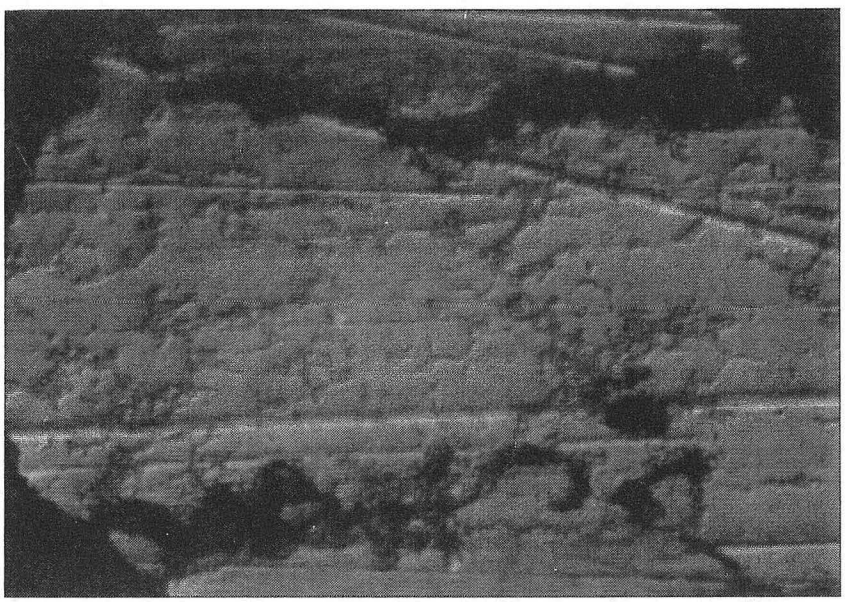

Figure 4.2.2-1 (f) *Microstructure of the thermally cycled low-strain samples, cross section; 1000 cycles*

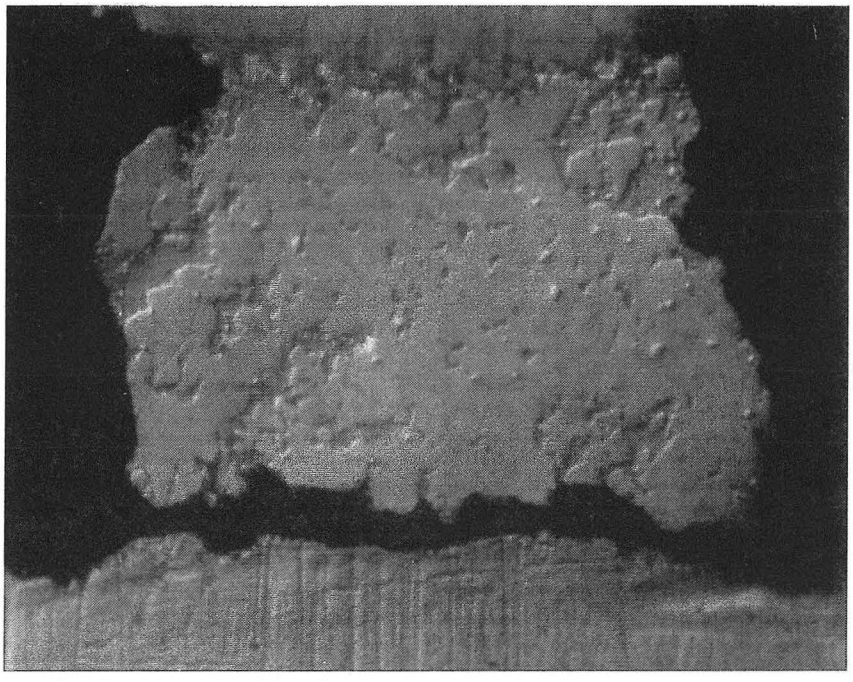

Figure 4.2.2-2: *Microstructure of the 25 cycles high-strain sample, cross section*

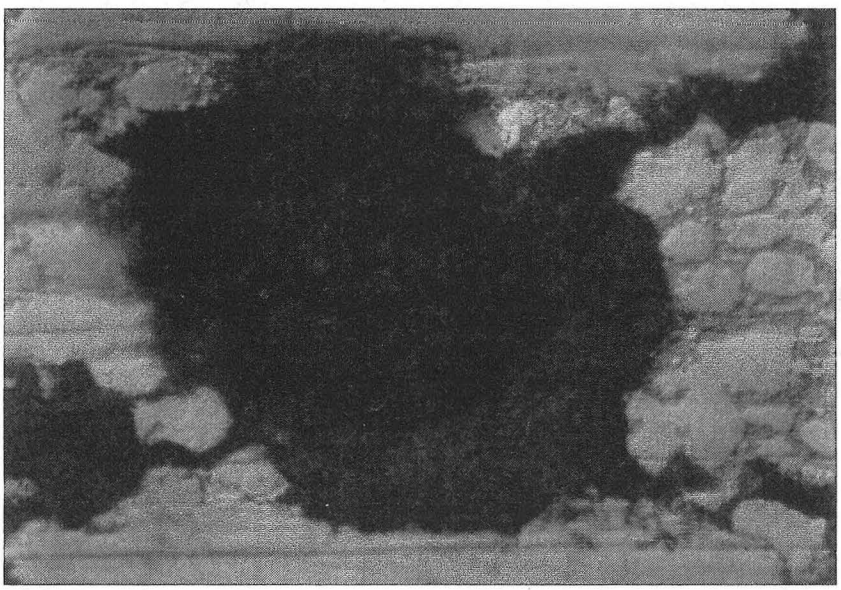

Figure 4.2.2-3: *Microstructure of the dominant void morphology in failed low-strain samples, cross section*

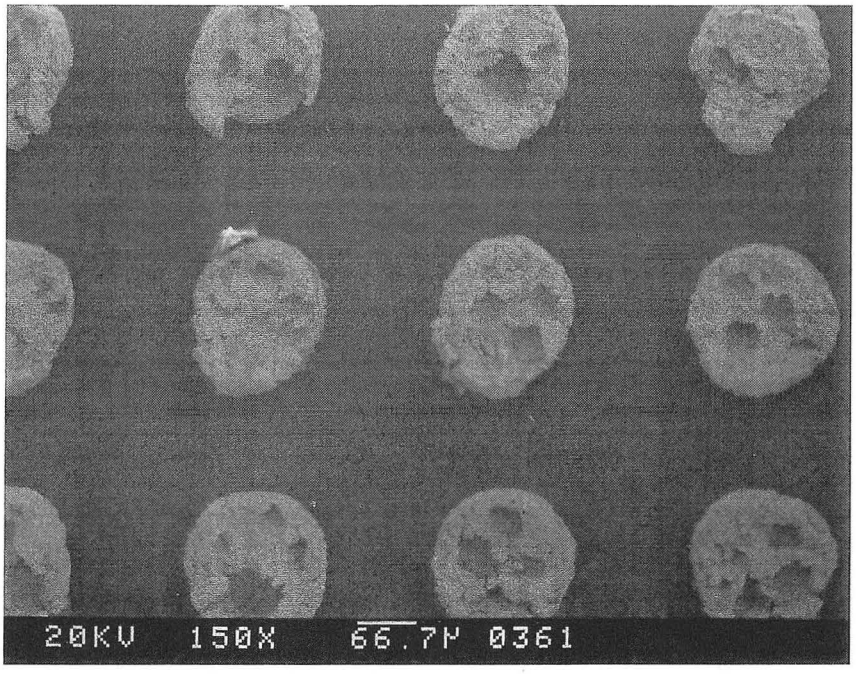

Figure 4.2.2-4: *Fracture surface showing void content of the failed low-strain samples*

Figure 4.2.3-1 (a) *Microstructure of the annealed low-strain samples, cross section; 50 equivalent cycles*

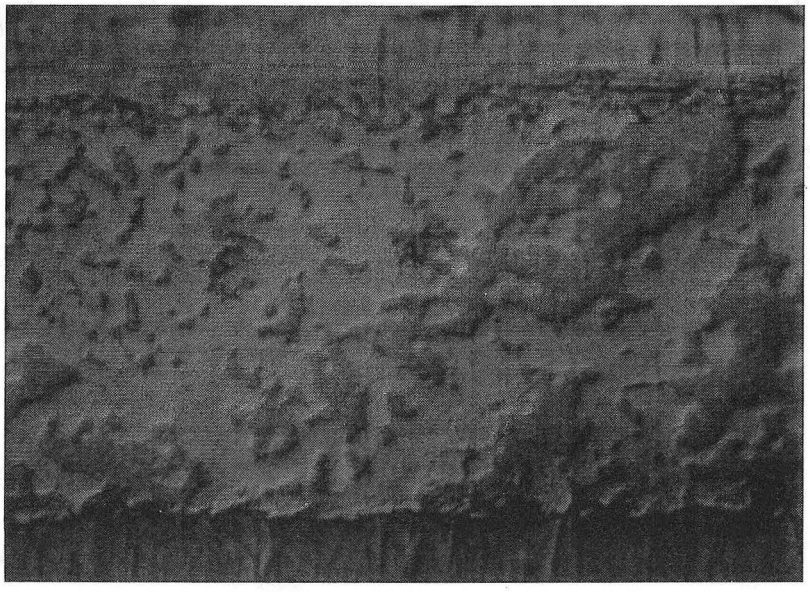

Figure 4.2.3-1 (b) *Microstructure of the annealed low-strain samples, cross section; 100 equivalent cycles*

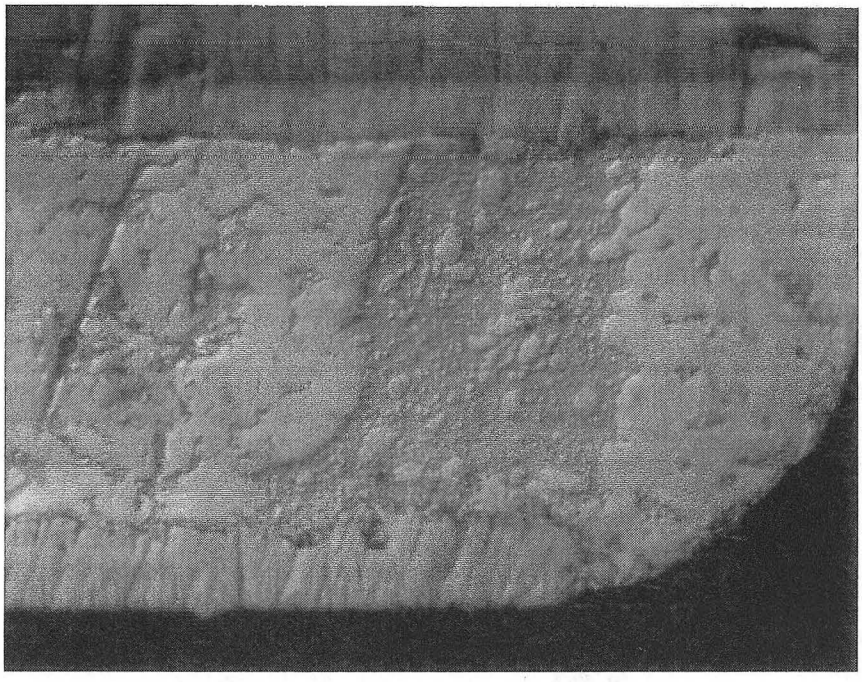

Figure 4.2.3-1 (c) *Microstructure of the annealed low-strain samples, cross section, 500 equivalent cycles*

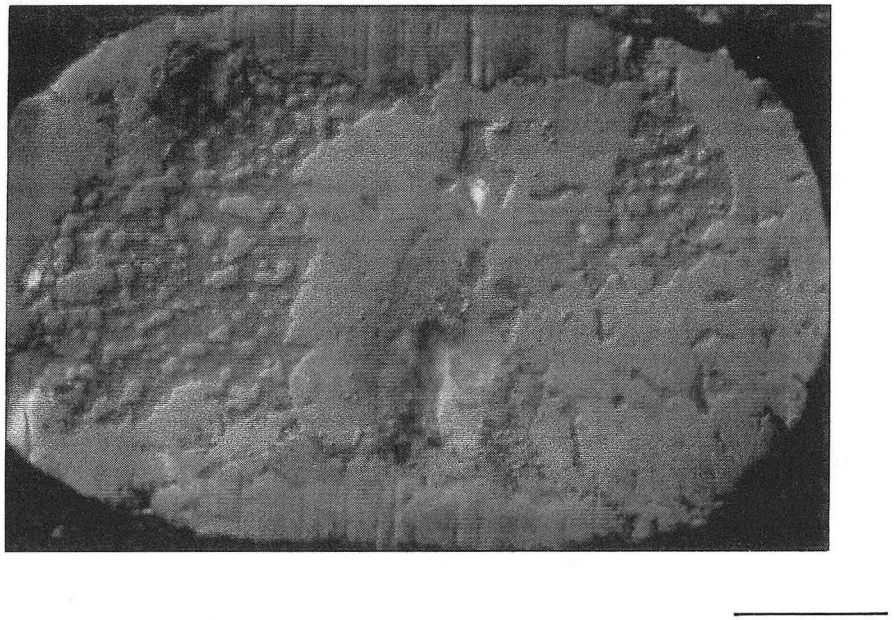

Figure 4.2.3-1 (d) *Microstructure of the annealed low-strain samples, cross section; 1000 equivalent cycles*

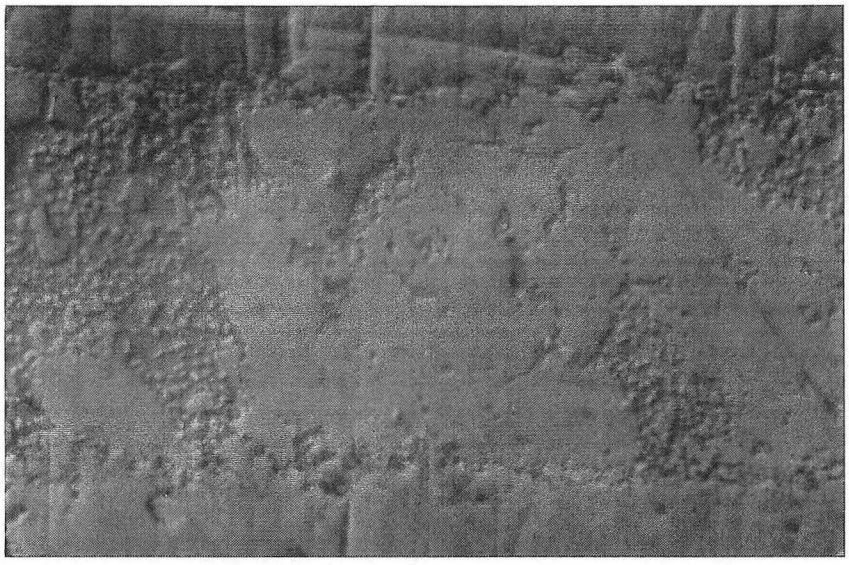

Figure 4.2.3-1 (e) *Microstructure of the annealed low-strain samples, cross section; 2100 equivalent cycles*

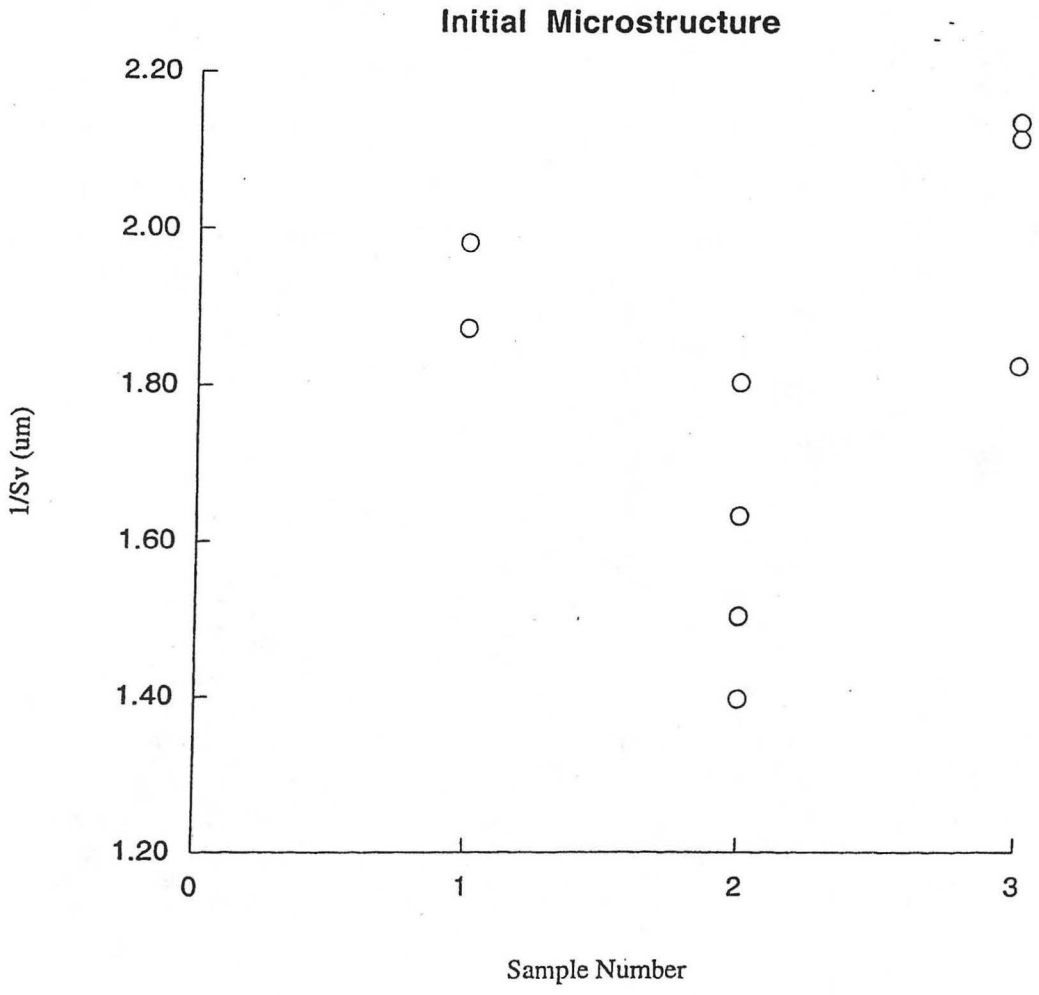

Figure 4.3.1-1: *Plot of the inverse surface-to-volume ratio for the initial microstructure samples*

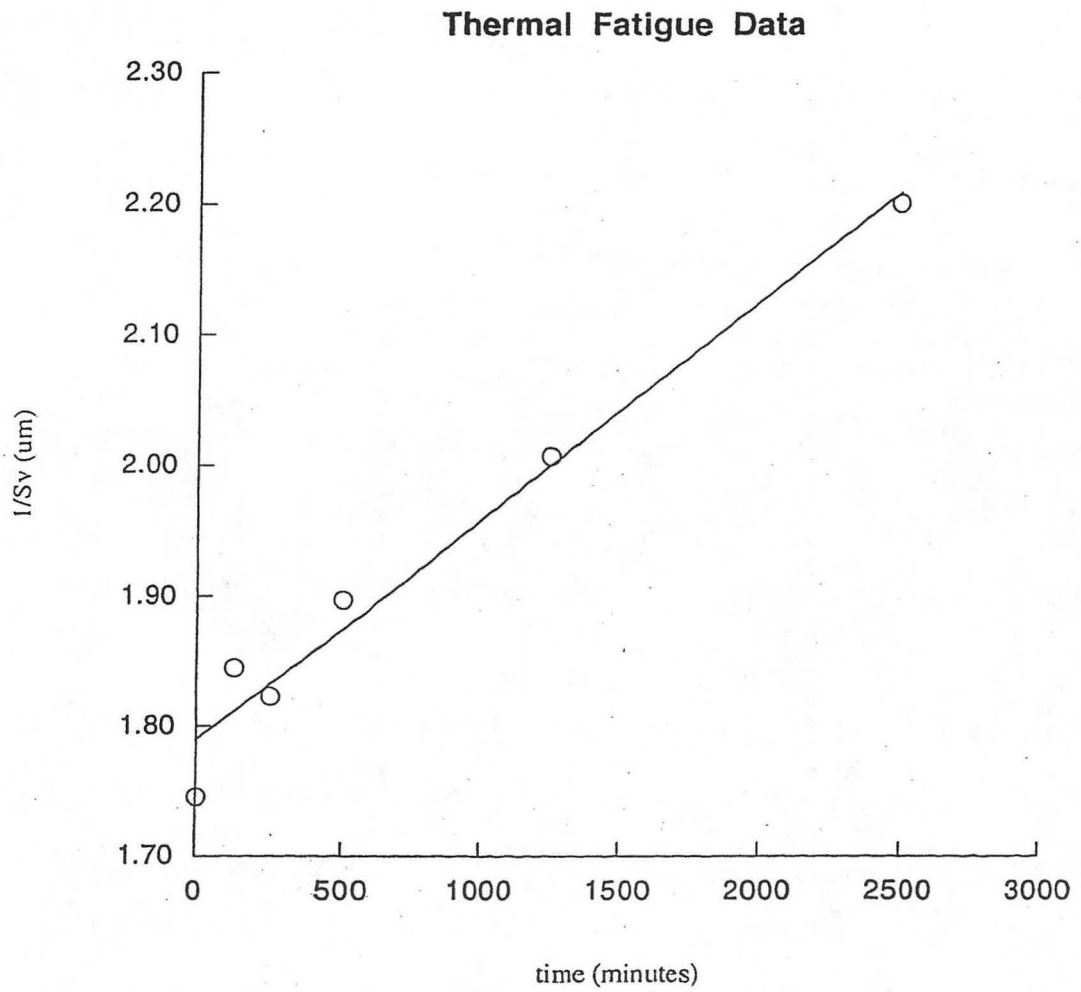

Figure 4.3.2-1: *Plot of the inverse surface-to-volume ratio verses the number of thermal cycles*

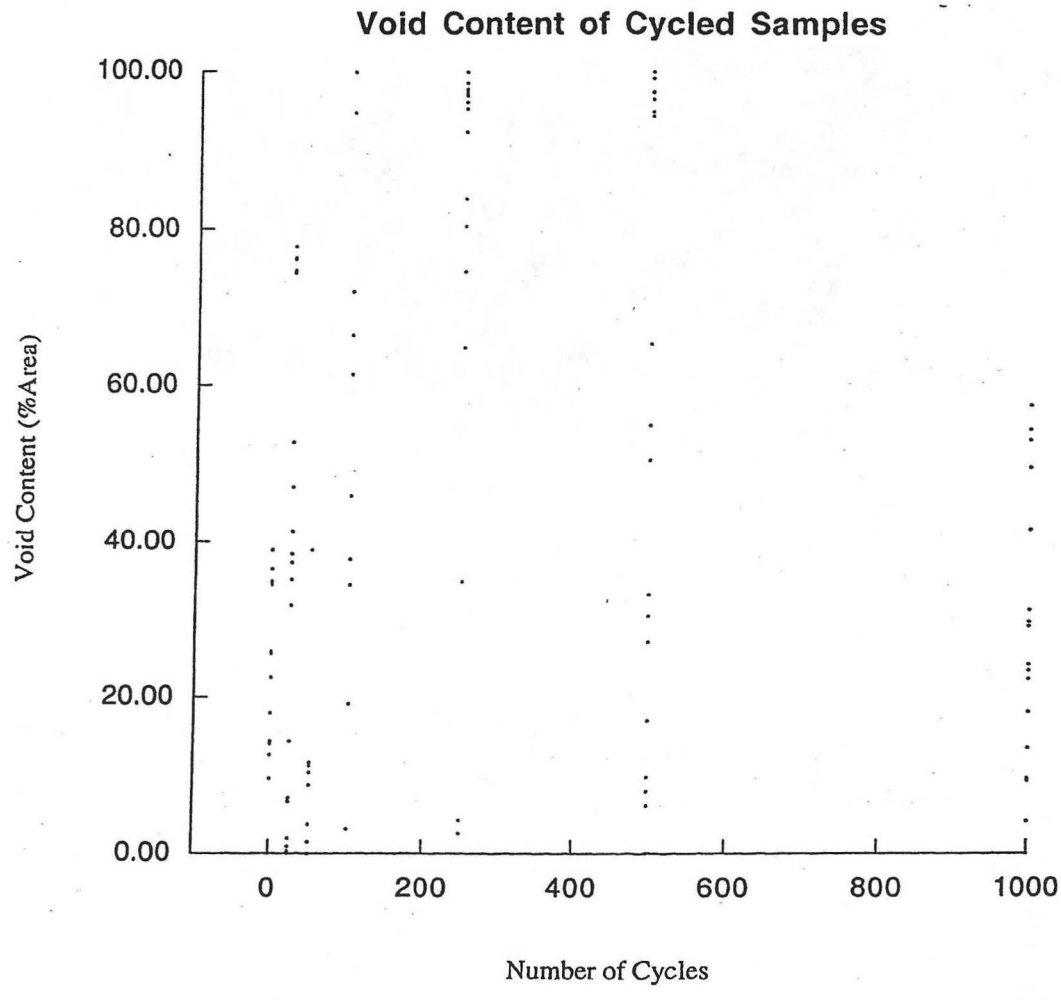

Figure 4.3.2-2: *Area fraction of voids (%) versus number of thermal cycles*

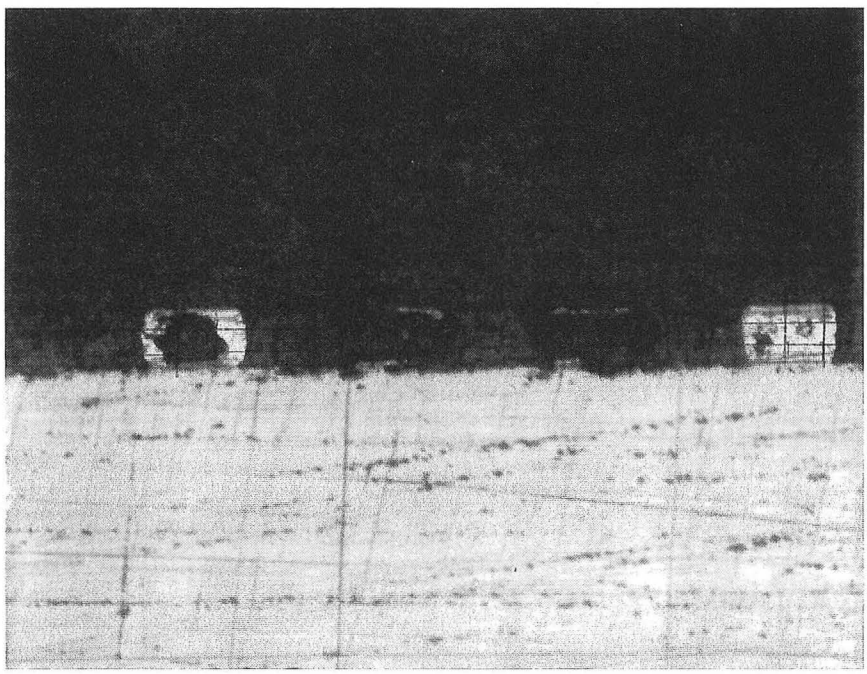

Figure 4.3.2-3: *Void content of 100 cycles sample with measurement lines shown, cross section, 100X*

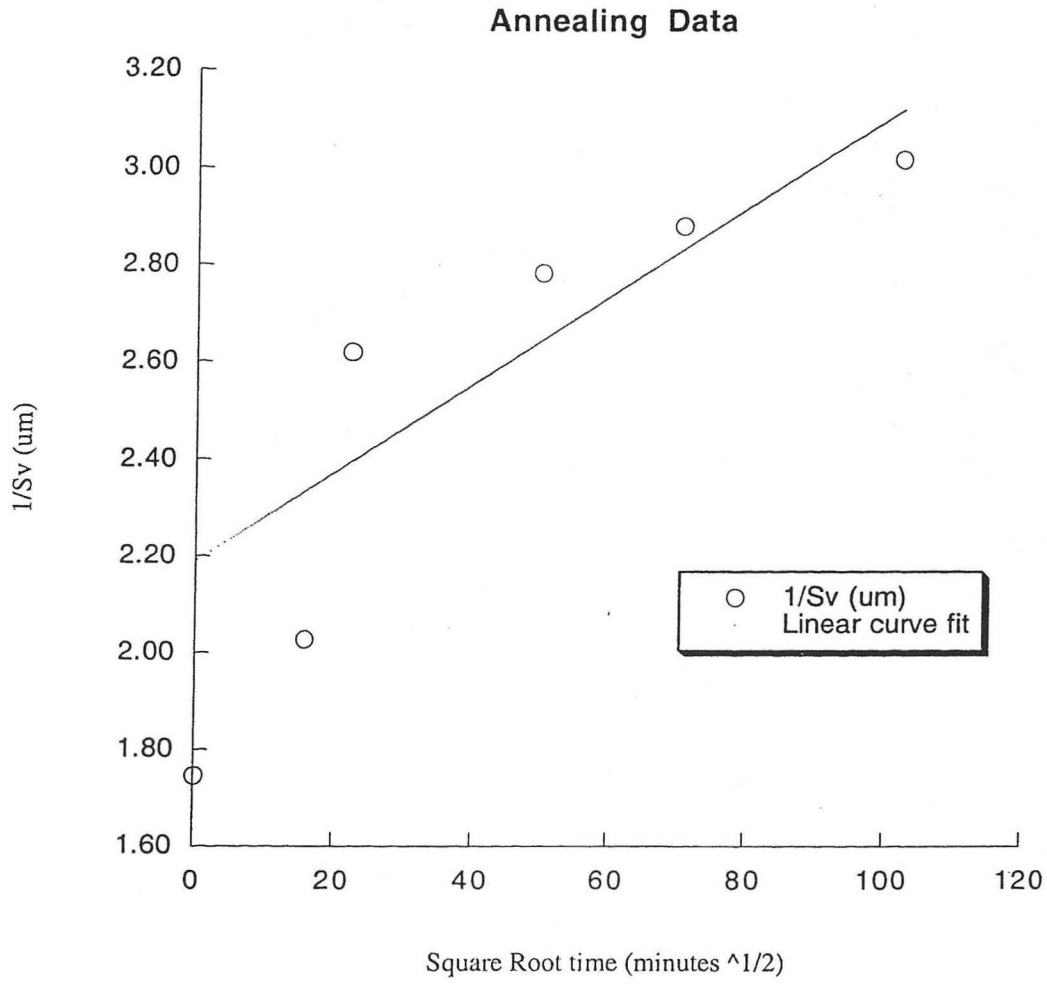

Figure 4.3.3-1a: *Plot of the inverse surface-to-volume ratio verses square root of time for annealed data*

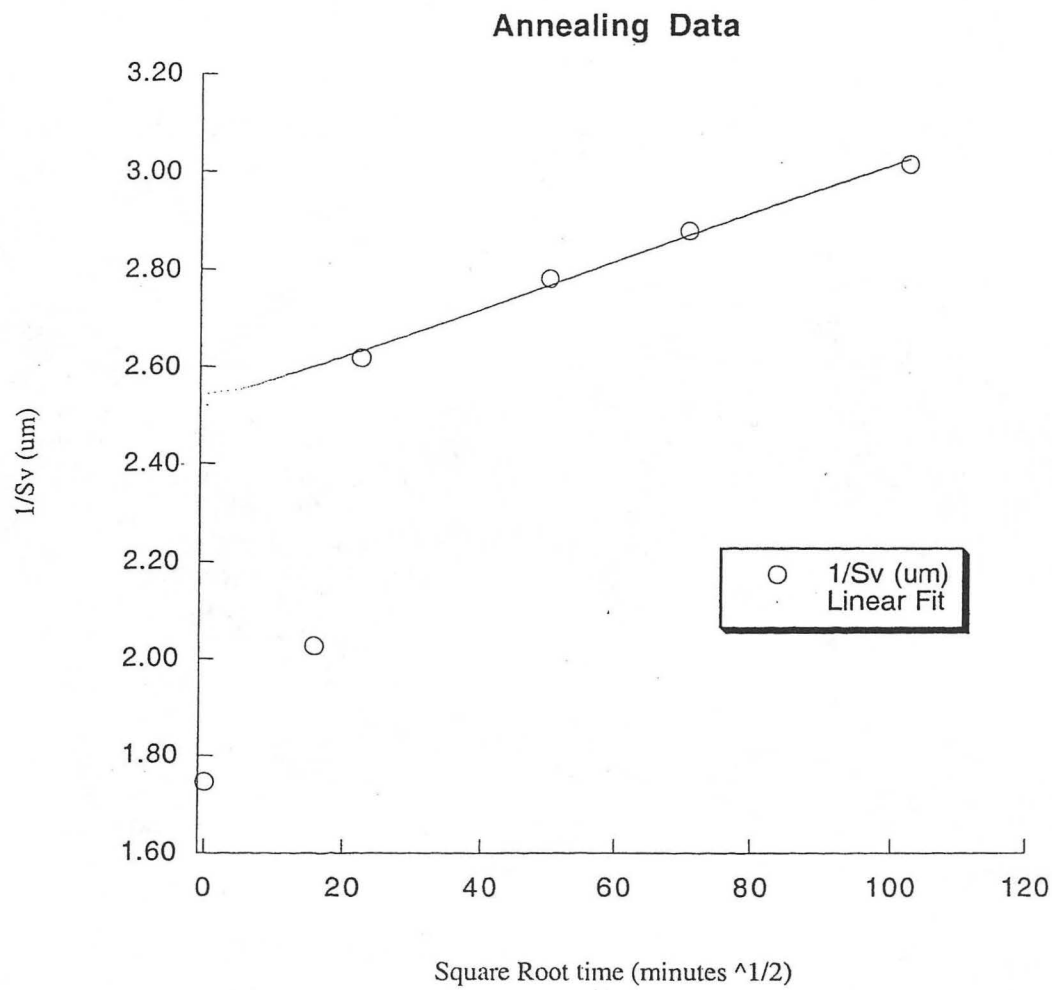

Figure 4.3.3-1b: *Plot of the inverse surface-to-volume ratio verses square root of time for annealed data, with a modified curve fit*

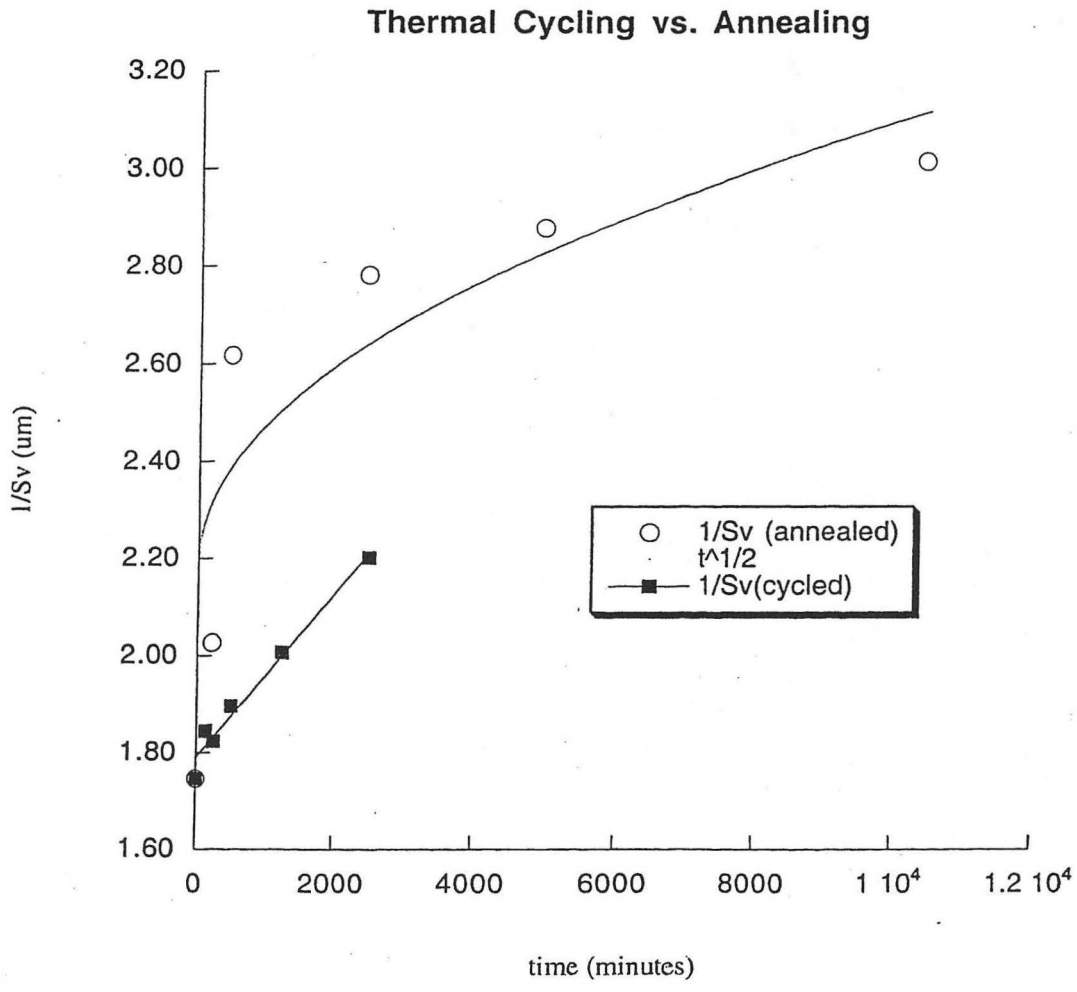

Figure 4.3.4-1a: *Plot of the inverse surface-to-volume ratio verses time for cycled and annealed samples*

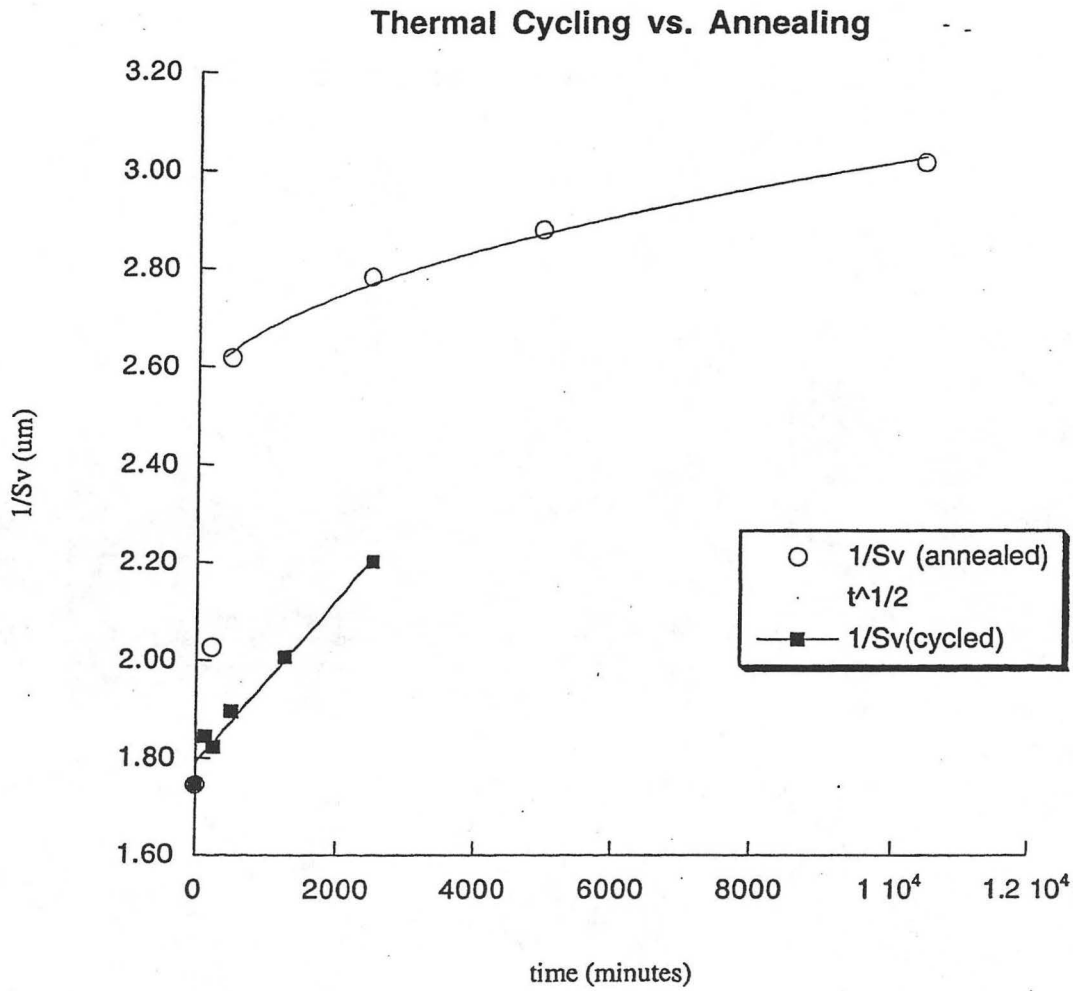

Figure 4.3.4-1b: *Plot of the inverse surface-to-volume ratio verses time for cycled and annealed samples, with modified curve fit (annealed data)*

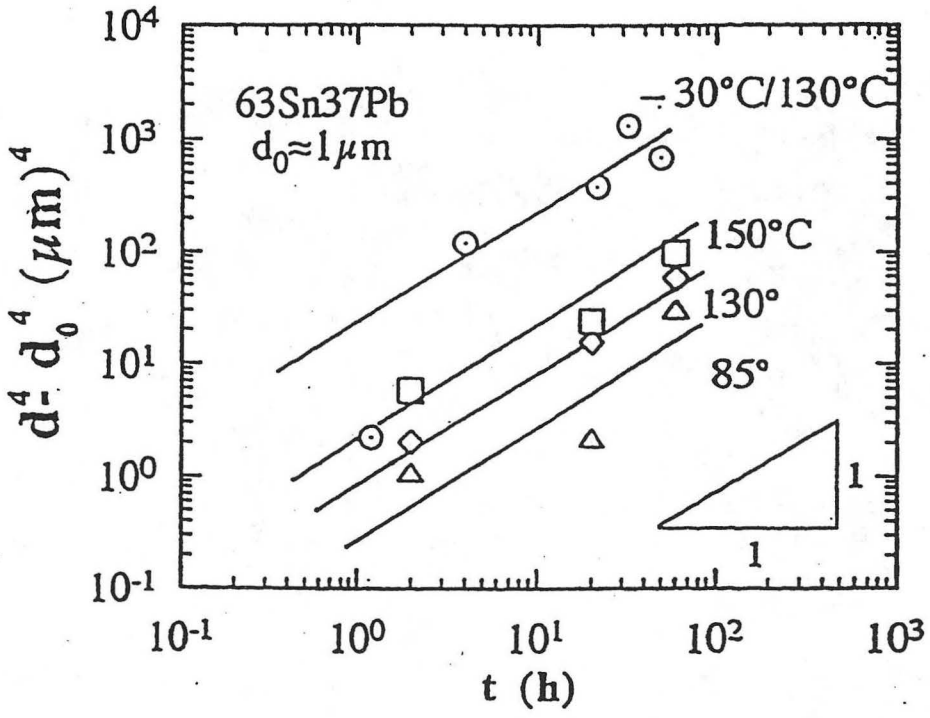

Figure 4.3.4-2: *Plot of thermal cycled and annealed data. Taken from P.L. Hacke, A.F. Sprecher, H. Conrad, "Microstructure Coarsening During Thermo-Mechanical Fatigue of Pb-Sn Solder Joints", Journal of Electronic Materials, Vol. 26, No. 7, 1997*

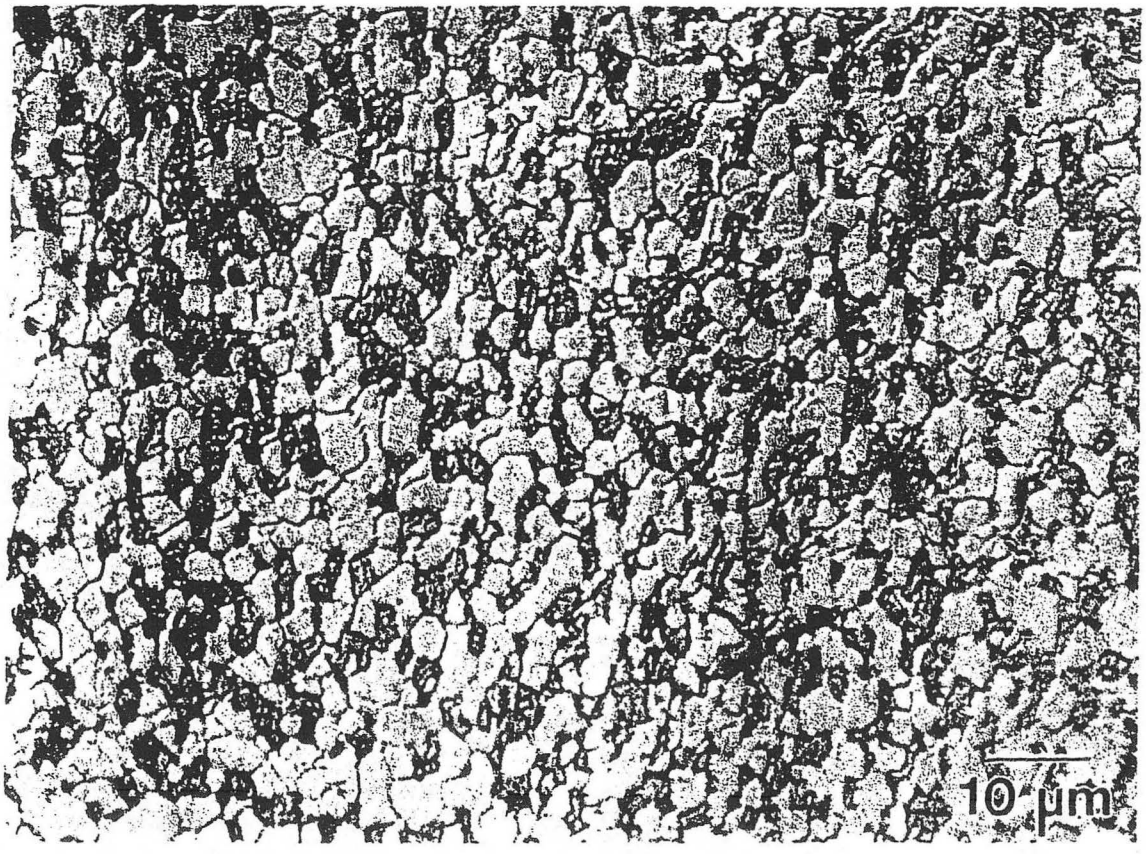

Figure 4.3.4-3: *An example of the equiaxed microstructure of eutectic Sn/Pb. Taken from D. Tribula, "A Microstructural Study of Creep and Thermal Fatigue Deformation of 60Sn-40Pb Solder Joints", Ph.D. Thesis, University of California, Berkeley, 1990*

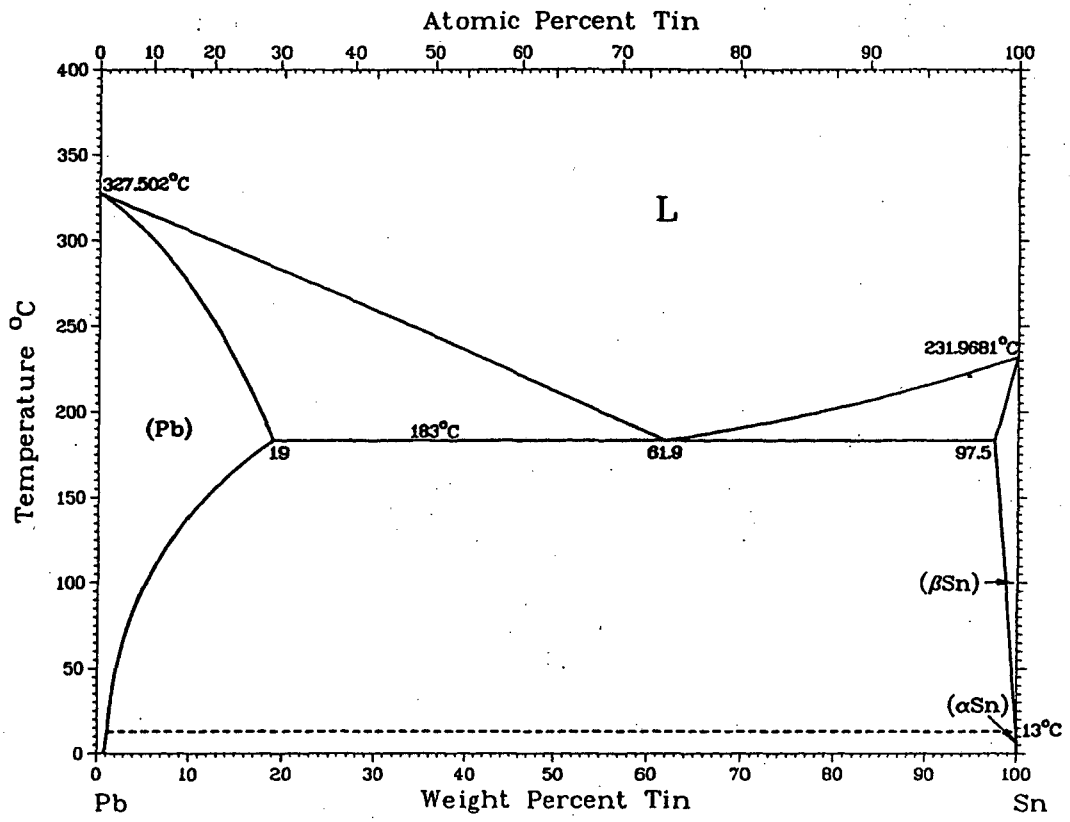

Figure 4.3.4-4: *Phase diagram of the Sn/Pb binary system. Taken from T.B. Massalski, "Binary Alloy Phase Diagrams", Vol. 2, American Society for Metals, 1986*

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