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Study of Bulk Electronic States in Monolayer Tungsten Telluride

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Physics

by

Mina Rashetnia

September 2023

Dissertation Committee:
Dr. Yongtao Cui, Chairperson
Dr. Nathaniel Gabor
Dr. Peng Wei

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The Dissertation of Mina Rashetnia is approved:

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University of California, Riverside

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skills. A bit later, Yadong Xu joined a group, and he became my teacher in learning the fabrication processes. Since then, he and I have grown into fast friends, strengthened through the difficulties of research and the joy of discovery, "old-guard" who were present in my first year. These include Brian Fransisco, Ben Niu, Qiran Wu, Thinh Truong and particularly Xiong Huang, who joined the group in 2018, since then, he and I have grown into fast friends, strengthened through the difficulties of research and the joy of discovery. Thank you all for your support, patience, and hard work. Outside the group, I'm grateful for my friends and colleagues, Jacky, Mark, Haoyu, Jed, Jason, Fatima, Tang, Wei, Jed, Dennis, Max, Trevor, Mashael, Matthew, Mohammed, Ao and Victor without their friendship and support the completion of this work would have been all the more difficult. I'm grateful for everyone that has helped me throughout my journey to this day including lab facilities and other research groups here at UCR. Finally, I would like to thank my family, my Mom, my Dad, and my brothers Reza, and Sina. Above all Abbas, I'm very lucky to have you in my life, and experience the true happiness around you, thank you.

DEDICATION

To my one and only best friend Abbas

I couldn't have done this without your support to my beloved parents

and to my brothers Reza and Sina

ABSTRACT OF THE DISSERTATION

Study of Bulk Electronic States in Monolayer Tungsten Telluride

by

Mina Rashetnia

Doctor of Philosophy, Graduate Program in Physics
University of California, Riverside, September 2023
Dr. Yongtao Cui, Chairperson

The merger of topology and symmetry established a new foundation for understanding the physics of condensed matter, beginning with the notion of topological insulators (TIs) for electronic systems. The "helical" mode at the system boundary, which is the ID edge of a 2D topological insulator or the 2D surface of a 3D topological insulator, is crucial for time- reversal invariant TIs. The complete lifting of spin-degeneracy while maintaining time- reversal symmetry makes these helical modes the ultimate limit of spin-orbit coupling. For proposals to realize unusual excitations like the Majorana bound state, this characteristic is essential.

In this dissertation, I present a series of experiments investigating electronic transport of monolayer WTe2. By bringing monolayer 1T' WTe2, a two-dimensional quantum spin Hall insulator, and few-layer Cr2Ge2Te6, an insulating ferromagnet, into close proximity in an heterostructure, we introduce an interfacial exchange interaction to transform the former into a ferromagnetic quantum spin Hall insulator, manifested by the anomalous Nernst effect, anomalous Hall effect as well as anisotropic magnetoresistance effect.

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Chapter 1: Introduction

1.1 van der Waals Materials

van der Waals (vdW) materials are often first introduced through the common material graphite. Graphite is made up of layers of pure carbon sheets placed one on top of the other. The individual sheets are rather simple to separate from the stack, much like a stack of paper. As seen in Figure 1.1A-C for WTe_2, another vdW material, macroscopic crystals are frequently seen to be peeling apart like book pages, which is part of the reason why they are used as the writing element in pencils.

In the lab, we peel off layers of vdW materials from the parent crystal using various types of sticky tape. The term "van der Waals" refers to the researcher Johannes Diderik van der Waals, who in 1910 was awarded the Nobel Prize in Physics for discovering the weak force that holds the sheets together, first in the context of gases and molecules [1]. Graphene is a sheet of carbon that can be separated from graphite and is just one atom thick. It was first reported in 2005 [2,3] , however measurements of a few-layer thick samples came first [4]. The field of vdW materials was introduced by these discoveries. Since then, insulators, metals, semiconductors, magnets, superconductors, and more have all been isolated as distinct crystalline layers, expanding the library of usable two-dimensional (2D) crystals to comprise a virtual zoo spanning to the full extremes of material properties. Individual sheets can be removed and repositioned on top of one another just as simply. These

atomically thin crystals can be combined in any way, without consideration to changes in crystal structure, according to the van der Waals force's isotropic nature. Van der Waals heterostructures are the name given to these man-made stacks [5]. These atomic sheets are actually more like cellophane wrap than they are like paper in reality; they are sticky, flexible, and prone to wrinkling and clinging back onto themselves. Consequently, it takes a long time and is not perfect to restack the layers onto each other in a controlled way. In the laboratory, we spend a lot of time working to produce cleaner, more uniform heterostructures, this method is used in Chapter 1 Introduction 1.1 van der Waals Materials [6] and explained more in Appendix A.

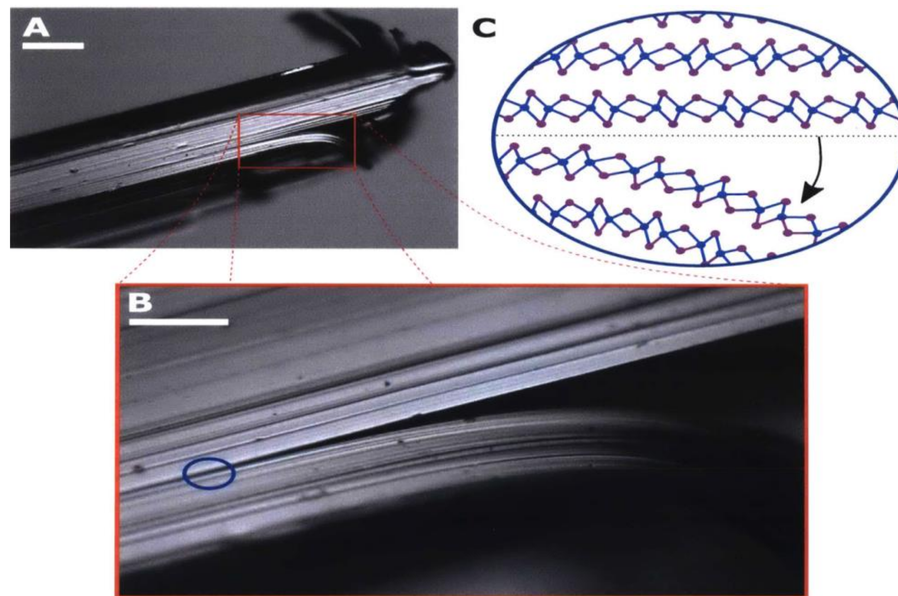

Figure 1.1: (a) a WTe_2 crystal. Scale bar is about 1 mm. (b) Zoom-in to area where the crystal is naturally peeling apart, indicative of the weak interlayer bonding. Scale bar is about 0.2 mm. (c) Schematic cross-section of the WTe_2 crystal structure at the van der Waals cleavage plane, where the region is being split apart. This demonstrates how monolayer and few-layer crystals are isolated by the exfoliation process.

Two broad categories can be used as a simplified foundation for what we intend to accomplish with vdW systems. The initial and (often) easiest phase for a new material is materials discovery, such as the extension of the library of existing 2D materials. This entails separating a single layer (or several layer) sample from its three-dimensional parent compound, identifying it, and measuring its properties. In some cases, the measured qualities have a clear relationship with the parent substance. This is frequently true for materials whose electrons are in the most extreme states that might exist. The materials are less prone to change as a result of the thinning process at these extremes. Examples include the superconductor $NbSe_2$, the magnet CrI_3, the semimetal WTe_2, and the insulator h-BN when thicker than 2 layers. The situation in which the thin crystals exhibit significantly altered or perhaps entirely novel behaviors is more interesting. This class includes graphene, monolayer semiconductors like MoS_2, the density-wave compound 2H-TaS_2, and monolayer WTe_2 are also can be mentioned. As we gain more insight into the behavior of the individual layers, we can start looking at the unique behaviors of layers when they are combined, such as in vdW heterostructures. Sometimes the heterostructures are beneficial for very commonplace purposes, such as using inert materials (like boron nitride and graphite) to sandwich a more sensitive ones such WTe_2 or CrI_3, to prevent the latter from degrading. The materials discovery previously mentioned is frequently made possible by this kind of structure. Combining two vdW materials in such a way that they "talk" to one another and display different phenomena than the individual materials would individually display is a very powerful and fascinating area of research. This type of material is referred to as a hybrid material. Graphene and boron nitride have received

significant attention for electronic transport so far, and science is only beginning to scratch the surface of this topic. As one example, studies shown that special types of graphene-hBN and graphene-graphene vdW heterostructures can transform the [7] normally metallic monolayers into a hybrid system that is an insulator (keep in mind that no chemical reaction has occurred) [8–10]. Incorporation of other vdW materials into such heterostructures promises an exciting future of new and interesting phenomena hybrid materials and devices are not the focus of this thesis but will be touched upon in the final outlook section.

1.2 Topological Insulators

We come into contact with electrical conductors and insulators on a daily basis. The value of conductors in producing and carrying electrical power and communications cannot be overstated in the context of contemporary life. We are shielded from these same electrical networks by insulators. A material will often be categorized as either one or the other. It's crucial to understand that the difference between a conductor and an insulator comes down to how the electrons behave within the material. If the electrons are allowed to move freely, the system is a conductor, and if they are tightly constrained, the system is an insulator. The possibility of spontaneously conducting surfaces in some insulators, as pure silicon [11], was previously recognized. These theoretically conducting surfaces are incredibly delicate, and even minor flaws can prevent them from conducting. These surfaces are consequently typically too challenging to work with for any practical purpose. Some nominal insulators, e.g., bismuth selenide ($Bi_2\,Se_3$), display a naturally conducting border that is

extraordinarily robust and guaranteed to withstand even significant mechanical and chemical degradation. This phenomenon is a relatively new discovery [7,12,13]. By contrast, a metal conducts electricity throughout its interior, while a typical insulator does not conduct electricity at all. This means that a block of this substance would not conduct electricity through its core, but the surface would. These materials' conducting surfaces have a number of peculiar characteristics that could lead to novel applications and intriguing new physics. These new materials were dubbed topological insulator [14].

What does this name mean? We quickly discuss the topology of geometric shapes in order to better understand this and create a comparison. A feature of an object's shape that does not change even after significant deformation is called topology. A typical illustration is the quantity of holes in an object. As shown in Figure 1.2A-C, we can draw relationships between different types of shapes that retain the same number of holes, regardless of how different they may otherwise seem:

1. Sphere: a sphere is the same as a soccer, which is the same as a deflated football.
2. Torus: A donut can be bent into a coffee mug shape. The hole in the center of the donut is preserved as the hole of the handle of the cup.
3. Double-Torus: The double-torus is equivalent to the hybrid donut-mug, which both have two holes. This particular mug has a hole in the handle and a hole in the center of the mug.

Figure 1.2: (a) Genus-0 surfaces: spheres and footballs (both inflated and deflated). (b) Genus-1 surfaces: a torus and a coffee mug. (c) Genus-2 surfaces: the double-torus and the hybrid donut-mug, which has a hole for the handle as well as in the center of the mug.

By using these parallels, we can see that the number of holes, which is defined as a topologically invariant number, can be a defining quantity. It is typically "simple" to add new holes in the actual world (say with a power drill), but mathematically this is seen as a dramatic action that fundamentally alters the item. For electrical insulators, equivalent types of topologically invariant numbers can be described, but more formally. The differences in the fundamental ways that the material's electrons are held in place and kept from conducting electricity are represented by the numbers in this case (see next section for more details). This number is zero for most materials, which represents the standard situation we are familiar with, such as in wood, most plastics and rubbers, typical gemstones, and air. We call these trivial insulators. Some materials have a non-zero number, and we call these materials topological insulators. Crucially, the different ways these materials prevent electrons from conducting electricity are incompatible with each

other. The electrons cannot be maintained in place at the boundary between a trivial and a topological insulator due to this fundamental mismatch.

Since the electrons are free to move, a conducting condition is unavoidably present. The study of two vdW materials which are also topological insulators is the main subject of this thesis. In order to develop a more quantitative understanding of topological insulators, we again take a quick look into the topology of closed orientable 2D manifolds. On such a manifold M, a local Gaussian curvature K_M can be defined. For a perfect sphere of radius r, the curvature is a constant $K_M\ r^{-2}$. For these kinds of manifolds, the Gauss-Bonnet theorem states:

$$\chi_M = {}^{1}\!/_{2}\, \pi \int_M \mathrm{K_M}\, d\mathrm{A} \tag{1.1}$$

that is, the integral of the curvature K over the area of the manifold M provides the Euler characteristic χ_M of the manifold g_M. For the case of the sphere, the integral is easy and gives $\chi_M = 2$. Finally, we can define the genus of the manifold g_M which is straightforwardly related to the Euler characteristic

$$\chi_M = 2 - 2g_M. \tag{1.2}$$

The genus equivalently counts the number of "holes" in the manifold, as discussed in the previous section. One can again clearly see that the sphere has g = 0. How does this relate to electronic systems? For electronic band structures, we can follow a process that is virtually identically analogous to the one described above. We are now concentrating on 2D crystals. Remember that the Brillouin zone, which periodically tiles the plane in

momentum space, is where the electronic spectrum for a crystal is described?

The electronic wave function ψ can be thought of as existing on a closed surface in momentum space due to the periodic boundary conditions of the Brillouin zone. Within the Brillouin zone, we can define a local number for the wave-function and integrate across all momenta. One such quantity is the Berry curvature $\Omega_i = \partial\Psi_i \times \partial\Psi_i$ where Ψ_i is the wavefunction in band i, which when integrated over an entire band result in the Chern number ν_i of that band, an integer.

$$\nu_i = 1/2\Pi \int_{BZ} \Omega_i \, d^2\mathrm{k} \qquad (1.3)$$

Note the similarity with equation (1.1). The additional twist in this situation is that in order to acquire the ultimate, total Chern number of the system, one must perform this integration for all active bands and add all of their respective band Chern numbers. $\sum_i \nu_i = \nu_{tot}$. We can deduce that the Chern number indicates a classical topology of a quantum geometry of the 2D electronic wave-function from the similarity with 2D manifolds [7,13,15]. The Chern number was first discovered for electronic systems in the early 1980s by Thouless and coworkers [16] as a fundamentally significant feature of the freshly found quantum Hall effect [17]. The total Chern number cannot change without closing of the band gap (or shifting the chemical potential out of the gap). Importantly, the Chern number enters into an observable, the integer quantized Hall effect:

$$\sigma_{xy} = (e^2/h)\, \nu_{tot} \qquad (1.4)$$

Fundamentally related to all these deep properties of the 2D bands is the question of what happens at the boundary. A conducting condition must exist at the interface of two

materials with various topological invariants, as previously stated in qualitative terms. One way to picture this is by recalling that the Chern number cannot change without closing the band gap. If the outside region (say vacuum) has a Chern number of v_{out} = 0, and the interior has a Chern number of v_{in} = 1, then one knows that the gap must close at the boundary between the two regions. There have been numerous formulations of the bulk-boundary correspondence, including this one [18–23] which is a generic concept for these types of topological systems. The finite Chern number v_{out} for quantum Hall systems dictates that exactly v_{out} edge modes must exist at the material's border and that these modes must be "chiral," or one-way directional, as shown in Figure 1.3A. It is crucial to understand that if time-reversal symmetry is preserved, the Chern number is zero.

We now reach the important development of the mid-2000s: the ability to establish new topological classes based on an enforced symmetry, producing symmetry-protected topological states. Time-reversal symmetry in two dimensions, which possesses a binary (Z_2) topological invariant n, was the first instance of this type to be found. In this case, the bulk-boundary correspondence dictates that the parity of counterpropagating edge modes is preserved to be odd.

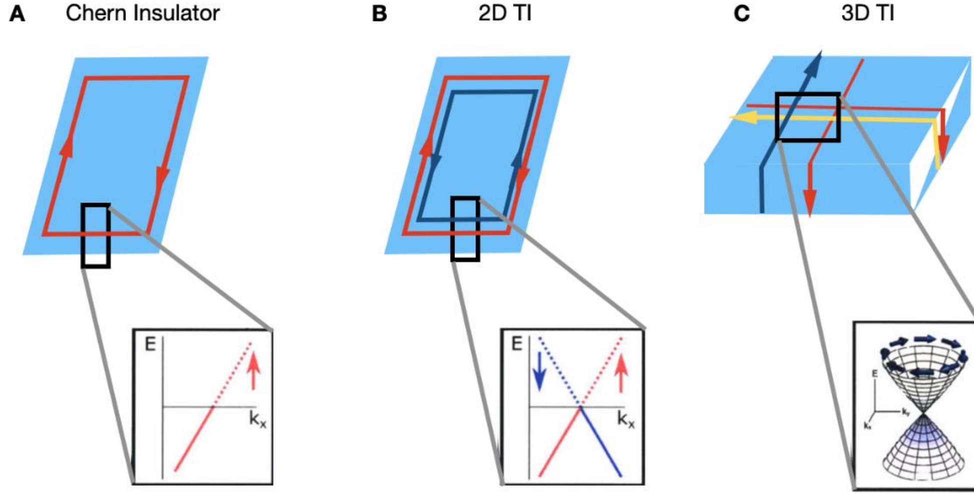

Figure 1.3: (a) Schematic of a quantum Hall state with v_{tot} = 1. Solid and dashed lines indicate occupied and unocupied states, respectively. (b) Schematic of a quantum spin Hall state with $Z_2 =$ 1. (c) Schematic of the 3D time-reversal invariant topological insulator.

In the simplest case, a single pair of counterpropagating boundary modes will exist, as shown in Figure 1.3B. The forward and backward moving carriers also carry opposite spin. Because only a single pair of such modes exists on the boundary, the spin degeneracy has been lifted. These types of modes have been dubbed helical, in contrast to the chiral modes of the quantum Hall systems. In a special case where S_z , (z-component of electronic spin) one can discover that each spin branch has a finite, opposing Chern number if it is kept. for example, for $\nu_{\uparrow} = +1$ and $\nu_{\downarrow} = -1$. The total Chern number is clearly 0 in this case, as required by time-reversal symmetry. The difference defines the topological invariant:

$$n = [\nu_{\uparrow} - \nu_{\downarrow}]/2 \tag{1.5}$$

which is also associated with an observable: a quantized spin Hall conductivity.

A quantized spin Hall conductivity may not be strictly realized in a particular material since

S_z, is not often conserved in a genuine material. Additionally, it is challenging to experimentally quantify the spin Hall conductivity, whereas electronic charge transport tests are much easier to carry out. Fortunately, 2D TIs continue to exhibit distinctive signatures in charge transfer and n maintains its uniqueness as a topological invariant regardless of S_z or conservation. These signatures have been used to identify candidate systems as topologically nontrivial [24]. Soon after the prediction of 2D TIs, its topological state was generalized to 3 dimensions (3DTIs) [25,26]. For this class, a 3D insulator hosts a 2D electron gas (2DEG) with spin momentum locking around its Fermi surface, e.g., a helical 2DEG, as shown schematically in Figure 1.3C. Materials that are 3D TIs are much more prevalent than 2D TIs, and since these materials' boundary modes are located on exposed 2D surfaces, a wider range of experimental approaches can be used to investigate them. As a result, 3D TIs were the subject of a sizable percentage of early topological insulator research. Soon again after that, symmetry protected topological electronic phases were expanded to all dimensions and 10 generic symmetry classes, forming a so-called periodic table of topological insulators and superconductors [27].

At their limits, topological superconductors include Majorana fermions, an exotic quasiparticle. These quasiparticles, which are Majorana zero modes or Majorana bound states (MBSs) when constrained to zero dimensions, are not fermions but instead exhibit non-abelian statistics [28–32]. MBSs come as correlated pairs that can be well separated, allowing for non-local storage of quantum information. This has been one of the driving motivations for continued work on topological insulator systems.

1.2.1 2D topological insulator

In 2005, Kane and Mele discussed strategies to open a gap or, equivalently, give a mass to the Dirac fermions in the graphene band spectrum to explain the idea of topological insulators [12,33]. There are two common approaches: 1. the first involves adding a standard mass that is identical at both Dirac points. The second way involves adding a Haldane mass, which has different signs at the two Dirac locations. It results from the sublattice potential difference, which breaks parity or inversion symmetry but preserves time-reversal symmetry. It can be produced by having hypothetical next-nearest-neighbor hopping matrix elements that preserve inversion symmetry but violate time-reversal symmetry. A Hamiltonian with four components that is similar to Dirac can condense them.

$$H = \nu F(\tau z \sigma x p x \ + \ \sigma y p y) + \ m R \sigma z \ + \ m H \tau z \sigma z$$

where the σ and τ Pauli matrices act on the sublattice and valley (or K and K') spaces respectively.

The A and B sublattices, as well as the K and K′ points, are reversed under inversion (also known as parity transformation, P), resulting in $\sigma_z \rightarrow -\sigma_z$ and $\tau_z \rightarrow -\tau_z$. We reverse the K and K′ points under time-reversal transformation (Θ), but the A and B sublattices stay the same, resulting in $\sigma_z \rightarrow -\sigma_z$ and $\tau_z \rightarrow -\tau_z$. It follows that the Haldane mass term (mH) is odd under but even under $\mathcal{P}$, whereas the regular mass term (mR) is even under but odd under $\mathcal{P}$. Therefore, it is only natural to inquire whether it is possible to have a mass term

that respects both $\mathcal{P}$ and Θ. If spin-orbit coupling is used, Kane and Mele pointed out that the answer is indeed affirmative. The simplest possibility would be a term of the form $m_{km}\tau_z\sigma_z S_z$, where S_z is the $\hat{z}$ component of the electron spin operator $\vec{S}$. Since $\vec{S}$ is even under $\mathcal{P}$ but odd under Θ, it is easy to see that this mass term is even under both $\mathcal{P}$ and Θ. Simply having two copies of the Haldane model, one for spin-up electrons and the other for spin-down electrons, with opposing next-nearest-neighbor hoppings, allows for the generation of this Kane Mele mass term. Due to cancellation between the up- and down-spin electrons, which is made possible by time-reversal symmetry, the charge Hall conductance is zero. When the chemical potential is in the band gap, there is quantized spin Hall conductance, though. The spin Hall conductance, which corresponds to the spin current response to a potential gradient, is the difference between the Hall conductance of up- and down-spin electrons. Hence, this state was initially dubbed a "quantum spin Hall state", which is topologically non-trivial. Two-dimensional topological insulator is another name for the two-dimensional quantum spin Hall insulator (2D QSHI) state (2D TI). For every edge, it has two edge mode branches that propagate in the opposite directions: one for spin-up and one for spin-down. They are thus

consistent with time-reversal symmetry and the overall system is achiral since Θ flips both the orbital motion and the spin direction. Helicoidal modes are those in which the spin and velocity directions of the modes are connected. It was discovered that topologically challenging bands with gapless helical edge modes can exist in the presence of time-reversal symmetry.

1.2.2 excitonic insulators

The usual semi metallic state can become unstable in the presence of Coulomb interactions in a system with electron-hole coexistence, or when bound e-h pairs spontaneously arise, as was predicted several decades ago [34]. This may cause a phase transition into the excitonic insulator (EI) or Bardeen-Cooper-Schrieffer (BCS)-like excitonic condensation, an insulating phase. Similar to the BCS gap in a superconductor, the excitonic insulator phase emerges with a gap opening at the semimetal's Fermi surface.

Low carrier densities and reduced dimensionality in a monolayer semimetal create the ideal environment for significant correlation effects. The pairing of electrons and holes to create excitons in the equilibrium state is one potential manifestation of such correlations. Such excitons might condense to create an exciton insulator at low temperatures [34–36]. Exciton production is predicted to take place only at low temperatures and close to charge neutrality because free carriers that screen the binding contact should be able to readily interrupt it. Numerous substances have been suggested as potential excitonic insulator materials ($TiSe_2$ [37], Ta_2NiSe_5 [38,39], Carbon nanotube[40], MoS_2 [41]).

1.3 Introduction to WTe2

Three-dimensional WTe_2 is a bulk crystal (see Figure 1.1) in an orthorhombic structural phase ("Td" structure) [42–44] The flux approach [45] is utilized to grow the samples that we used in our research. Not only is it a layered vdW material, but also within each layer the

tungsten atoms dimerize into chains layer by layer. The conclusion is that the substance is entirely anisotropic (all it is one of the earliest measured monolayers (three cardinal directions are not comparable). crystals with a lattice that is not triangular.

The crystal structure of T_d-WTe_2 is shown in Figure 1.4, alongside the case for 1T'-$MoTe_2$ for comparison. There are two qualitative differences in the atomic coordinates:

1. Within each plane, the metal-tellurium rhombus is distorted in the T_d structure but inversion symmetric in the T' structure.

2. The stacking of the layers is different, resulting in a tilted unit cell in the IT' structure and an untitled unit cell in the T_d structure.

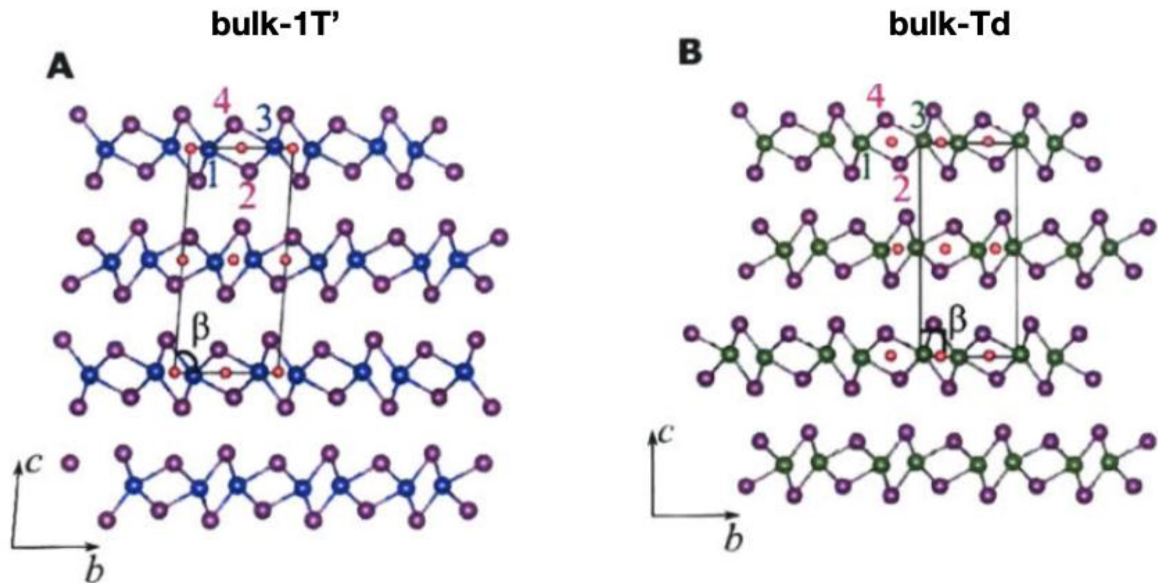

Figure 1.4: (a) Bulk atomic positions for the A, IT' and (b) T_d structures. Orange dots represent centers of the M-Te rhombi, which represent true inversion centers for the IT' case (picture take from reference 42).

The two crystal structures differ in the set of symmetries they respect the IT' structure preserves an in-plane two-fold rotating axis, a mirror symmetry, and inversion symmetry. The T_d structure has an out-of-plane two-fold screw axis and two mirror planes, one of which is not symmorphic, despite breaking inversion symmetry. Table 1.1 displays a comparison of crystal symmetries.

A schematic band structure of 3D WTe_2 is shown in Figure 1.4 for K_z =0. Valleys for electrons and holes are found in the $\Gamma - X$ direction. Due to a spin-orbit splitting brought on by broken inversion symmetry, each valley includes a nested pair of pockets with significant spin texture [46]. The occupation of these pockets is virtually compensated, with equal amounts of electrons and holes, according to magnetoresistance tests, quantum oscillations, and spectroscopy studies [45,47–52]. At strong magnetic fields, it has been discovered that WTe_2's magnetoresistance ratio exceeds 10^5 at large magnetic fields, indicating good crystalline quality and significant mobilities [45] Since the initial discovery of the extreme magnetoresistance [47], numerous more semimetallic systems with comparably strong magnetoresistance effects have been found [53–61]. Along with the aforementioned, WTe_2 has also generated a lot of discussion regarding potential topological facets of the electronic structure. For the 3D crystal and the 2D crystal, there are two separate cases. Weyl semimetals with Type-II Weyl nodes have been anticipated to make up the 3D complex [62]. Because inversion symmetry is only weakly broken, the Weyl nodes are close to each other in momentum space. As a result, there has been some

evidence for this topological phase, but not yet a smoking-gun proof [46,63–66]. The 2D topological phase will be discussed in the next section.

Table 1.1: Properties of the 3D versions of the distorted 1T structure, known as 1T'and T_d. I is inversion symmetry, C_{2x} is a two-fold rotation about the X axis, and M_x is a mirror plane normal to the X axis. In the T_d structure M_b is actually a glide plane and C_{2c} is actually a screw rotation.

	bulk-1T'	bulk-T_d
Structural Phase	primitive monoclinic	primitive orthorhombic
Lattice Constants	a ≠ b ≠c	a ≠ b ≠c
Unit Cell Angles	$\alpha = \gamma = 90°, \beta \neq 90°$	$\alpha = \beta = \gamma = 90°$
Space Group	P2/m (#11)	Pmn2_1 (#31)
Point Group	C_{2h}	C_{2v}
Symmetry Operations	I, C_{2a}, M_a	M_a, M_b, C_{2b}

1.3.1 Two Dimensions- Crystal Structure of WTe2

The 3D crystal structure of the parent crystal is typically well-known, thus the simplest assumption for the crystal structure of an exfoliated monolayer is that it is the same as if one were to extract a single layer from it. In the case of monolayer WTe_2, this refers to the T_d structure. The literature does not always make a distinction between IT' and T_d, though.

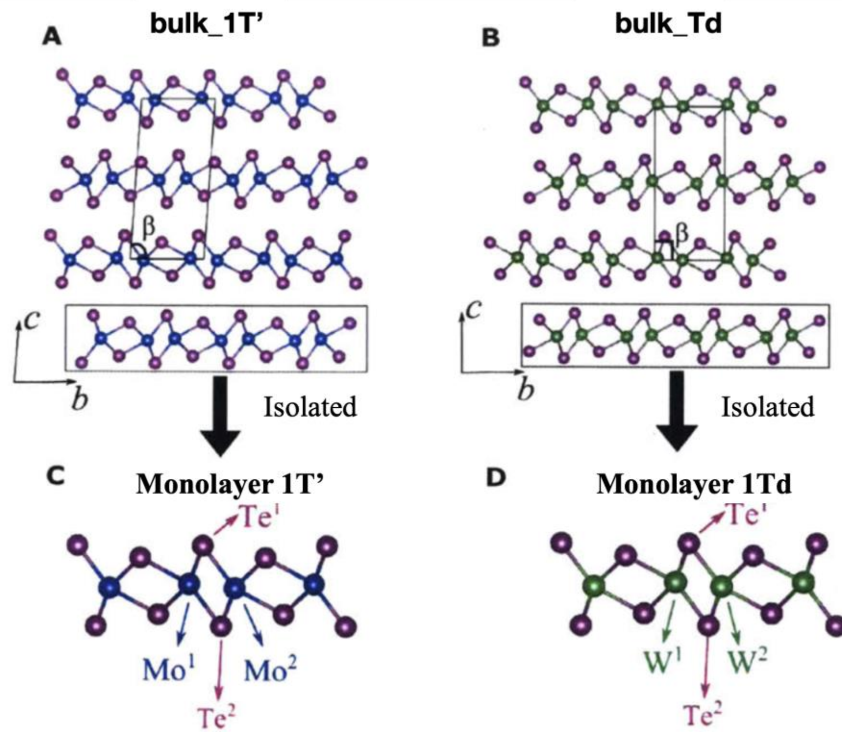

Figure 1.5: Monolayer atomic positions, as (a, c) 1T' and (b, d) Td structures (picture take from reference 42).

In the T_d scenario, the difference between the two structures amounts to a minor distortion of the W-Te rhombus, leading to weakly broken inversion symmetry, as was previously mentioned. In contrast to the inversion symmetric 1T' phase, the T_d monolayer (and in fact

all feasible layer numbers) would be predicted to have an intrinsic spin-orbit splitting. This spin-orbit splitting is documented in 3D bulk crystals from quantum oscillation data [67,68] as well as ARPES spectra [46,48] interpreted alongside band structure calculations. Raman spectra taken on ultra-thin samples has been found to be consistent with theoretical calculations of the vibrational modes of Td-WTe2 [69,70]. STM studies on MBE-grown films has found a structure consistent with the 1T' phase [71,72] but did not specify or were unable to make the distinction between the 1T' and T_d structures.

Table 1.2: Properties of the 3D versions of the distorted is inversion symmetry, C_{2x} is a two-fold rotation about normal to the X axis.

	monolayer-1T’	monolayer-T_d
Structural Phase	primitive monoclinic	primitive monoclinic
Lattice Constants	a ≠ b	a ≠ b
Unit Cell Angles	$\alpha = 90^{\circ}$	$\alpha = 90^{\circ}$
Space Group	P2/m (#11)	P1m1(#6)
Point Group	C_{2h}	C_{1s}
Symmetry Operations	I, C_{2a}, M_a	M_a

1.3.2 Band Structure and Topology

The 2D topological insulator state in the monolayer exists independently of the hypothesized topological semimetal phase in 3D. This was first conceived by Qian, et al,

who proposed that monolayer transition metal dichalcogenides in the IT' structure are 2D time-reversal invariant topological insulators [73]. The reasoning goes as follows:

1. We start with the 1T structure that is undistorted. This phase is structurally unstable, but it has been calculated to be metallic [74], with the largest fermi surface near the K points.

2. The Brillouin zone shifts from hexagonal to rectangular with distortion to the 1T' structure, but the bands close to the chemical potential still come from the same orbitals. The band inversion caused by the Te p-orbitals' higher hopping strength between W atoms decreases the total band energy at Γ. The topologically non-trivial nature emerges from these orbitals with different parities in the band inversion at Γ [27,75]. This energy scale is quite powerful, of the order of 0.5eV, as a result of the band inversion being produced by crystal fields. More information about this intuition is provided by Qian, et al [73].

3. The band gaps in the $\Gamma - X$ direction is then produced at limited momenta by spin-orbit coupling. This spin-orbit driven hybridization gap is projected to have a narrower energy scale, with values between 10 and 150 meV [73] Nevertheless, depending on the computation, the transport gap could be smaller or even negative (for example, a semi metallic state).

4. Finally, the actual crystal structure might not be 1T' but rather T_d. Small spin-orbit splitting (of order 5 meV) occurs as a result of this inversionbreaking distortion in the conduction and valence bands, but the band gap is not closed. As a result, although not

precisely belonging to the 1T' structure, we know that the T_d monolayers maintain a non-trivial topological invariant.

Only WTe_2 and $MoTe_2$ were known to exhibit a 1T' phase among the normal transition metal dichalcogenides. Depending on the growth circumstances, $MoTe_2$ can be produced in the 1T', T_d , and 2H forms. [76–83] while WTe_2 is almost universally stable in the T_d structure [42–44,47], Fortunately, the 1T' and T_d structures are quite near to one another according to the reasoning above, and we know that both should be topologically non-trivial. We conclude that WTe_2 is an excellent candidate material to search for a 2D topological insulator phase in a vdW material because of its structural stability and high crystalline quality.

Figure 1.6. illustrates the results of a tight-binding model calculation of the monolayer WTe_2 band structure.

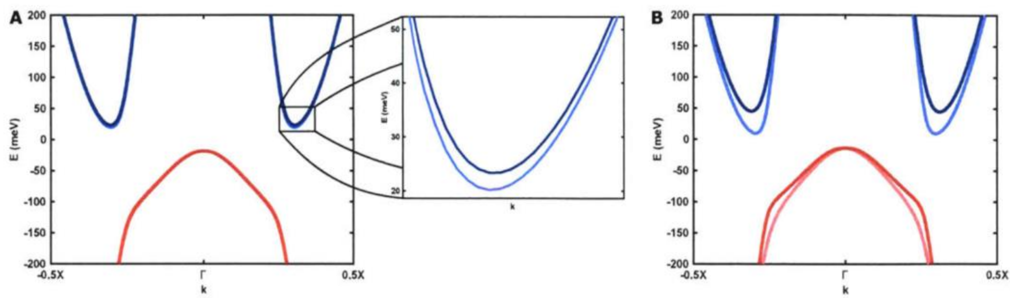

Figure 1.6: (a) Band structure of monolayer WTe_2 from a DFT-derived tight-binding model. (b) The conduction and valence bands were shifted have roughly the band gap seen in spectroscopy measurements [84]. Center: zoom-in to the bottom of one of the conduction band valleys to show.

the intrinsic spin-orbit splitting. B, Same calculation with a large displacement field added, showing that the spin-orbit splitting can be enhanced.

1.4 Getting Things Ready

Experimental evidence already existed that ultra-thin WTe_2 deteriorates when exposed to air, most likely as a result of oxidation [85–87]. Our internal studies, which are not shown here, demonstrated that tiny samples (single-digit layers thick) would exhibit insulating-like behavior whereas thicker samples would have high mobility semimetal behavior as one would anticipate for 3D samples. As a result, the challenge was to develop techniques that would enable the fabrication of transport devices in which thin WTe_2 flakes would survive without oxidation or other chemical degradation. With similar objectives in mind for a wide variety of air-sensitive vdW materials, we embarked upon the creation of a glove box with equipment specialized for exfoliation and inspection of these vdW materials as well as the creation of novel vdW heterostructures.

The glove box itself was purchased from vacuum technology, Inc, and is filled with a slight over-pressure of pure argon gas supplied from pressurized Dewars of liquid argon. The internal oxygen and water levels are continuously monitored and remain below 0.1 parts-per-million under normal use. Jacky, Jeremiah, and I were working together to designed and constructed a custom mechanical transfer setup for creating vdW heterostructures, similar to those described elsewhere [6], but with the added functionality of remote operation for the x-y-z motion of the sample stage and transfer arm as well as the focus knob. For details regarding this setup, please contact me.

Scientifically, we began with monolayer samples as our "canary in the coal mine" to test that our new fabrication schemes are indeed working. By using the MIM technique at low temperature and seeing the edge mode we could test our monolayer sample quality [88]. Following this, we pursued the monolayer samples. By this time, several groups had determined that monolayer WTe_2 does indeed have a full band gap [84,89,90] and one group explicitly showed edge conduction in transport devices [89]. However, the nature of this bulk gap is unclear. Recently, there are new studies which they are talking about the Evidence for equilibrium excitons and exciton condensation in monolayer WTe_2 [91,92]. These exciting results motivated more careful studies of this band gap. To investigate and study of this band gape, we combine Scanning, Microwave impedance microscopy (MIM), Kelvin probe force microscopy (KPFM), and capacitance measurements on monolayer WTe_2 devices. By correlating these measurements, we will discuss their implications on the bulk electronic structure in monolayer WTe_2 in this thesis, chapter 2 and chapter 3.

Finally, during our investigation of the bulk gap, we happened upon a surprising discovery: we systematically investigate the Anomalous Nernst effect and Anisotropic magnetoresistance in monolayer WTe_2 /$Cr_2Ge_2Te_6$ heterostructure due to MPE. Our experimental results clearly show that the monolayer 1T' WTe_2 is magnetized, and the induced magnetism become absent above the Curie temperature of $Cr_2Ge_2Te_6$. The Anomalous Nernst effect and Anisotropic magnetoresistance can be tuned by gate-voltage, provide an effective way to manipulate and probe the Berry curvature near E_F and topological nature of the material. The results on this state are presented in Chapter 4.

Chapter 2: Device Fabrication

As an experimentalist, I always strive to fabricate high quality devices. Fabrication of devices is a vital component in experimental research, because the intrinsic physics can only be revealed in devices with low impurities and disorders.

In this chapter, we describe in detail the procedures used to fabricate such devices. First, we explain the methods used to prepare Si chips for the fabrication process. Next, mechanical exfoliation of bulk material is performed to generate each ultrathin layer of the heterostructure. We investigate a variety of exfoliation methods and evaluate their efficacy. After getting each layer, we stack these layers into a finished heterostructure using a modified dry transfer technique. We also provide a few methods for streamlining the assembly procedure. We next go into detail about how to create devices using cleanroom fabrication techniques employing these heterostructures. We outline the precise processes that were employed in the fabrication process as well as alternate methods for improving device performance.

2.1 Wafer Preparation

WTe2 heterostructures are fabricated on standard Si substrates. We utilize Si/SiO2 wafers with a 280 nm oxide layer which we got them from University, Inc. Since commercial Si wafers exhibit a variety of surface defects and contaminants, cleaning procedures must also

be performed in order to prepare them for device fabrication. To clean the substrate, Diced chips (they are cut into square chips about half a centimeter on a side using a diamond scribe) were sonicated in acetone, isopropanol, and finally blow-drying with dry nitrogen gas. Because contamination may occur at a micro- or nanoscale, more sophisticated cleaning requirements are also performed. We utilize the RIE (Or ICP) station to perform O2 plasma on Si chips for 30 s (you can see more ICP details in table 1. A for a cleaning SiO2 recipe) in order to ensure atomic-scale cleanliness of the chips. Usually, both the sonication and O2 plasma steps are performed in conjunction to get the good size monolayer. However, through O2 plasma generates cleaner Si chips, this method also makes it harder to transfer atomic layer flakes from one Si substrate to another. Because of this, there is a balance and trade-off in using these two cleaning procedures. Sonication leads to dirtier substrates yet allows for easier transfer. O2 plasma, on the other hand, creates cleaner substrates but makes transfer more difficult. The choice of which procedure to use, one procedure or both, depends on the specific needs of the device to be made [93–95].

2.2 Exfoliation of Atomic Layer Materials and Optical Identification

The van der Waals materials used in this work were isolated by manually exfoliating from parent crystals with scotch tape. In some cases, for finding the thinner of materials can be good to use blue semiconductor dicing tape which has less residue than scotch tape while it's harder to get monolayer. We use a wide range of equipment, shown in Figure 2.1, to

carry out the exfoliation process. We get bulk Kish graphite from Covalent Materials, hBN from National Institute for Materials Science, Namiki, Japan, bulk WTe2 flakes from Jiun-Haw Chu from University of Washington, also 2D Semiconductor company and CGT crystal from Fokwa research group at UCR. Throughout the exfoliating procedure, gloves are worn to avoid contamination from hand oils and other impurities. A normal glass slide is taped to the lab bench to create an exfoliation station that may be used for all exfoliation techniques. During the exfoliation procedure, Si chip can attach to a small piece of carbon tape that has been placed in the center of the glass slide. By using these materials and equipment, ultrathin layers of these materials can be produced, as shown in Figure 2.2. The many exfoliation techniques used to create these flakes are discussed in this section, along with the benefits of each approach for exfoliating particular materials. In Section 2.2.1, we present a standard exfoliation procedure adapted from techniques in the literature. Section 2.2.2 describes a razor blade exfoliation method that improves upon the standard method for exfoliating TMDs. In Section 2.2.3, we explain a third technique as the gold exfoliation method, which can substantially improve FeGtTe and CrGeTe exfoliation. Finally, Section 2.2.4 describes a novel exfoliation Technique which is using PDMS for exfoliation. For air sensitive materials we are using one of these techniques but instead of doing it at air, we are using the glove box facilitating the creation of CGT and WTe2 heterostructures.

2.2.1 Exfoliation: Standard Method

Our standard method of exfoliating 2D materials involves repeated peeling of bulk flakes with Scotch tape, similar to previous reports in literature [96]. The materials and equipment

used in this method are shown in Figure 2.3. The bulk material is placed in the center of a large piece of tape, either Magic brand tape or scotch clear tape. We peel off layers of the bulk flakes and spread them across the surface of the tape by continuously attaching and unsticking it to itself, ideally creating a uniformly thin layer of either graphene or WTe2. Here, you must take care to avoid damaging the parent crystal by exfoliating, which means avoiding repeatedly putting the crystals on top of each other to attach and peel off. Examples of this are labelled "Graphene on tape" and "WTe2 on tape" in Figure 2.3. As seen in these figures, WTe2 on tape is distinguished by sharper flakes compared to graphene which looks more like powder. After that, we stick a Si chip to an exfoliation tape and place the chips on the prepared tape, sticky side up. The tape is then improved contact with the substrate by being pressed into the Si using a cotton swab, as shown in Figures 2.3. We believe that utilizing a cotton swab rather than just using finger strength during this procedure preserves the integrity of the flakes and produces larger, thinner flakes for heterostructure creation. Following the exfoliation method, we annealed the substrates together with graphite/tape on a hot plate at 100 C for 2 min. After the sample was gently pressed and cooled to room temperature, the tape was likewise peeled off. After exfoliation, suitable flakes for a heterostructure are found by searching the Si chip using an inspection microscope.

For the samples prepared by the modified exfoliation method with annealing prior to tape separation, the total graphene areas for all samples are larger than exfoliation without annealing the tape. We performed additional experiments aimed at identifying the role of time and temperature of the annealing step introduced here for different 2D materials, the

results of these experiments are summarized in the table 2.1. In fact, even though we varied the annealing time and temperature from 2 to 30 min and 80 to 140 C, the total graphene area did not significantly depend on either. All samples produced significantly more exfoliated thin layer than the usual approach, with the maximum yield (obtained for annealing at 100 C for 2 min) being about 60% greater than the lowest yield (seen at 140 C, 2 min). Practically speaking, increasing the annealing time and temperature has another negative effect, which is a significantly greater distribution of adhesive residue. from the substrate surface to the adhesive tape. Hence, we find that annealing at 100 C for 2 min represents a good overall compromise of large 2D flakes, high exfoliation yield, and minimal amounts of residual glue. This step promotes the evacuation of gas molecules from the interface of flakes and SiO2 via the edge, caused by an increase in pressure there. Our understanding implies that the flake edges effectively serve as a one-way valve in this process, allowing pressure to build up. To be released by the passage of gas away from the interface during annealing; but, as soon as a tighter, more uniform contact is made between the support and the outermost flake layer, the enhanced van der Waals force prevents gas from entering again throughout cooling The consequence is the elimination of trapped species from the contact and the formation of a tighter, more uniform contact, Ultimately, the additional annealing step acts in three ways to increase the force between 2D materials and SiO2 surface: via the established pressure difference, increased contact area, and decreased overall contact distance. This combination of factors should facilitate the transfer of large area 2D flakes from bulk material. Also, Raman spectroscopy has proven to be a versatile tool for studying 2D materials, and especially in detecting defects and identifying

the number of layers. We used Raman spectroscopy to assess if the additional annealing step to 100 C in air causes any defects in the graphene or other 2D materials, exfoliated by the modified method, e.g., by chemical reactions with H2O, O2, etc.

Our Raman results are consistent with other reports on graphene and WTe2 flakes with different number of layers. From the fact that the spectra of graphene exfoliated by the two methods are indistinguishable, we conclude that the additional annealing step in the modified method does not cause any detectable increase in defect density as shown in Figures 2.4.

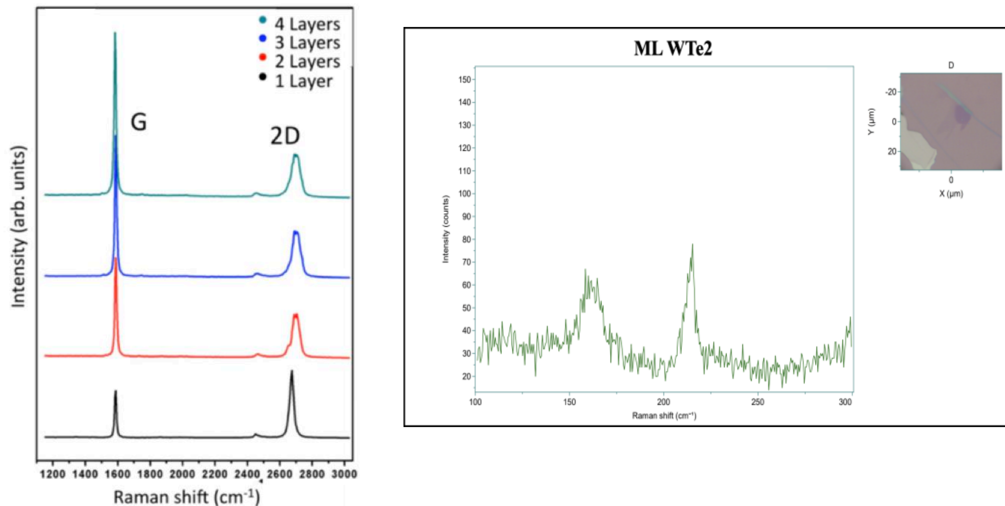

Figure 2.1: Characterization of graphene and WTe2 flakes**.** (a) Raman spectroscopy of graphene flakes with thickness between 1 to 4 layers. The G peak is at 1587 $(cm)^{-1}$ for all the flakes. The 2D peak is at 2675 $(cm)^{-1}$ for monolayer graphene, and at 2690 $(cm)^{-1}$ for 2-to-4-layer graphene. (b) Raman spectroscopy of monolayer WTe2 flakes with Optical image of a ML WTe2 flake prepared on 100 nm SiO2/Si substrate.

This technique works quite well for producing different thicknesses of graphene flakes and WTe2 even in monolayer limit, enabling us to create the top and bottom layers of the heterostructure that we want. Additionally, we discovered that this technique is effective for producing thin flakes for magnet TIs, ferromagnetic and antiferromagnetic. However, the standard method is generally not effective for producing monolayer of CGT, FGT or MBT as the bulk material tends to break apart in to small, unusable chunks rather than separate along the van der Waals bonds into thin sheets. Because of this, alternative methods of exfoliation that specifically improve the results for ML of these materials are necessary.

In addition, for creating ultrathin flakes of hBN, another 2D material, which is the protection layers of our desired heterostructure this exfoliation method without heating the tape also works well.

Table 2.1: SiO2 surface oxidation recipe for different materials

	ICP recipe for cleaning SiO2	**Heating the tape**	**Tape**
Gr	O_2 20mTorr RF 50W ICP 0W O2 flow 50sccm 15s	2 min 100 ∘C	scotch
hBN	No need	No need	scotch
WTe2	O_2 20mTorr RF 50W ICP 0W O2 flow 50sccm 20s	2 min 100 ∘C	scotch
TaIrTe4 NbIrTe4	O_2 20mTorr RF 50W ICP 0W O2 flow 50sccm 30s	2 min 100 ∘C	scotch
CGT	O_2 20mTorr RF 50W ICP 0W O2 flow 80sccm 20s	2 min 90 ∘C	blue
FGT	O_2 20mTorr RF 50W ICP 0W O2 flow 50sccm 80s	2 min 90 ∘C	blue
MBT	O_2 20mTorr RF 50W ICP 0W O2 flow 80sccm 30s	3 min 100 ∘C	scotch
ZrTe5	O_2 20mTorr RF 70W ICP 0W O2 flow 80sccm 20s	2 min 100 ∘C	blue
BSCCO	No need	2 min 100 ∘C	PDMS exfoliation

2.2.2 Exfoliation: Razor Method

The razor procedure is a further exfoliation technique that enhances the conventional approach to exfoliating TMDs. We again build an exfoliation station in this technique, and we affix a Si chip on top of the carbon tape. On the other hand, this method does not use Scotch tape. Rather, a large flake of the substance is applied directly to the Si substrate. The carbon tape on the tweezers is then covered with a second, sizable flake of the same substance as the flake placed on the substrate, ensuring that no tape is visible. Then, to ensure good contact between the two, the coated tweezers are used to press the into the flake on the substrate. After being somewhat anchored to the substrate so that it won't move around easily, the bulk flake is painstakingly separated into layers using a razor blade. Pieces of ultrathin material may start to develop at the borders of the bulk flake or separately on another area of the Si chip after several repetitions of cleaving. This technique improves on the exfoliation of TMDs, and works particularly well for MoS2, MoSe2, WS2, and WSe2. However, this method only moderately improves the effectiveness of generating ultrathin flakes of MoTe2. This may be due to the large lattice mismatch between Mo and Te, which makes the material less physically stable and harder to exfoliate.

2.2.3 Exfoliation: Gold Assisted Method

Another reliable method of creating 2D flakes of MBT, CGT, FGT, and MoTe2 is known as the gold assisted technique, which has been adapted from a procedure developed by

Desai et al [97–99]. Since the connections between individual layers of a TMD are weaker than those between van der Waals interactions between Au and TMDs, covering bulk TMDs with gold makes it possible to peel off the gold layer and take an ultrathin flake of TMD material with it. The atomically thin TMD can be seen by etching away this gold layer. First, a piece of transparent Scotch tape is obtained, and the sticky side of the tape is covered with a number of bulk flakes of material. The sticky side of the tape is then coated with a tiny coating of gold (between 1-2 nm thick) using an electron beam evaporator. At this point, a piece of thermal tape is attached to the Scotch tape, and the two are quickly peeled apart, leaving gold residue and thin flakes of material on the thermal tape. The polished side down of the Si chips are then adhered to the thermal tape. After that, the tape with the Si substrates attached is placed on a hotplate and heated to 100°C, melting the tape's adhesive and releasing the Si chips. The Si substrates, which now contain ultrathin flakes of material coated with gold on their surfaces, are etched in a commercial gold etchant solution for 30 s to remove to gold layer, leaving behind atomically thin material. Since CGT or FGT are air sensitive materials then after getting monolayer of them, if we put the flake in gold etchant solution can oxidied the flake. For this reason, this method is generally preferred for creating extremely thin layer, yet the gold assisted procedure is still useful when large-area, thin flakes of CGT or FGT are absolutely necessary. In short, the standard exfoliation method proves effective in generating ultrathin graphene, TMDs, TIs, FM, and AFM materials.

Van der Waals flakes' color contrast with the silicon oxide backdrop allowed optical microscopists to manually identify the candidate flakes (see Figure 2.5). Here, in figure 2.5

attached monolayer of several materials that we could get with different exfoliation techniques as I explained here. we also did an atomic force microscopy to confirm the thickness of the different flakes.

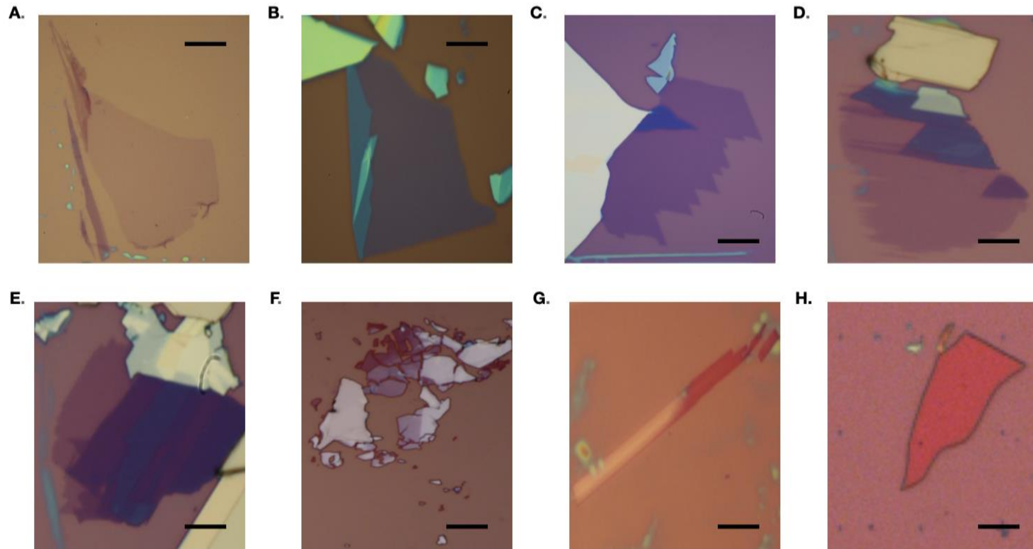

Figure 2.2: Examples of exfoliated van der Waals Materials. (a) Exfoliated graphite. The region with the weakest color contrast is monolayer graphene. (b) Exfoliated hexagonal boron nitride shows a terraced structure. The dark blue region is the monolayer. (c) Exfoliated WTe2 also shows the terraced structure, which mostly connected to the yellow bulk WTe2. (d) TaIrTe4, E. Cr2Ge2Te6, F. Fe3GrTe2, G. ZrTe5, H. Bismuth strontium calcium copper oxide. The black scale bar in images is 20 µm.

2.3 Building a Heterostructure: Dry Transfer Technique

Once ultrathin samples of Graphite and ML of WTe2 have been isolated, we assemble them into a heterostructure [100–102]. The heterostructure devices are assembled using a highly customized, temperature-controlled transfer microscope that ensures that the interface between the two layers has no intentional contact to polymer films. The dry pick-up transfer

process, described below, results in heterostructures with minimal interfacial contamination, and is followed by two cleaning and annealing processes.

The microscope shown in figure 2.6a consists of a sample stage where the target layer will be placed which can move both in x-y plane and Z direction, objectives with different magnifications to monitor the process, and stamping stage that holds the glass slide with an attached viscoelastic stamp. Figure 2.5b shows a schematic of a stacked multi-layer of CGT on a monolayer of WTe2.

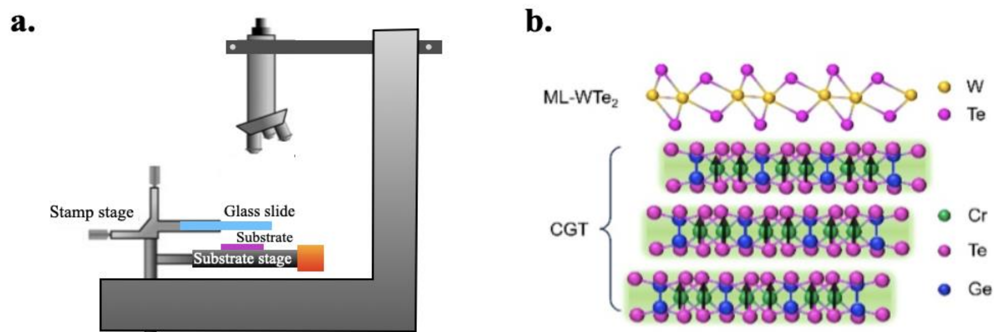

Figure 2.3: (a) a Transfer microscope with constituent components. (b) A stacked heterostructure that is made using this microscope.

The sample stage is composed of a machined aluminum surface with aluminum tape and carbon tape, respectively, attached to the surface. The aluminum tape improves adhesion of the carbon tape to the stage while the carbon tape itself holds the sample. A small hole is drilled into the sample stage and provides access for a thermocouple wire to be placed about 4 mm below the surface of the sample. This allows for accurate temperature readouts during the transfer process through a multimeter attached to the thermocouple The temperature of the sample stage is controlled through a resistive heating wire attached to the bottom of the stage. The cantilever is also constructed from machined aluminum and

contains two slots that hold a stamp used to pick up atomically thin flakes in the transfer process. The stamp consists of a base made out of a standard glass slide. On top of this, we place a small square section of polydimethylsiloxane (PDMS) polymer, in the center of the glass slide. A polymer film is first made by dissolving poly (bisphenol A carbonate) (PC) crystals in chloroform (8% by weight) and spreading a droplet between two clean glass slides to create a thin coating. The PC polymer can be cut with a sharp blade and applied to a suitable surface after it has dried in the air for a little while. The PC film was placed on top of a polydimethylsiloxane (PDMS) "stamp" situated on the center of a glass slide (it's easier to use the smaller size of PC than the PDMS). Here you can use both PC and PPC technique to pick up flakes. Using the PC has some advantages, first PC has less residue than other polymer like PPC (Polypropylene carbonate), and second you can pick up different flakes even in monolayer limit without using hBN or other insulator material. Depending on the transferring stage at the transfer microscope (We have 2 different controller stage inside the glove box) you can put the PDMS on the middle of the glass slide or at the end of it. We present challenges inherent to this process when creating these structures and methods to overcome them. In Section 2.3.1, we explain a useful variation to the standard transfer method known as the direct stamp exfoliation technique.

2.3.1 Dry Transfer Technique

Using a polymer-based transfer process, suitable flakes were manually piled to create heterostructures [103]. A micro-manipulator at an optical microscope with a long working distance lens is used to manipulate the polymer stack. Van der Waals flakes can be

collected by first lowering the polymer stack to make contact with the silicon wafer. The PDMS expands when heat is applied to the silicon chip, allowing the waveform of the PC film to gradually get closer to the desired flake. Increasing the temperature can help you to be in contact with the desire flakes without making bubbling Once the PC film covers the flake or folding the flake. Keep the temperature high for some minutes and then cool down the chip, for some materials pick up the material at higher temperature is easier and you have higher chance to pick up clean whole piece. The polymer stack is retracted with the van der Waals flake attached as illustrated in Figure 2.7.

Once a suitable flake is picked up by the polymer film (typically hexagonal boron nitride), additional flakes can be picked up by using the attractive van der Waals forces between any two flakes in contact as shown in Figure 2.7.

Many layers can eventually be built. The step-by-step procedures for carrying this out are depicted schematically in Figure 2.7. As seen in Figure 2.7.a, we begin by attaching the PC/PDMS stamp to the cantilever and placing a Si/SiO2 substrate containing a few layer hBN flake onto the sample stage. We then lower the cantilever such that the stamp contacts a corner or one edge of hBN flake (Figure 2.7.b), not fully in contact!! By heating the sample stage to 90°C, first let the PC fully cover the hBN flake and second adhesion between the PC and the hBN flake is enhanced, such that the hBN preferentially binds to the PC over the Si substrate underneath. Next, we cool the stage back down to 60°C or below in order to harden the PC layer, and also let the PC with hBN coming off. If by lowering the temperature PC didn't come off, we then not too fast, not too slowly lift up

the stamp, picking up the hBN flake with it (Figure 2.7c). After successful pickup of a few-layer hBN flake, we place another Si/SiO2 substrate containing a monolayer flake of WTe2 on the sample stage. Since monolayer of WTe2 has very small contrast with SiO2/Si substrate, more like shadow, it's very hard to see it over the 5X or 10X magnification, in this case it's better to use 50X magnification lens.

We then slowly lower the cantilever, aligning the hBN flake on the stamp with the WTe2 before bringing the two into contact. Before making contact, applying the heat and heating the stage to 100 °C and slowly lowering the stage down and keep hBN and WTe2 flakes together for 3-5 minutes at 100 °C temperature and then cooling to 90 °C and lift up the stage slowly, I usually used speed of 0.5rmp at our lab view program. The reason we increased the temperature to 110 °C, to increase the adhesion Van der Waals force between the hBN and the WTe2 flake and remove the bubbles which may can appear while you make hBN and WTe2 in contact with. A hint here, if you make a part of WTe2 in contact with hBN and let the heat at 110 °C let the rest being in contact you have almost bubble free device. So since after 120 °C PC started to soft, while you want to make contact between flakes you should never go above 120 °C, because you cannot lift the PC with PDMS and PC will drop on surface. If this happened you need to lower temperature to 60 °C and let the PC be cold and firm and repeat the process again, although it's very harder to pick up PC again. Next, we need to pickup of a few-layer hBN flake, we place another Si/SiO2 substrate containing an ultrathin flake of hBN on the sample stage. We then slowly lower the cantilever, aligning the hBN/WTe2 flake on the stamp with the new hBN.

After applying the same heating and cooling procedures as before, we pick up the hBN flake. At this point, we place the final substrate to the bottom thicker graphene layer. Once again, we lower the cantilever, aligning the hBN/WTe2/hBN structure with the bottom multi-layer graphene, and we bring the stamp and substrate into contact at 110°C (Figure 2.7h). For this final transfer step, we heat the sample stage to 150°C, which passes the glass transition temperature of the PC, causing it to be soft and sitting on the SiO2/Si substrate. We then raise the stamp very slowly, such that the soft PC peels off the PDMS and stays on the substrate (Figure 2.7l). The PC film can then be dissolved in chloroform or other solvents, leaving behind the van der Waals heterostructure. After using the chloroform for 10-15 minutes is better to put the stack in Acetone and IPA for short time 30 min to 1 hour to get rid of the chloroform residue, removal of the PC, and leaving behind the completed graphite-hBN-WTe2-hBN heterostructure.

The final stack can then be thermally annealed to remove the bubbles or some residue, and also, we can use atomic force microscopy to clean the surface and characterized it. For annealing you can use a chamber with Ar gas, but since we don't have it here, we keep the sample inside the glove box which has Ar gas flowing inside and put the sample on the hot plate with 350-400 °C for 5-7 h.

Additional challenges occur in the later steps of this process. This includes some difficulty in making the electrodes on WTe2 layer. As mentioned before, WTe2 is an air sensitive material, and we cannot etch the hBN to make the space to deposit the metal on top of it.

This problem can be ameliorated by prefabrication the electrodes and then transfer the hBN-WTe2 on top if it as we show the recipe on figure 2.8.

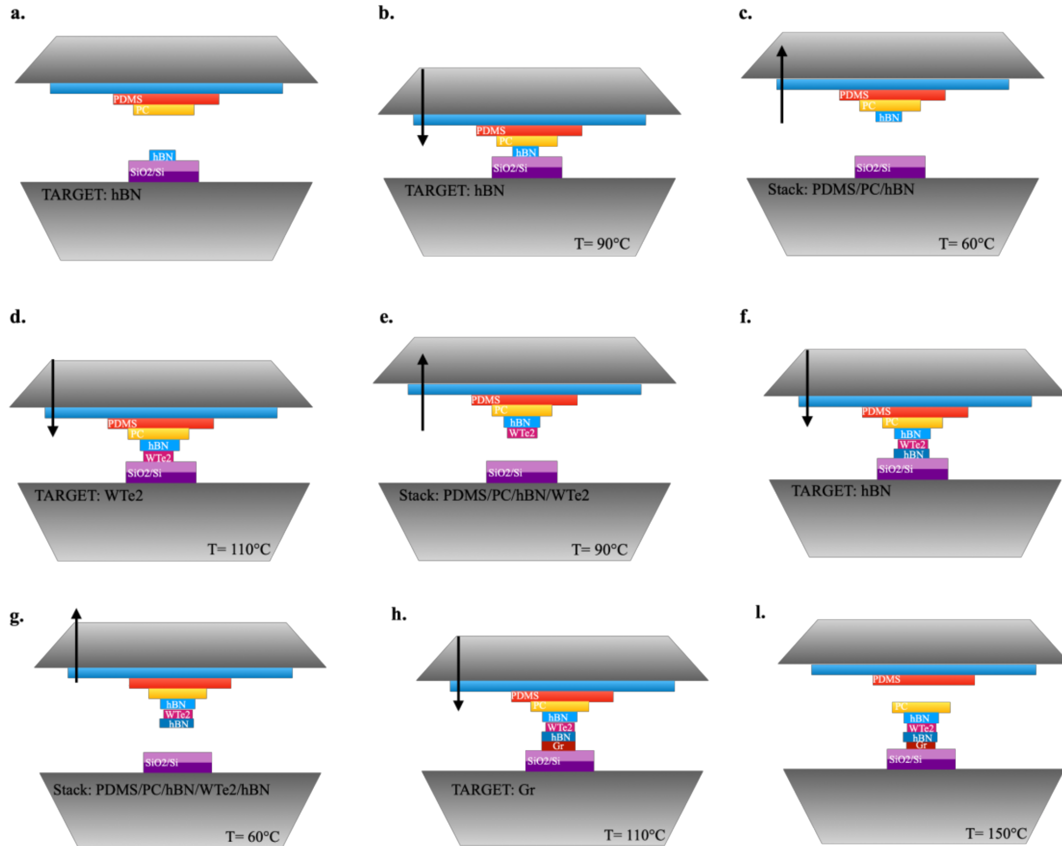

Figure 2.4: Schematic of standard method of dry transfer assembly of Graphite- hBN- WTe2- hBN heterostructures. (a) Initially, a hBN flake is placed on the sample stage and a stamp is made consisting of a glass slide, PDMS, and PC. (b) The stamp is lowered until it encounters the hBN on the sample stage. (c) After cooling the stage to 60˚C the stamp is removed from the stage, picking up the hBN flake. (d) The same procedure is used to pick up the next layer of WTe2. (e) then the layer of WTe2 is pick up. (f) next hBN flake is placed on the stage and used the same recipe to pick up at (g). (h) placed the heterostructure on Graphit gate. (l) The stage is heated to 150˚C to soft the PC layer, and the stamp is raised slowly to allow the PPC to separate from the PDMS, leaving the completed heterostructure on the desired substrate. The PC layer is then removed in an acetone bath.

As we described above, first we need to make G/hBN heterostructure and fabricate the electrodes which we describe it in the next section. So, for making the Gr-hBN we followed

the same procedure and need to pick up the hBN first and then pick up the Gr gate and then drop it on the SiO2/Si which we make the align mark on it. We make the align mark and transfer the sample on it due to this fact that, first to avoid the resist, each time fabrication needs to do spin coating and put some resist on our heterostructure, so we need to minimize this step. Second, you can choose the cleanest area on your SiO2/Si substrate from dark field image and drop the heterostructure.

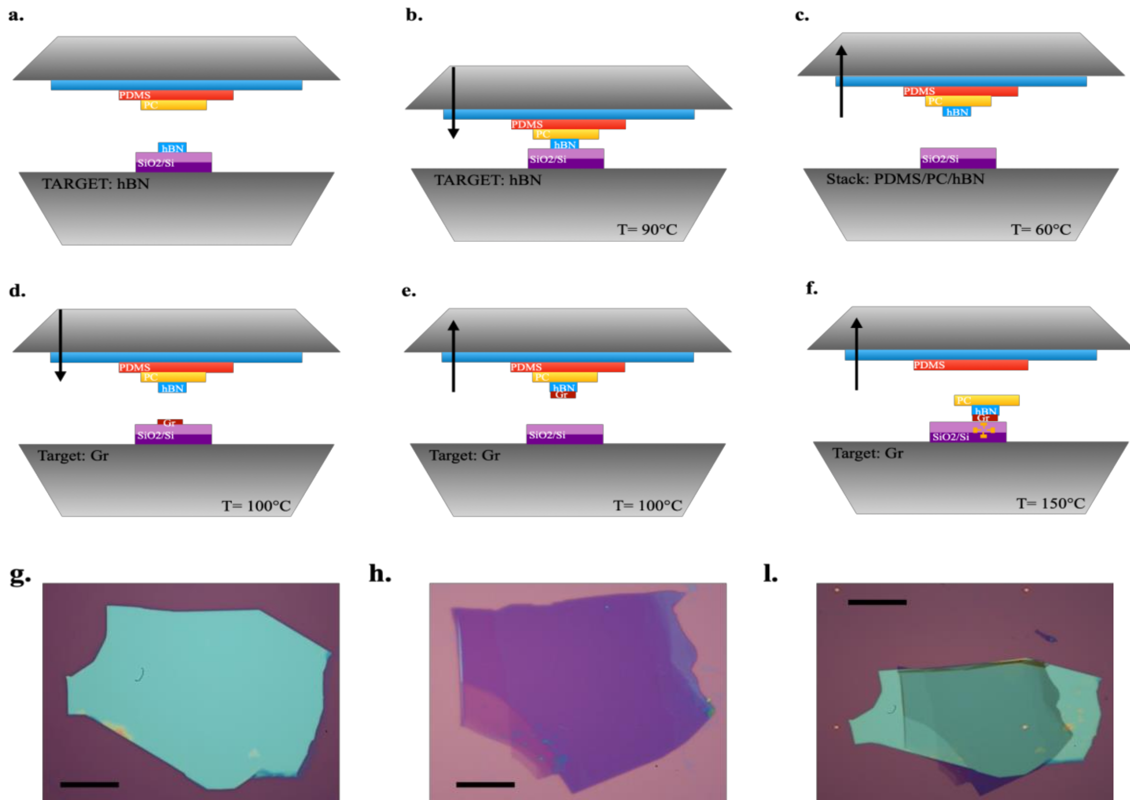

Figure 2.5: Schematic illustration and optical images of the dry-transfer process. (a) Initially, a hBN flake is placed on the sample stage and a stamp is made consisting of a glass slide, PDMS, and PC. (b) The stamp is lowered until it encounters the hBN on the sample stage. (c) After cooling the stage to 60˚C the stamp is removed from the stage, picking up the hBN flake. (d) The same procedure is used to pick up the next layer of Gr at 100 ˚C. (e) then the layer of Gr is pick up. (f) The stage is heated to 150˚C to soft the PC layer, leaving the completed heterostructure on the desired substrate. (g) bottom BN, (h) Graphite, (l) Gr/hBN on SiO2/Si with align marks. The black scale bar in images is 20 µm.

Next, after we make the electrodes on the substrate is the time for transferring the WTe2 on it which we explained it in section 2.3.1 Dry Transfer Technique. On figure 2.9 we showed Schematic illustration and optical images of the heterostructure. The illustration of the PPC transferring also explain in Appendix A.

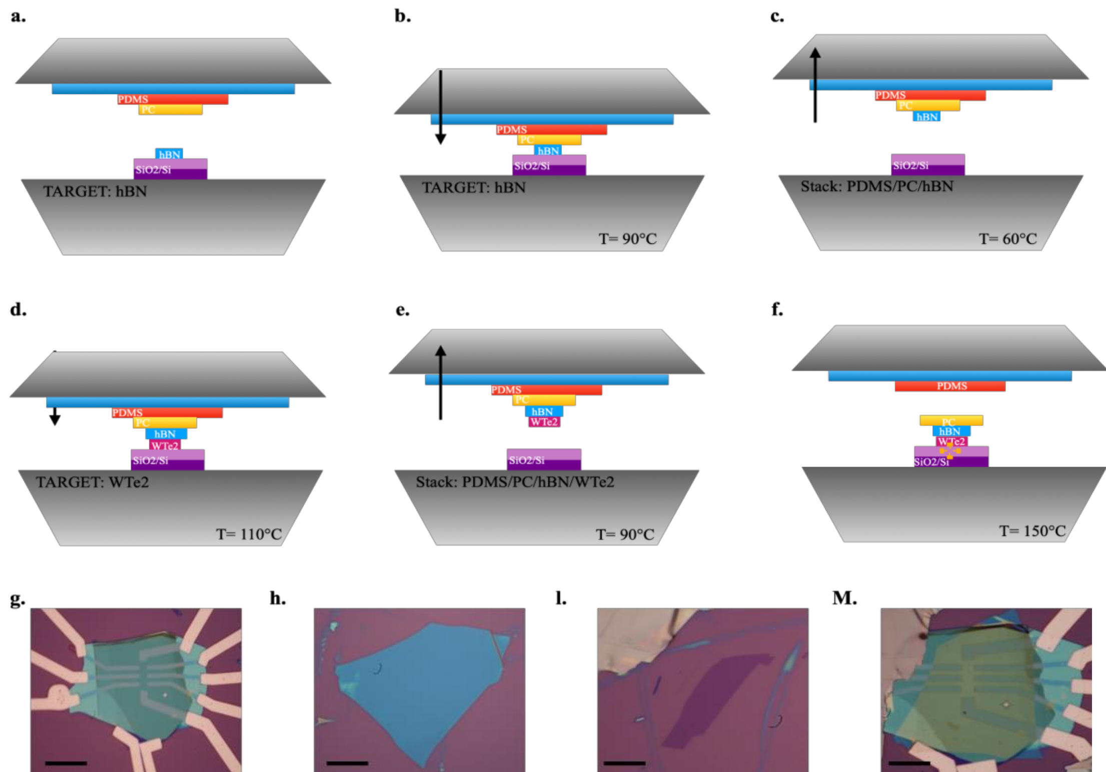

Figure 2.6: Schematic illustration and optical images of the dry-transfer process. (a) Initially, a hBN flake is placed on the sample stage and a stamp is made consisting of a glass slide, PDMS, and PC. (b) The stamp is lowered until it encounters the hBN on the sample stage. (c) After cooling the stage to 60˚C the stamp is removed from the stage, picking up the hBN flake. (d) The same procedure is used to pick up the next layer of WTe2 at 110 ˚C. (e) then the layer of WTe2 is pick up. (f) The stage is heated to 150˚C to soft the PC layer, leaving the completed heterostructure on the desired substrate. (g) prefabricated electrodes on Gr/hBN, (h) top BN, (l) monolayer of WTe2, (M) hBN-WTe2-hBN-Gr heterostructures. The black scale bar in images is 20 μm.

2.4 Device Fabrication

We utilize fabrication tools in a cleanroom environment to transform a just-transferred heterostructure into a device suitable for measurement. First, Using Design CAD 2000 and Nanometer Pattern Generation System (NPGS) software developed by JC Nabity Lithography Systems, we design patterns necessary for the lithography process. We then feed these designs into a Leo XB1540 focused ion beam (FIB) milling system, which writes the patterns onto a layer of resist coated on a desired heterostructure. In this section we propose a standard fabrication method that successfully produced the majority of our devices. We utilize two major steps in the standard fabrication procedure of heterostructure devices. First, we write alignment markers onto the sample near the heterostructure, which allows for precise writing of electrical contacts in the subsequent step. To carry out the fabrication of alignment markers, we are using the align mark file at Design CAD 2000 workspace which we construct a square array of alignment markers consisting of small crosses a few microns long on a side separated from each other by distance of 60 μm, and after each 10 small align mark, we have a bigger marker. Our array consists of a series of both large and small alignment markers, which we use for rough and fine alignment, respectively, of our desired contact pattern. We overlay this alignment pattern onto the optical image of the heterostructure in the CAD file. We need to estimate the position of the flake under the optical microscope and record the numbers to have tough idea to tell the FIB equipment to draw the align mark there. In this case you can use the optical microscope with the 5X. We load the completed alignment file into the NPGS software on

the FIB machine. Next, we spin-coat a suitable resist onto the sample in preparation for writing the alignment markers. We first spin-coat a layer of methyl methacrylate (MMA) onto the surface of the sample at 4000 rpm for 40 s with a 1000 rpm/s ramp. Afterward, we heat the sample at 180°C for 10 min to let the polymer set. We then spin-coat a second layer of poly-methyl methacrylate (PMMA) onto the sample using the same parameters, and we heat the sample under the same conditions as well. We utilize a double-layered resist since exposure to the electron beam and developer will cause the MMA layer to undercut relative to the PMMA, leading to more structurally stable contacts. After coating the sample with resist, we utilize the FIB to write the alignment markers. The use of this machine involves a series of specific steps. First, with the toothpick we drop a solution of IPA and silver paste (make sure not to use Acetone which can dissolve the MMA and PMMA) along one edge of the substrate, which to have a conductive surface to focus the electron beam. We then load the sample into the main chamber and evacuate it. After sufficient vacuum has been reached, at roughing pump levels, we engage the electron beam in secondary electron mode. Next, we find the conductive silver paste, and focus the electron beam on a small fleck of unearthed material about 1 μm in size. With the beam focused, we reposition it over the chosen big align mark at top center to put origin there. Immediately, we initiate the writing of the patterns through the NPGS software in order to minimize overexposure at the origin point. We then remove the sample from the FIB and develop it using a combination of solutions. We place the sample in a solution to prepare 3 to 1 deionized water and isopropanol by weight in a clean glass beaker. (We can use MIBK for developing here too!) Place beaker with solution in an ice bath for at least 10

min. While holding chip in tweezers, agitate gently in the cold solution for 2 min. Immediately blow-dry with dry nitrogen gas. check your pattern, if fully develop then put the solution to cold place if not continue putting your chip in solution for 1 min and check the process and continue till your pattern fully develop.

Two points here: first: If you are using MIBK instead of DI Water/IPA, you only need to agitate gently in the MIBK only for 20 seconds and then leave in the IPA for 20 seconds and check the pattern with optical microscope then if the pattern didn't develop do the same recipe for 5 second MIBK and 5 second IPA and continue the process to get the fully developed pattern.

Second, For the material which has Te inside like FeGeTe or CrGeTe bake the resist both MMA and PMMA at 120 ∘C for 10 min, because high heat can damage and change the properties of this material. Next, we load the sample into the ICP, using reactive ion etching to clean the the pattern and make a fresh interface. As the last step in the fabrication of alignment markers, we bring the sample to an e-beam evaporator for metal deposition. We load the sample into the chamber, and pump down to a pressure less than 6.5 x 10-6 torr. We then deposit successively 5 nm of Cr followed by 50 nm of Au. The Cr forms an adhesion layer to the surface of the Si substrate. Though any material could be used for the alignment markers since they make no contribution to the electrical contact of the device, we utilize Au for its high visibility under an electron beam, and we use Cr simply because this is the adhesion layer used when writing the actual contacts. After evaporation, we place the sample in an acetone bath for several hours to allow the remaining resist to dissolve.

Finally, we rinse the sample to lift off excess Au, leaving behind our completed alignment markers, which we again confirm by inspection under an optical microscope.

Once the alignment markers are produced, we then turn our attention to fabricating the actual contacts of the device. As in the case with the alignment step, we begin by taking a series of optical images of the sample. We take a single large-area, good resolution image at 5x magnification that captures the heterostructure as well as all the alignment markers. We then choose 4 large alignment markers to use for rough alignment, and we take 50x magnification images of these 4 large crosses. Similarly, we choose 4 small markers for fine alignment. We utilize 4 small crosses adjacent to each other that are located next to the heterostructure, in order to maximize alignment fidelity. We take a single 100x magnification image that includes both the heterostructure and the 4 chosen small crosses. In order to make sure all these images are in the same orientation; we initially zoom in to the central large cross and a small cross on its right or left and rotate the image such that these crosses are connected by a straight line. We take all the optical images only after this step. With these optical images, we load them into another Design CAD 2000 workspace and align all the images relative to each other. We take samples of large and small cross designs from the alignment CAD file and overlay them carefully onto the chosen large and small crosses in our optical images. We then design the actual contacts to be written onto the heterostructure. Each contact terminates at a large square contact pad used for wire-bonding to a chip carrier. After completion of contact design, we choose an origin point for the contact file, typically the central large cross or one of the other large crosses. Since

the portion of the contacts closer to the heterostructure needs to be written much more precisely than the large contact pads far away, we break up the CAD file into several files that can be written at various resolutions. Three files are composed from the contact design, and a separate file contains the alignment markers. We then load all of these files into the FIB machine. After spin-coating resist onto the sample for a second time using the same procedures described earlier, we write contacts using the FIB. We utilize all of the same procedures used in writing the alignment markers up to navigating to the origin point of the alignment markers. Usually, at this stage we choose the center of the big align mark as an x= zero and y= zero and then we know the distance from the origin (one of the small align mark close to the sample) and we can tell to FIB what the starting point is. After this, we navigate to the origin point of the contact files, and we run the NPGS software, which performs both rough and fine alignment of the sample before finally writing the contacts. Once the contacts have been written, we develop them in the same way as for the alignment markers, and we once again bring the sample to the evaporator for metal deposition.

For the Back gates were mostly contacted with a Cr/Au layered thermal evaporation. Typically, the chromium sticking layer was about 5 nm thick while the gold was around 50 nm thick (Ti has same sticky behavior and can use it instead of Cr). For contact to graphene encapsulated devices, one-dimensional edge-contacts were utilized 104. For WTe2 based devices, we made the 5 nm inner electrodes first and 5/50 nm Cr/Au for the outer parts to have better contact with monolayer WTe2 and electrodes. Again, using reactive ion etching to clean the pattern and make a fresh interface. The sample was then

quickly loaded into a thermal evaporator equipped to deposit the metal contact. Afterward, we lift off the metal in the same manner as before, leaving behind a completed device. For the large patterns of photolithography, we also can use a Karl Suss mask aligner in a cleanroom environment. First, we spin-coat a layer of 5214 resist onto the wafer at 4000 rpm for 40 s with a ramp of 1000 rpm/s. Next, a layer of HMDS polymer is also spin-coated onto the wafer under the same conditions. We then heat the wafer on a hotplate at 110°C for 5 min in order to let the resist set. We then expose the resist to ≈ 15 s of ultraviolet radiation. The sample is developed in AZ 400K developer for 1 min and rinsed with DI water.

In order to remove unwanted portions of the layer-transferred heterostructure, electron beam lithography was first utilized to create a mask from PMMA. Etching through graphite and graphene was achieved with an O2 plasma while etching through hexagonal boron nitride and all air sensitive materials like WTe2 required a SF6 plasma etching. For devices with an underlying graphite back gate, the device outline was defined with a substantial SF6 to remove all encapsulating hexagonal boron nitride (as well as monolayer graphene) outside. The graphite was not significantly affected because SF6 etch carbon-based materials very slowly. Any unwanted graphite was removed with a final O2 etch with a double-layer PMMA etch mask Conventional metallic contact was then made to the back gate and for the electrodes (see below).

Table 2.2: ICP information

	RF power(W)	ICP power(W)	Step time(S)	Gas (Sccm)
Gr	50	600	3	O_2, 50
hBN	50	600	10	SF_6, 30/ O_2, 3
WTe_2	50	500	5	SF_6, 25/ O_2, 2

Chapter 3: Compressibility and Capacitance Measurements

3.1 Introduction

The shape and size of Landau level density of states (DOS) peaks in a two-dimensional (2D) electron gas in the presence of a magnetic field applied perpendicular to the plane of the electron gas has generated considerable interest over the past two decades [105]. A 2D electron gas equilibrium characteristic is the thermodynamic DOS. No differentiation is made between localized and extended states. Nevertheless, theories regarding the mechanisms leading to the localization of states can be examined by observing the form density of state peaks connected to Landau levels [106].

Developing theories about the Quantum Hall Effect has relied heavily on the assumption of a nonzero DOS between Landau levels. A variety of experiments, including specific heat, magnetization, and capacitance studies have ought to probe the 2D DOS. In most cases, measurements have determined the DOS of a system with a fixed electron density in the 2D layer, with variation of parameters such as applied field and temperature [107–109]. Instead, the density of states at the Fermi energy as the Fermi energy varies is typically discussed in models of the 2D electron gas. To compare information with data, it must be transformed in the proper way. This process could add uncertainty in the original DOS

peak's form as a function of energy. Many of these experiments have, in fact, given only qualitative results on the DOS shape, and not a quantitative description of the DOS.

3.2 Thermodynamic Relations

Measuring the equilibrium characteristics of huge ensembles of particles is a focus of thermodynamics. By gaining access to an important thermodynamic property called compressibility, which has a direct relationship to the free energy of the electronic system, we may measure the ground state of a significant number of electrons.

It is helpful to explain the more well-known mechanical compressibility before going into the electrical compressibility, while keeping the temperature T and the number of particles N constant, assesses the relative change in an object's volume V (Here, V can be replaced by the area for a two-dimensional system) in response to an applied pressure p.

$$\kappa = -\frac{1}{v}\left(\frac{\delta V}{\delta P}\right)_{T,N} \tag{3.1}$$

A hard object, such as a tungsten rod, has a very little compressibility, as depicted in the cartoon in Figure 3-1, whereas an object that is easily deformed, like a rubber ball, has a considerable compressibility. With a few thermodynamic relationships, the mechanical compressibility can be transformed into an electrical compressibility. The intensive variables μ, T, and p are constrained by the Gibbs-Duhem equation:

$$Nd\mu = Vdp - SdT \tag{3.2}$$

By considering constant temperature:

$$(\frac{\delta\mu}{\delta P})_T \;=\; \frac{V}{N} \Rightarrow (\frac{\delta\mu}{\delta(\frac{V}{N})})_T = \frac{V}{N}(\frac{\delta\mu}{\delta(\frac{V}{N})})_T \tag{3.3}$$

There is a derivative with regard to the reduced volume V/N on each side of the equation. Without changing the relationship in Equation 3.3, we are free to discriminate while holding either N or V constant. We decide to keep V constant on the left [110].

$$(\frac{\delta\mu}{\delta(\frac{V}{N})})_{T,V} \;=\; (\frac{\delta\mu}{\delta N})_{T,V}(\frac{\delta N}{\delta(\frac{V}{N})})_{T,V} = -\frac{N^2}{V}(\frac{\delta\mu}{\delta N})_{T,V} \tag{3.4}$$

Holding N constant, we may determine the derivative on the right side of Equation 3.2.

$$\frac{V}{N}\;(\frac{\delta\mu}{\delta(\frac{V}{N})})_{T,V} \;= \frac{V}{N}(\frac{\delta P}{\delta V})_{T,N}\;(\frac{\delta V}{\delta(\frac{V}{N})})_{T,N} = \mathrm{v}\;(\frac{\delta P}{\delta V})_{T,N} \tag{3.5}$$

Putting everything together so

$$\frac{1}{\kappa} = -\mathrm{v}\;(\frac{\delta P}{\delta V})_{T,N} = \frac{N^2}{V}\;(\frac{\delta\mu}{\delta N})_{T,V} \tag{3.6}$$

The electronic compressibility takes into account changes in the total particle number in reaction to changes in the chemical potential, as seen in panels c and d of Figure 3-1, as opposed to assessing relative changes in volume with regard to pressure.

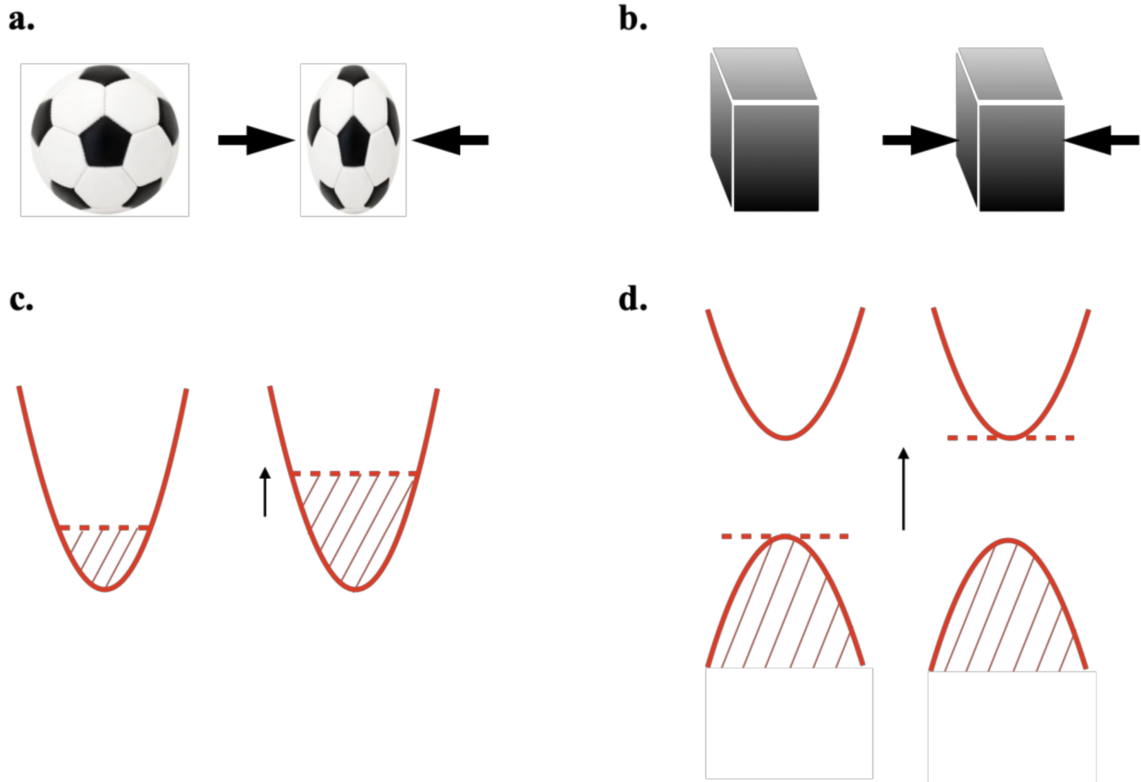

Figure 3.1: Compressibility comparison between mechanical and electrical. a) A ball has a high mechanical compressibility and can deform with only moderate pressure. b) The mechanical compressibility of a tungsten rod is low. c) Increasing the chemical potential $\delta\mu$ admits a significant number of extra carriers δn when it is in the midst of an energy band. It is very compressible electrically. d) When there is a gap in the chemical potential, increasing the chemical potential $\delta\mu$ admits no extra electrons, hence $\delta n = 0$ which it is very incompressible.

It is important to note that κ is regarded as a thermodynamic variable since it may be connected to a derivative of a thermodynamic potential, just like heat capacity or magnetization. In this instance, the suitable potential for a constant volume and temperature is the Helmholtz free energy F:

$$F = U - TS \tag{3.7}$$

$$dF = TdS - pdV + \mu dN - TdS - SdT \tag{3.8}$$

$$= -SdT - pdV + \mu dN \tag{3.9}$$

where the first law of thermodynamics, dU = TdS - PdV + μdN, has been applied. The chemical potential can be determined using

$$\mu = (\frac{\delta F}{\delta N})_{T,V} \tag{3.10}$$

and

$$\frac{1}{\kappa} = \frac{N^2}{V} (\frac{\delta^2 F}{\delta N^2})_{T,V}. \tag{3.11}$$

In the context of solid-state physics, μ and the electron density n = $\frac{N}{V}$ are more conveniently used to express k:

$$\kappa = \frac{\mathbf{1}}{\boldsymbol{n}^2} (\frac{\boldsymbol{\delta n}}{\boldsymbol{\delta \mu}})_{\boldsymbol{T,V}} \tag{3.12}$$

Additionally, the compressibility is frequently confused with the thermodynamic density of states when the pre factor is dropped:

$$\kappa \sim \frac{\boldsymbol{\delta n}}{\boldsymbol{\delta \mu}} \tag{3.13}$$

We usually refer to $\frac{\boldsymbol{\delta n}}{\boldsymbol{\delta \mu}}$ as the compressibility, and we frequently refer to an electronic phase as compressible or incompressible depending on whether it has a significant or negligible thermodynamic density of states.

3.3 Thermodynamic Density of States

One of the most essential parameters describing an electronic system is the thermodynamic density of states, along with the band structure. For instance, whether a material is electrically insulating or conducting depends on the presence of gaps in the density of states and how they relate to the chemical potential. The shift in the chemical potential caused by the addition of more electrons is measured by the thermodynamic density of states. This quantity is logically connected to the number of possible electronic states at the Fermi level if electron-electron interactions can be disregarded. Pauli exclusion forces us to only contribute electrons to the vacant states directly above the Fermi level as we increase charge. Electrons can inhabit states that are very close in energy to μ if the system has a significant amount of degeneracy at the Fermi level, perhaps in a metal or the middle of a Landau level. The compressibility $\kappa \sim \frac{\delta \boldsymbol{n}}{\delta \boldsymbol{\mu}}$ is then very high since the change in $\delta\mu$ caused by the addition of $\delta \boldsymbol{n}$ electrons is very modest. The Fermi level is compelled to rise quickly in order to access available states, however, if the Fermi energy lies in the middle of a band gap, as in the case of a band insulator. In this case, the shift $\delta\mu$ following the addition of $\delta \boldsymbol{n}$ electrons is significant and $\kappa \sim \frac{\delta \boldsymbol{n}}{\delta \boldsymbol{\mu}}$ is quite small.

It is necessary to compare the single-particle density of states to the thermodynamic density of states. How much energy is required to add additional electrons after waiting for the system to relax and return to equilibrium, according to the thermodynamic density of states? The important thing to remember is that the electrons are being added in the

adiabatic limit, allowing the remaining electrons to rearrange themselves and reach a new ground state. The single particle density of states poses the question, "How many possible electronic states exist at ΔE if I abruptly add an electron with energy $\Delta E = E$ - E_f away from the Fermi level?" The system is not allowed to relax. The slow, equilibrium charging of electronic systems characterized by the thermodynamic density of states will be the subject of the capacitance measurements in the next Chapter.

The two values can be directly connected to one another in the absence of electron-electron interactions. As illustrated in panel (a) of Figure 3-2, if we make a tunneling test with the Fermi level fixed at E_0 and tunnel up in energy to the unoccupied levels at $E = E_0 + E_1$, we can estimate the density of states g ($E_0 + E_1$). The thermodynamic density of states $\frac{\delta n}{\delta \mu}$ as seen in panel b would be equal to the chemical potential if we then moved it from $E_0 \rightarrow E_0 + E_1$ to that location. The assumption that the band structure stays constant while we adjust the electron density allows for the equivalency.

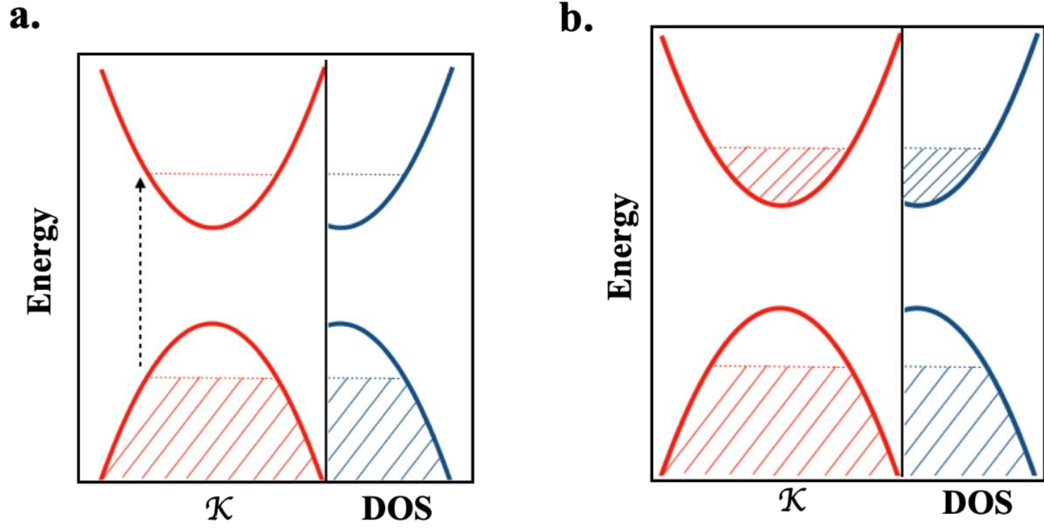

Figure 3.2: (a) Density of states with no electron-electron interactions. In the absence of interactions, the Fermi level at E_0 and measurement of the spectral (single particle) density of states at $E_0 + E_1$ are identical. (b) measurement of the thermodynamic density of states while the Fermi level is at $E_0 + E_1$.

The situation becomes more complex when electron-electron interactions are present. The electron density and curvature $\frac{\delta^2 E}{\delta \kappa^2}$ of the band structure have a significant impact on coulomb interactions between electrons often. As one adjusts the carrier density, the relative significance of electron-electron interactions may alter. The static band structure that could be easily filled or drained with electrons is no longer available to us. Electron-electron interactions can significantly alter the physics at the Fermi level and, to a lesser extent, the physics of the excitation spectrum at energies below the Fermi level when the band structure becomes dynamic. In this case, $\frac{\delta \boldsymbol{n}}{\delta \boldsymbol{\mu}}$cannot be equated with the total number of energy levels. The energy cost of adding charge is still rigorously defined by $\frac{\delta \boldsymbol{n}}{\delta \boldsymbol{\mu}}$ in this scenario, but its relationship to the single-particle density of states is broken. By examining

a spectrum measurement that accesses an electron at an energy below the Fermi level, which is located in a band gap in panel a, Figure 3-3 graphically illustrates this effect. If a band is entirely empty, there is typically little to no electron-electron contact since there is no charge present to experience the Coulomb force. The same analysis holds true if we think of a fully occupied band as acting like a completely empty hole energy band. As in the case of a quantum Hall ferromagnet, when energy bands are only partially filled, if non-orbital degrees of freedom such as spin or valley are present, the orbital degrees of freedom may decide that it is energetically advantageous to rearrange their energy hierarchy in order to reduce Coulomb repulsion. The general scenario is depicted in panel b, where a gap at the Fermi level appears when the conduction band is only partially filled. This gap is distinct from the band gap, a single-particle effect caused by the interaction of electrons and ions.

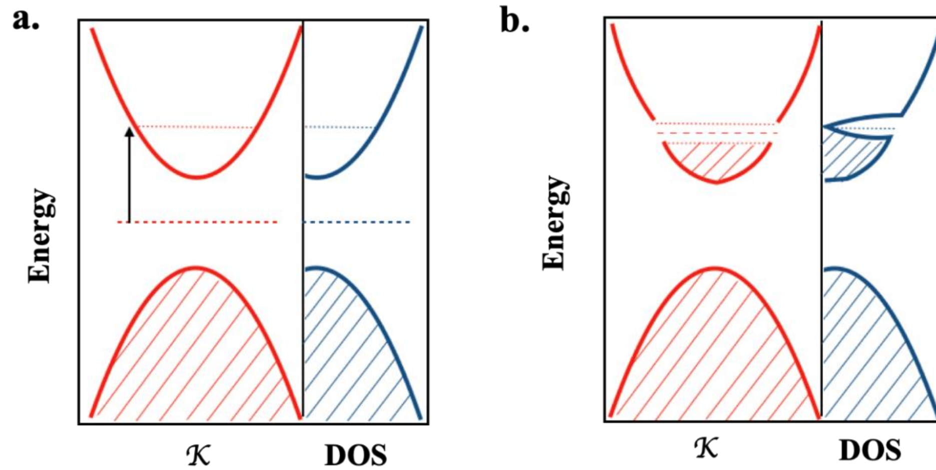

Figure 3.3: electron-electron interaction density of states the band structure is altered by electron-electron interactions as the chemical potential changes. In a) a predictable parabolic dispersion is seen when the Fermi level is placed within a band gap and excited to the center of the empty conduction band. In b) density-dependent interactions may cause a many-body energy gap to be created around the Fermi level when it is at a specific point. Due to the energy gap at the Fermi level, the thermodynamic density is greatly reduced.

3.4 Capacitance

It turns out that the relationship between the electrical compressibility and the capacitance between a two-dimensional material and a neighboring metallic electrode is very close. This section will go over the capacitance between two metal pieces before considering the capacitance between objects with finite densities of states. Any two metals have a mutual capacitance that indicates how likely they are to build up charge in response to an applied voltage differential, $Q = CV$. where V is the voltage applied across the structure, C is the mutual capacitance coefficient, and Q is assumed to be positive and denotes the net excess charge that has built up on one of the capacitor plates. Superposition is the recurrence

relation of the linear charge-voltage connection. If increasing the charge density to Q_0 causes a voltage V_0 to be produced between two metal objects, then finding $2V_0$ as a result of doubling Q_0 is necessary. The two pieces of metal's geometric arrangement and orientation, as well as the surrounding dielectric environment, are the sole determinants of capacitance. The inverse-square Coulomb force and the capacity of metals to produce a perfect equipotential on their surface because of the high density of mobile charge are what cause the geometric dependence. Any voltage difference that develops in the surface's tangential direction will be easily cancelled out by the free electrons on a metal's surface. After equilibrium is reached, it will come out that sharp and tightly bound patches draw a larger percentage of the total charge density as a result of their spatial isolation from the rest of the electron sea. Due to the increased, more expensive electric field density created by these enclosed areas, the geometry becomes crucial in deciding the final charge capacity. It is important to emphasize that the metal's internal electrical structure is unimportant. Classical electrostatics rarely specifies the specific metallic material gold, brass, aluminum, etc. when describing capacitors. Due to the fact that the densities of metal states are essentially unlimited, this estimate is quite accurate. Effectively, what does that mean here? Think about a parallel plate capacitor made of two pieces of gold operating in vacuum $C = \frac{\epsilon A}{d}$, where ϵ is the vacuum permittivity, A the lateral area, and d the plate separation. The charge increases as a voltage (δV) is applied across the capacitor (δQ = CδV). In the lateral region and at a depth of around a few Fermi wavelengths, $\lambda \sim n^{-1/3}$, where n is the total electron density, the charge builds up and $\lambda \sim$ 1 nm for gold. The carrier density is

$$\delta n = \frac{\delta Q}{e\lambda A} = \frac{C\delta V}{e\lambda A} = \frac{\frac{\epsilon\delta V}{d}}{e\lambda} \quad (3.14)$$

The density of states of gold can be approximate by $\frac{\delta n}{\delta\mu} \sim \frac{n}{E_f} \sim 10^{28}\ eV^{-1}m^{-3}$ where E_f is the Fermi energy. We are free to vary the separation d. We can consider an extreme limit by letting d = 1 nm, for every volt we apply across the capacitor, the chemical potential only rises by a few meV which constitutes a change of a few parts in a thousand of the Fermi energy of gold. This is a small change, and more importantly, it ensures that any shift in the anticipated charging rate of the capacitor due to chemical potential drift is constant over any reasonably accessible voltage range. This is because the value of the compressibility in gold will remain essentially unchanged as the chemical potential moves by negligible amounts. Additionally, the value of d = 1 nm is unphysical in the majority of cases because electron tunneling and subsequent vacuum breakdown would take place at low voltages (<1V), effectively shunting the capacitor. The impacts indicated above would have been correspondingly weaker if we had chosen a more realistic 10 nm.

3.4.1 Quantum Capacitance

A helpful approach of conceptualizing capacitance is suggested by the analysis that came before. When a voltage is put across a capacitor, a specific quantity of energy is supplied to the system to be used for work. In order to create an electric field, the voltage can transfer charge density, but in doing so, it must use some of the energy allotted to it to modify the Fermi level in the plates. In contrast to the cost of charging that is solely electrostatic, the quantum mechanical cost to raise or lower the Fermi level is relatively negligible for

materials like metals that have a very high density of states. However, in many materials, the density of states can be fairly low compared to how easily they can be charged, which makes the chemical potential change caused by applying voltage considerable. The chemical potential shift will be substantially reliant on the gate and magnetic field, making monitoring of changes in the compressibility practical even if it only causes a minor perturbation on the essentially linear charging rate. This chemical potential shift expresses itself as a contribution to the capacitance signal, which may be monitored and related to the compressibility of the electronic system, as will be made obvious below. Consider a parallel plate capacitor, as shown in panel of Figure 3-4, with one perfect metallic plate having an unlimited density of states and the other plate composed of monolayer graphene (which has very small $\frac{\delta\mu}{\delta\boldsymbol{n}}$). It may be any other electronic system with a finite density of states, though. As shown in panel c, by applying a voltage to the metal plate and grounding the graphene through an ohmic contact at the boundary, a total electrochemical difference of eδV is produced across the capacitor. You can create a complete loop with no network by imagining transporting a test charge (e) from ground via the voltage source, across the geometric capacitance, increasing the material's chemical potential by dμ, and returning to ground through the ohmic contact. keeping track of the energy in each area we have:

$$0 = -e\delta V + e\delta\phi + \delta\mu \tag{3.15}$$

When the geometric capacitance $\frac{\delta Q}{C_{geo}}$ and accumulated charge of the graphene cause a shift in electrostatic potential $\delta\phi$. This equation can be interpreted as describing the energy expenditure for charging graphene with δQ. We must pay the potential energy cost $e\delta\phi$ as

well as the quantum kinetic energy cost within the material $\delta\mu$. We can rearrange this to demonstrate quantum capacitance.

$$\frac{\delta\mu}{\delta V} = e(1 - \frac{1}{C_{geo}}\frac{\delta Q}{\delta V}) \tag{3.16}$$

However, for our purposes, it makes sense to define a differential capacitance $C_T = \frac{\delta Q}{\delta V}$ in terms of the total charge modulated as a function of the voltage V. Previously, we described capacitance in terms of the ratio of charge to voltage $C = \frac{Q}{V}$, and by expanding the $C_T = \frac{\delta Q}{\delta V} = \frac{\delta Q}{\delta\mu}\frac{\delta\mu}{\delta V}$. We can convert from charge units to density using the formula $\delta Q = eA\delta n$, where A is the lateral area of the capacitor, in an effort to correlate with the compressibility $\frac{\delta n}{\delta\mu}$. By using the 3.16, the total capacitance is $C_T = e^2A\frac{\delta n}{\delta\mu}(1 - \frac{C_T}{C_{geo}})$ and we can solve for C_T.

$$\frac{1}{C_T} = \frac{1}{C_{geo}} + \frac{1}{Ae^2\frac{\delta n}{\delta\mu}} \tag{3.17}$$

$$\approx \frac{1}{C_{geo}} + \frac{1}{C_q} \tag{3.18}$$

where we define the quantum capacitance as being directly proportional to the compressibility $Ae^2\frac{\delta n}{\delta\mu}$ [111]. Although this word has been described as a capacitance, it's vital to keep in mind that it only results from energy conservation and the circuit's closed equipotential channels. The quantum capacitance behaves as if it were in series with an ideal geometric capacitance, as shown by the fact that the geometric and quantum capacitances sum up reciprocally. However, it is always there any time a two-dimensional system is gated, even though it certainly plays a significant part in any direct measurement

of the total capacitance of a system with limited density of states. The field effect modulates the charge density of a two-dimensional structure even in transport measurements where the capacitance is not observed, and the quantum capacitance impacts how quickly an applied gate voltage adds charge to the system.

The thermodynamic equilibrium of the entire capacitor system, which produced $e\delta V = e\delta\phi + \delta\mu$, should be distinguished from the sense in which $\frac{\delta n}{\delta\mu}$ is an equilibrium thermodynamic property, in order to avoid any mistake. The electrochemical potential μ_{e-ch} is the appropriate chemical potential for the entire capacitor construction that meets the first law of thermodynamics, dF = μdN at constant temperature and volume. The voltage source and potentials would shift electrons within the circuit to achieve electrochemical equilibrium if it were not already there. In the prior procedure, the external voltage μ_{e-ch}, graphene μ_{e-ch}, metal $e\delta V = e\delta\phi + \delta\mu$ was used to determine the electrochemical potential difference between the metal and graphene. We assume that the metal's fixed ground electrochemical potential. The compressibility $\frac{\delta n}{\delta\mu}$, which is defined with reference to the chemical potential, is not identical to graphene's n/$\delta\mu_{e-ch}$, graphene $\frac{\delta n}{\delta\mu_{e-ch}, graphene} \sim \frac{\delta n}{\delta V} \sim C_T$. The answer lies in comprehending that the electronic system is presumed to be isolated from any external potentials when the compressibility $\frac{\delta n}{\delta\mu}$ is defined as a thermodynamic property. In this instance, $\mu = \mu_{e-ch}$ represents the increase in internal energy caused by the addition of one electron. To obtain the compressibility $\frac{\delta n}{\delta\mu}$, a

thermodynamic property of the isolated two-dimensional system, we can employ a capacitor structure that is in electrochemical equilibrium with an external voltage source.

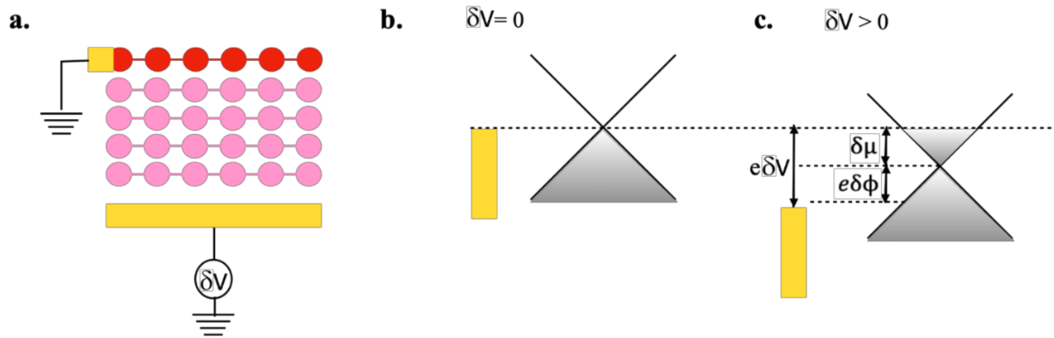

Figure 3.4: Diagram of quantum capacitance (a) a metal gate is separated from a layer of monolayer graphene (gray) by an insulator (pink). Between the gate and an ohmic contact on the graphene, δV is applied as a voltage. (b) If $\delta V = 0$, electrochemical equilibrium exists between the gate and graphene (we assume no work function difference). (c) If $\delta V > 0$, an electrochemical difference of δV is acquired between the gate and the graphene. By an amount eδV, the gate is lowered below a ground reference. This is made up of two contributions: the change in chemical potential $\delta\mu$, where μ is measured from the charge neutrality point, and the electrostatic potential eϕ.

Typically, experimentalists make the approximation eAn = $C_{geo}\delta V$ which is only ever approximately true. Whenever a parallel-plate capacitor is gated, the relationship

$$\frac{1}{C_T} = \frac{\delta V}{\delta Q} = \frac{1}{C_{geo}} + \frac{1}{Ae^2\frac{\delta n}{\delta \mu}} = \frac{1}{C_{geo}} + \frac{1}{C_q} \quad (3.19)$$

To highlight the significance of quantum capacitance in a material with low density of states, we took into account a metal gate and graphene in the aforementioned example, where $\frac{\delta n}{\delta \mu}$ refers to graphene's thermodynamic density of states. However, since this relationship is fully universal, we might have substituted another metal for the graphene. In this case, $\frac{\delta n}{\delta \mu} \gg \frac{C_{geo}}{Ae^2}$ for normal C_{geo} values so that $\frac{1}{C_T} \approx \frac{1}{C_{geo}}$. The implicit presumption

that the typical area-normalized geometric capacitance $\frac{C_{geo}}{A} \ll e^2 C_q$ lies beneath many of these estimates and assumptions about the extent of the compressibility of metals. Only in respect to the other capacitance scale in the system, C_{geo}, can the existence of a large (irrelevant) quantum capacitance in a two-dimensional system be determined. By altering the ratio $\frac{\epsilon}{d}$, it is simple to build a metal-graphene parallel plate capacitor with a ratio $\frac{C_{geo}}{C_T}$ that is arbitrarily near to 1. The ratio for parallel plate capacitance can be calculated explicitly as follows:

$$\frac{C_{geo}}{C_T} = 1 + \frac{C_{geo}}{C_q} = 1 + \frac{\epsilon}{de^2 \frac{\delta n}{\delta \mu}} \tag{3.20}$$

Since the area is proportional to both the geometric capacitance and the overall charge introduced into the material as a result of $e \quad A \frac{\delta n}{\delta \mu} \delta \mu$, the area has fallen out. However, the ratio $\frac{\epsilon}{d}$ greatly influences the length scale d. If we modify ϵ or d to improve geometric capacitance, eventually $C_{geo} \approx C_q$ and both will make significant contributions to C_T.

There are numerous definitions of chemical potential used in the disciplines of condensed matter physics, semiconductor physics, and electrochemistry. The Fermi-Dirac distribution defines $\delta \mu$ as the energy of the highest occupied electron, or the appropriate location within an energy gap, which is often defined with respect to a band minimum (in the case of a semiconductor) or charge neutrality point. We will refer to μ as the energy of the highest occupied electron (or appropriate location within an energy gap so that μ is the 50% electron occupancy probability in accordance with the Fermi-Dirac distribution), which is

frequently defined with respect to a band minimum (in the case of a semiconductor) or charge neutrality point (in Dirac-like systems). At zero temperature, μ is equivalent to the Fermi level E_F relative to the band minimum or charge neutrality point.

3.4.2 Circuit Perspective of Quantum Capacitance

Any single parallel plate construction, as depicted in Figure 3-5, can be thought of as containing a geometric and quantum capacitance contribution.

One can solve a simple capacitive voltage divider to determine the chemical potential change in response to an applied voltage:

$$\frac{\frac{\delta\mu}{e}}{\delta V} = \frac{C_{geo}}{C_{geo}+C_q} = 1 - \frac{C_T}{C_{geo}} \tag{3.21}$$

The intended result is that $\delta\mu \rightarrow 0$ if $C_q \rightarrow \infty$ (as in a perfect metal). In particular, Equation 3.21 is helpful. It is not necessary to explicitly measure the gate-dependent (and potentially complex) quantum capacitance in order to compute changes in the chemical potential.

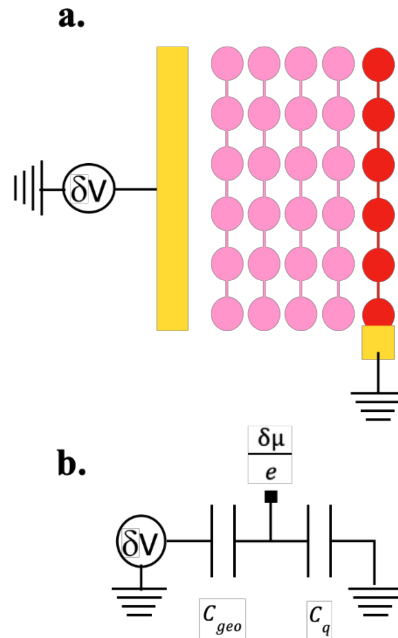

Figure 3.5: Circuit representation of quantum capacitance. (a) parallel-plate capacitor is made from a piece of metal (gold) and graphene (gray), which are separated from one another by a pink dielectric. (b) The geometric capacitance and the quantum capacitance are two components that can be separated out of the parallel-plate geometry. The voltage δμ/e between the geometric and quantum capacitances can be used to describe the chemical potential change.

3.4.3 Extraction of the DOS from capacitance measurements

The technique presented in this chapter use capacitance measurements to determine the 2d DOS. like many experiments, ours are carried out a different magnetic field strength and we also vary the electronic density in a quantum well by means of a gate bias. The technique used here relates this gate bias to the Fermi energy in the quantum well and yields the DOS from the capacitance data, which can then be plotted as a function of Fermi energy.

As the Landau index is changed, there are significant conductivity fluctuations in the plane of the 2d electron gas, which pose challenges for capacitance spectroscopy-based DOS

estimates. These findings from Goodall, Higgins, and Harrang have shed light on some of these challenges. Attempts at circumventing these problems have been made by restricting the experiments to low measuring frequencies.

3.5 Measurements Scheme

Simply measuring the capacitance C_T and applying the existing relationships to extract C_q, which is specified by the compressibility, is all that is required to access the compressibility. It turns out that it is difficult to measure the capacitance to the resolution needed for this thesis. We will now cover a collection of well-established methods for monitoring high-resolution capacitance signals at cryogenic temperatures [112].

3.5.1 Limitations of the Simple Transport measurement

To measure a device with an unknown impedance Z, the easiest method is to source a voltage across it and measure the current I am flowing through it, as is done in normal electron transport. Using Ohm's law $V = IZ$, the impedance can be simply related. First, let us imagine Z ≈ R (any capacitive or inductive terms are small). Long cables that add line resistance are required if we wish to install the gadget in a cryostat. Where ohmic connections come into touch with van der Waals or semiconductor materials at low temperatures, there might also be a high contact resistance. Each line's parasite resistances might collectively be referred to as R_{par}. In order to ignore rotations caused by the capacitance of the measurement lines to ground, we assume that the measurements are

performed at DC or very slow AC excitations V. The total impedance inferred from a two-terminal measurement will be

$$Z = R + 2R_{par} \tag{3.22}$$

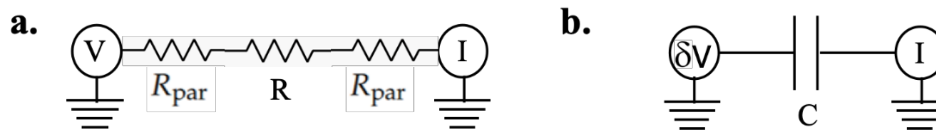

Figure 3.6: Transport-style measurement scheme. a) A voltage V is used to source an impedance Z = R, and an ammeter is used to measure its current. In a laboratory setting, parasitic resistances resulting from the lines and connections R_{par} are simple to handle. b) It is difficult to implement an analogous measuring scheme for a capacitor since most ammeters cannot operate beyond a frequency of around 10 kHz, which limits currents to around 1 pA for a sample of at least 1 pF.

Typically, the baseline is shifted by the simple additive $2R_{par}$ term. The signal, which is recorded at room temperature using a two-probe geometry, is frequently only minimally altered by the parasitic elements' addition to the sample impedance in series. A four-probe geometry can be used if accuracy is needed, such as when measuring the zero-resistance state of a superconductor. In this geometry, the current is sourced along two lines that experience a voltage drop due to the contact resistance, and the voltage difference across the sample can be probed with different contacts. This just costs the experimenter one extra voltmeter in the lab when done at room temperature. With the exception of requiring four ohmic contacts as opposed to two, the cryogenic section of the circuit can stay the same. If $Z \approx \frac{1}{i\omega C}$, the situation is significantly different. First of all, Z is infinite in the DC limit, necessitating the application of an AC method. In a similar vein, the measurement frequency must be sufficiently high to prevent the current output I is proportional to ω

from being unreasonably tiny in relation to noise. However, the majority of current amplifiers encounter high input impedance above 10 kHz, which restricts the range of detectable currents to picoamperes for a source voltage of 1 mV and samples of 1 pF or less.

3.5.2 Capacitance Bridge

Using a capacitance bridge, which enables two voltage sources to balance an unknown capacitance against a known reference capacitor, is a significant advance. It is possible to determine a value for C_{ex} by using the relationship between the sources and capacitances when the output voltage at the balancing point is null. First, we will go through a very simple variation that merely balances two ideal capacitances. Finally, we'll include the complicating factor of resistive resistance. The fundamental plan is shown in Figure 3-7. The voltage source V_{ex} is applied to C_{ex}, the experimental capacitance, which is unknown, at a fixed frequency and amplitude. The standard capacitor C_{ref}, which has a known value, is subjected to a different voltage, V_{ref}, which has variable amplitude and phase. When balanced, V_{ref} is roughly 180 out of phase with V_{ex}. Since we are balancing two pure capacitances in this basic scheme, we never need to change the phase from 180°, but we shall employ the phase degree of freedom when we consider an experimental impedance Z_{ex} that contains a resistive component. In actuality, the two voltage sources are initially set to a certain value, the output of the bridge is measured at the balancing point, and V_{ref} is then modified till $\delta V_{out} = 0$.

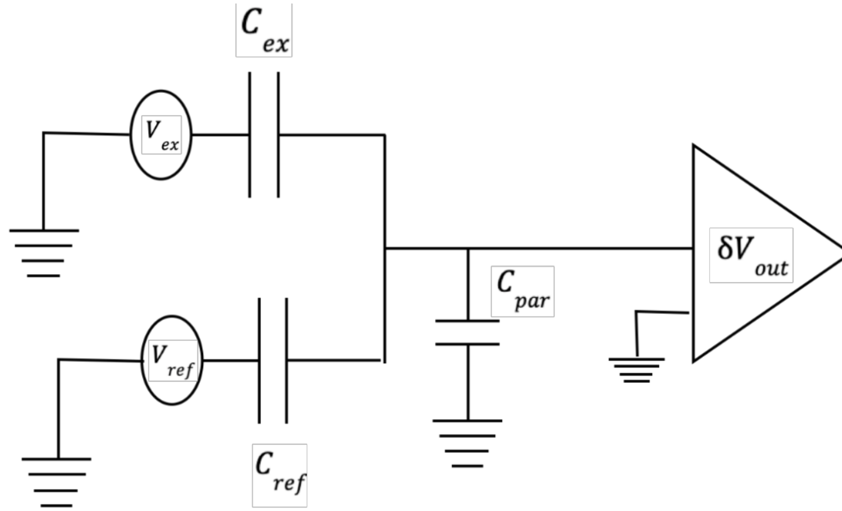

Figure 3.7: The fundamental capacitance bridge method balances an experimental capacitance C_{ex} against a standard capacitance C_{ref} using two voltage sources. The voltage V_{ex} is set to an excitation frequency and amplitude that are suitable for the sample. If there is resistive resistance present, the phase must also be slightly modified. The standard excitation is 180° out of phase and merely adjusted in amplitude. At the balance point of the bridge, the output signal δV_{out} is monitored with a shunting capacitance C_{par} caused by wiring, bond pads, wire bonding, etc.

The signal output and bridge's resolution are both decreased by the shunt capacitance that results from the cabling. Two capacitive voltage dividers are superposed to calculate the output at the balance:

$$\delta V_{out} = V_{ex} \frac{C_{ex}}{C_{ex}+C_{ref}+C_{par}} + V_{ref} \frac{C_{ref}}{C_{ex}+C_{ref}+C_{par}}$$

(3.23)

$$= \frac{V_{ex}C_{ex}+ V_{ref}C_{ref}}{C_{ex}+C_{ref}+C_{par}} \tag{3.24}$$

And balance is achieved when

$$\frac{C_{ref}}{C_{ex}} = -\frac{V_{ex}}{V_{ref}} \tag{3.25}$$

The experimental capacitance is given in units of the standard capacitance by the ratio of the source voltages, $-\frac{V_{ex}}{V_{ref}}$. This formula clearly states that for large parasitic capacitance, the magnitude of δV_{out} is divided by the total capacitance. Because the charge imbalance term $V_{ex}C_{ex} + V_{ref}C_{ref}$ will be muffled by C_{ref} and the balance will not be sensitive above noise, it may be challenging to get an accurate bridge balance for sufficiently large parasitics. Finding an appropriate balance at each location in phase space takes time in ordinary measurements. We often do an initial balancing to remove a significant amount of background capacitance and then measure off balance to identify modest relative changes in C_{ex} that result from gating, shifting magnetic fields, etc. if changes in the overall capacitance remain small.

We can next inquire: What voltage accumulates at the balancing point if $C_{ex} \rightarrow C_{ex} + \delta C_{ex}$ if we discover an optimal balance? To first in line

$$\delta V_{out} \approx \frac{\delta C\, V_{ex}}{C_{ex}+C_{ref}+C_{par}} \tag{3.26}$$

The shunting capacitance divides the signal in this instance as well. Thus, lowering the shunt capacitance C_{par} in front of the amplifier is equivalent to having good capacitance sensing. The capacitance for typical coaxial cable is 30 pF ft^{-1} from the core to the shield (ground). Long wires must extend all the way into the refrigerator for a cryogenic measurement and then return for a room-temperature measurement. The cable between the balance point and the measurement will be between 10 and 20 feet, resulting in a shunt of

about 500 pF. In the best case scenario, the signal will experience no noise beyond the intrinsic noise floor of the lock-in amplifier. Typical noise floors experienced with cryogenic bridge circuits are more like 50 nV/√Hz at the input of the lock-in, and below 10 kHz the noise is typically much worse arising from 1/f noise in the cryogenic amplifiers. long averaging times, as demonstrated in one work on carbon nanotubes for a constrained range of carrier density at zero magnetic field, can theoretically address some of these problems[113]. Long averaging periods become impractical, especially in the low frequency limit where $\frac{1}{f}$ noise is higher, if one attempts to sweep two parameters such as carrier density and magnetic field while taking tiny point spacing. Furthermore, even with very long averaging times, particularly low-frequency noise and DC drift could be challenging to average away. The requirement for lengthy cabling is the main obstacle to capacitance sensing in a cold environment. Due to the fact that the capacitance balancing point must start inside an isolated cryogenic area on one plate of the nanoscale capacitor, it is challenging to overcome this restriction whenever the primary stage of the measurement circuit is set at ambient temperature. The first stage amplifier should be positioned as close to the sample capacitor as is practical in the cryogenic area. By creating a significant resistance, this effectively decouples the balance point from the remainder of the measurement line. The work of Ashoori is where the concept originated [114] who first utilized a high electron

mobility transistor (HEMT) as a first stage "bridge on chip" amplifier at low temperature as shown in Figure 3-8. The operational point of the HEMT transistor is frequently chosen

to have a unit or even a subunit voltage gain. The slight loss of the HEMT at this operating point is more than offset by its ability to serve as an impedance bridge, which can lower the shunt capacitance from around 500 pF to less than 1 pF, this reduction in the shunt

capacitance increases our capacitance sensitivity. Two additional circuit components can be seen in the schematic. The DC operating point of the HEMT is set using the resistor R_{bias} and the DC voltage V_{bias}.

The HEMT drain-source voltage and current are controlled by R_{drain} and V_{drain}. At room temperature, it is possible to deduce that the voltage across the HEMT will change as the gate voltage is modulated. There is no problem with the huge capacitive cabling going to room temperature because the HEMT has a low output impedance of 500Ω. Further details of the cryogenic bridge amplifiers scheme can be found in Appendix B. For the rest of this section, we will assume we have some low-temperature bridge similar to Figure 3-9 which is capable of measuring capacitance with high resolution. In the following, we will discuss about the bridge's output and how it relates to the capacitive and resistive impedances of actual capacitive devices. At the conclusion of the chapter, we will explore data processing methods and relate the bridge output signal to relevant real physical parameters as compressibility, chemical potential, in-plane conductivity, and carrier density.

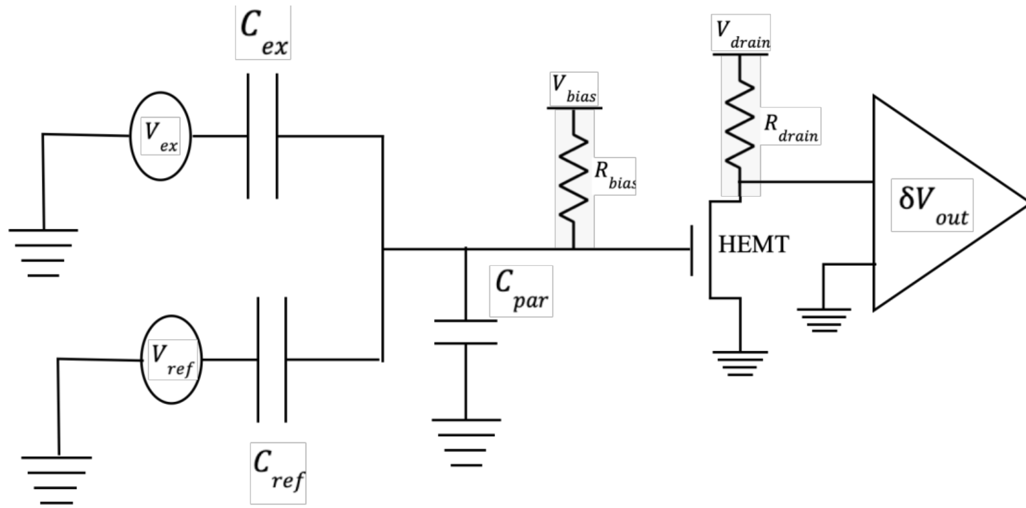

Figure 3.8: The capacitance bridge with HEMT amplifier is quite similar to the original bridge, but a low temperature high electron mobility transistor (HEMT) preempts the room temperature measurement and isolates the balance point from the extensive cabling to room temperature. Cpar's new value is 1 pF.

3.6 In and out of phase signals

3.6.1 Impedance of van der Waals capacitance

Since both sides of the bridge only had reactive impedances, we could more readily derive the balancing condition without phase rotations using the approximation that $Z_{ex} = \frac{1}{i\omega C_{ex}}$ in the preceding derivations. The in-plane resistance can be large in conventional van der Waals systems, though, at low temperatures and strong magnetic fields. In reality, interpreting capacitance data in terms of compressibility depends critically on the capacity to measure efficiently low in-plane resistance relative to the magnitude of the capacitive impedance. We require a practical, yet hopefully straightforward, model for the impedance of van der Waals capacitors with ohmically connected (with one plate constructed of

metal). This can be effectively captured to leading order by a resistance R connected in series with the capacitance C_T (which includes both the geometric and quantum capacitances). As a result of capacitive coupling between the bond pads, wire bonds, and additional metal attached to either side of the capacitance structure, there is also a stray background capacitance, or C_{back}. The initial balancing point effectively removes this, which appears as a steady addition to the total capacitance in measurement $C_{measurement}$ = C_T + C_{back}. However, when conducting a quantitative analysis of capacitance data, it is crucial to precisely subtraction this contribution which in subsection 3.4.4, accurate background subtraction will be covered. We should discuss a few additional sample impedance models before moving on to a circuit analysis. Contrary to our accepted lumped element model, the in-plane resistance and capacitance really form a distributed RC network. Some of the frequency response curves presented below undergo a numeric shape change due to the distributed model, while the qualitative behavior remains unchanged. In particular, both models converge at low frequencies. (See Appendix E of Gary Steele's thesis for details 115. We could also be concerned about a leakage resistance R dielectric, which would seem like a parallel resistance to the sample capacitance C_T, but in reality, this resistance is so great that it can be ignored because it is effectively infinite.

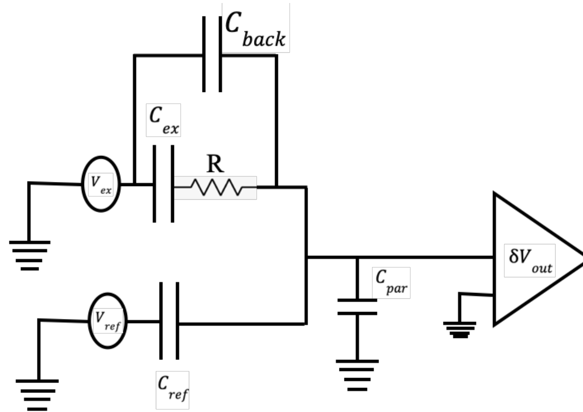

Figure 3.9: An effective model for the sample impedance consists of an in-plane resistance R in series with the total capacitance C_T. Additionally, stray capacitance C_{back} from coupling between bond pads, wire bonds, etc. adds a constant background on the measurement signal

The efficient measurement circuit that we want to examine is shown in Figure 3-9. To calculate the off-balance signal to leading order in response to minute changes in C_T and R, we shall first determine the balance situation. The total sample impedance Z_{ex} is given by summing the three impedances:

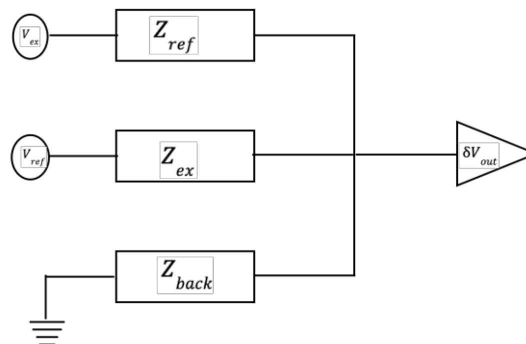

Figure 3.10: Sample impedance model

$$Z_{ex} = \frac{\frac{1}{i\omega c_{back}} * (\frac{1}{i\omega c_{ex}} + R)}{\frac{1}{i\omega c_{back}} + \frac{1}{i\omega c_{ex}} + R} = \frac{\frac{1}{i\omega c_{back}} * (1 + i\omega C_{ex}R)}{\frac{C_{ex}}{c_{back}} * (1 + i\omega C_{ex}R)} \tag{3.27}$$

Similarly, the impedances of the standard capacitor and parasitic capacitance are

$$Z_{ref} = \frac{1}{i\omega C_{ref}} \tag{3.28}$$

And

$$Z_{back} = \frac{1}{i\omega C_{back}} \tag{3.29}$$

If the amplifier at the balance point has a total amplification G, then the output voltage is given by superposition:

$$V_{out} = G(V_{ex} \frac{Z_{ref} \,||\, Z_{back}}{Z_{ex} + Z_{ref} \,||\, Z_{back}} + V_{ref} \frac{Z_{ex} \,||\, Z_{back}}{Z_{ref} + Z_{ex} \,||\, Z_{back}})$$

$$= G(V_{ex} \frac{\frac{Z_{ref} * Z_{back}}{Z_{ref} + Z_{back}}}{Z_{ex} + \frac{Z_{ref} * Z_{back}}{Z_{ref} + Z_{back}}} + V_{ref} \frac{\frac{Z_{ex} * Z_{back}}{Z_{ex} + Z_{back}}}{Z_{ref} + \frac{Z_{ex} * Z_{back}}{Z_{ex} + Z_{back}}})$$

$$= G(V_{ex} \frac{\frac{Z_{ref} * Z_{back}}{Z_{ref} + Z_{back}}}{Z_{ex} + \frac{Z_{ref} * Z_{back}}{Z_{ref} + Z_{back}}} + V_{ref} \frac{\frac{Z_{ex} * Z_{back}}{Z_{ex} + Z_{back}}}{Z_{ref} + \frac{Z_{ex} * Z_{back}}{Z_{ex} + Z_{back}}})$$

$$V_{out} = G(\frac{Z_{back}(V_{ex} * Z_{ref} + V_{ref} * Z_{ex})}{Z_{back}(Z_{ex} + Z_{ref}) + Z_{ref} * Z_{ec}}) \tag{3.30}$$

The balance condition is achieved when

$$V_{out} = 0 \Rightarrow \frac{Z_{ref}}{Z_{ex}} = -\frac{V_{ref}}{V_{ex}}. \tag{3.31}$$

In the limit $C_{back} \to 0$ and $R \to 0$ this reduces to Equation 3.25. Z_{ex} has impedances that are both reactive and resistive, hence the voltage V_{ref} must have a nonzero phase. We can solve for the real and imaginary parts of $\frac{V_{ref}}{V_{ex}}$which we will label X and Y, respectively:

$$X = -\frac{\frac{(C_{ex}+C_{back})}{C_{ref}}}{1+(R\omega C_{ex})^2} - \frac{\frac{C_{back}(R\omega C_{ex})^2}{C_{ref}}}{1+(R\omega C_{ex})^2} \tag{3.32}$$

$$Y = \frac{\frac{R\omega {C_{ex}}^2}{C_{ref}}}{1+(R\omega C_{ex})^2} \tag{3.33}$$

Let's have a look at the low frequency restriction defined by $R\omega C_{ex} \ll 1$. Where $\tau = RC_{ex}$, we can extend to leading order in powers of $\omega\tau$:

$$X = -\frac{(C_{ex}+C_{back})}{C_{ref}}(1-(\omega\tau)^2) + \alpha(\omega\tau)^3 \tag{3.34}$$

$$Y = \frac{C_{ex}\omega\tau}{C_{ref}}(1-(\omega\tau)^2) + \beta(\omega\tau)^4 \tag{3.35}$$

These statements have a very obvious physical meaning. The resistance R is insignificant because it cannot outperform the impedance $\frac{1}{i\omega C_{ex}}$ at low frequencies. The entire capacitive term in Z_{ex}, expressed in units of the common capacitor, constitutes the inphase component. The fact that the in-phase signal primarily specifies the capacitive impedance may seem counterintuitive. This is true because there is no net phase shift with regard to the excitation at the balancing point in the low frequency limit (where R is minimal). Furthermore, if we were to measure impedance using a resistive impedance as Z_{ref}, this

would essentially modify the "units" that we use to measure impedance and would result in the capacitance showing up in the out-of-phase component. Importantly, we can observe that the background capacitance simply arises as a constant additive term if we consider variable C_{ex}. Due to the presence of both reactive and resistive components, the out-of-phase component is a little more complicated. Although expressed in units and a shape that typically do not permit direct access to any well-defined resistivity elements such as ρ_{xx} or ρ_{xy}, it effectively monitors the bulk transport behavior of the sample because it is exactly proportional to the in-plane resistance of the sample.

Now let us consider the high frequency limit. At high frequency $R\omega C_{ex} \gg 1$ and

$$X \approx -\frac{C_{back}}{C_{ref}} - \frac{\frac{(C_{ex}+C_{back})}{C_{ref}}}{(R\omega C_{ex})^2} \tag{3.36}$$

$$Y \approx \frac{1}{R\omega C_{ref}} \tag{3.37}$$

The capacitance of the sample needs a time of several t = RCT in order to completely charge. The sample fails to fully charge in the high frequency limit, and the background capacitance C_{back} shunted the sample's series resistance and capacitance. Regarding the out-of-phase component, there are no other resistive components that are not at high frequency suppressed by the sample's inability to charge. As a result, Y decreases evenly with time as $\frac{1}{R\omega C_{ex}}$, which can be thought of as the bulk conductivity $\frac{1}{R}$ measured in ωC_{ref} units. We can interpolate the two bounds at intermediate frequencies. The way that X behaves is fairly obvious. As frequency rises, the sample gradually stops charging, killing its contribution to the charging signal at the balance. From a value of C_{ex} + C_{back} to C_{back} in units of the reference, it declines monotonically. It is difficult to directly infer the whole

expression for Y in Equation 3.35; nevertheless, it is possible to apply the heuristic that Y reflects the unitless rivalry between resistive and reactive impedances. When the two impedances are similar, there is intense competition; but, when one prevails, there is intense suppression. At extremely low frequency, the impedance of the capacitance is much larger and dominates. Y ≈ 0 and increases linearly with $\omega\tau$. Due to the sample's inability to charge, the resistive component predominates at very high frequencies, and $Y \approx 0$ and falls off as $\frac{1}{\omega\tau}$. The out-of-phase signal peaks at some intermediate regime when $R = \frac{1}{\omega C_{ex}}$. By doing so, It turns out that the background subtracted ratio is equal to the loss tangent tan(δ) of the sample, which is defined as the ratio of the resistive to reactive impedances.

$$tan(\delta) = loss\ tangen = \frac{Z_{res}}{Z_{react}} \tag{3.38}$$

The quantity known as the loss tangent is frequently used to illustrate how far a capacitor deviates from its ideal capacitance. Due to parasitic resistances and the dielectric's lossy relaxation, all capacitances have a series resistance. The effective series resistance of a capacitor serves as the numerator of the loss tangent (commonly ESR in data sheets). In order to calculate this quantity for the sample Z_{ex} we must first background subtract the C_{back}contribution.

3.6.2 Off-Balance Measurements

Feedback software can adjust the magnitude and phase of V_{ref} to identify the circumstance where V_{out} = 0 in order to measure capacitances with a bridge method. At every gate voltage, magnetic field, or other independent parameter, the bridge must be rebalanced. In

spite of the fact that the total changes to the capacitance that we are interested in are frequently fairly minor, this results in lengthy measuring times. In this regime, it is possible to use a linearized off-balance signal to back out the relative changes dX and dY. For some combinations of independent variables, such carrier density and magnetic field, we can discover an initial equilibrium. Then, we can ask: What voltage accumulates at the balance point in response to changes $C_T \rightarrow C_T + \delta C$ and R → R + δR from sweeping one of the independent parameters?

Let's say G is the overall gain of our amplifier. Assume that V_{ref}^0 represents the initial balance voltage when $\delta C = 0$ and $\delta R = 0$. By expanding equation 3.30 to linear order in dC and dR we get:

$$\delta V = G \frac{V_{ex}(\delta C - i\delta R\omega C_T^2)}{(1+i\omega\tau)(C_\Sigma + i(C_\Sigma - C_T)\omega\tau)}$$

(3.39)

Here, $C_\Sigma = C_T + C_{ref} + C_{back} + C_{par}$. This expression can be cleaned up significantly with one other measurement. We can purposefully throw the bridge out of balance by letting $V_{ref}^0 \rightarrow V_{ref}^0 + \delta V_{ref}$ while the bridge is balanced, $\delta C = 0$ and dR = 0. The bridge's result will be

$$\alpha = \frac{\delta V_{out}}{\delta V_{ref}} = G \frac{C_{ref}(1+i\omega\tau)}{C_\Sigma + i(C_\Sigma - C_{ec})\omega\tau} \tag{3.40}$$

Where α is a bridge response function. By multiply equation (3.39) with $\frac{1}{\alpha}$ we can get

$\frac{\delta V}{\delta V_{ex}} = G\,\frac{\delta C - i\delta R C_T^2 \omega}{C_{ref}(1-i\omega\tau)^2}$ that isolating the in- and out-of-phase components we get in the low-frequency limit:

$$\left(\frac{\delta V}{\alpha \delta V_{ex}}\right)_X = \frac{\delta C}{C_{ref}} \tag{3.41}$$

$$\left(\frac{\delta V}{\alpha \delta V_{ex}}\right)_Y = -\frac{\left(\frac{\delta R}{R} C_T + 2\delta C\right)\omega\tau}{C_{ref}} \tag{3.42}$$

In the balanced situation with $C_{ex} \rightarrow \delta C$ and no background capacitance, the first expression matches X. In the limit that the first term in the numerator proportional to dR dominates, the second expression fits Y with R→ δR. Note that the ratio between the two expressions is proportional to the fractional change: $\frac{\frac{\delta R}{R}}{\frac{\delta C}{C_{ex}}}$. Typically, increases in resistance go hand in hand with decreases in capacitance. Because the geometric term often dominates the total capacitance, the change in total capacitance is typically the smaller of the two. If there are numerous localized states within a gap that prevent the quantum capacitance from reaching zero, the fall in the total capacitance may also be just marginally noticeable. But because the resistance is so sensitive to the number of extended states accessible, it might possibly rise much more sharply whenever a gap is crossed. In either instance, the Y-function component's is never quantitative; rather, it just serves to confirm that variations in the X-component are linked to actual modifications of the quantum capacitance δC_q and not to increases in R connected to the numerator of Equation $\frac{\delta V}{\delta V_{ex}} = G\,\frac{\delta C - i\delta R C_T^2 \omega}{C_{ref}(1-i\omega\tau)^2}$. In the low-frequency limit, the X-component, which is frequently utilized quantitatively, continues to be well approximated as solely capacitive. Given the possible significance of

the in-plane conductivity, the question of whether capacitance is a valid indicator of the density of states was first raised in [107]. Since the exact value of R is seldom known in practice, it is assumed that the low frequency limit is reached anytime the off-balance Y term stays zero or varies just slightly while a significant change in X takes place. In this situation, the modulation of X may be attributed to the quantum capacitance (density of states). It is difficult, if not impossible, to be quantitative about the changes in compressibility if Y changes significantly, which typically happens in significant band gaps and at high magnetic fields in the quantum Hall regime where the in-plane conductivity can become very low in cyclotron or exchange gaps. In this way, capacitance can be separated into roughly two limits. At low frequency, changes in X are attributed to changes in $C_q = \frac{\delta n}{\delta \mu}$. At high frequency, X is no longer directly proportional to the compressibility. When a significant background impedance is removed from a bridge measurement, tiny changes can be seen. The resistance that is felt is also genuine bulk spreading resistance. In the quantum Hall domain, where conventional two- and four-probe geometries are unable to measure the bulk conductivity because they are shorted out by the extended edge states, this can be a crucial quantity to measure. For instance, was able to assert the existence of a quantum-spin-Hall-like phase in monolayer graphene at high magnetic field by observing insulating bulk with capacitance sensing[116].

3.6.3 Background Subtraction

The background capacitance must be able to be subtracted from the measured signal at low frequency, as was previously described. Making measurements at both the low- and high-

frequency limits is one way to address this. At high frequency the in-phase component is $X \approx -\frac{C_{back}}{C_{ref}}$ and at low frequency it is $X \approx -\frac{(C_{ex}+C_{back})}{C_{ref}}$, taking the difference removes the background. For all samples, this is not always achievable, especially for little samples moderate in-plane resistance of 100 fF. Depending on the measurement lines used, the roll off frequency at 1 MΩ will be in the MHz regime, which may or may not be accessible. For samples with a quantifiable quantum Hall effect regime and low in-plane resistance, there is an alternative method. No matter the host substance, in the quantum Hall regime, each Landau level's orbital degeneracy is given by

$$\frac{\Phi}{\Phi_0} = g\frac{BAe}{h} \tag{3.39}$$

where Φ is the total flux at field B through sample of lateral area A and Φ_0 is the flux quantum. There may be additional degeneracy arising from spin, valley, etc. which we will label g. As a result, $g\frac{BAe}{h}$ represents the total number of states present in each Landau level. We may determine the proper $C_0 = C_{back}$ to remove off if we integrate the entire capacitance (in-phase signal) between two Landau level minima at low frequency by applying:

$$g\frac{BAe^2}{h} = \int_{\Delta V} \quad (C_T(V) - C_0)\mathrm{dV} \tag{3.40}$$

where DV is a voltage range determined from the field and gate dependence of the capacitance data.

3.6.4 Carrier Density

Typically, gate voltage is used as the "fast" independent variable while measuring capacitance data. For samples where the geometric capacitance predominates, the relationship between gate voltage and carrier density is roughly linear. However, using capacitance data, it is possible to precisely calculate the density by integrating the entire capacitance:

$$n = \int_{V_0}^{V} \frac{(C_T(V') - C_{back})}{eA} \mathrm{d}V' \tag{3.41}$$

where V_0 represents the voltage associated with charge neutrality (or depletion).

3.6.5 Geometric capacitance

The geometric capacitance is a quantity that is challenging to measure and frequently needs to be estimated. The fact that the two are entangled with C_q, which is never known a priori, prevents there from generally being a relationship that allows one to perfectly extract C_{geo} from C_T. A method for predicting C_{geo} will be covered in Chapter 4.

3.6.6 Chemical potential

One can calculate the change in the chemical potential μ by subtracting an estimate for the C_{geo} and C_T background and expressing the result in terms of density. Since we know that $\frac{\delta\mu}{\delta n} = Ae^2(\frac{1}{C_T} - \frac{1}{C_{geo}})$, by integrating with respect to density we can get:

$$\Delta\mu(n) = \int_{n_0}^{n} Ae^2\left(\frac{1}{C_T} - \frac{1}{C_{geo}}\right) \mathrm{dn}.$$

As long as the overall out-of-phase component is sufficiently tiny across the entire range of carrier density, it is possible to determine gaps and the bandwidth of energy bands by measuring the change in chemical potential. Chapter 4 will give an illustration on WTe2 samples.

Chapter 4: Electronic Compressibility of WTe2

4.1 Introduction

Quantum spin Hall (QSH) materials are 2D systems exhibiting insulating bulk and helical edge states simultaneously. A QSH insulator processes topologically non-trivial edge states protected by time-reversal symmetry, so that electrons can propagate unscattered. Recently, a family of transition metal dichalcogenides (TMDC), monolayer 1T′-MX2 (M = Mo, W, X = S, Se, Te), were predicted to be QSH materials, based on density-functional theory calculations [73]. The monolayer WTe2 has the 1T′ structure its bands are spin degenerate due to inversion symmetry and, near the Fermi energy E_f, there is a valence (v) band maximum at Γ flanked by two conduction (c) band minima located at k_x = ± kΛ. Monolayer 1T′-WTe2 was predicted to be semimetallic QSH materials, though with a negative band gap [73]. The quasiparticle spectrum generated using a hybrid functional method directly demonstrates that the monolayer 1T′- WTe2 QSH gap is positive. Also, some tunneling spectroscopy measurements [84], angle-resolved photoemission [84,117] and density functional theory (DFT) calculations [118,119] point to a positive bandgap, Eg, of the order of 50 meV. However, the nature of this bulk gap is unclear. Recent measurements suggest it may be an excitonic insulator [91,120]. In their study they showed that this bulk state has a very unusual nature, containing quasiparticles of electrons and holes bound by Coulomb attraction – excitons – that spontaneously form in thermal equilibrium.

To investigate and study more about the nature of this bulk gap, we used capacitance measurements, and combine scanning microwave impedance microscopy (MIM), and Kelvin probe force microscopy (KPFM), on monolayer WTe2 devices. MIM probes the local conductivity; KPFM measures the local chemical potential, and quantum capacitance is associated with the electronic density of states. We measure these quantities as a function of carrier density, magnetic field, and temperature. In this chapter by correlating these measurements, we will discuss their implications on the bulk electronic structure in monolayer WTe2.

4.2 Capacitance Measurement Scheme

In order to probe and study the ground state of monolayer WTe2, we use a low-temperature capacitance bridge to access the electronic compressibility of the several devices originally characterized with microwave impedance microscopy. By measuring the compressibility as a function of carrier density, we study the evolution of the gap inside monolayer WTe2. Figure 4-1 shows the device geometry and measurement schematic. Monolayer WTe2 samples were fabricated by using dry transfer technique inside the glovebox as described previously in chapter 2. The monolayer WTe2 is encapsulated between two layers of hexagonal boron nitride (hBN) and placed on top of a local, metal back gates, with top and bottom graphite gate. Also, in order to initiate the transport measurements, we made the Hall geometry for electrodes. However, in our capacitance measurements, we electrically

short all contacts together to reduce the RC charging time of the devices, allowing the measurements to take place at higher frequency where the signal-to-noise ratio is improved.

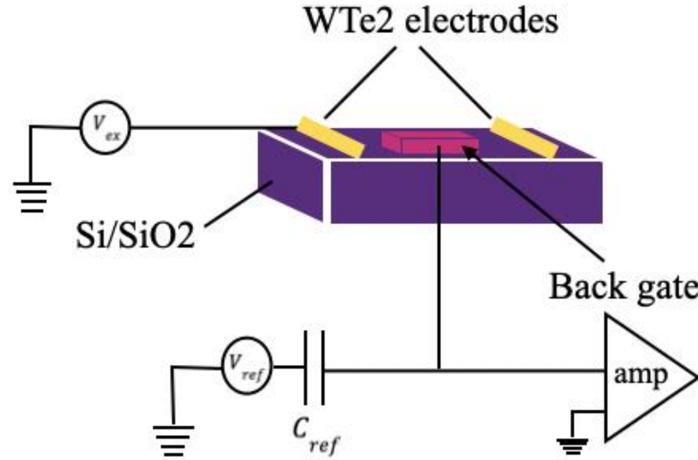

Figure 4.1: Schematic of monolayer capacitance devices. Here, we tie together all electrical leads to reduce the in-plane spreading resistance. Devices are measured on a cryogenic capacitance bridge in cryostat.

We apply an AC excitation to the monolayer WTe2 contacts and a balancing AC excitation of variable phase and amplitude to a $\sim$ 0.2 pF reference capacitor connected to the back gate in a bridge configuration as shown in Figure 4-1. We measure small changes in the sample impedance by monitoring off-balance voltage accumulation at the balance point, and we model the total capacitance C_T of the monolayer WTe2 structure as consisting of two contributions: $C_T^{-1} = C_{geo}^{-1} + C_q^{-1}$, C_{geo}^{-1} is the geometric capacitance arising from the parallel plate geometry of the monolayer WTe2 and local graphite back gate while $C_{geo} = Ae^2 \frac{\delta n}{\delta \mu}$ is the quantum capacitanc which is directly proportional to the

thermodynamic compressibility $\frac{\delta n}{\delta \mu}$ (A is the lateral device area and e is the elementary charge). By measuring modulation of the capacitance as a function of gate voltage and magnetic field, we detect the presence of a gap in the density of states. Importantly, we limit our measurements to low enough frequencies to make sure that the recorded signal's modulation results solely from changes in the electrical compressibility and not from charging-rate effects from slow in-plane transit, which are covered in Chapter 3 of this thesis.

4.3 Capacitance Data

From equation 3.30, we got the relation between V_{out} and total capacitance and sample resistivity. Unfortunately, we cannot directly measure the C_{ref}, and our presenting data is based on C_{ref}. From our calculation, by considering our balance bridge at a condition where R_{sample} is small, at high gate voltage we can get the relation between in_phase and out_phase signal to $R_{sample}\omega C_{total}$, and $\frac{C_{total}}{C_{ref}}$.

$$V_{out} \quad (in\,phase) = (gain)\frac{(\frac{C_{tot}}{C_{ref}}V_{sample}+V_{ref})(1+\frac{C_{tot}}{C_{ref}})+(\frac{C_{tot}}{C_{ref}})^2(R\omega C_{ref})^2 V_{ref}}{(1+\frac{C_{tot}}{C_{ref}})^2+(R\omega C_{ref})^2(\frac{C_{tot}}{C_{ref}})^2} \tag{4.1}$$

$$V_{out} \quad (out\,phase) = (gain)\frac{(\frac{C_{tot}}{C_{ref}})^2(R\omega C_{ref})^2}{(1+\frac{C_{tot}}{C_{ref}})^2+(R\omega C_{ref})^2(\frac{C_{tot}}{C_{ref}})^2} \tag{4.2}$$

Panels (a) and (b) of Figure 4-2 show total capacitance and resistivity measurements at zero magnetic field at 2K for the monolayer device with back gate.

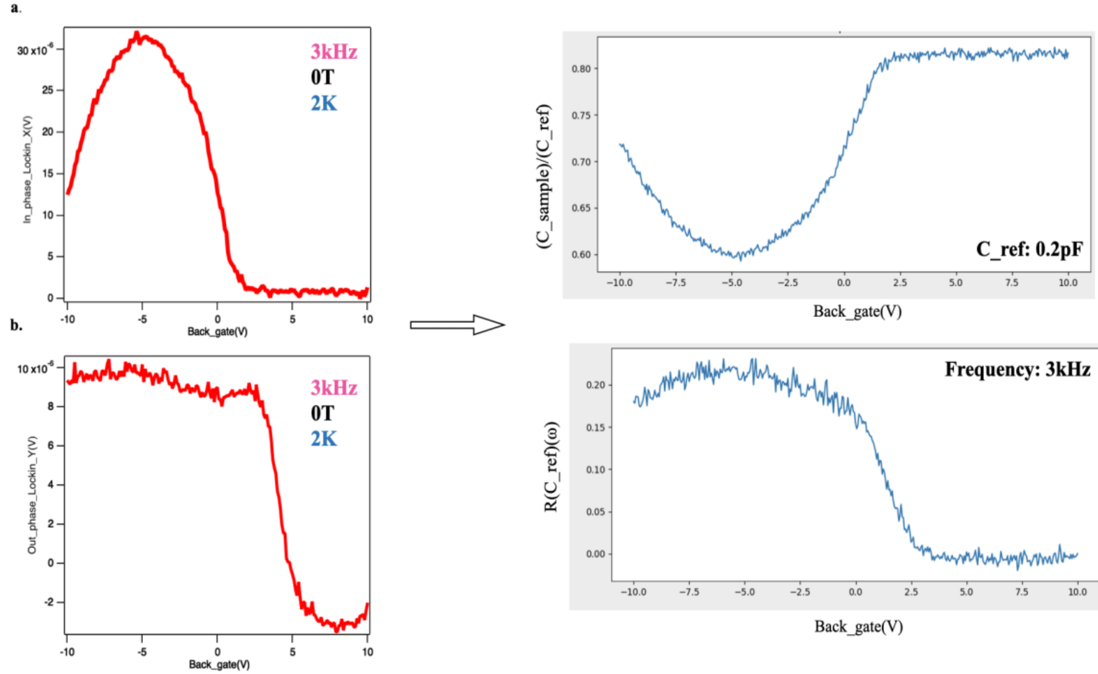

Figure 4.2: Extraction of capacitance data for the monolayer device at 2K, with B= 0T, and frequency at 3kHz by considering C_{ref}= 0.2pF.

From data here, at high positive back gate voltage ~10V as we expected sample resistivity goes to zero and capacitance data which is $C_T^{-1} = C_{geo}^{-1} + C_q^{-1}$ has maximum signal.

At $V_{gate} = 2.5V$ and below that we reached at the minimum of the conduction band and going to the band gap, which resistivity increased, and quantum capacitance decreased while geometry one is constant. As we are lowering the back gate fermi energy passed the band gap and reaching to the max the valance point. Then, total capacitance, due to the quantum capacitance is going to increase and sample resistivity will decrease.

Unfortunately, based on the bottom BN thickness we have limitation for applying the V_{gate}. We chose 3kHz frequency, since we could get reasonable signal noise ratio. We perform the same measurement on different monolayer devices, and we got the consistent data. To measure the quantum capacitance, we can subtract the geometric capacitance from total one. Geometric capacitance is a constant number, and we can estimate it based on the BN thickness, and effective area. Also, while we are inside the band gap, Density of state decrease inside the gap, the quantum capacitance is close to zero and we can get the geometric capacitance. By knowing the geometric capacitance, and total capacitance we can get the quantum capacitance.

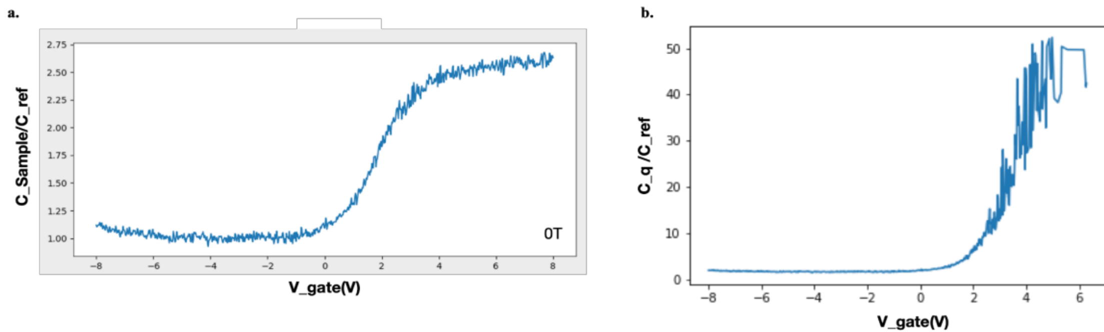

Figure 4.3: Extraction of quantum capacitance data for the monolayer device at 2K, with B= 0T, and frequency at 3kHz from total capacitance data, C_{ref}= 0.2pF.

4.4 Field dependence Capacitance Data

We also measure the evolution of the compressibility with magnetic field.In panel a of Figure 4-4 we plot the capacitance as a function of gate voltage and magnetic field. As we expected there is no big change in higher positive gate voltage which consistent that edge

signal doesn't dependent to magnetic field and field dependance is mostly related to bulk behavior which is related to lower back gate $V_{gate} < 2.5V$ [89] .

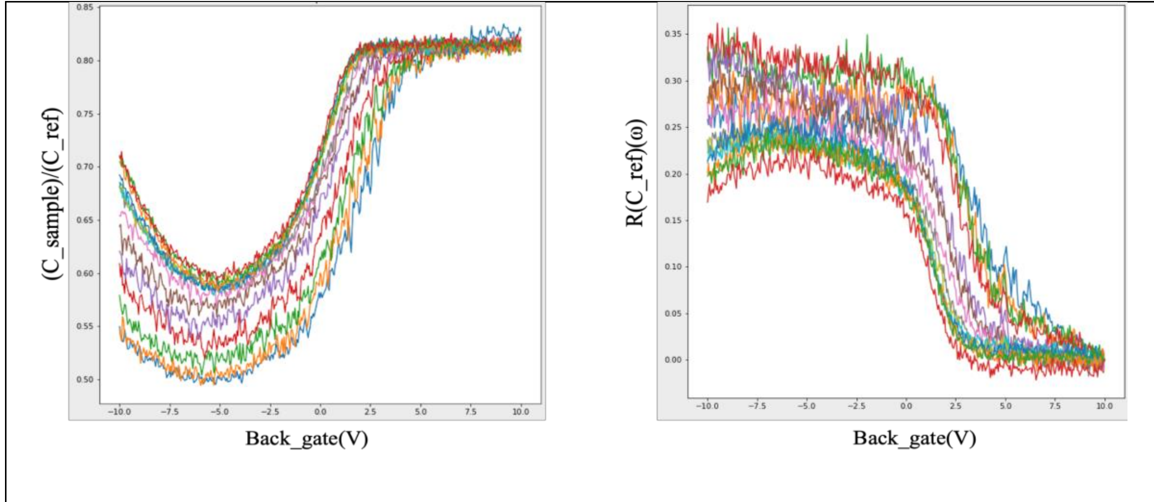

Figure 4.4: The field-dependence of the capacitance data of the monolayer WTe2 device at 2k, with frequency= 3kHz.

4.5 Frequency Dependance

To determine the capacitance circuit's frequency response, the earlier calculations were crucial. The frequency is crucial to comprehending the bridge response since it naturally affects the impedance of a capacitor, which is what we ultimately want to measure. To feel relative changes in the total capacitance, independent factors like density (gate voltage) or magnetic field are modulated while the capacitance bridge is locked to a working measurement frequency, or f_0. It is important to consider what will happen to the signal if C_T and R are changed by a gate voltage change. Imagine that at zero gate voltage V = 0 the total capacitance is 10 pF and the resistance is 100 kΩ. Then as we change the voltage to V = 1 V the capacitance enters the edge of a band gap. The total capacitance decreases to

9 pF and the resistance increases to 500 kΩ. At V = 2 V, the sample enters the band gap completely and the total capacitance further reduces to 8 pF while the resistance blows up the 50 GΩ. These changes cause the roll off frequency to decrease. Even in the band gap, the sample's density of states may be substantial due to localized states which cause $C_q \neq 0$. Therefore, the total capacitance may only deviate slightly from the geometric value C_{geo}, particularly in the limit $C_{geo} \ll C_q$. The in-plane resistance, however, is highly sensitive to the absence of extended electronic states. Because R changes much more dramatically than C_{ex} typically, it pulls the rolloff frequency to the left more than the decrease in C_{ex} pulls it to the right. If we were to plot the values of X(V) and Y(V), we would see a steady drop in X as well as a single peak in Y. The lowest frequency f = 57 Hz is close to the low frequency limit because at all values of V, the change in Y is small in comparison to the changes in X. The middle frequency f = 1 kHz is not in the low frequency limit. The change in X which is measured is not truly associated with pure capacitance change. Y will show a double-peak structure if the gate voltage pushes through the band gap and enters another highly compressible band. The highest measurement frequency f = 100 kHz is close to the high-frequency limit in this measurement setup. The value of the capacitance is not properly measured at any gate voltage V and Y shows a dip as the band gap is entered.

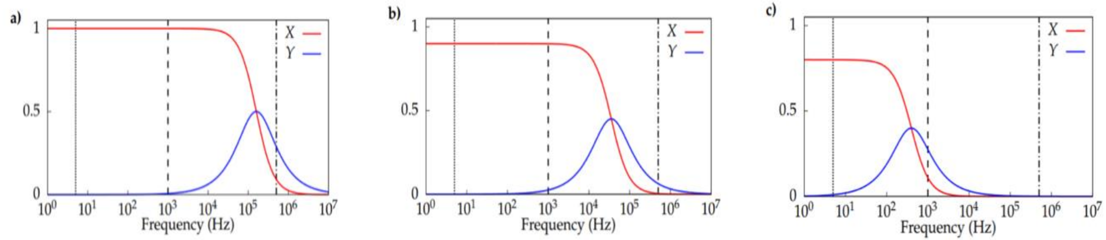

Figure 4.5: (picture taken from [121]) The in-phase and out-of-phase curves shift as the sample becomes increasingly resistive. The measurement takes place at any one of the black dotted/dashed traces. a) At V = 0 the sample has CT = 10 pF and R = 100 kW. b) At V = 1 V the sample is at the edge of a band gap. CT = 9 pF and R = 500 kW. c) At V = 2 V the sample enters a full band gap. CT = 8 pF and R = 50 GW. The frequency 5 Hz (dotted trace) is near the low-frequency limit whereas the frequency 500 kHz (dot-dashed trace) is near the high-frequency limit. The frequency 1 kHz (dashed trace) is intermediate.

From our calculation in chapter 3 we showed that at lower frequency sample resistivity which is in series with sample total capacity close to zero and we have a chance to get the total capacity. But at lower frequency unfortunately the signal ratio is smaller, and we have noise problem. So, in our same set up as above we checked different frequency and show the data in figure 4-6.

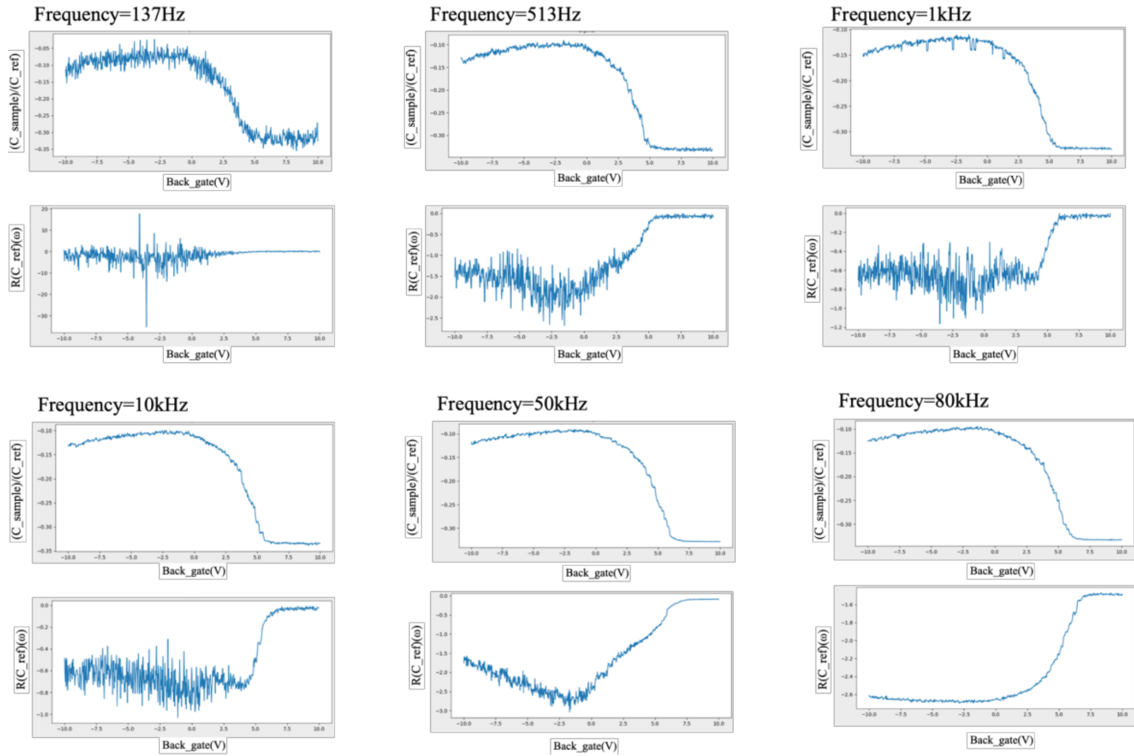

Figure 4.6: Frequency measurement at 2K with B = 0T of monolayer WTe2 with bulk WTe2 gate device (a) Frequency=137Hz, (b) Frequency=513Hz, (C) Frequency=1kHz, (d) Frequency=10kHz, (e) Frequency=50kHz, and (f) Frequency=80kHz respectively.

From the plot we can see the how the sample resistivity is increasing by increasing the frequency while at higher frequency we faced less noise. At higher positive gate voltage, while total capacity is at maximum, resistivity reached to zero.

4.6 Capacitance at Higher Temperature

We also checked temperature sweep for different frequency here, although we expected to get closing of the gap around 100K, here after 30K we cannot get the actual signal, however, gain of the transistor doesn’t change a lot with temperature. We tried different

solutions like, replacing R_{bias} with another HEMT transistor, using different kind of C_{ref}, and using different $R_{bias}$with various numbers and material. However, still we can not solve the problem and our new idea is due to increasing the C_{Par} in our board. Since by increasing the C_{Par} we can detect the small signal. We calculated the C_{Par} from equation 4.4.

$$V_{out} = (gain)\, V_{ac} \tag{4.3}$$

$$V_{out} = (gain) \frac{V_{sample}C_{total} + V_{ref}C_{ref}}{C_{total} + C_{ref} + C_{par}} \tag{4.4}$$

So here in figure 4-7, we the plot gain vs temperature which gain of the transistor is not changing by applying magnetic field, different frequency or different temperature.

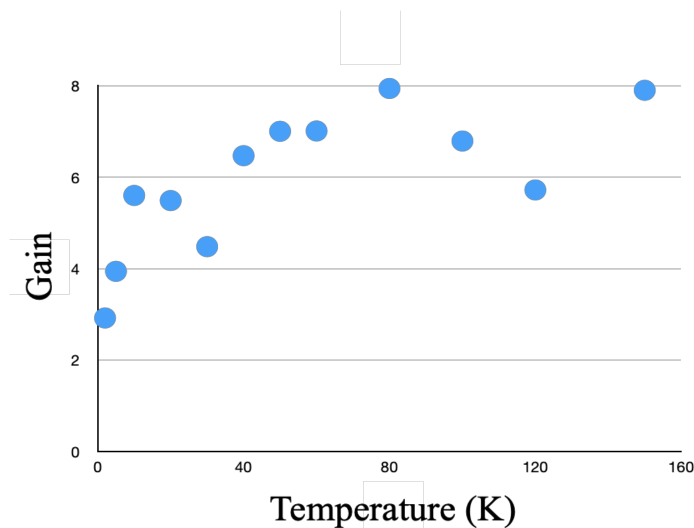

Figure 4.7: Showing the Gain vs Temperature at zero magnetic field.

4.7 Scanning Microwave Impedance Microscopy

Microwaves are electromagnetic radiation with wavelengths between 1 mm and 1 m and frequencies between 300 MHz and 300 GHz. When compared to optical excitations, the photon energy for a microwave range from 1.24 ueV to 1.24 meV, which is very low. Therefore, the way that microwave radiation interacts with materials is more like a classical process. The complex permittivity is what distinguishes a material's electric response to external ac fields:

$$\varepsilon = \varepsilon' + i(\varepsilon'' + \frac{\sigma}{\omega}) \tag{4.5}$$

Where ε' and ε'' are the real and imaginary parts of the dielectric constant, σ is the conductivity and $\omega = 2\pi f$ is the angular frequency. In MIM, a microwave voltage is applied to move a pointed metallic tip close to the surface of the sample. Local currents (on the nanoscale) may flow under the tip in the sample as a result of periodic dielectric polarization caused by an ac coupling between the tip and sample. The tip-sample admittance (specified as Y = 1/Z, the inverse of impedance) determines the displacement current with a magnitude and phase. Local information about the material, like as its conductivity and dielectricity, can be obtained from an ac measurement of the tip-sample admittance. When achieving a low tip-sample contact resistance is difficult (Schottky barrier at the contact location) or impossible (protective insulating layer on top of sample surface), this is especially helpful because a direct resistance measurement (current against voltage) is not accessible. A common tip size for a scanning MIM measurement is about

100 nm, which is orders of magnitude smaller than the microwave wavelength. The tip-sample admittance can be described by a lump-element in the microwave near-field domain (in the quasi-static limit), where the imaginary component (capacitance C) and the real part (1/R) depend on the sample electric characteristics. Particularly, the ratios of C and 1/R to ε' and σ, respectively When the imaginary and real admittance are comparable, the ideal frequency is established in usual measurements:

$$\omega C \approx \frac{1}{R} \rightarrow \omega\varepsilon' \approx \sigma \tag{4.6}$$

The ideal measuring frequency falls between the microwave frequency range of 0.1 to 10 GHz for materials with a typical resistivity $(\frac{1}{\sigma})$ ranging from 10 to $10^5 \Omega.cm$ and $\varepsilon' \sim 1 - 10\varepsilon_0$. According to the equation above, a greater frequency should be employed to measure the conductivity of a bigger sample[122].

Here, we directly map the local conductivity of monolayer WTe2 devices using microwave impedance microscopy (MIM) [123,124]. The electrical and geometrical nature of the gapless conduction that we see localized to the sample edges is compatible with the QSH effect. Additionally, MIM discloses additional significant characteristics of this system's conduction qualities that could not be inferred from transport, giving critical information for designing devices and opening up chances to access and manipulate helical edge channels.

We first show edge conduction in a sample configuration that contains prefabricated electrodes and a monolayer WTe2 flake exfoliated onto a graphite gate. (For further

information, see to chapter 2) and directly covered with a bigger hexagonal boron nitride (hBN) flake. An optical image is shown in figure 4-7. b, and figure 4-7.d displays MIM-Im measurements of the locations indicated in Figure 4-7.b, taken at 8 K in temperature and B=0T in magnetic field. The MIM-Im signal over the substrate and inside the flake are similar, indicating a highly insulating condition. We notice a number of small, brilliant lines piercing the interior that don't correlate to any optically discernible features. These seem as single lines, albeit thicker and brighter than the line that follows the outer border, and are probably certainly caused by minuscule tears that are so small that the two opposing edges of each tear cannot be resolved. These observations clearly demonstrate that edge conductance exists in monolayer WTe2. We also did an atomic force microscopy (AFM) in figure 4-7.c to measure the thickness of the flake, Line cut along the black dashed line in (b) matches the monolayer thickness, ~0.7nm.

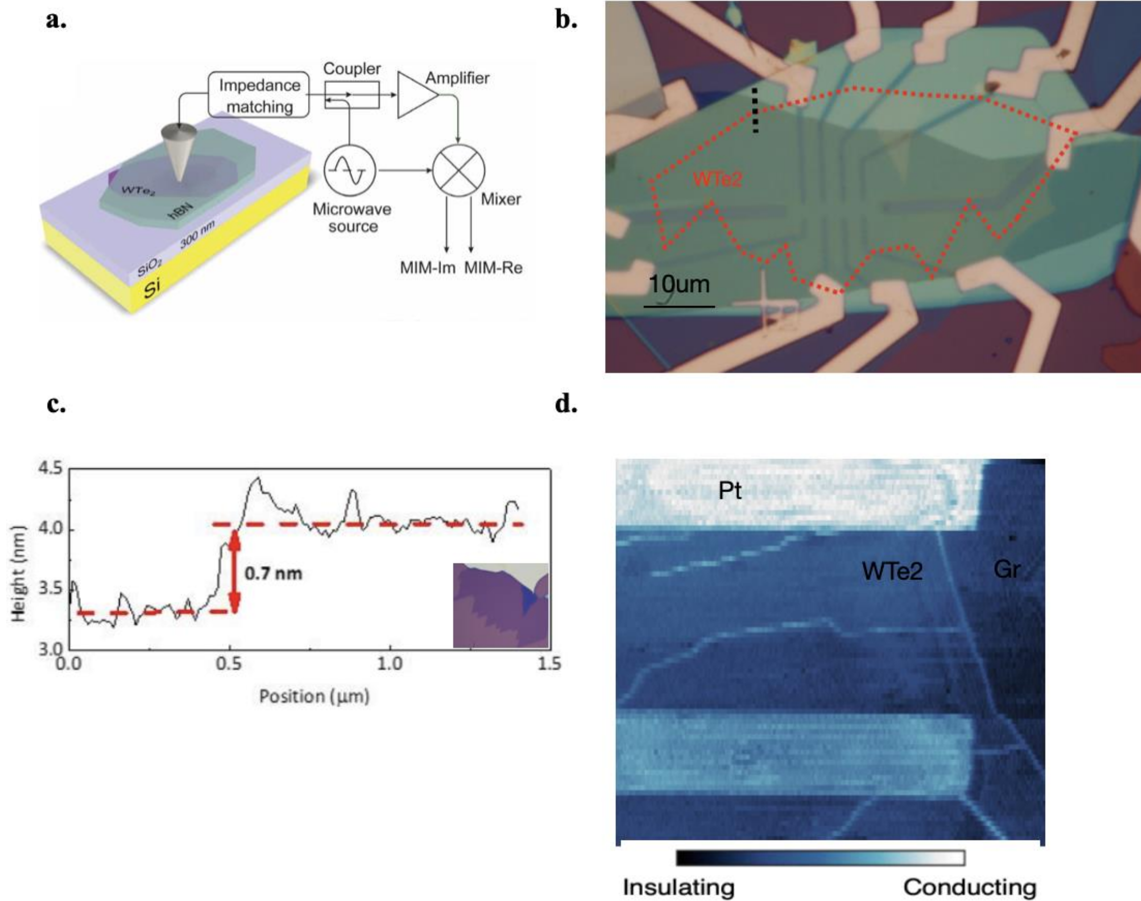

Figure 4.8: Imaging edge conductivity in monolayer WTe2. (a) Schematics of the technique and device structure (Taken from the 88). (b) Optical image of a WTe2 monolayer exfoliated onto prefab graphite gate and covered with a 20-nm-thick hBN. (c) Line cut along the black dashed line matches the monolayer thickness ~0.7 nm. (d) MIM-Im images, measured at T = 8 K and B = 0. Scale bars, 10 um.

Figure 4-8. a shows measurement of MIM_Im versus back gate and temperature T, these data are on the simple sample, monolayer WTe2 on SiO2 which covered with hBN. We used microwave impedance microscopy on devices with no top gate. On cooling from 100 K to 5.2 K, conductivity versus back gate voltage produces a ‘V’ shape centered near to V_{gate} = 0. Although the sharpness of the V varies, most likely due to varied sample homogeneity, we have seen consistent behavior across a dozen monolayer devices. Below

100 K, as T decreases conductivity collapses over an increasingly wide range of back gate. This insulating behavior, which allows the edge conduction to dominate in normal geometries, is consistent with the findings in [92]. The drop-off of conductivity at low temperatures, even at large back gate can be explained by the fact that the monolayer adjacent to the metal contacts is partially screened from the gates and so is less doped and remains insulating. From the conductivity versus $\frac{1}{T}$ we can calculate the activation energy with:

$$\sigma(n) = \sigma_0 \frac{e^{\frac{-E_g}{K_b T}}}{ln\,\sigma} = -\frac{E_g}{K_B}.\frac{1}{T}\ ln\sigma_0 \tag{4.7}$$

which here is close to 45 meV.

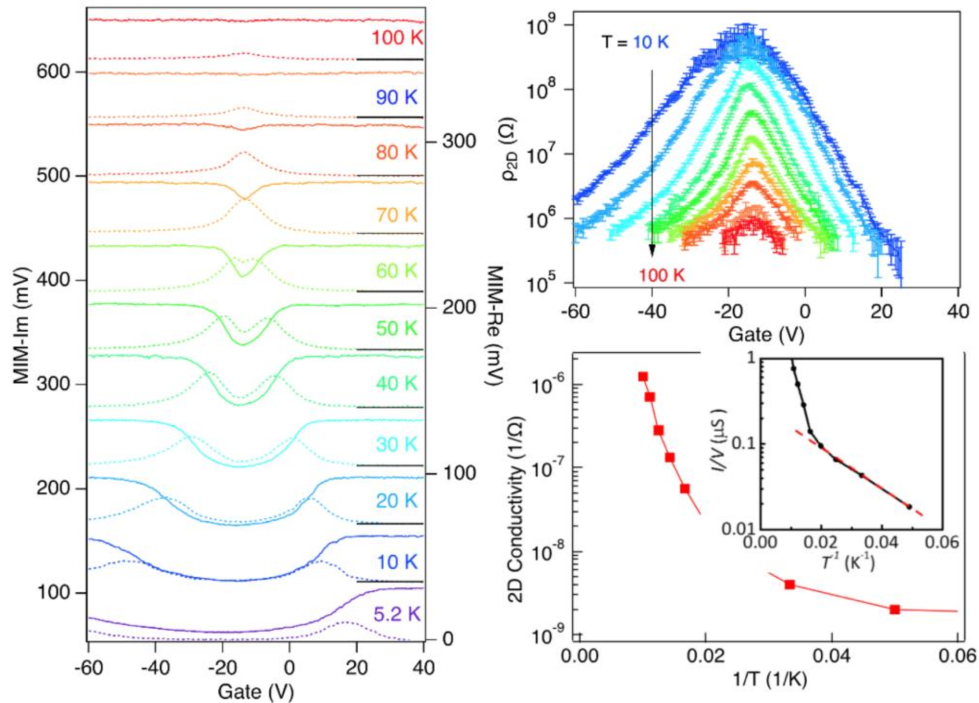

Figure 4.9: Local conductivity measurement**.** (a)conductivity versus gate-induced density at a series of temperatures T on the same device. (b)Conductivity versus ng and T at 2 GHz deduced from MIM measurements. (c) conductivity versus 1/ T.

4.8 Kelvin Probe Measurements

The Kelvin probe (KP) technique measures the contact potential difference (CPD) between two surfaces brought in close proximity. Figure 4-9. a shows two metals in proximity, but without electrical contact between them. Their Fermi levels align at the vacuum level at energies corresponding to the respective work functions Φ. As the two metal pieces are connected by a wire (Figure 4-9. b), electrons flow from the metal with the smaller work function to the metal with the larger work function. This causes the smaller work function

metal to charge positively while the other charges negatively. This creates an electric potential between the two metals, shifting their electronic states relative to each other. The electron transfer process stops once the electric field between them compensates for the work function difference. In this equilibrated state, the potential associated with the electric field exactly equals the work function difference, i.e., the CPD, between the metals.

They can be utilized for the measurement of the CPD. Gradual application of a counter potential to the CPD and monitoring the charge on one of the metals (for example with an electrometer) allows the determination of the charge-free point. The counter potential V_b that achieves this state is equal to the CPD. In practical instruments one of the metals (the actual Kelvin probe) is vibrated at a certain frequency ω (see Figure 4-9.c). Using a lock-in amplifier, the AC(ω) current generated by the oscillation (due to the varying distance, the amount of charge varies that is necessary to maintain the electric field between the surfaces) is monitored. Gradual ramping of the counter potential and finding zero AC current yields CPD. Since small currents are difficult to detect, usually an I/V curve is measured and the I=0 point is found through a curve fit.

Since KP measurements can only detect the CPD, actual work function measurements are only possible through calibration. In other words, the KP needs to be calibrated against a surface with known work function. The challenge in this respect is that under ambient conditions it is challenging to generate a surface with a defined work function. Hence KP measurements are more reliable in vacuum, where a well-defined surface can more reproducibly be generated and controlled.

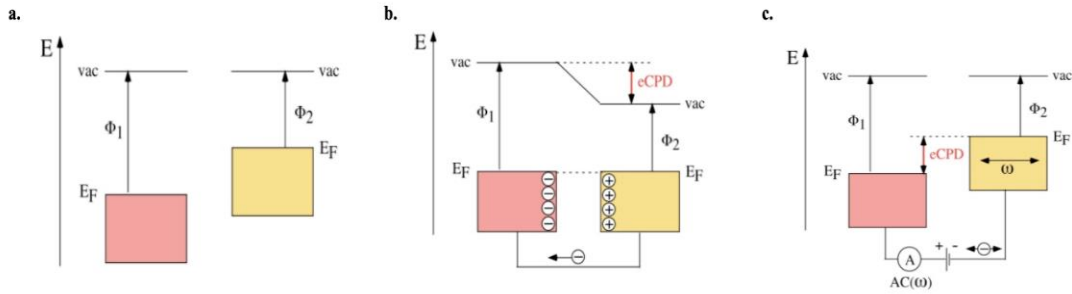

Figure 4.10: Kelvin probe (KP) measurement process.

So, to confirm about our technique here, we first perform KPFM measurement on the graphene sample. High conductivity and low optical absorption make graphene an attractive material to test. In this study, we apply scanning Kelvin probe microscope techniques to back-gated graphene devices and demonstrate that the work function can be controlled over a wide range by electric field effect induced modulation of carrier concentration.

Graphene samples were prepared by mechanical exfoliation [125] on Si wafers covered with 300 nm thick SiO2, and then Cr/Au electrodes (5nm/50nm thickness) were fabricated by standard electron beam lithography. The thickness of each graphene samples was characterized by Raman spectroscopy.

In this subsection, we have studied single layer graphene (SLG) transistors. Figure 4-10.a shows a schematic diagram of the simultaneous KPFM experiment. Transport measurement (Figure 4-10. b) on the same device as a function of Vg. In the particular device shown in this figure, we determine the charge neutral gate voltage from the gate voltage corresponding to a sharp resistance peak.

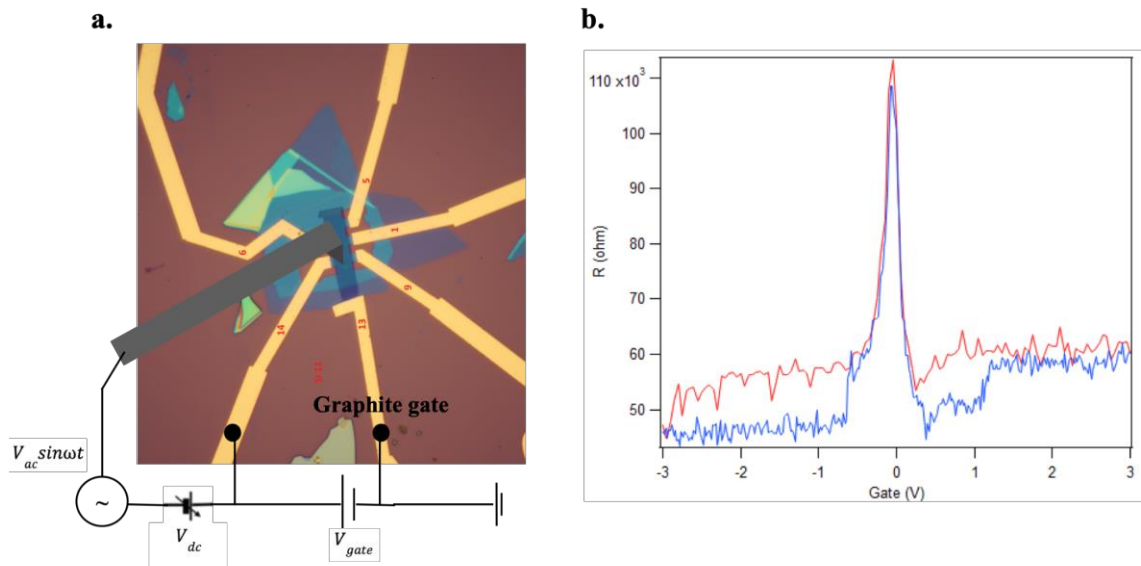

Figure 4.11: (a) Schematic diagram for measuring the Electric Field Effect modulation of the surface potential of graphene devices using the KPFM. Gate voltage Vg is applied to the graphite gate and the electrodes of graphene device are grounded. (b) Transport measurement using the two outer terminals. From the peak position we have CNP.

The carrier density, and hence the Fermi energy, E_f of the graphene, is controlled by the gate voltage Vg applied to the graphite gate. In general, the local surface potential, VCPD, obtained from the contact potential difference between the KPFM probe and local surface, is sensitively influenced by Vg. By comparing VCPD maps taken at Vg =0V (Figure 4-11.c) and 0.65V (Figure 4-11. e), we notice a much larger signal contrast at higher Vg. In particular, VCPD tends to increase to values comparable to Vg on the insulating SiO2 substrate.

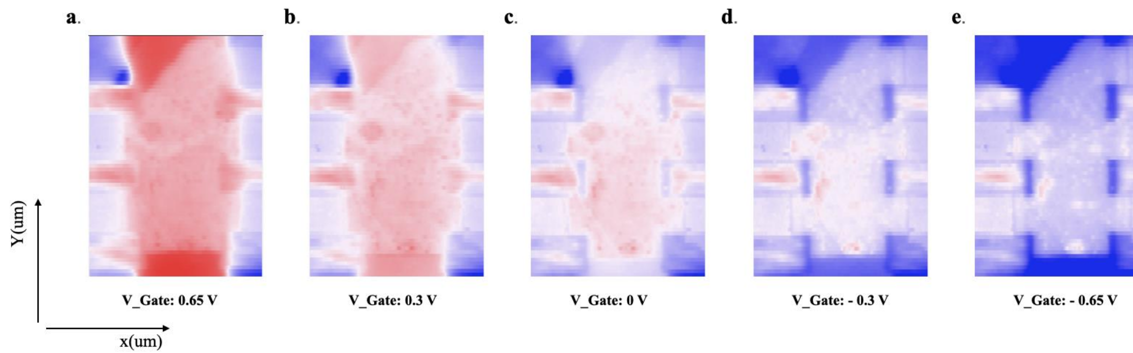

Figure 4.12: KPFM images with B = 9T of graphene device (a)Vg = 0.65 V, (b) Vg= 0.3 V, (C) Vg= 0V, (d) Vg= -0.3V, and (e) Vg= -0.65V respectively.

Now let's use the same technique to measure the chemical potential on monolayer WTe2 device. We study a device including a graphite gate sheet in parallel with the WTe2 monolayer separated with hBN for the back gate, as shown in Figure 4-3. a. There are two possible band structure of monolayer 1T'-WTe2, first: with the insulator band gap or second: with the interaction driven gap. How to measure energy gap? In 2D materials, carrier density can be tuned by gate, which means we need to measure chemical potential. So, to address this question we perform the KPFM at different temperature on monolayer WTe2 device, as you can see the data on one of our devices in figure 4-13.

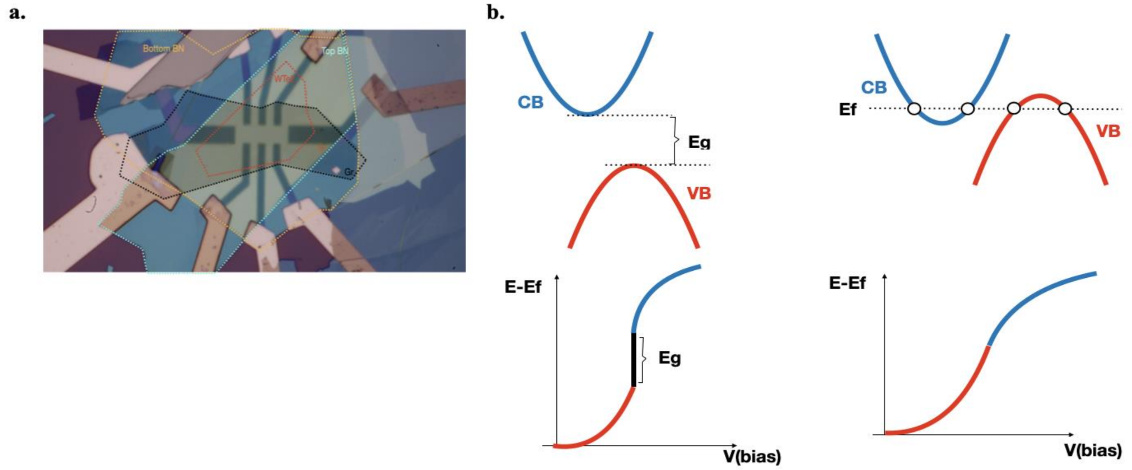

Figure 4.13: (a) Schematic diagram for measuring the surface potential of 1T'-WTe2 devices using the KPFM. Gate voltage Vg is applied to the graphite gate and the electrodes of WTe2 device are grounded. (b) Two possible band structure of monolayer 1T'-WTe2, left panel: With band gap, and right panel: With an interaction driven gap.

In particular, the Electric Field Effect (EFE) induced local surface potential change in WTe2, ΔV_{CPD} can be obtained by $\Delta V_{CPD} = V_{CPD}^{electrodes} - V_{CPD}^{WTe2}$. Interestingly, a sudden change ΔV_{CPD} is observed at the charge neutrality point ~Vg =0V. Similar features are always present at the charge neutrality point in other monolayer WTe2 samples studied in this experiment. Unlike the Capacitance measurement data there is such sudden change of ΔV_{CPD} in a smaller back gate voltage range. We still need to measure more monolayer devices to figure out about this difference, but from KPFM data here we can see the nature of this gap is coming from the interaction. at temperatures below about 100 K, monolayer WTe2 does become insulating in its interior.

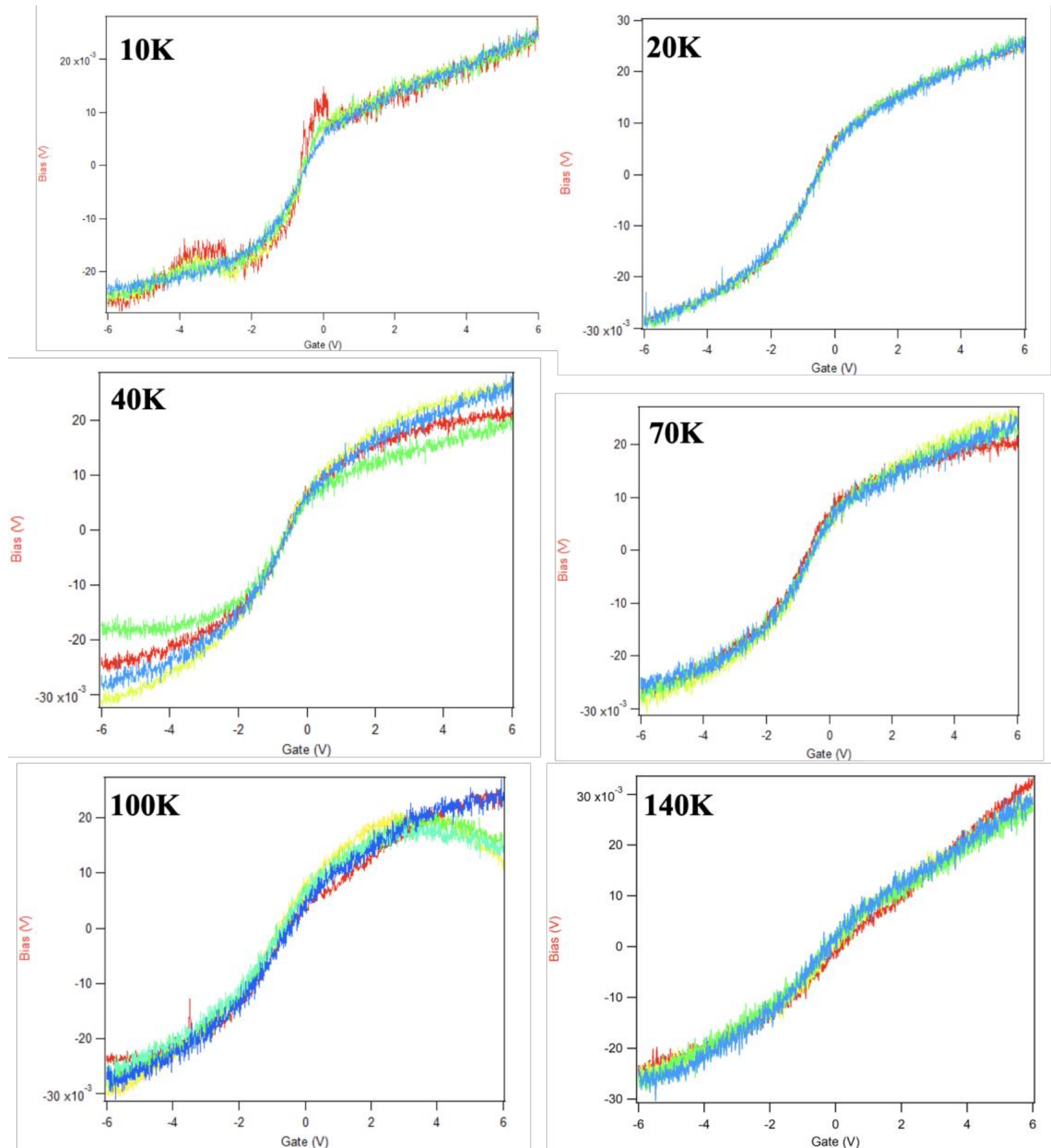

Figure 4.14: The T dependence at zero field data. On cooling from 100K to 10K there is sudden jump at CNP, which corresponding to interaction driven gap.

In our measurement there is a background signal which is due to the unscreened long-range electrostatic interaction between the conducting cantilever probe and the back gate and, thus, is insensitive to a small spatial position change of the KPFM tip. Since V_{gate} should not influence the local surface potential in metallic electrode, the background signal on the

metal electrode surface can serve to separate the spatially constant background from the relative change in the local surface potential. In conclusion, by employing a gate modulated KPFM measurement, we have demonstrated that changing in the ΔV_{CPD} of monolayer WTe2 can be illustrate that this gap can follow second scenario as I described above.

Chapter 5: Ferromagnetic order induced in the monolayer WTe2 via proximity with 2D magnet Cr2Ge2Te6

This chapter is a reproduction of a published work[126], with a few modifications to the text to adapt for the structure of this thesis.

5.1 Motivation

5.1.1 Overview

Topological insulators (TIs) provide intriguing prospects for the future of spintronics due to their large spin–orbit coupling and dissipationless, counter-propagating conduction channels in the surface state. The combination of topological properties and magnetic order can lead to new quantum states including the quantum anomalous Hall effect that was first experimentally realized in Cr-doped (Bi, Sb)2Te3 films. One way to have magnetic topological insulator is doping TIs with magnetic material like Cr or Mn. The creation of heterostructures using molecular beam epitaxy is flexible method, to create magnetic or anti ferromagnetic topological insulator, including rare-earth-doped TIs, magnetic insulators, and antiferromagnets, which result in unusual phenomena like skyrmions and exchange bias. These examples go beyond transition-metal-doped and undoped TI

heterostructures. Also, recently the new intrinsic magnetic topological insulator like MnBiTe family was introduced which there is evidence for interlayer magnetic coupling in the layered magnetic topological insulator $MnBi_2Te_4$. The intrinsic magnetic topological insulator MnBi2Te4 has attracted much attention due to its special magnetic and topological properties. To date, most reports have focused on bulk or flake samples. For material integration and device applications, the epitaxial growth of MnBi2Te4 film in nanoscale is more important but challenging.

Alternative strategies are being investigated since magnetic doping can have negative effects and requires extremely low working temperatures. The obvious choice to increase the temperature for seeing the various quantum effects is proximity coupling to magnetically ordered systems.

5.1.2 Proximity in the heterostructure of vdW materials

Low-dimensional material evolution has regularly produced exciting new physical norms and offers a distinct strategy for scientifically designing a revolutionary technology. However, reducing the size of spin-electronic devices necessitates in-depth understanding and fine-tuned control over engineering interfacial structures, which presents an interesting prospect. Atomically thin two-dimensional van der Waals materials incorporate control and tuning of different physical states by coupling with external perturbations including pressure, gating, Moire pattern, and proximity effect in order to expose unusual quantum phases. Till date, the modifications in two-dimensional crystals like semiconductor, superconductor, semimetal, metals, topological insulators, the magnetic semiconductor is

mostly seen via doping, or proximity introducing magnetic species or inducing defect, coupling with substrates, where extrinsically the impurities were introduced to amend and modify their properties. These modifications suggest a new path to realize intrinsic magnetic behavior in vdW heterostructure, where dynamics of spin are predicted to be significantly enhanced. Extrinsically introduced dopants or defects in 2D vdW crystals have been commonly employed to alter the surface and interfacial phenomena leading to produce exciting outcomes. However, even with a successful realization and modifications of extrinsically induced phenomena in 2D atomic crystals, they have certain restrictions in the context of doping concentration, which results in disordered spins and notably reduces the mobility of electrons in 2D layered crystals. Another factor that makes it difficult to determine the physical and chemical properties is the low solubility of the dopant or defect concentration.

A remarkable route for material design has been opened by proximity effects in order to get over the drawbacks of extrinsically produced phenomena. In order to manipulate spintronics, superconductors, topologically non-trivial phenomena, and excitonics, proximity effect is one of the most important tools. When two or more dissimilar materials are combined and brought close to one another due to the proximity effect, this effect is extremely adaptable to interfacial phenomena.

5.1.3 Ferromagnets and QSH insulators

Ferromagnets are known to exhibit a series of magnetization-dependent transverse transport phenomena as linear responses to electric field or temperature gradient, many of

which are intimately interrelated. In metals and semiconductors for example, the anomalous Hall effect (AHE) and anomalous Nernst effect (ANE) are connected by the Mott relation through the anomalous Hall conductivity's energy derivative, and their respective unquantized coefficients are quantitatively determined by either intrinsic and/or extrinsic mechanisms [127–129]. In magnetically doped topological insulators, on the other hand, the anomalous Hall conductance is quantized to $\frac{e^2}{h}$ due to the one-dimensional (1D) ballistic chiral edge transport, the hallmark of the quantum anomalous Hall effect [130,131]. According to the Mott relation, a 1D ballistic chiral edge is not expected to generate any ANE. In ideal quantum spin Hall insulators (QSHI) [13,24,33,132–136], on the other hand, the two counter-propagating helical edge currents produce neither Hall nor Nernst signal due to time reversal symmetry (TRS), although each edge channel has the same but opposite quantized Hall conductance. To understand the edge current transport in these two different topological systems, it is instructive to introduce a ferromagnetic order to break TRS in the QSHI systems.

Among existing 2D QSHIs including HgTe/CdTe [24,134] and InAs/GaSb[136] quantum wells, 1T' monolayer (ML)-WTe_2 has recently attracted much attention for its well-defined bulk and gapless edge band structure with a large QSHI gap [73,84,118] spatially resolved metallic edge states [88], possible exciton insulating state [91,92], and close-to-quantized conductance [89,137]. In general, ferromagnetic order can be introduced via doping or interfacial proximity coupling in heterostructures containing a ferromagnet. The latter approach has been demonstrated in several material systems including graphene [138] and topological insulators[139,140]. For ML-WTe_2, the heterostructure approach has a particular appeal

because van der Waals (vdW) heterostructures such as CrI_3/WSe_2 [141], CrI_3/WTe_2 [142] have proven very effective in creating proximity coupling due to the atomically flat interfaces. In CrI_3/WTe_2 edge state transport revealed fascinating nonlinear and nonreciprocal characteristics which were attributed to electron-magnon interaction between the metallic edge in WTe_2 and the magnetic CrI_3. It gave rise to interesting questions such as the magnetic state of the bulk and possible bulk-edge coupling [142].

5.2 Experimental Results

5.2.1 Fabrication Of WTe2/CGT heterostructure devices

We fabricate high-quality vdW heterostructures comprised of ML-WTe_2 and few-layer vdW ferromagnet $Cr_2Ge_2Te_6$ (CGT) using a glove-box transfer/pickup technique to probe edge and bulk transport responses to both AC temperature gradient and electric field.

We fabricate our devices using the following processes (from bottom to top). (1) The few-layer graphene (FLG) gate is transferred (with the BN using Polycarbonates pick-up procedure) on a SiO2/Si substrate with prepatterned Cr (5 nm)/Au (30 nm) heater using electron beam lithography (EBL). (2) A thin hexagonal boron nitride (BN) layer (~35 nm) is transferred to electrically isolate the FLG gate and the pre-patterned heater from the ML 1T' WTe2 to be transferred on top. (3) Pt-electrodes are patterned on the top of the bottom BN using EBL and lift-off. (4) For device D7 with the edge insulated from the ML-WTe_2 interior (bulk) channel, a thin BN layer is transferred to cover the Cr/Au electrodes except the far ends (Fig. 5.1.a). (5) A suitable ML-WTe_2 flake is identified under optical microscope (as

shown in Fig. 5.1.a and 5.1.b) and picked up using a thin flake of CGT, then the ML-WTe_2/CGT heterostructure as a composite layer is transferred onto the prepatterned Pt-electrodes (as shown in Fig. 5.1.c). The WTe_2 bulk crystals in our experiments are purchased from 2D Semiconductor and the CGT crystals are provided by Prof. S. Jia's group at Peking University. (5) The ML-WTe_2/CGT heterostructure device including Pt electrodes is encapsulated by a top BN layer to prevent degradation and maintain device stability. We have fabricated and studied seven devices in this work.

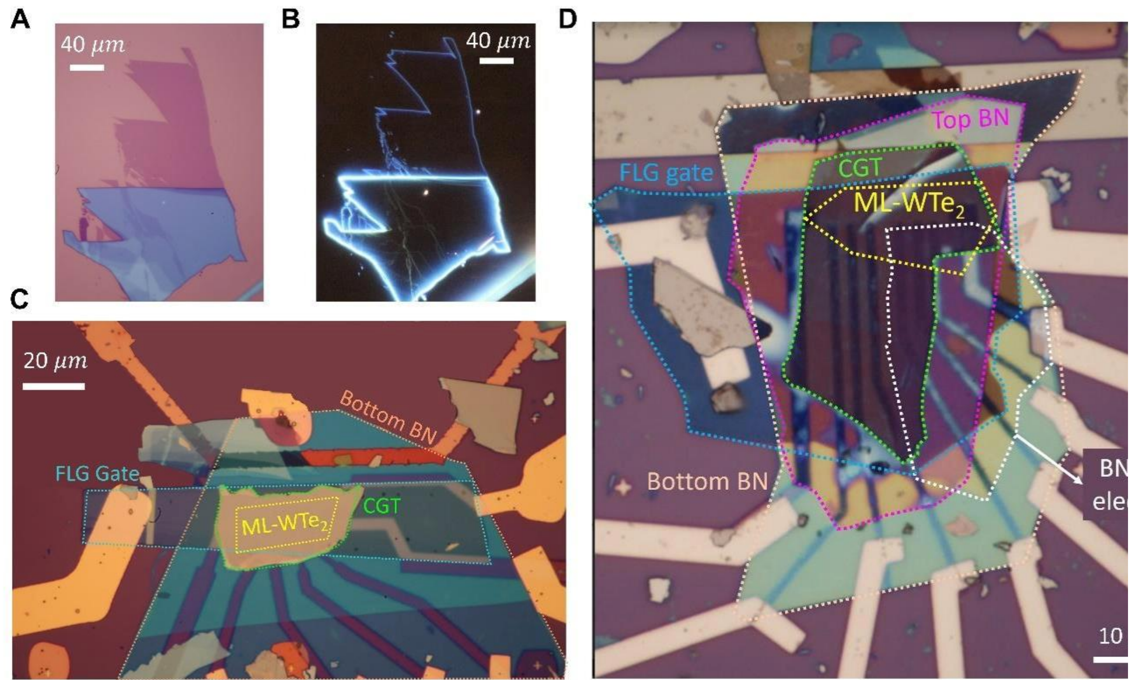

Figure 5.1: Optical images of monolayer (ML) WTe_2 and ML-WTe_2/CGT devices after fabrication**.** (**a**) Bright-field image of exfoliated ML-WTe_2; (**b**) Dark-field image of exfoliated ML-WTe_2. (**c**) Optical image of device D1 after transfer of ML-WTe_2/CGT heterostructure on to the Pt electrodes. A thin BN layer around 35 nm is encapsulated on the top of the device later for protection. (**d**) Optical image of the device D7 after fabrication. All the layers are identified by the dashed polygons.

Figure. 5.2.a shows a schematic illustration of the ML-WTe_2/CGT vdW heterostructure. CGT is an insulating ferromagnet (well above ~10 GΩ in thin flakes) below its Curie temperature T_c of 61 K with the magnetic anisotropy perpendicular to its atomic layers. We expect a strong exchange interaction between ML-WTe_2 and CGT at the atomically flat interface, and consequently, for the former to acquire ferromagnetism via proximity coupling. We electrically probe the induced ferromagnetism in ML-WTe_2 by measuring the ANE, AMR and AHE responses. The ANE device structure is shown in Figure 5.2.b. Figure 5.2.c is the optical image of the device (D1) prior to transfer of ML-WTe_2/CGT

composite layer by the pickup/transfer technique which we describe in chapter 2 of this thesis.

5.2.2 Anomalous Nernst effect

The anomalous Nernst effect (ANE) is the generation of a thermoelectric voltage transverse to the imposed temperature gradient and applied magnetic field in a ferromagnet. This effect enables magnetic metals and alloys to be exploited for heat to electrical energy conversion.

To measure ANE responses, we fabricate a heater for generating a lateral temperature gradient perpendicular to both the heater and the voltage channel. While passing an AC current through the heater (via 1-2 electrode pair in Figure 5.2.c), we record the second harmonic voltage responses from electrode pairs 3-8, 4-7 and 4-5 (as shown in Figure 5.2.c) as an out-of-plane magnetic field H_z is swept through the bi-stable magnetic states of CGT. An AC current with the frequency of 13 Hz is fed to the nonlocal heater using Keithley 6221 current source, and the second harmonic (2*f*) ANE voltage from different channels of ML-WTe_2 is detected using the standard lock-in technique. A magnetic field is swept perpendicular to the layers of the devices. All measurements for devices are performed using either a homemade closed-cycle system or Quantum Design's DynaCool Physical Property Measurement System (PPMS).

Figure 5.2.d summarizes the H_z-dependence of the voltage signals from the three electrode pairs at the nominal system temperature of 4.0 K. Hysteresis behaviors are observed in all three channels which resemble the anomalous Hall loop in CGT/Pt [143,144], strongly

indicating their acquired origin from CGT. In well-studied ferromagnetic insulator (FMI)/heavy metal (HM) heterostructures, two possible mechanisms can give rise to similar magneto-thermoelectric voltage hysteresis: ANE due to induced ferromagnetism in HM and spin Seebeck effect (SSE). Here in ML-WTe_2/CGT, the SSE mechanism can be straightforwardly excluded based on the device geometry. In general, SSE voltage is generated by spin-charge conversion in the HM layer with strong spin-orbit coupling (SOC) [143]. The out-of-plane spin current flow should be primarily sensitive to the in-plane magnetization of the FMI. In these loops, however, there is no apparent in-plane magnetization characteristic present. In addition, the spin-charge conversion by a 3D HM layer via the inverse spin Hall effect (ISHE) requires more than one atomic layer in thickness for spin current diffusion and spin-charge conversion [145,146]. In our heterostructures, WTe_2 contains strictly one atomic layer; therefore, together with the out-of-plane magnetization characteristics in the voltage loops shown in Figure 5.2.d, we exclude the SSE mechanism and attribute them to ANE, i.e., $V_{ANE} \sim L\nabla T \times M_z\hat{Z}$, here L being the channel length and M_z the out-of-plane component of the induced magnetization in ML-WTe_2. The induced M_z should follow that of the CGT surface layer, the source of the induced ferromagnetism. The slanted V_{ANE} loops with vanishing remanence at H_z=0 are results of multidomain formation, which was previously reported in the anomalous Hall and magnetic force microscopy study of CGT thin flakes [144].

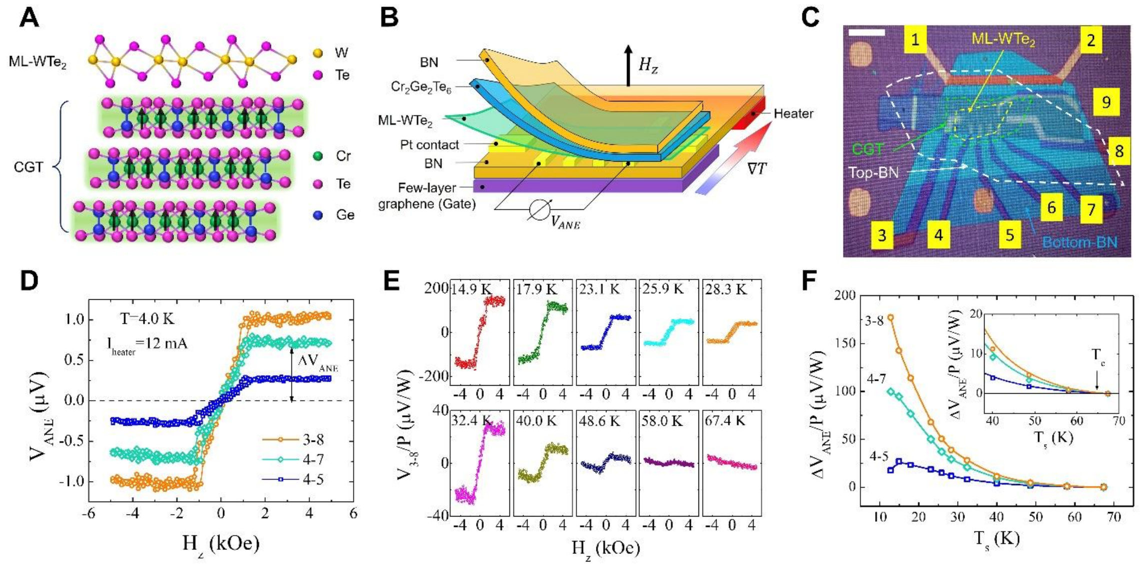

Figure 5.2: Device structure and anomalous Nernst signals in monolayer 1T' WTe2/Cr2Ge2Te6 heterostructure. (a) Schematic of monolayer (ML) 1T' WTe2/Cr2Ge2Te6(CGT) vdW heterostructure. (b) Schematic of the ANE device structure. BN stands for hexagonal boron nitride. The nonlocal heater for generating ∇T is underneath the bottom BN. Open circuit voltage V_ANE due to ANE is measured in sweeping out-of-plane magnetic field Hz. (c) Device optical image before transfer of ML-WTe2/CGT composite layer on pre-patterned Pt electrodes. The scale bar is 20um. (d) Magnetic field dependence of ANE signal from electrode pairs 3-8, 4-7 and 4-5. The heating current in channel 1-2 is 12 mA and the system temperature is set to 4.0 K. (e) Magnetic field dependence of ANE signal from channel 3-8 at different sample temperatures ranging from 14.9 K to 67.4 K. The vertical axis is the ANE voltage normalized by the heating power P. The actual sample temperature Ts is indicated in each panel which is calibrated with the temperature dependence of ML-WTe2's four-terminal resistance measured with a small current. (f) Heating-power-normalized ANE signals from channels 3-8, 4-7 and 4-5 vs. Ts. Inset shows the data between 40 K and 70 K, where the ANE signals in all three channels vanish around the Curie temperature Tc=61 K of CGT.

5.2.3 Heating power dependence of ANE

To further confirm the thermoelectric nature of ANE signal in Figure 5.2.d, we perform heating-power dependence of the ANE signals from channels 3-8, 4-7 and 4-5 of device D1. Under fixed system temperature, the sample temperature rises due to Joule heat from nonlocal heater. To obtain the heating-power dependence of ANE signal at a fixed sample

temperature, we adjust the system temperature accordingly to maintain the targeted sample temperature (Ts=26.5 K) monitored by the sample resistance. As summarized in Figure 5.3.C, the hysteresis loops from channel 3-8 (Figure 5.3.a), 4-7 (Figure 5.3.b) and 4-5 (Figure 5.3.c) shrink as the heating-power decreases. Clearly, the linear power dependence displayed in Figure 5.3.d entails a linear temperature gradient ∇T -dependence, and thus is consistent with the ANE responses.

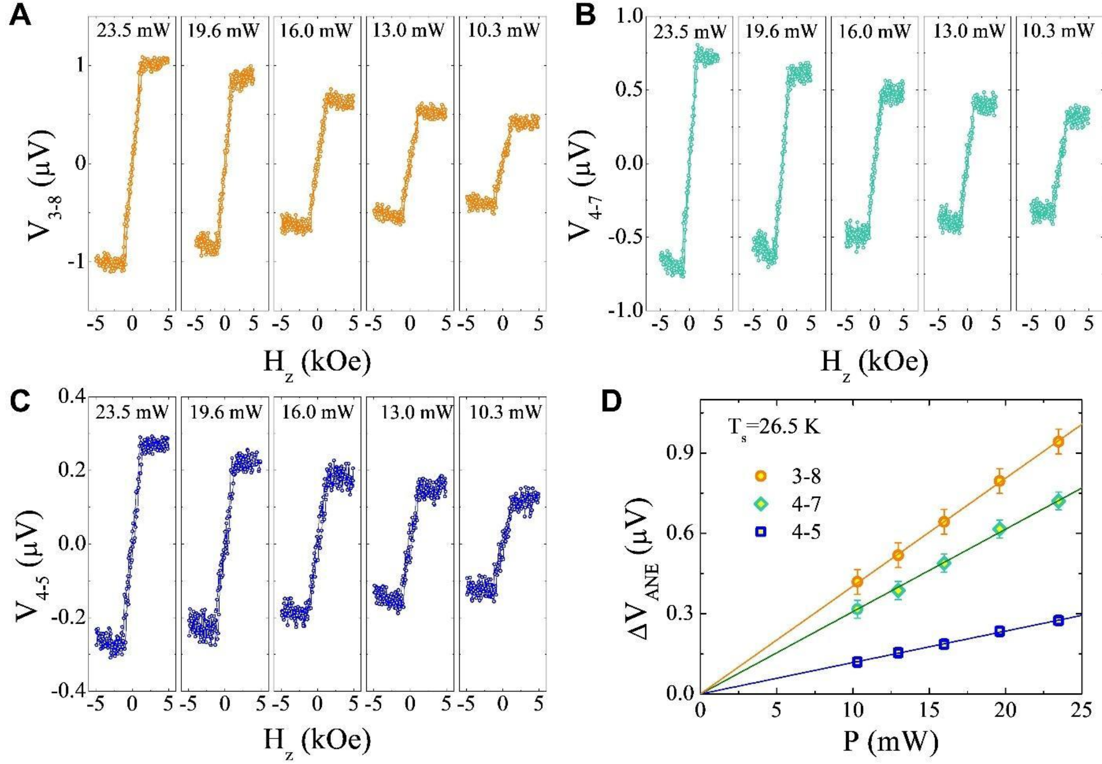

Figure 5.3: Heating power dependence of anomalous Nernst effect (ANE) signal from ML-WTe2/CGT heterostructure. ANE voltages from channel 3-8 (a), 4-7 (b) and 4-5 (c) as a function of out-of-plane magnetic field under different heating power. The sample temperature is fixed at 26.5 K by keeping resistance of ML-WTe2 a constant during the measurements. (d) Heating power dependence of ANE voltages from 3-8, 4-7 and 4-5 channels, the sample temperature is fixed at 26.5 K. The straight lines are linear fitting results.

5.2.4 Temperature dependence measurement

To further investigate the correlation between the magnetic order in CGT and the induced ferromagnetism in ML-WTe_2, we carry out temperature dependence measurements of V_{ANE}. As shown in Figure 5.2.e, we perform intricate, temperature-dependent experiments to look into the relationship between the ANE signals that have been recorded and the ferromagnetic order in the CGT layer. The similarities between the properties of the two

channels are evident: the hysteresis loop diminishes in size as the sample warms up and disappears above the CGT crystal's Curie temperature (Tc=61 K), the magnitude of ANE signal, which is defined as the V_{ANE} value extrapolated from saturation to H_z= 0, decreases as the device warms up before it disappears at 61 K, the T_c of CGT. The linear H_z-dependent background of V_{ANE} is due to the ordinary Nernst effect. We perform heating-power dependence of the ANE signals from channels 3-8, 4-7, and 4-5 of device D1 to further support the thermoelectric nature of the ANE signal in Figure 1D. Under constant system temperature, the nonlocal heater's Joule heat causes the sample temperature to rise. We change the system temperature appropriately to maintain the intended sample temperature (Ts=26.5 K) tracked by the sample resistance in order to determine the heating-power dependency of the ANE signal at a fixed sample temperature. Hysteresis loops from channels 3-8, 4-7, and 4-5 contract as the heating-power drops. It is obvious that the linear power dependence seen in Figure 5.3.d implies a linear temperature gradient T -dependence and is therefore consistent with the ANE responses.

We plot in Figure 5.2.f the ANE magnitude as a function of actual sample temperature T_s obtained using the sample resistance as a thermometer. It is clear that the ANE magnitude tracks the ferromagnetic order of CGT. So, the hysteresis behavior on ANE signal, temperature dependence measurements of ANE signal, and linear Heating power dependence of anomalous Nernst effect showing the existence of ferromagnetism in monolayer WTe2.

5.2.5 Determination of sample temperature

Temperature plays a key role in determining the transverse Seebeck coefficient's value, here, we show how both experimental methods and finite element simulations can be used to determine. In an experiment, we calibrate the real temperatures at each site using the resistance of the heater and the ML-WTe2. A very low current density is used as a temperature calibration curve before measuring the resistances as a function of temperature. Local temperatures increase above the system temperature as the heater is turned on, and the resistance can be used to precisely measure this change. The heater and ML-real WTe2's temperatures are measured using resistive thermometry. In our measurements of P-dependent ANE voltages (as shown in Figure 5.3), the actual sample (ML-WTe2) temperature is held at Ts=26.5 K which is monitored by its resistance while adjusting the measurement system temperature.

In actual devices, the local temperature near the heater is not a linear function of the distance; therefore, we use a finite element method (COMSOL) to simulate the temperature profile in our ANE device. Based on the device configuration (Fig. 5.4), the width and thickness of the Au heater are 5 µm and 50 nm, respectively. The heater sits on top of a 285 nm thick SiO2 on a Si substrate. The WTe2/CGT heterostructure composite layer is separated from the FLG by a BN flake. The overall dimensions of the entire device are 160 um x 160 um x100 um. A 3D view of the simulated domain is shown in Figure 5.4.d. A constant temperature boundary condition of 4 K is applied to the bottom and four side surfaces of the Si substrate. We use experimentally measured resistivity of Au film in the

simulation of heating generated by heater. Due to the large electrical resistance of SiO2 and BN in contact with the Au wire, the electric current in the heater is converted to a uniformly distributed heat flux along the Au wire. The temperature-dependent heat capacities, thermal conductivities and interfacial thermal conductivities of relevant materials are obtained from literatures [1-17]. Figure 5.4.e shows the temperature profile of the ANE device for different heating-power. It is clear that the temperature profile is highly nonlinear. The local temperature gradient at 27.5 um (the center of WTe2/CGT heterostructure) extracted from the simulation is 0.1742 Kum for P=23.5 mW, which is ~11.6 times smaller than the global average temperature gradient (30.3 K/15um) assuming a linear temperature distribution. Therefore, we greatly underestimate the value of Sxy by assuming a linear temperature distribution, and the actual Sxy should be one order of magnitude greater than the value determined from the experimentally measured local temperatures assuming a linear temperature profile.

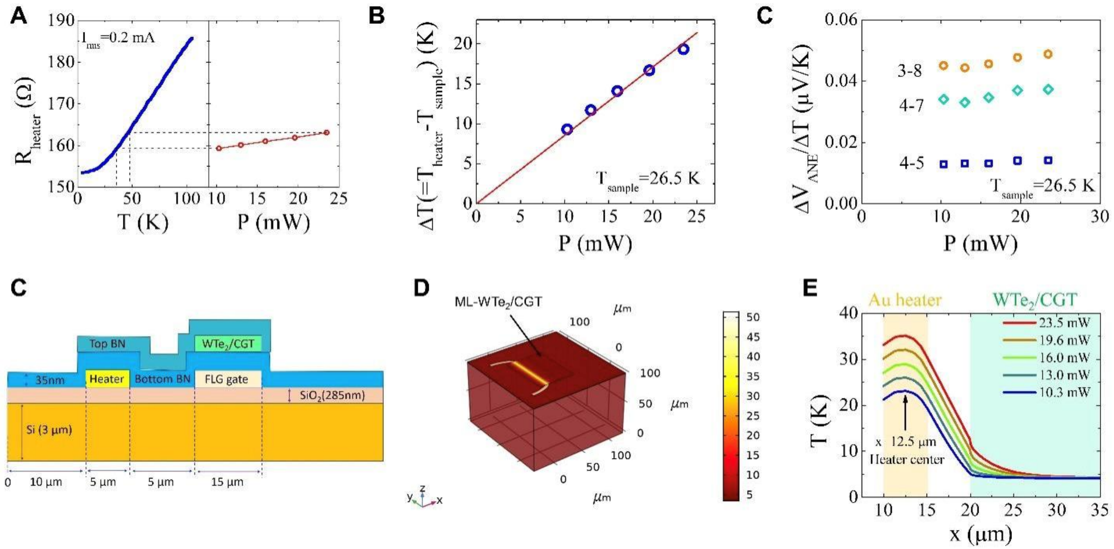

Figure 5.4: Experimental and simulated temperature difference in the anomalous Nernst effect (ANE) device. (a) Heater resistance as a function of temperature and heating power in device D1. AC current with rms magnitude from 8 mA to 12 mA is applied in the nonlocal heater to produce different heating-power. (b) Heating-power dependence of temperature difference *ΔT* between nonlocal heater and ML-WTe2, where the sample temperature is fixed at 26.5 K during the measurements. (c) *ΔT*-normalized ANE magnitudes from three different channels as a function of nonlocal heating power. (d) Cross section of ANE device structure used in the COMSOL simulation for heat conduction. (e) Simulated 3D distribution of the temperature in the ANE device. (f) Simulated temperature under different heating powers as a function of lateral distance x. The position of Au heater and ML-WTe2/CGT device is marked with yellow and green shades.

5.2.6 Magneto Transport Properties

After experimentally establishing the induced ferromagnetism in ML-WTe_2, we turn to magneto-transport properties of the ferromagnetic ML-WTe_2. By passing an AC current in ML-WTe_2 with the frequency of F (13 Hz) and the root-mean-square (rms) amplitude of I_{rms} (3 μA), we simultaneously measure the first- and second-harmonic longitudinal voltage responses, i.e., 1*f* and 2*f* voltages as sketched in Figure 5.3.a. Figure 5.3.b plots the H_z-dependence of the 1*f* (top panel) and 2*f* (bottom panel) voltages from the 4-7 channel

measured at 4 K. The raw $1f$ signal clearly contains both H_z-symmetric V_{4-7}^{1f-S} and H_z-antisymmetric V_{4-7}^{1f-AS} components with comparable magnitude. The large mixing of the antisymmetric signal in the longitudinal channel can be caused but may not be fully accounted for by the irregular WTe_2 shape and suggests a spatially non-uniform current density distribution in WTe_2. After summarization and antisymmetrization, we obtain V_{4-7}^{1f-S} and V_{4-7}^{1f-AS} hysteresis loops that are characteristic of the AMR and AHE responses of ferromagnetic conductors, respectively as shown in middle panel of Figure 5.3.b. These loops are the expected outcomes of the proximity-magnetized ML-WTe_2. In FMI/HM heterostructures such as YIG/Pt, there has been a long-standing debate on the origin of similar magnetoresistance and AHE. Spin Hall magnetoresistance (SMR) was proposed to be wholly or partly responsible because the spin current generation in and reflection across the HM layer thickness are highly relevant in such heterostructures [147]. However, the SMR mechanism is clearly not applicable here due to the single atomic layer thickness of WTe_2 despite its strong SOC.

Additionally, the SMR mechanism can be refuted from the H_z-dependence of the $1f$ MR signal with the following arguments. As H_z is swept below the saturation field H_s CGT starts to evolve to multi domains as previously imaged by magnetic force microscopy and thus develop in-plane components, M_x and/or M_y. According to the SMR theory [147] the finite M_x component does not produce any resistance change, whereas M_y only causes the resistance to decrease from its saturation value as M is aligned with the z(-z) direction. This is obviously contradictory to the peak feature in our $1f$ MR signal. Hence, the $1f$ MR signal is clearly the AMR effect expected for the magnetized ML-WTe_2. Additionally, the $1f$ AHE

signal provides another proof of the induced ferromagnetism in ML-WTe_2. Similar proximity-induced AHE has also been observed in other quantum materials including graphene [138] and topological insulators [140,148]. Apart from the $1f$ AHE hysteresis, a strong $2f$ hysteresis loop is also present in Figure 5.5.b-bottom, which has the same but inverted shape as the $1f$ AHE loop In YIG/Pt heterostructures, passing a large AC current in Pt can indeed produce both $1f$ and $2f$ responses, but normally the former dominates [148]. and the $2f$ signal originates from the SSE due to the Joule heating generated by the AC current in Pt. Just as discussed earlier for the nonlocal heating, here the SSE mechanism can be easily excluded as well. However, a self-heating induced lateral ∇T is capable of producing an ANE-like $2f$ response. Since the AC current induces an AC temperature rise in the ML-WTe_2 with the frequency of $2f$ and the ML-WTe_2 flake acts as a heating element, the heat is dissipated outward into the surrounding medium to generate a ∇T around the edge of the flake. Along the device lower edge Figure 5.5.a where the detecting electrodes are placed, the in-plane ∇T s perpendicular to the longitudinal voltage channel, which is the geometry for detecting ANE. In fact, the $2f$ signal has the same polarity as that of the ANE signal in Figure 5.5.d, which agrees with the fact that the in-plane ∇T at the lower edge is in the same direction as that generated by the nonlocal heater. Here, we tentatively attribute the $2f$ hysteresis to ANE from the Joule heating in ML-WTe_2, the very effect presented earlier in the same device generated with the nonlocal heater. Because of the hysteretic characteristic, the $2f$ voltage appears to be a unidirectional or nonreciprocal transport response, i.e., the apparent $2f$ resistance depends on the direction of the magnetization. More discussions about this mechanism will follow later. Since the $1f$ *and* $2f$ signals are all

consistent with the induced ferromagnetism in ML-WTe_2, they should vanish when CGT becomes paramagnetic. Figures 5.5.d, 5.5.e, and 5.5.f show the H_z-dependence of AMR, AHE and ANE signals at various temperatures, respectively. Indeed, they all disappear at and above the T_c of CGT. Below 61 K, the AHE and ANE hysteresis loops have the same shape in spite of the opposite signs, indicating that they both probe the same source, i.e., ferromagnetic ML-WTe_2.

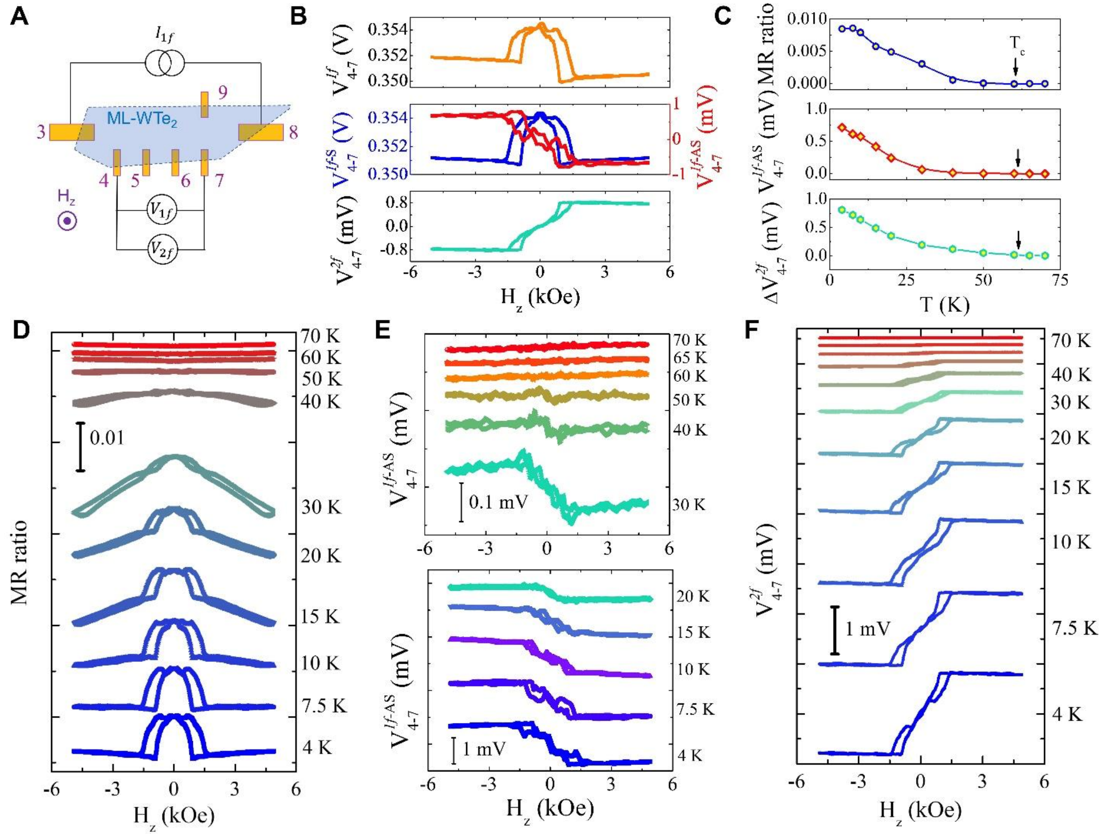

Figure 5.5: Temperature dependence of linear and non-linear responses in ML-WTe2/Cr2Ge2Te6 heterostructure. (a) Schematic illustration of measurement geometry. An AC current of 3 uA flows in the ML-WTe2 flake through channel 3-8 (x-direction), and the 1f and 2f voltage responses are measured from channel 4-7 in sweeping Hz with f=13 Hz here. (b) Magnetic field dependence of the raw 1 , 1f, V_{4-7}^{1f}(top), 1f Hz-symmetric, V_{4-7}^{1f-S} and Hz-antisymmetric, V_{4-7}^{1f-AS} (middle), and 2f V_{4-7}^{2f} voltage (bottom) at 4 K. (C) Temperature dependence of the magnetoresistance (MR) ratio (top), AHE voltage (middle) and 2f voltage (bottom) taken from the data in (d)-(f) below. MR ratio magnitude is defined as $[\frac{V_{4-7}^{1f}(5kOe)-\ V_{4-7}^{1f}(0\ Oe)}{V_{4-7}^{1f}(0\ Oe)}]$, and $\Delta V_{4-7}^{2f} = \Delta V_{4-7}^{2f}(H_s) - \Delta V_{4-7}^{2f}(0)$. $H_s$is the saturation magnetic field of V_{4-7}^{2f} . (d) to (f) Magnetic field dependence of MR ratio (d) ΔV_{4-7}^{1f-AS}, (e) and ΔV_{4-7}^{2f} (f) voltage at various temperatures, respectively. The temperatures denoted here are read from the thermometer of the measurement system and the actual sample temperature should be higher due to local heating.

5.2.7 Separating the bulk and edge contributions

The electrodes in device D1 are placed close to the lower edge as shown in Figures 5.2.c and 5.5.a, but they also contact the interior of the 2D ML-WTe_2 flake due to the lithography resolution limit; therefore, the ANE and magneto-transport signals contain contributions from both edge and bulk components. We know that the pristine ML-WTe_2 is a QSHI with gapless edge states, and we expect the magnetized ML-WTe_2 to contain both bulk and edge states as well.

To understand their respective contributions, we fabricate another type of devices represented by D7 as illustrated in Figure 5.6.a, in which one set of electrodes (from #3 to #6 in Figure 5.6.b) make electrical contact only with the bulk and the other set (from #11 to #14 in Figure 5.6.b) with both the bulk and edge. The bulk electrodes are electrically insulated from the sample edge using an additional thin layer of BN (~ 35 nm thick) to cover part of the electrodes before transfer of ML-WTe_2. With these two sets of electrodes, we first measure the two-terminal resistance as a function of temperature for the Bulk electrodes, i.e., $R_{5\text{-}6}$, and the Bulk +Edge electrodes, i.e., $R_{13\text{-}14}$. Figure 5.6.c reveals a striking contrast between these two pairs. First, $R_{5\text{-}6}$ (Bulk) is always greater than $R_{13\text{-}14}$ (Bulk + Edge) over the entire temperature range, indicating that the edge is more conductive than bulk. Second, while the difference between them remains relatively small at high temperatures, Bulk resistance $R_{5\text{-}6}$ rises steeply below 10 K while Bulk +Edge resistance $R_{13\text{-}14}$ only shows a moderate increase. This is a sign of bulk carrier freezing indicative of a bulk gap. From the temperature dependence, we determine an activation

energy of 3.16 meV. This value is smaller than that found in CrI_3/WTe_2 (2.5 meV) [149] and much smaller than the QSHI bulk gap in standalone ML-WTe_2 (~ 45 meV) [84]. Compared to QSHI, a magnetized QSHI is expected to exhibit a smaller gap due to spin splitting. For example, the spin splitting in conduction bands is about 30 meV for CGT/WTe_2 according to our density functional theory calculations. We note that a wide discrepancy in the band gap exists in the literature among various theoretical and experimental groups [73,84,118,142]. On the other hand, $R_{13\text{-}14}$ is essentially dominated by edge conduction below 10 K where the bulk carriers freeze out. We also note that $R_{13\text{-}14}$ approaches 303.7 kΩ at 2 K, which is over two order smaller than $R_{5\text{-}6}$ but at least a factor of 10 larger than h/e^2 (=25.8 kΩ), the quantized resistance from a single 1D ballistic edge channel. This large edge resistance, which corresponds to an order of magnitude smaller than the quantized edge conductance, was also previously reported in similar heterostructures or standalone ML-WTe_2 and attributed to backscattering in the edge channels of ML-WTe_2[89].

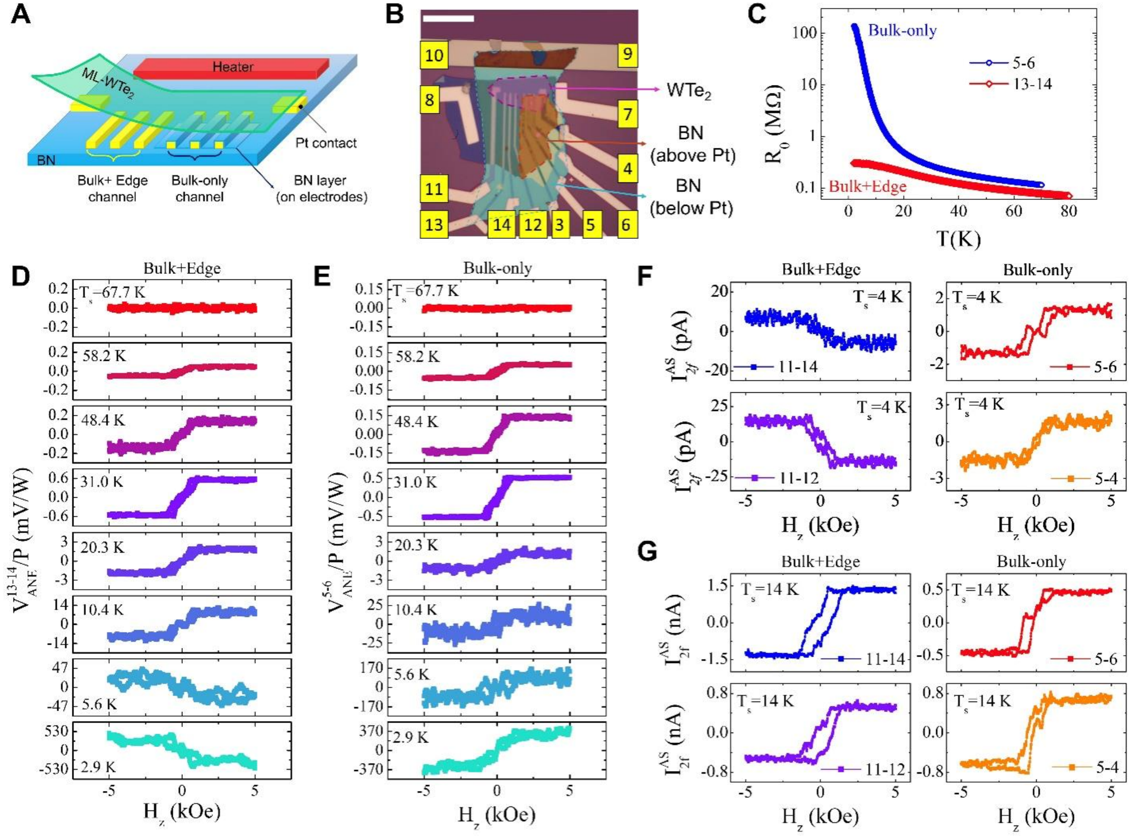

Figure 5.6: Anomalous Nernst effect and anomalous Hall effect from edge and bulk channels of ML-WTe2/Cr2Ge2Te6. (a) Schematic diagram of device structure. Electrodes on the left side probe combined edge and bulk signal of ML-WTe2, and those on the right side are partly covered with BN to prevent edge contact with ML-WTe2, thus only detect the bulk ANE. (b) Optical image of device D7 prior to transfer of ML-WTe2/Cr2Ge2Te6 composite layer. The ML-WTe2 flake is indicated by the purple dashed polygon. Electrodes from 11 to14 probe the ANE signal from both edge and bulk, and electrodes from 3 to 6 probe the bulk only ANE signal. The scale bar is 10 um. (c) Temperature dependence of resistance from 5-6 (Bulk) and 13-14 (Bulk + Edge). (d), (e), Magnetic field dependence of ANE signals from 13-14 and 5-6 at selected temperatures, respectively. (f), (g) 2f current response to AC voltage from Bulk + Edge (11-14 and 11-12) and Bulk-only (5-6 and 5-4) channels vs. Hz at Ts=4 K (f) and 14 K (g).

Because of the small bulk gap, we need to go below 10 K to access the QSHI edge transport. To avoid sample heating and achieve lower sample temperature T_s than in Figures 5.1 and 5.2, we use a much smaller AC current (I_{rms} =0.5 mA) in the nonlocal heater and

simultaneously recording ANE voltages from the Bulk +Edge (13-14) and Bulk-only (5-6) channels. Figures 5.3.d and 5.3.e show the T_s-dependent ANE voltages from the Bulk + Edge and the Bulk-only channels scaled by the heating power P. The following surprising differences stand out from the side-by-side comparison. First, the edge ANE signal does not vanish at low temperature as one would expect for QSHI ballistic edge channels. On the contrary, it increases in its magnitude. Second, the edge ANE changes the sign as T_s varies, whereas the bulk ANE remains the same sign, which clearly delineates contributions from the edge and bulk components. Furthermore, by ensuring smaller AC currents flowing in ML-WTe_2, we achieve lower sample temperatures and perform transport measurements even at the same nominal system temperature. Interestingly, the $2f$ signals in the left panels of Figures 5.6.f and 5.6.g unmistakably show opposite signs between 4 K in Figure 5.6.f and 14 K in Figure 5.6.g in their actual sample temperatures determined by the resistive thermometry for different AC amplitudes. In contrast, the $2f$ signals from the Bulk-only channel remain the same sign. These distinct $2f$ responses between the edge and bulk channels coincide with those of ANE signals measured with nonlocal heater as shown in Figure 5.6.e, further suggests their common physical origin, i.e., the ANE.

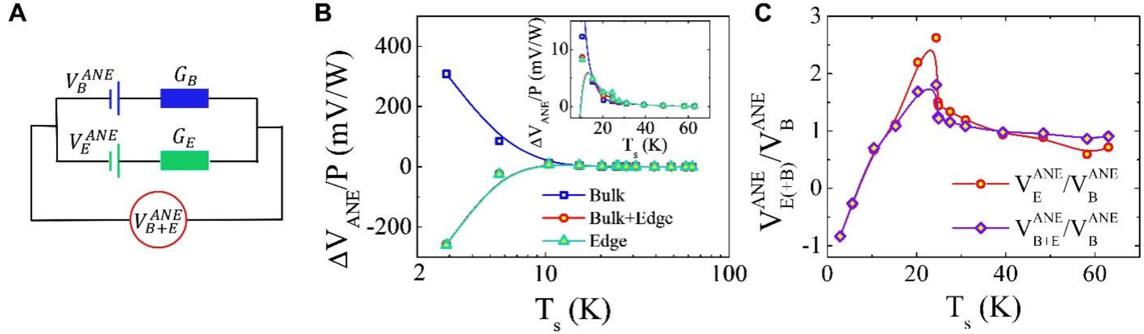

Figure 5.7: Two-component transport from edge and bulk channels of ML-WTe2. (a) Illustration of the "parallel battery-resistor" model with ANE voltages from Edge (V_E^{ANE}) and Bulk (V_B^{ANE}) channels. $G_E(G_B)$ is the conductance of the Edge (Bulk) channel. V_{B+E}^{ANE} is the total ANE signal from both edge and bulk. (b) Temperature dependence of the ANE signal from Bulk, Bulk + Edge, and Edge channels. The Edge ANE is calculated using the "parallel battery-resistor" model. Inset shows a zoom-in plot of the high-temperature data. (c) Ratio of ANE from Edge (Bulk + Edge) channel to that from Bulk-only channel as a function of sample temperature.

From the data taken with the two sets of electrodes, we can readily separate the bulk and edge contributions using a simple two-component circuit model (as sketched in Fig. 5.6.a). The P-normalized ANE signals from channels 5-6 and 13-14 in device D7 become significantly larger at low temperatures, a trend contradictory to the third law of thermodynamics. Figure 5.6.b plots the temperature dependence of ANE signals from bulk and edge channels, the latter of which is calculated using the circuit model. We explain this apparent rise in both channels as the result of the thermal conductivity rapidly dropping at low temperatures, which considerably increases the true T because $\nabla T \sim P\kappa$, ANE voltage is increased as T increased. Clearly, both edge and bulk ANE signals increase in magnitude as T_s approaches zero. This apparent low-temperature magnitude increase in both channels is possibly caused by the rapidly decreasing thermal conductivity, which greatly enlarges

the actual ∇T. While it is difficult to correct this effect, both channels are equally affected by the same thermal conductivity. In order to eliminate this common factor, we plot the ratio of the edge to bulk ANE voltages in Figure 5.6.C. Interestingly, aside from the sign change, the ratio shows a quick dive at low-T_s, because the bulk ANE approaches zero faster due to carrier freezing. The thermoelectric coefficients S are defined by E=$S\nabla T$, where $\boldsymbol{E}$ is the electrical field produced by the temperature gradient and S the thermoelectric tensor. To understand how thermoelectric transport behaves, it is appropriate to taking thermal conductivity into the account. If we crudely assume that the thermal conductivity is dominated by phonons in the surrounding materials. For constant heating power, we should multiply the ANE voltage signal by phonon thermal conductivity. As shown in Figure 5.8, we find that both curves approach zero as $Ts \to 0$ after they are multiplied by Ts, which is consistent with the expectation from the thermodynamic third law.

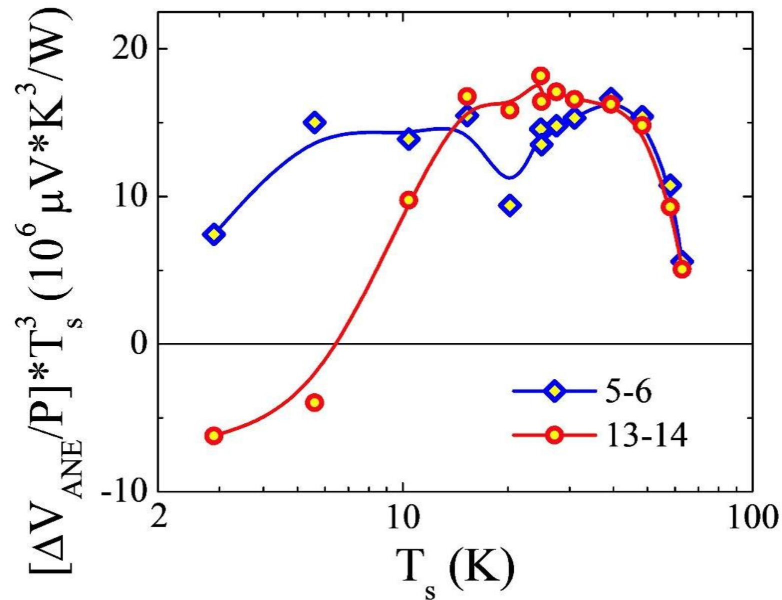

Figure 5.8: Correction of the influence of thermal conductivity on anomalous Nernst effect (ANE) signals from Bulk+Edge channel (13-14) and Bulk-only channel (5-6). T_s is the sample temperature.

5.2.8 Gate dependance

We also perform gate voltage Vg dependence measurements of the Bulk + Edge resistance. It generally shows a broad and shallow maximum centered around Vg= 0 at 4 K (Fig. 5.9), which is likely due to the overlap between the small edge gap and bulk valence band. Information about a material's electrical structure is contained in the gate voltage (Vg) dependency of resistance. We measure the 1f and 2f voltages using an AC current that is supplied into ML-WTe2 at 4K with a rms magnitude of 3uA and a frequency of 13 Hz. Figure 5.8.a plots the Vg-dependent 1f resistance from channel 4-7 of device D1 which probes the edge conduction at low temperatures. In line with other studies and our finding in the previous section, only a very broad peak is seen around zero gate voltage, indicating

the absence of any detectable gap close to the charge neutral point in the edge states. Figure 5.9.b summarizes the out-of-plane magnetic field Hz dependence of the 2f voltage signal at selected Vg's. It is evident that at high gate voltages, the size of the ANE hysteresis loop is greatly reduced. In Figure 5.9.c, which displays more richer structures than the 1f signal, we describe the Vg-dependence of magnitude of the 2f voltage hysteresis. In order to fully understand the detailed Vg-dependence, the Berry curvature of the electronic band need to be calculated, and AHE conductivity, as well as ANE coefficient, need to be studied.

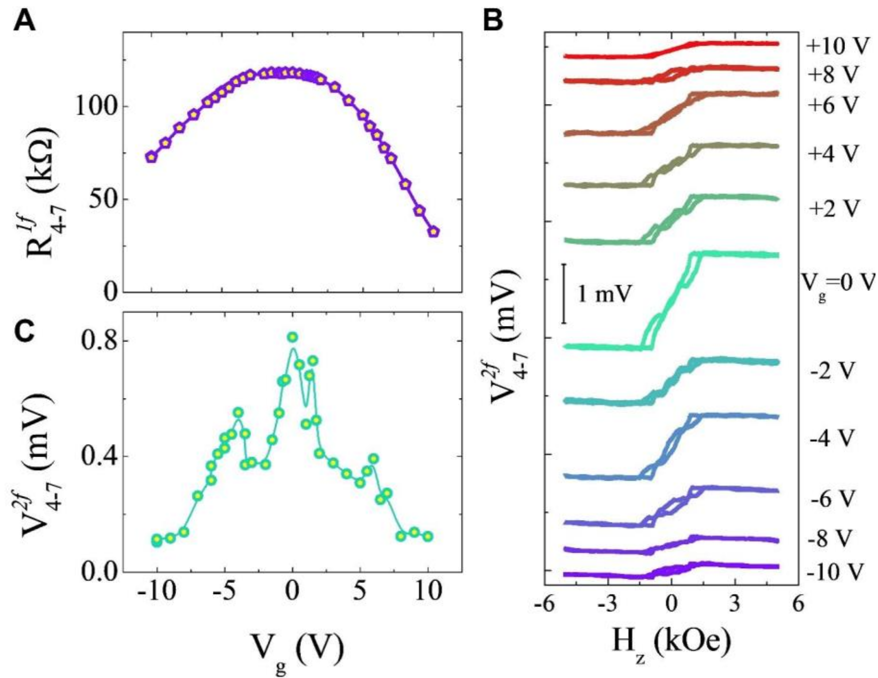

Figure 5.9: Gate voltage dependence of 1f resistance and 2f voltage from 4-7 channel of device D1 at 4 K. (a) 1f resistance from 4-7 channel of device D1 as a function of bottom gate voltage Vg. (b) Out-of-plane magnetic field dependence of the 2f voltage at selected gate voltages. $V4{-}72f$ is measured while an AC current with rms magnitude of 3 uA and frequency of 13 Hz is fed in 3-8 channel. (c) Gate voltage dependence of the magnitude of $V4{-}72f$.

5.2.9 Discussion

After successfully disentangling the two-component transport behavior, now we discuss implications of these observations. It was previously known that in channels longer than 100 nm [89,137], the smaller than quantized 1D conductance indicates that the QSHI edge states suffer from backscattering possibly due to inhomogeneous bulk states [150,151]. Thus, the 1D gapless edge transport is diffusive. However, a strictly 1D system should not produce any diffusive transverse transport responses such as AHE or ANE signals. The unequivocal $2f$ responses suggest that the edge of our ferromagnetic QSHI is likely a quasi-1D system with finite width. We note that the smaller bulk gap in our ML-WTe_2 leads to a wider edge channel. Therefore, these quasi-1D QSHI edge states can produce their own AHE and ANE signals that are different from the bulk counterparts. An interesting alternative scenario is the edge nonreciprocity arising from the broken TRS. Although the nonreciprocal edge transport may explain the observed $2f$ hysteresis, it is not obvious how this mechanism can reconcile with the low temperature $2f$ sign change.

5.2.10 Summary

In summary, we have demonstrated proximity-induced ferromagnetism in ML-WTe_2 using the vdW heterostructure approach. By bringing monolayer 1T' WTe_2, a two-dimensional quantum spin Hall insulator, and few-layer $Cr_2Ge_2Te_6$, an insulating ferromagnet, into proximity in an heterostructure, we introduce an interfacial exchange interaction to transform the former into a ferromagnetic quantum spin Hall insulator, manifested by the

anomalous Nernst effect, anomalous Hall effect as well as anisotropic magnetoresistance effect. When driven by an AC current excitation, the second harmonic voltage responses closely resemble the anomalous Nernst responses to an AC temperature gradient generated by a nonlocal heater, which appear as nonreciprocal signals with respect to the magnetization orientation. Using local electrodes, we identify separate transport contributions from the metallic edge and insulating bulk components. In the absence of TRS in this magnetized QSHI, we find that the edge channel acquires finite ANE responses, distinguishing itself from the ideal 1D chiral or 1D helical edge channels.

Chapter 6: Outlook

We have been able to manufacture a variety of devices with amazing performances thanks to the discovery of many two-dimensional materials and the swift development of controllable fabrication techniques during the past ten years. These techniques led us to discover and confirm the quantum spin Hall insulator (QSHI) state of 1L WTe_2. It makes it possible for QSHI to exist outside of a quantum well in nature. Following this, 1L WTe2 was shown to be a superconductor, while 2L WTe2 was discovered to be ferroelectric. The immense potential of two-dimensional materials is reflected in these. The constructed phase diagram of 1L WTe2 makes us reconsider the ground state of 1L WTe2. I focus on the nature of electronic states and possibility of excitonic condensation in 1L WTe2 in this thesis. The exploration of correlated topological states may find a new direction with a deeper knowledge of the ground state in 1L WTe2, where the interaction of the excitonic insulator phase, topology, and superconductivity. Additionally, because ferroelectricity must be taken into account in this theoretical framework, this research is made more difficult by 2L WTe2's potential as an excitonic insulator candidate. The variety of phases in 1L and 2L WTe2 extends the possibility of electronics from the perspective of applications. In this thesis, we have discussed two measurement techniques to study van der Waals systems: capacitance sensing measurement and contactless microwave impedance measurement in Chapter 4. There are many promising directions for both techniques to explore in the near future. The ability to access the electronic compressibility allowed us to measure and study the band gap associated with strongly correlated phases at zero magnetic field in addition to

exploring the magnetic field dependence. In chapter 4, we discussed about the broad change in moving from conduction band into the WTe2 gap although we can't see this broad feature in KPFM measurement which needs to do more study to access the WTe2 electronic structure. In addition to monolayer WTe2, also bilayer WTe2 due to its exclusive behavior, and moire material can be great chance to study with these techniques. Ferroelectricity of 2L WTe_2 paves the way for potential ultrathin nonvolatile memory applications. Additionally, there are other classes of materials which would be fascinating to study with compressibility and tunneling. Studying the carrier-density and temperature dependence of two-dimensional topological insulator would be a worthwhile venture.

In the last chapter, I discussed about the how proximity-induced ferromagnetism in ML-WTe2 using the vdW heterostructure approach and introduce attempts to enrich fabrication methods to get the cleaner interface. Next step in study the ML WTe2, can be interesting to study the behavior of monolayer WTe2 by putting anti ferromagnetic material like Cr2O3 and see how proximity can affect its behavior. Also, checking the properties of few layer WTe2 which has strong spin orbit coupling can be interesting too.

The interest in two-dimensional and layered materials is growing as a result of new fabrication techniques and dimensions to examine. There are numerous prospects for us to delve into unexplored scientific waters and unearth 2D materials that are technologically advantageous. By using the capacitance technique to study the compressibility and density of state could illuminate this interesting topic and would provide a useful guidepost by allowing direct comparison of the compressibility to the density of states.

Appendix A

Resist-free transfer technique

The development of the resist-free pickup technique [104] has improved the quality of devices by orders of magnitude. The graphene flakes encapsulated between two hBN layers are very clean, since during the fabrication, graphene flakes do not contact any resist or solution. The main challenge is the bubbles' formation at the graphene/hBN interfaces.

A-1 Assembly of hBN/graphene/hBN stacks

To fabricate hBN/graphene/hBN heterostructures, we start with exfoliating graphene on Si/SiO2 substrates as described in chapter 2. The exfoliating and pre-cleaning of hBN flakes on Si/SiO2 follow the same procedures described in section 2.2.1. As shown in Figure A-1, the stamp consists of a base made out of a standard glass slide. On top of this, we place a small square section of polydimethylsiloxane (PDMS) polymer, about 0.75 in long on a side, in the center of the glass slide. With this complete, we spin coat a thin layer of polypropylene carbonate (PPC) polymer onto the stamp at 6000 rpm for 40 s with a 1000 rpm/s ramp. We then heat the stamp at 180°C for 5 min on a hotplate in order to let the PPC set. To make the PPC sticky enough on the PDMS we first do the PDMS slide the oxygen cleaning with the ICP with the recipe as O2 flow 90 sccm, 80mTorr power, RF power 200 Watt, and ICP power zero for 2 minutes and 30 seconds.

The glass slide with PDMS/ PPC is then inverted and attached to a home-built micromanipulator as shown Fig A-1. a. Then the prepared glass slid and the hBN flake on Si/SiO2 substrate are aligned and put into contact with each other by the micromanipulator. The Si/SiO2 substrate is then heated up to 40◦C. After reaching the desired temperature, the glass slide is lifted slowly. At this point, the hBN flake will be picked up from the Si/SiO2 substrate and attached to PPC. Then the process is repeated to pick up a chosen graphene flake on substrate at temperature 60 ◦C, as shown in Fig A-1. d. As discussed earlier; the main challenge of this technique is to reduce the bubbles formed at the interfaces between layers. To reduce the number of bubbles, the process of bringing hBN into contact with graphene needs to proceed as slowly as possible, during my fabrication, the contact front line of hBN and graphene moves at the rate of ∼ 1 μm/min, and make them in contact from one edge and let the temperature bring the rest in contact. Since the melting temperature for PPC is around 80 ◦C, you cannot follow the same temperature as PC recipe. After picking up the graphene flake, the stack on the glass slide is shown in Fig. A-1.c with the graphene/hBN stack on PPC. Next, we need to pick up another hBN and isolate the graphene layer from graphite gate as you can see in Fig. A-1. d. The last step is to transfer the stack onto the chosen graphite flake by repeating the above procedure, which should proceed slowly to reduce the bubbles' formation. Finally, the substrate is heated up to 90 ◦C, when PPC melts and detaches from PDMS, leaving the whole hBN/graphene/hBN/ graphite stack on Si/SiO2 substrate. The sample is then washed in an acetone bath for 30 min to 1 hour in order to ensure complete removal of the PPC, and then 30 min of IPA to get the clean device. The optical image of a typical stack is shown in Fig.

A-1. The hBN/graphene/hBN stack is then annealed at 400 ◦C for 2.5 hours in H2 (0.53 sccm) and Ar (4 sccm) mixture. We note that the annealing process could reduce the number of bubbles and make the stack flatter.

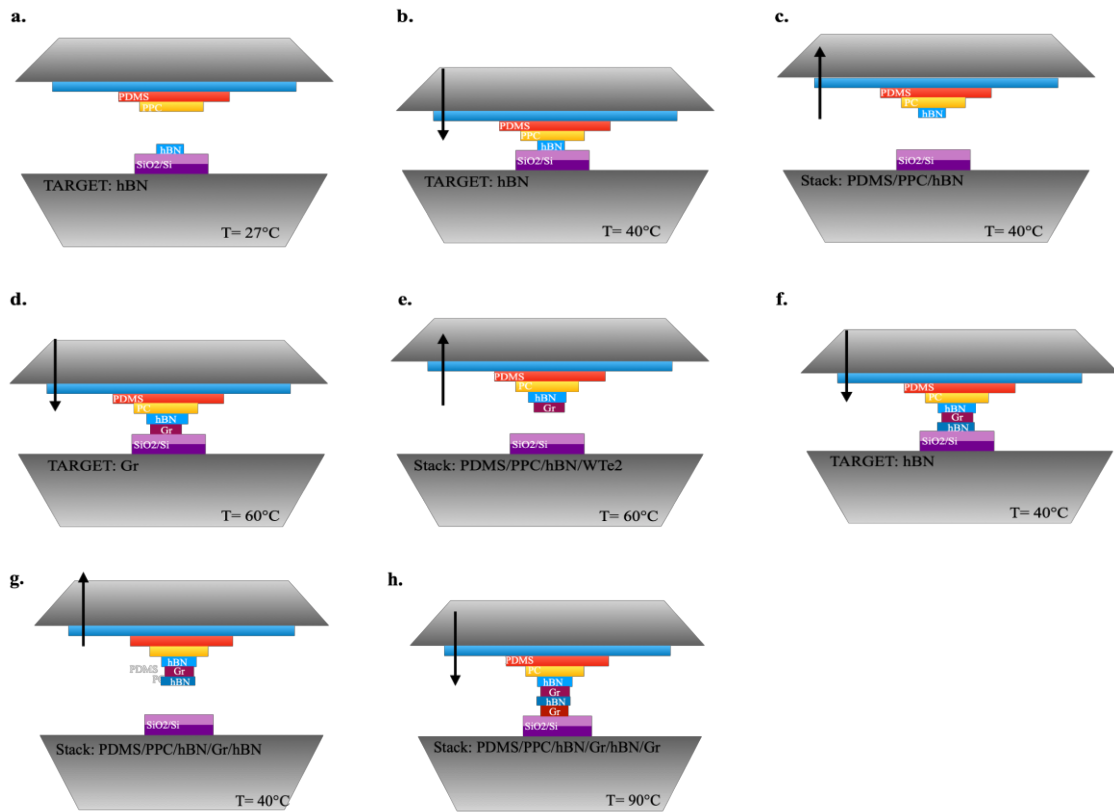

Figure A.1: (a) A prepared microscope slide with PDMS and PPC is used to pick up a hBN flake on Si/SiO2 substrate. (d) The hBN flake is used to pick up a graphene flake on Si/SiO2. (f) try to pick up another hBN at 40◦C (h) The hBN/graphene/hBN stack is transferred onto a Gr flake resting on Si/SiO2 substrate.

Once encapsulated, the challenge is to make contact to the graphene sheets. One dimensional contact has been demonstrated to be a very stable and effective approach to achieve high quality graphene devices [104,152–154].

To fabricate hBN-encapsulated graphene devices, we first follow the same procedures described in chapter two to define metalized alignment marks. Figure A-2 shows the process to fabricate the Hall bar geometry. Firstly, we spin coat two layers of PMMA, as shown in Fig. A-2. b. Using EBL and developing in MIBK afterwards, we define a Hall bar mask on the stack, as shown in Fig. A-2. d. Then we use the ICP etcher to etch away the exposed portion of the stack with SF6 plasma, leaving a Hall bar geometry on the chip (Figure A-2. (e-f)). The RF and ICP generator powers are 50 W and 600 W, respectively. The etching time is ∼ 13 seconds under the pressure of 20 mTorr. Etching time needs to be adjusted according to the thickness of the stack. Finally, we need to put the chip in Acetone to remove the PMMA, but to have a cleaner device it's worth to use the UV light to break the bonding between PMMA polymer. We use the UV light chamber for 10 minutes and then putting the chip in warm acetone (65 ◦C) for at least 1h to remove the PMMA layers.

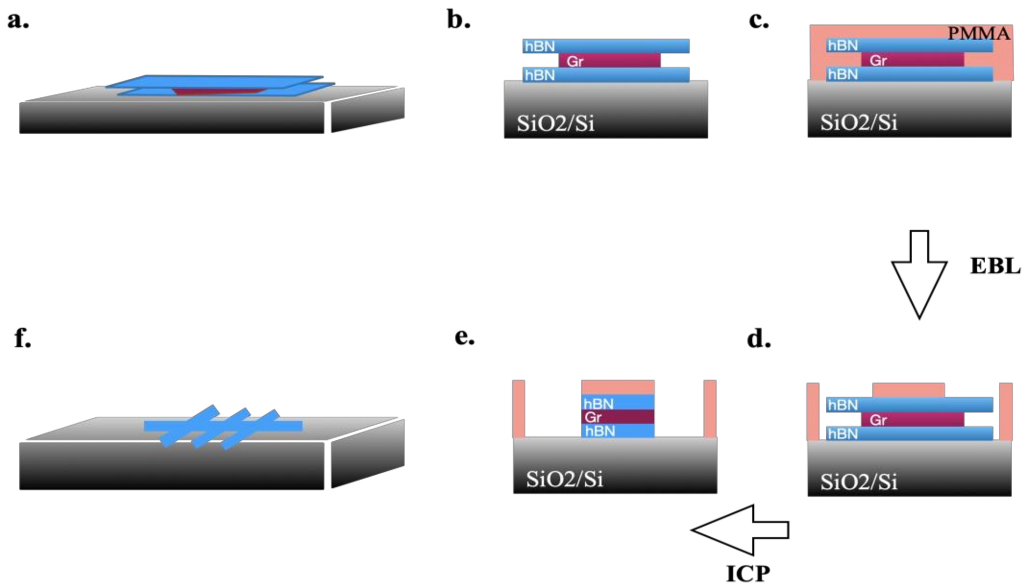

Figure A.2: (a) A completed hBN (light blue)/Gr (deep red)/hBN stack on SiO2 substrate. (b) The cross-sectional view of the stack in (a). (c) Two layers of PMMA (pink) are spin coated on the chip. (d) The open window of Hall bar pattern after EBL and developing in MIBK. (e) The stack is etched in ICP etcher with SF6/O2 plasma. (f) The completed Hall bar after removing the PMMA mask.

Figure A-3 shows the process of making one-dimensional edge contacts to hBN/graphene/hBN heterostructures. After fabricating the Hall bar geometry, we spin coat a layer of MMA and a layer of PMMA, as shown in Figure A-3. a. Then, as shown in Figure A-3. b, we use EBL to expose the edges of the Hall bar terminals. We note that a weak O2 plasma treatment before metallization can improve the contact of devices. We put the chip in ICP and treat the stack with O2 plasma with RF generator power to be 50 W and ICP generator power to be 0 for ~ 10 seconds. Finally, we immediately deposit Cr/Au with thickness of 5/50 nm onto the stack with e-beam evaporator.

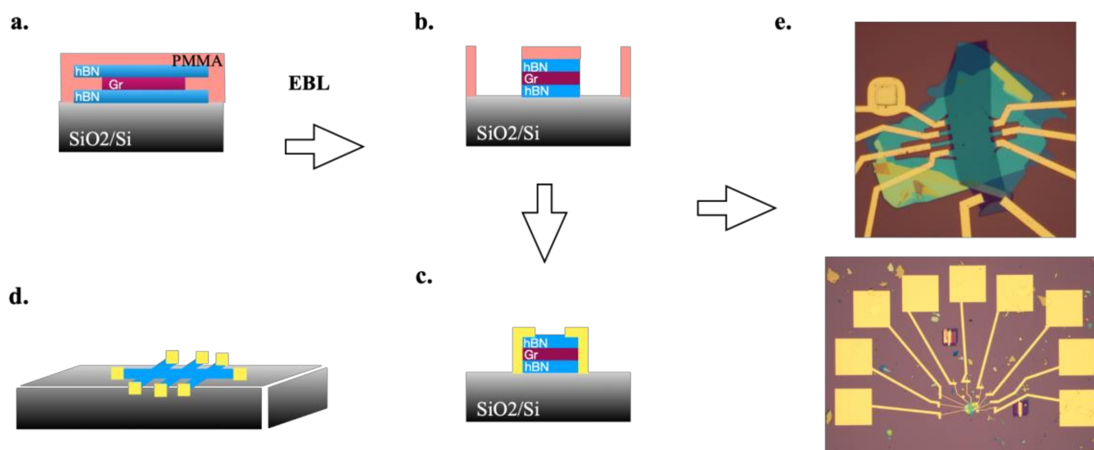

Figure A.3: (a-c) Two layer so PMMA (pink) are spin coated on the chip. (b) The edge of the Hall bar are exposed by EBL and developing in MIBK. (c) Metal electrodes (yellow) are deposited onto the Hall bar edges. (d) Schematic of a Hall bar device with electrodes. (e) The completed Hall bar hBN/Gr/hBN/graphite gate.

Appendix B

Cryogenic HEMT Amplifiers

The cryogenic amplification stages used in this thesis were mounted on the same chip carrier as the sample. We spoke about how crucial it is to lower the input parasitic capacitance in impedance bridge setups in Chapter 3. We use the Fujitsu FHX35X, an unpackaged high electron mobility transistor (HEMT), as a flexible low temperature amplifier to lower the input shunt capacitance, as initially developed in [114]. It bridges the significant impedance differential provided across the balancing point and signal line going to room temperature, delivering significant power gain, even though it is frequently operated with unity or sub-unity voltage gain. It significantly simplifies the measurement process by isolating anything below the balancing point.

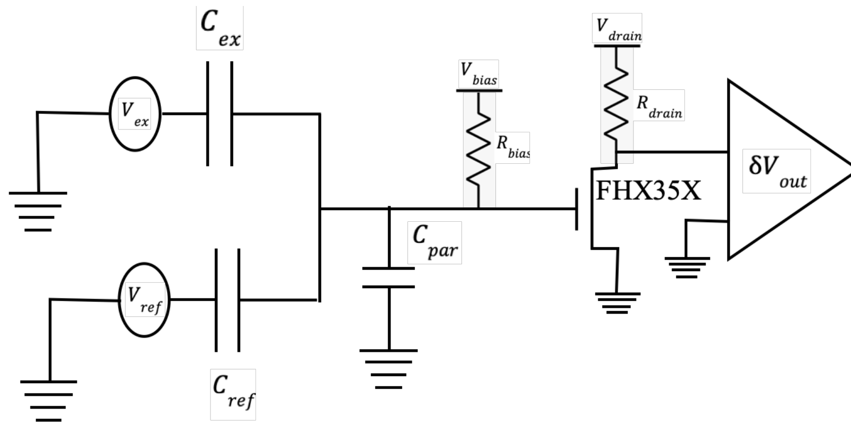

Figure B.1: The common-source Fujitsu FHX35X HEMT is used in the single-stage HEMT amplifier. R_{drain} is typically 1 kW, and R_{bias} is 100 MΩ.

B.1 Single-Stage Design

As seen in Figure B-1, the fundamental HEMT amplifier employs a single HEMT in a common-source design. The HEMT's gate is where the balance point is formed. A DC voltage is delivered through the resistor R_{bias} in addition to the AC excitation that is capacitively linked to the balancing point. There are two uses for this DC voltage. First, it enables us to cut off the HEMT's channel, making its operational point more delicate.

Second, we can adjust the carrier density by applying DC gate voltages across our capacitance device and determining the DC voltage at the balancing point. The measurement circuit's low-frequency cutoff is set by the bias resistor, and the total capacitance at the balance $C_{\Sigma} = C_{ex} + C_{ref} + C_{par}$. The accumulated charge on the balancing point, which is synchronous with the excitation, is shunted to ground through R_{bias} at measurement frequencies below $R_{bias}C_{\Sigma}$ before it can be amplified and carried to room temperature. For van der Waals devices, $C_{\Sigma} \sim 1$ pF so we typically set $R_{bias} \sim 100$ MΩ in order to ensure the roll off frequency f $\sim$ 1kHz. This ensures that we are able to measure successfully in the $10 - 100$ kHz range. To access the compressibility rather than the in-plane conductivity, low frequencies are required to ensure that the sample charges on each cycle of the excitation (see Chapter 3 for details). The drain resistance is selected so that the HEMT's output impedance is of low enough order to drive the signal to room

temperature along the significant capacitance from the coaxial cabling of the cryostat, which is of order 0.5 nF. The HEMT resistance must satisfy

$$R \leq \frac{1}{2\Pi} (100 \text{ kHz}) (0.5 \text{ nF}) \sim 1\text{k}\Omega$$

for a measurement frequency in the 100 kHz range.

B.2 Double-Stage Design

The FHX35X can be split in half and a double-stage cryogenic amplifier can be used, as initially explained in Misha Brodsky's thesis, to lower the input shunt capacitance [155]. In Figure B-2, the entire double-stage circuit is depicted. The gain of the cleaved transistor can be increased much higher than that of a singlestage amplifier despite having a smaller input capacitance. To further reduce the shunt capacitance, we additionally employ a cleaved transistor in place of the bias resistor because it has a lower stray capacitance (150 fF) than a standard thin film resistor (1 pF). A standard single-stage HEMT amplifier using a previously described uncleaved HEMT serves as the amplifier's second stage. The first stage amplifier may be pinched off substantially more than the output stage because it is just driving a small load (only the parts preceding the uncleaved transistor across a brief wire bond length). This provides greater gain without the previously described effects of output loading. Typically, the value of R1 is chosen around $1\text{k}\Omega$, similarity to the single-stage amplifier. The cleaved transistor cH2 which biases the gate of the cleaved measurement transistor cH1 is typically pinched off to around $10 - 100$ MΩ. Due to the

great sensitivity of the DC operation point, the cleaved transistor that serves as the biasing resistor for the first-stage amplifier is typically most prone to introducing noise into the experiment. The noise broadcast into the input of the amplifier in the relevant audio spectrum is greatly reduced by connecting cold cryogenic low-pass RC filters manufactured from standard surface mount components in line with both the DC line going to the biasing transistor's gate and the DC line going to its drain.

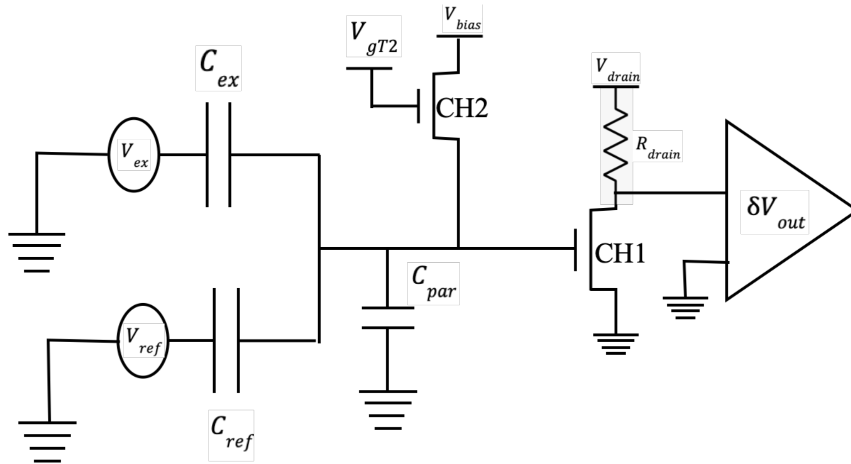

Figure B.2: In order to minimize the input shunt capacitance, the double-stage HEMT amplifier employs a first stage made up of a cleaved measurement transistor (cH1) that is pinched off by another cleaved transistor (cH2). The signal is transmitted to the following amplification stage over a lengthy capacitive cable load by the second stage, which consists of an uncleaved transistor.

B.2.1 Cleaving Transistors

The Fujitsu FHX35X can be cut in half when it's not bundled. The entire, uncleaved HEMT on the right is represented by the cleaved HEMT on the left. The uncleaved HEMT has labels for the gate, source, and drain. Where to cleave is indicated by the star.

As seen below, the Fujitsu FHX35X can be simply disassembled using standard laboratory equipment.

1. Set an unlatched HEMT on a spotless glass slide so that it is facing up.

2. Cover the HEMT with a tiny drop of PMMA to thoroughly encapsulate it.

3. Hold off until the PMMA has had time to cure in the air (or on a hot plate set to 100 C).

4. Position the glass slide under a long-range microscope, particularly one made for use with fine electronics.

5. Place a razor blade's tip.

6. The HEMT will cleanly break into two pieces with a respectably high yield if you press the razor down forcefully. The cleaved HEMTs won't be able to fly off the glass slide because to the encasing PMMA.

7. Carefully remove the PMMA film from the glass slide using tweezers, then drop the entire piece into a beaker of acetone to dissolve it.

8. Sonicate using isopropanol first, then acetone.

9. Tweezers cannot be used to remove the split HEMTs because they are too tiny. Pitch after pitch most of the solvent, then pour the remaining liquid onto a fresh fabrication wipe and let it air dry.

10. The cleaved HEMTs can now be picked up and saved for later usage with tweezers.

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