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PROPOSED THIN FILM ELECTRONICS FOR A-SI:H PIXEL DETECTORS

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**Authors**

Perez-Mendez, V.
Cho, G.
Fujieda, I.

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**Proposed Thin Film Electronics for a-Si:H PIXEL Detectors**

V. Perez-Mendez, G. Cho, I. Fujieda,
S.N. Kaplan, S. Qureshi, and R.A. Street

April 1989

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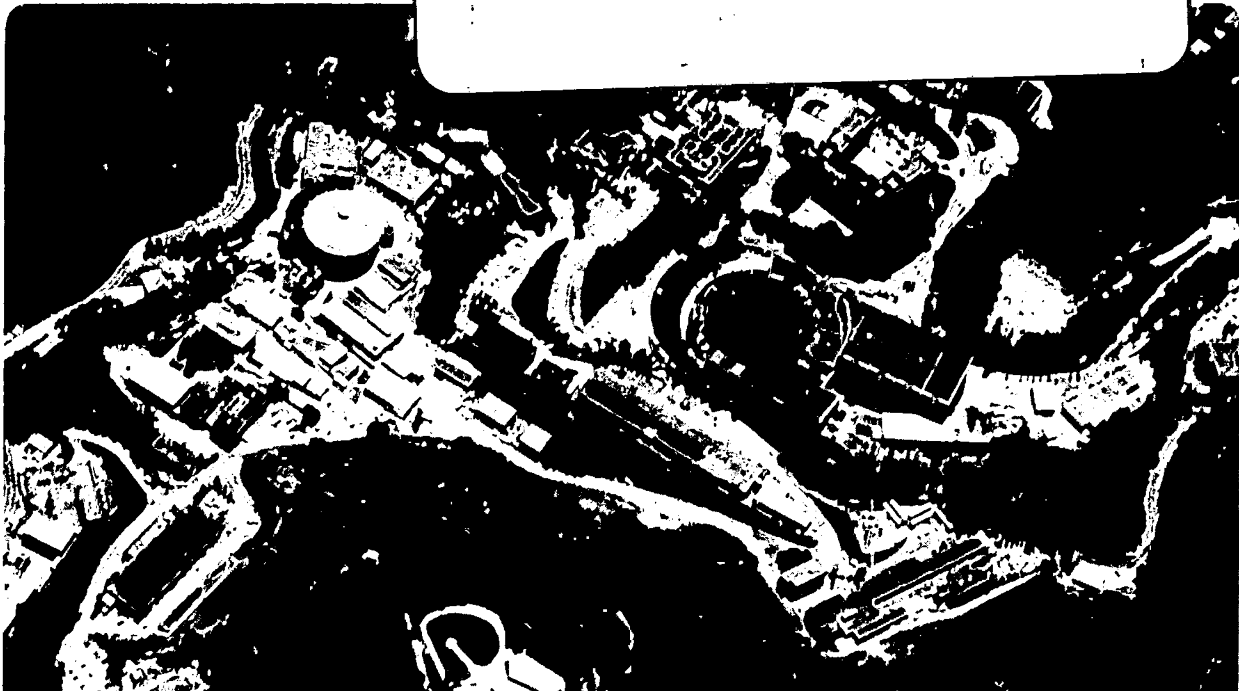

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# Proposed Thin Film Electronics For a-Si:H PIXEL Detectors

V. Perez-Mendez, G. Cho
I. Fujieda, S.N. Kaplan, S. Qureshi

Lawrence Berkeley Laboratory, University of California
Berkeley, California 94720

and R.A. Street

Xerox Palo Alto Research Center, Palo Alto, California 94305

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## I Proposed System

We describe a proposed 2-D PIXEL detector and its electronic circuit. The dimensions of each PIXEL are 300 x 300 $\mu m^2$. Signal-to-noise ratio is in excess of 8 when connected to an a-Si:H TFT with $g_m$ = 3, and 10 when a polysilicon PMOSFET with $g_m$ = 50 is used. For both cases we assume an RC-CR shaping time of 1 μsec.[1] The signal amplification and readout circuit will be placed under the detector and can consist of 5 or 6 FETs and some passive elements. For these amplifiers we consider the following 3 choices.

1. A-Si:H TFTs with advanced lithographic technique (4 μm)
   a) 4 A-Si:H FET Amplifier
   b) 5 A-Si:H FET Amplifier
2. High temperature polysilicon MOSFETs ( 4 FETs )
3. Vertical a-Si:H TFTs

Table 1 is a summary of the properties of several noncrystalline-Si TFTs. Figure 1 shows a schematic diagram of the 2-D PIXEL array. Figure 2 shows a schematic diagram of the electronics.

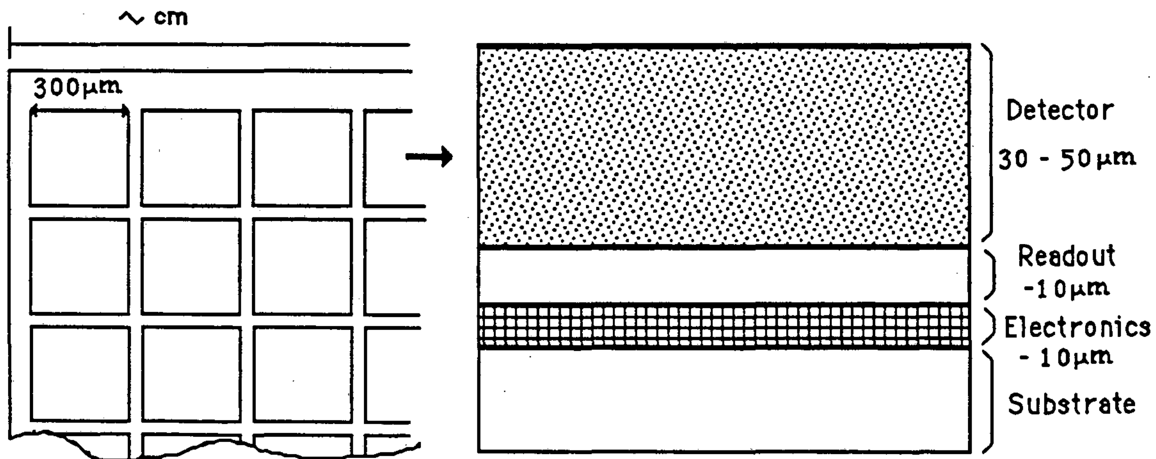


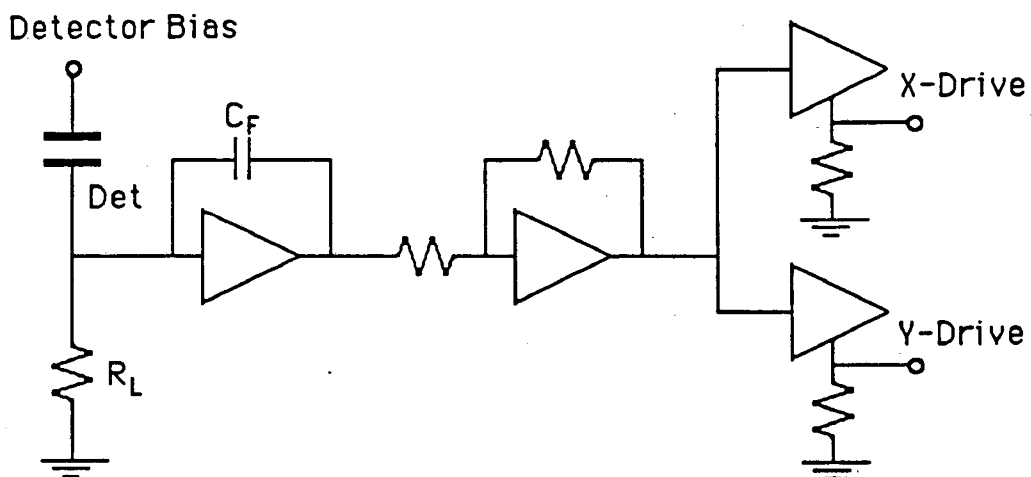

Fig. 1. Schematic Diagram of 2-D PIXEL Array

Table 1 Estimated Properties of Thin-Film-Transistors ( TFTs )

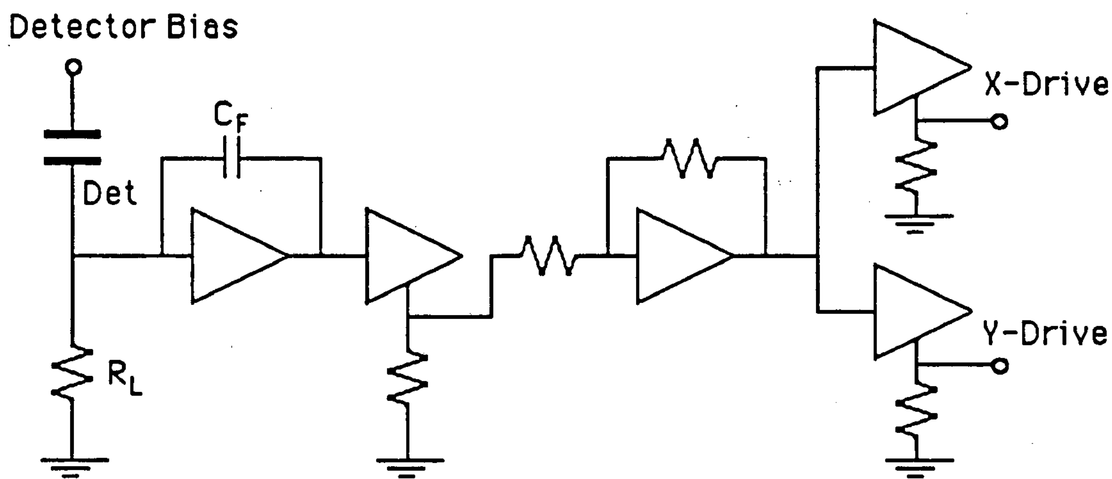
| Type of T.F.T. | Electron Mobility ($cm^2/Vsec$) | W/L | $g_m$ ($\mu A/V$) | Frequency Limit (3db) (MHz) | Noise * (1 μsec) (electrons) | Radiation Resistasnce |
|---|---|---|---|---|---|---|
| a-Si:H 10 μm Tech. | 0.3 - 0.8 | 2-20 | 2 - 4 | 1-3 | ~ 350 | Excellent |
| a-Si:H 4 μm Tech. | 0.3 - 0.8 | 2-50 | 2 - 5 | 3-10 | ~ 350 | Excellent |
| a-Si:H Vertical | 0.3 - 0.8 | 100-1000 | 30-300 | 5-10 | ≥ 1000 | Unknown |
| Polysilicon 400°Anneal | 10-20 | 2-20 | 3-30 | 10-20 | ≥ 500 (expected) | Unknown |
| Polysilicon 900°Anneal | 50-100 | 2-20 | 15-150 | 50-100 | ~300 (PMOS) ~480 (NMOS) | Unknown |
| c-Si on Insulator (SOI) | 1000-1500 | 2-20 | 1000-2000 | > 100 | Same as c-Si FET | Excellent |

* Noise values are given for a typical size of each TFT with 1 μsec CR-RC shaping amplifiers. However these measurements are preliminary because we have not measured enough samples.

## PROTOTYPE AMPLIFIERs

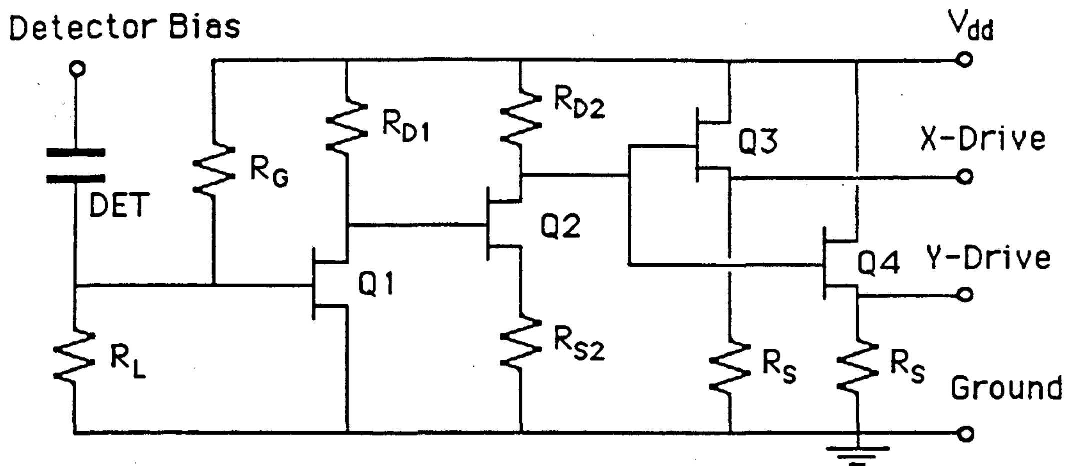



a) 4 FET Amplifier

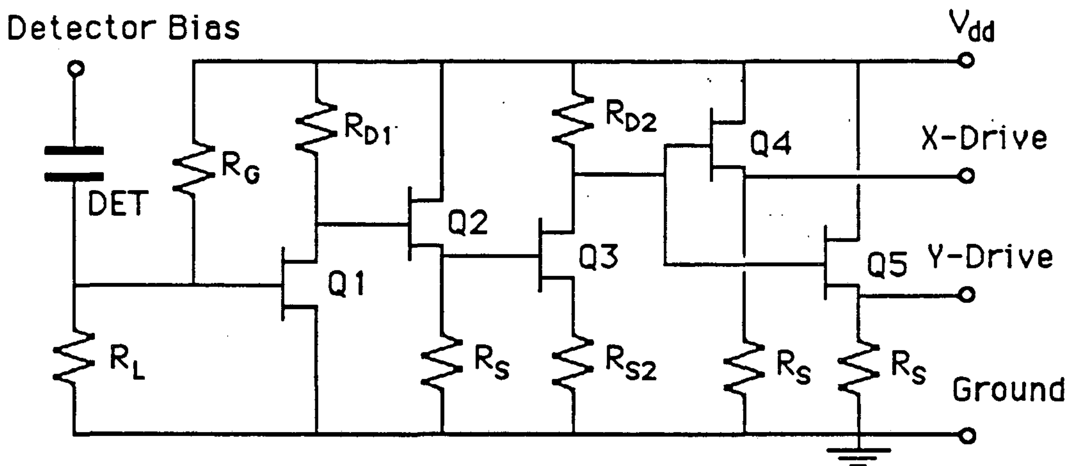



b) 5 FET Amplifier

Fig. 2. Schematic Circuit Diagram of PIXEL Electronics




a) 4 FET Amplifier




b) 5 FET Amplifier

Fig. 3. Amplification Stage for 4 and 5 FET Electronics

## A. Detector

The proposed PIXEL detector has characteristics as shown in table 2. Signal and charge collection are assumed to be generated by minimum ionizing particles.[1]

Table 2 Characteristics of the Proposed PIXEL Detector

| | | |
|---|---|---|
| Size | ($\mu m^2$) | 300x300 |
| Thickness | ($\mu m$) | 50 |
| $C_{DET}$ | (pF) | 0.2 |
| $S_{SIG}$ | (electrons) | 3000 |

## B. Amplifier

Amplification of the signal charge in the 4-FET amplifier is performed by two FETs. Both FETs are operated in the saturation mode which gives a high output impedance, $r_o$, and a low gate-to-drain capacitance, $C_{gd}$, which is mainly due to the overlaping area of the gate electrode over the drain contact.[2] The first FET is used as a charge sensitive preamplifier by using this inherent gate-to-drain capacitance, $C_{gd}$, as a feed-back capacitance, $C_F$. The equivalent circuit of the amplifier stage is shown in Figure 3-a).

The input voltage signal, $V_i$, without the feed-back loop is

$$V_i = \frac{Q_{SIG}}{C_T} \tag{1}$$

where $Q_{SIG}$ is the total signal charge ( $= q * S_{SIG}$ ) and $C_T$ is the total input capacitance of the first stage amplifer.[3]

$$C_T = C_{DET} + C_{gs} \tag{2}$$

$A_v$ is open loop voltage gain given by

$$A_v = -g_m * ( r_o // R_{D1} ) \tag{3}$$

and the gain of the first stage ( charge sensitive ) preamplifier with a capacitive feed back loop is

$$G_1 = \frac{C_T}{C_T + (1 + |A_v|) * C_F} * A_v \tag{4}$$

The output voltage signal of the first stage, $V_1$, is

$$V_1 = \frac{Q_{SIG}}{C_F} * \left( \frac{A_v * C_F}{C_T + (1 + |A_v|) * C_F} \right) \sim \frac{Q_{SIG}}{C_F} \quad \text{when } |A_v| \gg 1 \tag{5}$$

The charge-to-voltage conversion gain $(G_1/C_T)$ can be increased by two methods.

1. By decreasing $C_F$
2. By increasing output resistance

Basically $C_{gd}$ is determined by the overlapping area between gate and drain of the FET, and its value can be made less than 0.02 pF by 0.5 μm overlapping. Also if we underlap the drain, as used in High Voltage TFT designs, then we can expect $C_{gd}$ to be in the range of a few femto farad.

The second method is limited by the frequency response ( RC time constant ) of the device which is determined either by the transit time of electrons in the FET channel or the RC value of the output stage. In our case the transit time is of the order of a few tens of nano seconds, so the latter determines the time response. Since the load capacitance from the next stage is the sum of the gate-to-source capacitance and the Miller capacitance of the 2nd FET, selecting the output resistance of the 1st stage is an optimization problem between gain and frequency response.

In the second stage, the voltage gain, $G_2$, is[4]

$$G_2 = \frac{-(g_o + g_m) * R_{D2}}{1 + (g_o + g_m) * R_{S2}} \tag{6}$$

where $g_o$ is the reciprocal of $r_o$.
Again, $G_2$ is limited by the frequency constraint of the entire circuit because it increases the Miller capacitance.

Finally the total output signal is

$$V_o = G_1 * G_2 * V_i \tag{7}$$

The RC time constant of the amplifier, $\tau$, is a product of the total output resistance of the first stage and total capacitance at that point.

$$\tau = (r_o // R_{D1}) * \{ C_{gs} + (1 + |G_2|) * C_{gd} \} \quad (8)$$

where the second component of the capacitance is increased due to Miller effect at the second stage amplifier.

As a 2nd choice, we propose the 5-FET amplifier scheme shown in Fig. 2-b) and 3-b). In this case we can decrease the RC time constant by a factor of 10 or more because the input capacitance of the 2nd stage ( source follower ) is only $C_{gd}$.

$$\tau = (r_o // R_{D1}) * \{ C_{gs} + C_{gd} \} \quad (9)$$

The 3rd choice is to use a polycrystalline MOSFET amplifier consisting of 4-FETs. In Table 3 we summarize the design parameters for these three choices of FETs and the calculations of the voltage output and RC time constant, $\tau$.

Table 3 Design and Calculated Data for PIXEL Electronics

| Parameters | a-Si:H(4FETs) | a-Si:H(5FETs) | Polysilicon(4FETs) |
|---|---|---|---|
| L (μm) | 8 | 8 | 12 |
| W (μm) | 250 | 250 | 70 |
| $L_o$ (μm) | 0.5 | 0.5 | 0.5 |
| $d_i$ (μm) | 0.5 ($Si_3N_4$) | 0.5 ($Si_3N_4$) | 0.1 ($SiO_2$) |
| $C_{gd}$ (pF) | 0.015 | 0.015 | 0.012 |
| $C_{gs}$ (pF) | 0.18 | 0.18 | 0.21 |
| $V_G$-$V_T$(V) | 10. | 10. | 10. |
| $I_D$ (μA) | 15. | 15. | 207. |
| $\mu_e$ ($cm^2/Vs$) | 0.8 | 0.8 | 20. |
| $g_m$ (μA/V) | 3.1 | 3.1 | 41. |
| $A_V$(Open Loop Gain) | 8.8 | 8.8 | 11.0 |
| $G_1$ | 8.5 | 8.5 | 10.4 |
| $G_2$ | 12. | 12. | 10. |
| $r_o$ (MΩ) | 10. | 10. | 2.0 |
| $R_{D1}$ (MΩ) | 4.0 | 4.0 | 0.3 |
| $R_{D2}$ (MΩ) | 4.0 | 4.0 | 0.3 |
| $R_{S2}$ (MΩ) | 0.1 | 0.1 | 0.01 |
| $V_i$ (mV) | 1.3 | 1.3 | 1.2 |
| $V_o$ (mV) | 130 | 130 | 125 |
| $\tau$ (μsec) | 1.0 | 0.44 | 0.08 |

Vertical types of a-Si:H TFT can be considered as another choice. The advantage of these devices are their high transconductance, $g_m$, and short transit time, $T_t$. Here using 7-10 $\mu$m lithography, channel lengths of 0.3 - 0.5 $\mu$m can be created by depositing the gate, source and drain metal contacts over each other with spacings determined by the deposition process. Transconductance values higher than 100 $\mu$A/V have been reported.[5-7] We did not consider this alternative here since the values of $C_{gd}$, $C_{gs}$, channel resistance and other parameters were not given completely in the reports available to us.

## C. Noise

The proposed detector and amplifier system has primarily six noise sources as shown in figure 4. The current noise sources, $i_{LD}^2$, $i_{SD}^2$ and $i_{FD}^2$ are called parallel noise and they are respectively the thermal noise of detector load resistance ($R_L$), the shot noise due to detector leakage current ($I_L$) and the flicker noise in the detector. The voltage noise sources, $v_{LT}^2$, $v_{TT}^2$ and $v_{FT}^2$ are called series noise and they are also respectively the thermal noise of the amplifier load resistance ($R_{D1}$), the thermal noise of the equivalent channel resistance of TFT and the 1/f noise or flicker noise of the TFT. These noise sources have spectra in the frequency domain and they are summarized in appendix B.

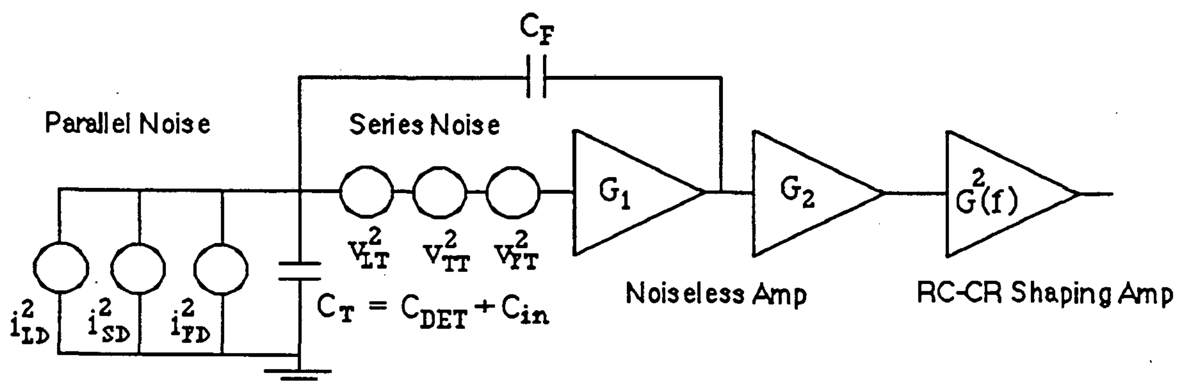



Fig. 4. Six Noise Sources in the Detector and Preamplifier System in the frequency domain when $R_LC_T >> \tau_o$

When a simple RC-CR shaping amplifier with a peaking time, $\tau_0$, is used at the output stage, these noise sources are conveniently expressed by the equivalent input noise charge in the time domain. The procedure is as follows; (1) find the equivalent input noise voltage spectrum of all six noise sources. (2) take an integral of a convolution of the noise spectrum and the transfer functions of the first and second and shaping amplifiers from zero to infinity. (3) divide by the output voltage signal voltage squared from single electron-hole pair which is

$$v_{out}^2 = \left(\frac{q}{e\,C_T}\right)^2 * (G_1 * G_2)^2 \tag{10}$$

where e is the base of natural logarithm and q is an electronic charge. The results are shown in the following equations.

$$N_i^2 = \left(\frac{e\,C_T}{q}\right)^2 * \int_0^\infty \frac{i_i^2(f)}{(2\pi f C_T)^2} * G^2(f)\,df \qquad i = \text{LD, SD or FD} \tag{11}$$

$$N_j^2 = \left(\frac{e\,C_T}{q}\right)^2 * \int_0^\infty v_j^2(f) * G^2(f)\,df \qquad j = \text{LT, TT or FT} \tag{12}$$

where the amplifier gain $G_1$ and $G_2$ are cancelled out and the transfer function of the shaping amplifier, G(f) for simple RC-CR is

$$G(f) = \frac{2\pi f\tau_o}{1 + (2\pi f\tau_o)^2} \tag{13}$$

In the time domain $N_{SD}$ and $N_{TT}$ are called Step Noise and Δ Noise respectively.[1,8] All results are summarized in appendix B. The total input equivalent noise in units of electrons is

$$N_{TOT} = \left(N_{LD}^2 + N_{SD}^2 + N_{FD}^2 + N_{LT}^2 + N_{TT}^2 + N_{FT}^2\right)^{1/2} \tag{14}$$

Finally the signal-to-noise ratio is

$$S/N = \frac{S_{SIG}}{N_{TOT}} \tag{15}$$

Table 4 shows the estimated noise of the system when a RC = CR = 1 μsec shaping time is used.

Table 4 Noise of the Detector and Preamplifier System for 1 μsec CR-RC shaping amplifier

| Noise (e) | | a-Si:H TFT | Poly-NMOS(900°C) | Poly-PMOS |
|---|---|---|---|---|
| $K_f$ | ($V^2/F$) | $1.3 \times 10^{-21}$ | $1.95 \times 10^{-22}$ | $7.0 \times 10^{-23}$ |
| a | | 1.0 | 0.78 | 0.8 |
| $N_{LD}$ | (Thermal noise of $R_L$) | 77 | 77 | 77 |
| $N_{SD}$ | (Shot noise of detector) | 72 | 72 | 72 |
| $N_{FD}$ | (1/f noise of detector) | 7 | 7 | 7 |
| $N_{LT}$ | (Thermal noise of $R_{D1}$) | 24 | 5 | 5 |
| $N_{TT}$ | (Thermal noise of TFT) | 107 | 27 | 33 |
| $N_{FT}$ | (1/f noise of TFT) | 340 | 480 | 280 |
| $N_{TOT}$ | (Total noise) | 370 | 490 | 300 |
| S/N | | 8.1 | 6.1 | 10. |

Among the six noise sources, the amplifier flicker noise turns out to be the dominant one. In order to reduce this 1/f type noise, other types of shaping amplifiers may be used. For example, 1/f noise will be reduced by 10 % when we use a CR- $(RC)^n$ filter for $n > 4$ which simulates gaussian type shaping.[8] Also it will be further reduced by using a time variant active filtering network such as correlated double sampling network which was originally used in charge coupled devices and showed a 6 dB decrease in 1/f noise of FETs.[9-10]

The equivalent noise voltage spectrum from a single TFT is analyzed as a sum of two different noise sources as in the crystalline MOSFET case. The first one is the Nyquist noise ( or the equivalent thermal noise ) due to the finite channel resistance which is expressed as $2/(3g_m)$. The second one is the flicker noise ( or 1/f noise ) which is generally inversely proportional to the frequency with some power $\alpha$.[11]

$$v_{TFT}^2(f) = 4\,kT\left(\frac{2}{3\,g_m}\right)\Delta f + \frac{K_f}{C_i\,WL\,f^{\alpha}}\Delta f \tag{16}$$

Following the process described earlier to express these terms in the time domain we obtain

$$N_{TFT}^2 = \left(\frac{e\,C_T}{q}\right)^2 * \frac{kT}{3\,g_m} * \frac{1}{\tau_o} + \left(\frac{e\,C_T}{q}\right)^2 * \frac{K_f}{2\,C_i\,WL} * F(\alpha,\tau_o) \qquad (17)$$

where $F(\alpha,\tau_o)$ is between 0 and 1. When $\alpha$ is 1, $F(\alpha,\tau_o)$ is 1 and the flicker noise is independent of the shaping time, $\tau_o$. See the formula in Appendix B.

Figures 5 and 6 is the calculation of these two noise contributions in the time domain for a simple CR-RC shaping amplifier for the proposed detector amplifier system. In the calculation, $K_f$ and $\alpha$ for a-Si:H TFT are extrapolated from the noise measurements done on the large sized XEROX a-Si:H TFT shown in section III-D. For the poly-Si MOSFET, the data are taken from our measurements and from a recently published paper by A.G. Lewis.[12] They are shown in table 4. As expected these TFTs were not optimally designed for low noise.

The flicker noise in a-Si:H TFT can be explained by the fluctuations of the density of electrons due to the interaction with the interface states between a-Si:H and $Si_3N_4$ layers and with the gap states in the channel region. The fact that the field effect electron mobility is lower than the bulk mobility is also attributed to these states. This phenomenon is also present in crystal Si MOSFETs. Better TFT can be possibly made in the future as the deposition techniques improve. A reduction of 1/f noise and an increase of the field effect electron mobility can be expected when the density of these states is decreased.

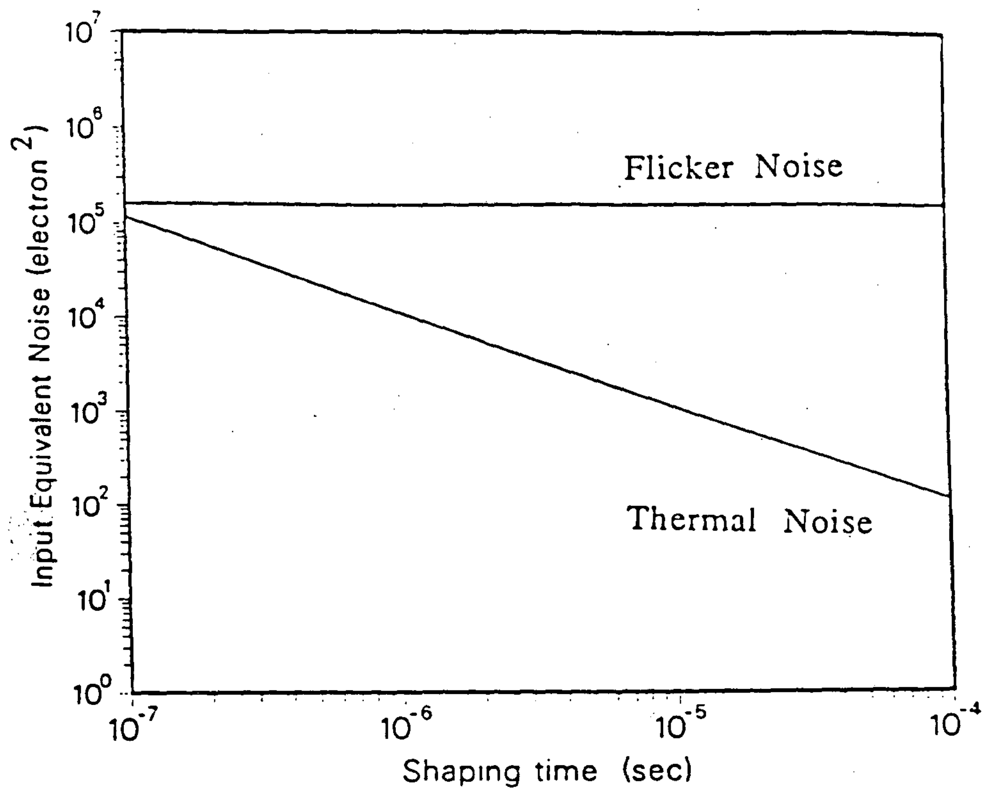



Fig. 5. Input equivalent noise of a-Si:H TFT amplifier in time domain ( $N_{TT}$ and $N_{FT}$ only )

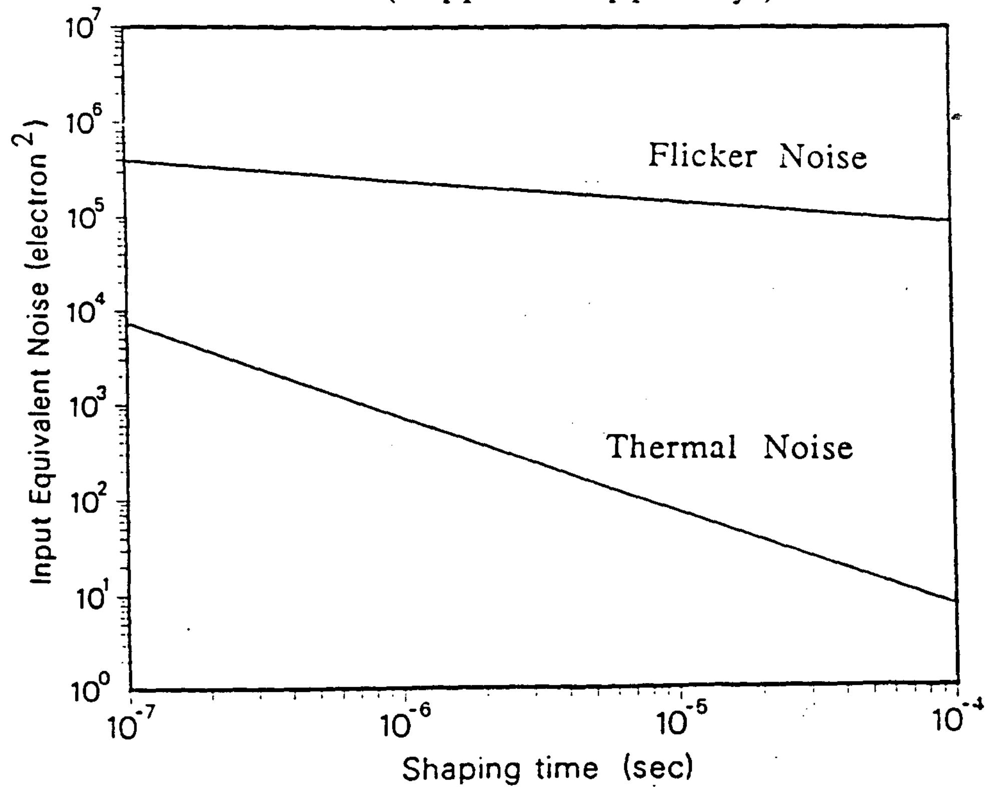



Fig. 6. Input equivalent noise of poly-Si TFT amplifier in time domain ( $N_{TT}$ and $N_{FT}$ only )

## II Description of TFTs

### A. A-Si:H TFT with reduced lithography

One of the differences between TFTs and crystalline Si MISFETs is that these devices are generally operated in the accumulation mode of electrons and the drain and source contacts are on the opposite side of the channel from the gate. Due to this geometry and the low mobility of the electrons, these devices have high channel resistance which allows appreciable open loop gains even though the transconductance is small. Furthermore the drain contact can be underlapped relative to the gate so that the gate-to-drain capacitance can be minimized. This type of structure is used for high voltage TFT.

### B. High Temperature Polysilicon MOSFET

Polysilicon TFTs are under developed now; NMOS, PMOS and CMOS techniques were been achieved recently at XEROX.[12] Polysilicon is annealed at two different temperatures, 900 °C ( high temperature )[12] and 400 °C (low temperature ).[13-14] The only advantage of low temperature polysilicon TFT is the diverse choice of the substrate material. For high temperature anneal polysilicon, a highly thermal resistant substrate, such as quartz, is required. High temperature polysilicon TFT has the following advantages compared to the low temperature variety. 1) Higher mobility gives higher $g_m$, larger voltage gain and faster time reponse. 2) better insulators can be made. ( $SiO_2$ or $Ta_2O_5$[15] ) 3) Lower noise is expected due to the larger grain size. For the proposed PIXEL system, the high temperature polysilicon TFT array would be fabricated on the substrate and then a-Si:H detector would be deposited at about 250 °C.

### C. Vertical a-Si:H TFT

Some of the pioneering a-Si:H vertical TFTs have been designed by M. Hack, et al., at Xerox Palo Alto.[5] Their transconductances vary from 30 to a few hundred and can give high gains. We do not have enough information concerning their dynamic characteristics such as $C_{gd}$ to have considered them in our amplifier design. Figure 7, 8 and 9 show typical configurations for the three types of TFTs.

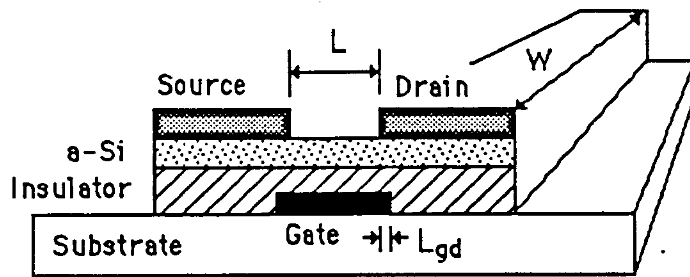



Fig. 7. Configuration of a-Si:H TFT

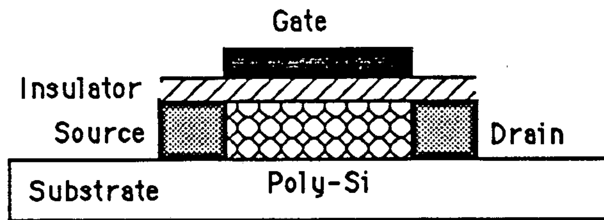



Fig. 8. Configuration of typical poly-Si MOSFET
( Courtesy of A. Lewis )

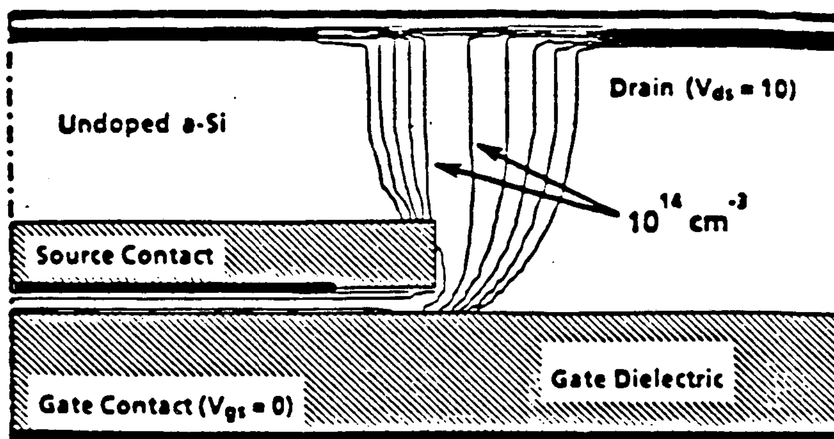



Fig. 9. Configuration of vertical TFT
( Courtesy of M. Hack )

## III Measurements on a-Si:H TFTs

We received and tested some a-Si:H TFTs from Xerox, which have large channel lengths and widths and were designed for switching purpose.

### A. Insulator Thickness

We measured the thickness of the gate insulator, $Si_3N_4$, indirectly by measuring the gate-to-drain capacitance.

$$d_i = \varepsilon_i * \varepsilon_o * \frac{W * L_{GD}}{C_{gd\text{-}Max}} \qquad (18)$$

using the value $\varepsilon_i = 7$ for amorphous silicon nitride.

Table 5 Dimensions of XEROX a-Si:H TFT (1986)

| | | |
|---|---|---|
| W | (μm) | 350 |
| L | (μm) | 20 |
| W/L | | 17.5 |
| $L_0$ | (μm) | 12 |
| $C_{gd\text{-}Max}$ | (pF) | 1.2 |
| $d_i$ | (μm) | 0.22 |

## B. I-V and Transconductance

We also measured the I-V characteristics and small signal parameters ( $g_m$, $r_o$ etc ) of these TFTs. The measured transconductance and drain current are compared with the calculated values by using the following equations.[16]

$$g_m = \mu_e * \frac{\varepsilon_i * \varepsilon_o}{d_i} * \frac{W}{L} * (V_G - V_T) \tag{19}$$

$$I_{DS} = \frac{g_m * (V_G - V_T)}{2} \tag{20}$$

Figure 10 shows the I-V curves and the transfer curve for a typical a-Si:H TFT of Xerox .

As we see from Table 6, the equations originally used for crystalline MOSFET, describe the static characteristics of a-Si:H TFT very well. For calculating $g_m$ and $I_{DS}$, we assumed only one fitting parameter, which is the electron field effect mobility, $\mu_e$, which is within the accepted value in the literature. This channel mobility is 2-3 times smaller than the bulk mobility as measured by the time of flight method. A lower channel mobility is also found in crystalline silicon FETs and is assumed to be due to additional trapping by the surface states between the a-Si:H and the insulator.

Table 6 Static Parameters of XEROX a-Si:H TFT

| | | |
|---|---|---|
| $V_{DS}$ | (V) | 20 |
| $V_G$ | (V) | 17.5 |
| $V_T$ | (V) | 3.5 |
| $I_{DS}$ | (μA) | 112 |
| $r_o$ | (MΩ) | 7.7 |
| $g_m$ | (μA/V) | 1.7 |
| $\mu_e$ | ($cm^2$/Vsec) | 0.25 |

## C. Output Pulse Rise Time

We measured the output pulse rise time of the Xerox TFTs by using various load resistances. We biased the drain at 20 volt through a passive probe with the load resistance directly connected to the probe tip in order to reduce the stray capacitance, and applied 15 volt to the gate. A square wave input pulse was applied to the gate and the output pulse signal was measured by an active probe ( Input capacitance = 0.1 pF ) capacitively coupled to the drain.

For a load resistance of 1MΩ, an RC time constant of 1.7 μsec is measured; we estimate the stray capacitance at the drain in this set-up to be about 1.5 - 2.0 pF. Using a 100 kΩ resistance we observed an RC time constant of 0.178 μsec. Since the transit time of the charge carriers of the TFT is shorter than the RC time, we conclude that the output pulse rise time is dominated by the measured RC time constant.

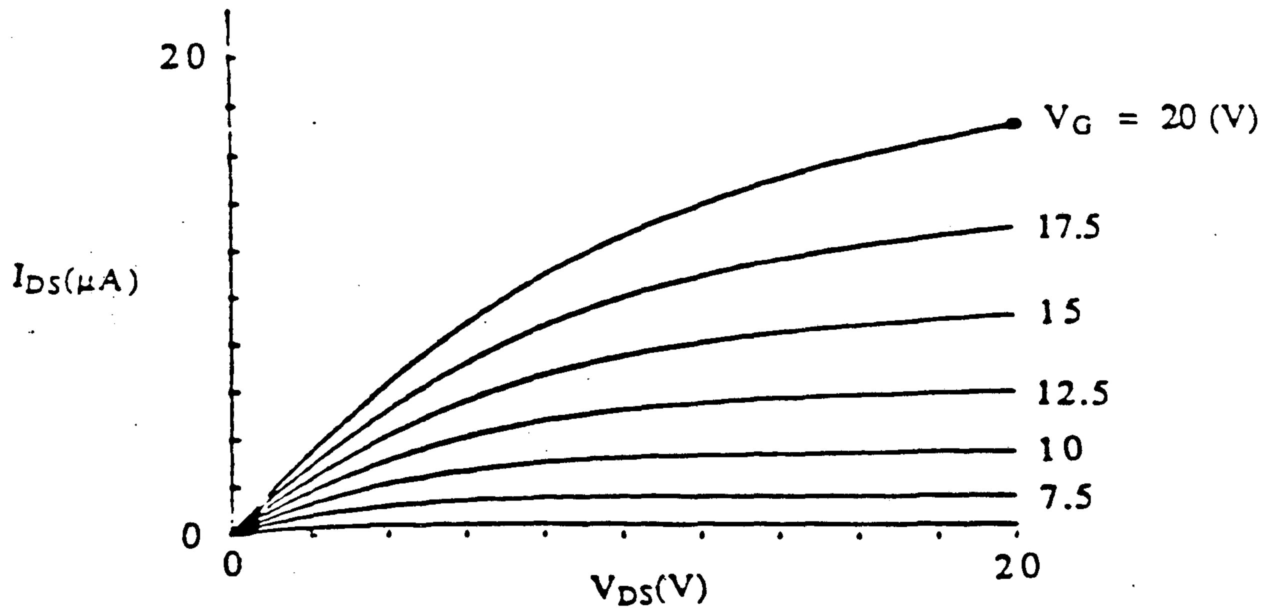
## D. Noise

Finally we measured the equivalent input-referred voltage noise of a-Si:H TFT as shown in Figure 11. The measurement system is described in reference [17]. We measured the drain current fluctuations directly and calculated the input equivalent noise voltage by the following equation.

$$v_{TFT}^2(f) = \frac{i_D^2(f)}{g_m^2}\Delta f \qquad (21)$$

The noise spctrum is measured only up to 500 kHz due to the limitation of the probe station system noise. For a typical XEROX TFT the flicker noise constant, $K_f$ is $1.2 \times 10^{-21}$ $V^2$/Farad and $\alpha$ is about unity. The measurement was done for a TFT which had input capacitance of 1.7 pF and $g_m = 1.6$ μA/V.

With the courtesy of XEROX, we measured I-V curves and the drain current fluctuations for high temperature polysilicon NMOS as shown in figure 12. The measured $K_f$ is $2 \times 10^{-22}$ $V^2$/Farad and $\alpha$ is about 0.78.



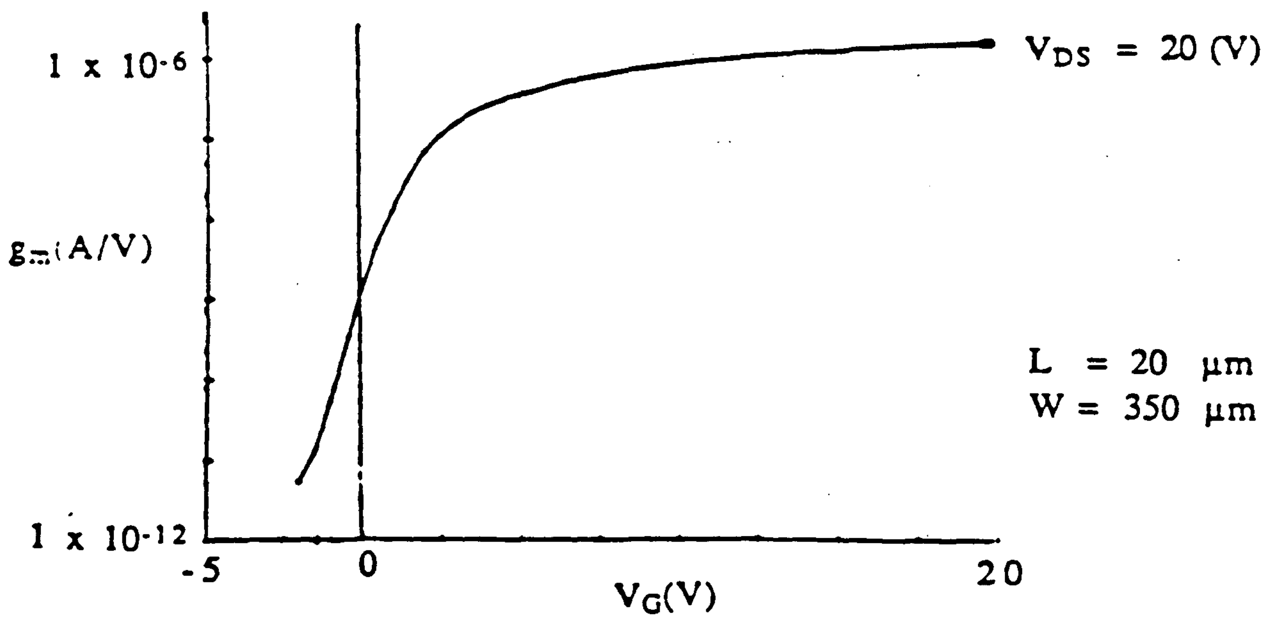
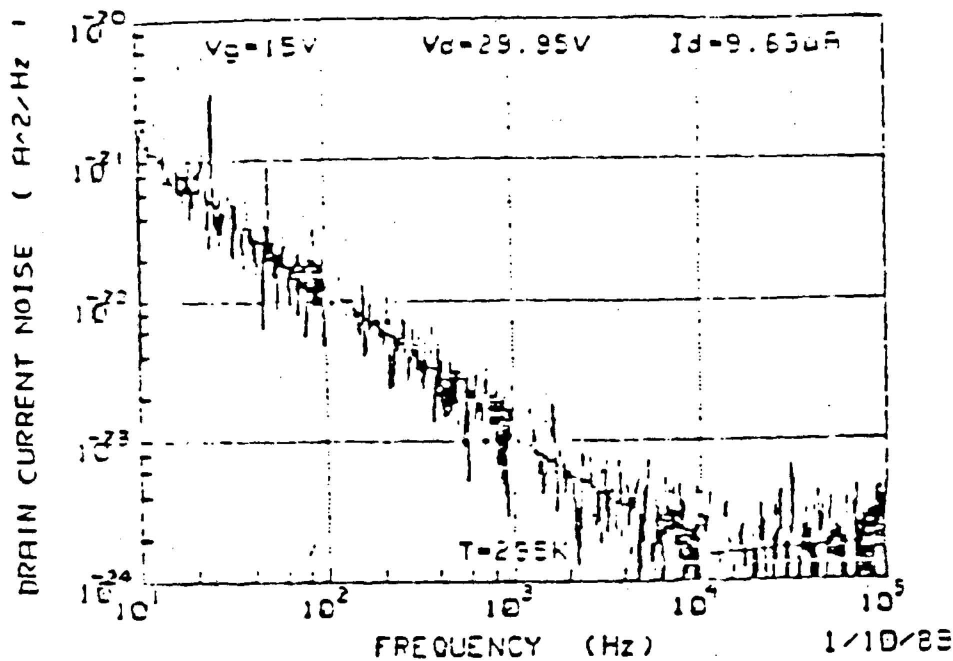




Fig. 10. I-V Curves and Transfer Curve of XEROX a-Si:H TFT



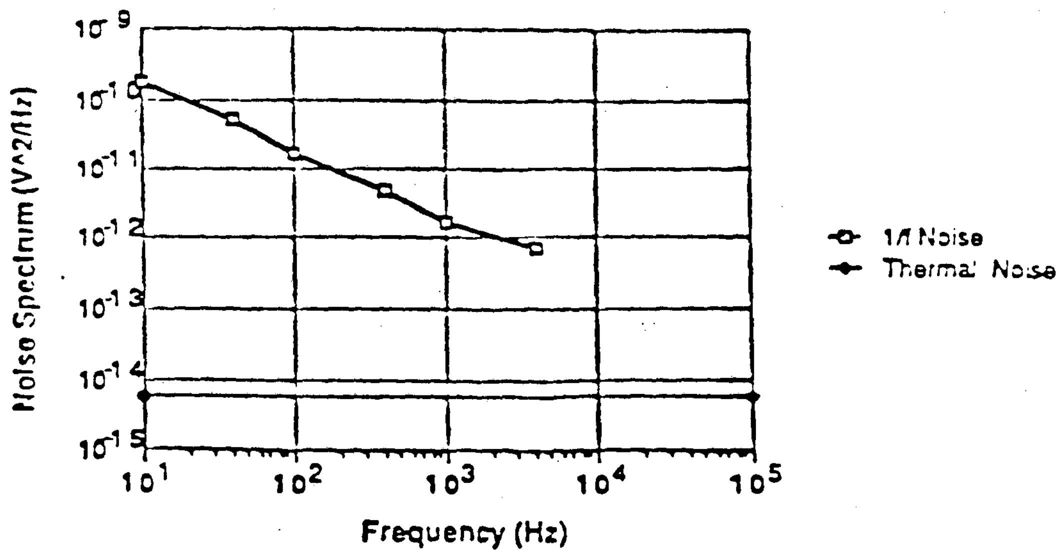
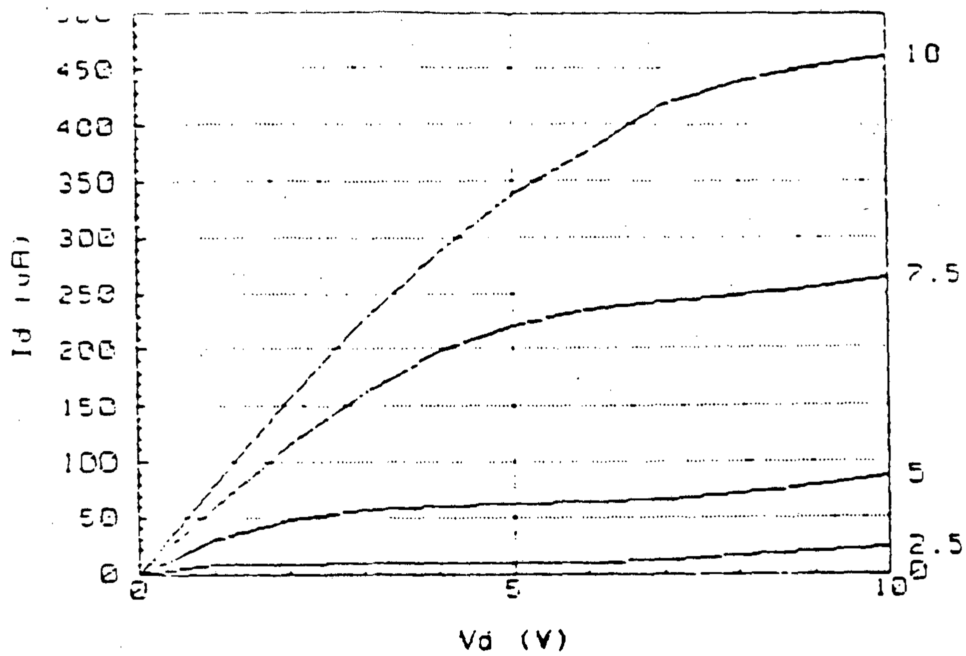




Fig. 11. Typical Input Noise Voltage Spectrum of a-Si:H TFT
(a) Measured drain current noise (the flat part above 10 kHz is due to the limit of system noise.)
(b) Equivalent input voltage noise



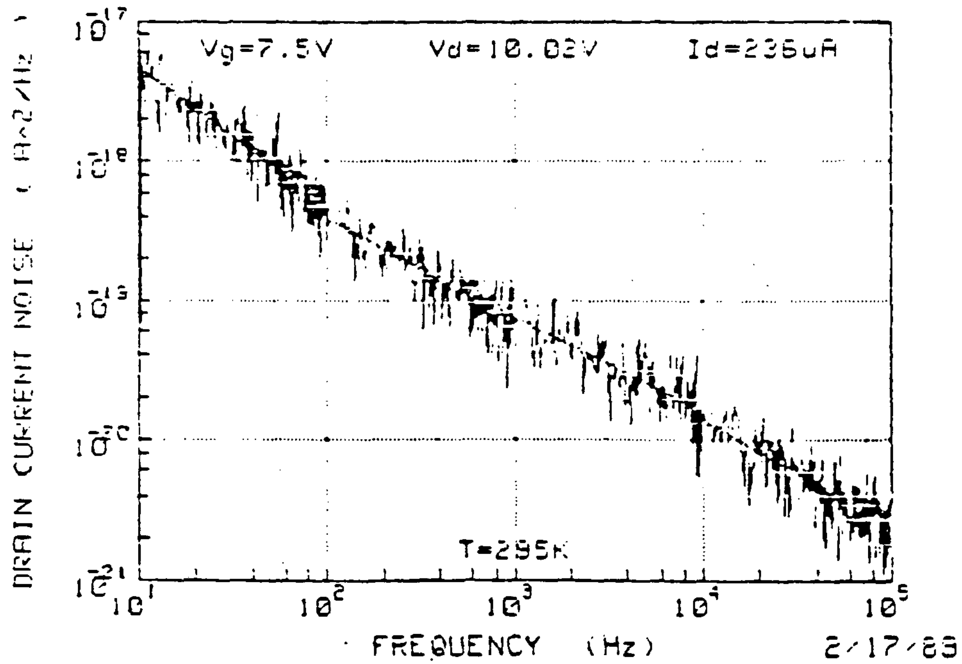




Fig. 12. Measurements on Polisilicon NMOS ( After A.Lewis )
( W/L = 50/10, Annealing at 900 °C )
(a) I-V Curves
(b) Drain current noise ( at $V_g$ = 7.5 V)

## IV Conclusion

This paper is intended only as a design consideration for a proto-type a-Si:H PIXEL array for medical applications and high energy particle track detectors. Various types of thin-film transistors are suggested as electronics candidates. A final design, however, should be made by considering several points which are not known yet like radiation resistance, reliability, yield, and convenience of manufacturing.

In this paper, three sample amplifier configurations are proposed with respect to three important design criteria; amplifier gain, time response and noise. No effort has been made to reduce the power dissipation for the sample system. However, the load resistance $R_d$ could be less than 4 MΩ for a-Si:H TFT when the operating drain current is less than 10 μA. For poly-Si TFT, the resistance could be less than 1 MΩ because the channel resistance is small. We even do not make use of the fact that CMOS techniques are possible for poly-Si TFTs amplifier systems. One additional FET to reset the PIXEL detector is required in the high energy application, which is not shown in figures 2 and 3, but may not be needed in medical imaging applications because of the slow data rate.

As we see, all three proposed amplifier systems have sufficient gain and have acceptable frequency responses. The five a-Si:H TFTs amplifier system has almost the equivalent gain and frequency response as the four polysilicon TFTs amplifier system. Reduced lithography TFTs are available now and the other two techniques are being developed. By extrapolating the RC time constant measurements done on the Xerox TFT (L = 20 μm) to the proposed a-Si:H TFT (L = 4 μm) at the same electric field strength, the transit time of charge carriers in the proposed TFT becomes at least a factor of 5 less than 0.18 μsec, ie., less than 360 nsec. In polysilicon TFT (L = 8 μm), the transit time is less than 100 nsec. So the output pulse rise time is dominated by the RC time constant that we used for the model design.

The noise measurement of the individual TFTs show that the flicker (1/f ) noise will be the dominant noise source in

the designed PIXEL amplifier system. The noise data shown in table 4 are the estimated values when a simple RC-CR shaping amplifier with 1 μsec shaping time is used. In this case the true 1/f noise is independent of shaping time as is well known. It may be reduced by 10 - 30 % by using more advanced shaping amplifiers such as gaussian shaping or time variant active filters such as correlated double sampling networks.

Signal-to-noise ratios of 6 - 10 are estimated with the current technology a-Si:H and with 900 °C poly-Si TFTs. Due to the larger grain size, high temperature poly-Si TFT ( 900 °C ) is considered the better choice than low temperature poly-Si TFT ( 400 °C ). Since PMOS devices show lower noise than NMOS,[12] the future design of PIXEL amplifiers is possible by using CMOS poly-Si technique with a PMOS input stage. A reduction of flicker noise and an increase of the field effect mobility of both a-Si and poly-Si TFTs can hopefully be achieved in future because the process technique is still new and undergoing improvements.

We want to thank Dr. M. Hack and Dr. A. Lewis from Xerox at Palo Alto for sending sample TFTs to test. We also would like to thank K. Lee, D. Landis, F. Kirsten, and S. Parker for useful discussions on PIXEL amplifiers. This work was supported by the Director, Office of Energy Research, O. H. E. R., Nuclear and High Energy Physics of the U. S. Dept. of Energy under contract # DE-AC03-76SF00098.

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Appendix A

# Notation

| | | |
|---|---|---|
| $A_{DET}$ | detector area | [$\mu m^2$] |
| $A_v$ | open loop gain of TFT | |
| $\alpha$ | frequency dependence factor of flicker noise in TFT | |
| $C_{DET}$ | detector capacitance | [pF] |
| $C_F$ | feedback capacitance of preamplifier = $C_{gd}$ | [pF] |
| $C_{in}$ | input capacitance of = $C_{gs}$ + $C_{gd}$ | [pF] |
| $C_T$ | sum of detector and input capacitance = $C_{DET}$ + $C_{gs}$ | [pF] |
| $C_i$ | insulator capacitance per unit area of channel | [pF] |
| $C_{gs}$ | capacitance between gate and source | [pF] |
| $C_{gd}$ | capacitance between gate and drain | [pF] |
| $C_{ds}$ | capacitance between drain and source | [pF] |
| $d_{DET}$ | a-Si detector thickness | [$\mu$m] |
| $d_i$ | insulator thickness | [$\mu$m] |
| $d_a$ | a-Si thickness in TFT | [mm] |
| e | basis of logarithm = 2.718 | |
| $\varepsilon_i$ | dielectric constant of insulator ( $Si_3N_4$ = 7, $SiO_2$ = 4 ) | |
| $\varepsilon_s$ | dielectric constant of a-Si = 12 | |
| $\varepsilon_o$ | dielectric constant of air = $8.854 \times 10^{-14}$ | [F/cm] |
| f | frequency | [Hz] |
| $G_1$ | gain of the 2nd stage = $V_1/V_i$ | |
| $G_2$ | gain of the 2nd stage = $V_o/V_1$ | |
| $G_T$ | total gain of preamplifier = $G_1G_2$ | |
| G(f) | transfer function of RC-CR shaping amplifier | |
| $g_m$ | transconductance of TFT | [$\mu$A/V] |
| $g_o$ | channel conductance of TFT | [$\mu$A/V] |
| $I_D$ | drain-to-source current | [$\mu$A] |
| $I_{DET}$ | detector leakage current = $J_L * A_{DET}$ | [$\mu$A] |
| $i_D^2$ | drain current noise sspectrum | [$A^2$/Hz] |
| $i_i^2$ | input current noise sources | [$A^2$/Hz] |
| $i_{FD}^2$ | flicker noise in the detector | [$A^2$/Hz] |
| $i_{LD}^2$ | thermal noise due to the detector load resistance, $R_L$ | [$A^2$/Hz] |
| $i_{SD}^2$ | shot noise of the detector leakage current, $I_L$ | [$A^2$/Hz] |
| $J_L$ | detector leakage curent density | [A/$cm^2$] |
| k | Boltzmann constant = $8.614 \times 10^{-5}$ | [eV/°K] |
| $K_d$ | flicker noise constant of the detector = $2 \times 10^{-18}$ | [Am] |
| $K_f$ | flicker noise constant of TFT | [$V^2$/F] |
| L | channel length | [$\mu$m] |
| $L_o$ | gate-to-drain or source overlapping length | [$\mu$m] |
| $\mu_e$ | field effect electron mobility in a-Si:H | [$cm^2$/Vsec] |
| $N_i$ | input equivalent noise from parallel noise source | [electrons] |
| $N_j$ | input equivalent noise from series noise source | [electrons] |
| $N_{FD}$ | flicker noise in the detector | [electrons] |
| $N_{LD}$ | thermal noise due to detector load resistance, $R_L$ | [electrons] |

| | | |
|---|---|---|
| $N_{SD}$ | shot noise due to detector leakage current, $I_L$ | [electrons] |
| $N_{FT}$ | flicker noise in the TFT | [electrons] |
| $N_{LT}$ | thermal noise of load resistance, $R_{D1}$ | [electrons] |
| $N_{TT}$ | thermal noise due to 1/gm in the TFT | [electrons] |
| $N_{TOT}$ | total noise | [electrons] |
| $N_{TFT}^2$ | input equivalent noise from TFT = $N_{TT}^2 + N_{FT}^2$ | [$electrons^2$] |
| q | charge on electron = $1.602 \times 10^{-19}$ | [Coul] |
| $Q_{SIG}$ | electron-hole pairs produced in the detector | [Coul] |
| $R_{D1}$ | drain load resistance of the 1st stage amplifier | [MΩ] |
| $R_{D2}$ | drain load resistance of the 2nd stage amplifier | [MΩ] |
| $R_G$ | gate bias control resistance | [MΩ] |
| $R_L$ | detector load resistance | [MΩ] |
| $R_S$ | source load resistance of source follower | [MΩ] |
| $R_{S2}$ | source load resistance of the 2nd stage amplifier | [MΩ] |
| $r_o$ | output resistance of TFT | [MΩ] |
| $S_{SIG}$ | electron-hole pairs produced in the detector | [electrons] |
| S/N | signal-to-noise ratio | |
| T | temperature | [°K] |
| $T_t$ | electron transit time in the channel of TFT | [μsec] |
| $\tau$ | RC time constant of the 1st stage amplifier | [μsec] |
| $\tau_o$ | peaking time constant of RC - CR shaping amplifier | [μsec] |
| $V_D$ | drain voltage | [V] |
| $V_{dd}$ | bias supply voltage | [V] |
| $V_G$ | gate bias voltage | [V] |
| $V_T$ | threshold voltage | [V] |
| $V_i$ | input voltage signal | [mV] |
| $V_1$ | voltage signal after 1st stage amplifier | [mV] |
| $V_o$ | output voltage signal | [mV] |
| $v_{out}$ | output voltage signal from single electron-hole pair | [V] |
| $v_j^2$ | input equivalent voltage noise sources | [$V^2$/Hz] |
| $v_{FT}^2$ | flicker noise in the TFT | [$V^2$/Hz] |
| $v_{LT}^2$ | thermal noise due to load resistance, $R_{D1}$ | [$V^2$/Hz] |
| $v_{TT}^2$ | thermal noise due to channel resistance | [$V^2$/Hz] |
| $v_{TFT}^2$ | input equivalent noise from TFT = $v_{TT}^2 + v_{FT}^2$ | [$V^2$/Hz] |
| W | channel width | [μm] |

Appendix B

## Noise Equations

| Spectrum in Freq. Domain | Eqv. Noise in Time Domain |
|---|---|
| $i^2_{LD}(f) = \frac{4\,kT}{R_L}\,\Delta f$ | $N^2_{LD} = \left(\frac{e}{q}\right)^2 * \frac{kT}{2\,R_L} * \tau_o$ |
| $i^2_{SD}(f) = 2\,q\,I_{DET}\,\Delta f$ | $N^2_{SD} = \frac{e^2\,I_{DET}}{4\,q} * \tau_o$ |
| $i^2_{FD}(f) = \frac{K_d\,I_{DET}}{d_{DET}\;f}\,\Delta f$ | $N^2_{FD} = \left(\frac{e}{q}\right)^2 * \frac{K_d\,I_{DET}}{d_{DET}} * \tau_o^2$ |
| $v^2_{LT}(f) = \frac{4\,kT}{R_{D1}\,g_m^2}\,\Delta f$ | $N^2_{LT} = \left(\frac{e\,C_T}{q}\right)^2 * \frac{kT}{2\,R_{D1}\,g_m^2} * \frac{1}{\tau_o}$ |
| $v^2_{TT}(f) = \frac{8\,kT}{3\,g_m}\,\Delta f$ | $N^2_{TT} = \left(\frac{e\,C_T}{q}\right)^2 * \frac{kT}{3\,g_m} * \frac{1}{\tau_o}$ |
| $v^2_{FT}(f) = \frac{K_f}{C_i\,WL\,f^{\alpha}}\,\Delta f$ | $N^2_{FT} = \left(\frac{e\,C_T}{q}\right)^2 * \frac{K_f}{2\,C_i WL} * F(\alpha,\tau_o)$ |

where

$$F(\alpha,\tau_o) = 1 \qquad \text{if } \alpha = 1$$

$$F(\alpha,\tau_o) = (2\pi\tau_o)^{\alpha-1} * \frac{\left(\frac{(\alpha-1)\pi}{2}\right)}{\sin\left(\frac{(\alpha-1)\pi}{2}\right)} \qquad \text{if } \alpha \neq 1$$

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