UC San Diego
Technical Reports

Title
Feedthrough Channel Effect on Wirelength Distribution in the Presence of Obstacles

Permalink
https://escholarship.org/uc/item/1m23w7cd

Authors
Kahng, Andrew
Cheng, Chung-Kuan
Liu, Bao
et al.

Publication Date
2005-10-12

Peer reviewed

Feedthrough Channel Effect on Wirelength Distribution In the Presence of Obstacles

Andrew B. Kahng[1], Chung-Kuan Cheng[1], Bao Liu[1] and Dirk Stroobandt[2]

[1] Department of Computer Science and Engineering
University of California at San Diego, La Jolla, CA, 92093, USA
{abk, kuan, bliu}@cs.ucsd.edu
[2] Department of Electronics and Information Systems
Ghent University, B-9000 Gent, Belgium
dstr@elis.rug.ac.be

Abstract

Wirelength estimation techniques typically contain a site density function and an occupation probability function. SOC designs bring large IP blocks which form routing obstacles and deviate wirelength estimation. In this paper we extend previous work of wirelength estimation in the presence of obstacles by considering feedthrough channel effect and derive complete expressions for several cases of two obstacles. Our results are one step further into the domain of wirelength estimation in the presence of multiple obstacles and towards finding equivalent obstacle relations to facilitate a priori wirelength estimation schemes in chip planning tools, i.e., wireload models to improve parasitic estimation accuracy and timing closure.

Keywords

Wireload models, interconnect length estimation, obstacles, floorplanning.

1 Introduction

In deep submicron design, the importance of estimating interconnect parameters such as delay, power, wirelength and routability increases; such estimates are part of the objectives of partitioning, placement and floorplanning tools. Also, the EDA flow is experiencing a trend of combining front end planning and physical implementation to help design convergence. In this process an efficient yet accurate predictor of interconnect parameters (resource usage, performance, etc.) is crucial. The efficiency and accuracy of front end planning tools depend on the performance of floorplanning, placement and partitioning tools, which in turn depend on that of the interconnect predictor.

RTL planning flows must constantly struggle with the chicken-egg conflict impasse (i) budgeting the path delays within blocks and between blocks, and (ii) finding a (good) placement of the blocks. Typically, this impasse is broken by using initial *wireload models*, i.e., statistically derived (or calibrated) estimates of routing lengths for given-sized nets placed in given-sized regions. These wireload models are certainly needed within blocks (since the blocks have not even been synthesized, let alone placed), and occasionally also between blocks (i.e., at the chip level); they are always needed at some point in the design flow. In this paper, we target a priori (pre-placement) and on-line (during placement) wirelength estimations.

Wirelength estimation was initiated by Landman and Russo's paper [1] on Rent's rule, which was the basis for models of Donath [2], Davis et el. [3], and Stroobandt et el. [4]. A review of recent progress is given in [5]. Apart

1

from techniques that estimate average wirelengths or wirelength distributions, individual net wirelength estimators have also been studied. These techniques exploit individual net information such as bounding box dimensions or number of terminals to yield more accurate estimates. Current industry tools use lookup tables of wirelength as a function of number of terminals [6].[1] The aspect ratio of the region or net bounding box is found to have a considerable effect on the expected wirelength for nets with few terminals [8].

All of these papers are based on regularly placed circuits such as gate array or standard cell designs, with the exception of [6] which considers a building block design methodology. With the trend toward IP-block-based System-on-Chip (SOC) design, it is more likely that the presence of macro cells as obstacles (e.g., memories or noise-sensitive memory blocks) may significantly lengthen wires and cause congestion. To the best of our knowledge, no work to date has provided interconnect wirelength estimates in the presence of routing obstacles. In [6], routing obstacles are handled by dividing routing area into small bins, applying global routing over bins and using lookup tables for each bin.

Wirelength estimation in the presence of obstacles has been studied recently. Expected average wirelength is provided in [16] and discrete wirelength distribution is presented in [17]. Our work is an extension of [17]. We adopt the same *generating polynomial* techinique [15] as in [17] and investigate the feedthrough channel effect on wirelength distribution.

Our paper is organized as follows. Section 2 present the related work and gives our definitions. Previous results in [17] are reviewed in section 3 for the completeness of this paper. Section 4 presents our contribution of investigating wirelength distribution and feedthrough channel effect in the presence of two obstacles in multiple cases - with identical or covering x-spans. Experimental analysis and observations are made in section 5 and we conclude our work in section 6.

2 Background and Definition

The well-known Rent's rule presents a simple empirical power law relationship between the number of terminals T and the number of gates N in a random logic network [1] [3] [5] [9] :

$$T = kN^p \tag{1}$$

with k the average number of terminals per gate and p the Rent exponent. The Rent exponent is an empirical constant ranging from 0.2 to 1 across different architectures and different placement optimizations [10][11] [12] [13]. Micro-processors, gate arrays and high performance computers have been reported to have Rent exponent values of 0.45, 0.5 and 0.63 respectively [14]. Circuits under good placement tend to have small Rent exponent values while randomly placed logic networks have Rent exponent $p = 1$.

This empirical relationship forms the foundation of most traditional wirelength estimators. The probability density function $n(l)$, defined as the percentage of wires with length l, is generally used to express the wirelength distribution [3] [5] [15]. It contains two main parts, a *site function* $f(l)$ that enumerates all possible shortest paths of length l between points in a grid and an *occupation probability function* $occ(l)$ that assigns to each path a probability to occur depending on its length. In other words [**?**],

$$n(l) = \frac{N(l)}{N_{total}} = \frac{f(l)occ(l)}{\sum_{l=1}^{l_{max}} f(l)occ(l)} \tag{2}$$

---

[1] Also, global routing may be used as a constructive estimator. Indeed, proponents of global routing – notably Scheffer and Nequist [7] – have argued that interconnect estimation can only be performed constructively. This is in some sense a religious issue (e.g., contrast with Monterey Design emphasis on non-constructive prediction and estimation). We believe that the door is still open to development of strong *non-constructive, a priori* interconnect estimation methods; this is the motivation for our present work.

with

$$occ(l) \approx p(1-p)2^{p-1}l^{2p-4}. \tag{3}$$

This probability density function $n(l)$ can then be used to derive various kinds of interconnect parameter estimations. For example, the average wirelength can be obtained as

$$\bar{l} = \sum_l n(l)l \tag{4}$$

and the probability to have all N wires shorter than l_0 is

$$Prob(l(p) < l_0 \mid \forall p \in P, |P| = N) = (\sum_{l < l_0} n(l))^N. \tag{5}$$

Previous publications do not take obstacle effects into account when computing the site function $f(l)$. In this paper, we adopt an enumeration technique based on generating polynomials [**?**] which allows us to augment current wirelength estimation techniques with our analysis of obstacle effects. In a row based layout the site function is a discrete distribution and the generating polynomial technique is used to express the site function as a polynomial by taking a summation of $x^{l(p)}$ for each path p between two terminals with length $l(p)$ over the finite set P of shortest paths between all possible terminal-pairs in the layout. In other words, the site function $f(l)$ can be expressed in a polynomial

$$V(x) = \sum_l f(l)x^l = \sum_{p \in P} x^{l(p)}. \tag{6}$$

We are the first to distinguish between several effects of rectangular routing obstacle on wirelength distribution site functions. We observe that the presence of an obstacle reduces the number of possible terminal-pairs by restricting the set of all possible terminal locations. Obstacles also introduce detours around the obstacle and increase the lengths of some wires. We thus separate an obstacle's effect into *terminal redistribution effect* and *blockage effect*, and define the following scenarios to screen out each individual effect.

Definition 1 (Intrinsic wires) *Intrinsic wires* [2] *are shortest paths between all possible terminal-pairs in a rectangular array of placement locations without any obstacle.*

Definition 2 (Redistribution wires) *Redistribution wires are shortest paths between all possible terminal-pairs in a rectangular array of placement locations with 'transparent' obstacles within which terminals cannot be located but through which wires can pass.*

Definition 3 (Blockage wires) *Blockage wires are shortest paths between all possible terminal-pairs in a rectangular array of placement locations with opaque obstacles within which terminals cannot be located and through which wires cannot pass.*

The difference between redistribution wires and intrinsic wires is due to the redistribution effect of the obstacles, and the difference between blockage wires and redistribution wires is due to the blockage effect. In the rest of this paper, these differences are respectively called *redistribution change* and *blockage change*.

---

[2]Following virtually all previous literature, we study only two-terminal nets in this paper. Wirelengths of multi-terminal nets could be defined as the length of the Steiner minimal tree, minimum spanning tree or another length, depending on the actual router. However, they may not have a closed-form formula. A lookup table of Steiner minimum tree intrinsic lengths is presented in [6] and extended in [8] for a rectangular layout region of arbitrary aspect ratio.

3 Related Work

3.1 Single Obstacle

In this section we briefly go over the previous work in [16] and [17] for completeness of our derivation. We analyze an array of $m \times n$ placement locations (with x indices from 0 to $n-1$ and y indices from 0 to $m-1$) in the presence of a rectangular obstacle spanning between (but not including) x indices a and b and y indices c and d ($0 \leq a < b \leq n-1$ and $0 \leq c < d \leq m-1$). The distance between two horizontally (vertically) adjacent placement locations is w (h) [3]. We use polynomials $V_I(m,n,w,h)$, $V_R(m,n,a,b,c,d,w,h)$ and $V_B(m,n,a,b,c,d,w,h)$ respectively to express the site function of intrinsic, redistribution and blockage wires in this scenario based on the generating polynomials technique.

3.1.1 Intrinsic Wires

Applying *generating polynomial* and *convolution* techniques [15]

$$
\begin{aligned}
V_I(m,n,w,h) &= \sum_{x_1=0}^{n-1}\sum_{x_2=0}^{n-1}\sum_{y_1=0}^{m-1}\sum_{y_2=0}^{m-1} x^{|x_1-x_2|w+|y_1-y_2|h} \\
&= f_1(n,w)f_1(m,h) \\
f_1(n,w) &= \sum_{x_1=0}^{n-1}\sum_{x_2=0}^{n-1} x^{|x_1-x_2|w} \\
&= \sum_{x_1=0}^{n-1}\left(\sum_{x_2=0}^{x_1} x^{(x_1-x_2)w} + \sum_{x_2=x_1+1}^{n-1} x^{(x_2-x_1)w} \right) \\
&= \frac{2x^{(n+1)w} - nx^{2w} - 2x^{w} + n}{(x^{w}-1)^2}.
\end{aligned} \tag{7}
$$

3.1.2 Redistribution Wires

By subtracting from intrinsic wires all paths with any terminal within the transparent obstacle, the site function $V_R(m,n,a,b,c,d,w,h)$ of redistribution wires is given by:

$$
\begin{aligned}
&V_R(m,n,a,b,c,d,w,h) \\
&= \sum_{x_1=0}^{n-1}\sum_{x_2=0}^{n-1}\sum_{y_1=0}^{m-1}\sum_{y_2=0}^{m-1} x^{|x_1-x_2|w+|y_1-y_2|h} - 2\sum_{x_1=a+1}^{b-1}\sum_{x_2=0}^{n-1}\sum_{y_1=c+1}^{d-1}\sum_{y_2=0}^{m-1} x^{|x_1-x_2|w+|y_1-y_2|h} \\
&\quad + \sum_{x_1=a+1}^{b-1}\sum_{x_2=a+1}^{b-1}\sum_{y_1=c+1}^{d-1}\sum_{y_2=c+1}^{d-1} x^{|x_1-x_2|w+|y_1-y_2|h} \\
&= f_1(n,w)f_1(n,h) - 2f_2(a,b,n,w)f_2(c,d,m,h) + f_1(b-a-1,w)f_1(d-c-1,h)
\end{aligned} \tag{8}
$$

where

$$
f_2(a,b,n,w)
$$

---

[3]Thus placement locations are located at absolute coordinates $0, w, 2w, \ldots, (n-1)w$ in the x direction and $0, h, 2h, \ldots, (m-1)h$ in the y direction. The obstacle spans from $aw+\varepsilon$ to $bw-\varepsilon$ in the x direction and from $ch+\varepsilon$ to $dh-\varepsilon$ in the y direction.

$$= \sum_{x_1=a+1}^{b-1} \sum_{x_2=0}^{n-1} x^{|x_1-x_2|w}$$

$$= \frac{x^{(b+1)w} + x^{(n-a)w} - x^{(a+2)w} - x^{(n-b+1)w} - (b-a-1)x^{2w} + (b-a-1)}{(x^w-1)^2}$$

3.1.3 Blockage Wires

Blockage wires are obtained by counting detour length for corresponding redistribution wires. We identify the redistribution wires that need a detour of length l, and use $V_R(l)$ to express the distribution of these wires.

We notice that a horizontal detour of length l only occurs when at least one terminal of the wire is located on y index $c + \frac{l}{2h}$ or $d - \frac{l}{2h}$ (this implies $\frac{l}{2h}$ is an integer) and the other terminal of the wire is located between y indices $c + \frac{l}{2h}$ and $d - \frac{l}{2h}$ since the obstacle spans between but does not include y indices c and d (Fig. **??**). By enumerating over all terminal-pairs with one terminal on y index $c + \frac{l}{2h}$ or $d - \frac{l}{2h}$ and the other terminal between y indices $c + \frac{l}{2h}$ and $d - \frac{l}{2h}$ on the other side of the obstacle (thus four combinations are formed as the first terminal can be on y index $c + \frac{l}{2h}$ or $d - \frac{l}{2h}$ and on the left or right side of the obstacle), subtracting the cases when both terminals are on y index $c + \frac{l}{2h}$ or $d - \frac{l}{2h}$ (which we double-counted) and counting a coefficient 2 for terminal permutation, the site function $V_R^h(l,m,n,a,b,c,d,w,h)$ of the redistribution wires with horizontal detour of length l is given by:

$$V_R^h(l,m,n,a,b,c,d,w,h)$$

$$= 2(4\sum_{x_1=0}^{a} \sum_{y_1=c+\frac{l}{2h}}^{c+\frac{l}{2h}} \sum_{x_2=b}^{n-1} \sum_{y_2=c+\frac{l}{2h}}^{d-\frac{l}{2h}} x^{|x_1-x_2|w+|y_1-y_2|h} - 2\sum_{x_1=0}^{a} \sum_{y_1=c+\frac{l}{2h}}^{c+\frac{l}{2h}} \sum_{x_2=b}^{n-1} \sum_{y_2=c+\frac{l}{2h}}^{c+\frac{l}{2h}} x^{|x_1-x_2|w+|y_1-y_2|h}$$

$$-2\sum_{x_1=0}^{a} \sum_{y_1=d-\frac{l}{2h}}^{d-\frac{l}{2h}} \sum_{x_2=b}^{n-1} \sum_{y_2=c+\frac{l}{2h}}^{c+\frac{l}{2h}} x^{|x_1-x_2|w+|y_1-y_2|h})$$

$$= \frac{x^{(n+1)w} - x^{(n-a+1)w} - x^{(b+2)w} + x^{(b-a+2)w}}{(x^w-1)^2} (8\frac{x^{(d-c+1)h-l}-1}{x^h-1} - 4 - 4x^{(d-c)h-l}).$$

Using the symmetry in the problem, the redistribution wires with detour length l can be expressed as

$$V_R(l,m,n,a,b,c,d,w,h)$$

$$= f_3(a,b,n,w)f_4(c,d,h,\frac{l}{2h}) + f_3(c,d,m,h)f_4(a,b,w,\frac{l}{2w}) \tag{9}$$

where

$$f_3(a,b,n,w) = \frac{x^{(n+1)w} - x^{(n-a+1)w} - x^{(b+2)w} + x^{(b-a+2)w}}{(x^w-1)^2}$$

$$f_4(c,d,h,k) = \begin{cases} 8\frac{x^{(d-c-2k+1)h}-1}{x^h-1} - 4 - 4x^{(d-c-2k)h} & : \quad 0 \le k \le \lfloor \frac{d-c}{2} \rfloor \text{ and } k \text{ is an integer,} \\ 0 & : \quad \text{otherwise.} \end{cases}$$

By adding detour length into the corresponding redistribution wires, the site function $V_B(m,n,a,b,c,d,w,h)$ of blockage wires is given by

$$V_B(m,n,a,b,c,d,w,h)$$

$$= V_R(m,n,a,b,c,d,w,h) + \sum_{l=0}^{L_{max}(a,b,c,d)} (x^l - 1)V_R(l,m,n,a,b,c,d,w,h)$$

$$= V_R(m,n,a,b,c,d,w,h) + f_3(a,b,n,w)(f_5(c,d,h) - f_6(c,d,h))$$

$$+ f_3(c,d,m,h)(f_5(a,b,w) - f_6(a,b,w)) \tag{10}$$

where

$$f_5(c,d,h) = \sum_{k=0}^{l_{max}(c,d,h)} x^{2kh} f_4(c,d,h,k)$$

$$= (l_{max}(c,d)+1)(8\frac{x^{(d-c+1)h}}{x^h - 1} - 4x^{(d-c)h}) - (4 + \frac{8}{x^h - 1})\frac{x^{2(l_{max}(c,d)+1)h} - 1}{x^{2h} - 1},$$

$$f_6(c,d,h) = \sum_{k=0}^{l_{max}(c,d,h)} f_4(c,d,h,k)$$

$$= (8\frac{x^{(d-c+1)h}}{x^h - 1} - 4x^{(d-c)h})\frac{x^{-2(l_{max}(c,d)+1)h} - 1}{x^{-2h} - 1} - (l_{max}(c,d)+1)(4 + \frac{8}{x^h - 1}),$$

$$L_{max}(a,b,c,d) = Max(\lfloor b-a \rfloor, \lfloor d-c \rfloor),$$

$$l_{max}(c,d,h) = \lfloor \frac{d-c}{2h} \rfloor.$$

In the following section we give some numerical examples and make observations regarding the effects of obstacle and layout region aspect ratio on the site functions of intrinsic, redistribution and blockage wires.

3.2 Multiple Obstacles

3.2.1 Redistribution Wirelengths

Redistribution wires can be derived for multiple obstacles by subtracting from intrinsic wires all the wires with at least one terminal in an obstacle. We have the following general expression[4]:

$$V_R(m,n,a_1,b_1,c_1,d_1,\ldots,a_k,b_k,c_k,d_k,w,h)$$

$$= V_I(m,n,w,h) - 2\sum_{i=1}^{k} f_2(a_i,b_i,n,w)f_2(c_i,d_i,m,h) + \sum_{i=1}^{k}\sum_{j=1}^{k} f_7(a_i,b_i,a_j,b_j,w)f_7(c_i,d_i,c_j,d_j,h) \tag{11}$$

where

$$f_7(a_i,b_i,a_j,b_j,w) = \sum_{x_1=a_i+1}^{b_i-1}\sum_{x_2=a_j+1}^{b_j-1} x^{|x_1-x_2|w}$$

$$= \frac{x^{(b_j-a_i)w} - x^{(b_j-b_i+1)w} - x^{(a_j-a_i+1)w} + x^{(a_j-b_i+2)w}}{(x^w - 1)^2}.$$

---

[4]This follows the polynomial expansion $(I - \sum_{i=1}^{k} s_i)^2 = I^2 - 2\sum_{i=1}^{k} IS_i + \sum_{i=1}^{k}\sum_{j=1}^{k} S_i S_j$.
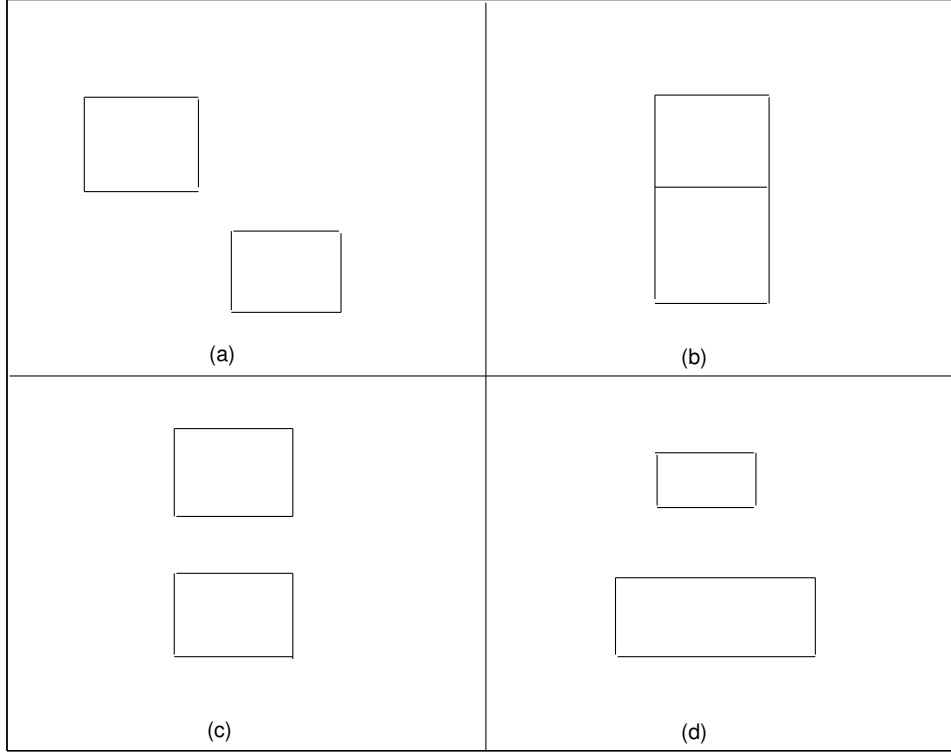
Figure 1: Two obstacles with different relative locations (a) with disjoint x/y-spans, (b) with a zero-width feedthrough, (c) with a non-zero-width feedthrough and (d) with covering x-spans.

3.2.2 Obstacles with Disjoint Spans

However the blockage wires depend on the relative location of the obstacles. For two obstacles with disjoint x- and y-spans [17] (Fig. 1 (a)), blockage is made by each obstacle individually, and the overall blockage effect is the sum of each obstacle's effect. So we have the following expression for redistribution wires with detour length l:

$$
\begin{aligned}
& V_R(l, m, n, a_1, b_1, c_1, d_1, a_2, b_2, c_2, d_2, w, h) \\
= \ & f_3(a_1, b_1, n, w) f_4(c_1, d_1, h, \frac{l}{2h}) + f_3(c_1, d_1, m, h) f_4(a_1, b_1, w, \frac{l}{2w}) + \\
& f_3(a_2, b_2, n, w) f_4(c_2, d_2, h, \frac{l}{2h}) + f_3(c_2, d_2, m, h) f_4(a_2, b_2, w, \frac{l}{2w}).
\end{aligned}
\tag{12}
$$

4 Feedthrough Channel Effects

In this section we extend previous discussion into two obstacle cases. We investigate feedthrough channel effect in the presence of multiple obstacles, specifically, we investigate two obstalces with identical or covering x-spans. The two obstacles (a_1, b_1, c_1, d_1) and (a_2, b_2, c_2, d_2) are located in an array of $m \times n$ placement locations (with x indices from 0 to $n-1$ and y indices from 0 to $m-1$). Obstacle $A(B)$ spans between (but not include) x indices $a_1(a_2)$ and $b_1(b_2)$ and y indices $c_1(c_2)$ and $d_1(d_2)$. The distance between two horizontally(vertically) adjacent placement locations is $w(h)$.

4.1 Zero Width Feedthrough Channel

In this subsection we study a single obstacle with a zero-width feedthrough channel, or say, two obstacles abut of location (a,b,c,l) and (a,b,l,d) respectively (Fig. 1 (b)). The redistribution wires with detour length l can be expressed as

$$V_R(l,m,n,a,b,c,d,f,w,h)$$
$$= f_3(a,b,n,w)f_4(c,f,h,\frac{l}{2h}) + f_3(a,b,n,w)f_4(f,d,h,\frac{l}{2h}) + f_3(c,d,m,h)f_4(a,b,w,\frac{l}{2w}). \tag{13}$$

4.2 Non-Zero Width Feedthrough Channel

Similarly, a feedthrough channel with width $c_2 - d_1$ or two obstacles (a,b,c_1,d_1) and (a,b,c_2,d_2) (Fig. 1 (c)) have the following redistribution wires around with detour length l:

$$V_R(l,m,n,a,b,c_1,d_1,c_2,d_2,w,h)$$
$$= f_3(a,b,n,w)f_4(c_1,d_1,h,\frac{l}{2h}) + f_3(a,b,n,w)f_4(c_2,d_2,h,\frac{l}{2h}) + f_3(c_1,d_2,m,h)f_4(a,b,w,\frac{l}{2w}). \tag{14}$$

The blockage wirelengths are obstained by adding detour lengths with the redistribution wirelengths as:

$$V_B(m,n,a,b,c_1,d_1,c_2,d_2,w,h)$$
$$= V_R(m,n,a,b,c_1,d_1,c_2,d_2,w,h) + \sum_{l=0}^{L_{max}(a,b,c_1,d_1,c_2,d_2)} (x^l - 1)V_R(l,m,n,a,b,c_1,d_1,c_2,d_2,w,h)$$
$$= V_R(m,n,a,b,c_1,d_1,c_2,d_2,w,h) + f_3(a,b,n,w)(f_5(c_1,d_1,h) - f_6(c_1,d_1,h))$$
$$+ f_3(a,b,n,w)(f_5(c_2,d_2,h) - f_6(c_2,d_2,h)) + f_3(c_1,d_2,m,h)(f_5(a,b,w) - f_6(a,b,w)) \tag{15}$$

with

$$L_{max}(a,b,c_1,d_1,c_2,d_2) = Max(\lfloor b-a \rfloor, \lfloor d_1 - c_1 \rfloor, \lfloor d_2 - c_2 \rfloor). \tag{16}$$

4.3 Two Obstacles with Covering X-Spans

Next we consider two obstalces with one obstalcle's x-span covering the other's (two obstacles (a_1,b_1,c_1,d_1) and (a_2,b_2,c_2,d_2) with $a_1 < a_2 < b_2 < b_1$ and $c_1 < d_1 < c_2 < d_2$) (Fig. 1 (d)). In this case blockage is made only by each obstalce individually, the same as in section 3.2.2, but we need to remove some area occupied by the obstacles when counting the redistribution wires with detour length l. The redistribution wires with detour length l are as follows:

$$V_R(l,m,n,a_1,b_1,c_1,d_1,a_2,b_2,c_2,d_2,w,h)$$
$$= f_3(a_1,b_1,n,w)f_4(c_1,d_1,h,\frac{l}{2h}) + f_3(a_2,b_2,n,w)f_4(c_2,d_2,h,\frac{l}{2h}) +$$
$$f_3(c_1,d_1,m,h)f_4(a_1,b_1,w,\frac{l}{2w}) + f_3(c_2,d_2,m,h)f_4(a_2,b_2,w,\frac{l}{2w}) -$$
$$f_{11}(a_1,a_2,b_2,b_1,w,\frac{l}{2w})f_{12}(0,c_1,c_2+1,d_2-1,h) -$$
$$f_{11}(a_2,a_2+\frac{l}{2w},b_2-\frac{l}{2w},b_2,w,\frac{l}{2w})f_{12}(0,d_1-1,d_2,m-1,h) \tag{17}$$

8

where

$$f_{11}(a_1,a_2,b_2,b_1,w,k) = \sum_{x_1=a_1+k}^{a_1+k}\sum_{x_2=a_2+1}^{b_2-1} x^{|x_1-x_2|w} + \sum_{x_1=b_1-k}^{b_1-k}\sum_{x_2=a_2+1}^{b_2-1} x^{|x_1-x_2|w}$$

$$= \begin{cases} \frac{x^{(b_2-a_1-k)w}-x^{(a_2-a_1-k+1)w}+x^{(b_1-a_2-k)w}-x^{(b_1-b_2-k+1)w}}{x^w-1} & : \quad k \le a_2-a_1 \ and \ k \le b_1-b_2, \\ \frac{x^{(b_2-a_1-k)w}+x^{(a_1-a_2+k)w}+x^{(b_1-a_2-k)w}+x^{(b_2-b_1+k)w}-2x^w-2}{x^w-1} & : \quad k \ge a_2-a_1 \ and \ k \ge b_1-b_2. \end{cases}$$

$$f_{12}(c_1,d_1,c_2,d_2,h) = \sum_{y_1=c_1}^{d_1}\sum_{y_2=c_2}^{d_2} x^{|y_1-y_2|h}$$

$$= \frac{1}{(x^h-1)^2}\left(x^{(d_2-c_1+2)h}-x^{(d_2-d_1+1)h}-x^{(c_2-c_1+1)h}+x^{(c_2-d_1)h}\right).$$

So

$$V_B(m,n,a_1,b_1,c_1,d_1,a_2,b_2,c_2,d_2,w,h)$$

$$= V_R(m,n,a_1,b_1,c_1,d_1,a_2,b_2,c_2,d_2,w,h)+\sum_{l=0}^{L_{max}(a,b,c_1,d_1,c_2,d_2)}(x^l-1)V_R(l,m,n,a,b,c_1,d_1,c_2,d_2,w,h)$$

$$= V_R(m,n,a_1,b_1,c_1,d_1,a_2,b_2,c_2,d_2,w,h)$$
$$+f_3(a_1,b_1,n,w)(f_5(c_1,d_1,h)-f_6(c_1,d_1,h))+f_3(a_2,b_2,n,w)(f_5(c_2,d_2,h)-f_6(c_2,d_2,h))$$
$$+f_3(c_1,d_1,m,h)(f_5(a_1,b_1,w)-f_6(a_1,b_1,w))+f_3(c_2,d_2,m,h)(f_5(a_2,b_2,w)-f_6(a_2,b_2,w))$$
$$-f_{13}(a_1,a_2,b_2,b_1,w)f_{12}(0,c_1,c_2+1,d_2-1,h)-f_{13}(a_2,a_2,b_2,b_2,w)f_{12}(0,d_1-1,d_2,m-1,h)$$

$$(18)$$

where

$$f_{13}(a_1,a_2,b_2,b_1,w)$$

$$= \sum_{k=0}^{l_{max}(c,d,w)}(x^{2kw}-1)f_{11}(a_1,a_2,b_2,b_1,w,k)$$

$$= (\frac{x^{a_2-a_1+1}-1}{x-1}-\frac{x^{-(a_2-a_1+1)}-1}{x^{-1}-1})\frac{x^{b_2-a_1}-x^{a_2-a_1+1}+x^{b_1-a_2}-x^{b_1-b_2+1}}{x-1}+$$

$$(\frac{x^{l_{max}+1}-x^{a_2-a_1+1}}{x-1}-\frac{x^{-(l_{max}+1)}-x^{-(a_2-a_1+1)}}{x^{-1}-1})\frac{x^{b_2-a_1}+x^{b_1-a_2}}{x-1}+$$

$$(\frac{x^{3(l_{max}+1)}-x^{3(a_2-a_1+1)}}{x^3-1}-\frac{x^{l_{max}+1}-x^{a_2-a_1+1}}{x-1})\frac{x^{a_1-a-2}+x^{b_2-b_1}}{x-1}-$$

$$(\frac{x^{2(l_{max}+1)}-x^{2(a_2-a_1+1)}}{x^2-1}-(l_{max}-a_2+a_1))\frac{2x+2}{x-1}$$

5 Experiments and Numerical Examples

To experimentally verify our theoretical analysis and extend our study to multiple obstacles, we have developed a program to observe the redistribution and obstacle wirelengths. The program takes as inputs a set of obstacles and
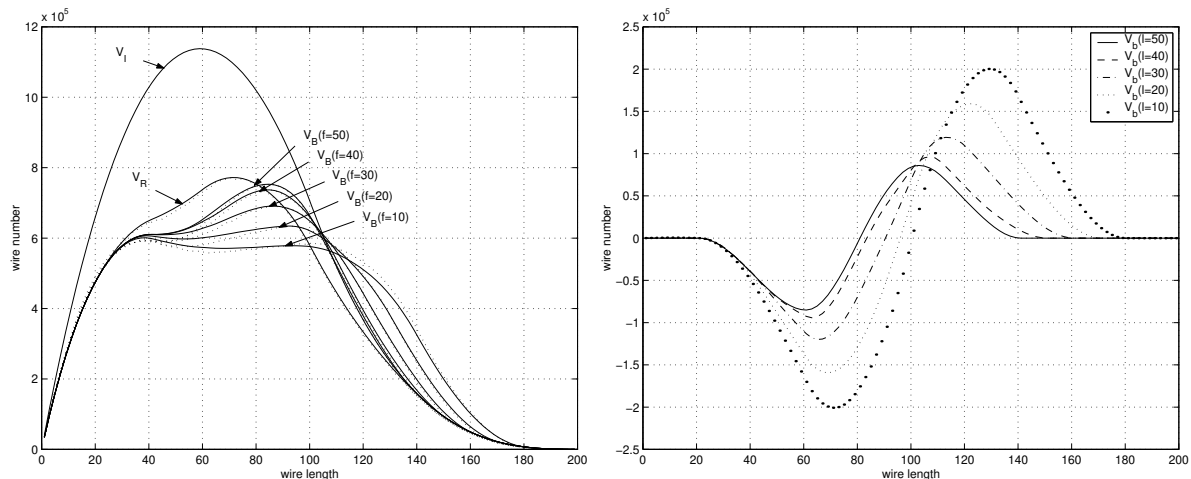
Figure 2: Wirelength distribution with different feedthrough locations $y = f$.

their dimensions and locations, as well as the number of net terminals. For calculation of the redistribution wirelength, obstacles are treated as areas where net terminals are not allowed but wires can pass through. For the calculation of the blockage wirelength, routing is prohibited inside the obstacle areas. The site functions are obtained over uniformly random terminal sets, and the probability density functions are obtained over random terminal sets with the l^{2p-4} wirelength distribution. All results are over 10,000 or more random sets per run.

5.1 Feedthrough Location

In this experiment an 20×80 obstacle is located at the center of a 100×100 array of placement locations (i.e., $m = n = 101, a = 40, b = 60, c = 10, d = 90, w = h = 1$). A feedthrough channel divides the obstacle by a horizontal line $y = l$. Fig. 2(left) presents the blockage wirelength distributions with different feedthrough locations ($l = 10, 20, 30, 40, 50$); Fig. 2(right) gives the blockage changes V_b. The dotted lines in Fig. 2(left) are experimental data from running our simulation code. They match well with the solid lines from previous expressions and verify the correctness of our theoretical analysis.

From Fig. 2 we further make the following observation:

Observation 1 *Feedthroughs reduce blockage. The closer is a feedthrough to the center of the obstacle, the larger is its effect.*

5.2 Feedthrough Width

In this experiment the same obstalce ($m = n = 101, a = 40, b = 60, c = 10, d = 90, w = h = 1$) as previous is studied. However we increase the feedthrough width by turning more obstacle area into feedthrough channel. The redictribution and blockage wirelength distribution with different feedthrough width are plotted in Fig. 3)(left); blockage change is presented in Fig. 3)(right). Our observation is :

Observation 2 *As more obstacle area change into feedthrough, redistribution wires, blockage wires and blockage change all decrease.*
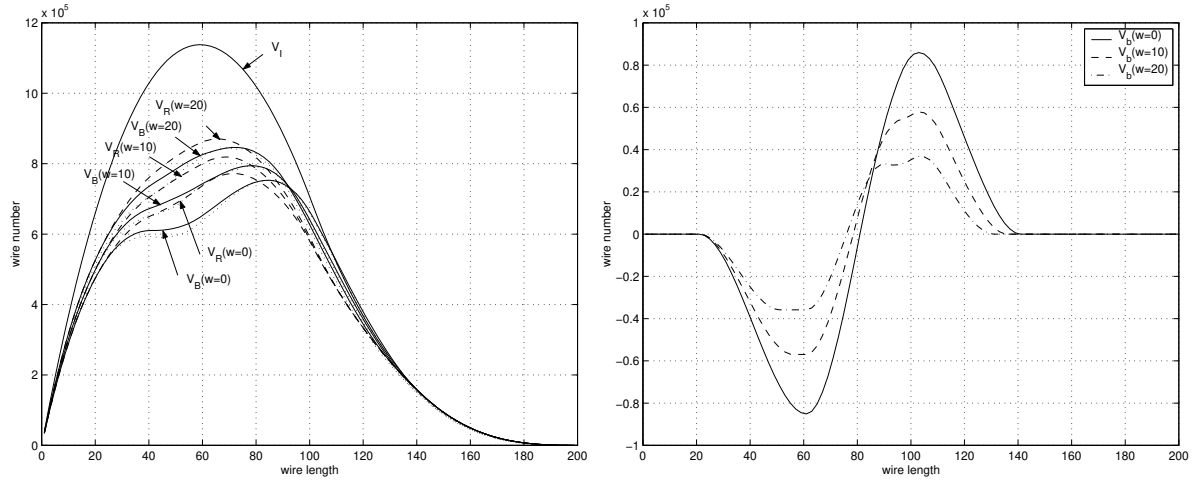
10

Figure 3: Wirelength distribution with different feedthrough width *w* (by turning obstacle area into feedthrough).
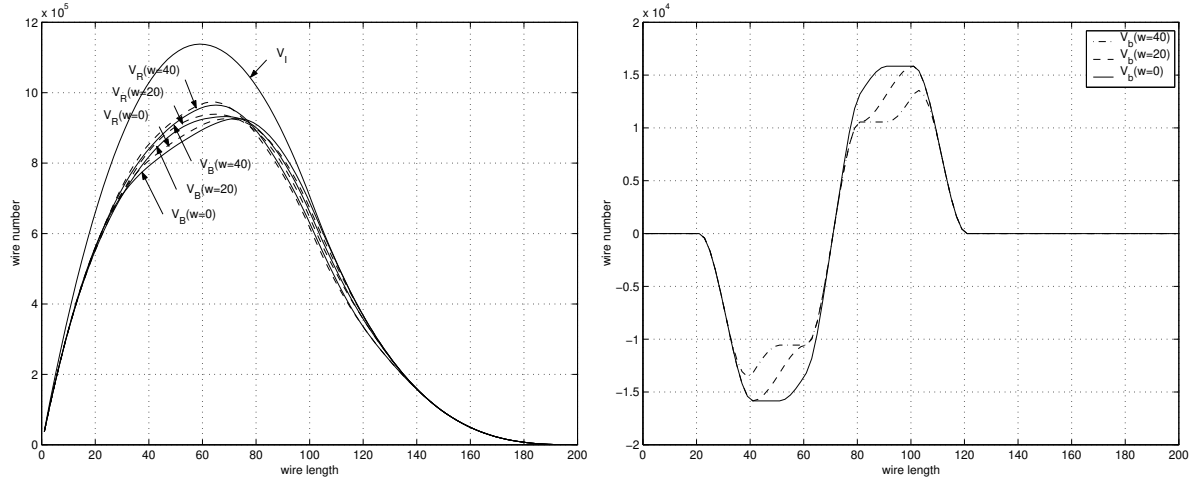

Figure 4: Wirelength distribution with different feedthrough width *w* (by shifting obstacles).

5.3 Feedthrough Width with Fixed Obstacle Area

In this experiment an obstacle with fixed area is seperated by a feedthrough channel. The two parts of the obstacle (each of dimension 20×20) are moved away from the center of the placement locations to change the feedthrough width. Fig. 4 (left) shows redistribution wirelengths decrease due to obstacle displacement; Fig. 4 (right) gives blockage changes with different feedthrough width.

Observation 3 *Blockage change decrease slowly as feedthrough channel getting wider.*

5.4 Obstacle Width

An Obstacle of fixed height 80 is located at the center of the 100×100 placement locations. The observation from the wirelengths in Fig. 5 (left) and blockage changes in Fig. 5 (right) is:
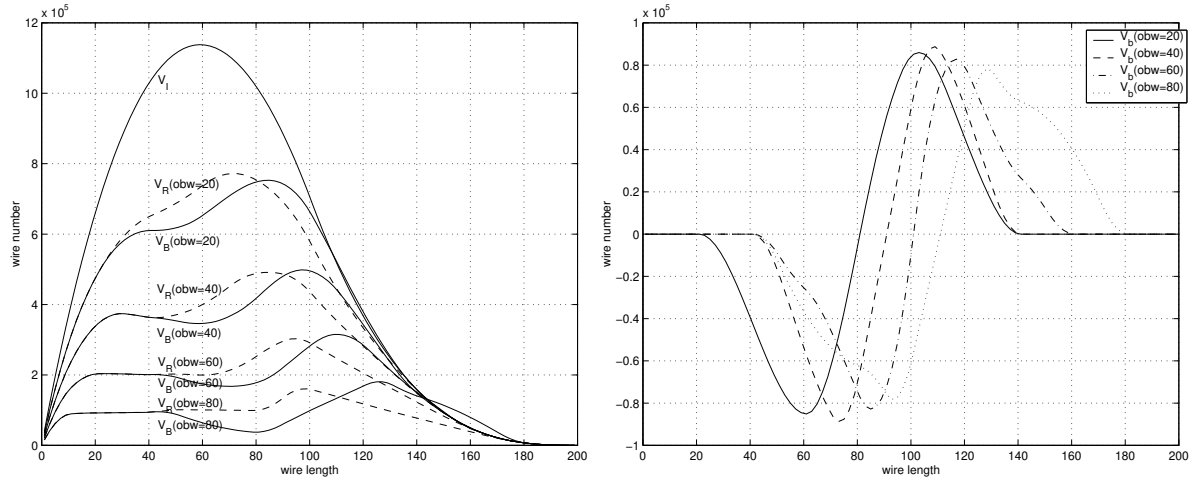
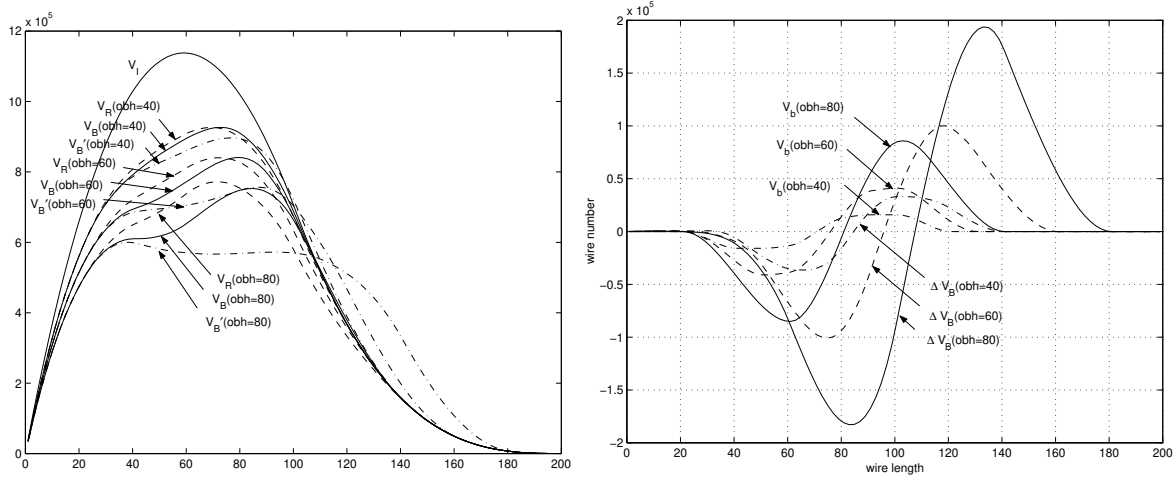Figure 5: Wirelength distribution with different obstacle width *obw* (shifting).

Figure 6: Wirelength distribution with different obstacle height *obh*.

Observation 4 *Blockage change is independent on obstacle width.*

However with wider obstacles the wires taking detour become a little longer.

5.5 Obstacle Height

We change the height of an obstacle of width 20 located at the center of the placement locations. Fig. 7 (left) gives the number of redistribution and blockage wires decrease as the obstacle area increases; Fig. 7 (right) presents blockage changes V_b and the blockage wirelength decreases ΔV_B caused by feedthrough.

Observation 5 *Obstacles with larger height have larger blockage changes. Feedthrough channels have larger effect when the obstacle has larger height.*
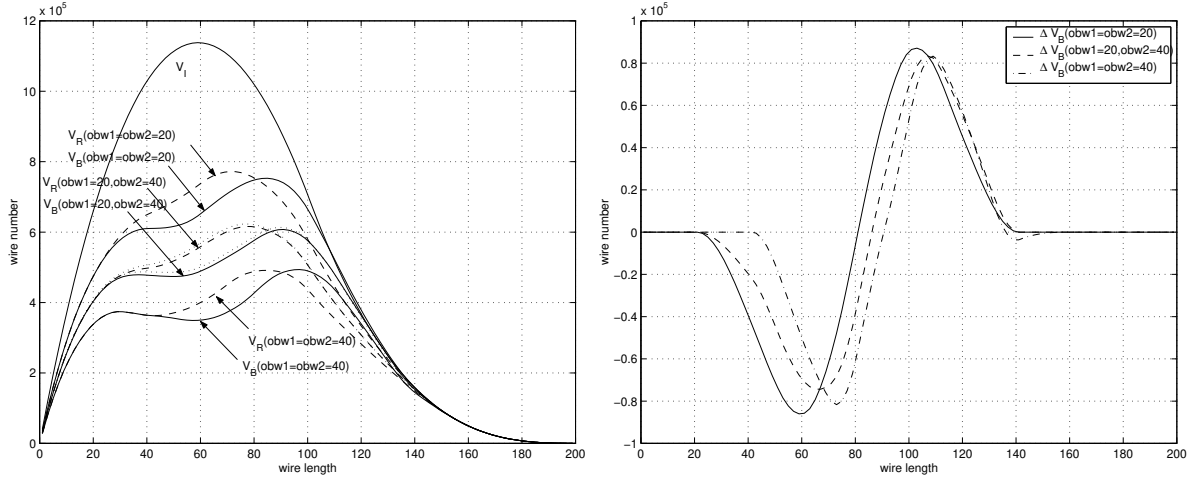
Figure 7: Wirelength distribution with different obstacle width *obw*1 and *obw*2.

5.6 Obstacles with Covering X-Spans

In this experiment we have an 20×80 obstacle at the center of the placement locations, with a horizontal zero-width feedthrough channel at $y = 50$ (case 1). We first change the width of the bottome part of the obstacle into 40 (case 2), then change the width of the top part into 40 also (case 3). We observe the redistribution and blockage wires of case 2 is the average redistribution and blockage wires of case 1 and case 3, respectively (Fig. 7 (left))[5]. We also observe the blockage change of case 2 is between that of case 1 and base 3 (Fig. 7 (right)).

6 Conclusions

Wirelaod models have been widely adopted to provide *a priori* interconnect parameter estimates, but their poor accuracy has been detrimental to convergence of modern design methodologies. In System-on-a-chip (SOC) designs embedded IP blocks form routing blockages and further deviate wirelength estimation. We extend the previous work of wirelength estimation in the presence of obstalces and investigate feedthrough channel effect and wirelength distributions for several multiple obstacle cases.

Expression for redistribution wirelength in the presence of multiple obstacles can be derived in a form of polynomial expansion; while blockage wires are much complicated: it depends on introduction of feedthrough channels, overlaps between obstacles and obstacle displacement. In this paper we study the feedthrough channel effect. Complete theoretical wirelength distribution expressions for many two obstalce cases are provided and help us better understand wirelength distributions in the presence of multiple obstacles.

Several parameters influence the feedthrough channel effect on the wirelengths: feedthrough location, feedthrough width, obstacle height, obstacle width and obstacle shape. Our experimental observations verify our theoretical anaylsis, give a clear understanding on feedthrough channel effect and help to guide SOC designs.

Our work is one step further into the domain of wirelength estimation in the presence of multiple obstacles. It aims to form the foundation of finding an *equivalent obstacle* for a group of small obstacles in order to facilitate the table-lookup of wireload models, make them more accurate and effective and helps design convergence.

---

[5]This is intuitive from symmetry.

13

References

[1] B. S. Landman and R. L. Russo, "On a Pin versus Block Relationship for Partitions of Logic Graphs", *IEEE Trans. on Computers*, C-20, 1971, pp. 1469-1479.

[2] W. E. Donath, "Placement and Average Interconnection Lengths of Computer Logic", *IEEE Trans. on Circuits and Systems*, CAS-26(4), 1979, pp. 272-277.

[3] J. A. Davis, V. K. De and J. D. Meindl, "A Stochastic Wire- Length Distribution for Gigascale Integration(GSI)-part 1: Derivation and Validation", *IEEE Trans. on Electron Devices*, 45, 1998, pp. 580-589.

[4] D. Stroobandt and J. Van Campenhout, "Accurate Interconnection Length Estimations for Predictions Early in the Design Cycle,", *VLSI Design, Special Issue on Physical Design in Deep Submicron*, 10(1), 1999, pp. 1-20.

[5] P. Christie and D. Stroobandt, "The Interpretation and Application of Rent's Rule", *IEEE Trans. on VLSI Systems, Special Issue on System-Level Interconnect Prediction*, 2000.

[6] C. E. Cheng, "RISA: Accurate and Efficient Placement Routability Modeling", *Proc. IEEE International Conference on Computer-Aided Design*, 1994, pp. 690-695.

[7] L. Scheffer and E. Nequist, "Why Interconnect Prediction Doesn't Work," *Proc. ACM Workshop on System-Level Interconnect Prediction*, 2000, pp. 139-144.

[8] A. E. Caldwell, A. B. Kahng, S. Mantik, I. L. Markov and A. Zelikovsky, "On Wirelength Estimations for Row-Based Placement", *Proc. International Symposium on Physical Design*, 1998, pp. 4-11.

[9] D. Stroobandt, "Tutorial: A Priori Wire Length Estimations Based on Rent's Rule", *In Workshop on System-Level Interconnect Prediction*, 1999, pp. 3-50.

[10] D. Stroobandt, "On an efficient method for estimating the interconnection complexity of designs and on the existence of region III in Rent's rule", *Proceedings Ninth Great Lakes Symposium on VLSI*, 1999, pp. 330-1.

[11] T. Chiba, "Impact of the LSI on high-speed computer packaging", *IEEE Trans. on Computers*, C-27, 1978, pp. 319-325.

[12] D. K. Ferry, "Interconnection lengths and VLSI", *IEEE Circuits and Devices Magazine*, vol. 1, 1985, pp. 39-42.

[13] D. K. Ferry and E. W. Greenwich, *Ultra Large Scale Integrated Microelectronics*, Prentice-Hall, 1988.

[14] H. B. Bakoglu, "*Circuits, Interconnections, and Packaging for VLSI*", Reading, MA: Addison-Wesley, 1990.

[15] D. Stroobandt and H. V. Marck, "Efficient Representation of Interconnection Length Distributions Using Generating Polynomials", *International Workshop on System-Level Interconnect Prediction*, 2000, pp. 99-105.

[16] A. B. Kahng, C.-K. Cheng, B. Liu and D. Stroobandt, "Toward Better Wireload Models in the Presence of Obstacles", *Proc. ASP-DAC*, Feb. 2001 (to appear).

[17] A. B. Kahng, C.-K. Cheng, B. Liu and D. Stroobandt, "Toward Better Wireload Models in the Presence of Obstacles", submitted.