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100Gbps Half-Rate Referenceless Injection-Locking Clock/Data Recovery Circuit in 0.18 μm BiCMOS Process

DISSERTATION

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DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

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2017

DEDICATION

To my wonderful parents, brother and sister, for their enduring love and support, and my beautiful wife for her dedication and partnership

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ABSTRACT OF THE DISSERTATION

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Broadband communication has become essential for the global informational infrastructure. Although not as ubiquitous for personal communications as voice-band wireless (e.g., cell phones), broadband is used for most high-speed internet communication. The use of optical fibers for broadband communication has dramatically reduced the speed bottleneck in wide-area networks (WANs). Indeed, the bandwidth capabilities of state-of-the art optical fibers are so large that it is the electrical components connected at the ends of the fibers that limit system transmission speeds. Over the past decade design innovations and scaling down of CMOS fabrication processes have enabled bit rates to steadily increase.

Throughputs of serial channels are now approaching 100 Gb/s, while at the same time there is more pressure to decrease power dissipation. Indeed, designers are being challenged to improve the efficiency of broadband transceivers by bringing the energy per bit down toward 1 pJ/bit.

With this in mind, this dissertation addresses one of the key issues in modern broadband system design. The design of a clock/data recovery circuit is one of the most challenging blocks in a broadband receiver. One of those challenges is the frequency acquisition range, which is naturally quite low for the phase detectors used in such circuits, thereby necessitating additional circuitry to enhance this acquisition range. Another challenge is the slow locking time exhibited by conventional methods, which is undesirable for some applications. We propose a different approach, based on injection locking, that does not require an external reference clock, and thus can reduce the form factor of the overall transceiver. The chip is implemented in the standard 180-nm BiCMOS process and represents the first implementation of 100Gbps injection locking based CDR.

1. INTRODUCTION

Optical communication systems have been used for high-speed data transmission since the early 1980s [1]. The demand for bandwidth intensive applications has increased significantly in the last decade. Applications such as video streaming, cloud based computing, cloud storage, and most recently Internet of Things (IoT) have created a demand that has rushed deployment of high-speed transceivers of 100 Gbps and even 400Gbps. Optical transmission has proved to be a promising method to meet the increasing demand for high-rate and long-distance communications with the required large bandwidth. Over the past decade design innovations and scaling down of CMOS fabrication processes have enabled bit rates to steadily increase. However, to satisfy the demand for greater network capacity scaling down of CMOS is not sufficient, thereby necessitating novel circuit design techniques. Figure 1 shows the block diagram of a simplified optical communication system. Indeed, the bandwidth capabilities of state-of-the art optical fibers are so large that it is the electrical components connected at the ends of the fibers that limit system transmission speeds.

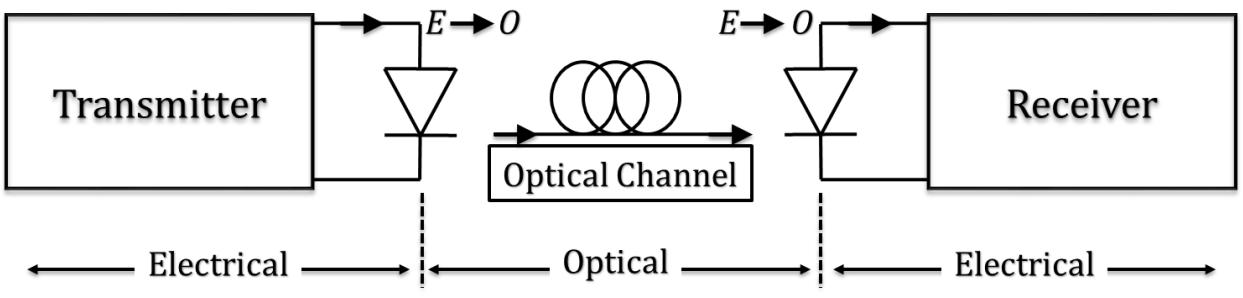

Figure 1. Optical communication system

The Trans-Impedance Amplifier (TIA), Limiting Amplifier (LA), and clock/data recovery (CDR) circuits are the essential blocks of the receiver as shown in Figure 2. The TIA amplifies the current at the output of the photodiode and generates a proportional voltage. The signal will then be amplified and clipped by the high-gain LA block. Due to the non-idealities and noise of the transmitter and the channel, the data is attenuated and distorted. Therefore, depending on the application there can be an equalizer block following the LA to minimize the distortion, noise, and high-frequency attenuation. This can avoid having the jitter exceed the jitter tolerance limits of the CDR circuit.

The CDR is one of the most critical and challenging blocks in a broadband communication receiver. It is used to generate an internal high-speed clock signal that is precisely synchronized with an incoming random data sequence. In addition to satisfying the necessary speed capability for a given bit rate, such circuits must meet several stringent specifications, such as locking time, jitter tolerance, jitter generation, and bit error-rate. Meeting all of these specifications requires various tradeoffs, which are made even more challenging at very high bit rates.

It would be instructive to start by comparing characteristics of the two most common data types used in wireline communications.

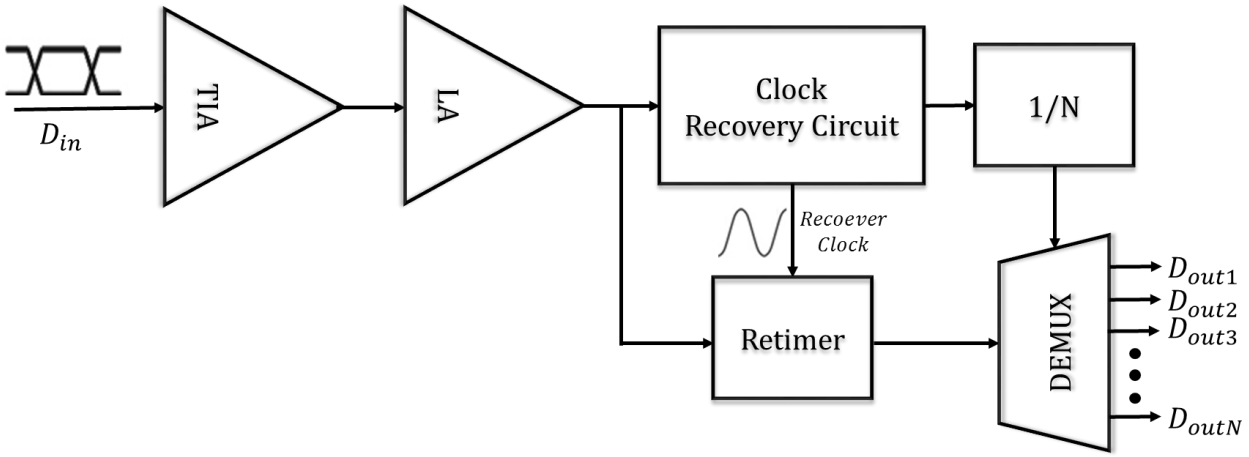

Figure 2. Broadband communication receiver

1.1 NRZ and RZ Data Formats

Non-Return-to-Zero (NRZ) and Return-to-Zero (RZ) data are two types of binary data formats that are commonly used in wireline communication. Compared to their multilevel counter-parts such as PAM4, PAM16, etc., NRZ and RZ data require more bandwidth. The need for more bandwidth can complicate the design of the high-speed channel and the electrical interface. On the other hand, multi-level signaling degrades the signal-to noise-ratio and requires higher linearity at the interface. These trade-offs have slowed the development of multi-level signaling for wireline communications.

In the RZ format, as it appears in the name, the signal always returns to low level in the second half of the period after representing the value of high or low in the first half of the period. In contrast, in NRZ data, the signal value remains at its level, either high or low, during the whole period. The waveforms are shown in Figure 3.

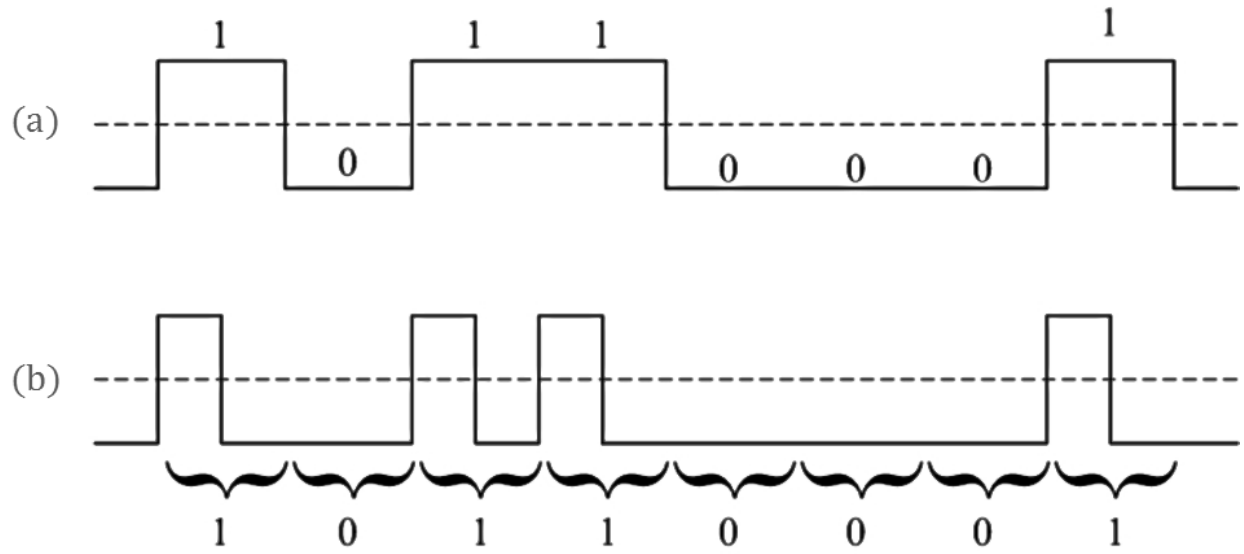

Figure 3. (a) NRZ and (b) RZ data formats

NRZ data contain at most one zero-crossing during each period while RZ data can contain up to two zero-crossings in each period. Therefore, from a bandwidth perspective, an NRZ signal requires half of the bandwidth needed for a RZ signal. For instance, a 0101 data of NRZ has its fundamental at $f_{NRZ} = \frac{1}{2T}$, while the same signal with RZ has its fundamental at $f_{RZ} = \frac{1}{T}$, where T is the period of the input data. The Spectra of RZ and NRZ random data are compared in Figure 4. Despite the simplicity of the clock recovery for RZ data, which can simply be done by an XOR block, the NRZ data format has been used in most of the transceivers due to superior bandwidth efficiency. In the following section, we will be focusing on injection-locking CDRs for NRZ data.

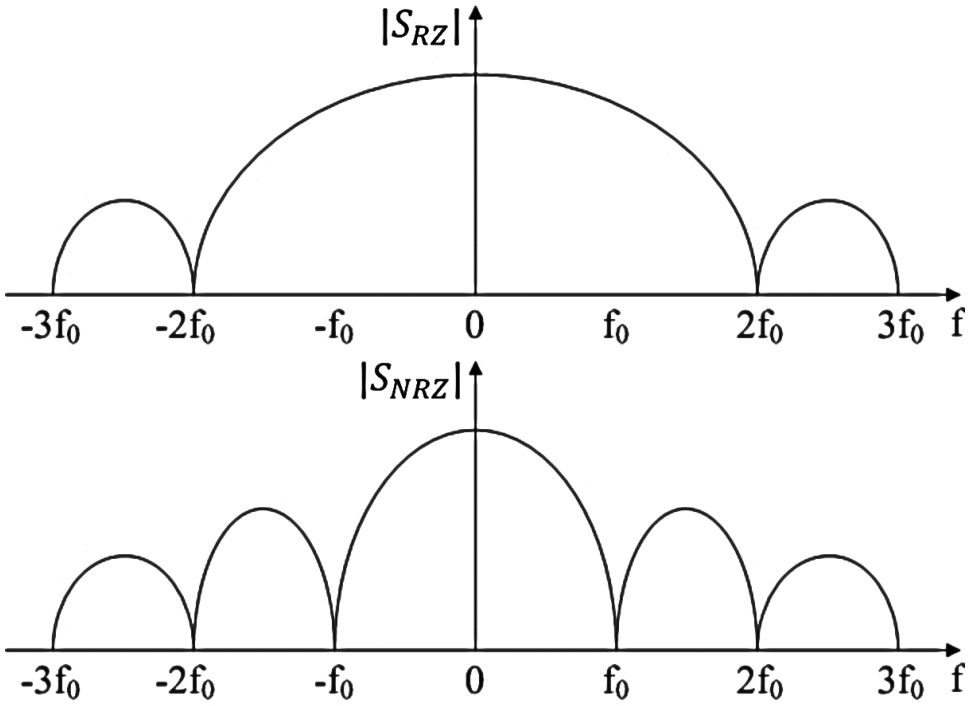

Figure 4. Spectrum of NRZ and RZ data

1.2 Clock/Data Recovery System

Per the explanation above, the CDR provides synchronized clock signals to support overall operation of the receiver and to recover the data with acceptable jitter characteristics. Clock/data recovery system is often the most complicated part of the receiver operation. At higher data rates, this can become even more challenging as the conventional architectures mostly rely on digital circuitry to extract the phase information of the signal. To address the deficiencies at higher data rates several different techniques and architectures, such as use of Current Mode Logic (CML), shunt peaking and series peaking are employed in prior art. Even with these techniques the bandwidth of the digital blocks is often significantly less than the maximum speed potential of the fabrication process as

measured by f_T. One particularly difficult challenge is the limited frequency capture range of a CDR loop, which can cause difficulty in locking due to the process and temperature variations in voltage-controlled oscillator (VCO) circuits. This problem is exacerbated by the wide locking range required by links conforming to multiple communication protocols. Conventionally, an additional frequency-locked loop (FLL) and a reference clock are introduced to aid the frequency acquisition. Once the FLL is locked, the CDR circuit then takes over to complete the final phase locking [1, 2]. However, in many applications, such as repeaters and active cables, it is costly and complicated to implement an accurate and adjustable reference clock. This problem becomes even more difficult at higher bit rates. Moreover, the CDR operation can be affected by coupling from the external reference if the board is compactly designed. Thus, the referenceless CDR architecture has become more popular in recent years because of its simplicity and flexibility for different applications.

CDR architectures can be classified based on their phase alignment method in to three categories:

1. Phase Detector-based CDRs

2. Blind ADC-based CDRs

3. Injection-Locking-based CDRs

In the following subsections, we will explain the operation, advantages and design challenges for each of these types of CDR architectures with a focus on high data-rate communication.

1.2.1 Phase Detector-based CDR

Phase Detectors (PDs) are widely used in most of the feedback loop-based CDRs such as those based on Digital and Analog PLL, DLL, and Phase Interpolation. An Analog PLL-based CDR is shown in Figure 5. The PD compares the phase of its input with that of the recovered clock and converts this phase difference into a proportional voltage. The PD output signal sets the VCO controls voltage by sending proper timing control signals to the charge pump. The filter determines the CDR open-loop and closed-loop behavior and therefore several key specifications of the loop dynamics.

There are several different PD architectures that can be used depending on application most commonly linear and binary PDs. PDs must meet several tight trade-offs that makes the design very difficult, especially at higher data rates.

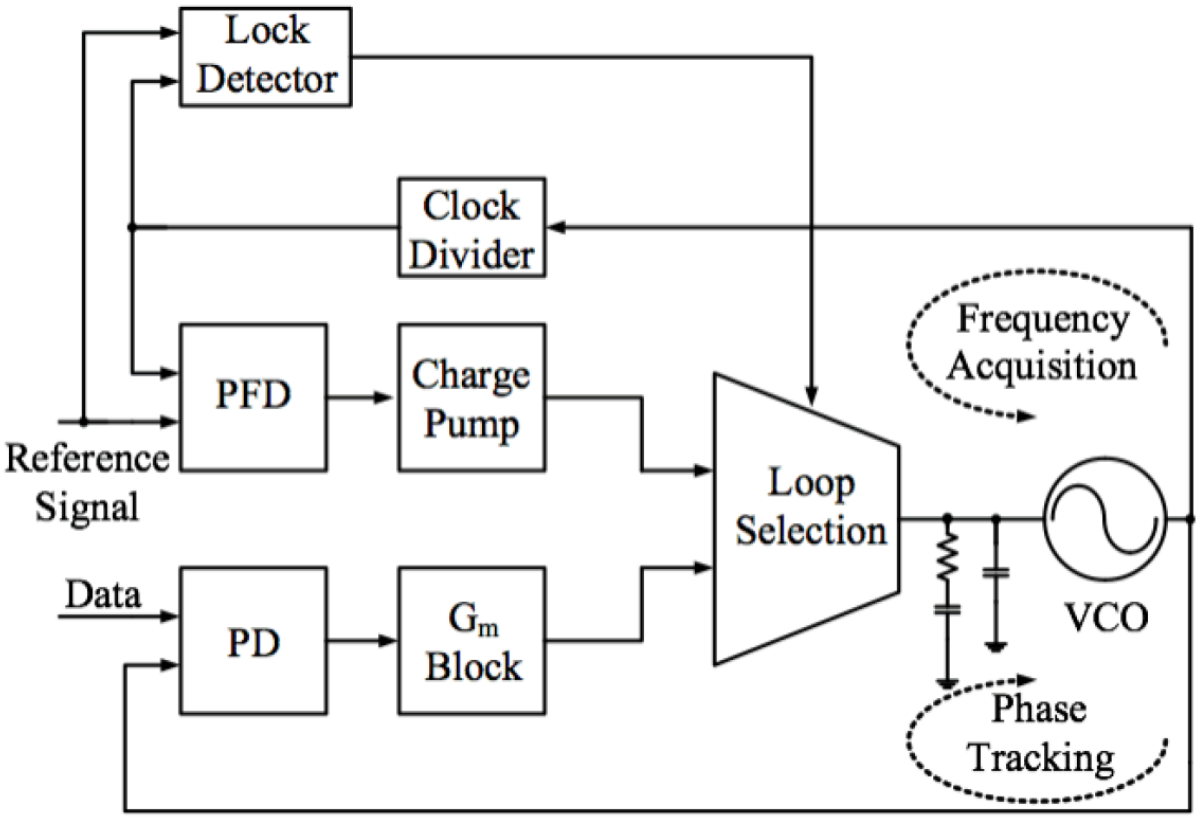

Figure 5. Conventional PD based CDR

The phase detection mechanism in PDs mostly relies on accurate phase difference sensing between the data and the recovered clock. This sensing is normally realized by digital circuitries such as XORs and DFFs. At higher data rates, e.g. 100 Gbps, this phase difference requires signal transitions within a few pico seconds, which makes the PD the bottle neck in the CDR design. Multiphase Phase Detectors are also popular at higher data rates, but they normally need quadrature VCOs, which have higher loading. Clock distribution circuitry that maintains the phase difference at high data rates is also difficult to design at higher data rates.

In PD-based CDRs, acquisition is generally slow even with frequency-acquisition aids due to a known trade-off in that occurs in PLL circuits. Minimizing jitter due to input data noise requires minimizing loop bandwidth; therefore, bandwidth is often much smaller than the tuning range. The large value of the filter capacitor takes more area on the chip, or in some cases requires off-chip capacitors that are hard to model and often low quality due to packaging, bond wire prasitics, etc. [3]. Using a DLL configuration acquisition, can then be faster than that of a PLL. Moreover, unlike the case of a PLL, jitter filtering is independent of the loop bandwidth. Unfortunately, due to the first-order behavior of a DLL based, the jitter performance is inferior.

- **Hogge Phase Detector**

As shown in Figure 6, a Hogge phase detector consists of two D flip-flops and two XORs. This combination can extract the phase difference between the input data and the VCO output. There is a known data transition dependency effect that is addressed by adding DFF2 and XOR2 in this architecture [4]. Due to the linear behavior of the Hogge phase detector, the jitter behavior of the block is well defined. This simplifies the modeling of the CDR and therefore optimization.

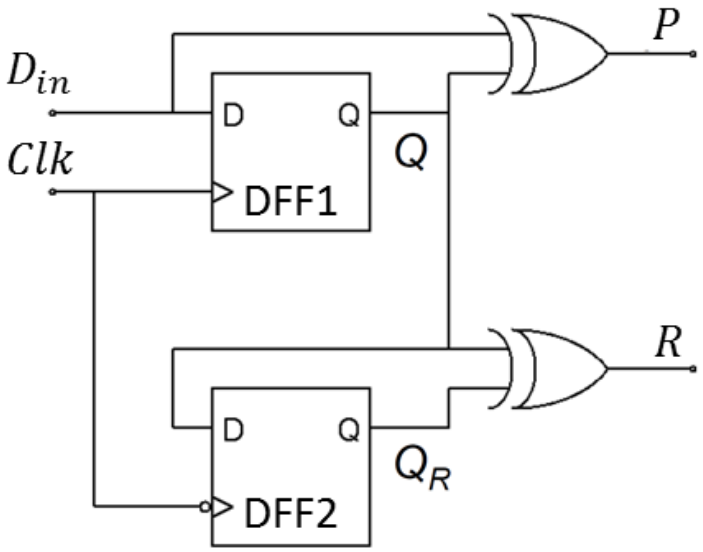

Figure 6. Hogge phase detector

Once the clock-to-q delay and fall/rise time of the signal become comparable to the period of the input data, the Hogge phase detector is proven to have shortcomings, as the operation relies on signal transition timing. One way of addressing these timing problems is to add a delay cell to the path of D_{in} and XOR1. PVT variations make design unreliable in this case and the *P* and *R* signals can become asymmetrical. Due to the long clk-to-q delay, DFF2 will also sample the signal Q at a point that is far from the center, degrading the signal-to-noise ratio (SNR). In practice, limited supply voltage leads to smaller gain of Linear PDs, and therefore the capture range is also smaller than binary CDRs.

- **Binary Phase Detectors**

The most widely used phase detector in CDRs is the Binary or Alexander phase detector, which consists of four DFFs and two XORs as shown in Figure 7. The output of this

phase detector has two values, depending on whether the data transition is lagging or leading the clock transition the clock transition. In the case that the phase difference in nearly equal to zero, the analysis becomes more complicated. When the phase difference approaches zero, two of the DFFs go into the metastable region, generating smaller amplitudes at their output. This behavior, along with the effect of input jitter of the data, leads to a characteristic that is smoother than ideal binary phase detector characteristic. The gain of a binary PD is much higher than its linear counterpart, leading to better locking speed and wider locking range.

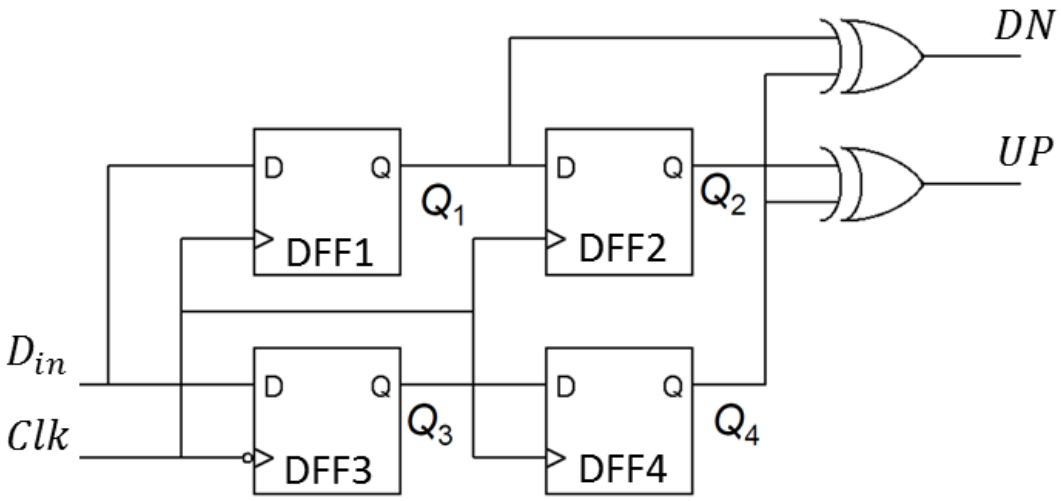

Figure 7. Binary phase detector

The same timing issue that was described earlier for the linear PD, also arises in the binary PD. As the clk-to-q delay becomes comparable to the data transition period, the sampling of DFF2 and DFF4 becomes unreliable. The phase detector gain can be very high in this case, which can lead to high amount of ripple on the VCO control voltage and ultimately

jitter at the output of the CDR. The transition region of the characteristic is also sensitive to PVT as it relies on the voltage values of the D flip-flops before they become stable. The complexity of the transfer curve due to the strong nonlinearity of binary phase detectors makes the CDR modeling complicated. Therefore, jitter transfer function and specifications would be hard to characterize.

1.2.2 Blind ADC-based CDR

Blind ADC-based CDRs have gained attention in recent years due to their mostly digital implementation. By eliminating the need to synchronize the clock to the input data at the interface, they ease the phase detector operation. The CDR will interface with the ADC, as shown in Figure 8, after the signal has already been sampled and digitally pre-processed. The CDR then interpolates between the blind samples to obtain a new set of samples from which the clock phase and data can be recovered. With a digitally implemented receiver and extensive equalization in the digital domain, in advanced CMOS processes superior performance of these receivers is expected [5].

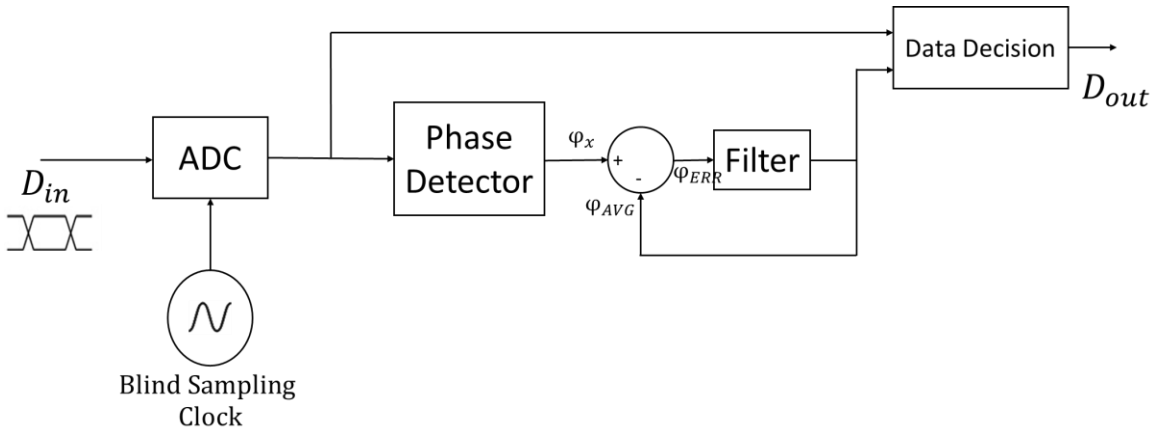

Figure 8. Blind sampling ADC based CDR[5]

To obtain a sufficient number sample points, the data must be sampled at least at the Nyquist rate. In practice, to attain samples with a sufficient signal-to-noise ratio, the data must be sampled at even higher rates. Even with the state-of-the-are CMOS processes, it is very difficult to design an ADC that operates at 100GS/s. Therefore, the time-interleaved ADC (TI-ADC) architecture is employed at higher data rates. In such ADCs, as shown in Figure 9, several individual ADCs operate in parallel at lower speeds to achieve a higher sampling rate.

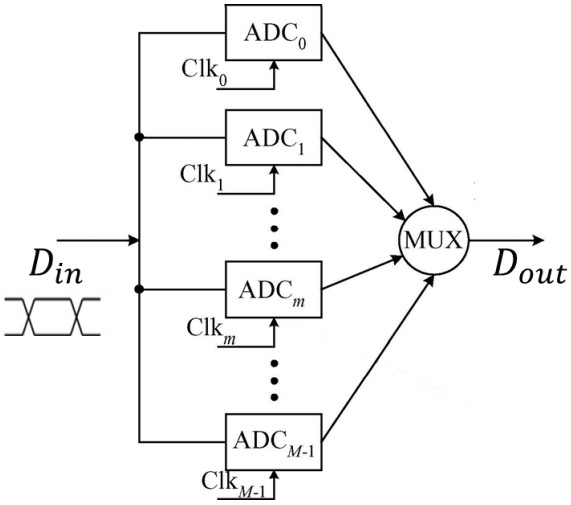

Figure 9. Time-interleaved ADC architecture

There are several difficulties with the design of this type of ADC. Not only it must operate at ultra-high speeds, but it must also meet other key specifications such as power consumption, noise, and jitter performance [5]. The ADC power dissipation grows exponentially with the ADC resolution. To oversample data at higher speeds, e.g. 100Gb/s, the sampling rate and therefore the power consumption would increase excessively. There is a tight trade-off in track and hold (T/H) design between speed and mismatch. Large devices are employed to minimize mismatch between different samples, which therefore leads to lower operation speed and higher power consumption. The high data-rate TI-ADCs also suffer from offset mismatch, gain mismatch and time skew, which can degrade the performance significantly. To address the mismatch problem between different samples and channels, a DSP with background calibration algorithms needs to be integrated along with the receiver for calibration purposes. Adding such a DSP will further complicate the design and increase the power consumption. Adding multiple stages of switches, buffers, capacitors etc. will ultimately tighten the noise margin, as each stage will contribute to the noise budget [6].

1.2.3 Injection-Locking-based CDR

This section will be discussed extensively in the next chapter. In an injection locking CDR, the phase locking takes place in open-loop form, relying on natural pulling of a free-running oscillator. Coupled oscillators experience an effect of locking or pulling by each

other; this effect is called injection locking. This phenomenon was first studied in [7] and it later extensively restudied in [8]. When a periodic signal with high enough power is applied to an oscillator, the tank circuitry will start oscillating off the resonance at the frequency of the applied periodic signal. The relationship between the tank frequency, locking range, and the signal strength shown in (1) can be derived using vector analysis.

$$\Delta\omega = \frac{\omega}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} \qquad (1)$$

where ω is the oscillation frequency, Q is the quality-factor of the tank and I_{osc} and I_{inj} are the oscillator and the injected current amplitudes, respectively. To employ injection locking for CDR applications, it is necessary to convert the transitions in the data into pulses. By doing this, a tone at the baud rate of the input data will appear in the spectrum of the resulted pattern. By injecting high levels of the tone into the oscillator loop, the oscillator will be locked to the tone, and therefore to the baud rate of the data. The output of the oscillator can then be used as the recovered clock of the data for data recovery purposes. A standard way to generate pulses is to XOR the data signal with a delayed version of itself to generate positive pulses corresponding to all input transitions, as shown in Figure 10. This will extract a tone at the baud rate of the data. This tone can be coupled in the oscillator using different methods. By bringing the VCO oscillation frequency close to the baud rate, the oscillator can then be injection locked to the data. This way the output VCO becomes the phase-locked clock associated to the input data. By using this method, most of the difficulties in the PD-based and ADC-based CDRs will be avoided. As long as the pulse generator circuitry can extract the

tone at the baud rate of the data with enough signal strength, the injection locking can take place. This makes injection locking an attractive method in CDR design for high-speed applications.

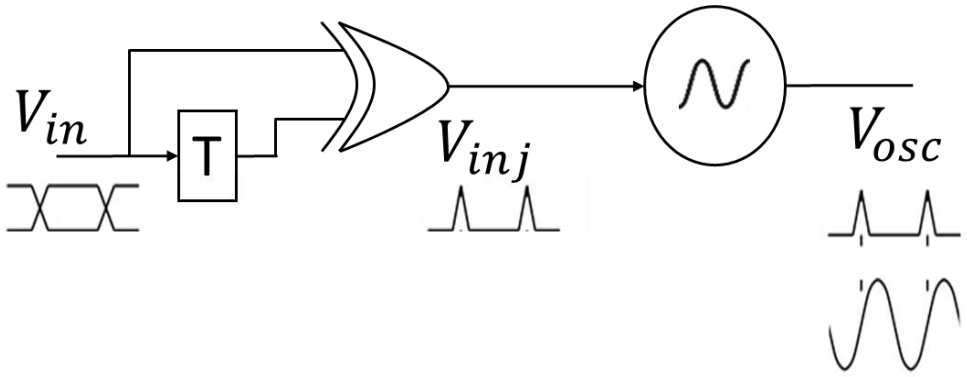

Figure 10.Injection locking clock recovery

At higher speeds, however, it becomes more difficult to generate short pulses corresponding to data transitions, with a signal power high enough to lock the VCO frequency. At 100 Gb/s the unit interval is only 10ps for a non-return-to-zero (NRZ) signal, and thus the pulse that corresponds to data transitions must have rising and falling time of only a few picoseconds. Moreover, applying these pulses directly to the tank at the VCO output, as was done in [9], can be problematic as it can cause amplitude noise at the output of the VCO. These deficiencies will be further discussed and addressed in the next two chapters.

1.3 Dissertation Outline

This dissertation reports the design and fabrication of the first 100 Gbps Injection Locking Clock/Data Recovery System. The equalizer is implemented in a 0.18um BiCMOS process. Through different architectural and circuit design techniques, the many implementation challenges are overcome and a low-power high-speed CDR is produced. In addition, for test purposes, a novel 100Gb/s on chip PRBS generator along with an 8x clock multiplier are implemented on the chip.

In Chapter 2, injection-locking theory in electrical oscillators is discussed. Disadvantages of the prior injection-locking-based CDRs at higher data rates are identified and a novel circuit that addresses those shortcomings is explained in Chapter 3. Chapter 4 is devoted to the implementation challenges and techniques of the referenceless injection-locking CDR suitable for higher data rates. The design of primary blocks is presented in detail. Finally, Chapter 5 provides a summary of the achievements and some suggestions on possible circuit enhancements for future work.

2. INJECTION LOCKING

In the previous chapter, different types of Clock Data Recovery circuits and their shortcomings at higher speeds were discussed. Injection-locking-based CDRs have received attention in recent years. As was described briefly in the previous chapter, due to the method of phase locking that is based on a natural pulling mechanism, they can be a promising candidate for higher data rates, e.g. 100Gb/s.

In this chapter, the theory of injection locking will be discussed. A mechanical model will be qualitatively analyzed to get more insight into the injection locking in electrical oscillators. Finally, the effect of the input and oscillator noise is discussed on the output jitter of an injection locked oscillator.

2.1 Background

Synchronization or pulling between two or more coupled electrical oscillators is called injection locking. This phenomenon, first studied in [7] and later extensively restudied in [8], is often an undesirable effect in electrical circuits such as transceivers and receivers. It can lead to pulling of oscillators causing frequency modulation and phase noise at the outputs, degrading the overall performance. On the other hand, this effect can be employed in circuits to improve the performance or in some cases as the main effect in the design.

Injection Locking has been extensively used in Dividers, PLLs, CDRs and several other circuits.

Injection locking, a nonlinear phenomenon universal to all types of oscillators, is observed in coupled oscillators with oscillation frequency close to one another. In this case, the output of the oscillator can be periodically perturbed by the injected signal, an effect known as "pulling". Under certain conditions, the oscillator can become injection locked to the periodic signal, meaning it will oscillate off its natural resonance frequency at the frequency of the periodic signal. This phenomenon is not only limited only to the electrical oscillators; it can be observed in mechanical, biological and other periodic systems.

There have been several studies on this effect in electrical oscillators in early 1960s. Adler's [7] analysis and experiments laid the groundwork for further investigation of this effect in electrical oscillators. He used the behavior of the motion of a pendulum suspended in a viscous fluid inside a rotating container as a simple mechanical model to explain injection locking. The viscous liquid enclosed in the drum, as illustrated in Figure 11, has angular speed of ω_0 equal to that of the rotating drum due to its high viscosity. It is assumed that the rotation of the liquid is not affected by the pendulum. The pendulum can have three different physical motions depending on the rotational speed of the drum:

- At low angular speed: the pendulum will come to rest at a certain angle of α. In this angle, the force exerted upon pendulum due to rotation of the viscous liquid equates to the force of gravity. If we move the pendulum it will go back to its rest position as shown in Figure 11.

- At the critical angular speed: At the critical speed, the pendulum becomes horizontal, which is where the gravity force has its greatest value in the vertical direction. Past the critical speed, the pendulum will follow the rotation with varying speed in the up and down directions, similar to the pulling condition of the oscillators.
- At higher angular speeds: The pendulum rotational speed becomes equal to that of the drum and a uniform rotation can be observed, similar to the Injection Locking condition of the oscillators.

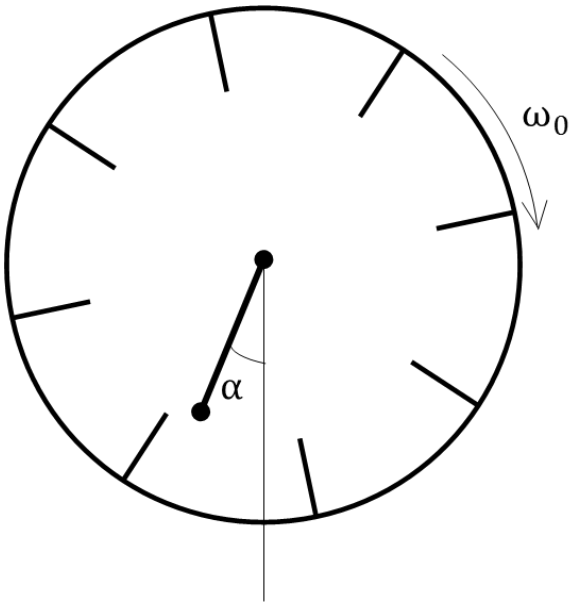

Figure 11. Simple mechanical modeling of injection locking, pendulum and drum

In most cases injection locking is an unwanted behavior and can cause severe jitter and therefore performance degradation when there are number of oscillators in close proximity of one another. For instance, pulling can happen among oscillators in multiple channel systems on the same chip that are used to improve the data rate, as illustrated in Figure 12 [8]. In this case, the victim receiver can come out of lock due to pulling, which leads

to degradation in the bit error rate. To avoid this the oscillators are often placed far from one another with separate supply traces and de-coupling capacitors, which can ultimately increase the chip area and cost. We will be focusing on electrical oscillators in the rest of this section.

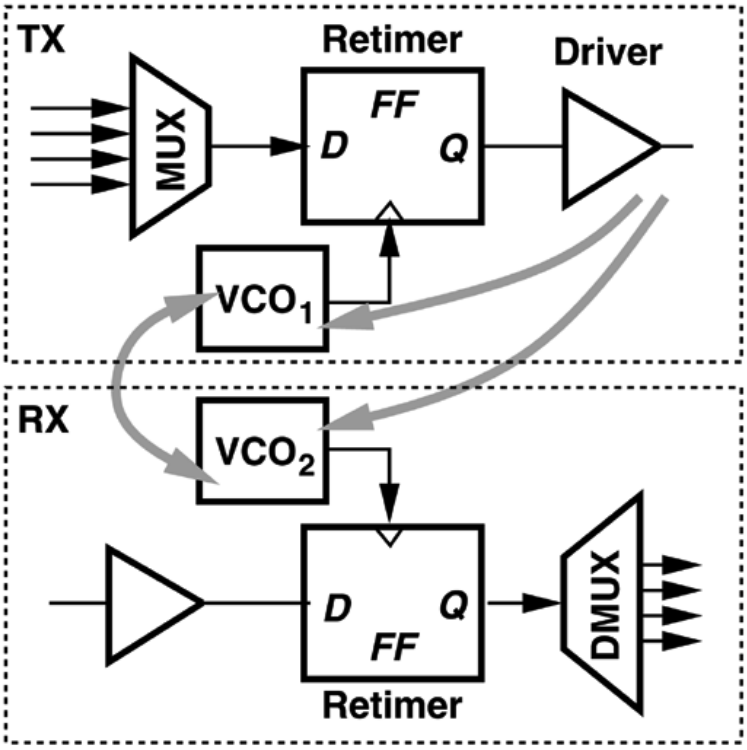

Figure 12. Unwanted injection locking in multi-channel systems [8]

On the other hand, in recent years injection locking has been increasingly exploited as a useful design technique. For instance, injection-locking-based CDRs have been used at higher data rates where the phase detector-based and ADC-based CDRs face limitations. Another example is subharmonic injection-locking clock dividers, which are widely employed in high-frequency PLLs for the first stages of the clock divider that is connected to

the output of the VCO [10]. There are also uses of injection locking in PLL-based phase arrays, where the injection-locked VCOs with varying phase difference are employed to move the beam at the output of the antennas by changing the phase relationship between them [11].

2.2 Injection Locking Analysis

To analyze the behavior of an oscillator under injection of a periodic signal we can use the following model, using a methodology similar to that used in [8]. For an oscillator to have sustainable oscillation, the Barkhausen stability criterion must hold. The circuit will sustain steady-state oscillations only at frequencies for which:

- The loop gain is equal to unity in absolute magnitude
- The phase shift around the loop is zero or an integer multiple of 2π

We then observe that a tank circuit would resonate when the resonator loss L is compensated with a gain as shown Figure 13. The loss of the resonator can be compensated with a gain equal to L^{-1}. The L and therefore G are real numbers. While the tank is resonating at its resonance frequency ω_0, the tank contributes no phase shift, and therefore the phase shift around the loop is zero.

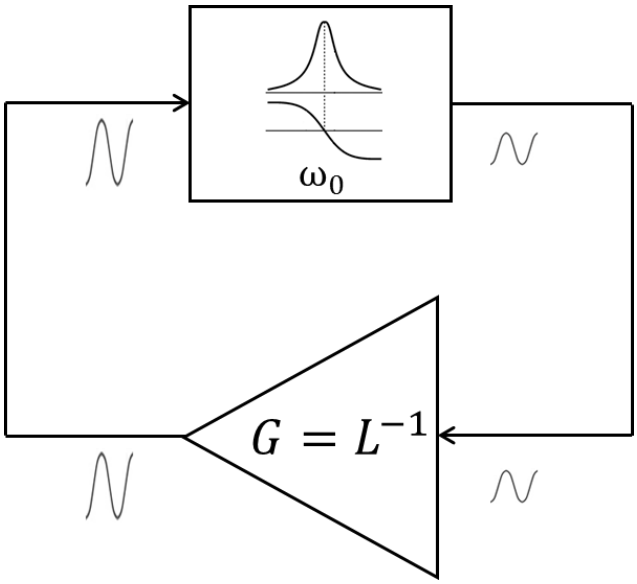

Figure 13. Resonator model

As described earlier, in the presence of injection locking the oscillation frequency is different from natural resonance frequency. To demonstrate this condition, first we can consider the case where a phase shifter is added. According to the Barkhausen Criterion, in order to have a sustainable oscillation there should be zero phase shift around the loop. Thus, the resonator will resonate off the natural resonance frequency at frequency ω_1 to compensate for the added phase shift φ, as shown in Figure 14.

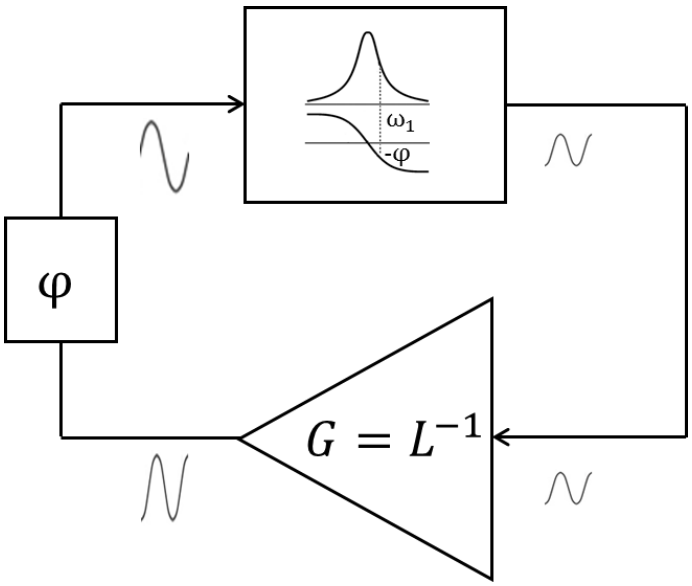

Figure 14.Resonator with a phase shifter in the loop resonating off the resonance frequency

For a parallel RLC tank we have:

$$Z_{RLC} = \frac{R}{1 + jR(\omega C - \frac{1}{\omega L})} \qquad (2)$$

The tank phase shift φ can then be written as:

$$\tan(\varphi) = -R(\omega C - \frac{1}{\omega L}) \qquad (3)$$

Near the resonance frequency $\omega_0 = \frac{1}{\sqrt{LC}}$, the phase shift introduced by tank can be approximated as:

$$\omega_1 = \omega_0 - \frac{\omega_0}{2Q}\tan(\varphi) \qquad (4)$$

The oscillator can only oscillate at a new frequency of ω_1 if the gain block provides sufficient gain to compensate for the higher loss resulting in the tank circuit at this frequency. This condition is equivalent to the uniform motion in the pendulum and rotating drum example. In the case that the gain block cannot provide sufficient gain to sustain the oscillation, the oscillator output frequency will be modulated. The oscillator in this case experiences a quasi-periodic behavior while the frequency varies between ω_0 and ω_1. This can only be explained by the nonlinear behavior of the oscillator.

A more realistic model of the injection locking is shown in Figure 15. It should be noted that the coupling can take place at any part of the oscillator loop. Similar to the phase shifter model in Figure 14, the coupling of the oscillators will lead to a non-zero phase shift that must be compensated by the resonator.

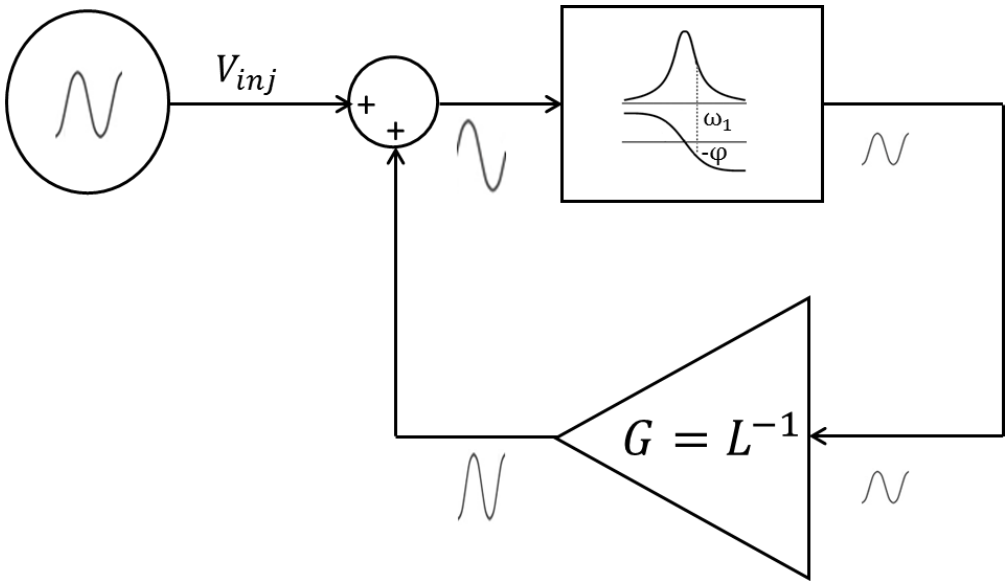

Figure 15. Injection Locking model in electrical oscillators

At a relatively low injection strength, the phase shift will increase by increasing the injection strength. It is also a function of the frequency difference between the resonance frequency of the tank and the injected signal. Depending on the values of the gain and the loss of the tank at the injection frequency, either pulling or injection locking can be expected. If the Gain Unit can provide enough gain to sustain oscillation at the new resonance frequency, injection locking will take place. At lower values of gain the system might not satisfy the Barkhausen Criteria, and therefore pulling occurs. The system will then alternate between the two conditions of having sufficient gain and zero phase shift periodically.

2.3 Injection Locking in Electrical Oscillators

Vector analysis can give more insight into the analysis of injection locking. As was described above, injection locking takes place when the loop oscillates off the natural resonance frequency to compensate for the extra phase shift exerted in the loop by the injected signal. As shown in Figure 16, the phase shift exerted by V_{inj} will be compensated by the counter clockwise rotation of V_{osc}, as shown in the Figure 17 diagram.

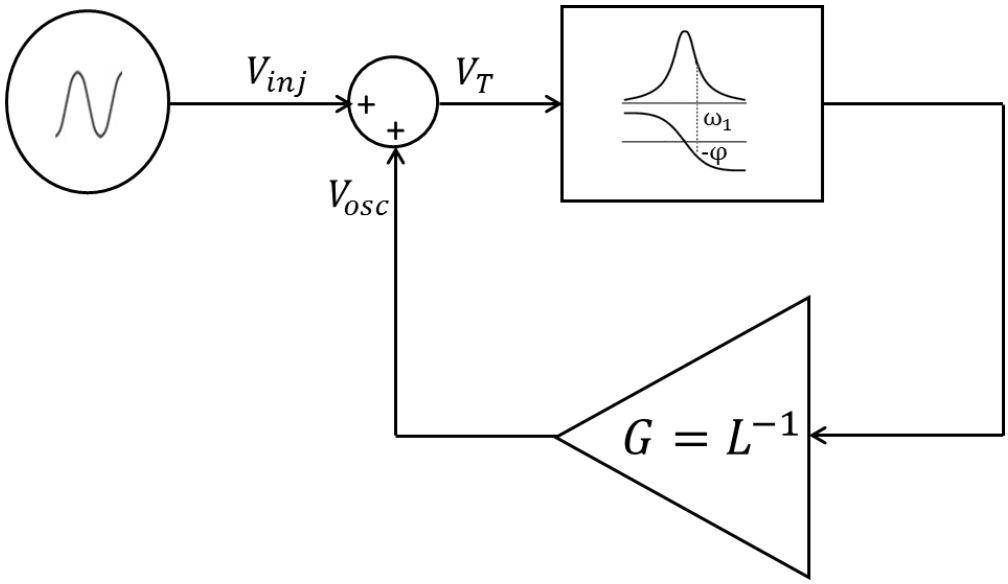

Figure 16. Oscillator under injection

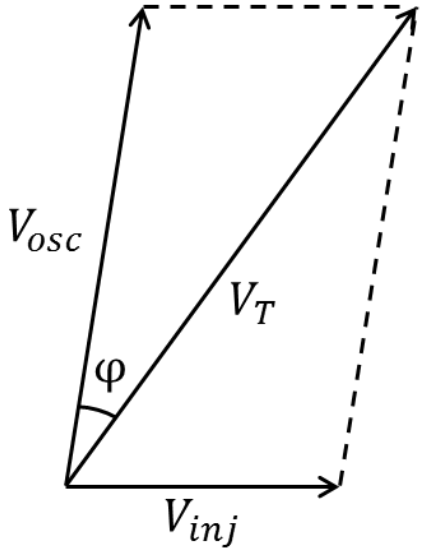

Figure 17. Injection Locking vector analysis

The injection strength can be defined as the ratio of the injected signal to the available signal $\frac{V_{inj}}{V_{osc}}$. By increasing the injection strength, V_{osc} continues its counterclockwise rotation

to compensate for the extra phase shift until V_T becomes perpendicular to V_{inj}, as shown in Figure 18. At this point, further increase of the injection strength will not increase the exerted phase shift ϕ and, therefore, will no longer change the frequency of oscillation. We note that for an LC oscillator, the frequency range can be translated to phase change near the oscillation frequency by the linear approximation in (5). The edge of the injection locking, which is called one-sided locking range ω_L, can be shown to be equal to (6) using a procedure similar to that in [8].

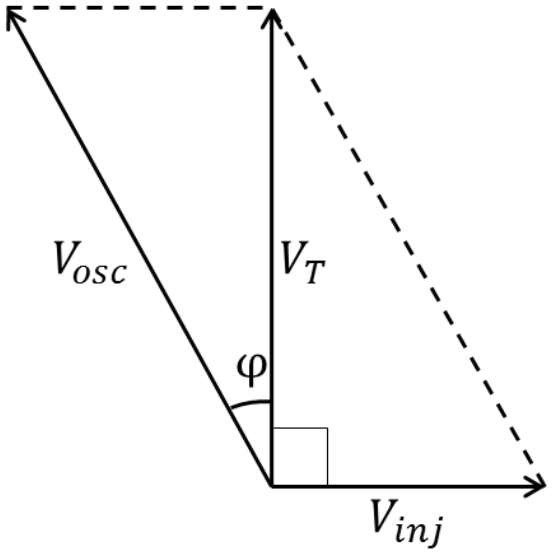

Figure 18. Maximum phase shift resulted from injection

$$\tan\varphi = \frac{2Q}{\omega_0}(\omega_0 - \omega_1) \qquad (5)$$

$$\omega_L = \frac{\omega}{2Q}\frac{V_{inj}}{V_{osc}}\frac{1}{\sqrt{1-\left(\frac{V_{inj}}{V_{osc}}\right)^2}} \qquad (6)$$

For low injection strength, $\frac{V_{inj}}{V_{osc}} \ll 1$ we have:

$$\omega_L \cong \frac{\omega}{2Q}\frac{V_{inj}}{V_{osc}} \qquad (7)$$

Where ω_0 is the natural resonance frequency, ω_1 is the frequency of the injected signal, ω is the oscillation frequency, Q is the quality-factor of the tank and V_{osc} and V_{inj} are the oscillator and the injected voltage amplitudes, respectively. The locking range is a function of the VCO tank quality factor, the oscillation frequency, and the injection strength.

2.4 Injection Locking Jitter Analysis

Once the oscillator becomes injection locked to an incoming data signal, the phase locking prevents jitter accumulation due to the phase correction with each data transition. The phase correction takes place only in the locking range; therefore, the input jitter transfer function has a low-pass behavior. Considering the vector diagram in Figure 19 the phase variation in output voltage θ_e due to the input noise V_n can be calculated. The output offset frequency $\Delta\omega$ due to injection locking is no longer a constant in this case.

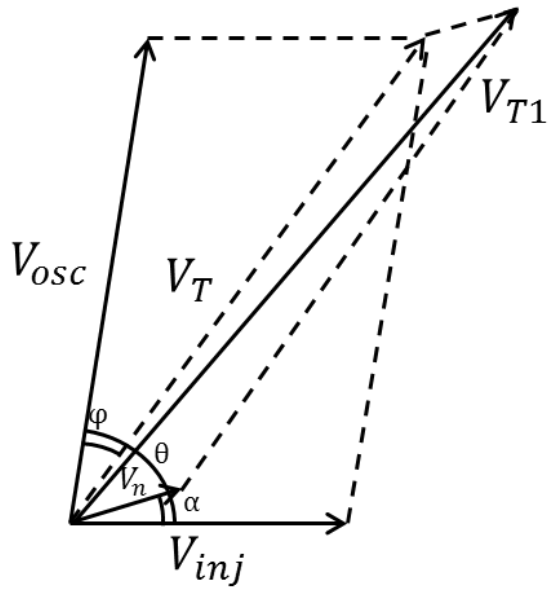

Figure 19. Injection locking jitter analysis

$$v_n(t) = V_n\cos((\omega_0 + \omega_n)t + \varphi_n) \qquad (8)$$

$$\Delta\omega = \Delta\omega_0 + \frac{d\varphi}{dt} \qquad (9)$$

where ω_n and φ_n are the offset frequency and phase, respectively. For low injection strength, (5) can be estimated as:

$$\varphi = \frac{2Q}{\omega_0}(\Delta\omega) = \frac{2Q}{\omega_0}\left(\Delta\omega_0 + \frac{d\varphi}{dt}\right) \qquad (10)$$

$$\theta = \theta_0 + \theta_e \qquad (11)$$

The phase error can then be calculated from the first-order differential equation with a derivation similar to [12]:

$$\frac{d\theta_e}{dt} + [\omega_L cos(\theta_0)]\,\theta_e = [\omega_L \frac{V_n}{V_{inj}} cos(\theta_0)]\,\sin(\omega_n t + \varphi_n) \qquad (12)$$

The bandwidth of the first-order transfer function is $\omega_L cos(\theta_0)$ which is a function of the locking range and the injection signal offset frequency. This bandwidth increases by increasing the injection strength. The maximum bandwidth ω_L happens once the offset frequency is equal to zero where we have $cos(\theta_0) = 1$.

2.5 Injection locking for Clock/Data Recovery

As was described in the previous section, the periodicity of the injected signal was what enabled injection locking. A periodic input signal can introduce a phase shift in the oscillator loop that can lead to injection locking. In clock/data recovery applications, the data is an NRZ random binary signal. This characteristic can be found in most of the transmitted signals as the signals are often sent using a local oscillator. The data therefore can contain periodic zero-crossings depending on the modulation type; these periodic zero-crossings are the tones hidden in the data spectrum. These tones can be extracted from the data using different methods. By injecting the tone within the locking range of the oscillator, injection locking can be achieved.

3. INJECTION LOCKING for CLOCK/DATA RECOVERY APPLICATIONS

In the previous chapter, the theory of injection locking was discussed. The effect of the input noise on the output jitter was discussed. It was shown that injection locking prevents jitter accumulation and an injection-locked oscillator has a jitter transfer function similar to that of a type-I PLL.

In this chapter, the injection locking for clock/data recovery applications is discussed. in Section 3.1. In Section 3.2, the prior art on injection locking-based CDRs will be discussed. The shortcomings of conventional designs, which are mainly due to their tone extraction technique, are described, and full-rate architectures are also pointed out. In Section 3.3, we introduce an innovative architecture for the pulse generation that addresses the challenges at high data-rate injection-locking CDRs and enables 100Gbps data rate.

3.1 Pulse Generation

Ideally the sequence that is being injected to an oscillator for injection locking purposes must be periodic. While a periodic signal can lead to an ideal injection locking scenario, a semi-periodic signal in some cases can also lead to injection locking. A semi-periodic signal has a cyclical behavior that experiences random absence and presence of the cycles. For injection locking, a discrete tone must be present in the spectrum which is the case for a semi-periodic sequence. If the tone is within the locking range of the oscillator it

will guarantee injection locking. In this section, we will describe how we can generate a semi-periodic signal from a NRZ sequence suitable for injection to an oscillator.

There are random polarity changes in the NRZ signal that inherently makes it unsuitable for injection. The polarity of the transitions at each zero-crossing is random, which can cause the oscillator to come out of its lock condition every time polarity change occurs. This can also be explained by observing the transient waveform of a random NRZ signal. We first observe that a random NRZ signal, as shown in Figure 20(a), can be considered as the superposition of a sequence of 0101 pulses with occasional polarity changes and a sequence of random pulses, as shown in Figure 20 (b) and (c), respectively.

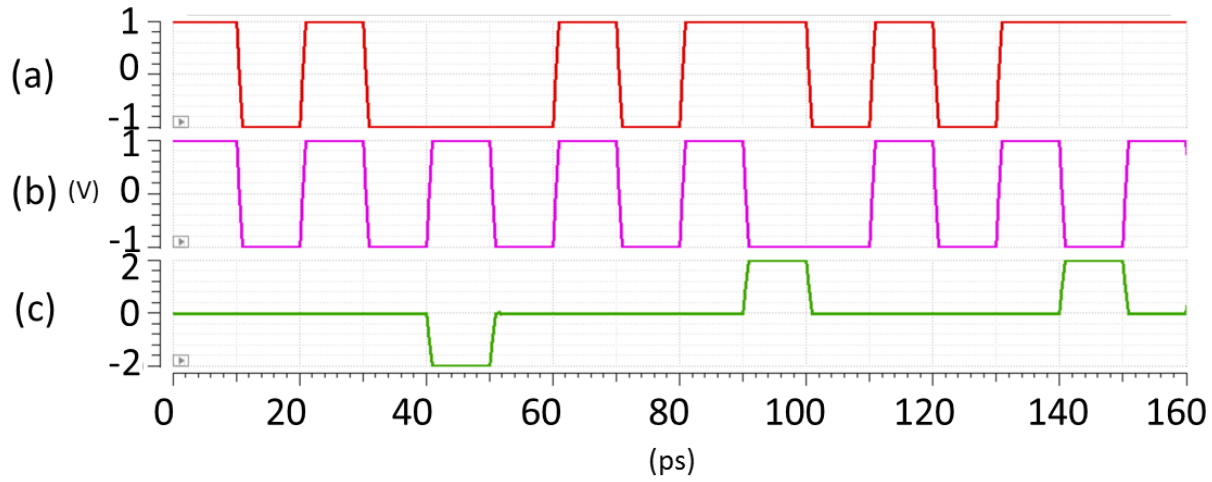

Figure 20. (a) NRZ signal; (b) 0101 pulses with phase change; (c) random pulses.

As shown in Figure 20(b) the phase-varying 0101 signal will experience a 180° phase change each time there is an even number of Consecutive Identical Digits (CIDs) present at the input data. The spectrum of the NRZ signal and phase-varying 0101 pulses are shown in

Figure 21 and Figure 22, respectively. It is worth mentioning that as was described earlier in Figure 4, the spectrum of a random NRZ signal as shown in Figure 21 contains nulls at $f_0 = \frac{1}{T}$. Here the signal is PRBS7 100 Gbps NRZ signal with $T = 10ps$ so the nulls are at 100GHz and its harmonics.

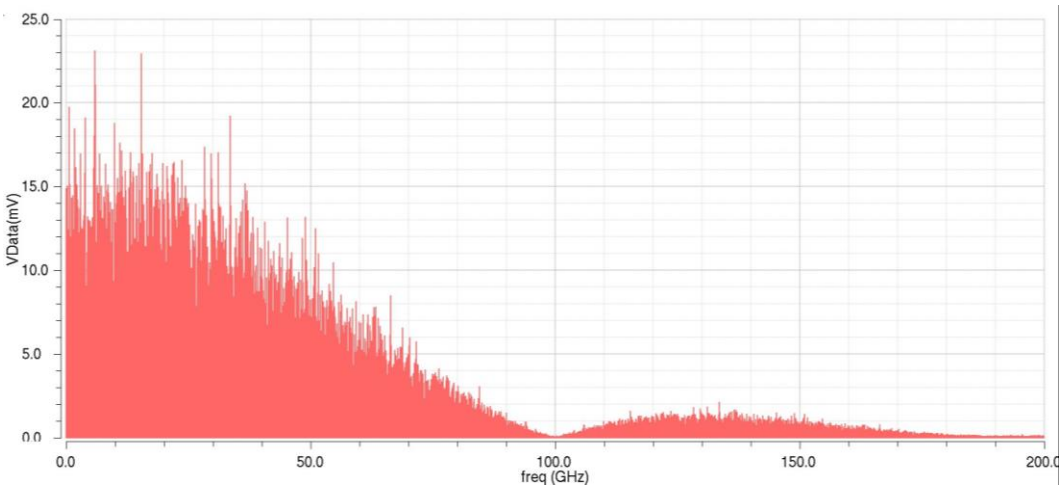

Figure 21. Spectrum of the PRBS7 100Gb/s data

Because of the occasional phase changes, the spectrum of the phase-varying 0101 sequence shown in Figure 22, which is centered at the baud rate, does not contain a discrete tone. The spectrum in Figure 22 looks similar to a phase modulated signal as the result of the random polarity changes.

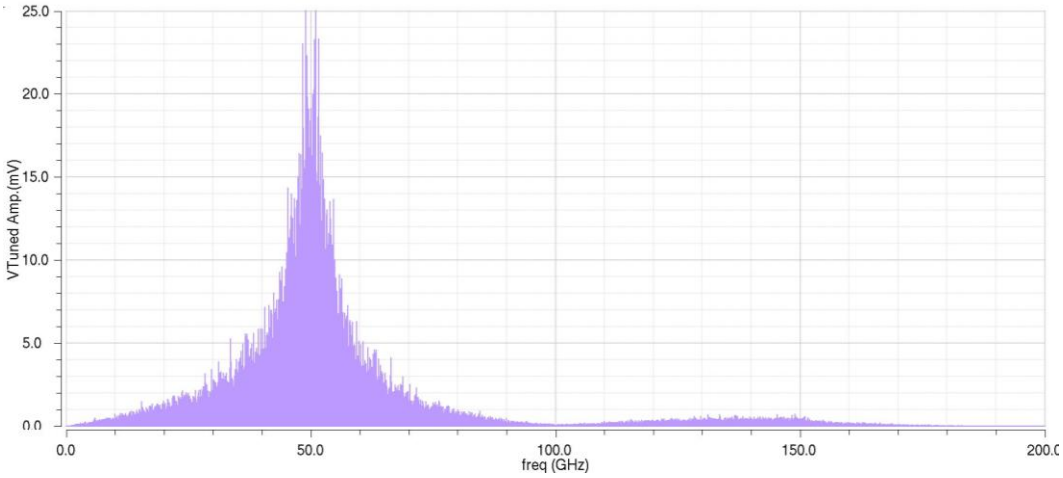

Figure 22. Spectrum of the phase-varying 0101 sequence, a phase modulated 50 GHz signal

If we were to use the phase-varying 0101 sequence for injection locking purposes, the occasional phase changes in the sequence would bring the oscillator out of lock every time the 180° phase change occurs. Neutralizing the polarity changes in Figure 20(b) sequence and creating a 0101 sequence from it, would be ideal for clock recovery purposes.

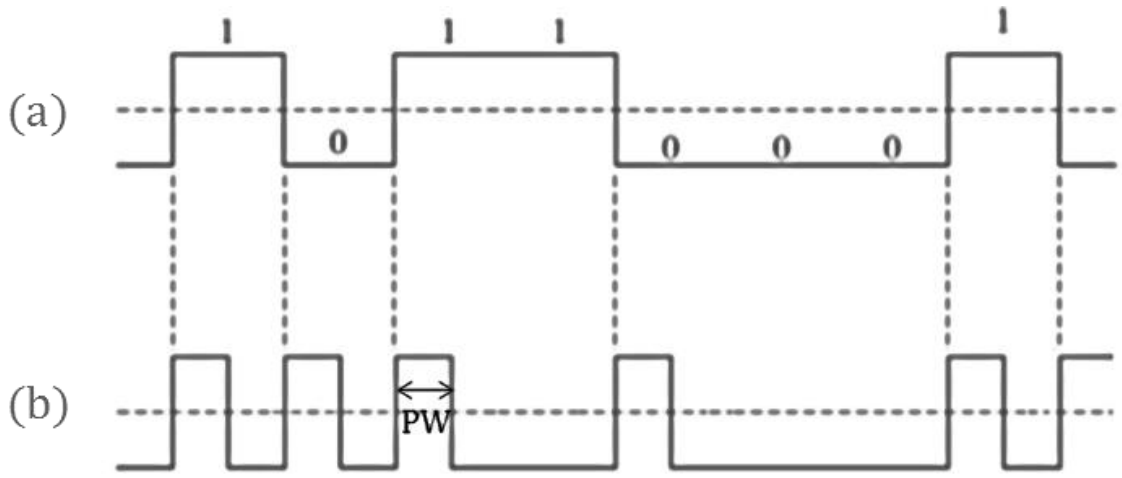

Figure 23. (a) Random NRZ sequence (b) Neutralized generated pulses from random NRZ sequence suitable for injection

One way to achieve this is to first convert the transitions in the data into pulses and then neutralize the pulses if necessary, as shown Figure 23. The spectrum of Figure 23 (b) contains a tone at $f_0 = \frac{1}{T}$, unlike the original random NRZ input data that has a null at f_0. The power of the tone at f_0 would be a function of the pulse width (PW) and the number of pulses. The Figure 23 (b) signal is suitable for injection locking as it is a neutralized signal. In the following section, we will discuss how this conversion has been done conventionally in prior art.

3.2 Pulse Generation in the Prior Art

A standard way to perform such a conversion, as was used in [9], [13], [14], [15] and [16] is illustrated in Figure 24, where the data signal is XORd with a delayed version of itself to generate positive pulses corresponding to all input transitions, regardless of polarity. Therefore, the signal will be neutralized with this method and there is no need for a separate stage for neutralization. The spectrum of the resulting set of pulses will have a component at the full-rate frequency, which can then be applied directly to the VCO to achieve injection locking. The work described [9] was designed for a 20 Gbps input data sequence and used a full-rate 20 GHz clock.

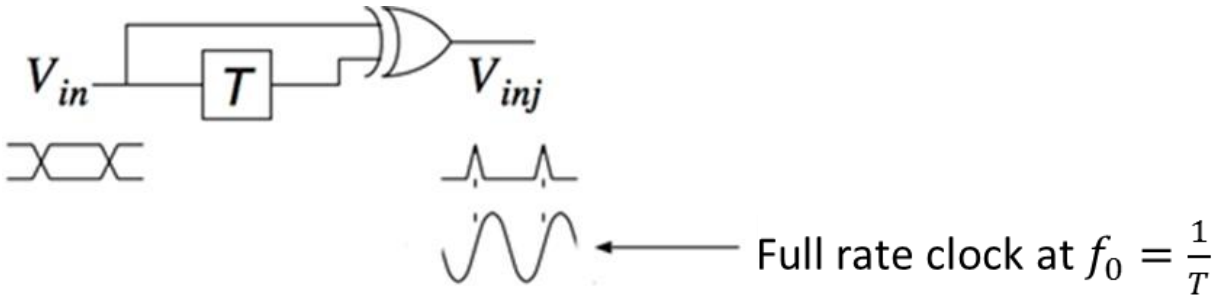

Figure 24. XOR based pulse generator and the output waveform

As was described in the previous section, the power of the generated tone will be a function of the pulse width and number of pulses (equal to the number of the transitions in the input data). The effect of pulse width can be understood by considering the spectrum of a series of random pulses that follows a sinc function spectrum. As illustrated in Figure 25 [9], a half bit-period pulse would exhibit the maximum power at the tone at $f_0 = \frac{1}{T}$ while a quarter-bit period exhibits a twice wider spectrum with lower magnitude. For both cases, the impulses would occur at $f_0 = \frac{1}{T}$ as it is the repetition frequency of the pulses and therefore the number of zero-crossings.

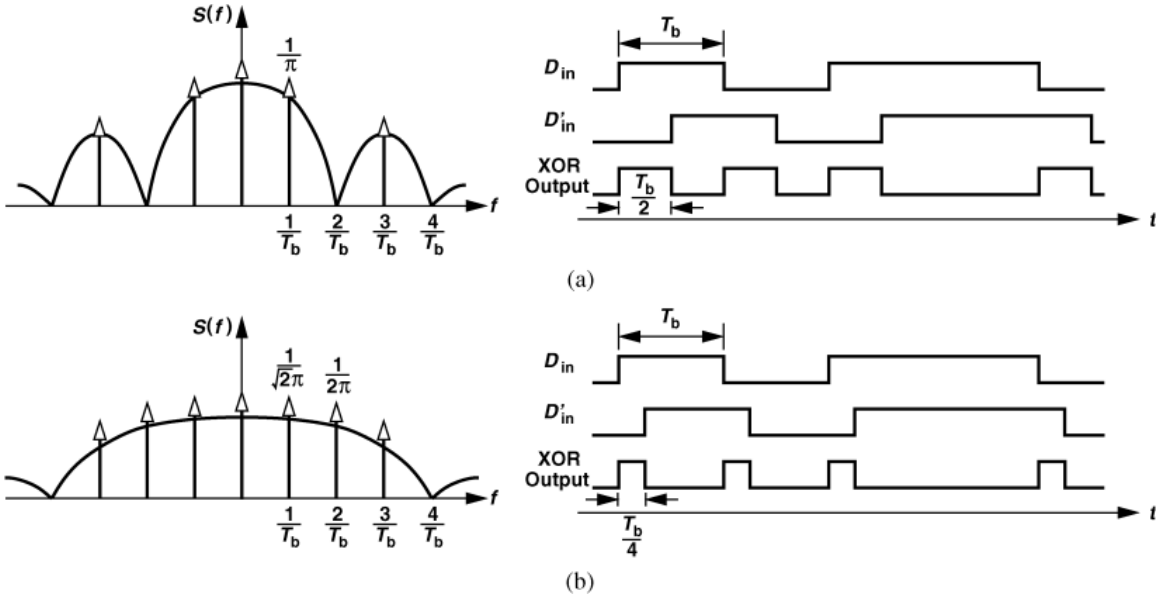

Figure 25. Half-period and quarter-period pulses [9]

An oscillator can lock to such a tone if it is within the locking range. It is worth noting that a half-period pulse would make more sense for design, as it generates the strongest tone as shown in Figure 26.

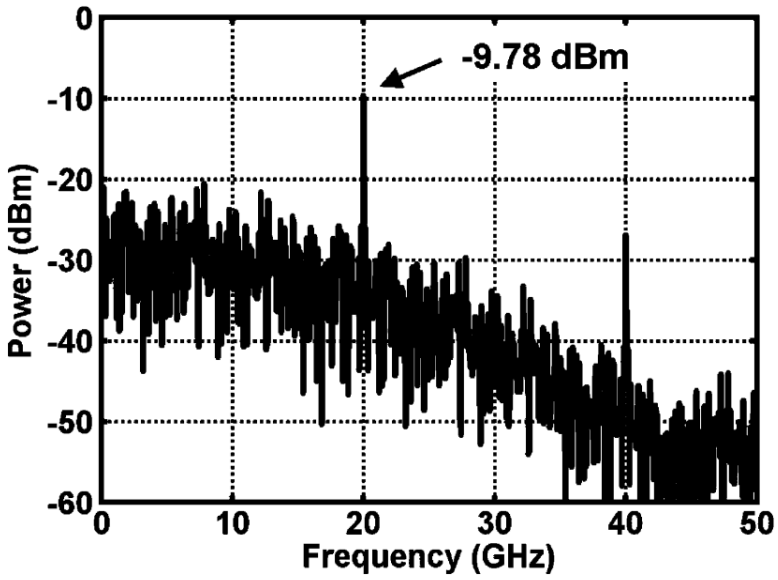

Figure 26. Spectrum of the half-period pulse sequence [9]

The tone is at $f_0 = \frac{1}{T} = 20GHz$, which is the full rate clock of the input data. Thus, the output of the pulse generator V_{inj} had to be applied directly to the VCO outputs in order to achieve injection locking. The architecture is therefore a full-rate architecture that requires all other blocks to work at the full-rate frequency. By bringing the VCO frequency close to the tone frequency, once the tone falls within the locking range of the VCO, locking takes place. To tune the VCO frequency, MOSCAPs and capacitor banks are employed to change the resonance frequency of the LC tank of the VCO.

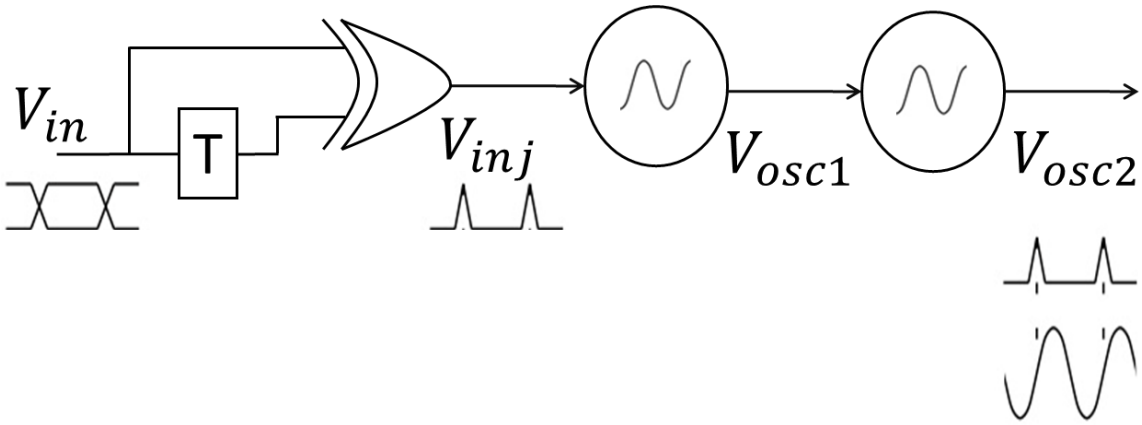

Figure 27. Injection locking based scheme in [9]

At higher speeds, however, it becomes more difficult to generate short pulses corresponding to data transitions, with a signal power high enough to lock the VCO frequency. At 100 Gb/s the unit interval is only 10ps for an NRZ signal, and thus the pulse that corresponds to data transitions must have rising and falling times of only a few

picoseconds. The delay value is a strong function of PVT variations, therefore a half-period pulse that can generate the strongest tone is not always practical.

Applying these pulses directly to the tank at the VCO output, as was done in [9], can be problematic. In particular, it requires a full-rate CDR since the tone is at the full-rate clock frequency. In a full-rate CDR all blocks, such as the phase detector, clock divider, and buffers, must work at the full-rate frequency, which increases the power consumption substantially. This will also limit the maximum possible data rates achievable with this scheme. The injection signal level must be sufficiently large, the connection will add more parasitic capacitance to the tank, and this direct connection will cause some amplitude modulation in the VCO output, thus increasing the jitter. To reduce the amplitude noise caused by the injection circuitry at the output of the VCO, another VCO was injection-locked to the main VCO in [9] as shown in Figure 27, adding further parasitic to the output of the VCO. In addition, this method would further limit the injection locking range as the mismatch between the two oscillators causes frequency shift at their outputs.

3.3 Pulse Generation in the Proposed Architecture

As was described in the previous chapter, an XOR-based pulse generator can have a number of shortcomings when used at higher data rates, since it becomes more difficult to generate short pulses, corresponding to the input data transitions, with a signal power high enough to lock the VCO frequency. At 100 Gbps the short unit intervals indicate that pulses must have a rising and falling time of only a few picoseconds. As was discussed in the

previous section, the delay value of the XOR based pulse generator must be equal to the half of the period of the signal to achieve the strongest injection level. The delay value in an XOR-based pulse generator is a strong function of PVT variation, and thus a half-period pulse that can generate the strongest tone is not always practical. The resonant injection circuit, shown in Figure 28, can overcome these challenges.

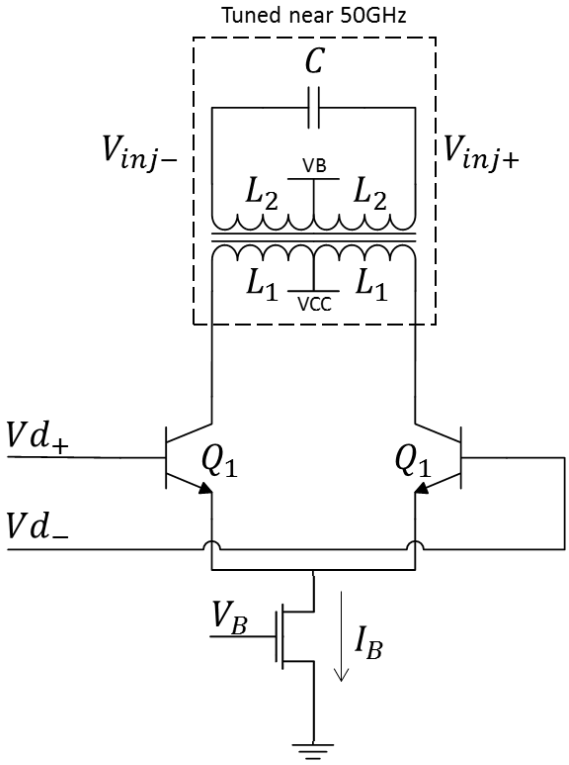

Figure 28. Resonant pulse generator (Tuned Differential Amplifier)

The use of resonance circuitry for clock/data recovery applications was first introduced in [17]. The resonant pulse generator circuit can be realized as a tuned amplifier shown in Figure 28. This amplifier is tuned at 50 GHz, corresponding to the baud rate of a 100 Gbps NRZ signal, and will generate a high-amplitude half-rate clock while filtering out

the unwanted random components. To neutralize the polarity variation in the 0101 signal, the output of the tuned amplifier V_{inj} is applied to a simple rectifier circuit, shown in Figure 29, which serves as a frequency doubler. The current at the output of the rectifier I_{rect}, will have a strong, low-jitter tone at 100 GHz with no polarity change; Its spectrum is shown in Figure 30.

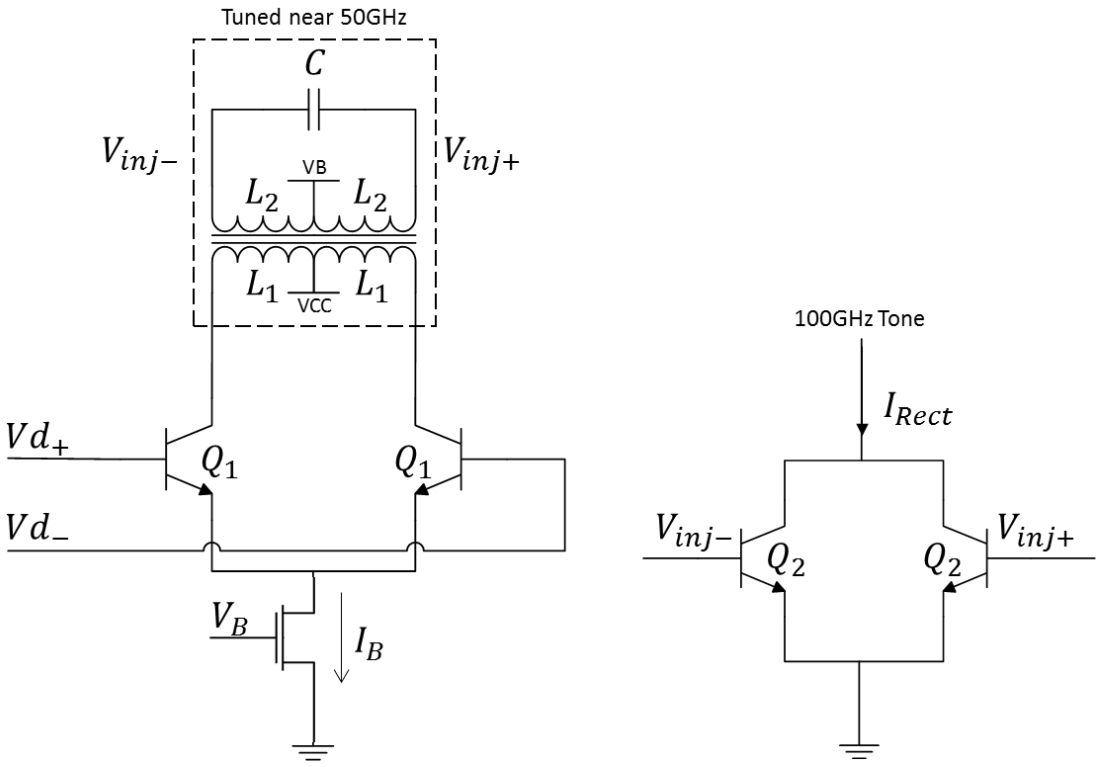

Figure 29. Injection circuit

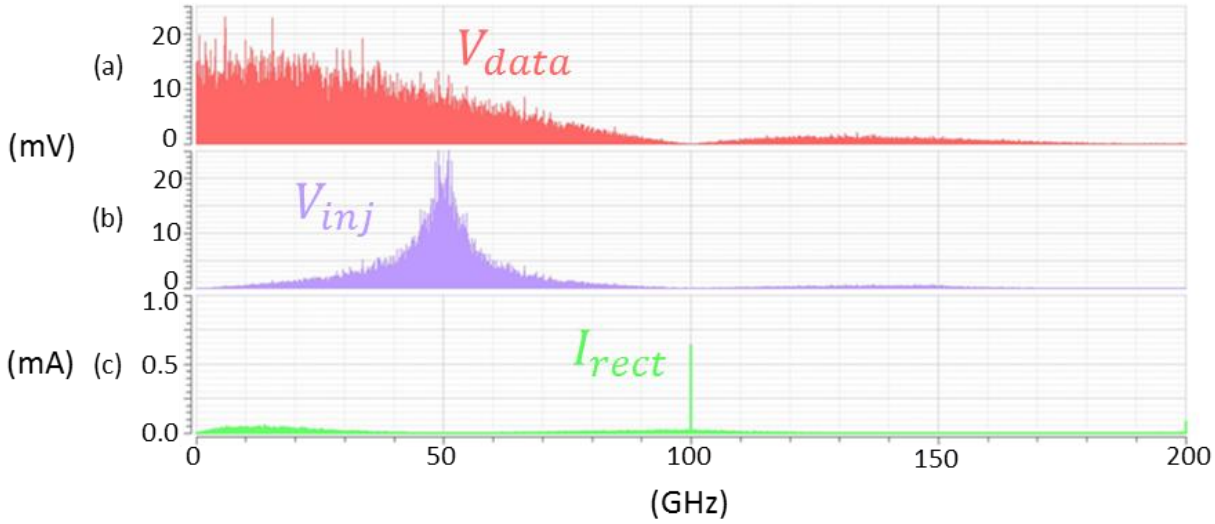

Figure 30. Resonant injection circuit spectrum for 100 Gbps PRBS7 input data (a) Input signal (b) Pulse generator step response (c) Rectifier output spectra

Simply using a tuned amplifier alone is not sufficient to produce an appropriate injection signal because the data is random and the output pulses will alternate between positive and negative polarity. For this reason, design of both the tuned amplifier and the rectifier is required. It should be noted that the resonant pulse generator always achieves the maximum injection level similar to the half-period pulses generated by the XOR-based counterparts. The resonance frequency of the tank is dictated by the passive values of inductor and capacitor that is less PVT sensitive compared to the delay generated by the active circuits. Therefore, unlike the XOR-based pulse generators, this optimal point is robust against PVT variations.

3.3.1 Circuit Model and Analysis

The pulse generator stage, shown in Figure 31, first presented in [18], converts each transition in the input data to a pulse. This stage is tuned near the half-rate frequency of 50 GHz to maintain a high pulse amplitude; Thus, some ringing will occur as well. Having this stage tuned at 50 GHz maximizes the injection strength as it generates pulses with $\frac{T}{2} = \frac{1}{2*f} = \frac{1}{2*50GHz} = 10ps$ for each data transition. As explained in [9] the injection level changes for different pulse widths. For a half-period pulse, which can be achieved by tuning the resonance circuitry at 50GHz, the maximum injection level can be achieved. The pulse generator block can be modeled as an ideal transformer with a parallel resistor that models all the losses as shown in Figure 31.

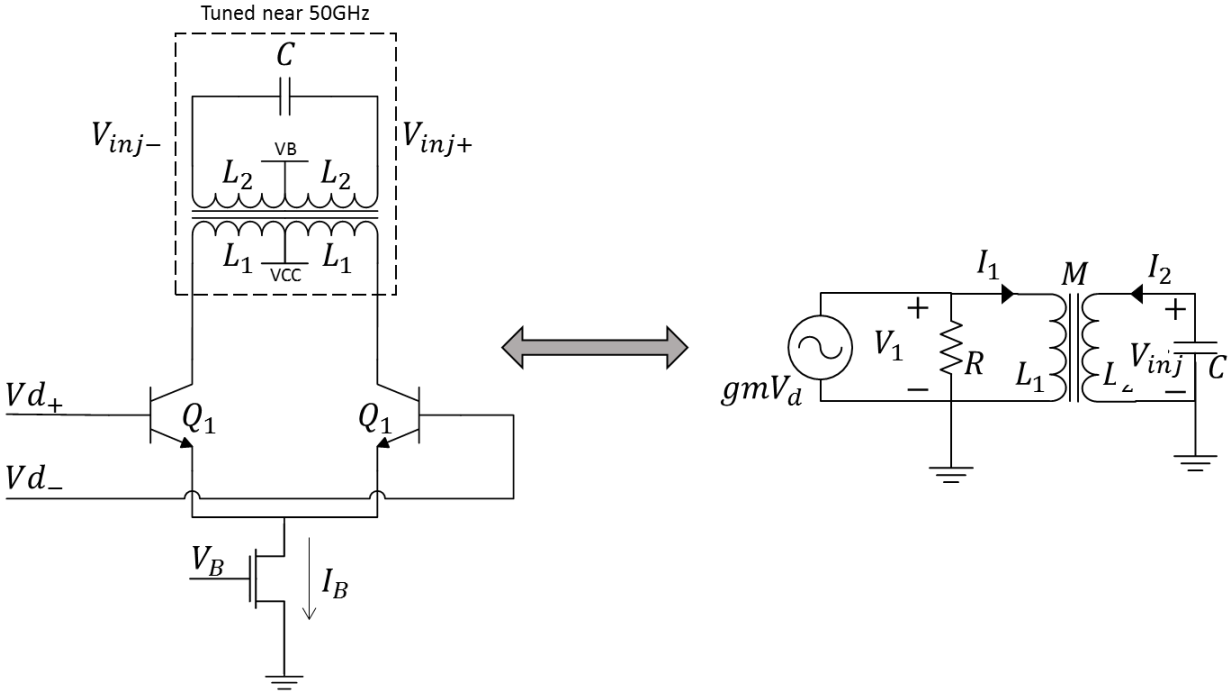

Figure 31. Pulse generator equivalent circuit model

The circuit has a third-order transfer function.

$$V_C = \frac{Ms}{(L_1L_2 - M^2)\frac{C}{R_1}s^3 + L_2Cs^2 + \frac{L_1}{R_1}s + 1} I_{in} \qquad (13)$$

where k is the inductor coupling coefficient; $L_1$and L_2 are the primary and the secondary inductance values, respectively; R_1 is the primary series resistance; and C is the capacitance in Figure 31. The step response of the circuit in Figure 31 is shown in Figure 32 for a tank with the following parameter values.

$L_1 = L_2 = 50pH, k = .8(M = 40pH)$

$R_1 = 100\Omega, C = 200f\text{F}$

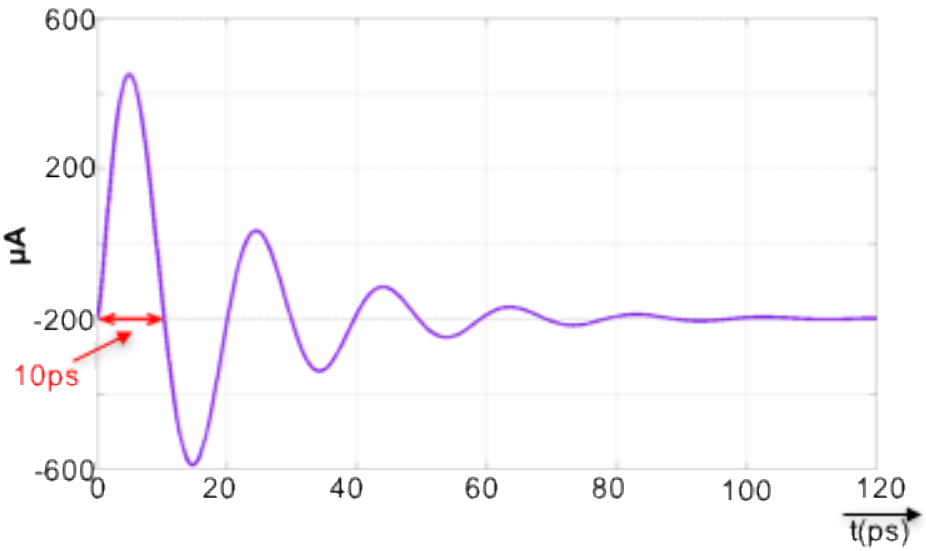

Figure 32. Step response of the pulse generator model

For $k \approx 1$, one of the poles in (13) goes to infinity, and thus the transfer function can be further simplified to be a second-order transfer function for a tank with a high coupling coefficient, since $M^2 = k^2 L_1 L_2$;

$$V_C = \frac{Ms}{L_2 C s^2 + \frac{L_1}{R_1} s + 1} I_{in} \qquad (14)$$

The natural frequency of oscillation ω_n and the damping factor ξ can then be calculated from (15) and (16):

$$\omega_n = \sqrt{\frac{1}{L_2 C}} \qquad (15)$$

$$2\xi\omega_n = \frac{L_1}{R_1 L_2 C} \qquad (16)$$

The tank can be designed to have its natural frequency of oscillation close to 50 GHz, although some mismatching can occur. Due to the underdamped behavior of the second-order transfer function some ringing is expected to occur, as shown in Figure 32. In the ideal case of a high-Q tank, tuned at the baud-rate of the data, the zero crossings of this waveform would be aligned with the zero-crossings of the data. However, the limited quality factor of the tank and PVT variations will lead to misalignment. Although the tank in this case is not operating at the optimum point, this will not introduce any new frequency components in the output spectrum. As studied in [19], the average waveform of a tuned circuit response becomes a damped sine wave with the correct (i.e, equal to the baud rate of the data)

frequency. When Q is large, the damping factor is small and as it reaches infinity, a pure sinusoidal is generated at the output.

3.3.2 Simulation Results

Transient simulation results showing the step response of the *Figure 29* circuit are plotted in Figure 33. The waveform in Figure 33 shows the input signal with a positive and a negative input transition.

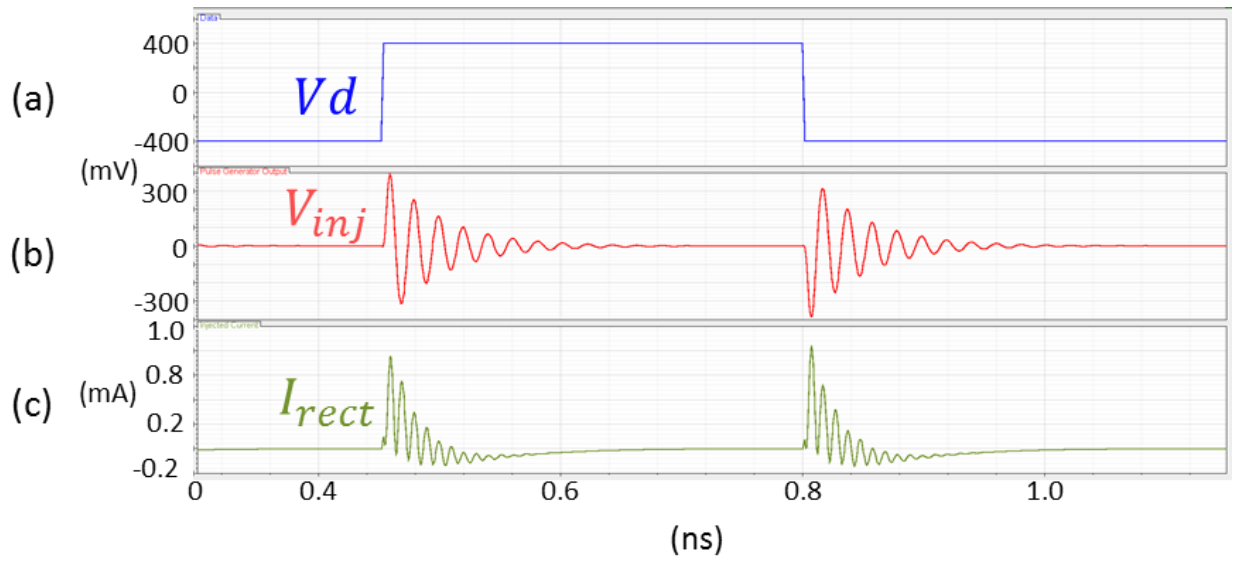

Figure 33. Time-domain step-response of the injection circuit for positive and negative data transitions (a) Input signal (b) Pulse generator step response (c) Rectifier output

The resulting injected and rectified outputs are shown in Figure 33(b) and (c), respectively. The differential pulse signal is applied to the rectifier circuit, whose output current injects a positive pulse regardless of the input polarity. In addition, the injection

circuitry does not capacitively load the tank. This configuration enables injection into a VCO with a half-rate clock signal. The simulated transient waveforms corresponding to 100 Gbps PRBS7 input data are plotted in Figure 34.

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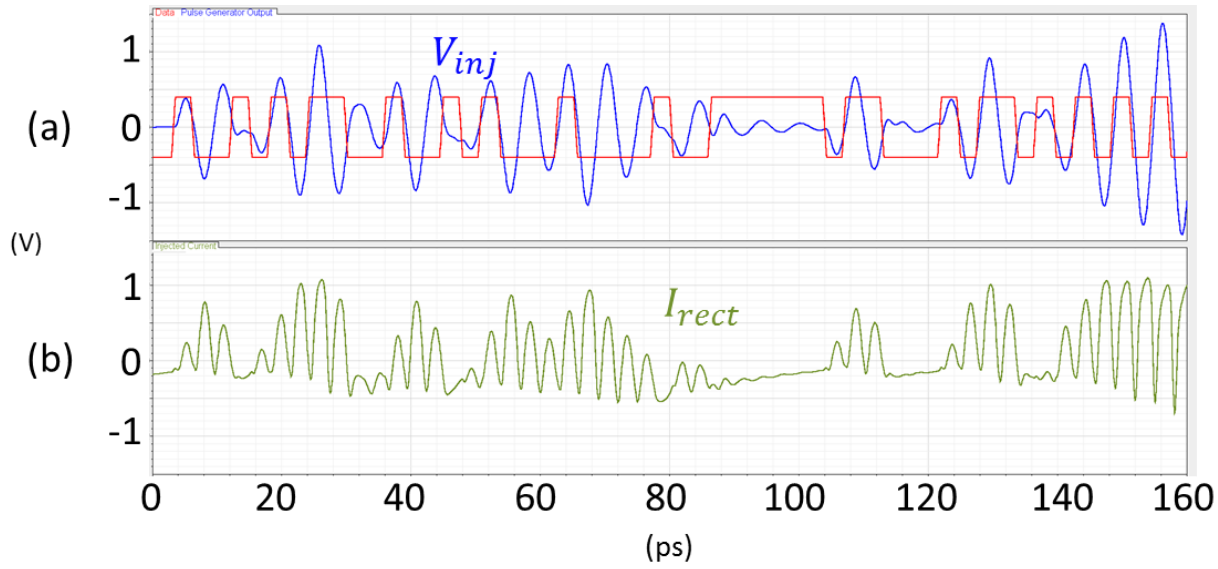


Figure 34. Injection circuit transient output (a) Pulse generator output (b) Rectifier output

An oscillator can be injection locked to the extracted tone in Figure 30 by applying the output current from the rectifier I_{Rect} in parallel with the VCO tail current as shown in Figure 35. The switching behavior of the VCO's cross-coupled pair down-converts the injected signal at the tail to produce the desired half-rate oscillation frequency at the VCO output. This accommodates the injection at the tail of the 50GHz VCO rather than directly into the tank circuit, enabling a half-rate architecture. In this way, the locking takes place with minimal disturbance of the differential output amplitude of the VCO. Zero-bias

fluctuation is accomplished by decoupling through C_{inj}; the bias is provided through L_{inj} as shown in Figure 35. As shown in Figure 35, the VCO outputs drive the common-collector buffers that minimize loading on the VCO output while accommodating appropriate phase shift required by the inductive tuning circuitry, as discussed in the next section.

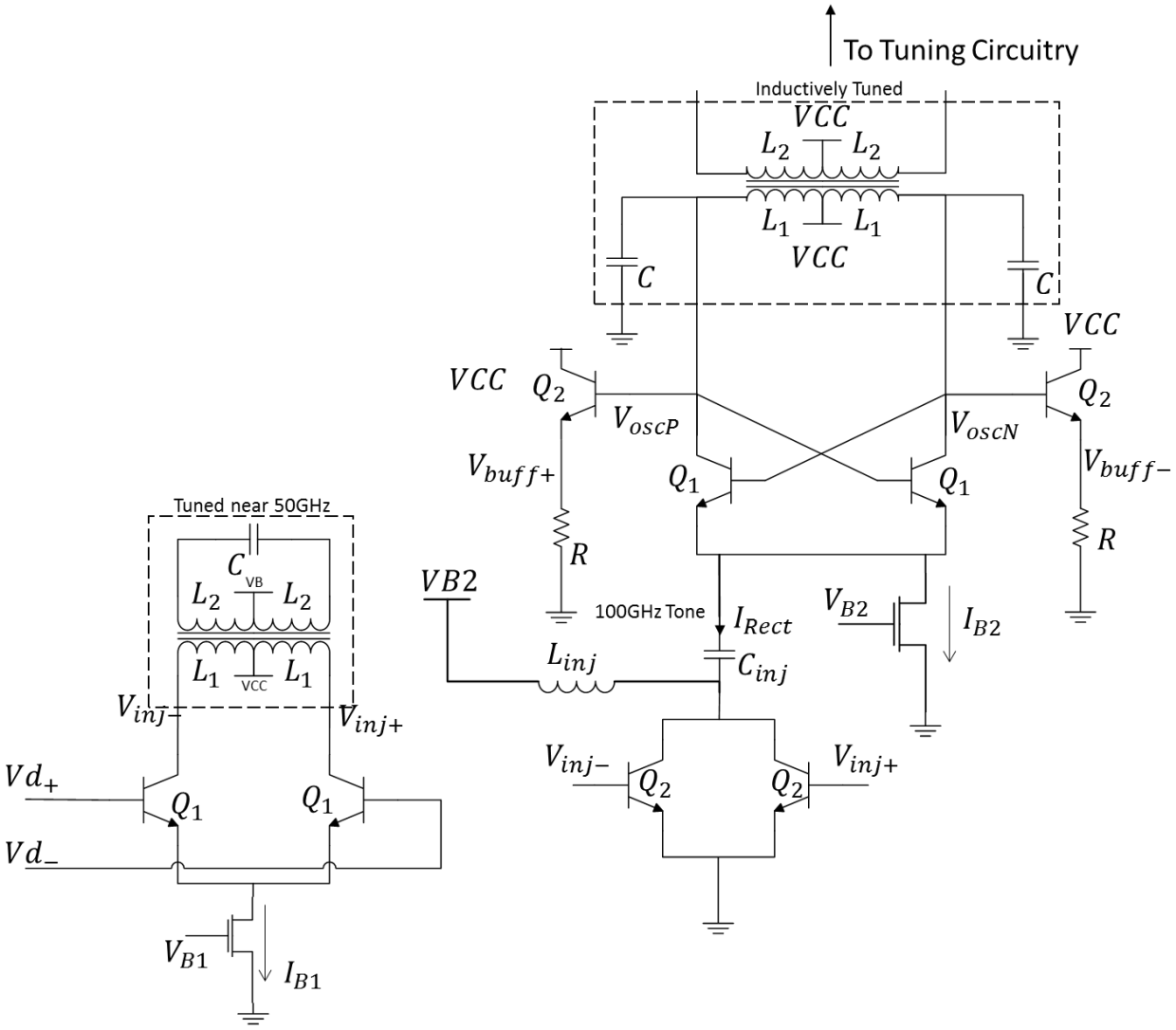


Figure 35. Injection locking VCO schematic

The pulse generator is realized as a tuned amplifier stage that improves the SNR, rather than dealing with accumulated broadband noise in conventional architectures, thereby reducing the jitter of the injected signal. Once the oscillator becomes injection locked to an incoming data signal, the phase locking prevents jitter accumulation due to the phase correction with each data transition. The jitter will be further lowered by the first-order PLL behavior of injection locking [8]. The behavior of the circuit can also be analyzed in the time-domain, similar to [7], by considering the tuned amplifier as a pulse generator block and the rectifier as a nonlinear block to extract a discrete frequency component in the frequency spectra that would not otherwise exist at the output of the pulse generator. However, the analysis in the frequency domain gives more insight into the channel effects, noise and jitter performance analysis.

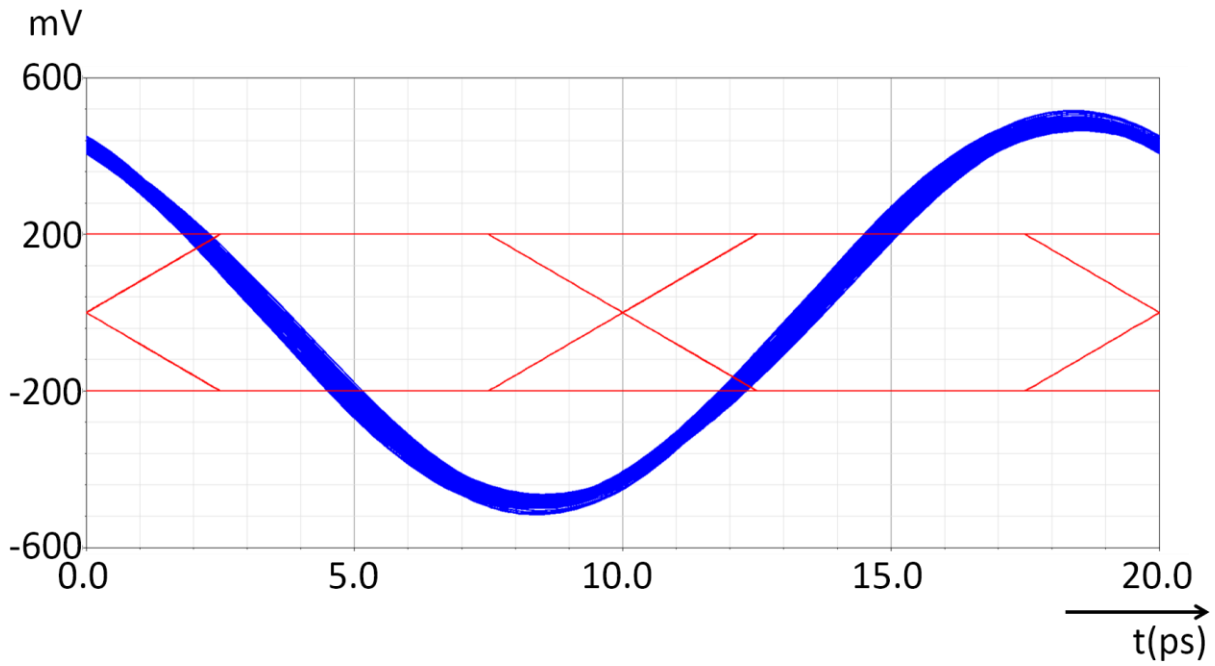


Figure 36. Recovered clock eye-diagram

To demonstrate the efficacy of the injection locking approach, the VCO is designed to self-oscillate at 50.08 GHz (i.e., 80 MHz higher than the locked frequency) when injection is not present. In Figure 34, the simulated signals corresponding to a 100 Gbps PRBS-7 input signal are shown, with the corresponding simulated eye diagrams of the clock and data shown in Figure 36. The open eye of the clock, exhibiting ISI of 0.7 ps p-p, confirms that the injection is effective in locking the CDR. Simulations indicate that locking will occur for a range of VCO frequencies of 50 GHz $\pm$ 80 MHz. The next chapter describes how the frequency capture range can be increased by using a quadricorrelator frequency acquisition approach. Based on VCC = 2 V, the power dissipation of the *Figure 29* circuit is 36.5 mW, corresponding to energy per bit of 0.37 pJ/bit.

4. 100 GBPS HALF-RATE REFERENCELESS INJECTION LOCKING CLOCK/DATA RECOVERY CIRCUIT

In the previous chapters, injection-locking theory and the prior art in injection-locking clock/data recovery circuits were discussed. The limitations of the conventional design were identified. As was discussed, an XOR-based pulse generator faces number of difficulties at higher data rates. A novel pulse generator, based on injection locking, that addresses these shortcomings was introduced.

In this chapter, a referenceless CDR is introduced in Section 4.1, based on injection locking, that does not require an external reference clock, and thus can reduce the form factor of the overall transceiver. An Inductive-tuning technique is used for the frequency tuning of the VCO that allows wide tuning-range and fine resolution at 50 GHz is described in Section 4.2. In Sections 4.3 and 4.4, a high-speed buffer, a variable-delay buffer and their design techniques are discussed. Dynamic D flip-flops employed for retiming purposes that allow 50Gbps data rate are explained in Section 4.5. Section 4.6 is dedicated to the quadricorrelator frequency acquisition loop and its components such as the second-harmonic 100 GHz mixer and the transition detector. In order to test the efficacy of the 100 Gbps CDR, an on-chip 100 Gbps PRBS7 generator was used with dynamic architecture along with 8X clock multiplier that are both explained in Section 4.7.

4.1 Referenceless Injection Locking CDR Architecture

The proposed architecture of the 100Gbps injection locking clock/data recovery circuit is shown in Figure 37. In this architecture, a half-rate inductively-tuned VCO is injection locked to the 100 Gbps NRZ input data. A resonant injection circuit is employed to extract a discrete frequency tone from the input data sequence suitable for injection locking. The same injection circuit is used in the quadricorrelator mixers to expand the frequency acquisition range. The VCO output is shifted by 45° using a delay line to generate orthogonal signals at its second harmonic at 100 GHz. The VCO output and its phase-shifted version are then applied to the second inputs of the second-harmonic 100GHz mixers. The mixers generate lead/lag signals with respect to each other depending on the VCO frequency and the input data half-rate clock offset polarity. A D flip-flop will work as a lead/lag detector to detect the offset polarity. The output of one of the mixers is also used as a clock that drives a 6-bit counter, which will bring the VCO frequency close to the extracted tone frequency. Once the injection locking takes place, the output of the mixer becomes a dc signal that will no longer generate a clock signal for the counter. At this point, the frequency acquisition loop becomes stable. The phase locked output of the VCO can then be used as the recovered clock, which also drives the retimer. In the following sections, each building block of the CDR is explained.

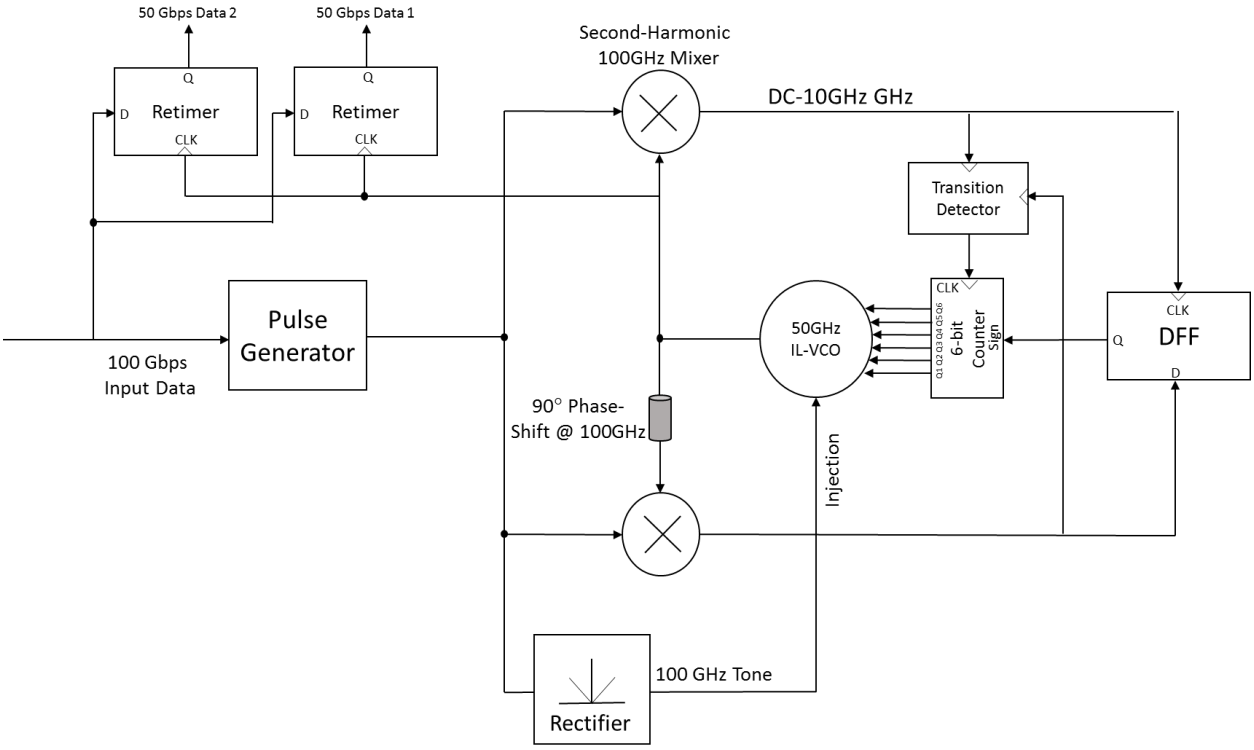


Figure 37. 100Gbps injection locking-based clock /data recovery block-diagram

4.2 VCO Frequency Tuning

The oscillator is a critical block in the CDR design, as it is crucial for phase/frequency adjustments and its performance has an important impact on the overall system performance. Therefore, LC oscillators are often preferred over ring oscillators due to their superior phase noise performance.

4.2.1 Capacitive Tuning

At higher frequencies, the quality factor of the LC VCO tank is limited by the quality factor of the varactors and capacitor banks, while they also limit the tuning range due to associated parasitic capacitances. The quality factor of varactors is as low as 2 for a 50GHz VCO [20]. The capacitor banks are also very difficult to realize at these frequencies as the high R_{on}xC_{off} (~700fs in the available process) of switches leads to a tight tradeoff between the tuning range and the quality-factor. Considering the MOSFET parasitic capacitances in Figure 38 as a switch in the capacitor bank, we have:

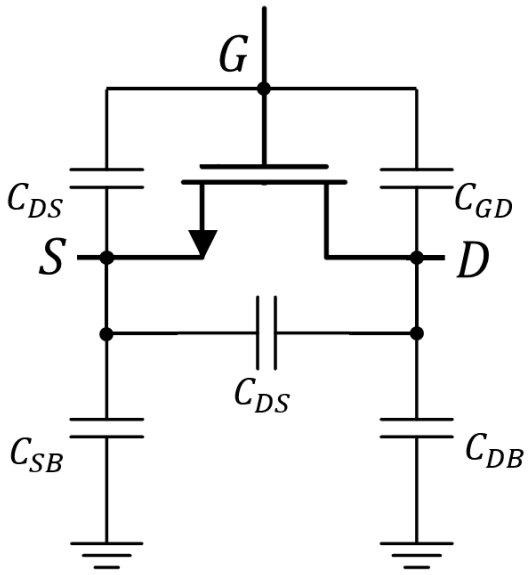


Figure 38. MOSFET as a high frequency switch

$$R_{on} = \frac{1}{\mu_n \frac{W}{l} C_{ox} V_{ov}} \qquad (17)$$

where $V_{ov} = V_{gs} - V_t$ Considering the parasitic capacitances at the drain of the transistor the C_{off} can be calculated:

$$C_{off} \cong C_{GD} + C_{DB} \qquad (18)$$

$$C_{GD} \cong \frac{\varepsilon_{ox}}{t_{ox}} w l_{ov} \qquad (19)$$

where l_{ov} is the gate-drain overlap and ε_{ox} and t_{ox} are the oxide primitivity and thickness, respectively. Assuming that the drain parasitic capacitance is dominated by the diffusion capacitance we have:

$$C_{DB} \cong C_j w l_D \qquad (20)$$

$$C_j = C_{j0}(1 + \frac{V_{SB}}{\psi_0})^{-M_j} \qquad (21)$$

where, C_{j0} is the junction capacitance at zero bias, M_j is the junction grading coefficient, typically between 0.5 and 0.33 depending on the abruptness of the diffusion junction, ψ_0 is the built-in potential that depends on doping levels, w and l_D are the drain width and length respectively.

Multiplying (17) and (18), we have:

$$R_{on}\text{x}C_{off} = \frac{(C_j l_D + \frac{\varepsilon_{ox}}{t_{ox}} l_{ov})l}{\mu_n C_{ox} V_{ov}} \qquad (22)$$

The $R_{on}\text{x}C_{off}$ constant in (22) is a process-dependent parameter. To lower the switch resistance, w must be increased, which increases the drain diffusion capacitance; therefore, the $R_{on}\text{x}C_{off}$ remains constant.

4.2.2 Inductive Tuning

Inductive tuning methods, which have been employed in recent works [20] and [21] give a wide tuning range with a tank quality factor that is dominated by that of the inductor, even at very high frequencies. By injecting into the secondary coil of a transformer a tunable current proportional to the current at the primary coil, the resulting effective inductance seen at the primary of the transformer can be varied, as shown in Figure 39. To derive the input impedance of this circuit, similar to that in [21], we begin by expressing the impedance parameters of the two-port network formed by the coupled inductors:

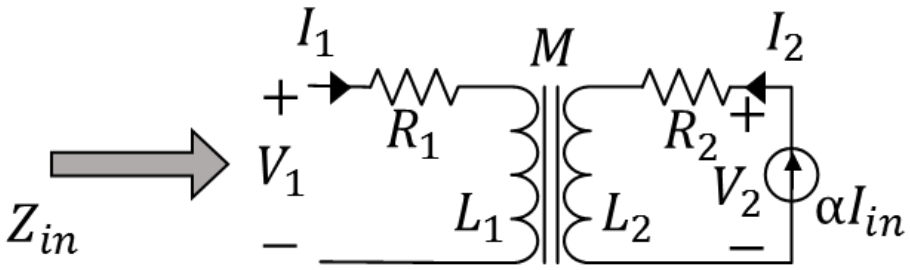


Figure 39. Inductive Tuning Model

The port constraints are given as:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{bmatrix} j\omega L_1 + R_1 & j\omega M \\ j\omega M & j\omega L_2 + R_2 \end{bmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \quad (23)$$

Substituting $I_2 = \alpha I_{in}$ into the first equation of (23), we have:

$$V_1 = j\omega(L_1 I_1 + \alpha M I_1) + R_1 I_1 \quad (24)$$

The impedance Z_{in}, and the input inductance L_{in}, can then be calculated as:

$$\frac{V_1}{I_1} = Z_{in} = j\omega(L_1 + \alpha M) + R_1 \quad (25)$$

$$L_{in} = L_1 + \alpha M \quad (26)$$

$$\frac{L_{in}}{L_1} = 1 + \frac{\alpha M}{L_1} \quad (27)$$

where L_1 and L_2 are the primary and the secondary inductance values, R_1 and R_2 are the primary and the secondary series resistances, and M is the mutual inductance. As shown in (

27), the effective inductance at the input can be varied by varying the α coefficient. In practice, sampling the current of the primary can be difficult and disturb the tank behavior. To generate such a current, instead the output voltage of the primary can be shifted by 90° and then applied to a transconductance cell as illustrated in Figure 40. If we now suppose that current I_2 is derived by phase-shifting V_1 by 90° and multiplying it by a transconductance g_m (i.e., $I_2 = jg_mV_1$), we have:

$$Z_{in} = \frac{j\omega L_1 + R_1}{1 + g_m \omega M} \qquad (28)$$

Using $L_{in} = \frac{imag(Z_{in})}{j\omega}$, we have:

$$L_{in} = \frac{L_1}{1 + g_m M\omega} \qquad (29)$$

Assuming that $g_m M\omega \ll 1$, the tuning range ΔL can then be approximated as:

$$L_{in} \cong L_1 - g_m M\omega L_1 = L_1 - \Delta L \qquad (30)$$

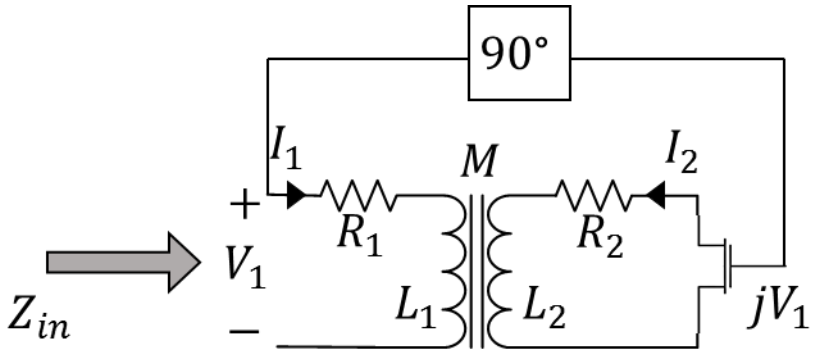


Figure 40. Transformer model

Thus, by adjusting the value of g_m, the effective input inductance $L_{in} = L_1(1 - g_m M\omega)$ can be varied.

To determine the quality factor of the inductive tuning circuit, we have:

$$Q_L = \frac{imag(Z_{in})}{real(Z_{in})} = \frac{\omega(L_1 - g_m M\omega L_1)}{(R_1 - \omega M g_m R_1)} = \frac{\omega L_1}{R_1} \qquad (31)$$

That is, the Q of the variable inductance realized by the Figure 40 circuit is identical to that of the port 1 inductance, independent of the tuned value.

4.2.3 Inductive Tuning Mismatch Analysis

Ideally the phase shift must be equal to 90° to achieve the maximum tuning range. In the case of small values of phase deviation $\Delta\varphi$ in the phase shifter we have:

$$Z_{in} = (j\omega L_1 + R_1)I_1 + jM\omega(g_m e^{j\left(\frac{\pi}{2}+\Delta\varphi\right)}(jL_1\omega + R_1))I_1 \qquad (32)$$

$$e^{j(90+\Delta\varphi)} = cos(\frac{\pi}{2} + \Delta\varphi) + jsin(\frac{\pi}{2} + \Delta\varphi) \cong -\Delta\varphi + jcos(\Delta\varphi) \qquad (33)$$

Substituting (33) into (32), we have:

$$Z_{in} = (j\omega L_1 + R_1)I_1 + jM\omega[g_m\big(-\Delta\varphi + jcos(\Delta\varphi)\big)(jL_1\omega + R_1)]I_1 \qquad (34)$$

$$L_{in} = L_1 - g_m M(\omega L_1 cos(\Delta\varphi) + R_1\Delta\varphi) \qquad (35)$$

The effective inductive turning range and the quality factor can then be derived as:

$$\begin{aligned} L_{in} = L_1 - g_m M(\omega L_1 cos(\Delta\varphi) + R_1\Delta\varphi) &\cong L_1 - g_m M\omega L_1 cos(\Delta\varphi) \\ &= L_1 - \Delta L cos(\Delta\varphi) \end{aligned} \qquad (36)$$

$$Q_L = \frac{im(Z_{in})}{real(Z_{in})} = \frac{\omega(L_1 - g_m M(\omega L_1 cos(\Delta\varphi) + R_1 \Delta\varphi))}{(R_1 - \omega M g_m (R_1 - (\Delta\varphi L_1 \omega))} \cong \frac{\omega(L_1 - g_m M(\omega L_1 cos(\Delta\varphi)))}{(R_1 - \omega M g_m R_1 + \Delta L \omega \Delta\varphi)} \quad (37)$$

By comparing (36) to (29), it can be seen that the effective inductive tuning range is degraded by a $cos(\Delta\varphi)$ factor. For instance, a phase deviation $\Delta\varphi = 10°$ can reduce the effective inductive tuning range by nearly 2%. The effect of phase deviation on Q is more complicated as it depends on the polarity and the value of the frequency offset set by the inductive tuning technique. The excess current injected to the oscillator loop due to the phase deviation can be either in phase or 180° out of phase with the current of the oscillator depending on the frequency offset polarity, which can in turn either enhance or degrade the effective negative resistance generated by the oscillator active circuitry. Therefore, to ensure the proper operation of the oscillator, the active circuitry must be designed to have adequate margin to overcome this excess current resulted by unaccounted mismatch.

Capacitively-tuned VCOs, must be designed for variable values of the quality factor. The variation of the quality factor over the tuning range would cause amplitude and phase noise variations. Achieving a constant quality factor, Q_L, results in less amplitude and phase noise variation, which leads to operation at the optimum point over the tuning-range.

4.2.4 Fully Differential Active Tuning Circuit Topology

The inductive tuning is realized by the circuit shown in Figure 41. Two differential pairs are used in order to realize positive or negative transconductance, which doubles the tuning range. Tuning is set by setting each digital input b_k either high or low, corresponding to binary-weighted current sources as shown in Figure 41. Thus, for this circuit thirty-two frequency bands can be realized. By increasing the number of binary scaled differential pairs the resolution could be increased.

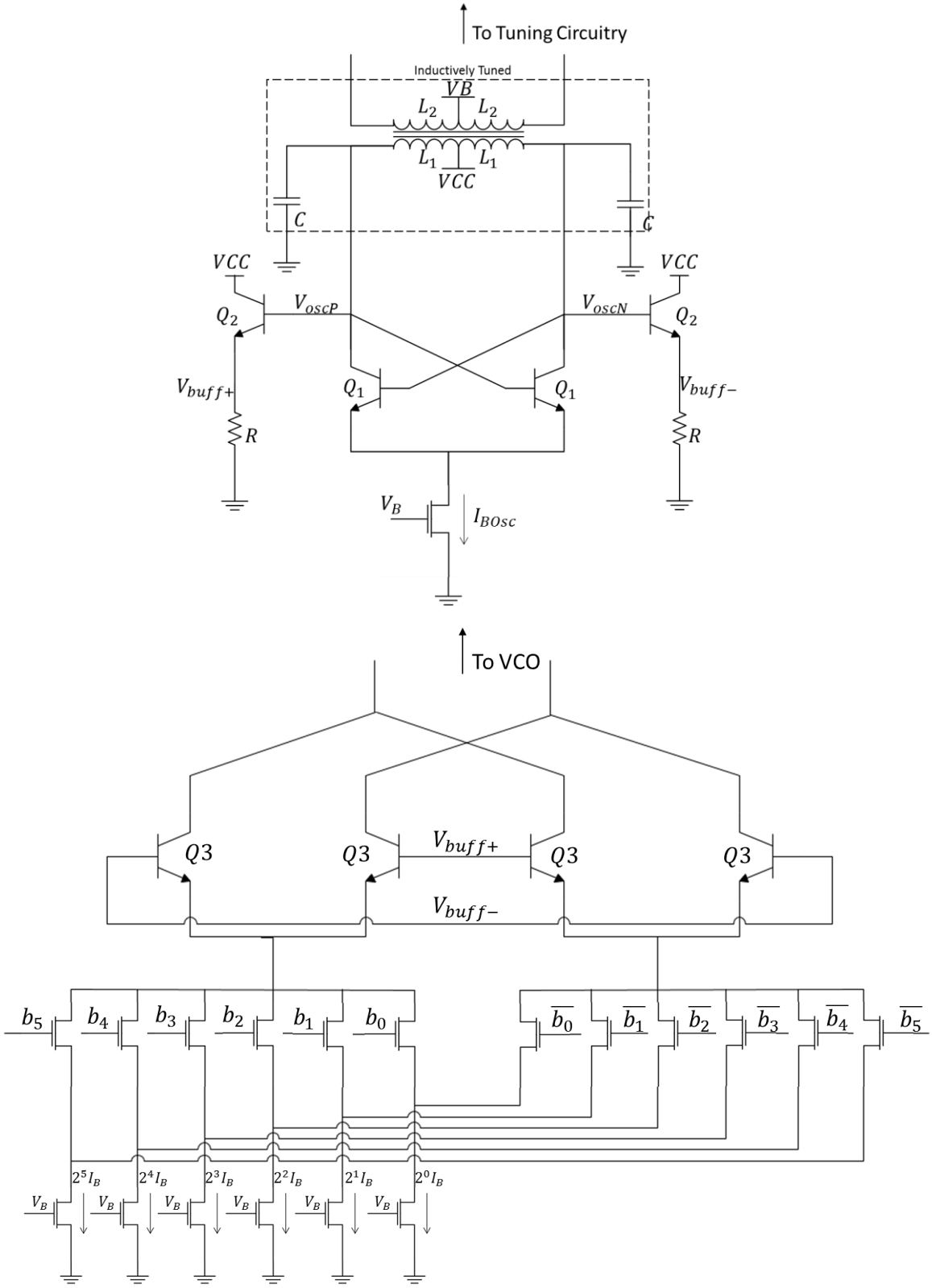


Figure 41. Fully differential active inductive tuning circuitry

The overall phase shift from the output voltage of the VCO to the output current of the tuning circuitry must be near 90° as shown in Figure 41. This phase shift is realized by the connection of the outputs $V_{\text{buff}+/-}$ of the injection-locked VCO to the inputs of the inductive tuning circuit. The capacitance between $V_{\text{buff}+/-}$ to the ground along with the capacitances C_{par}, which is the parallel combination of the layout parasitic and the C_{μ} of the transistors, give rise to a right half-plane zero and a left half-plane pole so that a phase shift between 85° and 95° is realized over the entire VCO frequency range. A more significant value of phase error can lower the tuning range and degrades the quality factor of the tank as was described, but the effect of the +/-5 degree in this case is insignificant.

Accurate EM simulation of the transformer is required as the coupling coefficient and inductor values play important roles in the VCO parameters. In addition, the transformer layout, shown in Figure 42, is critical as the VCO output is driving the active tuning circuitry, which has its outputs connected to the transformer.

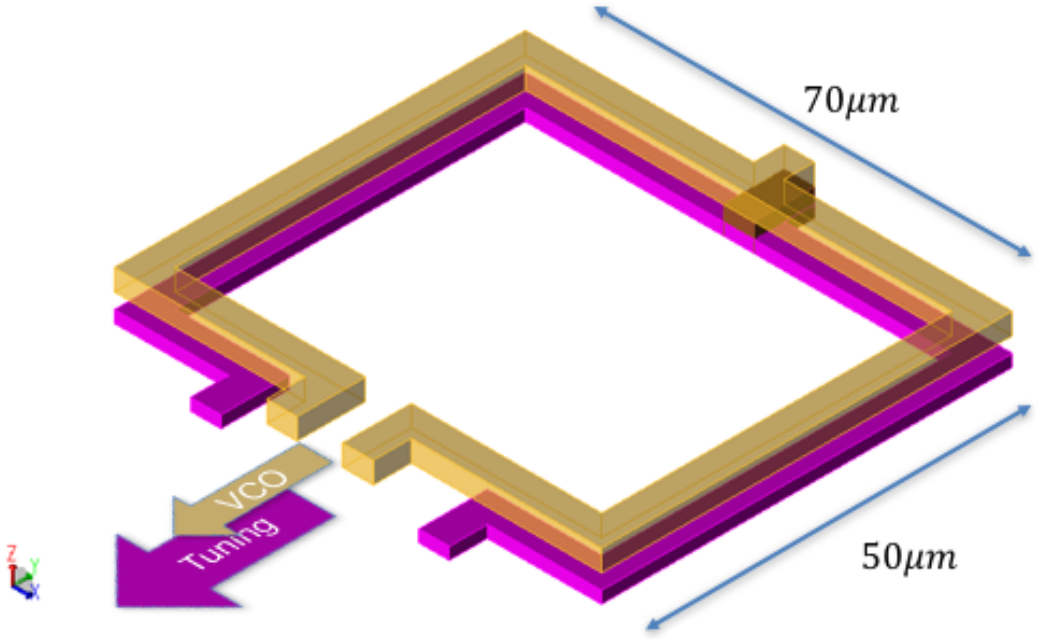


Figure 42. Transformer Layout

4.2.5 Tuning Circuitry analysis

To gain more insight and calculate the values of the circuit components, the differential half circuit is shown in Figure 43. The required 90° of phase shift is achieved through the parasitic from the common-collector buffer, layout parasitics and the tuning circuitry C_{par} and C_{μ}.

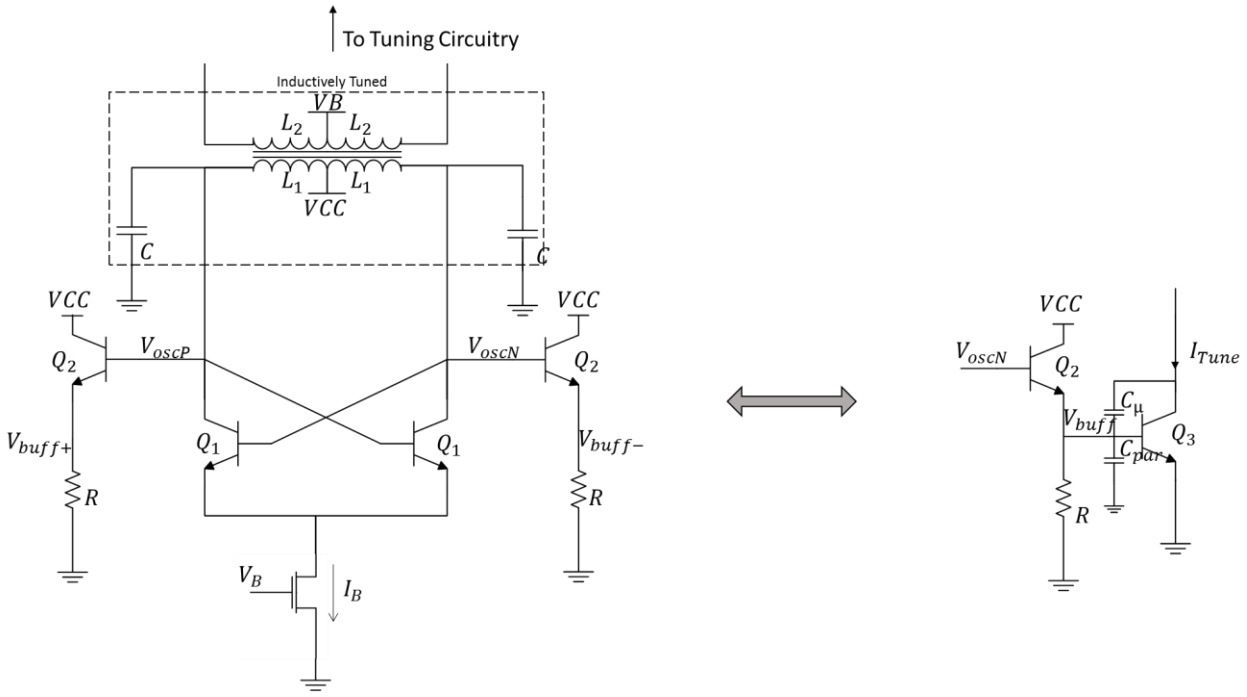


Figure 43. The differential half circuit

The circuit parameters to meet the 90° of phase shift can be calculated by analyzing the half circuit model in Figure 43.

$$V_{buff} \cong \frac{R||\,1/C_{par}j\omega}{R||\,1/C_{par}j\omega + {}^{1}/_{gm_2}} * V_{OscN} \qquad (38)$$

where gm_2 is the transconductance of Q_2. Assuming $\omega \gg 1/RC_{par}$ we have:

$$V_{buff} \cong \frac{gm_2}{C_{par}j\omega + gm_2} * V_{OscN} \qquad (39)$$

We can also write:

$$I_{Tune} \cong \frac{gm_3 - C_\mu j\omega}{1 + Lj\omega C_\mu j\omega} V_{buff} \qquad (40)$$

Substituting (39) into (40), we have:

$$I_{Tune} \cong \frac{gm_2(gm_3 - C_\mu j\omega)}{C_{par}j\omega + gm_2} * V_{OscN} \qquad (41)$$

where we assume that $L\omega^2 C_\mu \ll 1$. Equation (41) shows that the phase shift is a function of gm_2, gm_3, C_{par}, and C_μ. To extract the actual values of the parasitic capacitances, accurate simulation of the layout is required as the phase shift is mostly dominated by the layout routing parasitics.

Assuming the inductive tuning transistor pair works as a pair of switches in Figure 43 (i.e., that the current waveform is a square wave), the maximum tuning range can be derived as:

$$I_{max} = \frac{4}{\pi} I_B \qquad (42)$$

$$V_1 = (j\omega L_1 + R_1) I_1 + j\omega M I_{max} \qquad (43)$$

$$L_{in} = \frac{im(Z_{in})}{j\omega} \approx L_1 - ML_1\omega \frac{I_{max}}{V_1} \qquad (44)$$

$$\frac{L_{in}}{L_1} = 1 - \omega M \frac{I_{max}}{V_1} \qquad (45)$$

In (45), V_1 is the VCO output voltage amplitude and I_{max} is a linear function of tuning circuitry bias current. Therefore, to increase the tuning range for a certain value of VCO output voltage amplitude, this bias current must be increased. This leads to a tradeoff between power consumption and tuning range similar to that of capacitively-tuned VCOs. To plot the VCO tuning range in Figure 44, the control signals b_{0-5} and $\bar{b}_{0-5}$ in Figure 41 are tied to each other and the differential voltage between them is varied between -.5V to 0.5V.

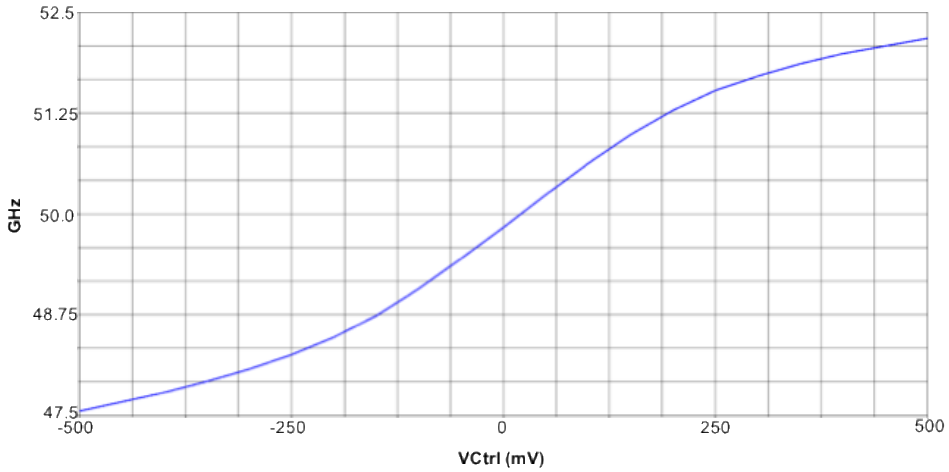


Figure 44. Overall tuning range

The VCO frequency vs. control voltage is shown in Figure 44, demonstrating a ± 5% frequency range overall for a 50GHz VCO with 2.7mA of bias current.

4.2.6 Phase Noise

Phase noise is a measurement of uncertainty in phase and can be measured as the ratio of the noise power within in 1-Hz bandwidth at a certain frequency offset from the oscillation frequency to the total oscillation power. Leeson's equation in (46) is used to calculate the phase noise of the electrical oscillators. In this, F is an empirical fitting parameter from measurement, ω_0 is the oscillation frequency, $\Delta\omega$ is the frequency offset and Q is the overall quality factor of the oscillator tank.

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{sig}}.\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \qquad (46)$$

In passive tuning such as with a MOSCAP, the noise contribution from the tuning circuit only degrades the quality factor Q. On the other hand, in an active inductively-tuned oscillator, the noise contribution from the tuning circuit can be from both passive and active noise sources. The loading effect of the inductive tuning circuit would degrade the quality factor of the transformer. This degradation is due to the loss of the transformer secondary coil as well as the loading of the tuning circuitry output resistance. This can be considered to be a passive noise source and thus can be lumped in to the resonator Q. The active tuning circuitry also contributes to the noise by injecting the noisy current of the tuning circuit into the tank. The tuning circuit generates the current I_{Tune}, that is proportional to the oscillator current, with its noise uncorrelated to that of the oscillator. Therefore, the phase noise follows the pattern in Leeson's equation, as shown in Figure 45, and it adds a variable noise source S to F in (46). The phase noise of the inductively-tuned oscillator can be driven similar to capacitively-tuned oscillator as:

$$L(\Delta\omega) = 10\log\left[\frac{2F_{New}kT}{P_{sig}}.\left(1+\left(\frac{\omega_0}{2Q_{New}\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \qquad (47)$$

where:

$$F_{New} = F + S \qquad (48)$$

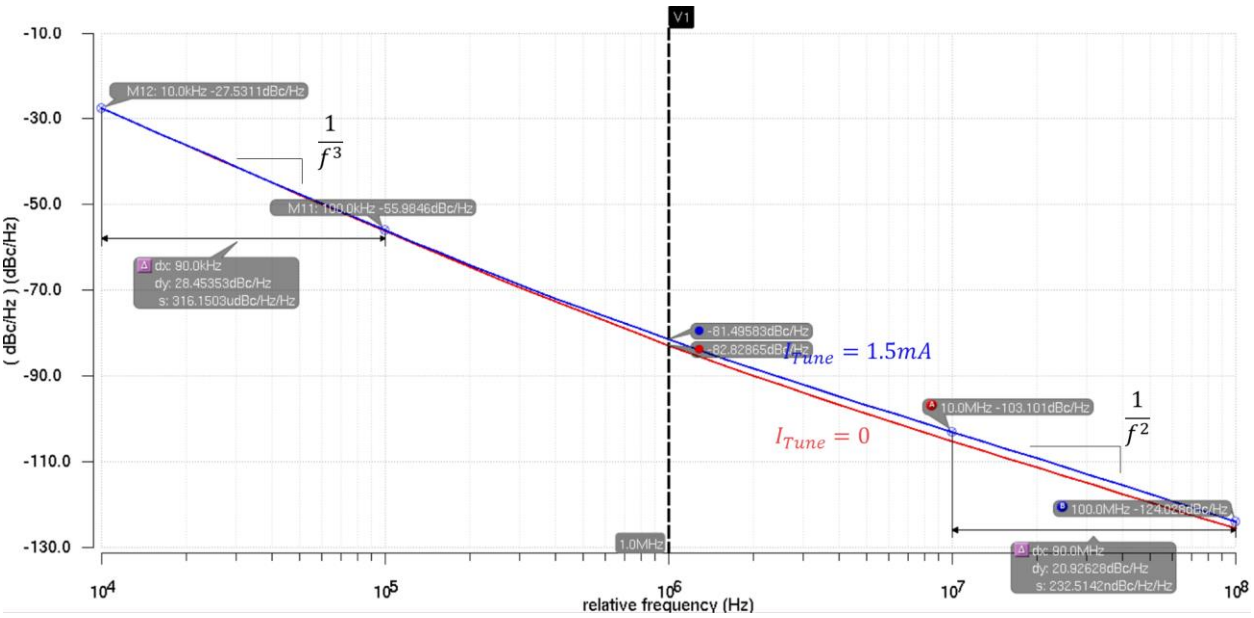


Figure 45. Phase noise simulation result of the inductively-tuned oscillator

F_{New} value depends on the offset frequency and increases with increasing the tuning offset, as it injects higher values of current into the secondary of the VCO transformer. As shown in Figure 45, at maximum tuning offset, the phase noise degradation at 1 MHz offset is $\Delta L(\Delta\omega) = |-81.49 - (-82.82)| = 1.33dB$, which is equal to 35% increase in F value due to the noise from the tuning circuit current.

The minimum phase noise occurs almost in the middle of the tuning-range, which is the resonance frequency of the tank and the inductive tuning circuitry conducts no current

as shown in Figure 46. The simulation shows that phase noise at 1 MHz offset is better than-81dBc/Hz at across the tuning range as plotted in Figure 46.

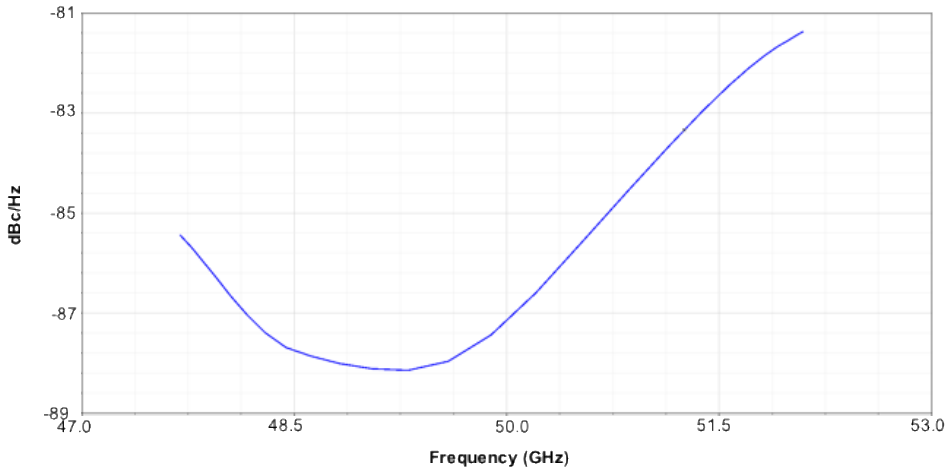


Figure 46. VCO phase noise at 1 MHz offset from oscillation frequency over the frequency range

4.3 High-Speed CML Buffers

Bipolar current-mode logic (CML) circuits have been extensively used for high speed digital and analog applications since the early days of ICs. Bipolar CMLs can reach higher speeds for two main reasons:

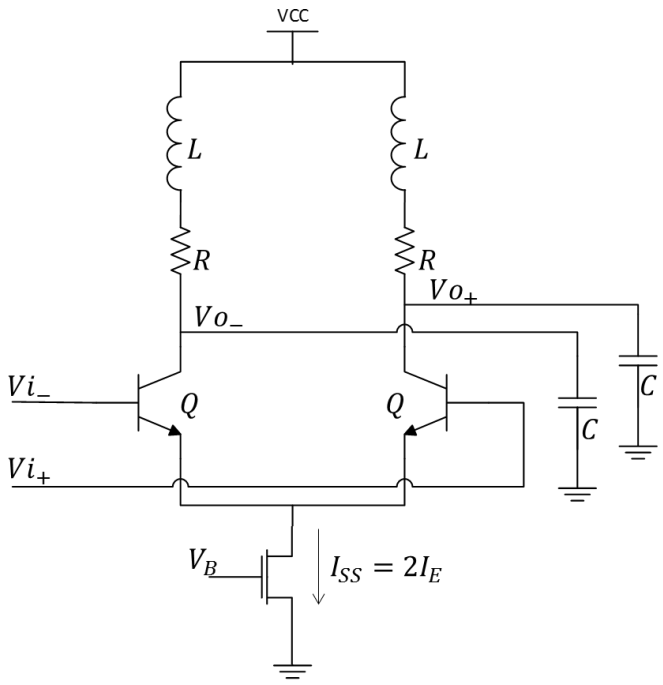


Figure 47. 50GHz Bipolar CML buffer

The first reason comes from the CML architecture, which minimizes the loading of the next stage. In the CML buffers, unlike CMOS buffers, each output of the differential buffer is driving only one transistor from the next stage. On the other hand, a CMOS buffer drives a n-channel and a p-channel transistor simultaneously. In addition, in a CMOS architecture the p-channel transistor is often sized up to compensate for the lower mobility of holes. Therefore, the operation speed of a CMOS buffer is four times slower than the theoretical maximum (f_T) due to n-channel and p-channel gates connected in parallel. In practice, this will lead to almost 2.5 times higher loading of CMOS buffers compared to CMLs [22].

The second reason comes from the fundamentals of the bipolar transistor. To maximize the bandwidth of the buffer it is preferred to bias the device where it achieves the

highest f_T, which can be calculated from (49). Both gm and C_π are proportional to the bias current of the device. The f_T of the bipolar transistor can be calculated as a function of I_C as (50) [23].

$$f_T = \frac{gm}{2\pi\left(C_\pi + C_{je} + C_{jc}\right)} \qquad (49)$$

$$f_T = \frac{1}{2\pi\tau_F}\frac{1}{1 + \frac{kT(C_{je} + C_{jc})}{q\tau_F I_C}} \qquad (50)$$

$$f_{Tmax} = \frac{1}{2\pi\tau_F} \qquad (51)$$

The maximum f_T is limited to (51), which is a function of device geometry in a certain process. At higher levels of current the f_T starts declining as a result of the Kirk effect. The effect is caused by high levels of charge density associated with the current passing through the base-collector region. When the charge density associated with the current becomes comparable to the charge density in the depletion region, the majority carriers will be built up in the region. This effect increases the effective width of the base-collector region [24]. The Kirk effect increases the transient time τ_F of the bipolar and therefore degrades the speed capability of the device. As shown in Figure 48 the maximum f_T occurs at a specific value of current I_{max}, therefore, for a high speed CML it is important to bias the device at this current.

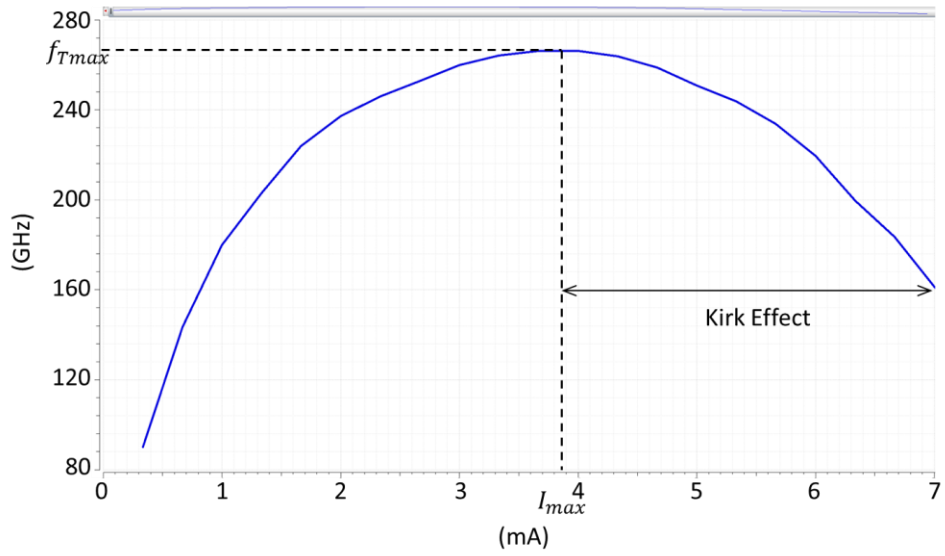


Figure 48. f_T versus collector current I_C

In the CML buffers the devices are biased using the tail current source connected to the emitter-coupled node. Therefore, the device current can be accurately biased close to its optimal point. The ability to bias a device where it exhibits its maximum performance can lead to superior speed capabilities. These advantages all come along with an inherent common-mode rejection due to the differential operation. Therefore, the CML buffers are also very robust in the presence of common-mode disturbance as well.

To further improve the performance and overcome the parasitics due to the connections in the layout, the well-known technique of shunt-peaking is employed. Shunt-peaking enhances the bandwidth by allowing a longer time to charge the capacitors at the output through the shunt-peaking inductor. Adding the shunt-peaking inductor leads to a zero at the location of the original pole and adds a pole at a higher frequency which increases the bandwidth as shown in

Figure 49. The value of the shunt-peaking inductor depends on the output resistance of the buffer and the load capacitance. The optimum value of the shunt-peaking inductor is often between $0.5R^2C$ and $0.7R^2C$ [22], to achieve maximum bandwidth enhancement while avoiding peaking in the frequency curve. In this topology, the inductor value is chosen to be 280pH which is based on $R = 100\Omega$ and $C = 40f$.

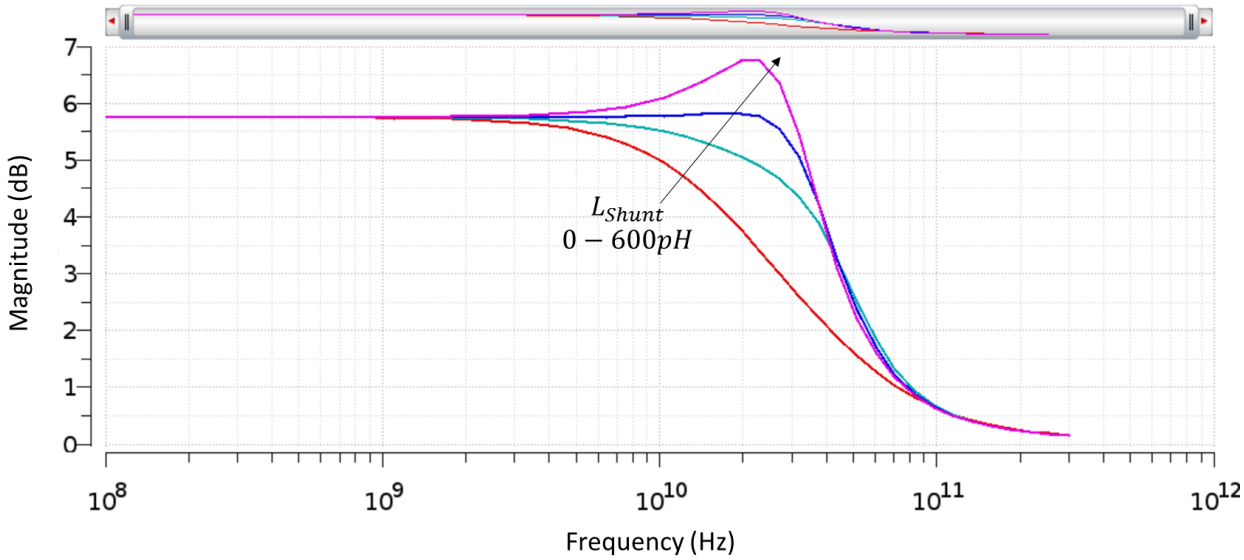


Figure 49. Frequency response of a bipolar CML buffer with different values of Shunt-peaking inductor

The self-resonance frequency (SRF) of the inductor plays an important role as it indicates how much inductance can be effectively added. As a rule of thumb, the SRF should be two or three times higher than the operation frequency. To achieve a higher SRF, the inductors are often realized as a single-ended inductor pair [25]. However, these single-ended inductors are susceptible to mismatch because they take more area. Moreover, the greater area of the inductor leads to longer traces between the output of the buffer and the next stage, which adds to the parasitic capacitance and can lower the bandwidth. In this

work, the inductor is instead realized as a differential inductor, as shown in Figure 50, and the SRF is increased by increasing the distance, d, between the inner and outer turns, and by the use of narrow metal lines, which lower C_s and C_{sub}, respectively, in Figure 50. The lower parasitic capacitance will lead to the SRF improvements.

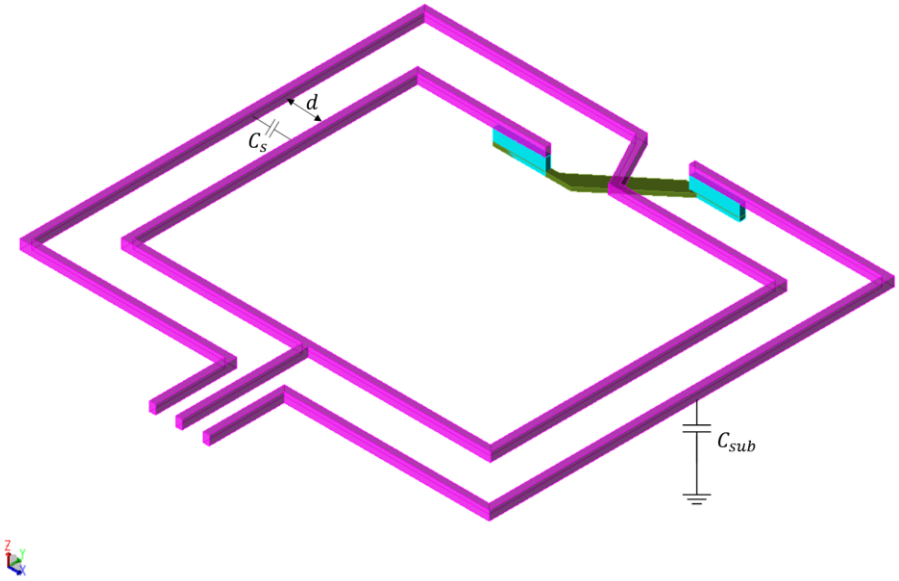


Figure 50. Differential inductor layout for shunt-peaking with high SRF

Shunt-peaking is robust against parasitic elements and the added series resistance and parasitic cap are can be compensated by the shunt-peaking inductor. The extra bandwidth using this method comes at no extra power consumption and the performance improvement comes at the expense of more area.

4.4 Variable-Delay Buffer

In a retimer, it is important to sample the data at the point that it has the highest signal-to-noise ratio. Sampling near the data transitions can lead to metastable behavior and higher bit-error-rate. For an injection-locking CDR the phase locking takes place at the oscillator and due to the PVT variation it is very difficult to maintain a certain delay all the way from the oscillator to the retimers. Therefore, a variable-delay buffer is inserted in the loop to compensate for these variations.

Variable-delay buffers normally sum a periodic signal with its phase-shifted version with varying weights. To ensure that the signals are adding up constructively, the phase difference between them must be below 90°. Therefore, the maximum value of the delay that can be achieved using a single-stage variable delay is limited to 90°. At lower speeds, the phase shift can be achieved using an RC delay. At higher frequencies, the attenuation due to the RC delay would require a greater amount of power to be compensated. The topology in Figure 51 uses a buffer to generate the 90° phase shift.

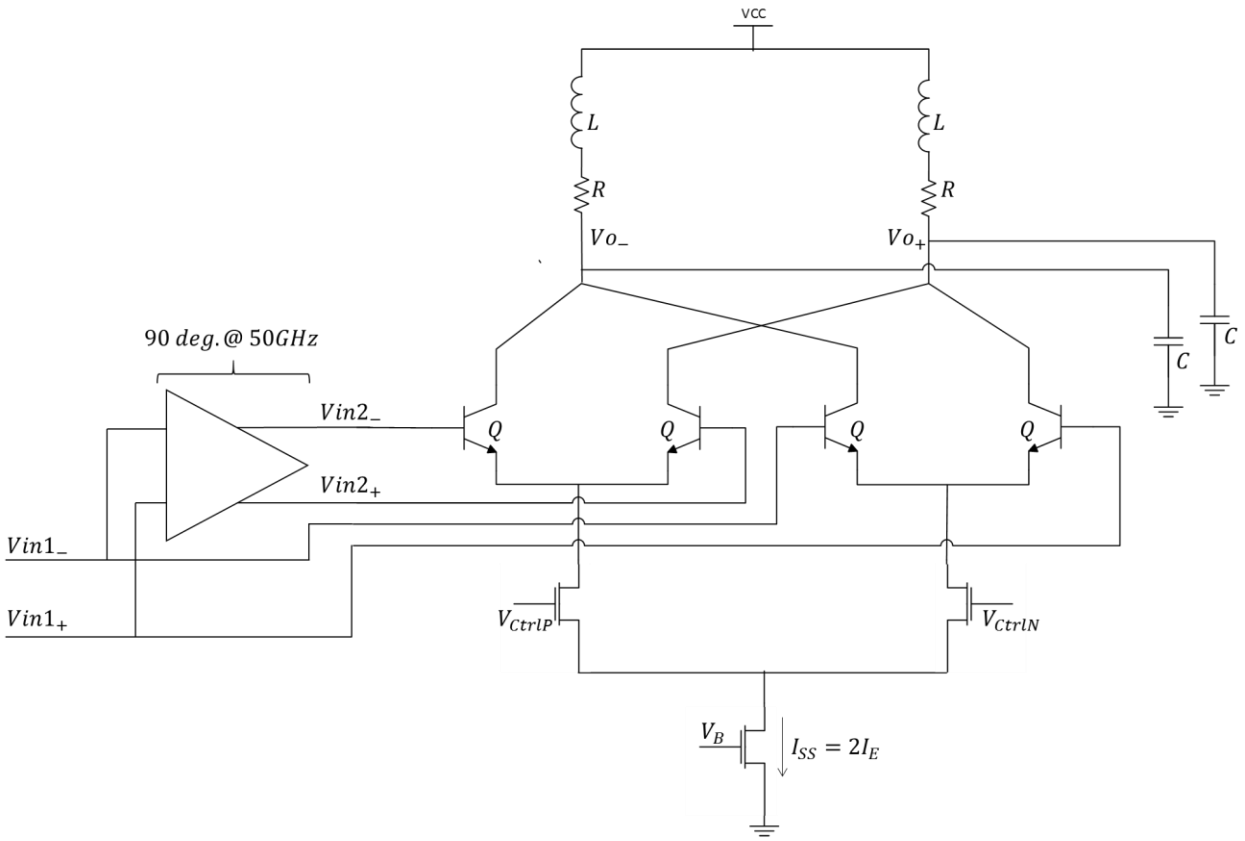


Figure 51. Variable-delay buffer

The buffer phase shift is designed to be close to 90° after taking into account all of capacitances at its output. The output phase can be varied by changing the control voltage $V_{CtrlP}-V_{CtrlN}$ from -0.5V to +0.5V, as shown in Figure 52. The 90° phase shift is adequate for this application as we are incorporating a half-rate architecture.

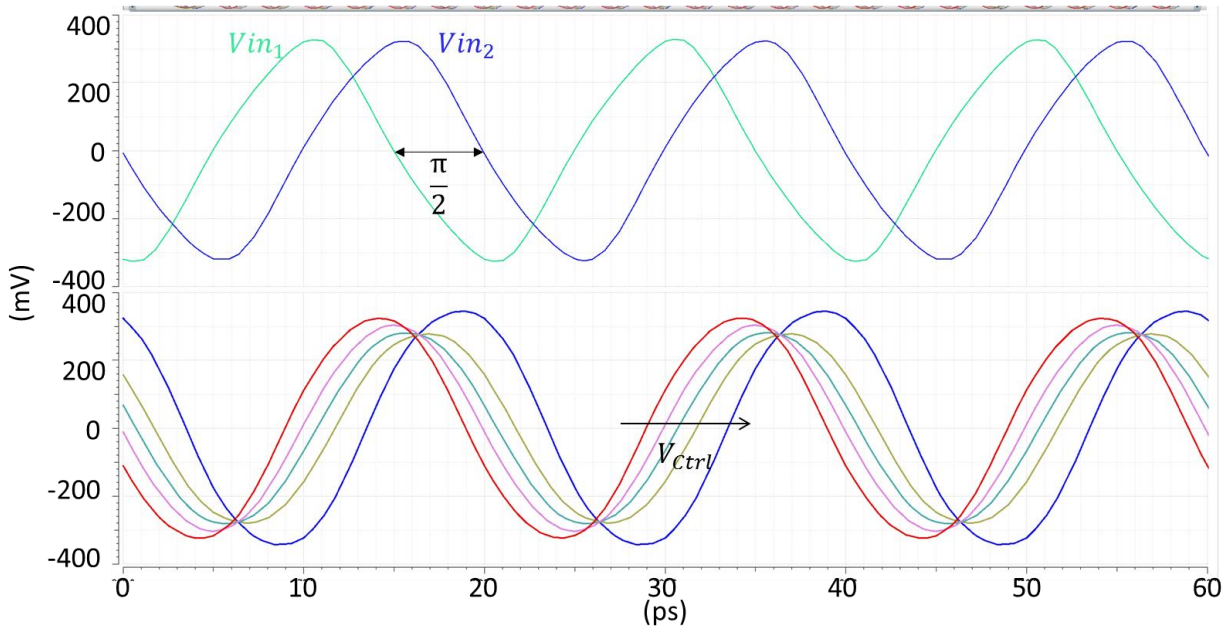


Figure 52. Variable-delay buffer transient output for different values of control voltages

4.5 Dynamic D Flip-Flops

The retimer D flip-flops must operate at 50Gbps to deserialize/retime the 100Gbps input data by the 50GHz recovered clock. Such a high-speed requirement is very difficult to meet with conventional cross-coupled based DFFs. The cross-coupled pair in such a DFF contributes to the loading of the stages, which can reduce the bandwidth. Therefore, a dynamic DFF architecture, first introduced in [25], is employed here. These types of DFFs are preferred at higher data rates where the signal transition and the clock-to-q delays are comparable. In the dynamic DFF, the second stage samples the data before the data value vanishes at the output of the first stage $V_{XP/N}$. To lengthen the signal stay at the output of the first stage and allow enough time for the second stage to sample, the shunt-peaking inductors

with high values of inductance can be employed. This will add to the inertia of the current at the output, and thus the signal at $V_{XP/N}$ will hold its value long enough after the clock transition.

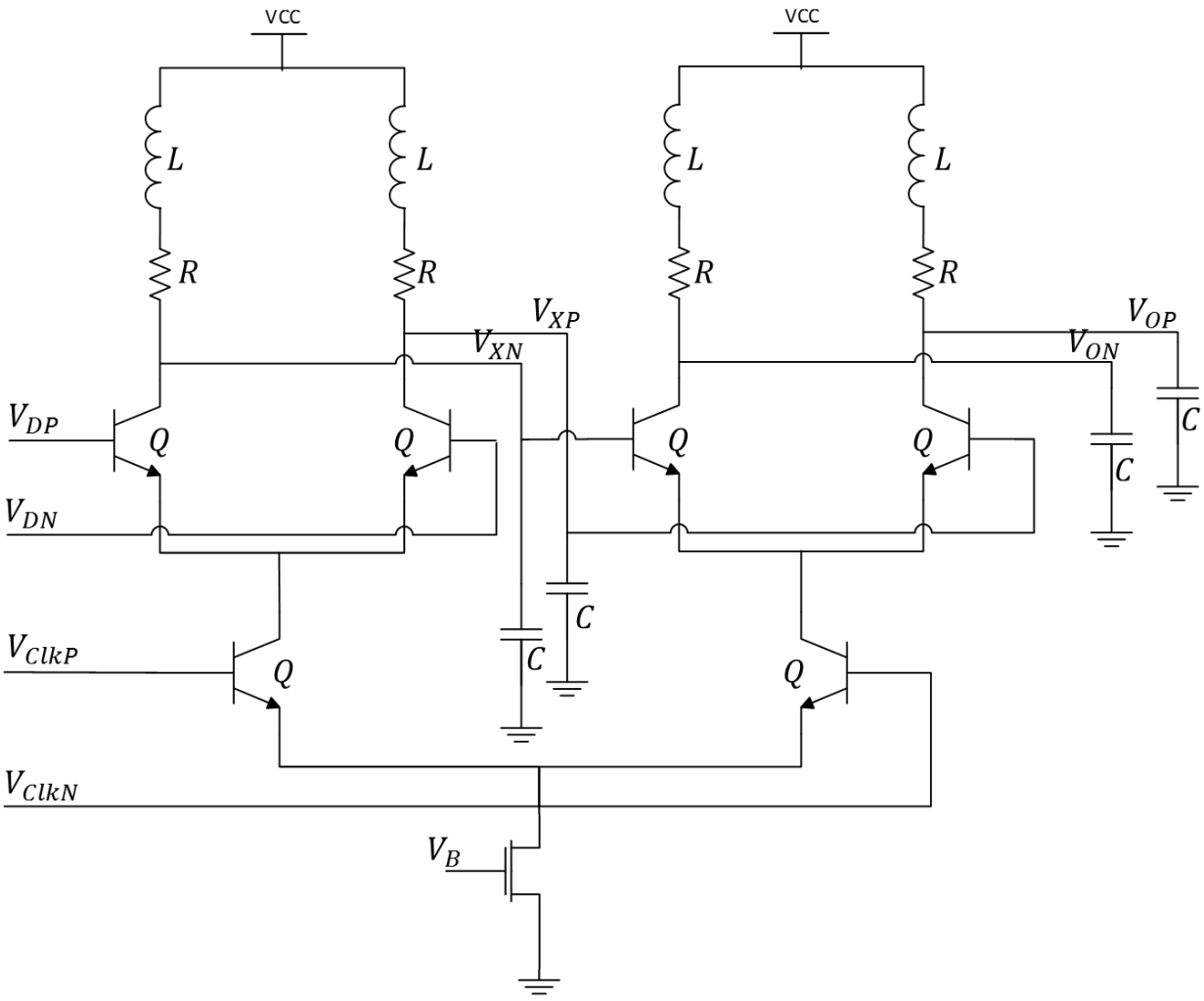


Figure 53. Dynamic D flip-flop schematic

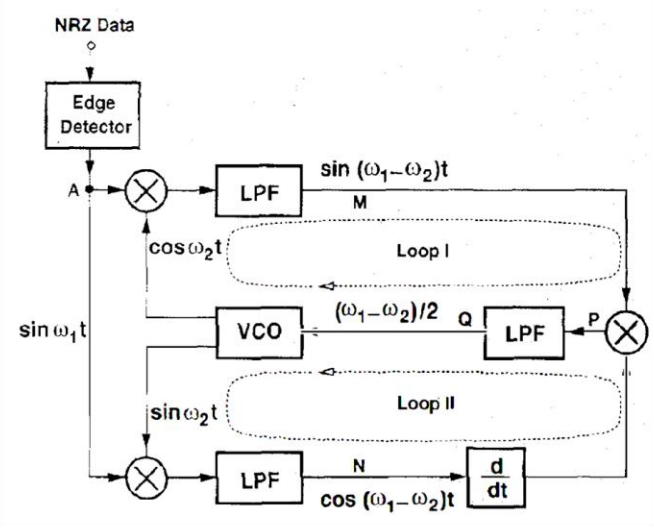
Ideally, proper values of *R*, *L* and *C* that lead to a ringing frequency that is near the baud rate of the data achieves the optimum behavior. In practice, the signal transition at the

emitters of the stages and the limited f_T come into view, and thereby accurate simulation of the parasitic extracted layout is required for optimization.

4.6 Referenceless Frequency Acquisition Loop

The 100-GHz tone generated by the injection circuitry can also be used for frequency acquisition. This tone can be mixed with the VCO output and its delayed version similar to the idea of the well-known quadricorrelator architecture, introduced by Richman [26] and shown in Figure 54 (a). The resulting mixer outputs will then exhibit the appropriate lead/lag properties depending on the sign of the frequency offset. In a conventional quadricorrelator, such as that used in [27], the lead/lag outputs of the mixers must exhibit a precise 90° phase shift, necessitating the use of quadrature VCOs at their inputs. Then the output of one of the mixers must be applied to a derivative block, which is very sensitive to noise, so that the frequency offset polarity can be extracted from the signal.

(a)



(b)

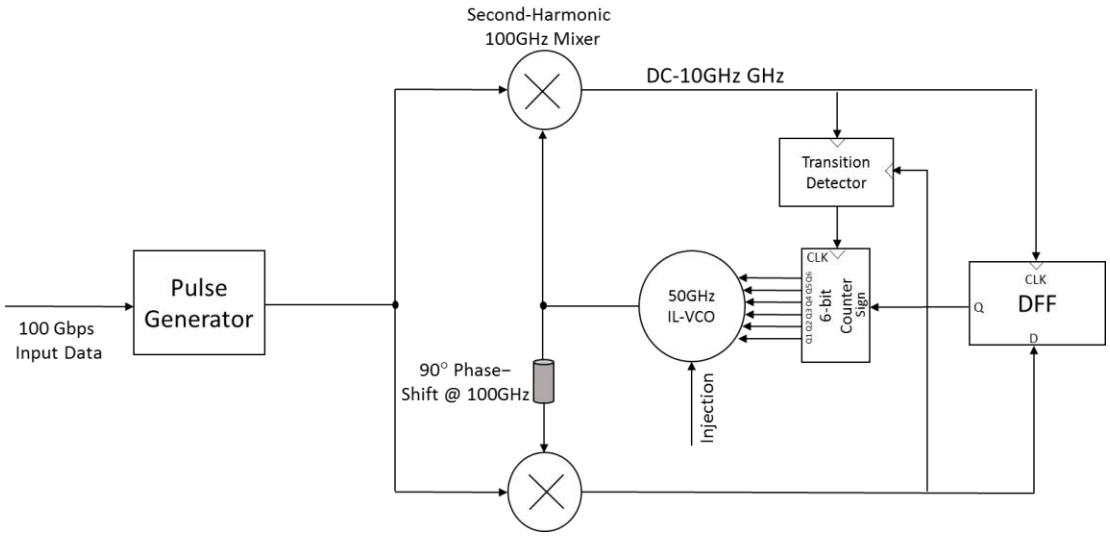


Figure 54. Frequency acquisition loop (a)Conventional quadricorrelator in (b)proposed quadricorrelator

In the proposed design, shown in Figure 54 (b), a simple DFF extracts the lead/lag information if the outputs of the mixers are applied to the clock and the data inputs. The output of the DFF can then drive the up/down signal of a counter, which controls the output frequency of a digitally-controlled oscillator (DCO). This also relaxes the need for a precise 90° phase shift, since the DFF can extract the information even if the clock is not sampled at

the optimum point. Therefore, a simple differential VCO with a nearly 90° phase shift would satisfy this requirement. Use of high-frequency mixers as the interface relaxes the requirements on the rest of the blocks as they will work at much lower frequencies; e.g. for a 100 Gb/s data and a 10% frequency acquisition range the output of the mixer will range from dc to 10 GHz. A transition detector is employed to improve the robustness. The frequency resolution of the DCO is chosen to be less than the locking range of the injection locking. The frequency acquisition loop will bring the VCO output frequency near the injection frequency, after which the injection locking takes over. Once phase locking takes place, the mixers will generate a DC signal. Simulation results demonstrating individual waveforms and output frequency are shown in Figure 54 (a) and (b), respectively.

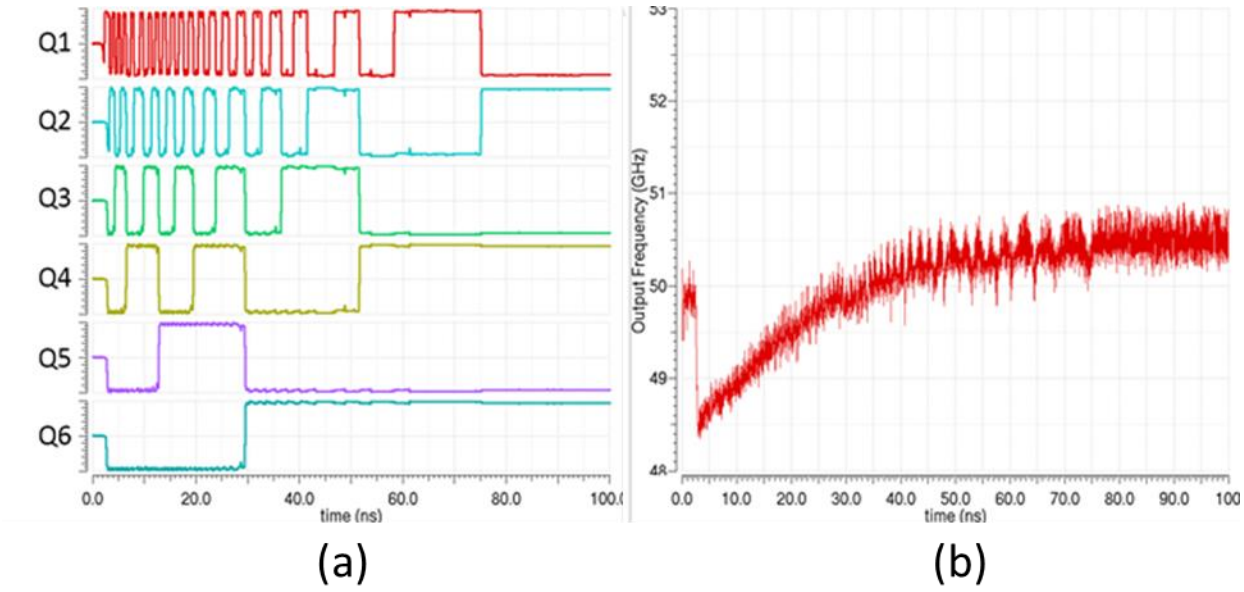


Figure 55. Frequency Acquisition Loop transient locking response (a)6-bit counter outputs (b)The VCO output frequency

The main components of the frequency acquisition loop, the second-harmonic 100GHz mixer, and the transition detector are discussed in the following subsections.

4.6.1 Second-Harmonic 100GHz Mixer

The circuit in Figure 56 is a second-harmonic 100 GHz mixer. The idea here is to extract a tone from the data, as was done for injection locking, and mix it with the VCO output to find the frequency offset. As shown in Figure 54, the mixer inputs are the VCO and the pulse generator circuitry outputs. One rectifier will generate a tone at 100GHz similar to the operation of the injection circuitry. The tone will then be down-converted by the second harmonic of the VCO output, generated by another rectifier. The rectifier outputs are both connected to the resonators that are tuned at 100 GHz. This will ensure high pulse amplitudes at the inputs of the Gilbert-cell mixer in Figure 56. The mixer output is connected to high-gain buffers to provide the digital circuitries with signal with sufficient amplitude.

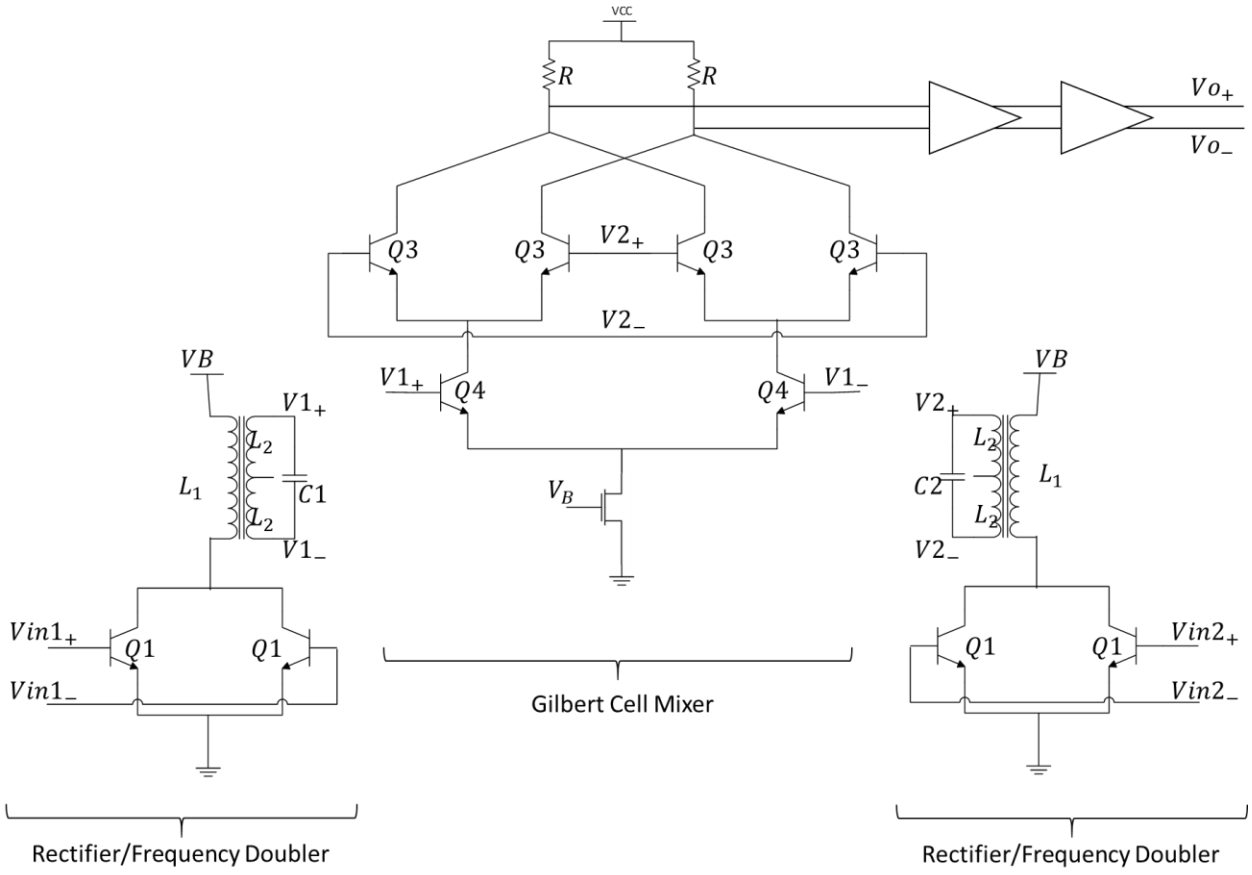


Figure 56. Second-harmonic 100 GHz mixer schematic

Figure 57 shows the transient behavior of the mixer where V_{inj} is the output of the pulse generator for a 100-Gbps PRBS7 input data signal, and V_{osc} is the mixer input from the VCO at 51 GHz. The down-converted signal will then be at $2 * (51\ GHz) - 100\ GHz = 2\ GHz$ as shown in Figure 57(c).

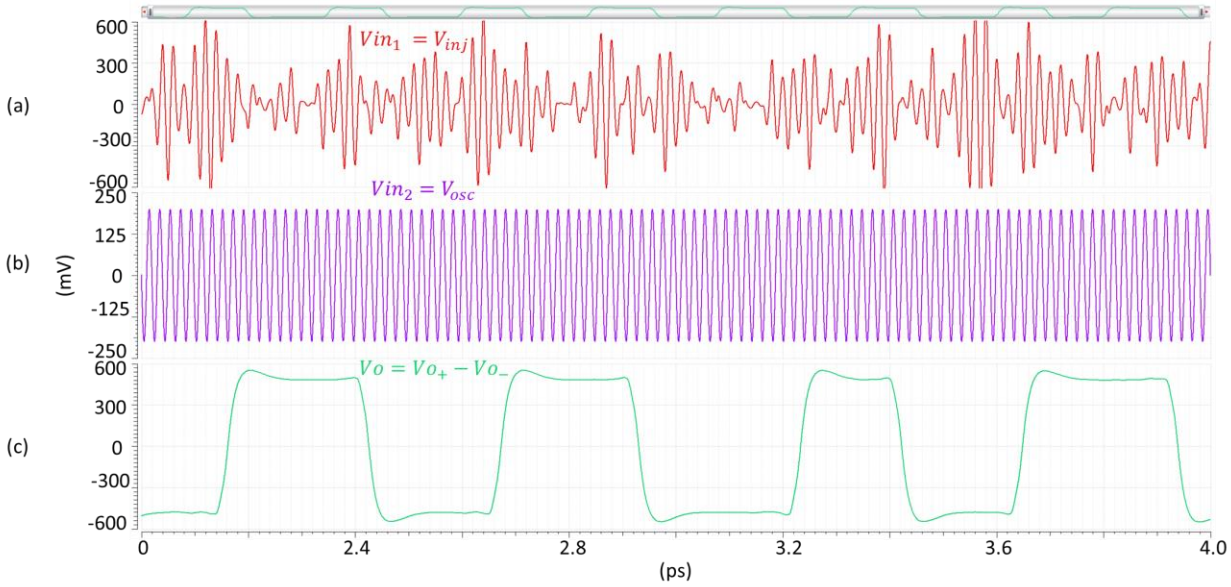


Figure 57. Second-Harmonic 100 GHz mixer transient inputs and output (a) Pulse generator output (b) VCO output (c) Mixer output

To improve the robustness, a transition detector generates the input clock of the counter as explained in the following section.

4.6.2 Transition Detector

When the phase locking takes place through injection locking, the VCO and the data generate tones at the same frequency as the mixer. The mixer output in this case is ideally a dc signal that will no longer generate a clock signal for the counter. The noise from the random input data can cause unwanted transitions after amplification in the high-gain buffers. To prevent the mixer output spikes from perturbing the frequency acquisition loop operation, a transition detector is implemented.

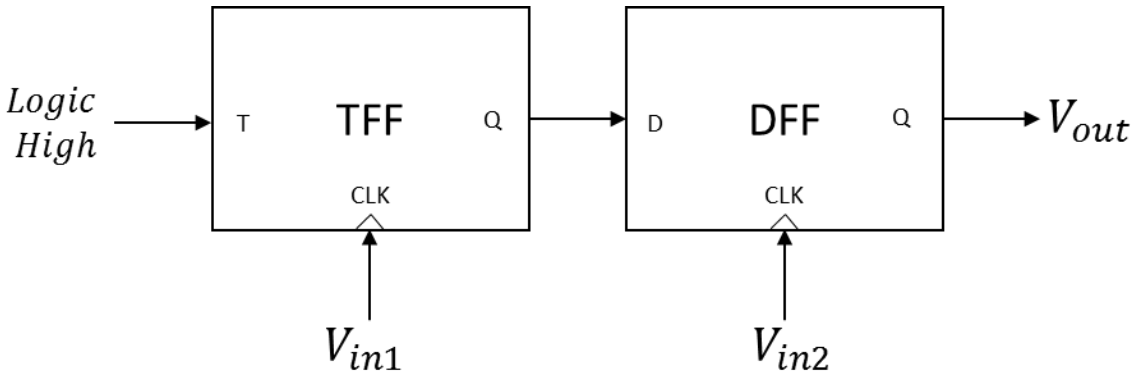


Figure 58. Signal Transition Detector

The transition detector simply consists of a T flip-flop, also knows at toggle flip-flop, whose input is tied to a logic high and a D flip-flop. The output of the circuit shown in Figure 58 toggles only when there is a transition in both of its clock inputs following one another. The inputs $V_{in1}$and V_{in2} are connected to the frequency acquisition mixers. The decision making based on two inputs improves the system robustness against faulty conditions.

4.7 Time-Domain Test

The time-domain test block diagram is shown in Figure 59. To test the efficacy of the 100 Gbps clock data recovery circuit, an on-chip 100-Gbps PRBS generator is designed. The CDR will recover a half-rate 50 GHz clock from a 100-Gbps PRBS7 data and deserialize the data to two 50-Gbps PRBS7 signals. There is a selector block that allows selection between 0101 data and the PRBS7 as the input data. The main blocks, including the 100 Gbps PRBS7 generator and the clock multiplier, are discussed in the following subsections.

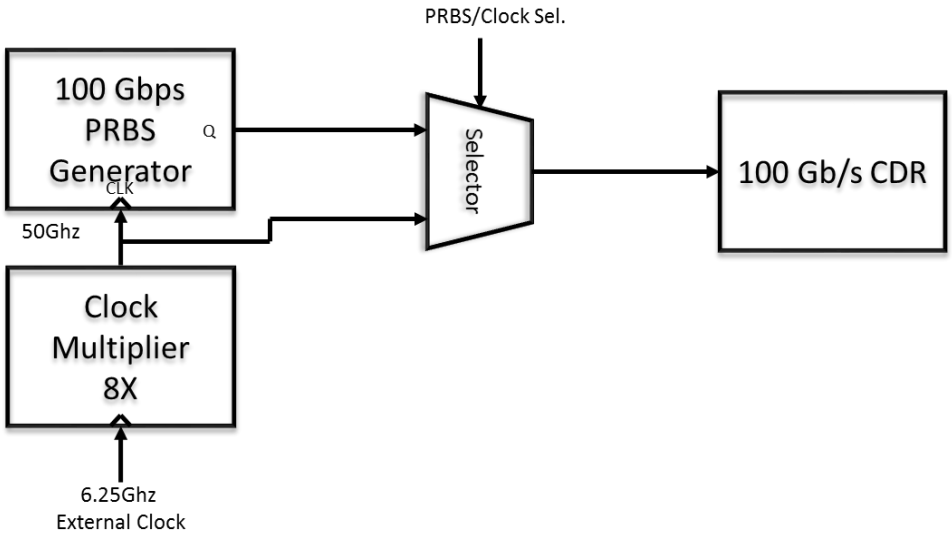


Figure 59. Time-domain test block diagram

4.7.1 PRBS Generator

Pseudo-Random-Bit-Sequence (PRBS) generators are widely used to measure some of the system time-domain specifications such as jitter and the bit-error-rate. PRBS generators normally consist of a number of DFFs, depending on their word length, and an XOR gate. In full-rate PRBS generators, all the blocks are clocked at full-rate. For instance, for a 100-Gbps PRBS generator the DFFs and the clock distribution circuitry must operate at 100 GHz. Thus, a full-rate 100-Gbps PRBS generator can be very challenging and costly to design.

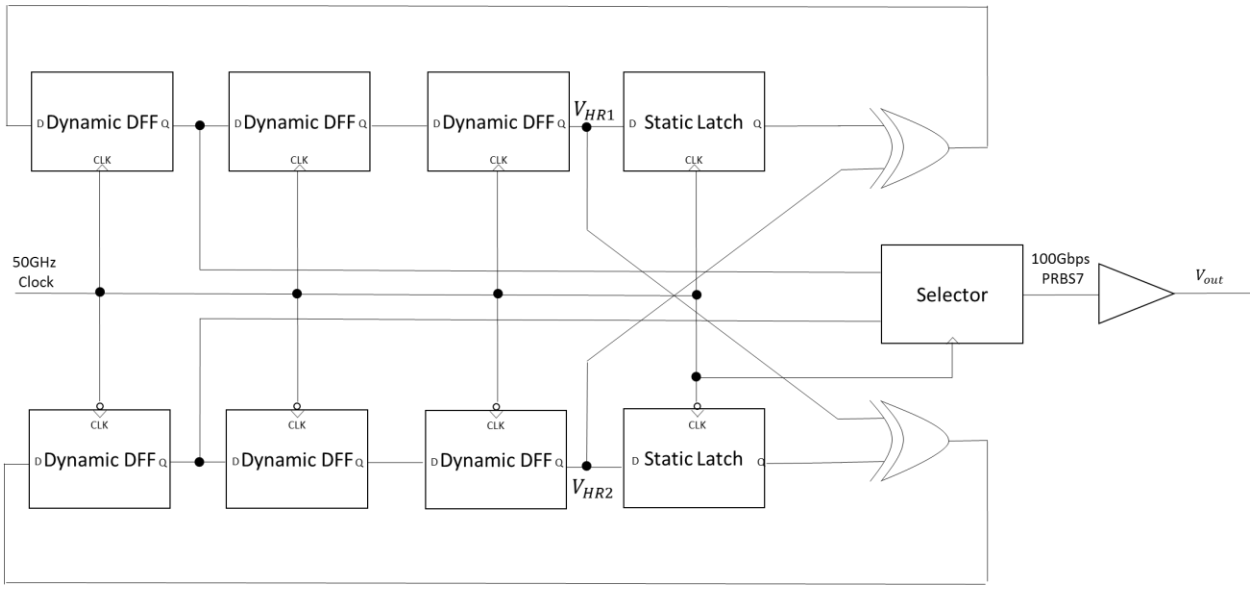


Figure 60. 100 Gbps PRBS7 generator with half-rate architecture and Dynamic DFFs

The architecture shown in Figure 60 operates with a 50-GHz half-rate clock to generate a 100-Gbps PRBS7signal; i.e., the DFFs, latches, and the XORs are operating at 50 Gbps, similar to [28]. The half-rate clock architecture simplifies the clock distribution circuitry as well. To achieve higher speeds, and to minimize the layout area and power consumption, dynamic DFFs similar to the ones in described in Section 4.5 are employed here. Figure 61 shows the eye-diagram outputs of two of the dynamic DFFs, $V_{HR1}$and V_{HR2}, operating at 50Gbps, one at the falling and one at the rising edge of the clock.

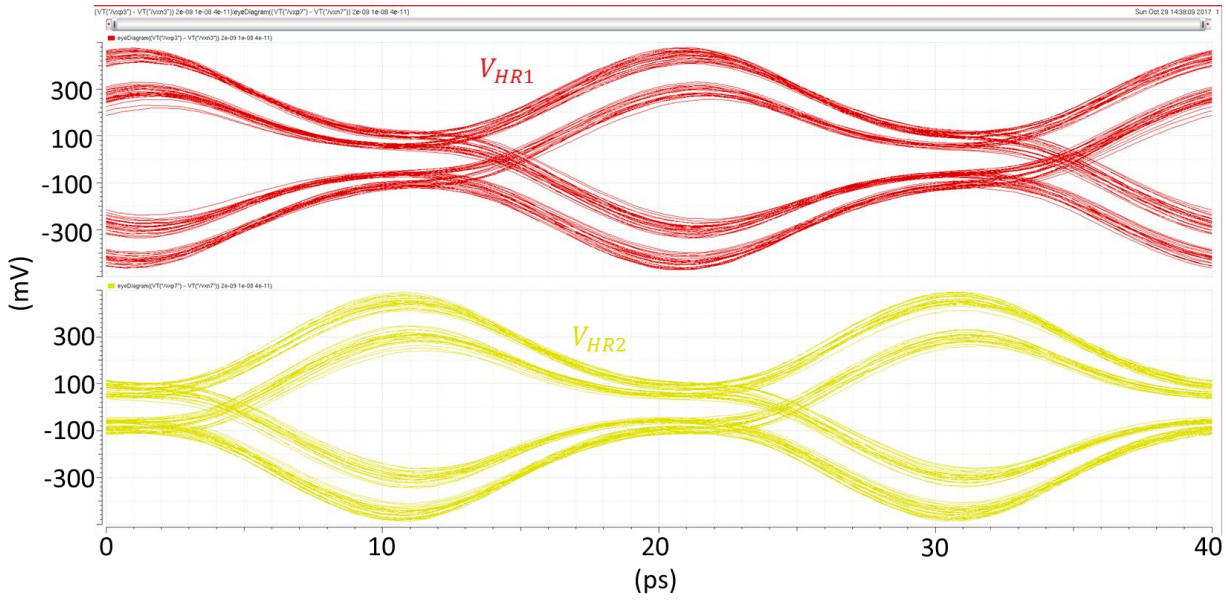


Figure 61. The outputs of the dynamic DFFs in 100 Gbps PRBS generator operating at 50Gbps

The selector multiplexes the half-rate signals at the falling and rising transitions of the clock, creating a 100 Gbps PRBS7 signal. The circuit can generate a PRBS7 signal at the output with word length of $2^7 - 1$, shown in Figure 62, which is a common word length for this type of test.

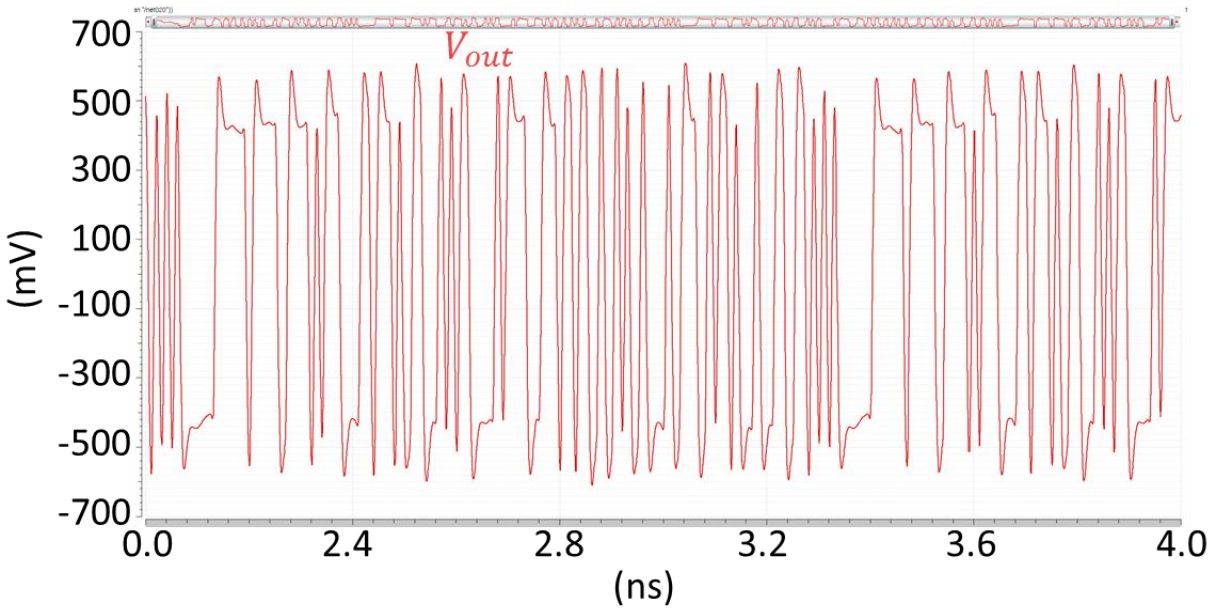


Figure 62. 100 Gbps PRBS7 generator transient output at the buffer output

With the Dynamic DFFs and proper values of shunt peaking at the selector and the buffer, the jitter at the output can be minimized. The data and clock delay between the blocks must be minimized to ensure meeting timing requirements. The layout parasitic extraction was analyzed and optimized a number of times to achieve the required timing specifications. Figure 63 shows the eye-diagram of the 100 Gbps PRBS7 signal.

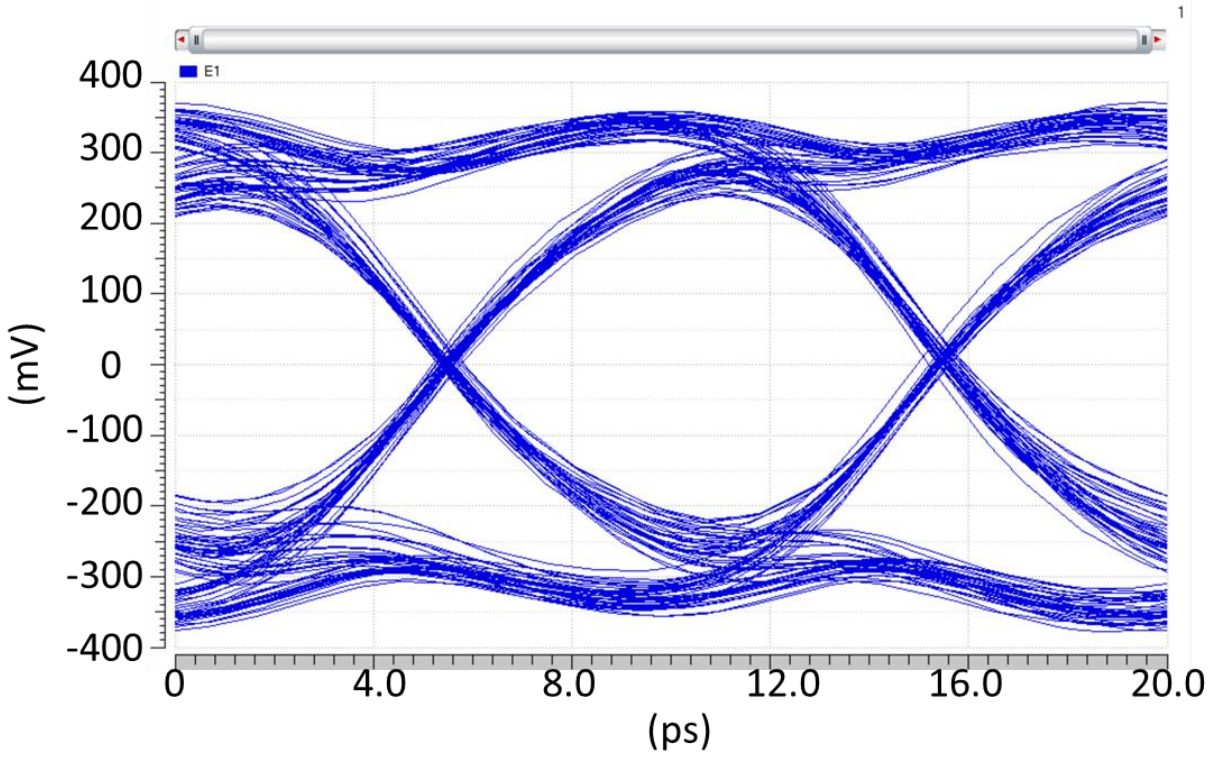


Figure 63. 100 Gbps PRBS7 generator output eye-diagram

The total jitter at the output of the PRBS generator is less than 0.5ps and the total power consumption of this block is 215mW from a 3-V supply.

4.7.2 8X Clock Multiplier

The 8X clock multiplier circuit consists of three 2X clock multiplier stages with similar topologies and brings the external input clock frequency from 6.25 GHz to 50 GHz. A 2X clock multiplier stage is shown in Figure 64. By properly biasing the rectifier transitors close to the V_{BEON} of the bipolar transistors, the second harmonic of the signal can be extracted, and a proportional current I_{Rect} is generated. The rectifier is followed by a transformer tuned at

the second harmonic of the input signal. This will ensure extraction of the second harmonic and rejection of the unwanted harmonics. The transformer also provides a conversion from single-ended to differential, making it compatible with the input of a CML buffer. It should be noted that the use of the transformer simplifies the biasing of the next stage, as the DC bias of the next stage VB2, can be simply applied to the center tap of the transformer.

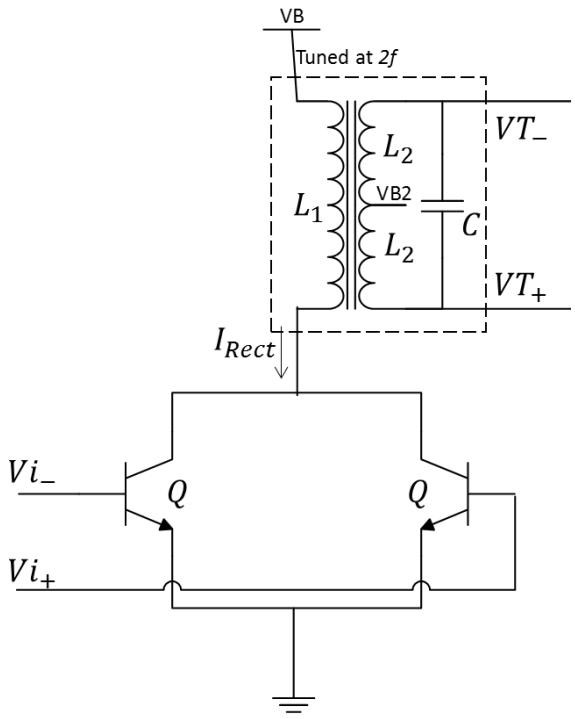


Figure 64. 2X clock multiplier stage

The input and output waveforms of the first stage 2X clock multiplier are plotted in Figure 65. The transformer resonates at 12.5 GHz in the first stage and can generate a clean second harmonic tone at the output.

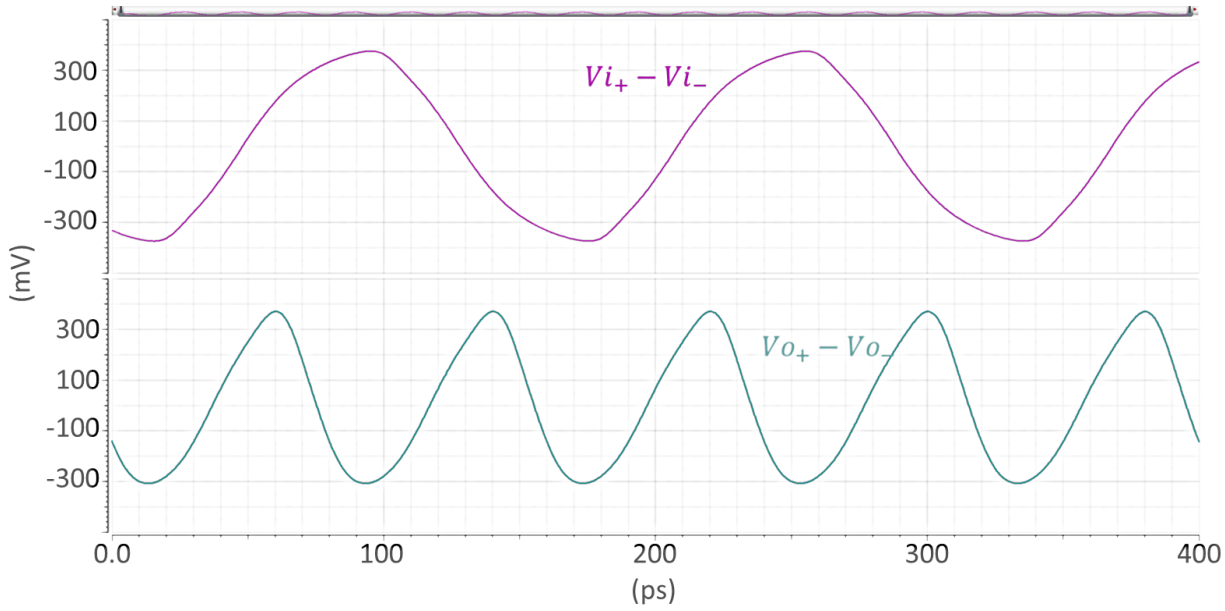


Figure 65. 2X clock multiplier transient output

Figure 66 shows the block-diagram of the 8X clock multiplier. The three 2X clock multipliers are similar in topology with differences only in the resonance frequency. The resonance frequency of the first, second, and third stages are 12.5 GHz, 25 GHz, and 50 GHz, respectively.

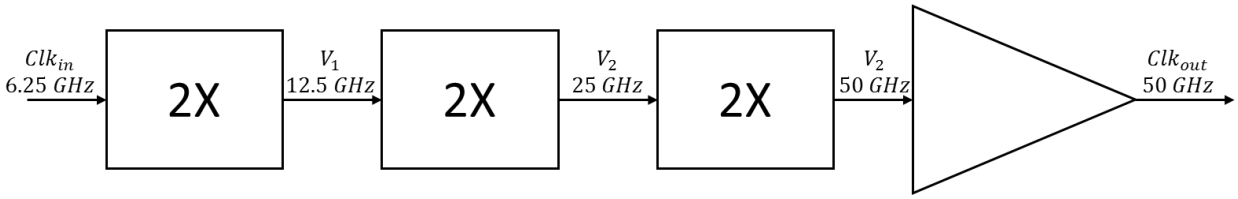


Figure 66. 8X clock multiplier block diagram

The third stage will then generate the proper 50-GHz clock for the half-rate 100 Gbps PRBS generator. In order to generate a clock signal with a sufficiently high amplitude, the generated 50-GHz tone is enhanced using a tuned buffer. The eye diagram of the output clock is plotted in Figure 67.

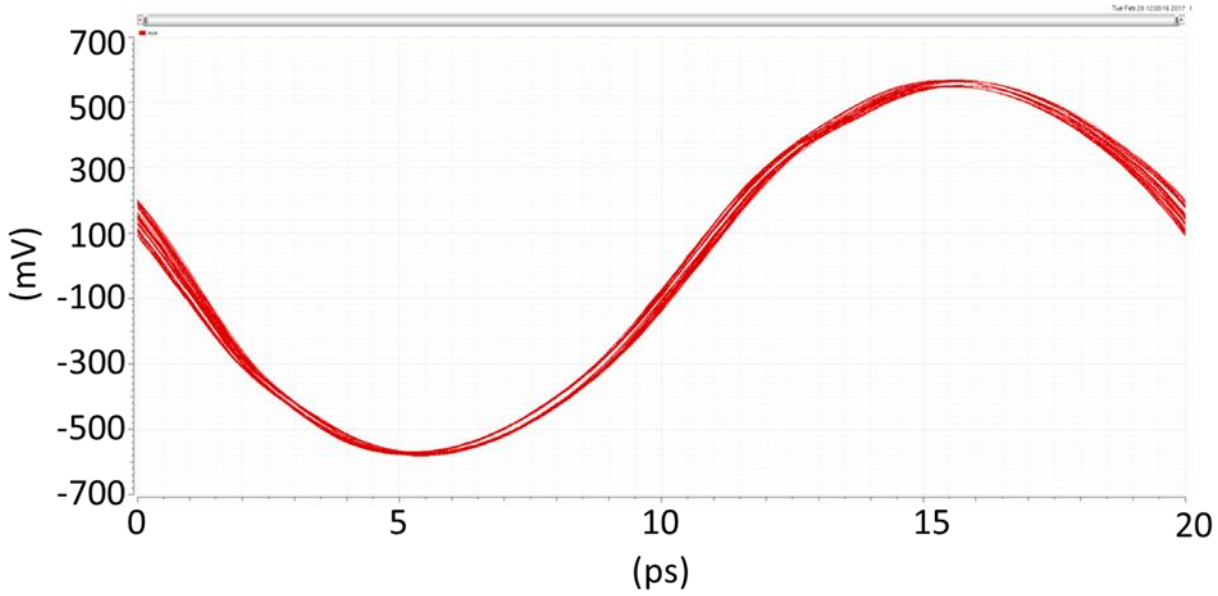


Figure 67. 8X clock multiplier output eye-diagram

The clock multiplier consumes 104.5mW of power and it exhibits .3ps of peak-to-peak jitter at its output.

4.8 Chip Top Level

The complete block diagram of the top level is shown in Figure 68. A 6.25 GHz external clock is applied to the input of the 8X clock multiplier. The output of the clock multiplier

generates a 50-GHz half-rate clock for the 100-Gbps PRBS7 generator. The incoming 100 Gbps data from this generator is fed into the injection-locking CDR. The CDR core of Figure 68 deserializes the received data. The CDR output is then transmitted out of the chip though the output drivers. There are several control signals to allow bias current adjustment for the VCO, injection circuitry, and other blocks.

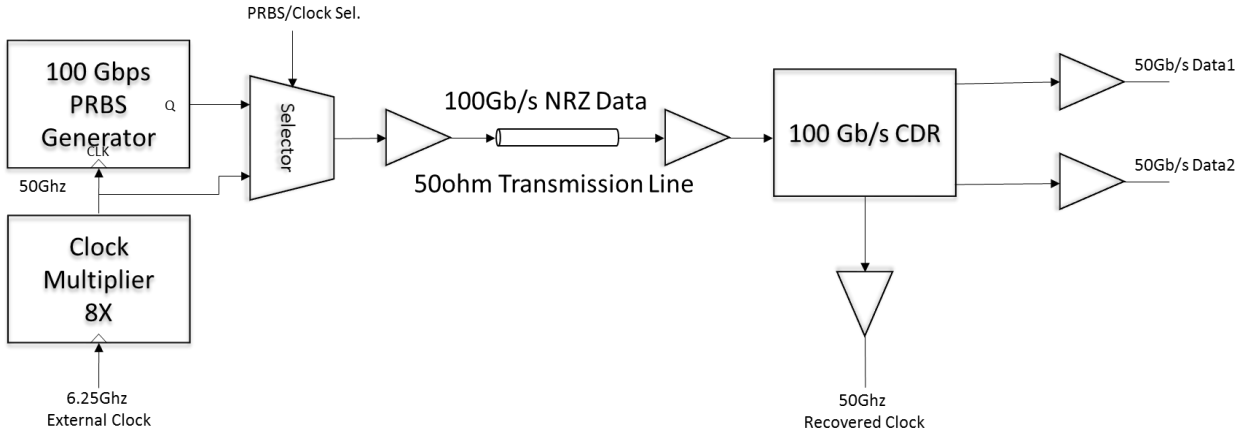


Figure 68. Chip top level block diagram

Table 1. 100Gbps injection-locking CDR simulated performance summary table

Supply voltage	2V - 3V
Power consumption-CDR without output buffers	290mW
Power consumption-total	640mW
p-p ISI	0.7ps
Frequency acquisition range	95Gbps-103Gbps

The chip was manufactured in a 0.18 BiCMOS process. The chip layout is shown in Figure 69, where the major building blocks are identified. The chip was fabricated on a Multi-Project Wafer (MPW) at TowerJazz Semiconductor with a dimension of 2.5 mm by 2.5 mm, whereas the active area is only 1.5 mm^2. The remaining area was used for DC decoupling capacitors as well as added metal layers to meet the 60% minimum metal density required by the process. The input and recovered clocks are placed on opposing sides of the die to minimize coupling. The core is placed at the corner of the chip close to the pads to improve the reflection coefficient at the output drivers. The symmetrical layout at the output of the drivers in Figure 69 minimizes the mismatch at the outputs.

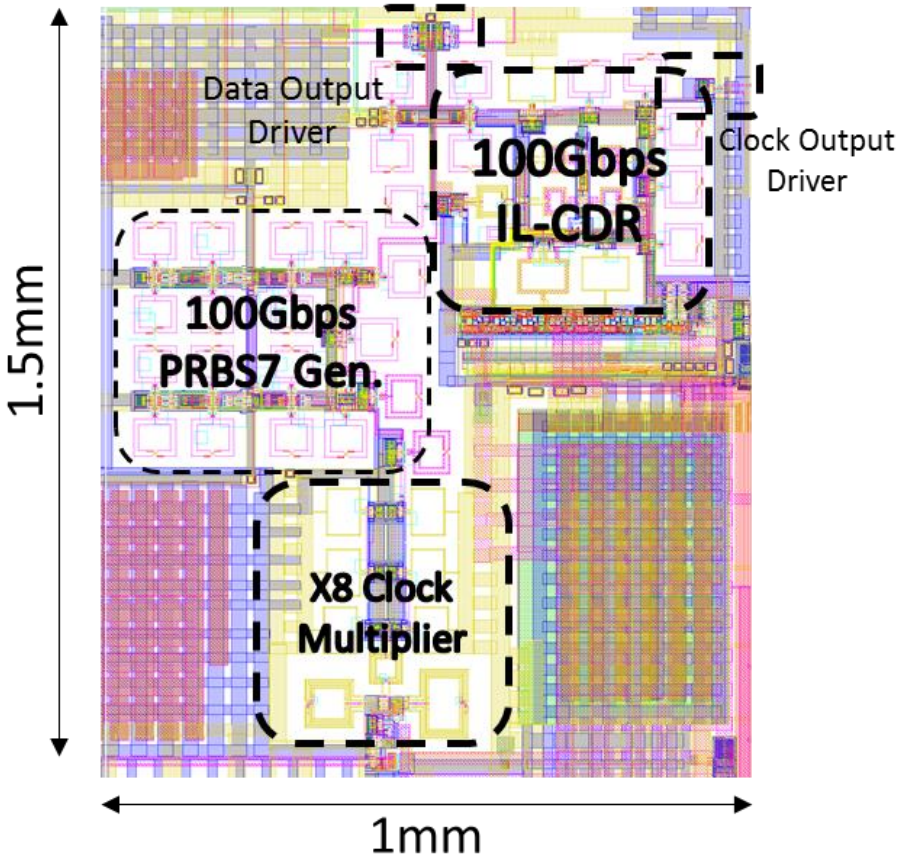


Figure 69. Core layout

5. Conclusions

In this dissertation, the design and fabrication of the first 100 Gbps referenceless half-rate injection-locking CDR have been presented. The chip was manufactured using TowerJazz 180nm BiCMOS process and includes an 8X 50-GHz clock multiplier and a 100-Gbps PRBS7 generator along with input termination and a 50Ω output driver in addition to the CDR circuit. The CDR, exhibits power dissipation of 290mW, which is among the best of previously reported CDRs at comparable speeds. The use of injection locking for phase locking with a novel pulse generation technique has enabled operation at 100Gbps.

The chip's performance was achieved through various architectural and circuit design techniques. A variation of the conventional quadricorrelator was used for frequency acquisition to extend the frequency capture range. The proposed frequency acquisition technique does not require a quadrature VCO, which enables a higher operating frequency in this process. The pulse generation technique is also used for the frequency acquisition. The proposed pulse-generation technique achieves superior power consumption compared to the conventional PD-based and ADC-based CDRs. In addition, various layout techniques were used in order to minimize interconnect parasitic capacitance and resistance.

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