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Process Development of Copper- Copper Thermocompression Bonding

for Power Delivery and Heat Extraction system

for the Silicon-Interconnect Fabric

A thesis submitted in partial satisfaction of the requirements for the degree

Master of Science in Electrical and Computer Engineering

by

Pranav Ambhore

2020

ABSTRACT OF THE THESIS

Process Development of Copper- Copper Thermocompression Bonding for Power Delivery and Heat Extraction system for the Silicon-Interconnect Fabric

by

Pranav Ambhore

Electrical and Computer Engineering

University of California, Los Angeles

Professor Subramaniam Srikantes Iyer, Chair

The Silicon-Interconnect Fabric (Si-IF) is a platform for heterogeneous integration that seeks to advance packaging scaling by integrating dies with short interconnection pitches (≤ 10 µm) with an inter-die spacing of ≤ 100 µm. For a large, high-performance system, the power requirement is estimated to be >50 kW. This short spacing of chips on the Silicon Interconnect Fabric will pose significant power delivery and cooling challenges. To address these issues, a polymer-metallic composite structure called PowerTherm is bonded to the Silicon Interconnect Fabric using Cu-Cu thermocompression bonding. The process conditions for bonding i.e. time, temperature, and pressure must be optimized to prevent any damage to the assembled Si-IF and the PowerTherm structure while ensuring high bond strength and low electrical resistance. Cu-Cu thermocompression bonding was performed in the atmosphere and vacuum at 150-350 °C at low pressure (≤ 3 MPa) for 2 hours. The bonding was performed between an electroplated Cu- sample and Cu rod/block configuration, and between two electroplated Cu-samples. Shear strength of 25 ± 1 MPa and specific electrical resistance of 2944 $\Omega.\mu m^2$ was achieved. The current bonding

system lacks a high bonding force as well as the ability to bond non-wafer samples. To address these issues, a custom bonder was constructed and the details of its design and progress are also reported. The bonder can apply 10X more force as well as bond non-wafer samples.

The thesis of Pranav Ambhore is approved.

Chee Wei Wong

Tim Fisher

Subramanian Srikantes Iyer, Committee Chair

University of California Los Angeles

2020

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Last but not least, I would like to thank my parents as well as all my family members for their constant support and help.

CHAPTER 1

1. Introduction

1.1. Silicon Interconnect Fabric: Enabling Heterogeneous Integration and Advanced Packaging

Performance and functionality enhancement from integrated circuits has been historically achieved by scaling minimum feature device sizes and increasing chip sizes. However, both these approaches can no longer be relied upon due to cost and yield issues. As a consequence of decreasing feature sizes, the wire density (wires/area) within the chip and the interconnections exiting the chip have increased. An increase in the number of inter-connections without a corresponding increase in chip area has led to fine pitch interconnections. In the last six decades, minimum feature sizes in chips have decreased by three orders of magnitude. At the same time, the interconnect pitches used on conventional packages made from organo-glass composites have scaled less than an order of magnitude (1). One of the major reasons for the insufficient scaling of interconnect pitches in laminates is due to their material properties and subsequent processing. Vias or inter-layer wiring connections in the laminate board are fabricated by mechanical or laser drilling process. These processes face various challenges like frequent drill bit failures, substrate incompatibility for drilling, yield, and productivity (2). Lack of scaling can lead to bandwidth bottleneck and latency rise due to limitations in the number of interconnects that can be accommodated in the restricted chip area.

The Silicon-Interconnect Fabric (Si-IF) consists of a-Si wafer which seeks to replace the laminate board as the packaging substrate (3). It consists of lithographically defined wiring levels and enables inter-die spacing of up to 100 µm. The inter-pillar spacing in the Si-IF is ≤10 µm, thereby offering 10-100X more connections than the conventional laminate board. In a package with a laminate board, 30-50 percent of power is lost in SERDES (serialization-deserialization) signaling protocol where data is collected, serialized, and sent at high frequency and then deserialized to account for fewer interconnect wires and large bump pitch (4). In the Si-IF, due to a significantly higher number of connections and parallel nature of communication, the Si-IF offers advantages of low latency, high bandwidth, and lower power consumption, etc. which makes the Si-IF well suited for high-power, Systems on Wafer (SoW) type of applications (5).

1.2. PowerTherm: Power delivery and heat extraction architecture for Si-IF

Many challenges arise in the Si-IF such as communication and routing within and outside the Si-IF, power delivery, heat extraction, reliability, etc. Typical power density in the system on chip (SoC) is 1 W/mm^2 (6). The estimated power density on Si-IF is comparable to this number. For a 300 mm Si-IF, assuming that 70 percent of the wafer area is populated with dies, the power to be delivered is ~50 kW which is significant. Correspondingly, a similar amount of heat needs to be extracted. In conventional packaging, chips are bonded to an organic laminate board which has a thermal conductivity of < 1 W/mK. Another disadvantage is the lack of heat spreading within the laminate board. Therefore, the heat has to be extracted from the top side of the chip. In an air-cooling system, heat is extracted by placing large heat spreaders and sinks over the chip. These heat sinks are 2-5X area of the chip and therefore, such a solution cannot be used to efficiently extract heat in Si-IF as chips are placed at a fine spacing of 100 µm. Additionally, the heat transfer coefficient of the cooling method required by Si-IF at peak performance is estimated to be ~10^4 W/m^{2}K indicating that heat removal by air or liquid cooling solutions may be impractical as these methods have 10-100X lower heat transfer coefficients (7).

To address these challenges, a novel architecture called PowerTherm is proposed to simultaneously achieve both the objectives of power delivery and heat extraction by leveraging the excellent thermal conductivity of Si-IF. There are two major components in PowerTherm.

1. The first component is Power Board which is a conventional laminate board. The components for power conversion and regulation such as capacitors are typically bulky and consume valuable areas on-chip or Si-IF. Therefore, the components required for power management

will be accommodated on this laminate board, thereby improving the efficiency of area usage on Si-IF.

2. The second major component is the heat exchange chamber which has three sub-components. The chamber consists of Cu pin-fins held together by a polymeric structure. The Cu pin-fins act as wires to deliver power. An advantage of numerous Cu pin-fins is that it enables achieving multi-voltage domains. The final subcomponent is a boron-nitride ceramic sheet which is a good electrical insulator but a good thermal conductor. The BN sheet along with Si act as heat spreaders which is a significant advantage over conventional laminate board packaging.

The heat exchange chamber is attached to the Si-IF by thermocompression bonding between Cu pin-fins and pads located on Through Wafer Via (TWV) terminations. The TWVs carry the power from the Cu-pin-fins to the dies bonded to Si-IF. As the dies consume power and get hot during operation, the heat will flow through the Si-IF and heat the Cu pin-fins. These Cu pin-fins will be cooled by a two-phase cooling technique, also called flash cooling. In flash cooling, the liquid is injected into the evacuated chamber. Due to a sudden decrease in pressure, the liquid vaporizes or flashes, and in the process of changing phase from liquid to vapor, absorbs latent heat of vaporization from the chamber thereby cooling the pin-fins. Consequently, power delivery and heat extraction can be simultaneously achieved. The focus of this thesis is the thermocompression bonding of Cu pin-fins to the Si-IF. The schematics of Si-IF integrated with the PowerTherm structure are shown in Figure 1 and Figure 2.

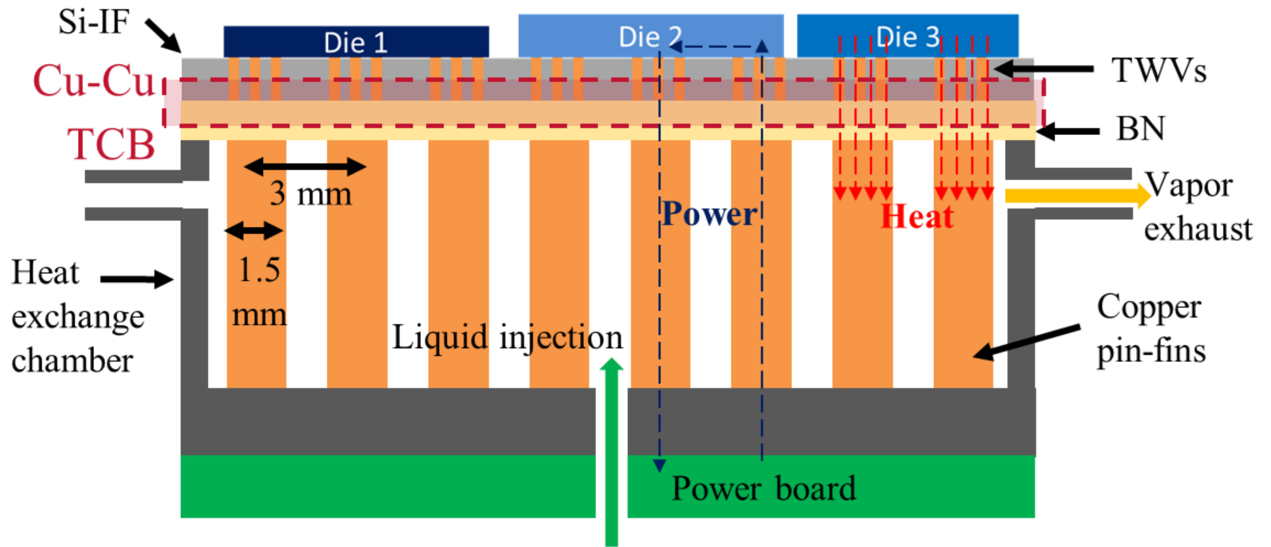

Figure 1: Schematic of Si-IF integrated with PowerTherm structure. Also shown are directions of flow of current (blue), heat (red), and cooling liquid-vapor (green (cold injected liquid) and orange(exhaust)).

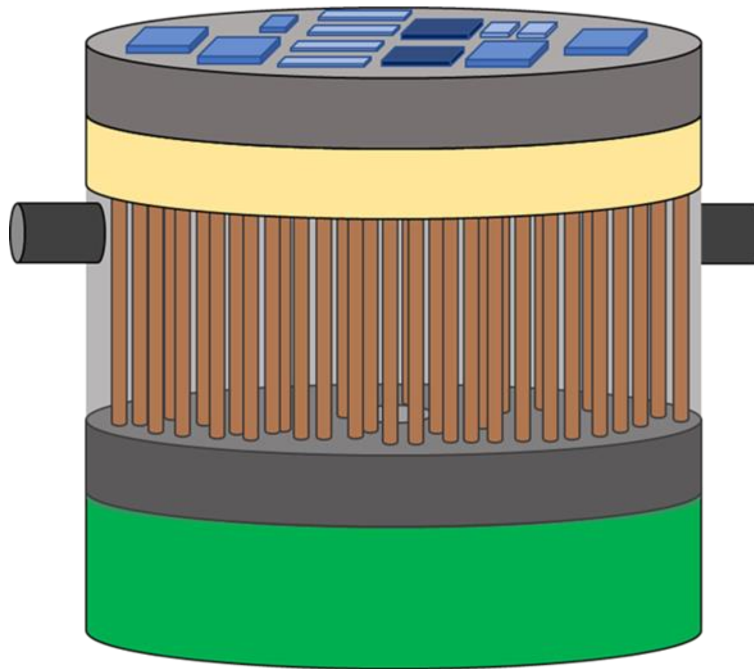

Figure 2: A three-dimensional schematic of the PowerTherm structure.

1.3. Cu-Cu Thermocompression Bonding

Eutectic bonding and its variations are the dominant bonding technology for attaching dies to laminates and printed circuit boards in packaging. However, these technologies possess' certain drawbacks. In eutectic bonding, an alloy composition deposited on the bonding surfaces is melted after the surfaces contact each other and a bond on solidification of this alloy. As the wiring pitch decreases, a significant concern is that the molten alloy might short with a neighboring wire due to molten metal extrusion (8) (9). Other drawbacks may include low reliability, bond strength and electrical resistance (10)

In thermocompression bonding, two surfaces are bonded by bringing the two surfaces atomically closer on the application of pressure to achieve metallic bonding. On a nanoscale, these surfaces consist of surface asperities which impart roughness to the surface. The true contact area of surfaces during bonding can be very different from the nominal area of contact and the true contact area depends on applied pressure, temperature, time, surface roughness, pristineness of surface, etc. (11). Thermocompression bonded structures have shown significantly higher bond strength and lower electrical resistance (10). Therefore, Cu- Cu thermocompression bonding was preferred for the integration of PowerTherm structure with the Si-IF.

1.4. Contribution of this Work

The primary objective of this work is to demonstrate and develop Cu-Cu thermocompression bonding for attachment of Si-IF to the PowerTherm structure. A suitable procedure for PowerTherm fabrication, including materials selection, process steps like chemical mechanical planarization of Cu pin-fins, CNC codes, etc. was developed. Materials, electrical and mechanical characterization of Cu-Cu thermocompression bonded samples were performed and controlling surface roughness and oxidation were found to be significant to improve the bonding process. A custom thermocompression bonder that can apply high force and accommodate non-wafer bonding structures was designed and constructed.

1.5. Organization of this Thesis

The thesis is organized as follows: Chapter 2 describes the process flow of PowerTherm construction as well as the details of custom tools and procedures used. The sample and experimental details, as well as results and results of Cu-Cu thermocompression bonding, are described in Chapter 3. Chapter 4 covers aspects of custom bonder for bonding, motivation, design, and construction progress. Chapter 5 includes the conclusion, summarizes the present work and future goals.

Chapter 2

2. PowerTherm Construction

The steps involved in choosing materials for the PowerTherm and its assembly are described in this chapter.

2.1. Materials Selection

The composite heat exchange chamber material must satisfy the following requirements:

1. Electrically insulating
2. It does not adversely react with methanol (cooling liquid).
3. It must be machinable.
4. It must be able to withstand high temperatures during fabrication, especially during the thermocompression bonding process (200-350 °C).
5. Resistant to plasma. Plasma is employed to achieve pristine surfaces for thermocompression bonding.

These requirements were satisfied by Polybenzimidazole (PBI) polymer and BN ceramic sheets. BN sheet has comparable thermal conductivity to Si wafer and satisfies other requirements. In the current form, a PBI sheet is used in place of the BN sheet due to machining difficulties. In the future, BN sheets with pre-drilled holes will be utilized.

2.2. Process Flow of PowerTherm Integration

The process flow of fabricating and bonding the PowerTherm heat exchange chamber to a Si wafer is described in this section:

1. The first step involved the drilling of holes (1.6 mm diameter, 3 mm pitch) in the PBI sheet using the Sherline CNC mill. Due to the elastic nature of PBI sheets, the holes were smaller than drill bit diameter. Multi-step drilling or “peck-drilling” was employed to ensure holes were sufficiently large to accommodate soft copper pin fins without pin fin deformation.
2. Cu pin fins were then mechanically inserted individually, and a tight fit was ensured.
3. Once all the pin-fins are inserted, they are planarized by lapping and polished by chemical mechanical planarization. Logitech PM-5 polisher with a custom-designed jig to hold the PowerTherm structure during polishing was used to achieve this step. An image of the jig along with the schematic cross-section showing PowerTherm structure mounted in the jig is shown in Figure 3. The PowerTherm structure is first bonded with a temporary adhesive (Crystalbond 509) to the stainless-steel block that applies pressure during lapping and polishing. This block has a diameter slightly smaller than the jig to minimize off-axis vibrations during lapping and polishing. Further details of the polishing step are provided in Chapter 3. The maximum length of Cu pin-fins extending out of the PBI sheet should be minimized to avoid Cu pin-fin deformation during polishing and to reduce polishing time.

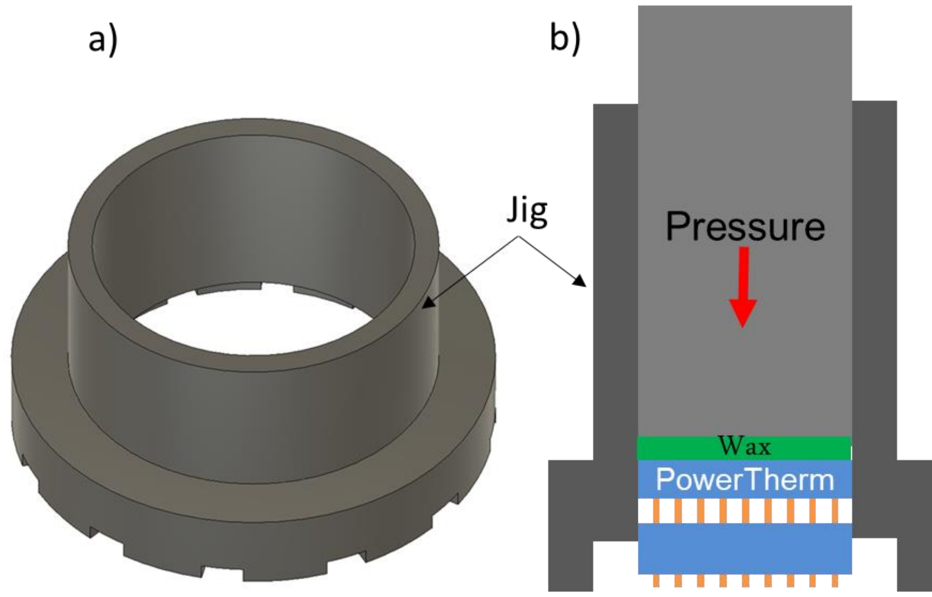

Figure 3: a.) Stainless steel jig used for planarizing and polishing Cu pin-fins. Inlets were provided at the bottom for slurry ingress. b) Schematic cross-section image showing pressure applied by a block on the pin fins during CMP.

4. The PowerTherm structure is then bonded to a Cu-terminated Si-IF wafer in the final step.

Figure 4 shows the process steps involved in the fabrication of PowerTherm.

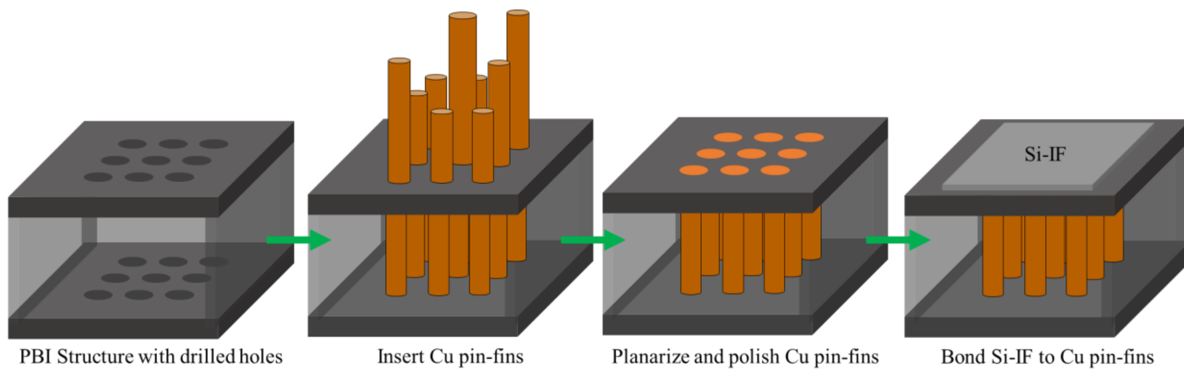

Figure 4: Steps involved in PowerTherm attachment process.

Chapter 3

3. Cu-Cu Thermocompression Bonding

3.1. Experimental Design

The objective of the bonding process was to achieve shear strength satisfying the MIL-883E standard. Higher temperatures are desirable in thermocompression bonding from a process perspective as this helps:

1. To breakdown and diffusion of contaminants away from the bonding interface
2. To reduce the mechanical properties of bonding surfaces such as yield strength and Young's modulus. Reduced mechanical properties enable greater deformation of surface asperities.
3. Increased diffusion of metal atoms along and across the bond interface

Wafers coated with electroplated copper were bonded in the air to determine the optimum bonding temperature. The optimum bonding temperature was decided based on shear force values. Once the optimum bonding temperature was found, bonding between Cu block to Cu coated wafer in atmosphere and Cu terminal block is demonstrated and shear strength is measured. Blocks were used for experiments conducted in atmospheric environment due to a different PowerTherm architecture (12). Wafer – Cu pin fins bonding in vacuum was performed next and the shear and electrical Schematic showing the bonding test structures is shown in Figure 5.

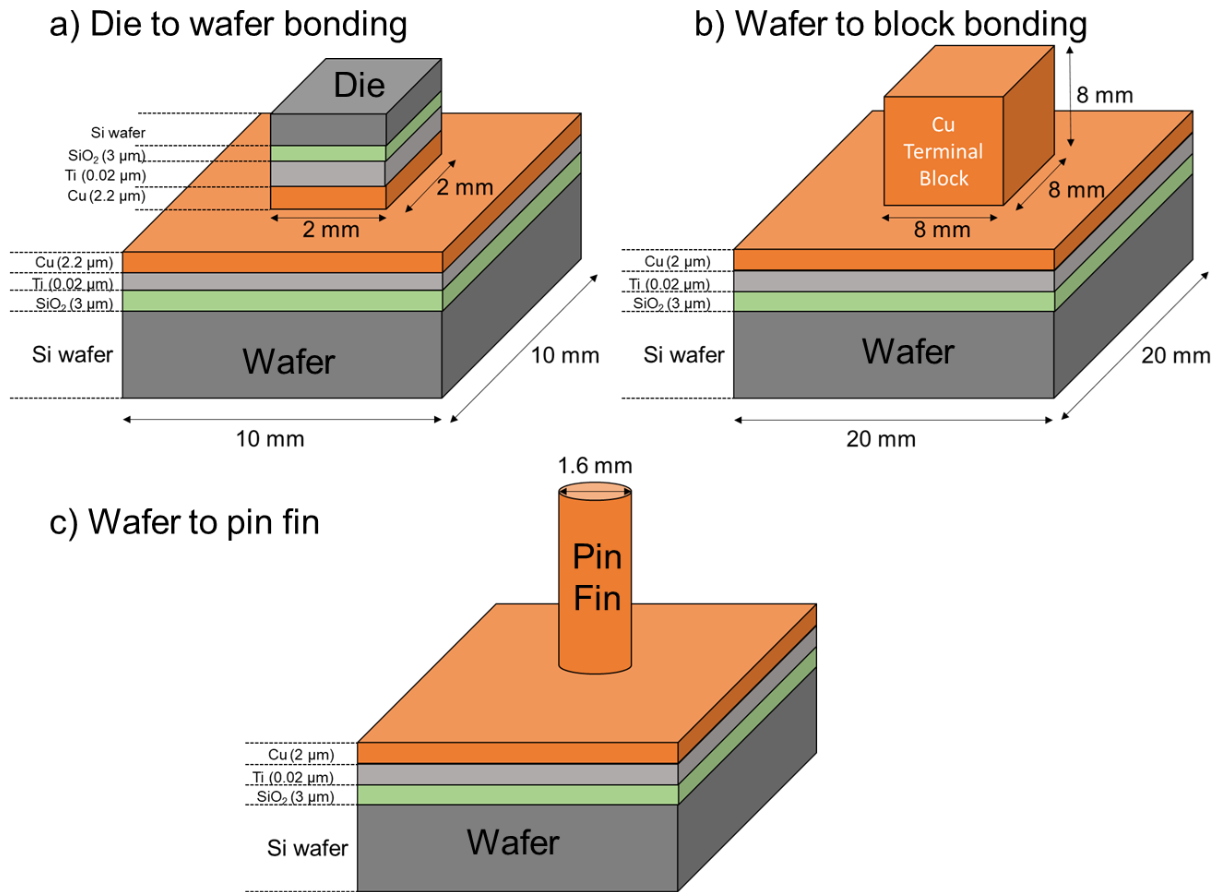

Figure 5: Bond test vehicles. Bonding in the air: a) Die-wafer and b) Wafer-block and bonding in a vacuum- c) Wafer to pin fin.

3.2. Sample Preparation

Samples were produced with a 100 mm Si wafer with <100> orientation. A 3 µm thick thermal oxide layer was grown on wafers. The metal layers, 30 nm Ti as barrier and adhesion layer and 200 nm Cu as the seed layer, were sputter deposited on the oxide-coated wafers in CVC 601 metal deposition system. 2 µm Cu was electro-deposited on the seed layer using Technic electroplating setup. The thermal oxidation and metal deposition processes are compatible with the Si-IF fabrication process (10). The wafers were then diced into 2x2 mm^2 (referred to as dies) and 10x10 mm^2 square samples for bonding in air. No polishing was performed on diced samples. Cu terminal blocks with dimensions 8 x 8 x 8 mm3, were polished to prepare a flat and smooth surface. The pin-fin samples, 1.6 mm diameter and 25 cm length, were lapped and polished to reduce surface roughness. Terminal blocks and pin-fins were both mounted on the custom jig as shown in Figure 3 and polished with a Logitech PM-5 polisher. Cabot C8902 was used with soft polyurethane pad and polishing was performed at 30 rpm and 5 kPa pressure.

3.3. Bonding Parameters and Procedure

Samples were cleaned ultrasonically in acetone for 5 min, water for 1 min, and then dipped in acetic acid for 20 min to clean the surface and reduce the native oxide on the copper bonding surface. Bonding in the air was performed on a hot plate from 200 to 350 °C with a ramp-up rate of 4 °C/min. These temperatures were chosen so that the PowerTherm bonding process is compatible with standard Si-IF die to wafer bonding. 2.5 MPa pressure was applied to all the samples. Samples bonded in the air were wrapped in Al foil to diminish oxidation of wafer and block. Wafer to pin-fin bonding was performed in a custom bonder that supported vacuum (10^{-5} Torr). Bonding in air and vacuum bonding was performed for 1 hour each. Table 1 shows the bonding experiment details.

Type of Cu-Cu Bonding	Surface Treatment	Temperature (°C)	Time of Bonding (min)	Bonding Pressure (MPa)	Measurements
Die - Wafer	N.A.	200 - 350	60	2.5	Shear
Die – Block	Lapped	300	60	2.5	Shear
Wafer – Pin fin	Lapped, Polished	300	60	2.8	Shear, Electrical

Table 1: Cu-Cu bonding experiment details for all the structures.

3.4. Characterization

Atomic force microscopy (AFM) was used to determine the surface roughness of copper surfaces. Quesant Q-Scope AFM system was used to collect roughness information, typically scanning 40 x 40 µm^2 randomly chosen area across the bonding surface. X-ray diffraction was used to qualitatively study materials properties of Cu film on wafer and block before bonding. The grain size of the electroplated Cu layer and the preferred orientation of bonding surfaces were determined with 2θ: ω scans. An ω offset of 3° was used to circumvent the high-intensity Si (004) peak. The scans were performed using a Jordan Valley D1 diffractometer, which had incident beam optics to produce a parallel beam of Cu Kα radiation. The electrical resistance of wafer-pin fin samples was determined by the four-probe measurement method. Shear strength was measured using Nordson Dage 4000 Plus shear tester. Since multiple pin-fins were bonded simultaneously, PBI jig needed to be removed before the shear test to measure the shear strength of the individual bond. The PBI structure was removed by wet etching Cu pin-fins using $FeCl_3$. A schematic showing this process is shown in Figure 6. A test height of 5 µm above the bonding surface and a test speed of 10 µm/s was applied. Three samples for each bonding condition were tested. Fracture surfaces were investigated with a Keyence VHX 6000 optical microscope.

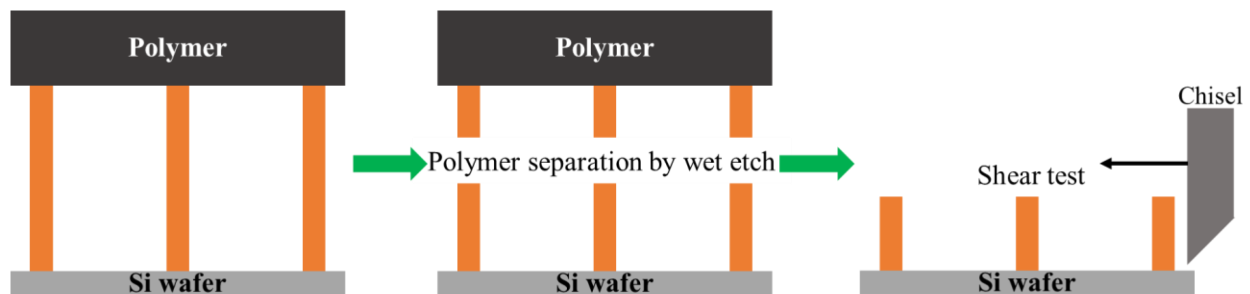

Figure 6: Schematic showing process flow to enable shear test on individual bonds.

3.5. Experimental Results

3.5.1. Cu-Cu Bonding in Air

X-ray diffraction of the unbonded wafer and Cu block is shown in Figure 7 and Figure 8Figure 8. The presence of peaks additional to those of Cu reveals the presence of copper oxides and hydroxides at both wafer and block surfaces even after the acetic acid treatment. From the same set of diffraction patterns, information about the preferred orientation of grains was extracted using Equation 1:

$$C_i = \frac{\frac{I_i}{I_{Ri}}}{\frac{1}{N}\sum_1^N \frac{I_i}{I_{Ri}}}$$

Equation 1:Equation for estimating preferred orientation.

where: where i refers to plane orientation, C_i is the texture coefficient, I_i is the integrated intensity of a peak, I_{Ri} is the intensity of randomly oriented sample, N is the number of reflections considered in the analysis. Peak intensities measured from wafer and terminal block along with the calculated texture coefficients are shown in

Table 2. The electroplated wafer showed a strong preferred orientation in (111) and (200) directions compared to (220) direction shown by the block. The grain sizes were also estimated from diffraction patterns and found to be 29 nm for wafer and 34 nm in terminal blocks.

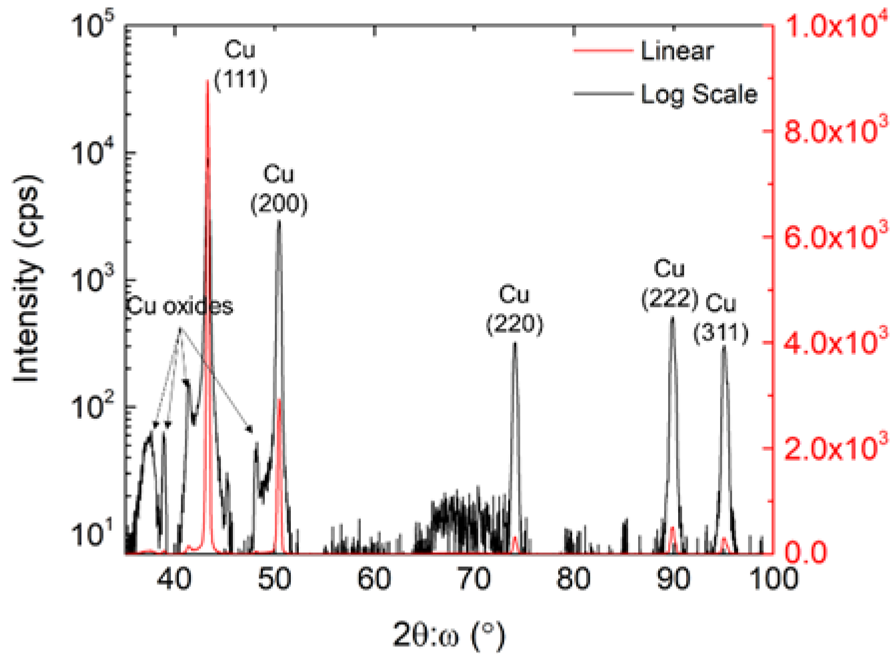

Figure 7: X-ray diffraction 2θ: ω scan of the unbonded wafer with indexed peaks. Linear intensity scale (red) and its logarithmic intensity scale (black) are shown.

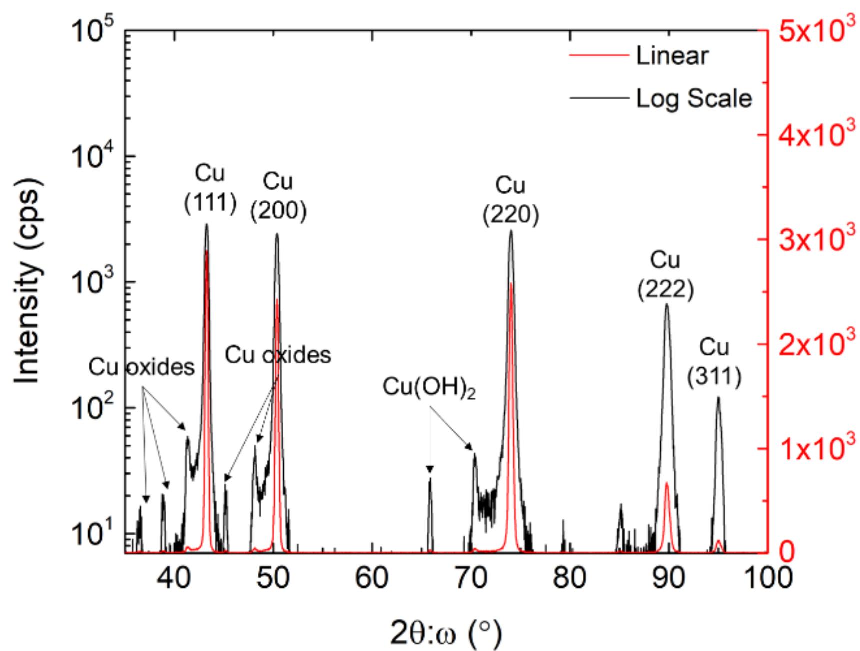

Figure 8:X-ray diffraction 2θ: ω scan of the unbonded terminal block with indexed peaks. Linear intensity scale (red) and its logarithmic intensity scale (black) are shown.

				Texture Coefficient	
Plane	Normalized I_{Random}	I_{wafer} (cps)	$I_{Terminal\ Block}$ (cps)	Wafer	Terminal Block
111	100	9012	2917	1.88	0.53
200	46	2971	2447	1.35	0.96
220	20	363.50	2605	0.38	2.36
311	17	324.80	137	0.4	0.15
Standard deviation				0.64	0.83

Table 2: Measured peak intensities from the diffraction patterns along with the calculated texture coefficient.

The AFM scans are shown in Figure 9a and b show surfaces of the plated wafer and terminal blocks post acetic acid treatment. The surface roughness of the lapped Cu terminal block was 23 ± 2 nm and the roughness of electroplated wafers was 9 ± 0.1 nm. The profiles of lines drawn in Figure 9and Figure 9b roughness can be seen in Figure 9c.

Figure 10 shows an average die – wafer shear strength for different bonding temperatures. The shear strength almost tripled for samples bonded at 300 °C compared to those at 200 °C, whereas it decreased by a similar amount when bonded at 350 °C. The highest average shear strength among all bonding temperatures was 11.2 MPa at 300 °C. We used MIL 883 E criteria to estimate the quality of our bonds. This standard requires 6 MPa or higher shear strength for bonding to be considered sufficient. Since highest shear strength between die-wafer samples were achieved at bonding temperature of 300 °C, copper block to wafer bonding was performed at this temperature. A maximum shear strength of 16.9 MPa was achieved.

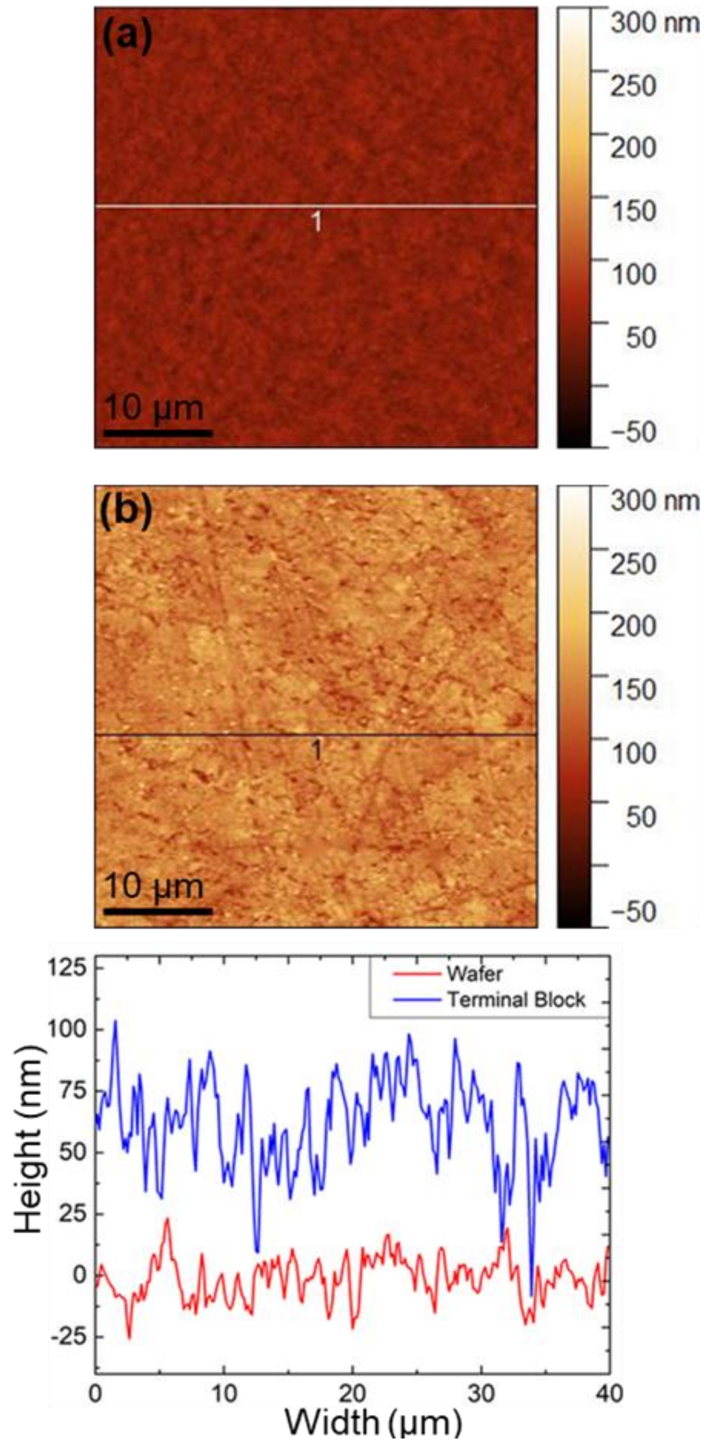

Figure 9: AFM topology of (a) as-electrodeposited Cu on Si wafer surface with RMS roughness of 9 nm, (b) lapped terminal block with RMS surface roughness of 22 nm. Corresponding line profiles were drawn in (a) and (b) are shown in (c).

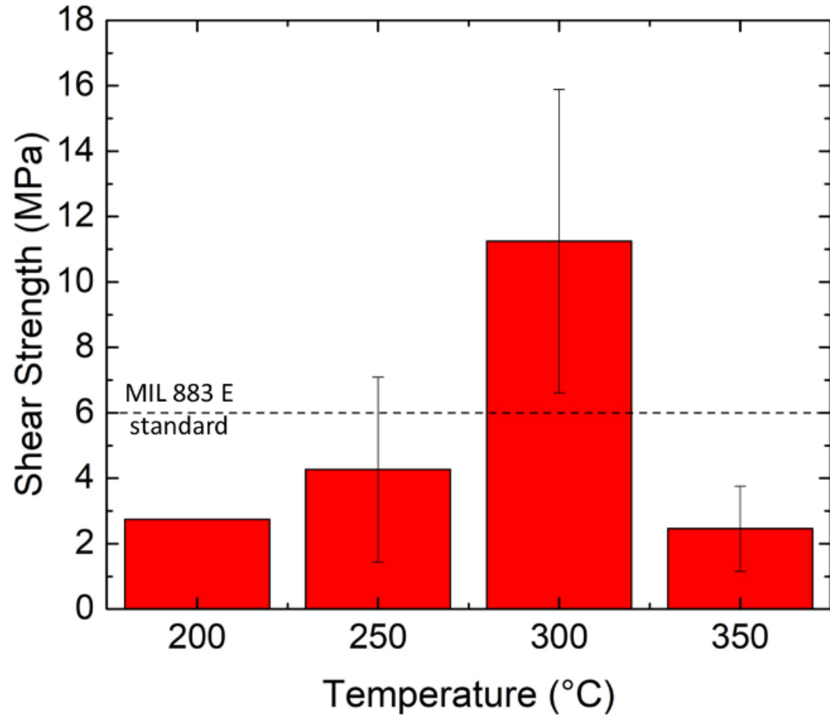

Figure 10: Shear strength of die-wafer bonding at 2.5 MPa, 200-350 °C for 60 min.

Fracture surfaces of Si and Cu were examined using optical microscopy. The fractures were classified as adhesive if the fracture occurred at the Ti-Cu interface; cohesive – if the fracture occurred either in Si wafer or Cu film or mixed fracture which had a combination of adhesive and cohesive modes (13). Optical images revealed a combination of cohesive fracture in Copper film and Si wafer. This indicates strong bonding as the fracture interface was different and away from the bond interface.

Figure 11 shows an optical microscope image of a sample bonded at 300 °C.

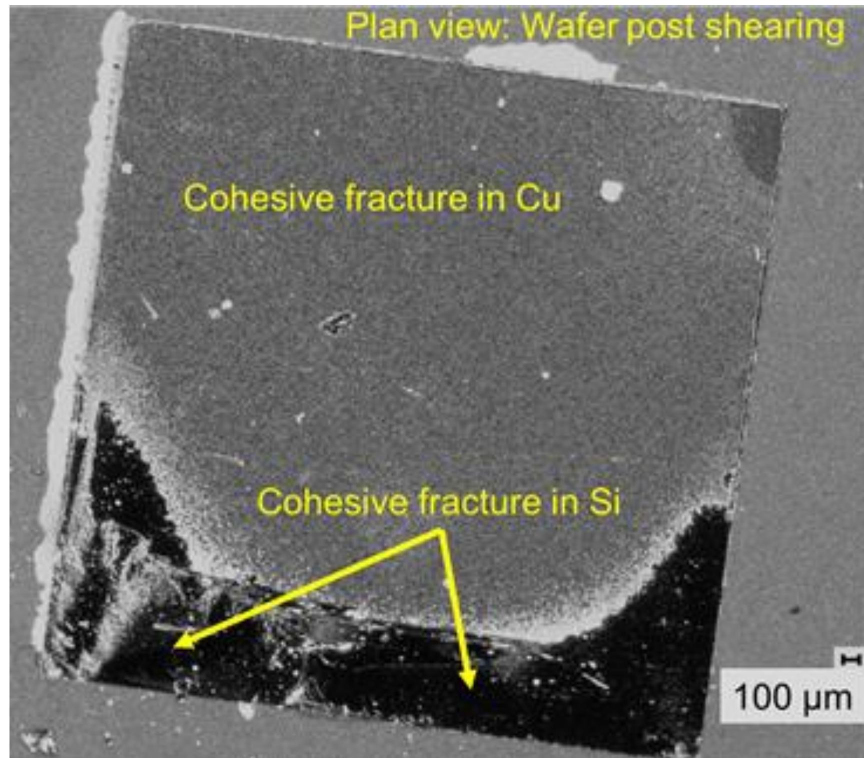

Figure 11: Optical microscope image of the wafer bonded at 300 °C, 1-hour post shear test. The image reveals a cohesive fracture in bulk Si and the copper layer.

3.5.2. Cu-Cu Bonding in Vacuum

AFM scans of samples post acetic acid treatment and before being bonded in vacuum are shown in Figure 12. The RMS surface roughness of ground Cu pin-fin was 104 nm, RMS surface roughness of polished Cu pin-fin was 22 nm and the roughness of electroplated wafers was 9 ± 0.1 nm. An optical image of the bonded structure is shown in Figure 13.

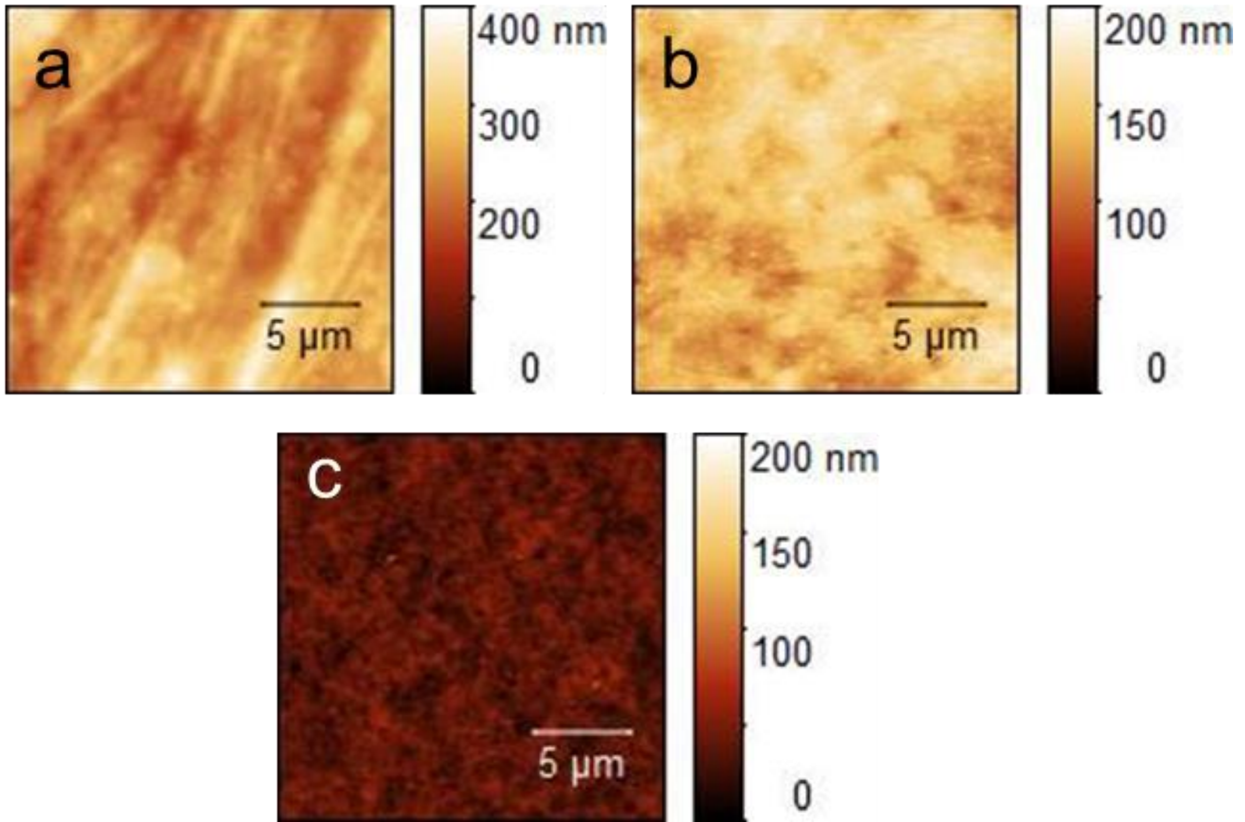

Figure 12: AFM scans of samples bonded in vacuum. a) Ground Cu pin-fin, b) Polished Cu pin-fin

c) Cu on Si wafer.

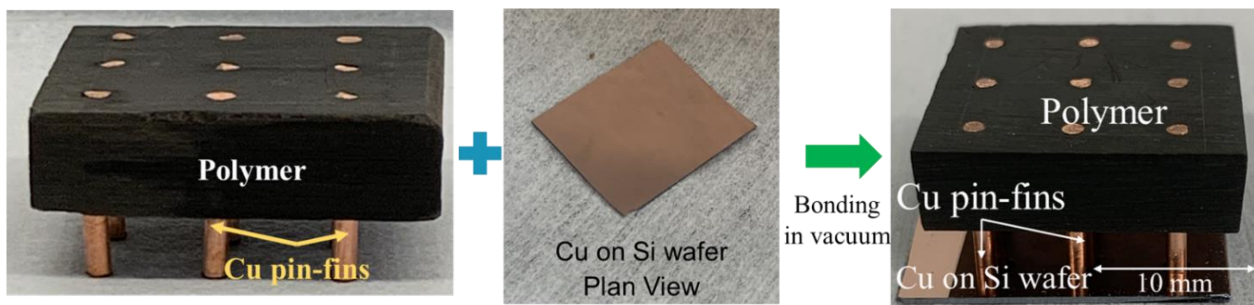

Figure 13: Cu pin-fins bonded to Cu on Si wafer in vacuum.

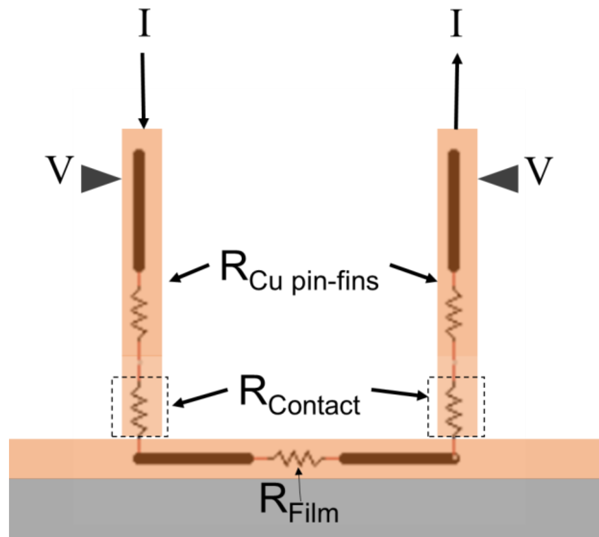

Figure 14:Schematic of the model used for extracting resistance of Cu-Cu bond.

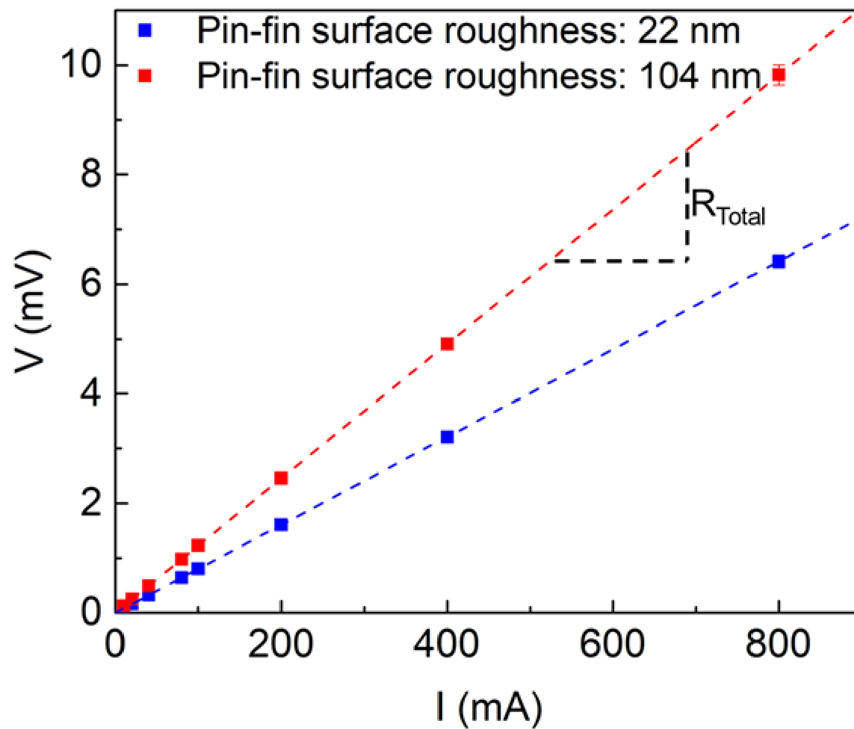

Figure 15: V-I plot obtained from the four-probe measurement.

The electrical resistance of the pin-fin – wafer – pin-fin structure was measured with the four-point probe method. A schematic model showing the pin fins and film is shown in Figure 14. The

total resistance i.e. the resistance due to Cu pin-fins, bond resistance, and film resistance was measured. It is defined as:

$$R_{Total} = 2R_{Cu\ pin-fin} + 2R_{Contact} + R_{Film} \text{ (Equation 2)}$$

Using this equation, $R_{Contact}$ for both the bonded samples was calculated and shown in Table 3.

Resistance (mΩ)	**Cu pin-fin surface roughness**	
	Rough (104 nm)	Smooth (22 nm)
R_{Total}	12.3	8
R_{Film}	6.3	5
$R_{Cu\ pin-fin}$	1.75×10^{-2}	1.75×10^{-2}
$R_{Contact}$	3	1.5

Table 3: The table shows the resistance of each component in the model.

The shear strength and force results are shown in Figure 16. The strengths are sufficient to satisfy the MIL 883 E standard and indicate strong bonding.

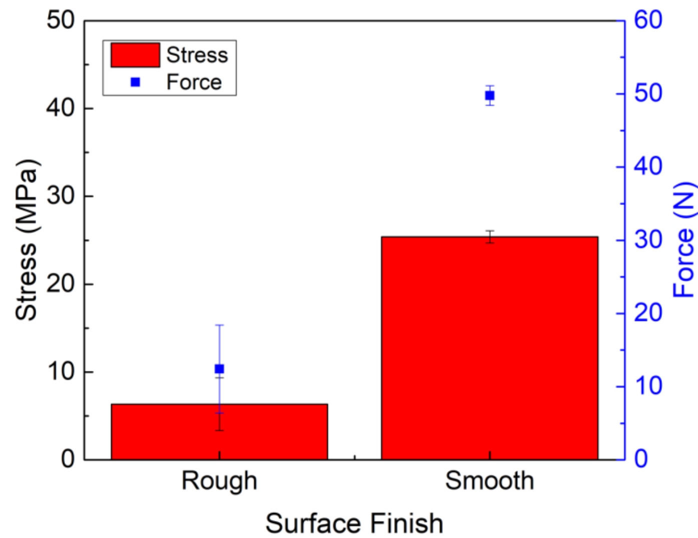

Figure 16: Shear strength and force vs. surface finish of Cu pin-fins.

3.6. Discussion

The roughness of the bonding surfaces, both at nano and macro-scale(flatness), plays a key role in bonding, especially at lower temperatures and pressures. Previous studies have studied the role of surface roughness on the threshold bonding temperature for Cu-Cu thermocompression bonding (14). The temperature of bonding for acceptable strength (300 °C) as seen in Figure 10, agreed well with the previously reported study (14) for 9 nm RMS roughness despite differences in other factors such as surface impurities, the presence of oxides, grain size, and texture. These factors have been qualitatively characterized in this study. Wafer and terminal block both have small grain sizes (29 and 34 nm), which are expected to help in bonding due to higher grain boundary density at the interface which in turn promotes the diffusion of copper atoms to the interface (15). A preferred orientation of (111) planes at the bond interface is desirable as Cu has the highest self-diffusion constant on (111) planes and has found to enhance bonding (16).

An increase in temperature reduces the mechanical properties such as Young's modulus and yield strength of copper apart from increasing atomic diffusivity. An increase in bonding temperature would, therefore, increase the true contact area between bonding surfaces on the application of pressure at the interface due to a reduction in mechanical properties and therefore, a stronger bond would form as evident in Figure 10. Previous study has linked shear strength to true contact area (11). This can explain the increase in shear strength with temperature as observed in Figure 10.

An increase in temperature would also increase oxidation as evident from Figure 17. Figure 17 shows a comparison of X-ray diffraction patterns of the annealed wafer and unbonded wafer. The increased number and intensity of copper-oxide peaks and reduced intensity of elemental

copper peaks in Figure 17 suggests that there exists a thick surface oxide at the bond interface. Figure 18 shows oxide growth vs. time at different temperatures, plotted from empirically derived equation (10):

$$T_{Ox}(\text{Å}) = 0.0076 \times e^{0.022} \times T \times \log t \text{ (Equation 3)}$$

where T_{ox} is the copper oxide thickness, T is the temperature in K and t is time in seconds.

Figure 18 suggests that copper oxide during bonding at 350 °C in the air is significantly thicker compared to oxide thickness before bonding began and at other bonding temperatures. Copper oxides at the interface and other contaminants need to be decomposed or dissolved before copper atoms can intimately come in contact with each other and diffuse across the interface (17) to form a bond. Therefore, the decrease in shear strength at 350 °C in Figure 10, might be an outcome of the growth of thicker copper oxide layer at the interface before sufficient areas of elemental copper surfaces can contact each other and initiate bonding. Additionally, reduction in the intensity of Copper peaks suggests that there might be insufficient elemental copper on bonding surfaces to initiate bonding.

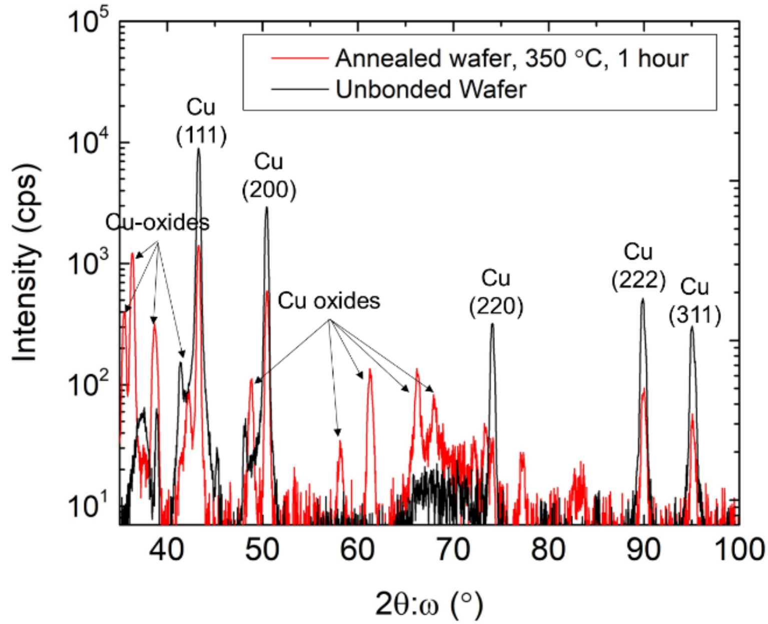

Figure 17: Comparison of X-ray diffraction scans for unbonded and wafer annealed in air (350 °C, 1 hour).

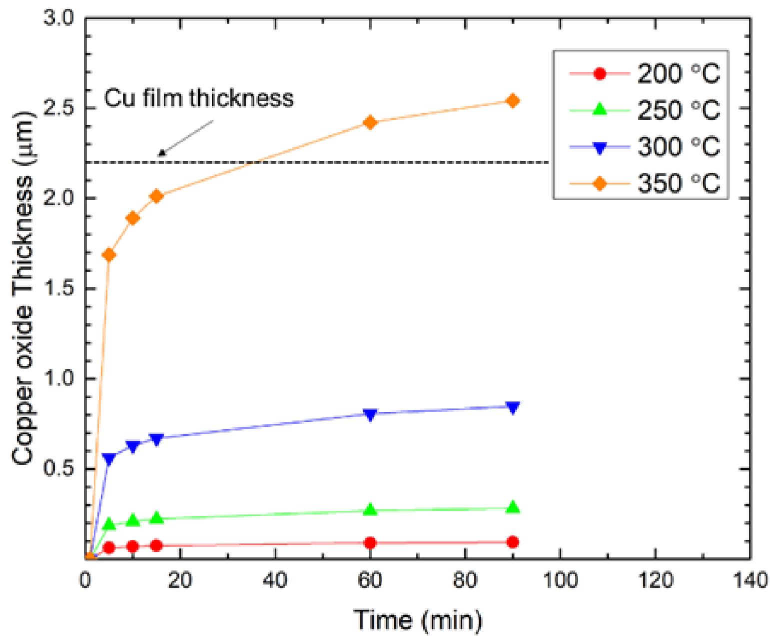

Figure 18: Copper oxide thickness growth at elevated temperatures plotted vs. time.

Copper oxidation can be diminished by bonding in vacuum. It is therefore expected that samples bonded in the vacuum will possess higher shear strength due to a cleaner metallic surface. This is evident by comparing Figure 10 and Figure 16 where samples bonded in vacuum and

having comparable roughness exhibited 2.2X shear strength as those bonded in air. Further, the increase in shear strength(Figure 16) and reduction in electrical resistance(Table 3) on reducing surface roughness can be attributed to an increase in the true contact area and consequently increased bonding.

4. Custom Bonder Construction

4.1. Motivation

Current experiments indicate that if the true contact area between the bonding surfaces can be increased, the shear strength can be increased, and electrical resistance can be decreased. So far, this was achieved by increasing bonding temperature, change of bonding environment from the atmosphere to vacuum, and reducing roughness. These parameters have their disadvantages. For example, a high bonding temperature, especially for a long bonding duration may cause atomic diffusion in other parts of Si-IF causing a reliability concern. The polishing of multiple pin-fins to sub 20 nm has proved to be challenging. Scaling of the process would also require additional efforts. Therefore, alternative ways to increase the true contact area need to be explored. A bonding parameter that was not varied in this study was pressure. This was due to constraints in the bonding apparatus and bonding force was limited to <200 N. If a high bonding force can be applied, then two alternatives are possible. Either the number of pin fins used for bonding can be increased, or the number of pin fins is kept constant while the bonding force is increased. Additionally, Cu-Cu bonding has also been achieved in reducing atmosphere (18). A reducing atmosphere is preferred over vacuum as it is expected to enhance productivity. Some other feasible bonding environments include N_2, N_2+H_2, CO+N_2, etc. To overcome the restriction of bonding force and to increase the choice of bonding atmospheres, the construction of a custom-designed bonder is underway and described in the next section.

4.2. Design and Specifications

The bonder consists of the following components:

1) Sample mounts: Samples are loaded on two chucks, each of which consists of two spring-loaded sample holders to grasp the samples. These chucks also have slots for thermocouples to measure temperature close to the sample-chuck contact area. The sample size that can be accommodated is 1.5” diameter, 1.5” height.
2) Temperature: The chucks are heated by insertion heaters that can reach a maximum temperature of 760 °C. The temperature is read from the thermocouples by a programmable temperature controller that controls the power provided to both the insertion heaters. Temperature control is achieved by inputting target temperature to the controller.
3) Pressure: A pneumatic cylinder fed by an air compressor is used to provide bonding force. The force can be controlled by a valve on the compressor. Piston speed is controlled by a speed control valve. The maximum force that can be applied is 4500 N. This can be increased in the future by changing the pneumatic cylinder. The force applied by the pneumatic cylinder is measured by a load cell placed at the bottom of the assembly. This temperature range of operation of the load cell is 10-60 °C. Therefore, the load cell is shielded from the chuck with low thermal conductivity ceramic insulator. Furthermore, a cooling water jacket is provided to further protect the load cell.
4) Bonding Time: Bonding time is controlled by the Arduino microcontroller which lowers and raises the piston.
5) Atmosphere Control: All the components are enclosed in a removable stainless-steel chamber. Sealing is achieved with the help of O-rings. A vacuum of ~10^{-3} Torr is expected.

Figure 19 shows a schematic of bonder with labeled components.

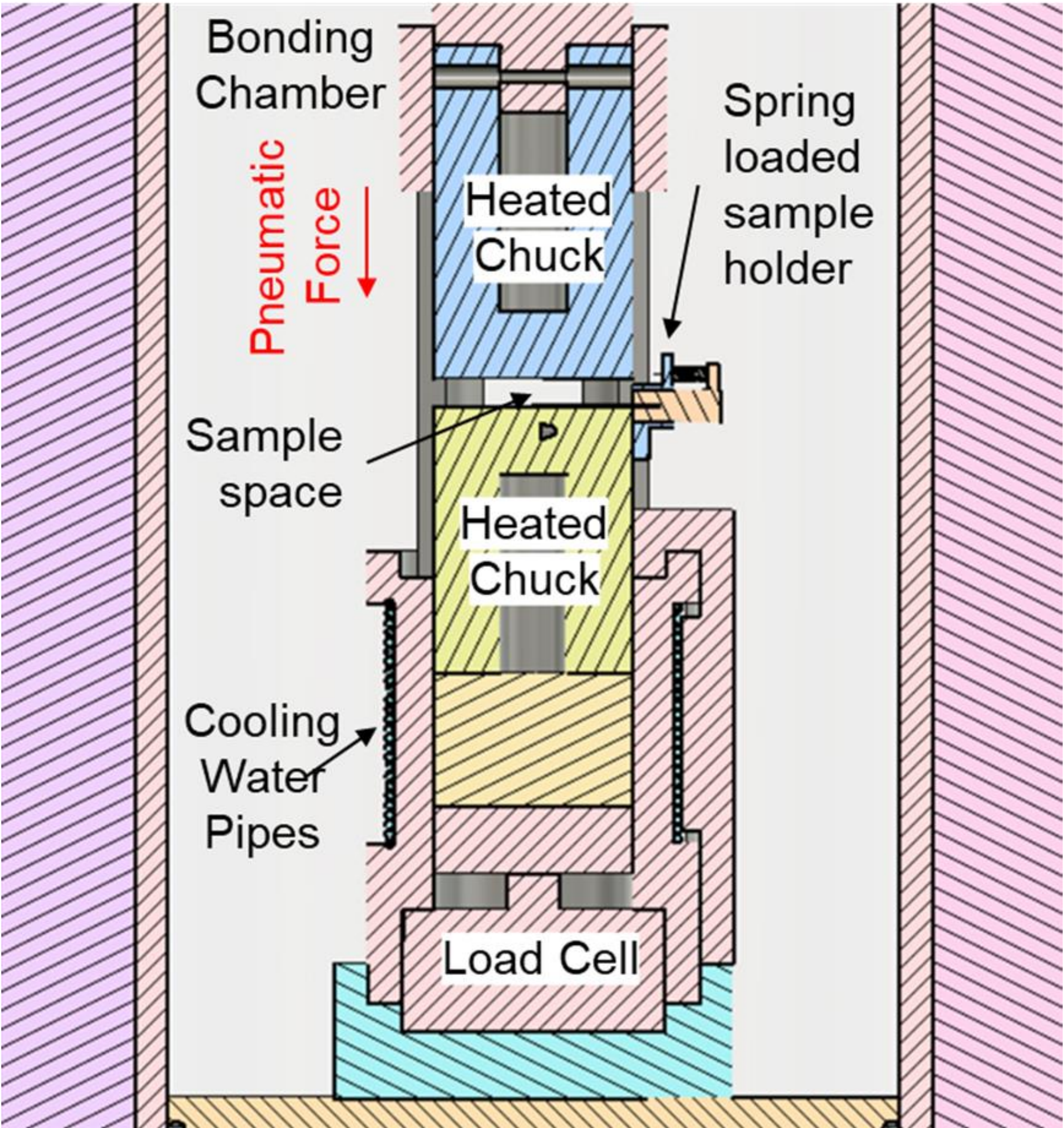

Figure 19: Computer-aided design of thermocompression bonder.

4.3. Progress

The current progress of bonder construction is shown in Figure 20. Major components to be completed on a priority include the addition of a cooling system to prevent cell heating and chamber assembly for atmosphere control.

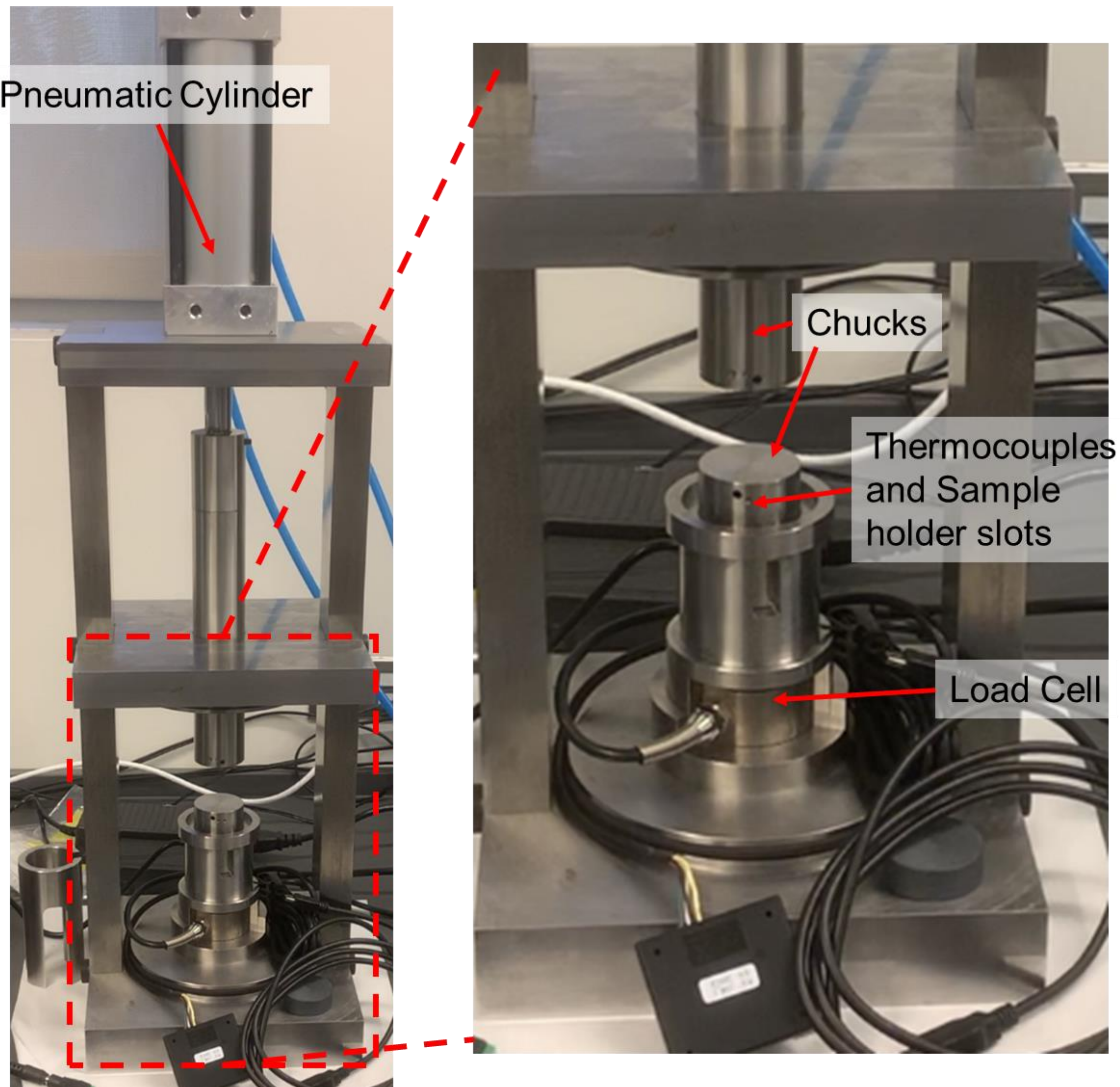

Figure 20: Components in the bonder assembly.

5. Conclusion

Cu-Cu thermocompression bonding at low pressure (≤ 3 MPa) for power delivery and heat extraction from Si-IF has been successfully demonstrated. Increasing bonding temperature, reducing surface roughness and changing bonding environment to vacuum as compared to air were found to be effective in improving bond strength. A maximum shear strength of 24 MPa was achieved. A quantitative study of the bond interface along with Characterization of the bond interface area and its correlation to strength and resistivity is an important future goal of the project. Further reduction of RMS roughness of Cu pin-fins to <10 nm and bonding experiments at higher pressures (5X, 10X and 20X) with the help of custom bonder under construction is planned.

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