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Variation-Aware Modeling and Design of Nanophotonic Interconnects

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by

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To my parents and all my family.

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Abstract

Variation-Aware Modeling and Design of Nanophotonic Interconnects

by

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Optical interconnects have started to replace electrical interconnects in the communications between racks and circuit boards with potential benefits in bandwidth, delay, power efficiency, and crosstalk. Silicon photonics has emerged to be a highly promising enabling technology for the short-reach nanophotonic interconnects because it offers favorable CMOS compatibility and high integration level. The fast-growing complexity of photonic integrated circuit (PIC) and close electro-optical integration call for computer-aided design (CAD) for integrated photonics, and electronic-photonic design automation (EPDA) including accurate behavior models and efficient simulation methodologies for integrated electro-optical systems. Also, the nanophotonic devices are highly sensitive to fabrication process variation and thermal variation effects, which requires proper modeling, optimization, and management schemes. To address these problems, this thesis is dedicated to the following two tasks: (1) compact modeling and circuit-level simulation of nanophotonic interconnects, and (2) power-efficient management of the variation effects in nanophotonic interconnects.

The first part of the thesis develops compact models for key components in nanophotonic interconnects including silicon microring modulators, diode lasers, electro-absorption modulators (EAM), photodetectors, etc. These compact models are developed based on their electrical and optical properties, and are then extensively validated by measurement data. The model parameters are extracted from common electrical and optical tests. Implemented in Verilog-A, the models are used in SPICE simulations of optical

links, whose results again agree well with measurement data. The compact model library and the simulation methodology enable electro-optical co-simulations and optical device design explorations in the circuit-level.

In the second part of the thesis, we propose modeling methods and power-efficient management schemes for the process and thermal variations in optical interconnects. The proposed adaptive tuning technique performs on-chip self-tests and adaptively allocates just enough power for link operations. The technique saves significant amount of power compared to worst-case based conservative designs, and scales well w.r.t. variations and network size. We also design power-efficient pairing algorithms for microring-based optical interconnects. Our algorithms optimally mix-and-match microring-based devices to minimize the power consumption for tuning. The algorithms are tested on both measured and synthetic data sets, demonstrating promising results of power reduction and scalability for handling a large number of devices. Lastly, we decompose and analyze wafer-scale spatial patterns of process variations in microring modulators. We further investigate the correlations between the spatial patterns and fabrication process steps, which is valuable for understanding process variation sources and improving fabrication processes for uniformity.

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Chapter 1

Introduction

The fast increasing complexity of optical interconnects and its sensitivity to process and thermal variations pose the great demand for compact modeling, efficient simulation, and variation management schemes. This chapter introduces background of optical interconnects, motivations of the thesis work, and summary of some related work.

1.1 Background and Motivation

Optical communication posses high bandwidth, high data rate capacity, small propagation delay, low power consumption, small crosstalk, and high tolerance of electromagnetic interference over traditional electrical communication. With the development of optical fibers with low loss, and semiconductor lasers in the 1970s, optical interconnects started to replace electrical interconnects. In the past several decades, the deployment of optical communications has been spread from long-haul backbone networks to metropolitan area networks (MAN) and local area networks (LAN). In recent years, fiber-to-the-home (FTTH) infrastructure are being deployed to address the bottleneck of last mile to customer. Nowadays, optical interconnects are starting to penetrate into the the

short-reach datacom regime [6]: Intel just rolled out its silicon photonics based optical transceivers for data center applications [7]. IBM has been devoted to bringing electrical-optical interfaces closer to processors and memories for over a decade through the development of photonic device and packaging technologies [8]. Oracle's 3D macrochip system enables intimate integration and co-manufacturing of photonic chip and electronic chip [9]. Already achieving the success in rack-to-rack communications, optical interconnects are highly promising for the board-to-board, chip-to-chip, and eventually core-to-core communications. The evolvement of the optical interconnect applications is illustrated in Fig. 1.1 .

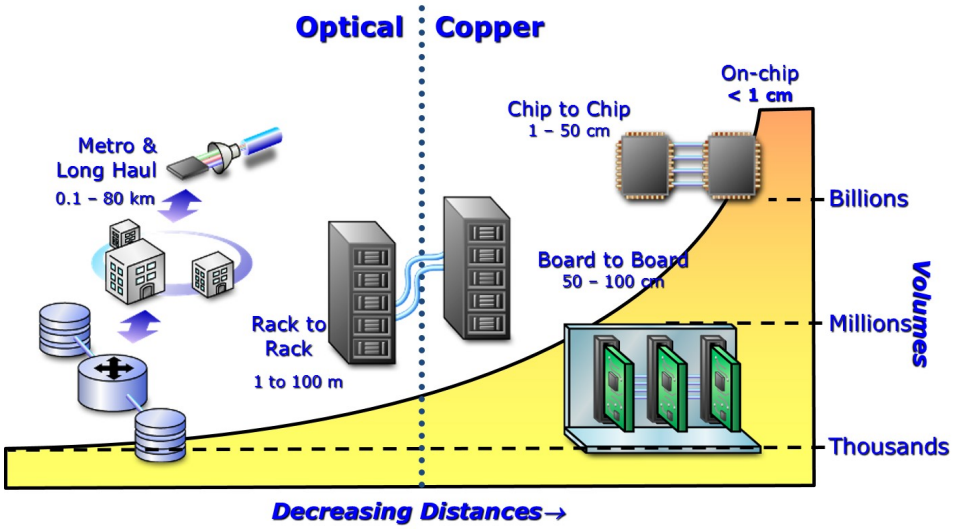


Figure 1.1: The evolvement of optical interconnect distance and production volume. (Courtesy of Intel)

As the distances of optical interconnects decrease, the production volumes grow rapidly, calling for smaller optical device size and higher integration level, and driving the need for nanophotonic devices. Meanwhile, smaller interconnection distances require closer integration of electronics and photonics. Silicon photonics is emerging to meet these demands because of its CMOS process compatibility, manufacturing cost efficiency, and some good optical properties. By sharing the same material with CMOS circuits,

silicon photonic devices can be fabricated side-by-side with electronic circuits (a.k.a. monolithic integration) [10]. Meanwhile, the legacy of the mature CMOS processes could greatly reduce the production cost of silicon photonics. Additionally, silicon/silica material system has high refractive index contrast and is transparent in optical communication wavelengths, enabling silicon waveguide with low propagation loss and low bending loss even for small bending radii [11]. The electro-optical effect (a.k.a. plasma dispersion effect) [12] in silicon makes some silicon based electro-optical modulators available, such as silicon microring modulators [13] and Mach-Zehnder modulators [14] that are based on silicon-on-insulator (SOI) substrates, and are all CMOS process compatible. Though it is hard to develop light emitting and amplifying devices on silicon due to its indirect band gap, several workarounds have been developed to wafer bond or directly grow III-V materials on silicon [15, 16].

With the CMOS friendly silicon photonics technology, the paradigm for future chip would likely be a hybrid electronic-photonic integrated circuit (EPIC) consisting electronic processor and memory parts, and optical transmission part. Fig. 1.2 shows a 3D view of a silicon photonic chip including photonic modulators, waveguides and detectors. These photonic components are fabricated with electronic transistors back-to-back.

The ever increasing integration level in short-reach optical interconnects drives more and more components integrated on one photonic integrated circuit (PIC). Fig. 1.3 shows the number of components on one PIC grows exponentially over time, which somewhat follows the Moore's Law of the microelectronics regime. The fast growing complexity of photonic integrated circuits (PICs) drives the need for photonics design automation tools, including trustworthy photonic circuit level models and simulators, photonics property-aware automatic floor planning [17], layout and routing [18], design rule checking (DRC), and logic vs. schematic (LVS) [19]. Photonics designers need circuit and link level PIC design, layout, and simulation tools. Meanwhile, electronic circuit designers need

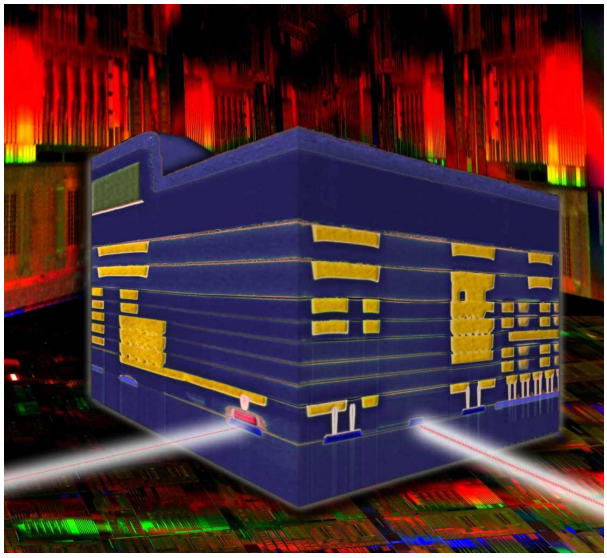


Figure 1.2: IBM's silicon photonic chip. (Courtesy of IBM)

accurate compact models of photonic devices to design the complex PIC drivers. All of these demands call for proper computer-aided design (CAD) tools for photonics and electronic-photonic design automation (EPDA) softwares.

Thermal variation and fabrication process variation problem significantly arise in short-reach optical interconnects. The performance and characteristics of optical devices can highly depend on its operational temperature. In conventional long-range optical interconnects, optical devices or modules can be individually cooled by dedicated temperature controllers because the conventional optical modules are individually packaged, and the long-range communications can afford the expense and power of the temperature controllers. In contrast, the nanophotonic components in short-reach optical interconnects are highly integrated and are even closely placed with electronic devices, which makes dedicated temperature controllers impossible. Therefore, it is desired to accurately model and manage the device performance with complicated temperature fluctuations in a electro-optical integrated system.

Fabrication process variation is another sever problem for nanophotonic devices, since

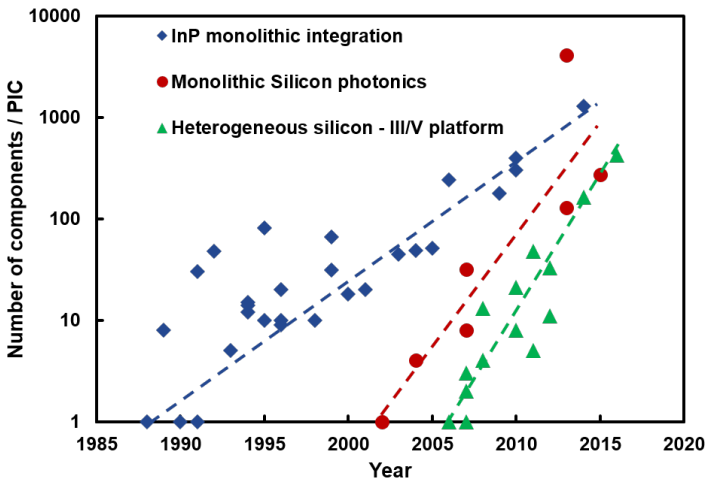


Figure 1.3: Number of photonic components integrated on one photonic chip over the past decades for three integrated photonics technology platforms. (Courtesy of J. Hulme)

the photonic device dimension enters the hundred of nanometers regime, and the absolute process variation amount takes a large portion of the device dimension. The process variations can cause performance degradation or even failure of the optical devices and systems, and therefore need to be modeled and managed effectively and efficiently.

In summary, silicon photonics based short-reach optical interconnect raises problems in CAD for photonics, and management of thermal and process variation effects. This dissertation focuses on these two problems.

1.2 Overview of Optical Interconnects and Devices

Fig. 1.4 illustrates an optical interconnect structure including one transmitter (Tx) and one receiver (Rx)[1]. The CMOS die consists modulator driver, and receiver circuits. Processor cores or memories could be placed on the CMOS die in on-chip or chip-to-chip interconnects. In this scheme, light is generated by an off-chip multi-wavelength

[1]It can be easily extended to multi-Tx/multi-Rx structure or network using optical switches.

light source, and then coupled onto chip by a grating coupler. To avoid the coupling loss, on-chip heterogonously integrated III-V on silicon lasers could be utilized [1], while the heterogonously integration will increase the process complexity. The light propagates through the silicon waveguide, and is modulated by an array of silicon microring modulators. The microring modulator is capable of modulating the light at a specific wavelength. The colors of the microrings in Fig. 1.4 represents various wavelengths. Similarly, in the receiver side, light at a corresponding wavelength is routed by a microring filter to a photodetector (PD). These wavelength selective microring structures implement wavelength-division multiplexing (WDM) without dedicated (de)multiplexers. The Tx and Rx could be on the same chip, on different chips, or different boards, connecting by on-chip waveguides, on-board polymer fibers, or optical fibers to achieve on-chip, chip-to-chip, or board-to-board communications.

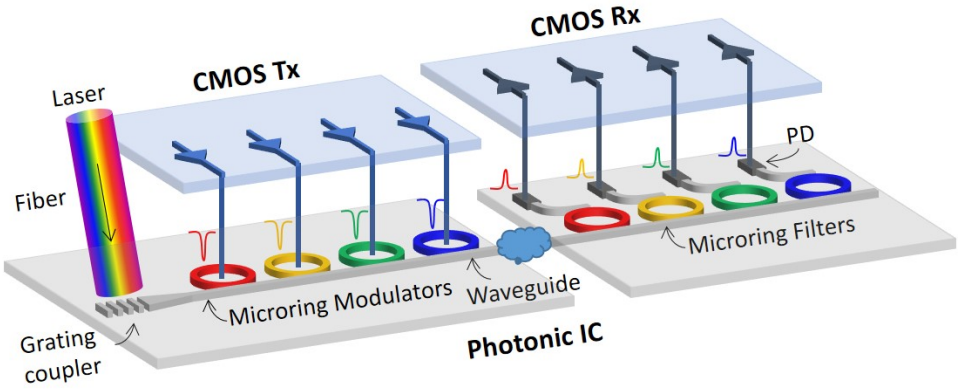


Figure 1.4: A silicon photonics based optical interconnect structure.

Here we introduce the SOI-based silicon photonics platform, and several selected photonic components.

1.2.1 SOI Platform and Silicon Waveguide

Silicon photonics usually utilize SOI wafers to fabricate photonic components, since the light confinement needs a high refractive index core and low index claddings, and the buried oxide (BOX) under the silicon layer in the SOI wafer can server as the lower cladding. The upper cladding could be either air or SiO_2. Fig. 1.5 (a) shows a silicon waveguide fabricated on the SOI platform, which serves as a basic building block for other complex silicon photonic components. The waveguide is defined by partially or fully etching the silicon layer, constructing wire[2] or rib waveguide. The partially etched rib waveguide needs careful control of etch depth, while it has the advantages that the rib could serve as the current path in active devices, and it is more tolerant to sidewall roughness and less likely to have resonance splitting in microrings than the fully etched waveguide. SOI wafers with various silicon thicknesses are being used, for example: 220 nm in [20], 250 nm in [21], and 500 nm in [1].

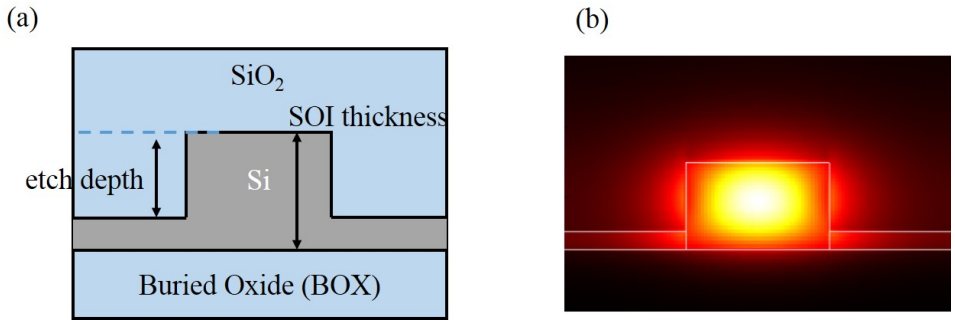


Figure 1.5: Cross section of a silicon waveguide and its optical mode illustration

Fig. 1.5 (b) illustrates the optical mode profile (or the optical power distribution) of the silicon waveguide. Silicon wire or rib waveguide could support certain number of discrete optical modes, depending the waveguide index profile and geometry [22]. Each mode has its effective refractive index n_{eff}, from which the propagation constant could

[2] a.k.a strip waveguide

be calculated. Usually on-chip waveguides are designed to be single-mode such that it supports only the fundamental mode.

1.2.2 Laser

Silicon is not suitable for light generation due to its indirect band gap. III-V materials, the traditional material to provide optical gain, could be bonded to SOI wafers. Fig. 1.6 shows a heterogenous III-V on silicon distributed feedback (DFB) in-plane laser and a microring laser. III-V material pieces are bonded to pre-patterned SOI substrates through low temperature bonding process[1, 2]. An InP layer helps the crystal transition between the III-V quantum wells and SOI. The III-V material layers generate optical gain when current is injected into the quantum wells. Optical taper structures allow the light to be evanescently coupled into the III-V layers from SOI waveguides (i.e. the optical mode appears both in the III-V and the silicon regions). In this way, light is generated in the III-V region and transferred to the silicon waveguide.

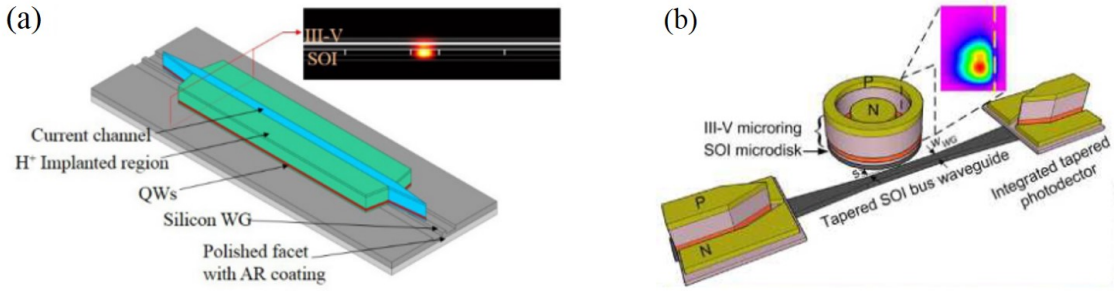


Figure 1.6: 3D view of in-plane and microring heterogeneous silicon lasers [1, 2].

Researchers also grow III-V quantum dots on SOI substrate [16, 23]. Quantum dots are investigated for direct growth because they could mitigate the unwanted dislocations caused by material difference between compound semiconductors and III-V and silicon. Additionally, quantum dot lasers promise high temperature stability and low threshold

current density due to three dimensional carrier confinement compared to quantum well lasers.

1.2.3 Microring-based Modulator, Filter and Switch

A basic microring resonator consists of a silicon microring waveguide and one or two straight waveguides. Fig. 1.7 (a) shows microring resonator with an input waveguide and a drop waveguide. The light is injected into the input port and is coupled into the microring waveguide. When the the optical path length around the microring is an integer number of the light wavelength (i.e. the resonance condition is met), the constructive interference lets the light energy build up within the microring. Consequently, the through port energy reaches a minima and and the drop port energy reaches a maxima. This wavelength selectivity property could be used to realize a modulator: In Fig. 1.7 (b), current is injected into the microring waveguide by p and n doping, such that the silicon index is changed and resonance wavelength is shifted, achieving on-off keying modulation. Additionally, the routing property of microring resonator makes it very suitable as the building block for complex optical switches [24, 25].

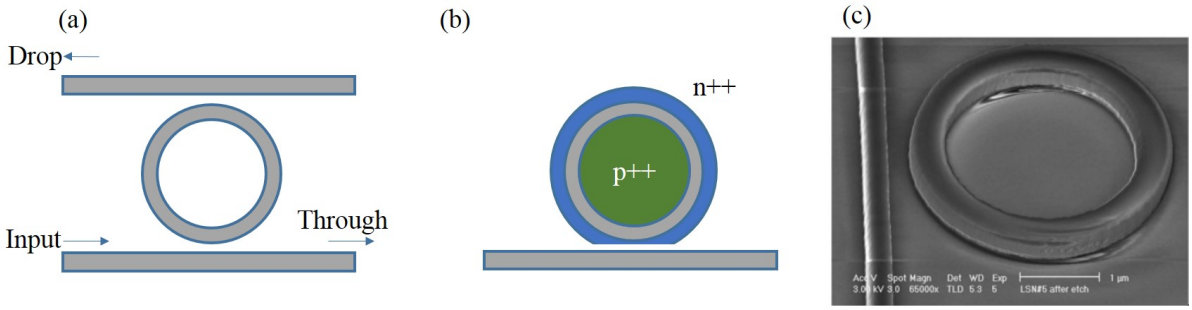


Figure 1.7: (a) Microring resonator, (b) microring modulator, (c) an SEM image of a microring resonator [3].

1.2.4 Photodetector

Silicon photonic interconnects usually use CMOS process-compatible Ge or SiGe photodetectors to convert optical light to photocurrent [26, 27]. In p-i-n based photodiodes, input light could generate electrons and holes in the intrinsic region. With negative bias on the diode, the photocurrent is approximately proportional to the input light energy. The weak photocurrent is usually amplified by receiver circuit.

1.3 Literature Review

There have been a number of prior studies on device-level modeling, and link- or system-level design space exploration of optical interconnects. This section summarizes selected work on device-level and system-level.

1.3.1 Compact Modeling of Photonic Devices

Similar to transistor models, compact photonic device models are needed for accurate link-level simulations of complex optical interconnects. Kononov [28] presented several simple photonic device models. These models were further implemented in Verilog-A by defining new optical natures to describe the optical magnitude and phase. Verilog-A is a analog hardware description language, and can be accepted by many modern versions of SPICE simulators (e.g. Synopsys HSPICE, and Cadence Spectre). Verilog-A photonic device models can be co-simulated with electronic circuits, and has been more and more attract for photonic device modeling: Christen *et al.* implemented a model of vertical-cavity surface-emitting laser (VCSEL) for efficient simulation of optical links [29]. Zhu *et al.* developed a detailed Verilog-A model for a traveling-wave silicon Mach-Zehnder modulator, successfully capturing its optical and distributed electrical

properties, and simulating optical eye diagrams [30]. The carrier-depletion based silicon microring modulator was modeled in Verilog-A by describing its optical and electrical behaviors [31]. In [32], the authors developed basic and composite models in Verilog-A, and simulated a WDM interconnect system and a frequency stabilization system. Many photonic foundry service providers are also developing their device models in Verilog-A, such as IMEC [33], and CEA-Leti [34].

1.3.2 System-Level Design of Optical Interconnects

Optical interconnects have been proposed to be used in network-on-chip (NoC) architectures (a.k.a. optical NoC). The unique properties of optical interconnect call for system-level design and management strategies. In the architectural design aspect, Vantrease *et al.* proposed Corona structure based on a fully-connected $64 \cdot 64$ optical crossbar, and a all optical, token-based arbitration scheme. A Clos optial network was proposed in [35] that used point-to-point optical links for state-to-stage communication and electrical routers for routing. Pan *et al.* proposed Firefly architecture that used hybrid electrical and optical interconnects for intra-cluster and inter-cluster communications, respectively [36].

System-level simulation and analysis of optical NoCs are done in many work: Chan *et al.* presented PhoenixSim, a system-level simulator for optical NoC taking into accounts of many photonic device features [37]. Sun *et al.* developed NoC modeling tool called DSENT that could accommodate both electrical and optical networks [38]. Authors in [39] performed systematic crosstalk noise analysis of various optical NoC architectures.

Microring-based optical interconnect suffers from sever thermal and process variation effects: The full system simulation with realistic applications in [40] demonstrated that process and thermal variation poses significant reliability challenges for nanophotonic

on-chip networks. The authors further modeled the reliability and proposed run-time thermal management guidelines regulating the peak temperature and the thermal gradient [41]. Similarly, Zhang *et al.* proposed a job allocation technique that minimizes the temperature gradients among the microring modulators/filters [42]. Cross-layer and thermal aware placement and floorplanning for optical NoC chips are performed in [43, 17]. To address the wavelength mismatch issue in an energy efficient manner, Zheng *et al.* proposed several techniques which greatly saved the total tuning power consumption [44, 45, 17]. The techniques include channel remapping, sub-channel redundant rings, transceiver-based network, fabricating fewer rings, and tuning fewer rings. Observing the fact that power consumption of an optical link scales with its data rate, authors in [46].

1.4 Thesis Outline

This thesis mainly consists two parts: Chapter 2-4 presents our work on compact modeling and link-level simulation of optical interconnects. Chapter 5-8 discusses modeling and management techniques of process and thermal variations in silicon photonic interconnects.

Chapter 2 presents compact models for various characteristics of microring-based modulators and filters. Several other common photonic devices are modeled in Chapter 3 including their optical and electrical models, forming a device model library together with Chapter 2. Chapter 4 demonstrates circuit-level simulation results of two fabricated links based on the well validated device library.

In Chapter 5, an adaptive tuning technique is proposed to save power consumption by allocating *just enough* power for each link through on-chip self tests. Chapter 6 designs optimization algorithms that pair microring-based optical transceivers so that their thermal tuning power is minimized. Spatial patterns of wafer-scale process variations are

decomposed and analyzed in Chapter 7. Lastly, this thesis is concluded by Chapter 8.

Chapter 2

Compact Models for Silicon Microring-based Modulators and Filters

In this chapter, we developed compact models for silicon microring modulators, an important and versatile component in silicon photonic platform, in several important aspects including its design space, spectra at bias, electrical properties and large-signal dynamic behavior. The model is extensively validated by measurement data and then implemented in Verilog-A that is compatible with CMOS simulators.

2.1 Introduction

In silicon photonic interconnects, microring modulators are of great importance. The carrier-injection p-i-n type and the carrier-depletion p-n type are widely reported [47, 48, 49, 50, 51, 52, 53]. The carrier-depletion type has a high intrinsic bandwidth, as it does not rely on slow diffusion of minority carriers [51, 52]. However, the carrier-

injection type outperforms the carrier-depletion one in modulation depth and insertion loss due to the large change of refractive index [53, 47]. Meanwhile, the speed of the carrier-injection microring modulator can be greatly enhanced by a pre-emphasis driving scheme [47, 48, 49, 50].

Integrating silicon photonic devices into modern CMOS-VLSI design flows requires co-design of electronic and photonic integrated circuits, in which compact models for nanophotonic devices are needed. Researchers have proposed Verilog-A compact models for the Mach-Zehnder modulator [30], the VCSEL [33], and the pulsed optical source and the photodetector [34]. The carrier-depletion microring modulator has also been compactly modeled in many photonic link simulators (e.g., Lumerical Interconnect [54], RSoft OptSim Circuit [55], and DSENT [38]). Sacher *et al.* proposed a dynamic model for microring modulators in [56]. However, the characteristics of the carrier-injection microring modulator, e.g., the resonance wavelength shift with respect to bias conditions, have not been accurately modeled. In this work, we develop compact DC and small-signal models for carrier-injection modulators to provide physical insights to the device performance for a variety of designs.

The resonance wavelength shift in the microring modulator is essential for the on-off keying modulation. Therefore, we derive a theoretical equation for the resonance wavelength shift. The equation is capable of distinguishing the electro-optical blueshift effect and the thermo-optic redshift effect, enabling the analysis of the device design parameters' impact on the modulator's DC performance. Additionally, the quality factor $\mathbb{Q}$ and the extinction ratio ER are important to determine the link power budget and signal quality [4]. Meanwhile, the $\mathbb{Q}$ and the ER of the carrier-injection microring modulator change significantly with injected current. Therefore, we quantify the dependence of the $\mathbb{Q}$ and the ER on the injected current.

In order to characterize the high-speed behavior of the carrier-injection microring

modulator, we propose a small-signal circuit model. The small-signal circuit parameters are extracted from S11 measurements. The small-signal circuit matches the device structure and provides insights to the dependence of small-signal capacitances and resistances on bias points and design parameters. The small-signal model, together with the DC spectrum model, is implemented in Verilog-A to facilitate co-simulations of photonic and electronic circuits.

2.2 Device Designs and Fabrications

Fig. 2.1(a) shows a microscopic image of a microring modulator fabricated in CEA-LETI's silicon photonic SOI process. The rib section of the microring waveguide is 250 nm x 450 nm, and a slab section of 50 nm is used to inject carriers from the p-doped ($3 \times 10^{19}\text{cm}^{-3}$) and n-doped ($3 \times 10^{19}\text{cm}^{-3}$) regions, as shown in the Fig. 2.1(b) inset. There are several device design variants including microring diameter, guard distance (GD) between the boundary of doped region and rib waveguide, and the coupling gap between the ring waveguide and the bus waveguide. As part of process development, 25 wafers are used for engineering purposes. A set of short-loop wafers (Batch B) are processed through some subset of the total process steps to provide a snapshot of process reliability and modulators performance before the final delivery. We find that the contact resistance in this batch is significantly higher than the expected value due to miscalculation of the via etch depth. This contact resistance error has been corrected in the final delivery (Batch A).

In the experimental setup, vertical fiber-to-chip grating couplers are used to provide optical input and output access. Using a tunable laser, a DC voltage source, and an optical power meter, we measure the transmission spectra sequence of a microring modulator with respect to different bias current as shown in Fig. 2.1(b), where the colorful

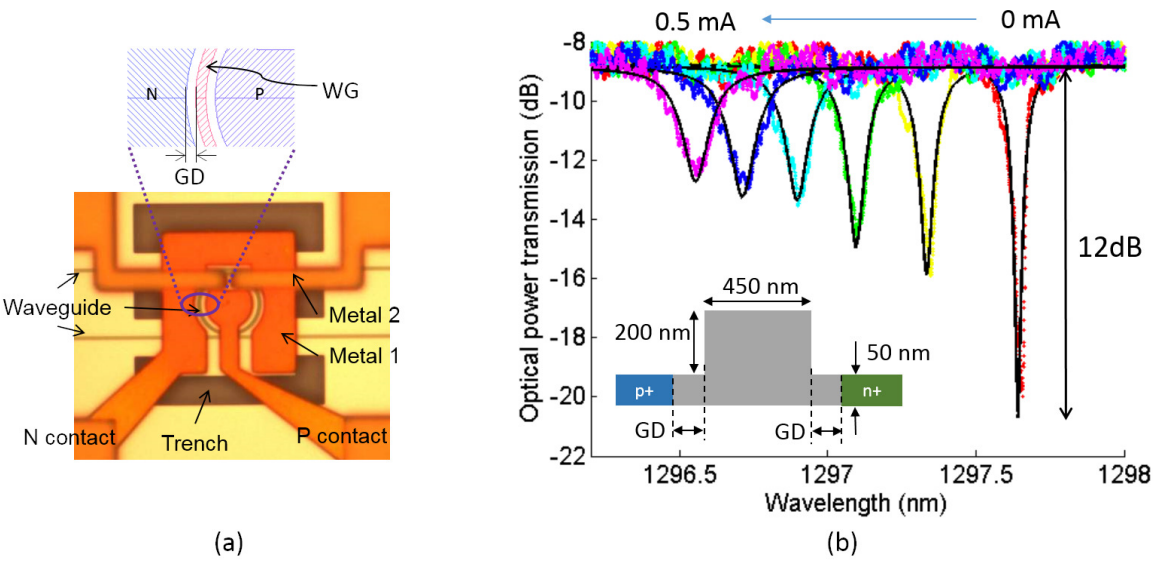


Figure 2.1: (a) A microscopic image of a microring modulator with 10 µm diameter; (b) Transmission spectra sequence with bias current ranging from 0 to 0.5 mA. The guard distance (GD) is 0, 0.2 µm, and 0.4 µm in our device designs.

dots represent measurement results, the black lines represent model results, and the inset shows the cross section of the microring waveguide. The microring modulator has a quality factor of 12,000 at zero injection, and achieves an on/off extinction ratio of 12 dB.

2.3 Device Design Space Model

In order to model the Q and ER of microrings in the device design space, we first model the dependence of Q and ER on coupling coefficient and optical loss in the microring, and then model the relationship between coupling coefficient and coupling gap. Here we define δ_1 as the through port coupling ratio, and δ_{2a} as the sum of ring cavity loss and drop port coupling ratio (both in terms of power):

$$\delta_1 = \kappa_t^2, \quad \delta_{2a} = \kappa_d^2 + \alpha L \tag{2.1}$$

Where κ_t (or κ_d) is through (or drop) port coupling coefficient in terms of field amplitude ratio; and αL is the round trip loss of optical power in the microring.

Bogaerts *et al.* presented equations for Q and ER of microring resonators in [57]. We simplify their expressions based on the approximation that both δ_1 and δ_{2a} are close to zero:

$$Q = \frac{2\pi\lambda_r}{FSR \cdot (\delta_1 + \delta_{2a})}, \quad ER = \left(\frac{\delta_1 + \delta_{2a}}{\delta_1 - \delta_{2a}}\right)^2 \tag{2.2}$$

In these expressions, FSR is the free spectral range of the microring spectrum. From the measured optical spectra of the microring resonator, we can extract Q and ER, and then δ_1 and δ_{2a}. By defining $\delta_c = \delta_1 + \delta_{2a}$, we have:

$$\delta_c = \frac{2\pi\lambda_r}{Q \cdot FSR} \tag{2.3}$$

When the microring is under-coupled:

$$\delta_1 = \frac{\delta_c}{2}(1 - \frac{1}{\sqrt{ER}}), \quad \delta_{2a} = \frac{\delta_c}{2}(1 + \frac{1}{\sqrt{ER}}) \tag{2.4}$$

And when the microring is over-coupled:

$$\delta_1 = \frac{\delta_c}{2}(1 + \frac{1}{\sqrt{ER}}), \quad \delta_{2a} = \frac{\delta_c}{2}(1 - \frac{1}{\sqrt{ER}}) \tag{2.5}$$

From Eqs. (2.4) and (2.5) we can see that the calculation of δ values depends on the coupling condition. Fortunately, we have 7×7 devices where the microring test structures were fabricated with different G_{thru} and G_{drop} as shown in Fig. 2.2. Some of the gap combinations lead to critical coupling indicated by high extinction ratios. Then we can identify under coupled devices with a larger G_{thru} and a smaller G_{drop} than the critical coupled devices, and vice versa (dot line and label in Fig. 2.2).

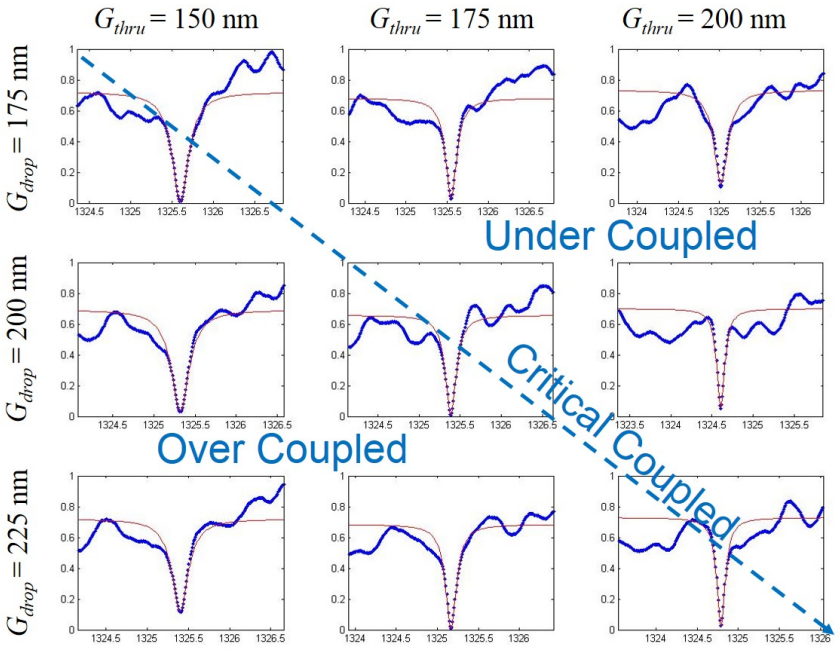


Figure 2.2: A subsection of design space of the microring resonators, with microring spectrum fitting, and the separation of critical, over, and under coupled conditions.

We first extract Q and ER from measured spectra of the microring resonators, and then extract δ values from Q and ER based on Eqs. (2.4) and (2.5). The extraction results in Fig. 2.3 show that δ_1 mainly depends on G_{thru}, and δ_{2a} mainly depends G_{drop}. These dependency trends are consistent with the definitions of δ_1 and δ_{2a}. The measured data of the microrings with $G_{thru} = 300$ nm is not included because of the weak coupling and unclear resonance dips.

Since there are some fluctuation errors in Fig. 2.3, we calculate the average δ_1 (or δ_{2a}) for different G_{drop} (or G_{thru}) and replot the data in Fig. 2.4. It can be seen that the values of δ_1 and δ_{2a} are close to zero, which confirms our previous approximation. Based on both the experimental data trend and theoretical analysis [22], we propose an exponential model for the two δ as shown in Eq. (2.6), where a, b, and c are fitting

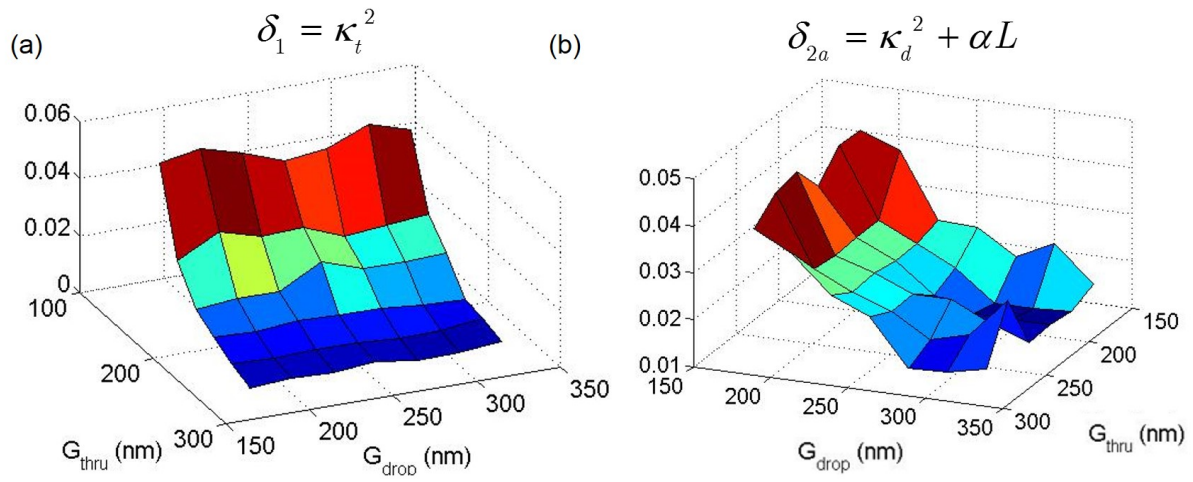


Figure 2.3: Extracted (a) δ_1 and (b) δ_{2a} from the measured Q and ER.

parameters. Fig. 2.4 shows that this exponential model can fit the measured data well.

$$\begin{aligned} \delta_1 &= a_1 \cdot \exp\left(-b_1 \cdot G_t\right) + c_1 \\ \delta_{2a} &= a_2 \cdot \exp\left(-b_2 \cdot G_d\right) + c_2 \end{aligned} \tag{2.6}$$

In summary, Eq. (2.6) can be used to calculate the coupling coefficients, and Eq. (2.2) to calculate the Q and ER. To validate our model, we compare the Q and ER values predicted by the model with the ones extracted from experiments, as shown in Fig. 2.5. The low relative errors indicate that our analytical model can accurately predict the Q and ER of the microring resonators. Also, this design space model is developed for passive microring structures, and therefore is valid to both microring-based modulators and filters.

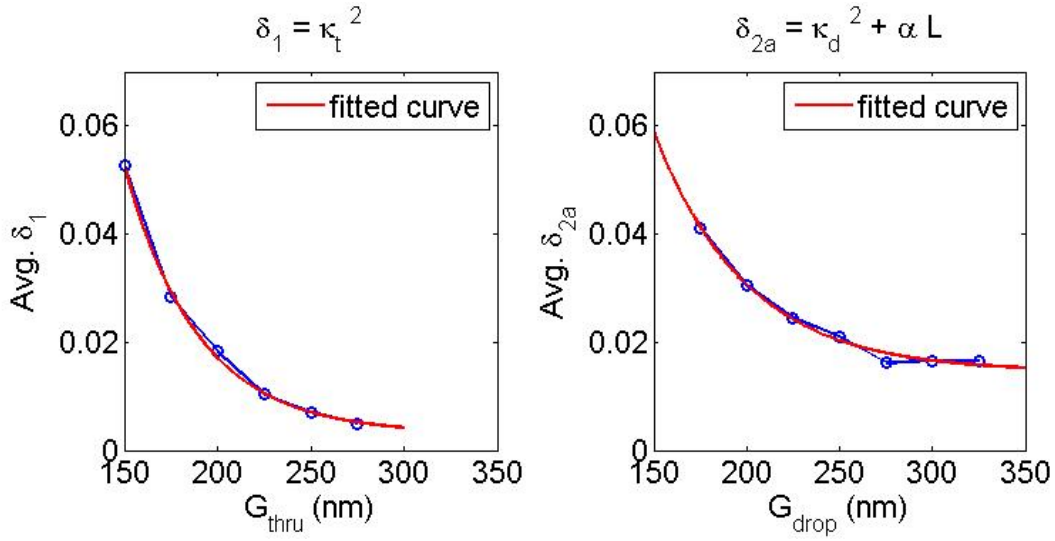


Figure 2.4: Average (a) δ_1 and (b) δ_{2a} with fitting results of coupling coefficient model, where circles are measured data, and red lines are fitting results.

2.4 Electro-Optic Modulation Model

The electro-optic modulation of microring resonators utilizes the plasma dispersion effect, in which the refractive index and optical loss of silicon are altered by changing the carrier concentration [12]. As the silicon index changes, the resonance wavelength shifts. Meanwhile, the quality factor and extinction ratio also change due to the increase of the optical loss. we derive theoretical models for the resonance wavelength, the extinction ratio, and the quality factor.

2.4.1 Resonance Wavelength Shift

The electro-optic (EO) effect changes the silicon refractive index, the mode effective index, and in turn the resonance wavelength. The relationship between the EO effect induced resonance wavelength shift $\Delta\lambda_r^{EO}$ and the carrier concentration change ΔN is given by:

$$\Delta\lambda_r^{EO} = -\frac{\lambda_r}{n_g}\Gamma n_f \Delta N \tag{2.7}$$

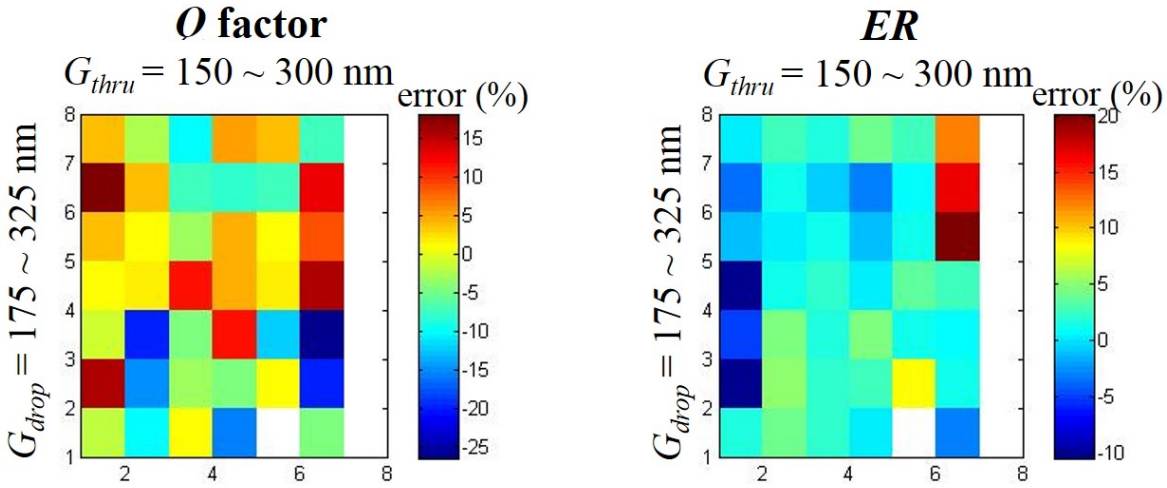


Figure 2.5: Model prediction relative error of the Q and ER, where ER is represented by $A = 1 - 1/ER$ to avoid the large ER values close to critical coupling. The 7×7 matrix represents the design variants of the microring modulator with different G_{thru} and G_{drop}.

where n_g is the group index of the optical mode; Γ is the mode confinement factor [58, 59]; $n_f \approx 2.13 \times 10^{-21}\text{cm}^3$ is the ratio between the change of silicon index and the change of carrier concentration when $\Delta N \sim 10^{18}\text{cm}^{-3}$ [47, 12, 22].

The steady state injected charge Q_{inj} in the p-i-n junction can be described by the following nonlinear equation [60]:

$$Q_{inj} = I\tau_c = I\frac{\tau_0}{1 + Q_{inj}/Q_0} \Rightarrow Q_{inj} = \frac{Q_0}{2}\left(\sqrt{1 + \frac{4I\tau_0}{Q_0}} - 1\right) \tag{2.8}$$

where τ_0 is the carrier lifetime at a low carrier density; Q_0 is a fitting parameter describing the dependence of carrier lifetime on the carrier density [60]. Considering the carrier concentration change $\Delta N = Q_{inj}/q\mathbb{V}$ where $\mathbb{V}$ is the junction volume, we can derive the lumped equation for the EO effect induced resonance wavelength shift:

$$\Delta\lambda_r^{EO} = -\frac{\lambda_r\Gamma}{n_g}n_f\frac{Q_0}{2q\mathbb{V}}\left(\sqrt{1 + \frac{4I\tau_0}{Q_0}} - 1\right) \triangleq -a \cdot (\sqrt{1 + I/I_0} - 1) \tag{2.9}$$

In a practical carrier-injection modulator, the thermo-optic (TO) effect caused by the self-heating of the injected current is non-negligible. The silicon index increases with the temperature:

$$\Delta n_{Si} = \frac{\mathrm{d}n_{Si}}{\mathrm{d}T} \cdot \Delta T \tag{2.10}$$

The temperature rise ΔT can be characterized as $\Delta T = \theta I^2 R$, where θ is the thermal impedance of the p-i-n junction. Therefore, the TO effect induced resonance wavelength shift is:

$$\Delta\lambda_r^{TO} = \frac{\lambda_r \Gamma}{n_g} \frac{\mathrm{d}n_{Si}}{\mathrm{d}T} \theta R \cdot I^2 \triangleq c \cdot I^2 \tag{2.11}$$

Consequently, the total resonance wavelength shift is given by:

$$\Delta\lambda_r^{total} = \Delta\lambda_r^{EO} + \Delta\lambda_r^{TO} = -a \cdot (\sqrt{1 + I/I_0} - 1) + c \cdot I^2 \tag{2.12}$$

The $\Delta\lambda_r$ model in Eq. (2.12) results in excellent fitting with the measured data from different device designs and fabrication batches, as shown in Fig. 2.6 and Fig. 2.7, where symbols represent measured data, and lines represent model fitting results. It should be noted that though the injection current in the testing experiments goes up to 3 or 4 mA, the actual bias of the device is usually limited in order to avoid the excess $I \cdot V$ power consumption and severe degradation of $\mathbb{Q}$ and ER. For comparison, the measured $\Delta\lambda_r$ is also fitted using the empirical polynomial model ($\Delta\lambda_r = -a \cdot I + b \cdot I^2$) in [61]. The fitting results demonstrate that the maximum fitting errors using our proposed model are only about 10% for Batch A and about 20% for Batch B of those using the polynomial model. Overall, our model provides a much better fitting accuracy than the polynomial model, since out model captures the nonlinear dependence of the EO effect on the injected current.

Our model can decompose $\Delta\lambda_r$ to electro-optic (EO) effect and thermo-optic (TO)

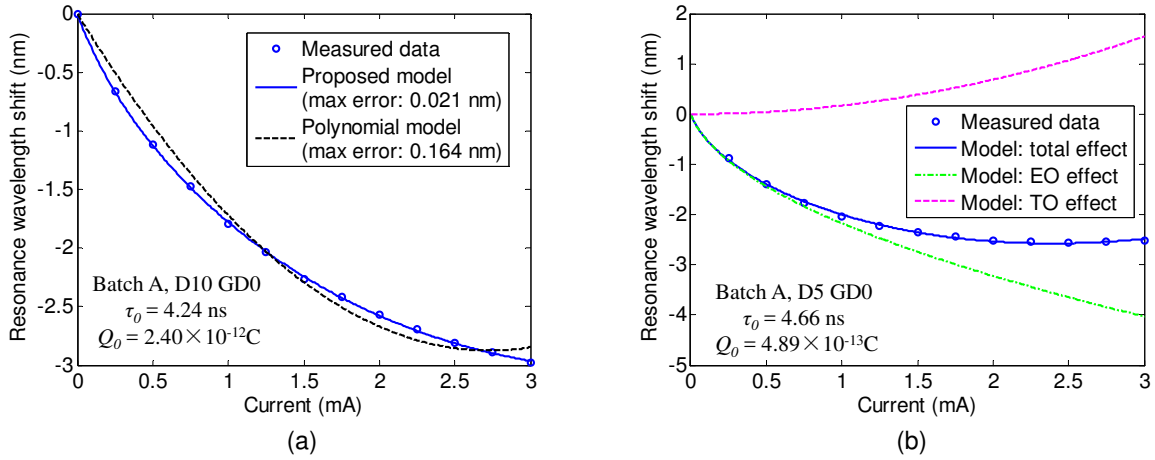


Figure 2.6: (a) Measured resonance wavelength shift with fitting results using our proposed model and empirical polynomial model; (b) Decomposition of wavelength shift to eletro-optic and thermo-optic effect.

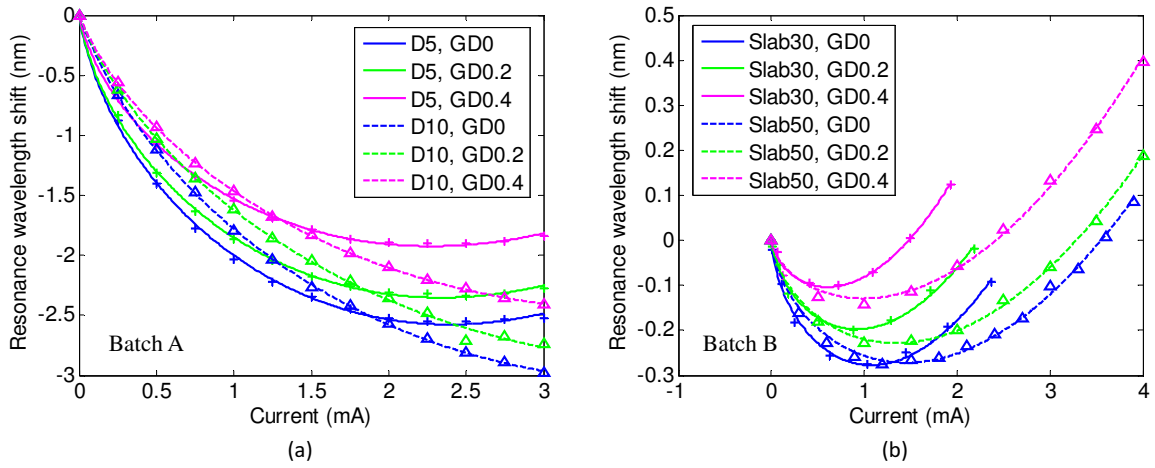


Figure 2.7: Resonance wavelength shift of modulators with model fitting: (a) Batch A with different diameters (D in µm) and guard distances (GD in µm); (b) Batch B with different slab heights (in nm) and GDs (in µm).

effect separately as shown in Fig. 2.6 (b). The EO and TO effect coefficients summarized in Fig. 2.8 have several implications on the device design parameters: (1) The modulators with a 5 µm diameter have a slightly smaller EO effect than that of 10 µm diameter in terms of the metric $a/\sqrt{I_0}$, while D5's TO effect (in terms of c) is about twice as that of D10. (2) For all devices, as the guard distance increases, the EO effect decreases while the TO effect fluctuates irregularly. (3) The devices with a 30 nm slab height have slightly greater EO effect and about two times TO effect than those of a 50 nm slab height. (4) By comparing the modulators with a 10 µm diameter and a 50 nm slab height from Batches A and B, one can see that Batch A's EO effect is much greater than that of Batch B, because the process error has been corrected in Batch A and the injection efficiency is greatly improved.

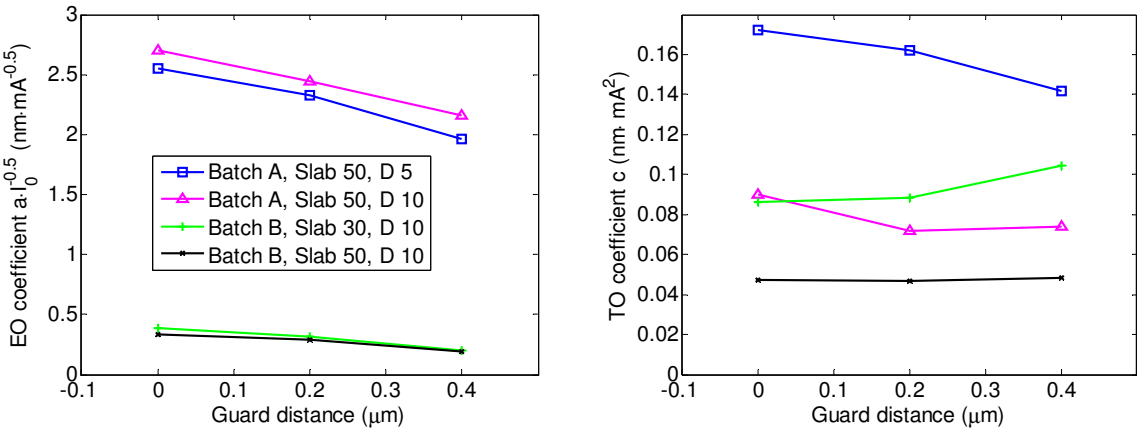


Figure 2.8: Fitting results of the resonance wavelength model for devices with different fabrications, diameters (D), and slab heights: (a) EO effect (metric: $a/\sqrt{I_0}$); (b) TO effect (metric: c).

2.4.2 Change of Extinction Ratio and Quality Factor

When carriers are injected into a microring modulator, ER and $\mathbb{Q}$ change since the optical loss within the microring increases. The dependence of ER and $\mathbb{Q}$ on the intra-

microring optical field loss coefficient α can be derived from Yariv's transmission relation in [62]:

$$T(\lambda) = 1 - \frac{(1-t^2)(1-e^{-2\alpha l})}{(1-te^{-\alpha l})^2 + (2t^{1/2}e^{-\alpha l/2}\sin(\pi n_{eff} l/\lambda))^2} \tag{2.13}$$

where t is the through-coupling coefficient that is related to the cross-coupling coefficient κ by $t^2 + \kappa^2 = 1$; l is the microring circumference. The transmission spectrum around a resonance wavelength ($\lambda_r = n_{eff} l/m$) can be approximated by:

$$T(\Delta\lambda) = 1 - \frac{A}{1 + (2\mathbb{Q} \cdot \Delta\lambda/\lambda_r)^2} \tag{2.14}$$

with

$$A = 1 - \left(\frac{t - e^{-\alpha l}}{1 - te^{-\alpha l}}\right)^2, \quad \mathbb{Q} = m\pi \frac{t^{1/2}e^{-\alpha l/2}}{1 - te^{-\alpha l}} \tag{2.15}$$

where A is related to ER by $ER = 1/(1-A)$. The loss coefficient α increases with the increase of the carrier concentration:

$$\alpha = \alpha_0 + n_a \Delta N = \alpha_0 + n_a \frac{Q_0}{2q\mathbb{V}} \left(\sqrt{1 + \frac{4I\tau_0}{Q_0}} - 1\right) \tag{2.16}$$

By incorporating Eq. (2.16) into Eq. (2.15), we can obtain the models for ER and $\mathbb{Q}$ as functions of the injected current I.

The effectiveness of the models is demonstrated by three devices with different coupling gaps on three coupling conditions as shown in Fig. 2.9, where the devices are from Batch B with a 5 µm diameter, a 0.4 µm guard distance, and a 50 nm slab height. In the over coupled case, the fitting parameter $t < \exp(-\alpha_0 l)$. As the injected current and thus optical loss increases, the $\exp(-\alpha l)$ decreases to be equal to t and then smaller than t. As a result, the ER (or A) first increases to reach infinity (or unity) from over coupled to critical coupled, and then decreases into the under coupled regime. Our model is consis-

tent with the non-monotonic change of ER. In the over coupled case, the relatively large discrepancy between the model and the measurement may be due to the abrupt change of ER around the critical coupled condition. In the critical coupled (or under coupled) case, our model shows both good fitting results as well as reasonable fitting parameters with t equals to (or greater than) $\exp(-\alpha_0 l)$.

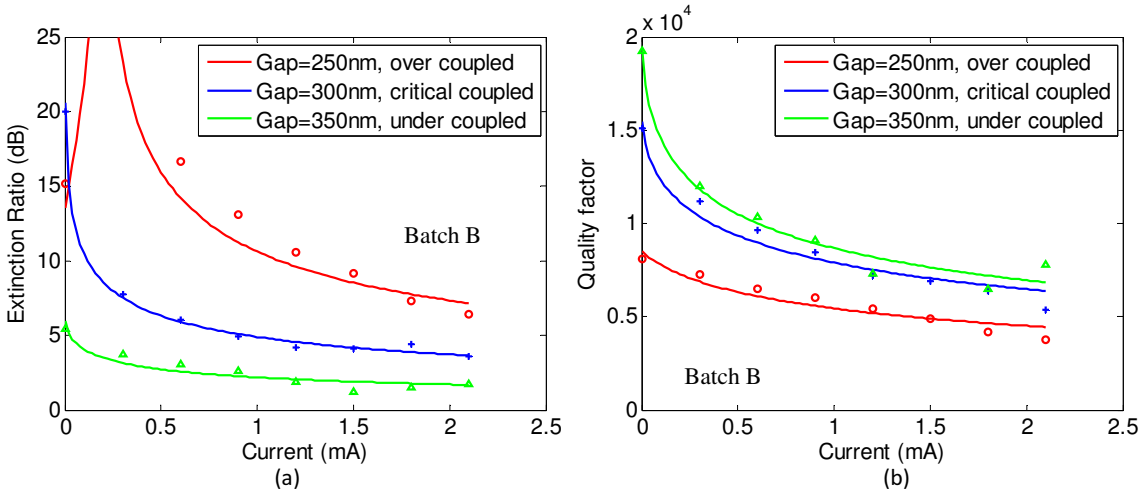


Figure 2.9: Measured data (circles) and model fitting results (lines) for (a) extinction ratio and (b) quality factor of devices with different coupling gaps and coupling cases.

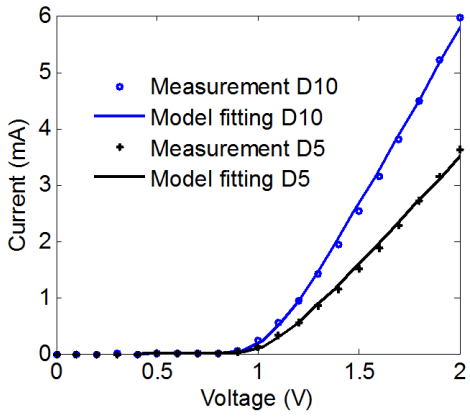
2.5 Electrical Model

2.5.1 DC Model

The governing equation describing the static I-V characteristics of the carrier-injection modulator is given by [60]:

$$I = I_S \exp\{q(V - IR - V_t)/(nkT)\} \tag{2.17}$$

where I_S is the reverse saturation current; R is the total series resistance including p/n doped region resistance, interconnect resistance and DC probe contact resistance during testing; n is the ideality factor. As illustrated in Fig. 2.10, the model shows that the devices with a diameter of 5 and 10 µm (denoted as D5 and D10) have similar V_t and n, while the resistance of D5 is almost twice of that of D10 because the microring circumference of D5 is half of that of D10.



(a)

Ring diameter (µm)	V_t (V)	R (Ω)	I_S (nA)	n
10	0.427	147.0	2.196	1.905
5	0.403	240.3	1.000	1.956

(b)

Figure 2.10: Measured and model fitted I-V curves of modulators with different diameters.

2.5.2 Small-Signal Circuit Model

In order to better understand the high speed performance of the carrier-injection modulator, we develop a small-signal circuit model with physical origins as shown in Fig. 2.11(a)(b). In the small-signal circuit, C_D and R_D respectively model the capacitance and resistance in the forward-biased p-i-n diode junction; C_{OX} denotes the capacitance through the cladding and buried SiO_2 layers; R_{s1} and R_{s2} model the resistances of doped silicon; C_p represents the capacitance between the electrodes. The small-signal circuit parameters are extracted by measuring and curve-fitting the S11 test data. The Fig. 2.11(c)(d) demonstrates the good curve-fitting results using the small-signal circuit

model.

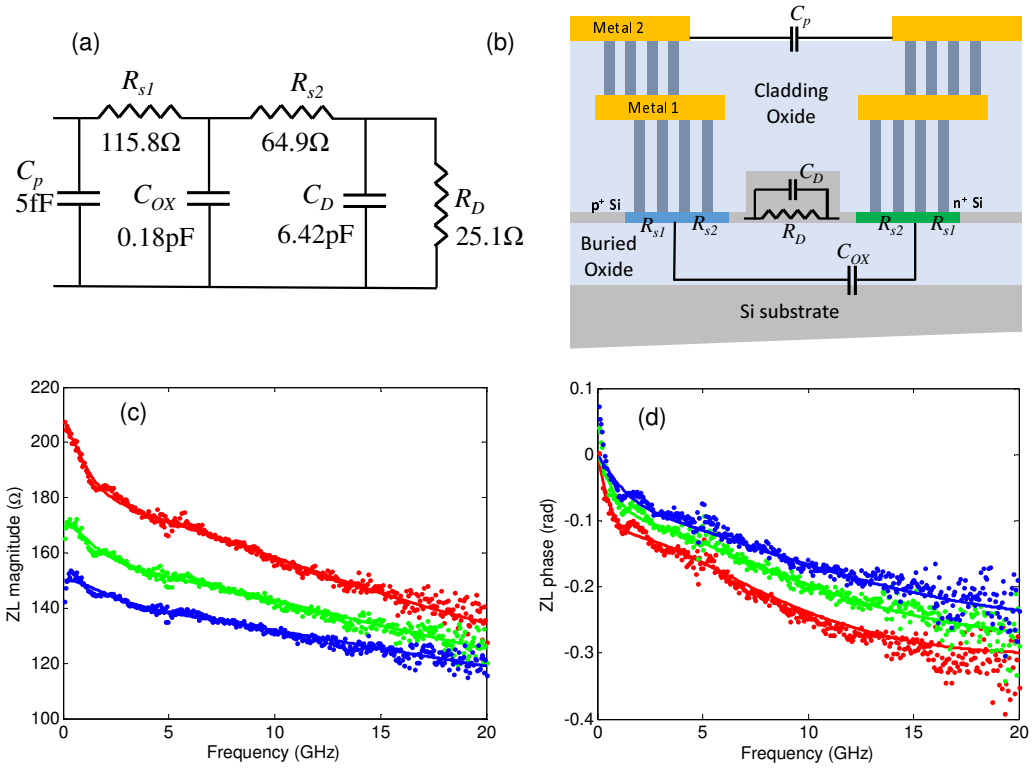


Figure 2.11: (a) The small-signal circuit model with circuit values at 1mA bias points; (b) The cross-section of the microring waveguide; (c)(d) Curve-fitting of the measured load impedance Z_L of the modulator with a 10 µm diameter. (bias points: red 1 mA, green 2 mA, blue 3 mA)

Using the small-signal circuit model, we estimate the RC-limited 3dB frequencies for devices with different diameters and injection levels (Fig. 2.12). The equation for the RC-limited 3dB frequency is $1/(2\pi((R_{s1}+R_{s2})//R_D)C_D)$, based on the approximation that both C_p and C_{OX} are much smaller than C_D. From Fig. 2.12, one can see that the RC-limited device bandwidth increases with the increasing of the injection level. The Fig. 2.12 also demonstrates that the device with a 5µm diameter has a higher RC-limited bandwidth than that of 10 µm. In Fig. 2.12, the minimum bias point is 0.1 mA instead of 0 mA because the p-i-n junction needs a positive bias to be turned on for small-signal modulation. The guard distance of the microring modulator is 0. It should be noted that

though the carrier-injection modulator inherently has a low electrical bandwidth limit, the optical modulation speed can be greatly improved by using pre-emphasis schemes [47, 48, 49, 50].

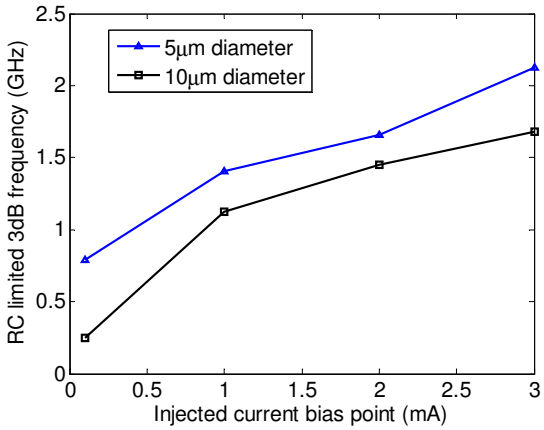


Figure 2.12: The RC limited 3dB frequency predicted by the small-signal circuit model for devices with diameter of 5 μm and 10 μm at different bias points.

2.6 Large-Signal Dynamic Model

In order to simulate the high speed behaviors of microring modulators, we develop a comprehensive large-signal model as illustrated in Fig. 2.13. The model framework includes the electrical model and the optical model. The large-signal electrical model is obtained by combining the electrical DC model and small-signal model, where R_S is the total series resistance, I_S is the reverse saturation current, n is the diode ideality factor, $V_T = kT/q$ is the thermal voltage, and C_D is the diffusion capacitance [63, 64]. In the DC situation, the large-signal electrical model is reduced to the typical exponential diode IV equation, which naturally fits our measurement data well. The output of the electrical model I_D (the current flowing through the intrinsic region of the diode) is then converted to resonance wavelength shift by $\Delta\lambda_r = -k_{mod} \cdot I_D$, where k_{mod} is the modulation efficiency (nm/mA).

In the optical model, the $\Delta\lambda_r$ is related to the optical transmission T. Lastly, the optical dynamics of the microring modulator are modeled as a low pass filter in a phenomenological approach, describing the cavity photon lifetime effect in the microring resonator. In the filter model, the cavity photon lifetime limited 3dB bandwidth can be calculated as $f_{\text{opt}} = c/(\lambda Q)$, where Q is the quality factor of the microring resonator.

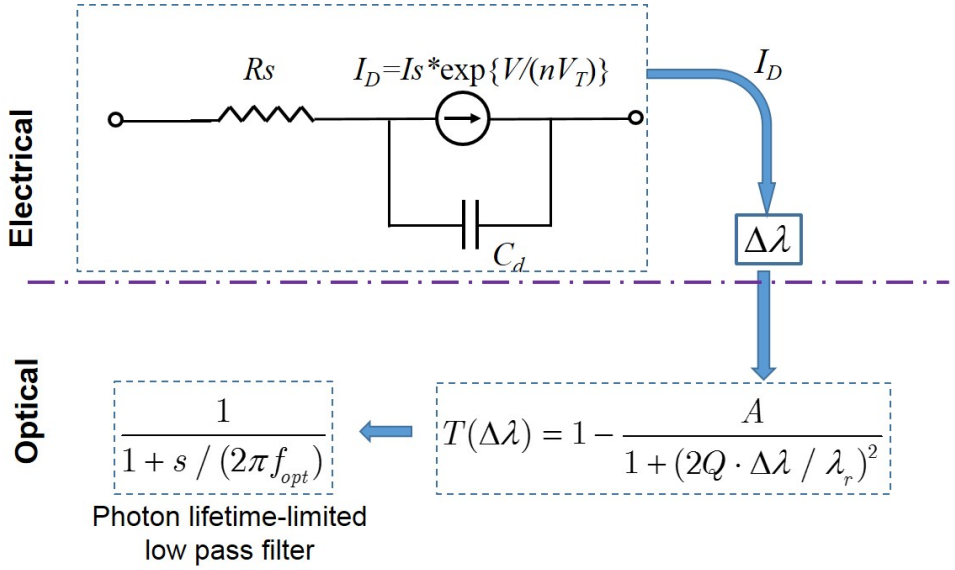


Figure 2.13: The large-signal model framework of the microring modulator.

In the large-signal model above, the parameters R_S, I_S, and n are extracted from static I-V test, the capacitance C_D is extracted from small-signal scattering parameter S11 test, and the parameters A (or ER) and Q are extracted from optical spectrum test.

Our model is validated by the comparison of eye diagrams simulated by the model and measured by our experiments. Our high-speed test setup ultilizes pre-emphasis driving scheme to boost the intrinsically low bandwidth of the carrier-injection microring modulator as shown in Fig. 2.14 (a). Meanwhile, we incorporate our large-signal model into Cadence simulation environment to simulate the optical eye diagrams 2.14 (b), where the optical power intensity is represented by the electrical voltage. The simulated eye diagrams agree well with the measured results for the microring modulators with 10 and

5 µm diameters (D10 and D5), as shown in Fig. 2.15. Both the measured and simulated eyes for D10 ring at 20 Gb/s and D5 ring at 25 Gb/s show that they are close to their bandwidth limits. The D5 ring is able to work at a higher data rate partly because it has lower quality factor and higher photon lifetime-limited bandwidth.

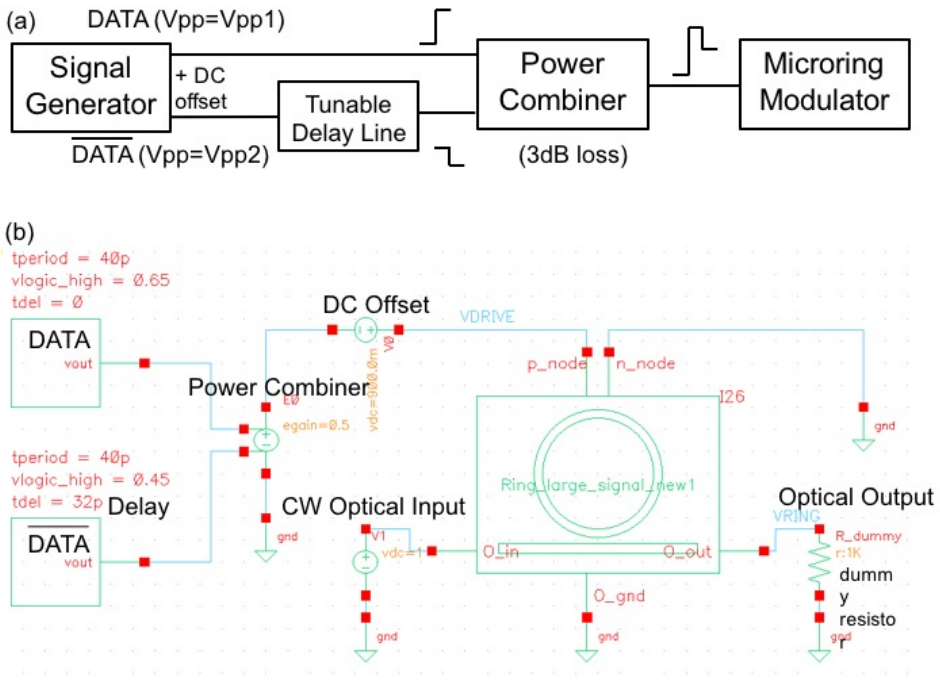


Figure 2.14: (a) The external pre-emphasized driving scheme synthesized by combining DATA and delayed $\overline{\text{DATA}}$. (b) The Cadence simulation schematic for the modulator with a pre-emphasized driving signal.

In order to further validate our model, we take measurement and compare the results with the simulated optical eyes of a D10 ring at 12.5 Gb/s with optimal and several sub-optimal driving conditions. The highest data rate is not chosen for model validation since the measured eyes at the highest data rate are noisy due to our present test setup noise. we first set the driving condition to the optimal (Vpp1=2V, Vpp2=1.5V, delay=30ps, DC offset=0.9V) as shown in Fig. 2.16 (b), and then deviate one parameter at a time. In Fig. 2.16, the simulated eyes are in good agreements with the measured results. For example, the overshoot phenomenon is well captured by our model when the offset is

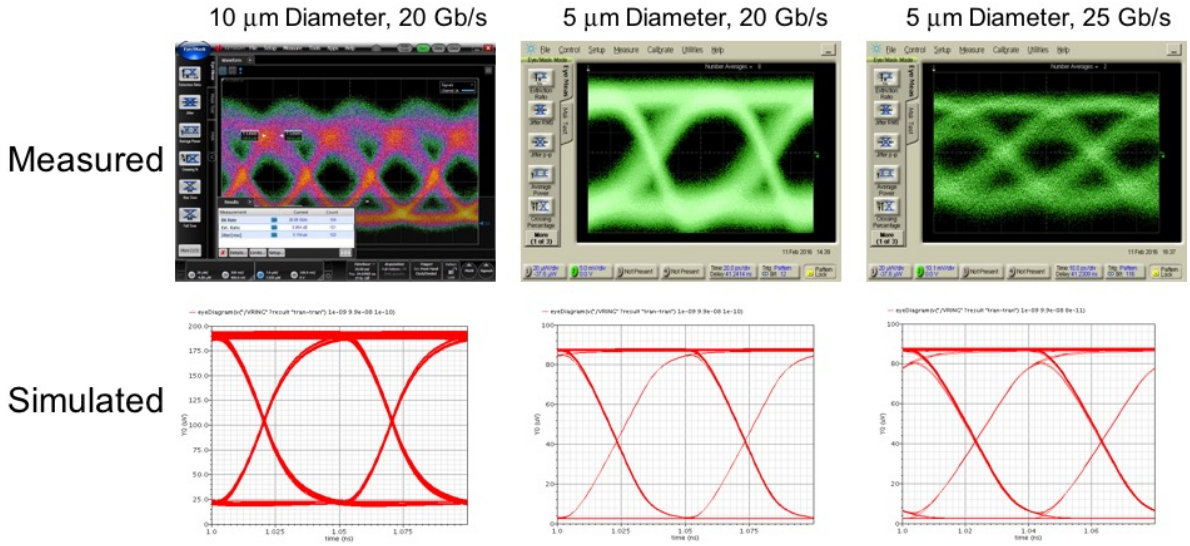


Figure 2.15: The experimentally measured and model simulated high-speed eye diagrams of microring modulators.

lower than optimal, or the Vpp2 is higher than optimal, or the delay is longer than optimal, as shown in Fig. 2.16 (a)(e)(g). Additionally, fast rising edges and slow falling edges are observed in both measured and simulated eyes in Fig. 2.16 (c)(d), which is also consistent with the discussions on extra falling edge delay in [47].

In summary, the measured eye diagrams at various data rates and driving conditions extensively validate our large-signal model.

2.7 Summary

In this chapter we have compactly modeled the silicon microring modulator in several aspects, including its design space, the spectra under electrical bias, its electrical characteristics, and its large-signal dynamic behavior. The design space model for microring resonators quantifies the Q and ER w.r.t. various through port and drop port gaps. The electro-optical (EO) modulation model accurately describes the spectra under bias voltage. The large-signal model framework combines the large-signal circuit model and the

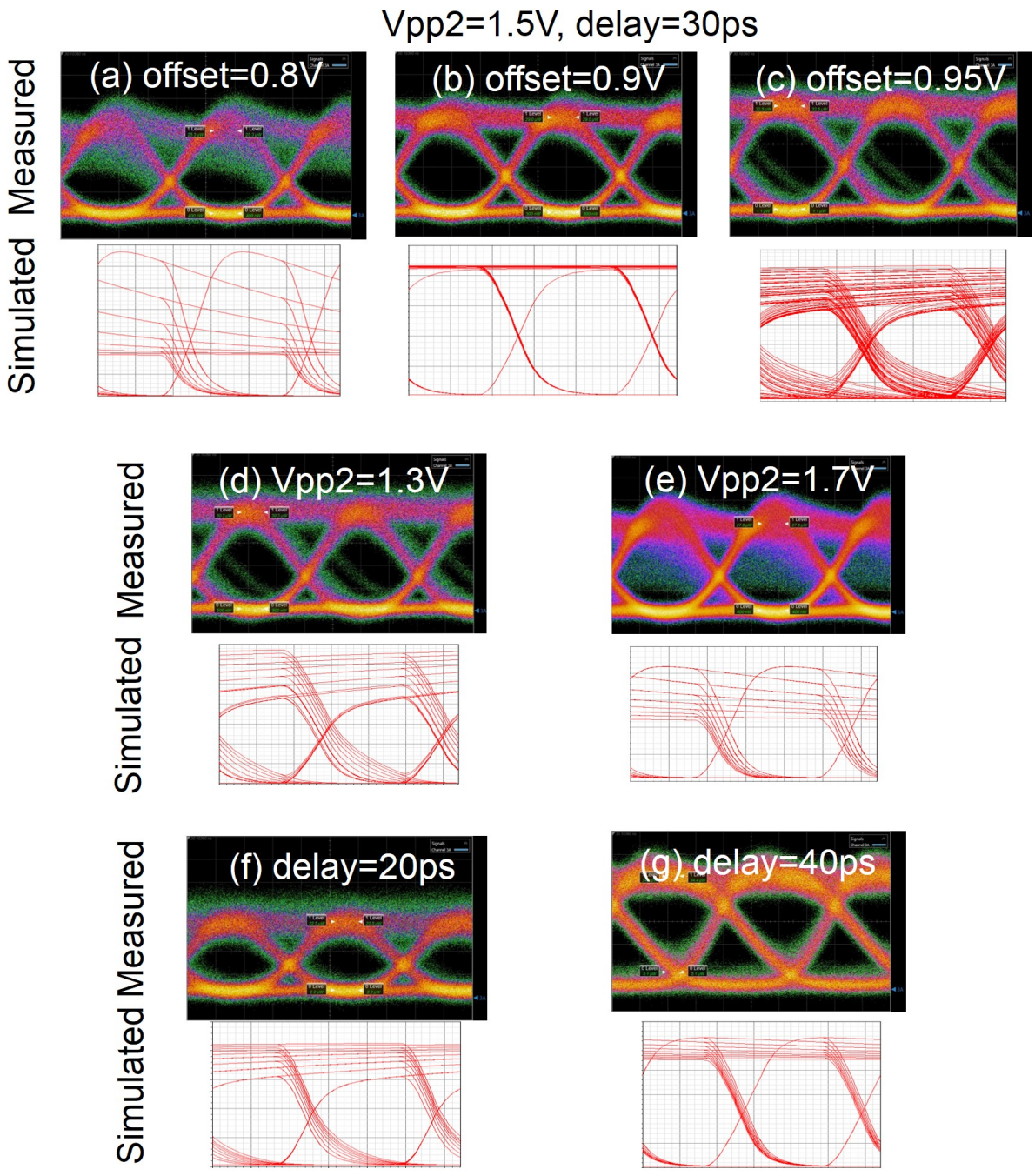


Figure 2.16: Measured and simulated eye diagrams with optimal and several sub-optimal driving conditions

EO modulation model, and is able to simulate the modulation eye diagrams. This model stack could be used together to comprehensively describe DC and AC, electrical and optical performance of the microring modulators, and to study the design parameters' impact on device performance.

Chapter 3

Compact Models for Other Common Silicon Photonic Devices

In this chapter, we study a heterogeneous silicon photonic NoC including high speed modulators and photodetectors. Several key components in the NoC are compactly modeled, including their optical and electrical properties. The models can fit the measurement data well, paving the way to a photonic PDK model library.

3.1 Introduction

Among the common integrated photonics technology platforms, the heterogeneous III-V/silicon platform can both enable laser integration and enjoy the CMOS compatibility by bonding III-V material epitaxial layers on silicon-on-insulator (SOI) wafers [15]. Integrating lasers on silicon is challenging due to silicon's indirect bandgap, but is very critical in making robust, energy efficient, and scalable interconnect systems [65]. To address this challenge, our target optical network-on-chip (ONoC) was fabricated on the heterogeneous silicon platform, which fully integrated lasers, high-speed modulators and

detectors, and other photonic components on a single chip and successfully demonstrated a total bandwidth of 2.56 Tb/s (40 Gb/s/channel $\times$ 8 wavelength-division multiplexing channels $\times$ 8 transceiver nodes).

To date, photonic designers are still heavily replying on empirical schematic design, manual mask layout, and manual design rule checking (DRC). The fast growing complexity of photonic integrated circuits (PICs) drives the need for photonics design automation tools, including trustworthy photonic circuit level models and simulators, photonics property-aware automatic floor planning [17], layout and routing [18], and DRC and logic vs. schematic (LVS) [19]. A number of system- and link- level studies for optical interconnects have been reported [66, 67, 68, 69], but due to the analog nature of photonics, it is imperative to perform accurate circuit-level (or equivalently SPICE-level) modeling and simulation of nanophotonic interconnects. Circuit-level compact models of a variety of photonic devices have been reported, e.g., carrier-injection [64, 63] and carrier-depletion [31] based silicon microring modulator, Mach-Zehnder modulator [30], etc. However, there is a lack of effort for integrating such models to enable simulation, validation, and optimization of a full optical link.

In this chapter, we develop accurate circuit-level models for the photonic devices in the heterogeneous ONoC. These models are implemented in Verilog-A so that the optical interconnects can be simulated in a SPICE environment. The photonic device models are extensively validated in several aspects using the measurement data from our implemented ONoC.

3.2 Overview of the ONoC

Our ONoC includes eight WDM transceiver nodes all connecting to a circular bus waveguide through eight broadband optical switches as shown in Fig. 3.1 [70]. Each

WDM transmitter (Tx) has eight wavelength channels. In each channel, a single wavelength distributed feedback (DFB) laser emits the light at the channel wavelength [1]. The light is then externally modulated by an electroabsorption modulator (EAM) [71]. The EAM has the advantages of wide wavelength and temperature operation range, and large bandwidth compared to silicon microring modulators [71]. The optical signals in the eight wavelength channels are multiplexed into a Tx bus waveguide by a silicon arrayed waveguide grating (AWG).

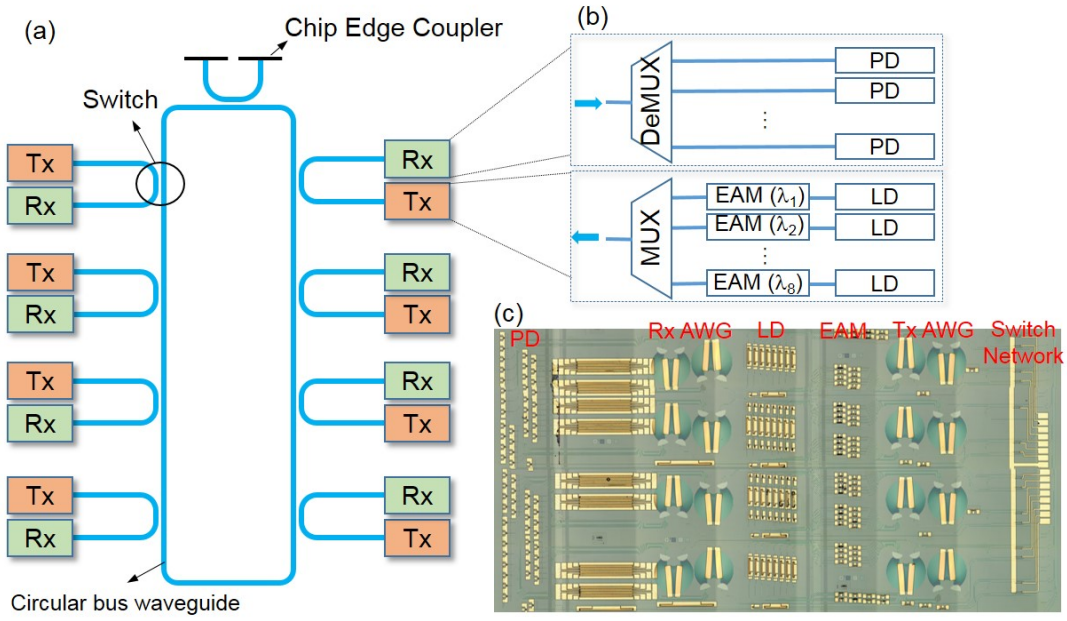


Figure 3.1: (a)(b) Our ONoC architecture with a zoom-in of a transmitter (Tx) and a receiver (Rx), where LD: laser diode, EAM: electroabsorption modulator, PD: photodetector, $\lambda_{1\sim8}$: channel wavelengths; (c) The microscopic image of the fabricated ONoC including 8 transceiver nodes.

The Tx bus waveguide is connected to the receiver (Rx) bus waveguide and the circular bus waveguide by a broadband switch, which is implemented by a silicon Mach-Zehnder interferometer (MZI) with two 3-dB adiabatic couplers. The switch's connectivity can be configured by tuning the TiPt local heater. In this way, a Tx can transmit data either to the local Rx at the same node, to an Rx at a different node, or to the edge

coupler for off-chip communication. At the receiver side, light is demultiplexed by an AWG into eight channels, and then sensed by InGaAs/silicon photodetectors (PD) [72].

3.3 Device Modeling and Parameter Extraction

This section describes the compact behavior models for the photonic devices in our ONoC. The compact models are implemented in SPICE-compatible Verilog-A, where the optical power is described by the potential between an optical signal line and a dummy optical ground. Model parameters are extracted from measurements including scattering parameter S11 test, IV test, and optical test. We then successfully validate the models by comparing the model simulated data (e.g., optical power, frequency response, etc.) with the measurement data.

3.3.1 Laser

Diode lasers utilize carrier injection in a p-i-n junction to provide stimulated emission and optical gain. A diode laser can be used for either continuous wave (CW, or static) operation with an external modulator or direct modulation, where the former mode is used in this work. The output light power vs. driving current (LI) of a diode laser can be expressed by (3.1) [73].

$$P = \eta_d \frac{h\nu}{q}(I - I_{th}) \tag{3.1}$$

The two performance parameters in the LI model are the threshold current I_{th} and differential quantum efficiency η_d. The DC electrical characteristics of the diode laser follows the Shockley diode equation as shown in (2).

$$I = I_0 \exp \frac{q(V - IR)}{nkT} \tag{3.2}$$

Where R is the series resistance, n is the emission factor, I_0 is the saturation current, k is the Boltzmann constant, and T is the temperature.

Model Validation: The optical and electrical models of diode lasers are implemented in Verilog-A and simulated in SPICE. Fig. 3.2 shows the simulated and measured LI and IV curves, which have good agreements. With these two models, designers can accurately determine the driving voltage and power of the laser based on the optical link's power budget.

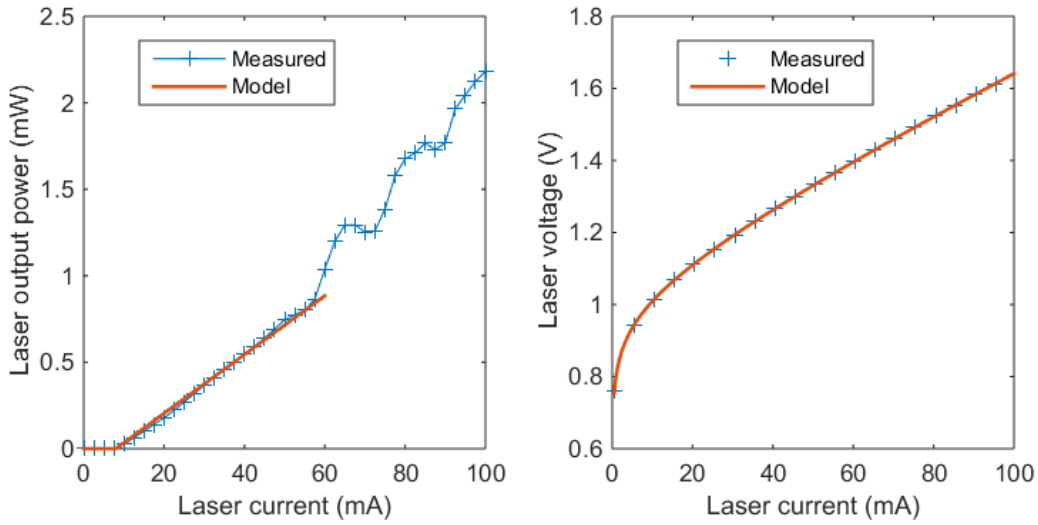


Figure 3.2: Measured and model simulated single facet light-current (LI) and voltage-current (IV) curves of the DFB laser.

3.3.2 Waveguide

Single mode silicon waveguides are widely used to guide the light on chip due to its low loss. We use (3.3) to model the loss along the waveguide with a length L.

$$P_{out} = P_{in} \cdot 10^{-\alpha L/10} \tag{3.3}$$

Where α is the waveguide loss per length in dB/cm, which is estimated to be 1 dB/cm in this work.

3.3.3 Electroabsorption Modulator (EAM)

EMAs utilize a reverse biased p-i-n junction to apply electrical field and to modulate the optical absorption coefficient [73]. We find that the dependency of the EAM optical transmission on the bias voltage can be described by the logistic equation in (3.4).

$$T_{opt}(V_j) = IL \cdot (\frac{1-b}{1+\exp(-k(V_j - V_0))} + b) \tag{3.4}$$

Where V_j is the voltage on the p-i-n junction, IL is the insertion loss, V_0 is the transition voltage, b is the residual optical transmission at a strong bias voltage. Fig. 3.3 (a) shows that our proposed model in (4) matches the measurement data well.

By applying a DC bias around V_0 and an AC modulation driving signal, the EAM can perform on-off keying (OOK) modulation of the optical signal.

The electrical characteristics of the EAM can be described by an equivalent circuit model as shown in Fig. 3.3 (b), where R_{sm} is the device series resistance, C_{im} is the junction capacitance, V_j is the junction voltage that determines the optical absorption and transmission in (3.4), and I_p is the photocurrent generated by the absorbed optical power and fed back into the electrical circuit [74]. Fig. 3.3(c) shows the IV curve of the photocurrent element, which can be equivalent to a resistance of multi kilo-Ohm. The photocurrent element has trivial influence on the EAM's scattering parameters S11 and S21, since the R_{sm} is in the order of 10 Ω.

The values of C_{im} and R_{sm} are extracted from the scattering parameter S11 data measured by a lightwave component analyzer (LCA). The measured S11 is first converted to the device or load impedance (Z_L), as shown in Fig. 3.4. Then it is observed that the

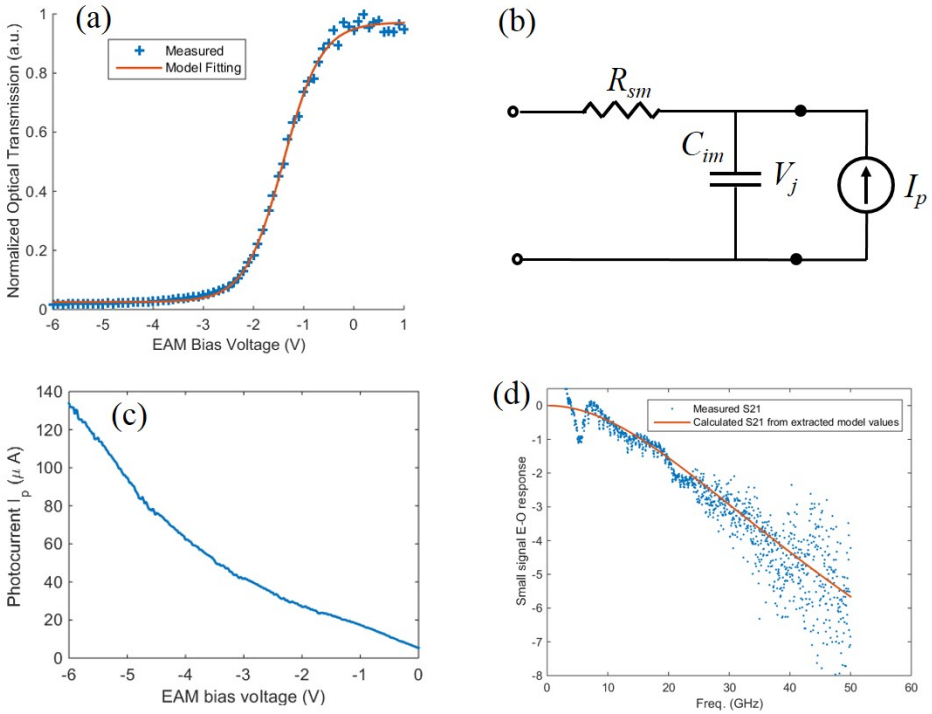


Figure 3.3: EAM: (a) Measured and model fitted optical transmission at 1550 nm wavelength; (b) Equivalent circuit model; (c) Measurement photocurrent generated by the absorbed optical power (input optical power = 316 μW); (d) Directly measured and model calculated small-signal E-O (electrical-to-optical) responses.

imaginary part of the device impedance is inversely proportional to the frequency, from which the C_{im} value is extracted. Meanwhile, the R_{sm} can be estimated from the Z_L real part at high frequency. Based on the extracted C_{im} and R_{sm} values, we in return calculate the S11, which is in good agreement with the directly measured S11 data as shown in Fig. 3.4. This agreement is one of the key evidences of the validity of our EAM circuit model.

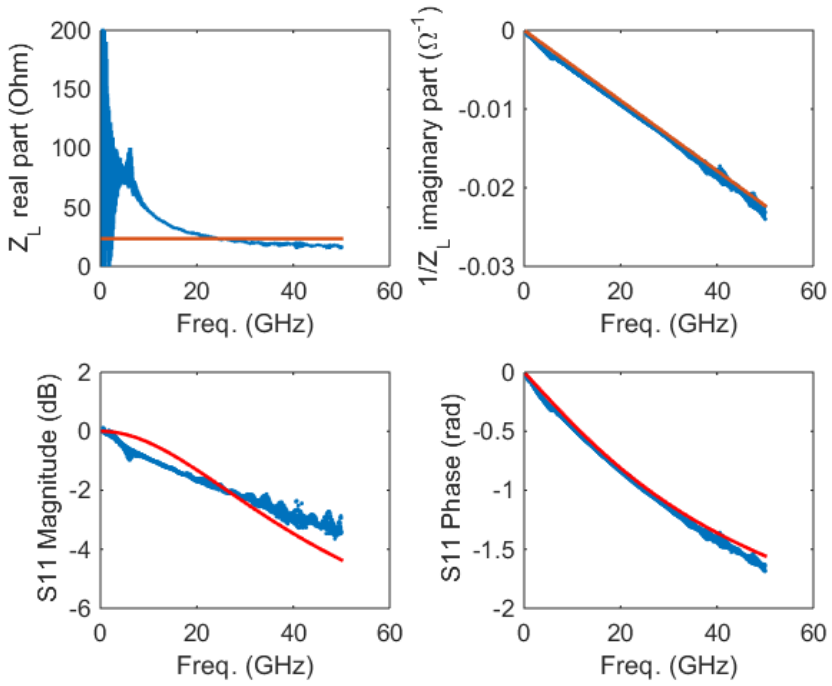


Figure 3.4: S11 and device impedance data of the EAM, where blue dots represent measurement data and red lines show model results.

Model Validation: An EAM's total bandwidth is subject to both RC limit and carrier transit time limit. However, the EAM in this work has a thin intrinsic region and a small carrier transit time. Therefore, the EAM here is only subject to RC limit, and we can use the extracted R_{sm} and C_{im} values to predict the EAM's frequency response. Fig. 3.3 (d) shows that our model predicted electrical-to-optical frequency response matches well with the directly measured S21 data, which is another piece of evidence for the validity

of our model. The measurement setup has a 50 Ω configuration.

3.3.4 Multiplexer and Demultiplexer

The structure of the multiplexer and demultiplexer in our design is an AWG, which utilizes phased-array to multiplex or demultiplex the light at a series of wavelengths with certain channel spacing [75]. A typical AWG spectrum is shown in Fig. 3.5, where eight colors represent eight channels. Each channel of the AWG functions as a bandpass filter, and can route the optical signal at its center wavelength in or out of the bus waveguide.

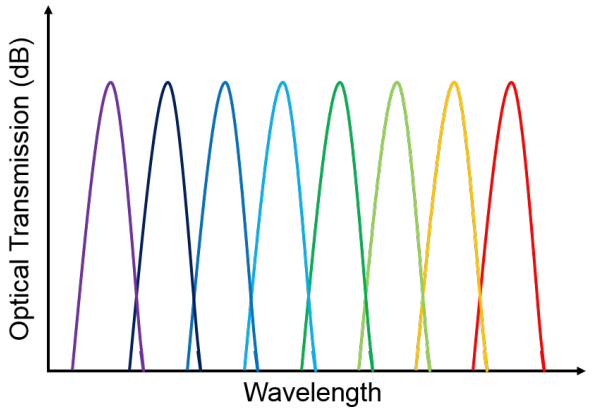


Figure 3.5: A typical optical spectrum of AWG.

The AWG will reduce the amplitude of the high speed optical signal due to its spectral filtering effect [76]. In order to illustrate the spectral filtering effect, we plot the optical spectrum of a commercial bandpass filter (BPF) in Fig. 3.6 (a), where f_c is the central carrier frequency, and f_m is the modulation frequency. By modulating the optical carrier wave using a sine wave, two sidebands located at $f_c \pm f_m$ appear, which will be suppressed by the slope of the filter's optical spectrum. The small signal optical-to-optical (O-O) response of the filter can be calculated as $T(f_c + f_m)/T(f_c)$, where $T(f)$ is the optical power transmission at frequency f. Fig. 3.6 (b) shows that our calculated frequency response using this approach agrees well with the directly measured frequency response

using an LCA.

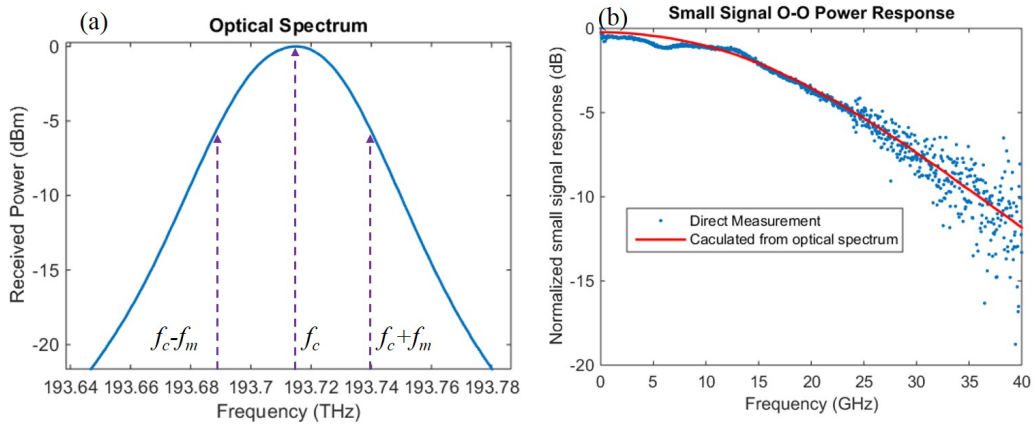


Figure 3.6: (a) Measured optical spectrum of a commercial bandpass filter (BPF); (b) Measured and calculated small signal responses of the BPF.

During our experiments we observed that the small signal response of the AWG cannot be directly measured by LCA due to large edge coupling loss. Therefore, we calculate the AWG's O-O small signal response based on the optical spectrum that can be easily measured using the aforementioned approach, as shown in Fig. 3.7. Because the measured AWG spectrum is asymmetric, the average of the spectrum's left-side slope and right-side slope is used to calculate the small signal response. The AWG's small signal response can be well approximated by a two-pole low-pass filter (LPF) as described in (3.5) up to 45 GHz.

$$H(f) = \frac{1}{(1 + j \cdot f/f_{LPF})^2} \tag{3.5}$$

Based on this approximation, we implement the AWG's dynamic model in Verilog-A using integral operators. The AWG Verilog-A model also includes the insertion loss effect, which is 1.5 dB in our experiments when the channel center wavelength is well aligned with the laser wavelength. Our AWG model does not include multi-channel wavelength information, since our focus is on modeling and simulating the dynamic characteristics of the device and the link at one channel wavelength. However, extension to considering

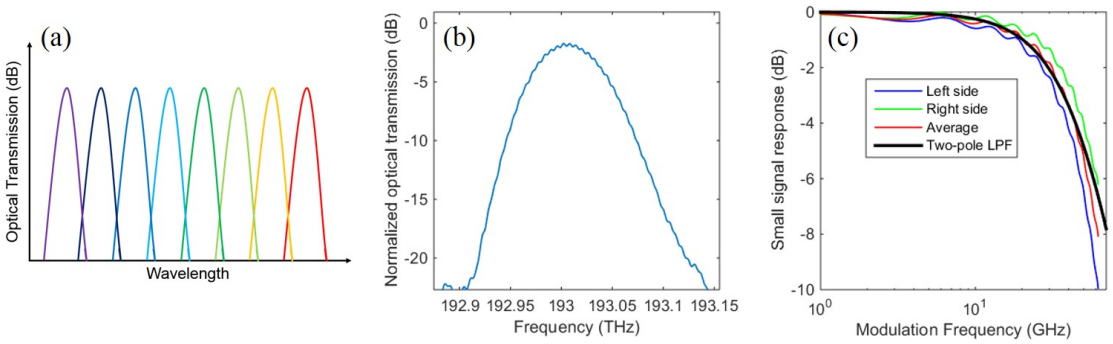


Figure 3.7: (a) Measured single channel optical spectrum of the AWG; (b) The calculated frequency response using AWG's optical spectrum, with an approximation by a low pass filter (black line).

multi-channel wavelengths should be quite straightforward.

3.3.5 Photodetector

The PD studied in this work is made of reverse-biased p-i-n junction, which generates photocurrent when there is light input. The PD's responsivity R_{sp} is defined as the photocurrent over input optical power. The electrical characteristics of the PD can be modeled by an equivalent circuit as illustrated in Fig. 3.8 (a), where the current source represents the photocurrent generated by the input light with power P_O and the dark current I_{dark}, C_D is the diode capacitance under reverse bias, and R_s is the series resistance. The values of C_D and R_s can be extracted in a similar approach as the EAM. Fig. 3.9 shows how the C_D and R_s are extracted from Z_L real part and imaginary part respectively, and that the calculated S11 agrees well with the measured data which validates our model.

Model Validation: Similar to the EAM, the PD in this study is also only subject to the RC limit since its intrinsic region is thin (400 nm). So we can calculate the PD's frequency response using the extracted R_s and C_D values. Fig. 3.8 (b) shows that the predicted frequency response agrees well with the measured O-E S21 frequency response,

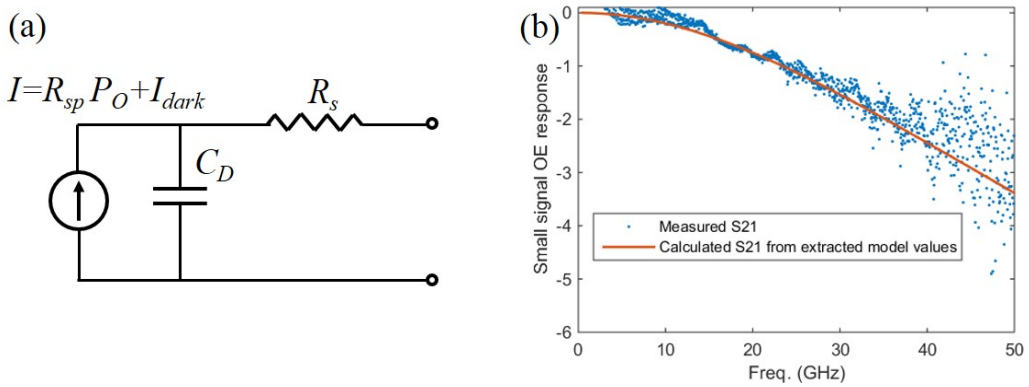


Figure 3.8: (a) PD's equivalent circuit model; (b) Directly measured and model calculated small-signal O-E (optical-to-electrical) responses of the PD at -3V bias.

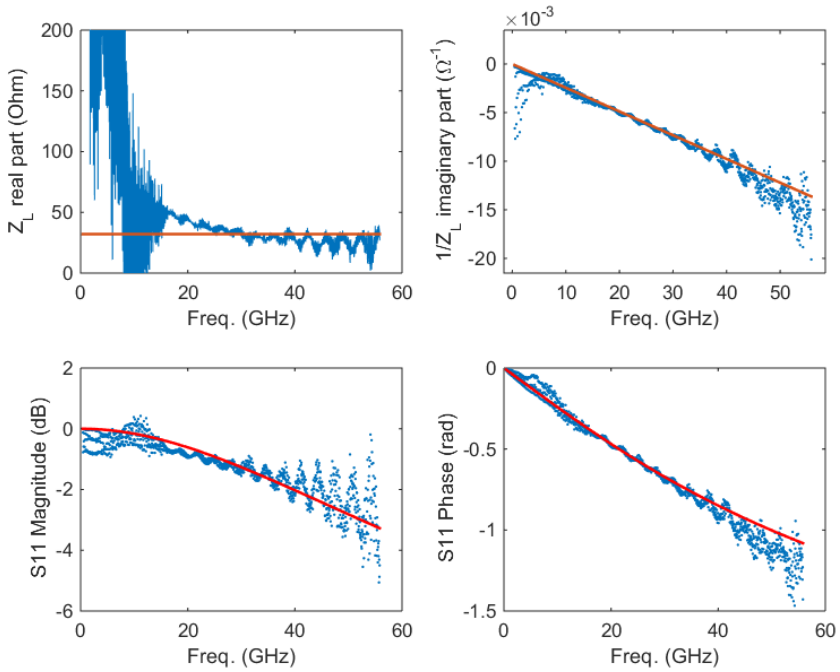


Figure 3.9: S11 and device impedance data of the PD at -3V bias, where blue dots represent measurement data and red lines show model results.

which is a strong piece of evidence of the validity of our PD model. The measurement setup has a 50 Ω configuration.

3.4 Summary

In this study, we develop accurate circuit-level models for silicon photonic devices based on their electrical and optical properties. Our models have been successfully validated in multiple aspects based on the measurement data of the fabricated photonic devices. These models are implemented in Verilog-A, and thus are compatible with all SPICE simulators. This work paves the way to a photonics PDK and link-level simulation and design space explorations of various types of optical links.

Chapter 4

Circuit-Level Simulations and Design Space Explorations of Nanophotonic Interconnects

Based on the well established models in the previous two chapters, we perform Cadence simulations and design space explorations (DSE) of two optical links. The simulated results agree well with measurement data. The DSEs demonstrate our capability of including photonics device design into the electro-optical co-simulations.

4.1 Introduction

State-of-art PIC has becoming more and more complex, and has been working closely with electronic circuits. It is imperative to efficiently and accurately simulate the behavior of PICs and their interactions with interface circuits. In this chapter, we simulate two optical communication links by incorporating the well established compact models for photonic devices. The simulation results are verified by the link measurement data. Our

models and simulation approach enable the electro-optical (EO) co-design and optimization of the photonic devices with electronic interface circuits that have been designed separately in the past. Additionally, the enrichment of photonic device library paves the way to a process design kit (PDK) for silicon photonics, and an EDA-style design process for PICs and electro-optical systems.

4.2 Optical Transceiver based on Silicon Microring Resonators

We simulate the transceiver in Fig. 4.1 (a) in Cadence as illustrated in Fig. 4.2 which reproduces our transceiver test setup. In the schematic, the comprehensive model of microring modulator combines the design space model and the dynamic behavior model. Similar to the microring modulator, the microring filter model first calculates Q and ER based on the design space model, and then use a low pass filter to capture the photon lifetime effect. The photodetector (PD) model mainly consists a diode capacitance and a series resistance [77]. The CW laser model simply provides the function of outputting a given optical power at a certain wavelength.

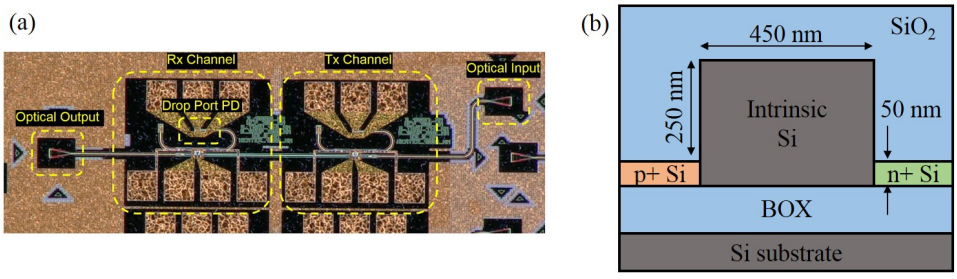


Figure 4.1: (a) Microscopic image of our back-to-back optical transceiver; (b) Cross section view of the microring waveguide.

During the transceiver measurements, the tunable laser is aligned to the resonance wavelength of the Tx microring modulator. The modulator is driven by an external pre-

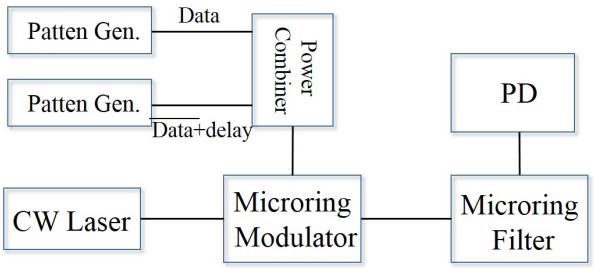


Figure 4.2: Cadence simulation schematic for the back-to-back optical transceiver.

emphasized driver (Fig. 2.14). Firstly, the modulated optical signal passes through the Rx and is received by a digital communication analyzer (DCA) as shown by the yellow eye diagrams in Fig. 4.3. Secondly, the Rx microring filter is thermally tuned to be aligned with the Tx microring so that the optical signal is routed to the on-chip drop port PD. The electrical signal from the on-chip PD is observed on the DCA (the green eye diagrams in Fig. 4.3). It can be seen that the electrical eye diagrams are more distorted than the optical ones due to the limited Rx microring bandwidth. The simulated eye diagrams well captures this phenomenon, as well as the eye closing trend toward high data rates. The good agreement between measurement and simulation again validates our model.

We also study the effect of device geometry (drop port gap) on the link performance, because we have integrated the design space model with the dynamic model of the microring modulator. In the three simulations, the G_{drop} of the microring modulator is swept from 175 nm to 275 nm, while other device geometries and driving conditions are the same (G_{thru} = 200 nm, data rate = 20 Gb/s). The resulting eye diagrams are shown in Fig. 4.4, where three different G_{drop} result in three coupling conditions. The under-coupled case has a small optical modulation amplitude (OMA) due to the small extinction ratio. The over-coupled case has a similar OMA as the critical-coupled case. This is because the G_{drop} is fairly large, the drop port coupling is weak, and the over-

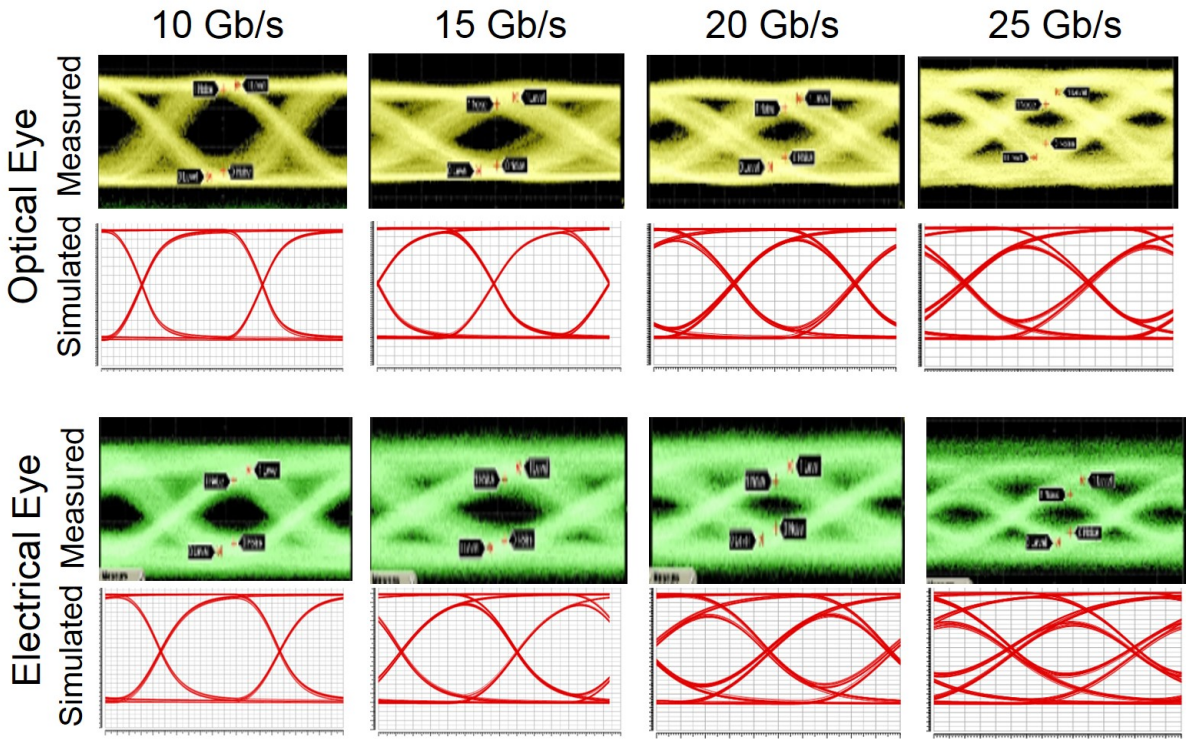


Figure 4.3: Measured and simulated optical and electrical eye diagrams of the back–to-back transceiver.

coupled case does not significantly deviate from the critical coupling condition. Fig. 4.4 also shows a trend that the link's bandwidth decreases as the G_{drop} increases. This is because a large G_{drop} leads to a small δ_{2a} and a high Q based on Eqs. (2.6) and (2.2), respectively. A microring with a high Q would have a low photo lifetime-limited bandwidth. The consistency between simulations and theory again supports the validity of our model.

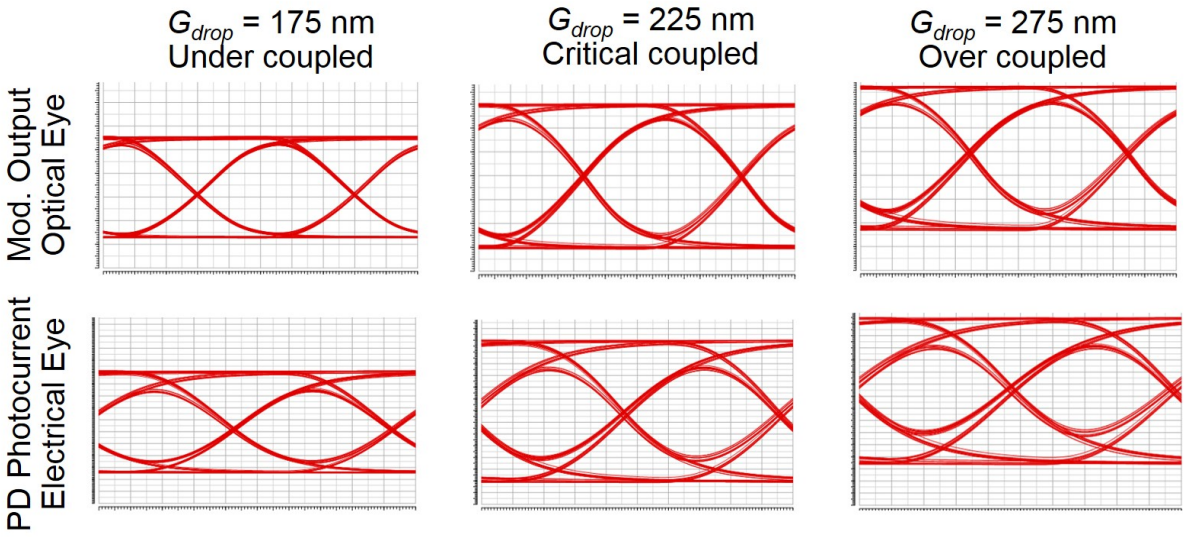


Figure 4.4: Simulated 20 Gb/s optical and electrical eye diagrams of the optical transceiver with respect to microring modulators with different G_{drop}.

4.3 Optical NoC on III-V/Silicon Heterogeneous Platform

We simulate an end-to-end single channel transceiver link in the heterogeneous optical NoC (Fig. 3.1) in Cadence Virtuoso. Fig. 4.5 shows the simulation schematic that reproduces the measurement setup. The measurement setup has a 50 Ω configuration (i.e., all testing equipment, RF cables and probes are 50 Ω matched), so in the simulation

schematic two 50 Ω resistances are added at the EAM driver and the PD receiver, respectively. The EAM is driven by a random bit sequence source swinging between -1∼-2 V, and the PD is biased at -3 V. The broadband switch model simply describes its insertion loss effect, since our switch has a wide wavelength operation range (1550∼1570 nm) and will not impose a bandwidth limitation to the link [70].

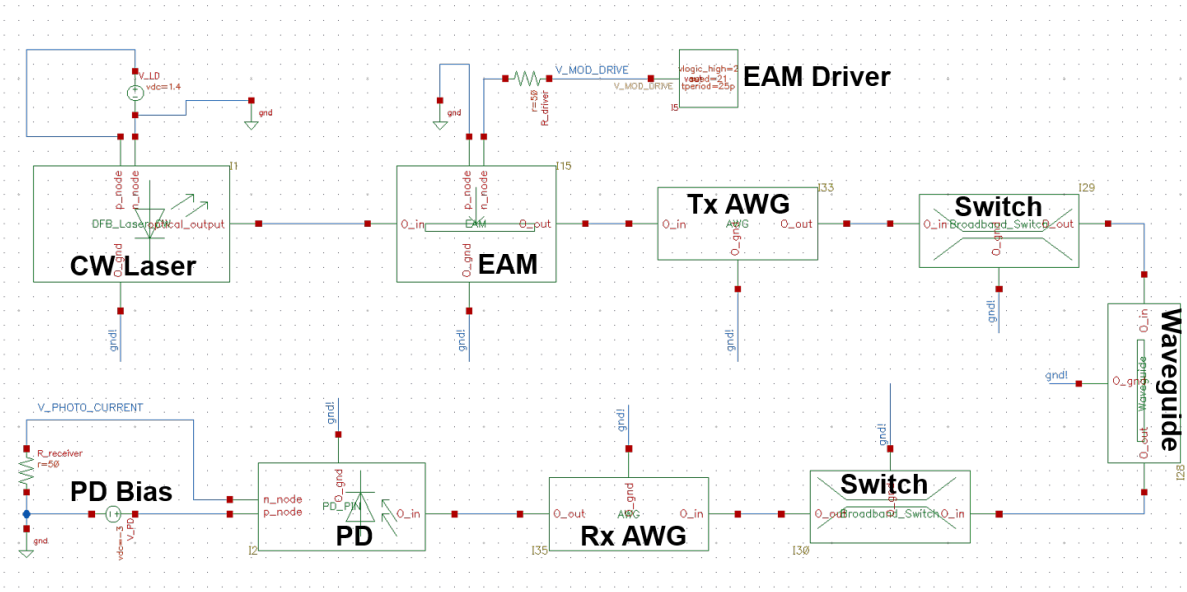


Figure 4.5: The Virtuoso simulation schematic of the entire transceiver link using our developed models.

We first perform AC simulations of the full transceiver link. Fig. 4.6 shows that the simulated frequency response matches well with the measurement data. Then transient simulations are run to obtain the eye diagrams of the link. Fig. 4.7 demonstrates that the simulated eye diagrams have good agreements with the measured ones. The simulations accurately capture the transmission bandwidth limit and pattern dependent noise of the optical link. The measured eye diagrams are noisier than the simulated ones because the large signal measurements includes noises and degradations from electrical components (e.g., RF probes, cables, amplifiers). Both the simulated and measured eye diagrams show that the link's data rate is close to its bandwidth limit seen from the increasing

inter-symbol interference (ISI) and decreasing optical modulation amplitude (OMA). Therefore, we can conclude that the AC and transient simulations give us high confidence that our models are sufficiently accurate.

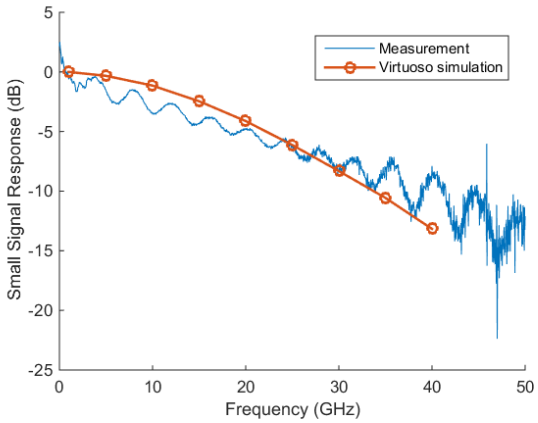


Figure 4.6: Simulated and measured frequency responses of a single channel transceiver link.

4.3.1 Design Space Exploration of the PD Design

Our photonic chip includes a large variety of individual PD test structures with different device lengths and widths, only a subset of which are used in the fabricated full transceiver links due to layout space limitation. In Table 4.1, PD #1 is used in the full transceiver link in Section IV; PD #2, 3 and and 4 are fabricated as individual test structures; the parameters of PD #2* are projected based on PD #2, 3 and 4. The PD #1 and the projected PD #2* have the same area (width $\times$ length). The resistances and capacitances of fabricated PDs are extracted from S11 measurements and the the bandwidth (BW) is obtained by the (R+50)C. It can be observed that the responsivity increases while the bandwidth decreases with the PD length.

We simulate the full link with the various PD designs above and obtain the link eye diagrams at 40 Gb/s, from which we extract the OMA values as shown in the last column in Table 4.1. The simulation results show that PD #4 leads to the highest OMA mainly

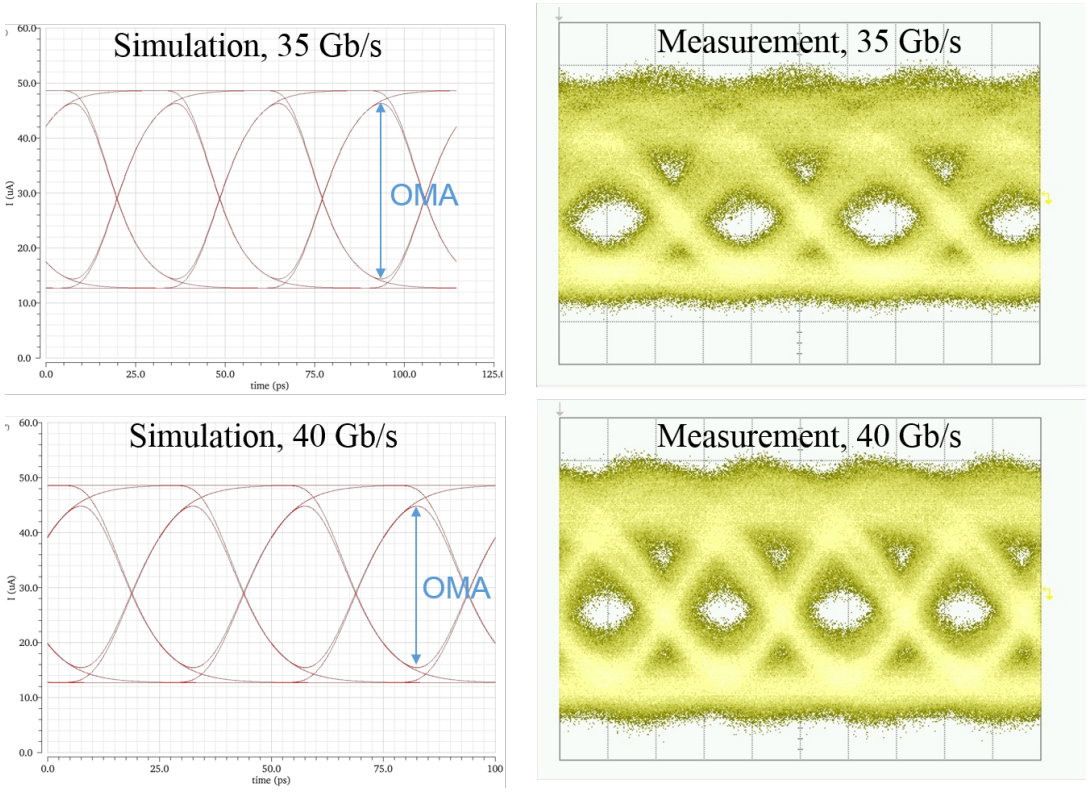


Figure 4.7: Simulated eye diagrams of the PD current, and measured eye diagrams of the RF amplifier that connects to the PD for a single channel transceiver link.

Table 4.1: PD Design Space and Simulated OMA

PD #	Width (μm)	Length (μm)	Resp. (A/W)	Cap. (fF)	Res. (Ω)	BW (GHz)	OMA (μA)
1	4	30	0.45	38.9	38.9	46.0	29.3
2	2	50	0.48	38.6	52.0	40.4	30.6
2*	2	60	0.52	43.4	46.9	37.8	32.8
3	2	75	0.56	54.8	36.0	33.8	34.4
4	2	100	0.66	71.5	29.4	28.0	38.3

because of its high responsivity. The PD #2* has the same area of PD #1 but results in a higher OMA than PD #1. [1] The observations show that the PD design could be optimized together with the full link configurations to optimize the link performance. This study of PD designs demonstrates that, with our models, the designers can now include photonic device designs in whole system optimization.

4.3.2 Optimization of the EAM Driving Voltage

In the link simulations above, 1 Vpp voltage is used to drive the EAM, which saves energy but compromises the OMA. This can also be seen from the EAM's transmission vs. voltage curve in Fig. 3.4 (a), where 1 Vpp is not enough to swing the optical transmission to the maximum or minimum point. We increase the EAM's driving Vpp, re-simulate the eye diagrams at 40 Gb/s, and extract the OMA and modulation energy consumption as plotted in Fig. 4.8 (other device parameters and driving conditions are the same as those in Section IV. A). The simulation results show that the OMA could be enhanced by increasing the EAM driving Vpp at the cost of consuming more transmitter power. A higher OMA reduces the requirement for the receivers sensitivity, which in turn reduce the receiver's power consumption [78]. Therefore, with our photonic models and simulation methodology, the transmitter and receiver could be co-optimized

[1] A higher OMA will result in a better signal to noise ratio (SNR) and, in turn, a lower bit error rate (BER).

for minimizing the overall power consumption while meeting the transmission quality requirement.

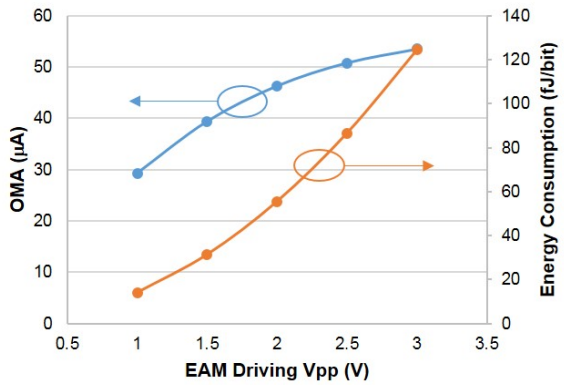


Figure 4.8: The OMA and modulation energy consumption with respect to different EAM driving Vpps.

4.4 Summary

In this chapter, we have simulated two full optical links in SPICE using our photonic device model library. The simulation results are in excellent agreement with the measured results. The simulations of the microring-based back-to-back transceiver utilize the comprehensive model of the microring modulator, which enables both device design explorations and dynamic behavior simulations. For the end-to-end link in the heterogeneous optical NoC, we perform two case studies for photonics-aware design space exploration. The studies reveal the benefits of exploring photonic devices for design optimization, and exploring the trade-off between the transmitter power, OMA, and the receiver power. Overall, we have successfully demonstrated that our models and simulation methodology enable electro-optical co-simulation, allowing designers to co-optimize photonic devices with electronic circuits seamlessly.

Chapter 5

Variation-Aware Adaptive Tuning Technique

In this chapter, we propose an energy-efficient adaptive tuning technique to address the process and thermal variation problems in optical interconnects. The adaptive tuning flow allocates just-enough power for fabricated links, which effectively saves the power consumption.

5.1 Introduction

Nanophotonic interconnects provide high bandwidth, low energy consumption and low latency compared to traditional electrical interconnects. It becomes increasingly promising that the nanophotonic interconnects could replace the electrical links in short-reach applications, such as data centers, inter-chip, and intra-chip communications [79].

The microring resonator is widely used in many optical network-on-chip (NoC) architectures [35, 80, 81, 36, 82, 83], because of its functional versatility, power efficiency, and compact footprint. However, the microring resonator is very sensitive to fabrication

process variation and runtime thermal variation. As a result of the process and thermal variation effects, the resonance wavelength of the ring resonator deviates from the desirable carrier wavelength, which leads to performance degradation or even failure. This wavelength mismatch problem has been extensively studied: many power-efficient tuning and channel arrangement schemes have been proposed [84, 69, 85]; several feedback-based wavelength stabilization circuits have also been implemented [78, 86]. Existing work on thermal and process variations mainly focuses on the tuning of the resonance wavelength[41, 87, 88, 37, 89]. However, the process variation induced variations of quality factor (Q) and extinction ratio (ER) of the microring resonator have not been well studied.

We have fabricated batches of microring modulators and filters on 8 inch silicon-on-insulator (SOI) wafers at the CEA LETI foundry. The optical transmission spectra of the fabricated microring devices across the wafer are measured, from which the quality factor and the extinction ratio are extracted. We notice significant variations of Q and ER from both our fabricated microring resonators and literature [4, 20]. Meanwhile, the Q and ER are very important to determine the BER and power budget of an optical link[4]. Our simulation results show that the variations of Q and ER lead to significant variation of BER of the links. If the link design is targeted at the average performance of the devices, some of the links do not satisfy the BER requirement. Therefore, the variation effects of Q and ER must be carefully addressed.

A naive worst-case based fixed design can guarantee that most of the links satisfy the BER requirement. However, such a fixed design leads to excessive power consumption. In this work, we propose a power-efficient adaptive tuning approach that tunes each link individually and allocates just enough power to meet the BER requirement. The adaptive tuning approach relies on on-chip fast BER estimation circuitry to monitor the link BER, and adaptively tunes either the laser or the photonic receiver to reach the target BER.

We evaluate the power savings gained by the adaptive tuning approach with respect to different NoC architectures, variation values, and link configurations. Overall, the work makes the following contributions:

- Characterizes the process variations of microring-based photonic devices using measured data.
- Demonstrates that the BER of the optical links could vary significantly due to the process variations of microring devices.
- Proposes an adaptive tuning approach that reduces the power consumption than the worst-case based fixed design with reasonable time and area overhead.
- Evaluates the adaptive tuning approach and demonstrates its scalability with respect to different levels of variations and various topologies.

5.2 Background

Nanophotonic interconnects mainly consist of light sources, waveguides, photonic modulators and photonic receivers (Fig. 5.1). On-chip laser arrays and off-chip comb lasers are common choices for the light source [65]. In this work, we consider a distributed feedback (DFB) hybrid silicon laser as an example of the on-chip single-wavelength laser [1], and a Gaussian shape comb laser for the off-chip laser [65]. Silicon waveguides are widely used to guide the light on SOI platforms. At the transmitter side, compact and energy-efficient microring modulators perform the on-off keying modulation of the light signal. At the receiver side, the light signal is redirected by the microring filter and sensed by the photodetector (PD).

The microring structure is critical in the nanophotonic interconnects, and a basic model is introduced here. When an integer number of the incident light wavelength fits the microring perimeter, the microring is on-resonance. At the on-resonance state, the

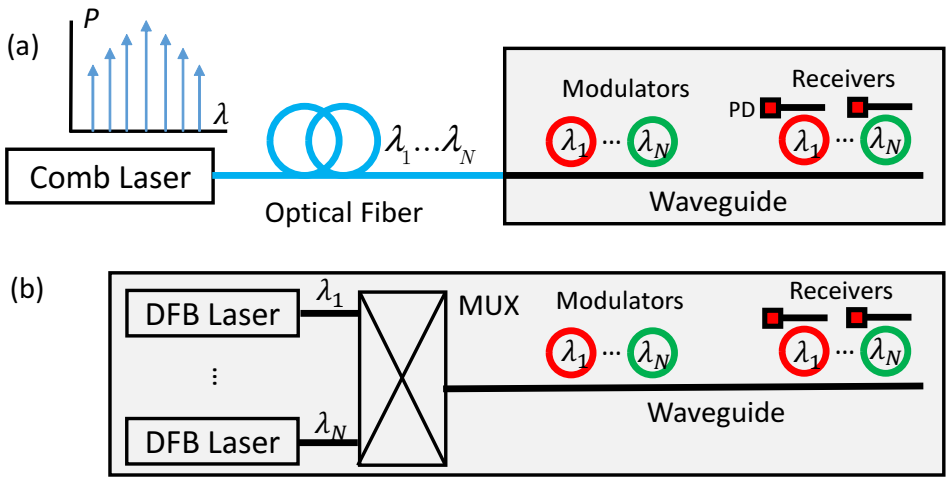


Figure 5.1: Schematics of wavelength-division multiplexing (WDM) nanophotonic interconnects using (a) an off-chip comb laser or (b) an on-chip DFB laser array.

through port power reaches its minima and the drop port power reaches its maxima. The optical transmission spectrum of the through port and the drop port can be described by the Lorentzian shape models [64] (Fig. 5.2):

$$T_{thru}(\lambda) = 1 - \frac{A_{thru}}{1 + (2Q \cdot (\lambda - \lambda_r)/\lambda_r)^2}$$
$$T_{drop}(\lambda) = \frac{A_{drop}}{1 + (2Q \cdot (\lambda - \lambda_r)/\lambda_r)^2} \tag{5.1}$$

where λ_r is the the microring's resonance wavelength; Q is the microring's quality factor; A_{thru} is a parameter that is related to the microring's extinction ratio: $ER = 1/(1 - A_{thru})$. Furthermore, we denote the optical transmission at the on- (off-) resonance state as $T_{on} = T(\lambda = \lambda_r)$ ($T_{off} = T(\lambda = \lambda_r + \Delta\lambda)$), where $\Delta\lambda$ is the wavelength detuning for the off-resonance state. In this way, when the microring functions as a modulator, the optical transmission at logic "0" and logic "1" are $T_0 = T_{thru,on}$ and $T_1 = T_{thru,off}$, respectively. When the microring functions as a filter, the input port to drop port insertion loss (the drop port efficiency) is $T_{drop,on}$. Microring structures could also be used to build optical routers [25, 24]. For instance, in the five-port optical router reported in [25], the west-

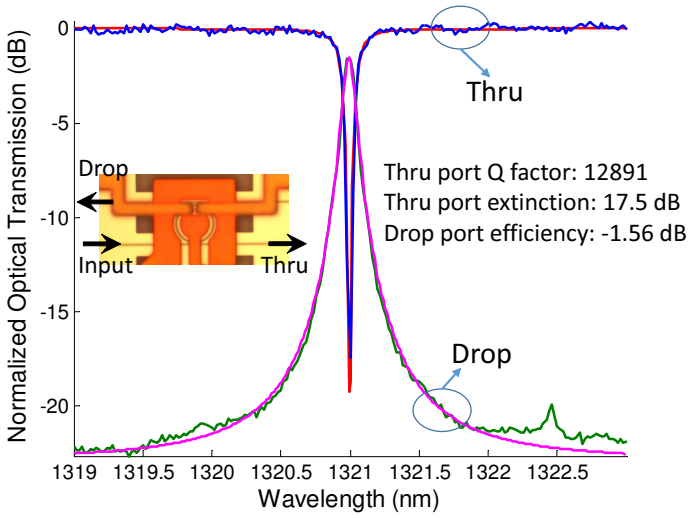


Figure 5.2: The optical transmission of the through port and drop port of a microring (blue and green: measurement; red: model). The inset shows a microscopic image of a fabricated microring modulator.

to-east insertion loss could be expressed as $T_{drop,on} \cdot T_{thru,off}^4 \cdot T_{WG\_loss}$.

Based on the theoretical device models above, we obtain the equation for the bit-error-rate (BER), a widely used figure of merit for communication quality:

$$\text{BER} = \frac{1}{2}\text{erfc}\left(\frac{z}{\sqrt{2}}\right), \quad z = P_{laser}\prod_i IL_i \cdot R_{pd}\frac{T_1 - T_0}{\sigma_1 + \sigma_0} \tag{5.2}$$

where P_{laser} is the laser output power; IL_i is the insertion loss of the photonic component i along the optical path; R_{pd} is the responsivity of the photodetector; $\sigma_1(\sigma_0)$ is the standard deviation of the logic "1" ("0") corresponding noise.

5.3 Variation Challenges

Similar to deep submicron electronic devices, the nanophotonic devices (e.g., microring modulators, microring filters, grating couplers, photodetectors) also suffer from significant process variations [20]. In this work, we mainly focus on the severe variation

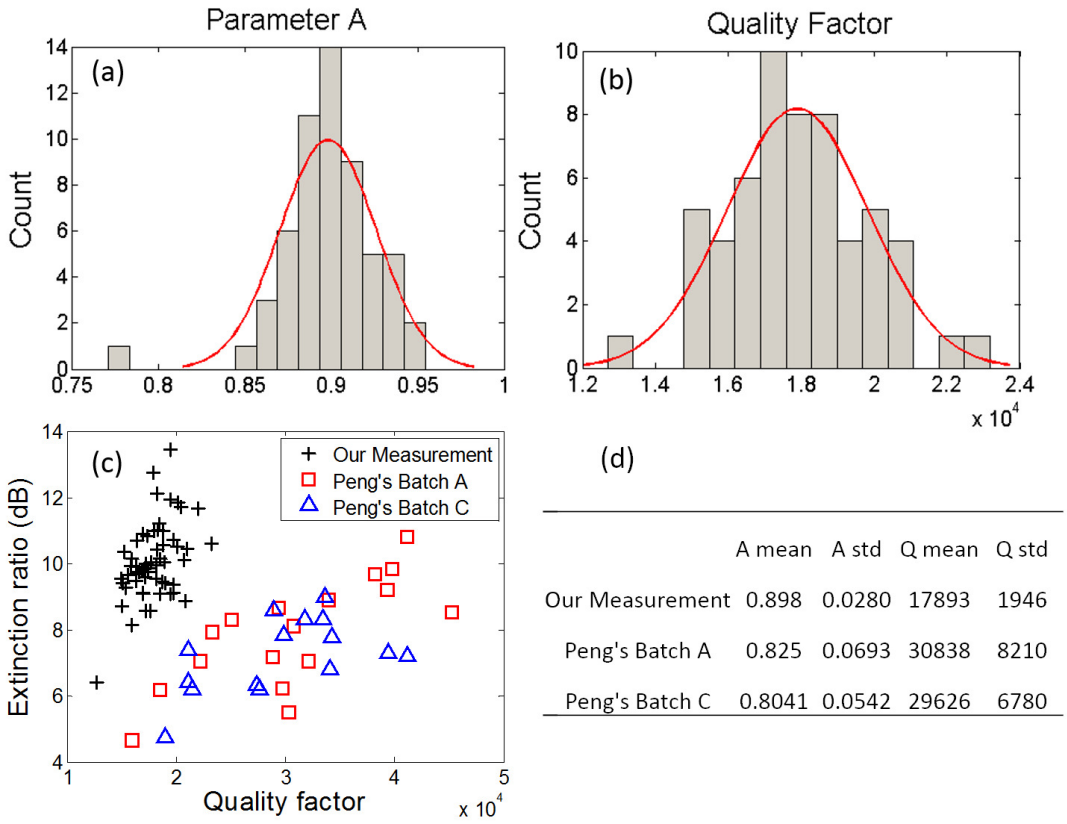
effects in microring based devices, while our variation-aware analysis and design can also accommodate variations in other types of devices.

The microring structure is very sensitive to runtime thermal variation and fabrication-induced process variation. Due to the thermal variation effect, the optical transmission spectrum redshifts as the temperature rises. Due to the process variation effect, the device geometry and the waveguide sidewall roughness vary in the fabrication process. Consequently, the λ_r, Q and ER deviate from the designed values. Both thermal and process variation effects will cause the mismatch between the resonance wavelength and the carrier wavelength. Many tuning schemes and circuits have been proposed to address the wavelength mismatch problem [84, 69, 90, 78, 86]. However, few tuning schemes take into account the variations of the Q and the ER.

Here we characterize the variations of the Q and the ER based on measured results. Fig. 5.3 plots our wafer-scale inter-die measured data of the fabricated microring devices, together with the intra-die variation testing result reported in [4]. Both the inter-die and intra-die measured results show wide distribution ranges of Q and ER, which may have great impact on the communication BER. From the histograms, one can see that the distribution of the parameter A and the Q approximately follow normal distributions.

The electrical tuning is usually utilized to compensate for the wavelength mismatch because it's more power efficient than the thermal tuning [44, 41]. However, the Q and the ER degrade significantly when the tuning voltage is applied to the microring resonator (Fig. 5.4). The severe degradation of Q and ER caused by the electrical tuning may greatly deteriorate the communication BER, which also needs to be carefully considered during the link analysis.

The Q and the ER are important to determine the microring's optical transmission and the BER (Eq. 5.1 and 5.2). The large variations of Q and ER may result in significant variation of the BER. We perform Monte Carlo simulations of a simple single-



	A mean	A std	Q mean	Q std
Our Measurement	0.898	0.0280	17893	1946
Peng's Batch A	0.825	0.0693	30838	8210
Peng's Batch C	0.8041	0.0542	29626	6780

Figure 5.3: (a)(b) Histograms of parameters A and Q of our inter-die measurement results; (c) Scatter plot of our inter-die measurement and Peng's intra-die measurement in [4]; (d) Mean and standard deviation (std) of the three measured data sets.

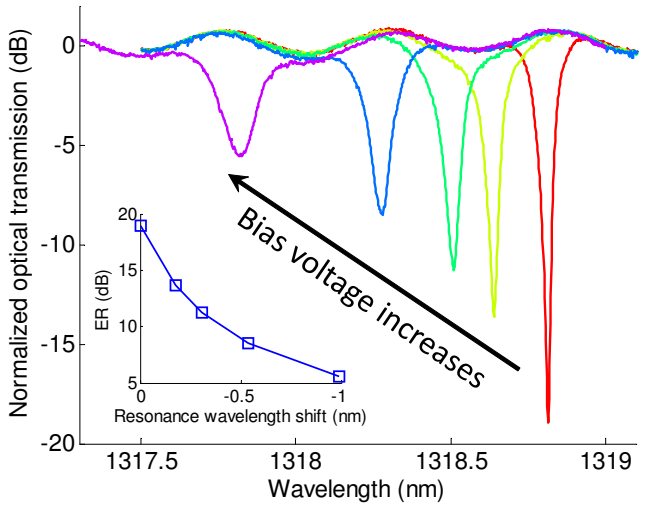


Figure 5.4: The measured spectra series of a microring modulator at different bias voltages.

writer single-reader (SWSR) link [35]. The process variation statistics of our fabricated devices are used (the first line in Fig. 5.3d), which has better ER and uniformity than the Peng's devices in [4]. The simulation results in Fig. 5.5 show that the BER has a wide distribution range. About half of the links do not satisfy the BER requirement if the link design is based on the mean parameter values of the devices. Naively, a worst-case based fixed design could guarantee that most of the links satisfy the BER requirement (the red line in Fig. 5.5). However, such a fixed design requires excessive power consumption. For instance, in our simulation the laser output power needs to be increased by 20% to guarantee that 99% of the fabricated links satisfy the 10^{-12} BER requirement.

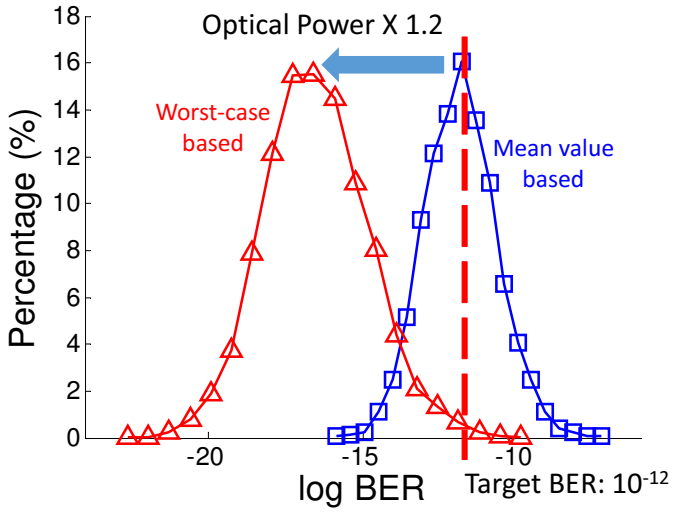


Figure 5.5: The BER distribution in the presence of process variations and the electrical tuning. The blue line represents the link configuration based on the means of the device parameters. The red line enhances the link optical power by 1.2X

5.4 Adaptive Tuning Approach

Instead of the power-consuming, worst-cased based fixed design, we propose an adaptive tuning approach that tunes each optical link individually to meet the BER require-

ment. At a given BER and data rate, the minimum required optical modulation amplitude (OMA) is determined by the receiver sensitivity P_{sense}:

$$P_{laser} \prod_i IL_i \cdot (T_1 - T_0) = P_{sense} \tag{5.3}$$

If the IL_i, T_1, and T_0 vary due to process and thermal variations, we could tune either the laser output power P_{laser} or the receiver sensitivity P_{sense} to satisfy the above equation. Intuitively, we could tune the DFB laser's output power by varying its driving current as illustrated in Fig. 5.6 a), where dots represent measurement result from [1], and line represents model results. However, for interconnect schemes using an off-chip comb lasers, it's inefficient to tune the laser's output power. This is because a comb laser has a fixed optical spectrum distribution; and individual wavelength cannot be tuned independently.

Fortunately, we notice an effective mechanism to trade off the power consumption for the receiver sensitivity as illustrated in Fig. 5.6 b), where the adaptive photonic receiver is from [78]. The supply voltage of the receiver circuitry, i.e. the trans-impedance amplifier (TIA), has a significant impact on the gain, bandwidth, and noise performance [78]. As the TIA supply voltage increases, the circuitry consumes more power and the receiver achieves a better sensitivity (Fig. 5.6 b). Another benefit of tuning the receiver is allowing the sharing of on-chip lasers [43]. In summary, for optical links using on-chip DFB lasers, we could tune either the laser output power or the receiver sensitivity. For links using off-chip comb lasers, we could only tune the receiver sensitivity.

Fig. 5.7 illustrates the flow of the adaptive tuning approach. At the beginning, a specific writer-reader communication pair is activated. The TIA supply voltage or the laser driving voltage is set to a relatively low value based on the best-case device parameters. Then an on-chip BER testing circuitry performs the BER test. The TIA or

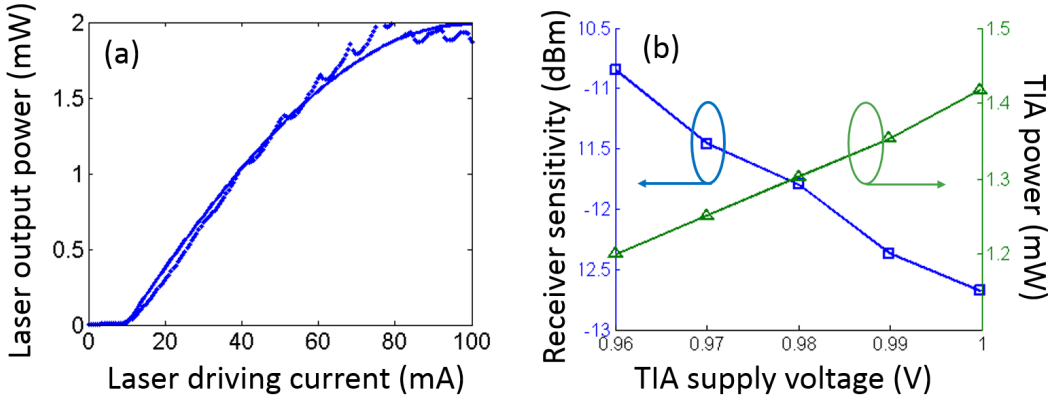


Figure 5.6: (a) The laser output power as a function of the driving current of a DFB laser; (b) The sensitivity and power consumption versus supply voltage of an adaptive photonic receiver.

laser voltage is gradually increased until the BER is below a pre-set target (eg. 10^{-12}). Finally, the *just enough* TIA or laser driving voltage is stored in the flash memory as a lookup table (LUT). At runtime, the laser or the TIA voltage is configured based on the corresponding data stored in the LUT. This adaptive tuning flow could be activated before shipment, after deployment, or whenever an abnormal error rate is observed by higher level blocks (e.g., by using parity check) during operation . It should be noted that when the electrical tuning is applied, the TIA or laser power should also be increased accordingly at runtime to compensate for the degradation of Q and ER.

One of the key enabler in the adaptive tuning scheme is the fast on-chip BER testing circuitry. The brute-force BER testing method is unaffordably time-consuming (over 100 seconds for 10^{-12} BER at 10Gbps data rate) for the proposed adaptive tuning. Fortunately, there are fast BER estimation methods that leverage voltage offsetting or sampling time offsetting [91, 92]. As illustrated in Fig. 5.8, the BER decreases when the received power decreases or when the sampling time deviates from the ideal sampling point. Therefore, the voltage offsetting method or the sampling time offsetting method could be leveraged to accelerate the BER test. These two methods use an additional

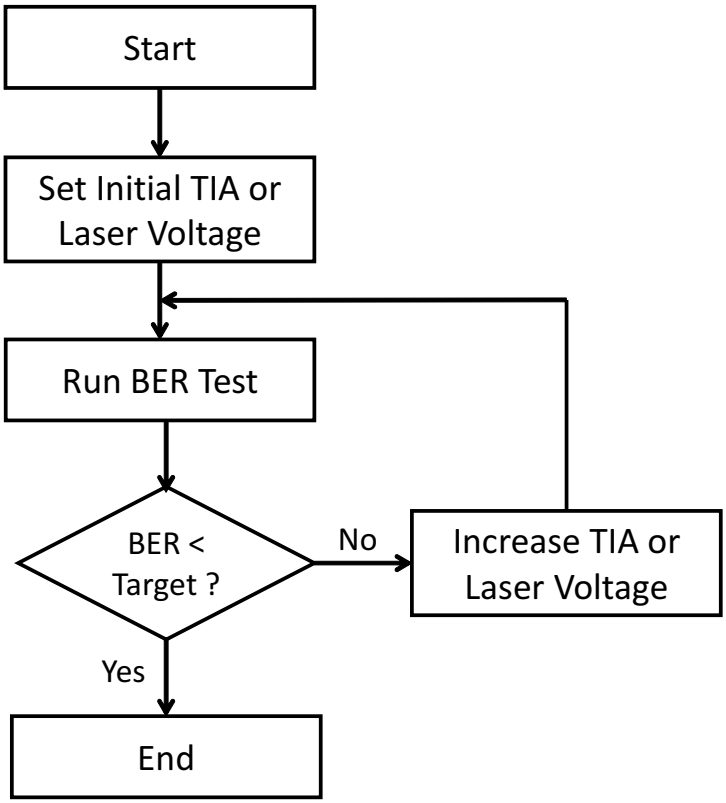


Figure 5.7: The adaptive tuning flow.

comparator that intentionally decreases the received power or deviates the sampling time. By comparing the additional comparator's output with that of the normal data comparator, eye closure could be detected much faster. For instance, if our target BER is 10^{-12}, the BER after voltage or sampling time offsetting can be intentionally increased to about 10^{-10}. It takes only several seconds to estimate such an increased BER for a 10 Gbps link.

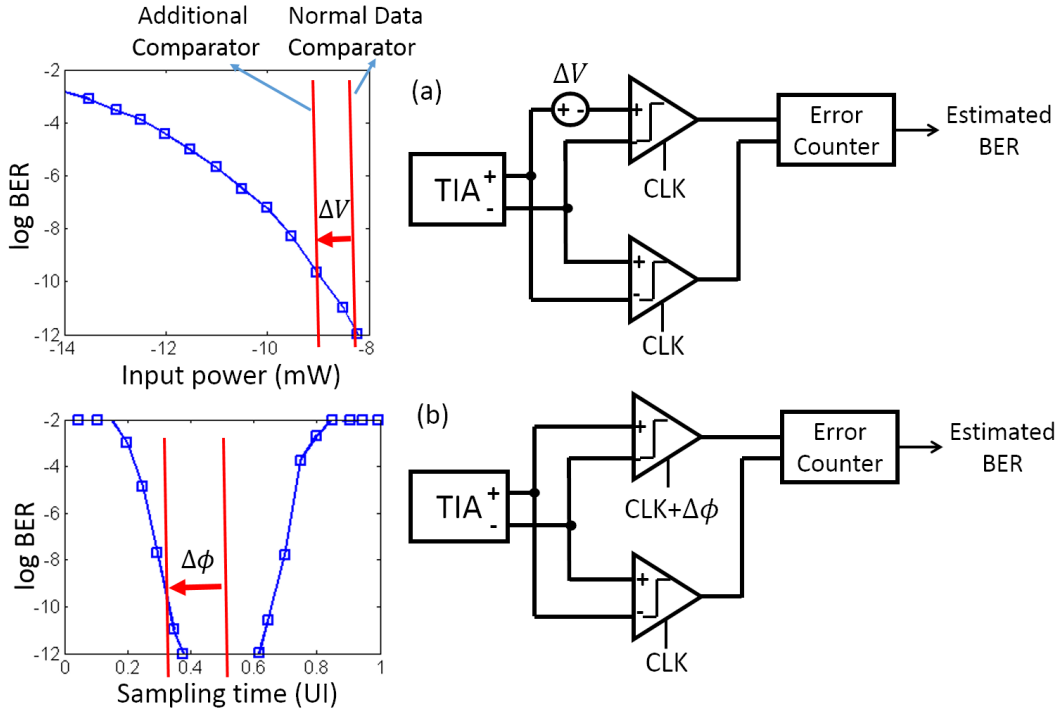


Figure 5.8: The two fast BER estimation methods: (a) offset the voltage; (b) offset the sampling time. The data in the left two figures are from [5].

There are two overheads associated with the adaptive tuning approach: the hardware overhead and the tuning time overhead. The hardware overhead, mainly in the BER monitor, includes an additional comparator with offset control and a small logic circuit, which takes about 30 μm x 30 μm area for a 65 nm CMOS technology [91]. For a multi-receiver link, its hardware cost can be amortized by sharing the BER monitor, as the multiple receivers on one link cannot receive signal simultaneously. In this way, for a

64-cluster crossbar with 64 WDM channels, the total area cost of the BER monitors is only 1.0% of the chip area (366.1 mm^2 in [43]). The tuning power overhead is avoided at runtime as the BER monitor circuit is switched off after the tuning process is complete. The tuning time overhead for a link is proportional to the number of communication pairs times the BER estimation time. For a WDM link, all wavelength channels could be tuned concurrently. For instance, assuming the BER estimation time is about 5 s, the tuning time for a many-writer single-reader (MWSR) link with 64 clusters (e.g., Corona [80]) is 320 s, which is reasonable for a one-time overhead. Overall, the hardware and time overheads are reasonable for practical applications.

5.5 Evaluations

In this section, we perform simulations and analysis of several common photonic NoC architectures to evaluate the power saving gained by the proposed adaptive tuning approach. Several representative types of link structures are identified (as illustrated in Fig. 5.9) for experiments among the common photonic NoC architectures:

- Single-writer single-reader (**SWSR**): The SWSR point-to-pint link is used in the three-stage Clos network [35]. The Clos network uses SWSR optical links for stage-to-stage communication and electrical routers for routing.
- Many-writer single-reader (**MWSR**): The MWSR optical links can be used to construct optical crossbars for optical NoC. For instance, the Corona architecture replicates the MWSR channel 64 times to fully connect the 64 clusters [80]. For the adaptive tuning, each possible communication pair is individually tuned and the just enough TIA supply voltages are stored in a LUT.
- Single-writer many-reader (**SWMR**): Similar to the MWSR structure, the SWMR links can also be used in crossbar structures. For instance, the Firefly architecture

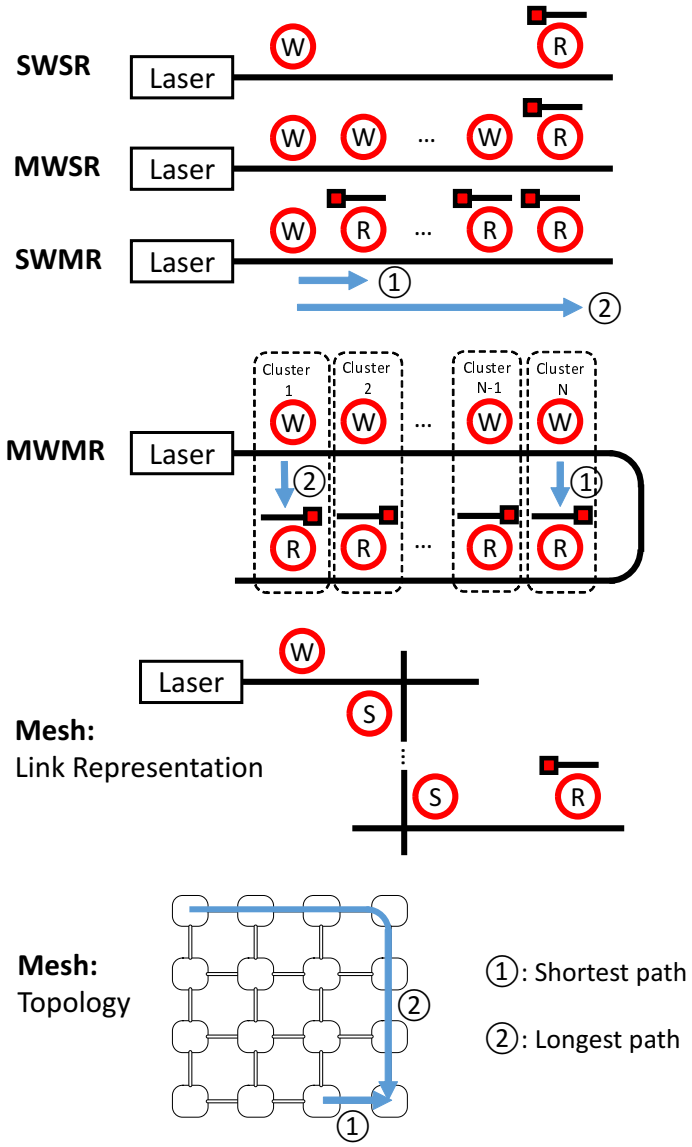


Figure 5.9: Five types of link structures. Notions: W: writer or photonic modulator; R: reader or photonic receiver; S: photonic switch or router. In a WDM system, the laser represents a multi-wavelength light source; each microring represents a microring array for multiple wavelength channels

uses a SWMR-based crossbar for inter-cluster communication and a concentrated mesh for intra-cluster [36]. Additionally, the SWMR structure is used in an optical bus-based NoC architecture to broadcast the optical signal [81].

- Many-writer many-reader (**MWMR**): LumiNOC leverages the MWMR structure for subnet design, where each cluster is connected with a writer and a reader such that any cluster can communicate with any other cluster [82].
- Optical router based **mesh**: Microring-based optical routers are used in mesh-based NoC architectures in a manner of circuit switching. For instance, Petracca *et al.* proposed a non-blocking mesh NoC architecture using 4x4 optical routers [83]. The light source for each node is either from its own lasers or from optical power waveguides.

5.5.1 Experimental Setup

We perform Monte Carlo simulations to calculate the power consumptions by the fixed design and by the adaptively tunable design. The process variation statistics of parameters A and Q in the first line of Fig. 5.3 d are used to generate random instances of microring devices. The standard deviation of resonance wavelength caused by the process variation is 0.44 nm [41]. The channel spacing is set to 0.9 nm (160 GHz) to match the grid of the laser [93]. Since the electrical tuning is power-efficient and the electrical tuning range (1 nm in Fig. 5.4) can cover the channel spacing (0.9 nm), we therefore adopt the electrical tuning with the channel remapping (or reshuffling) technique to compensate for the wavelength mismatch [84, 69]. Other than specified for parameter sweeps, the number of clusters is set to 16; the maximum temptation variation is set to 17°C [41]; the laser type is on-chip DFB laser. The length of the longest communication path is set to 4 cm to accommodate the chip area (366.1 mm^2 in [43]). The waveguide loss is

assumed to be 0.74 dB/cm [94].

The fixed design uses the same TIA supply voltage for all photonic receivers; the yield target is set to 99%. The adaptive tuning leverages the sensitivity-adaptive photonic receiver illustrated in Fig. 5.6 b, and configures each TIA's supply voltage individually depending on the present communication pair. Each writer (or reader) in the many-writer (or reader) structure is assumed to have the same probability to write (or read). The average power consumption of a TIA for the fixed design and the tunable design are reported in the simulations. Fig. 5.10 shows the Monte Carlo simulation result of a SWMR link, where the fixed design has to set the TIA power as high as 1.32 mW while the adaptively tunable design achieves an average TIA power of 1.05 mW.

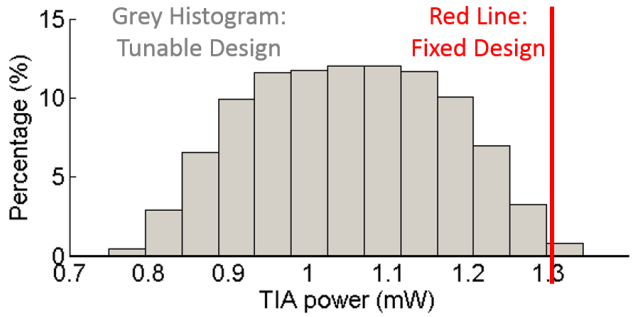


Figure 5.10: The simulated TIA power consumption for the fixed design and the tunable design.

5.5.2 Process and Thermal Variations

From Fig. 5.3 (c)(d), one can see that the process variation statistics are very distinct for different fabrication processes. In order to evaluate the performance of the adaptive tuning approach at different process variation levels, we sweep the standard deviation of the parameter A, which is an important factor to determine the link's BER. Fig. 5.11 shows that the average receiver power by the adaptive tuning is decoupled from the process variation.

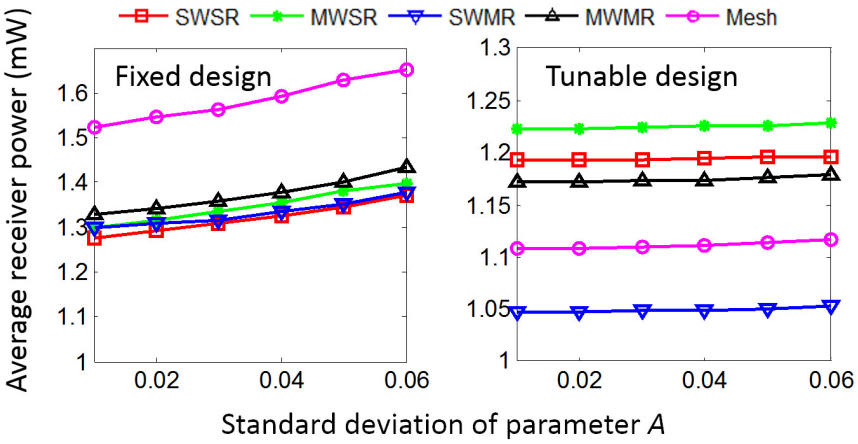


Figure 5.11: The average receiver power consumption at different process variations and for different link structures with 16 communication nodes.

Temperature variations of an NoC is design- and workload- dependent. We simulate the average receiver power at different maximum temperature variation values. The simulation results in Fig. 5.12 show that the receiver power of both the fixed design and the tunable design are decoupled from the temperature variation. This is because the channel remapping technique [44] decouples the required tuning distance from the the thermal variation when the process variation ($3\sigma = 1.32nm$) is greater than the channel spacing (0.9 nm). This decoupled phenomenon has also been observed in [44, 69].

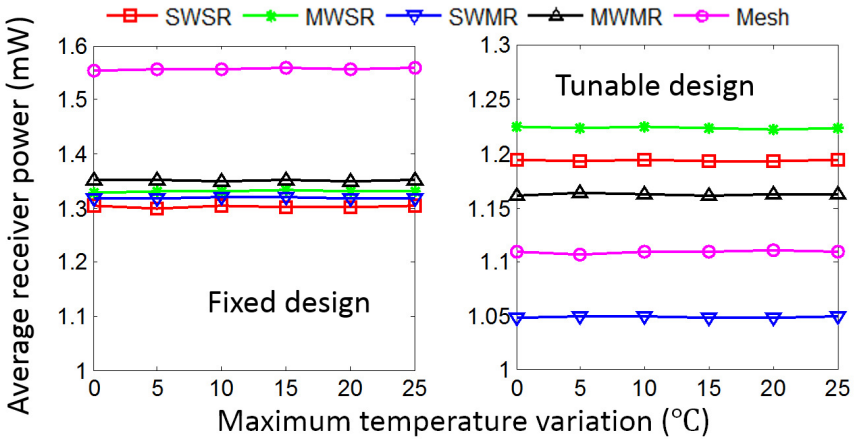


Figure 5.12: The average receiver power consumption at different temperature variations and for different link structures with 16 communication nodes.

5.5.3 Number of Clusters

We also evaluate the power savings with respect to different numbers of clusters. Fig. 5.13 shows that, for SWMR, MWMR, and Mesh links, the power saving will be greater for a design with more clusters. This is due to the fact that the communication path lengths are highly non-uniform in SWMR, MWMR, and Mesh links, as illustrated by the shortest and longest paths in Fig. 5.9. The shortest and longest paths potentially lead to very distinct best-case and worst-case link performance [39]. In other words, the non-uniformity of the communication path lengths, together with the process and thermal variations, contribute to the power savings.

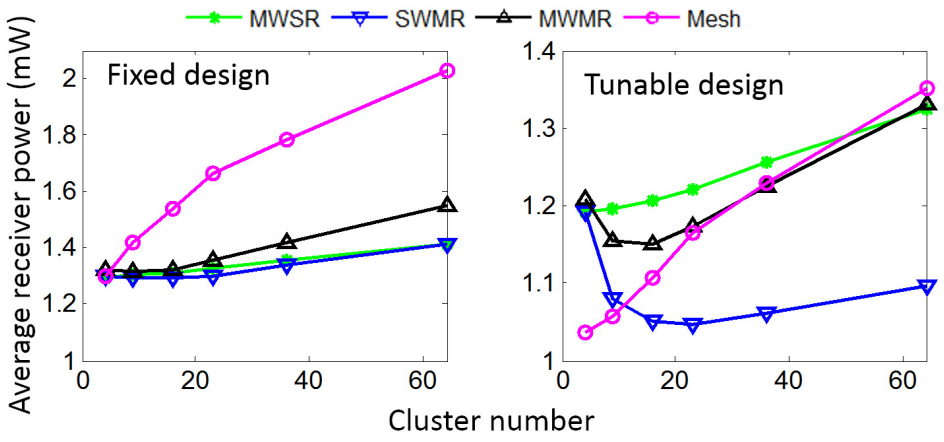


Figure 5.13: The average receiver power consumption at different numbers of clusters and for different link structures.

5.5.4 Type of Lasers

Previous simulations all assume the links use on-chip DFB lasers as the light source. Comb lasers intrinsically have non-uniform output power at different wavelengths, for which the adaptive tuning should achieve even greater power saving. We simulate the comb laser based optical links with 16 channels. The output spectrum of a Gaussian comb laser is described in [65]. In the simulations, we assume that the output power

of the comb laser at its center wavelength (the maxima) equals the DFB laser output used in previous simulations plus the fiber-to-chip coupling loss. The simulation results confirm that the adaptive tuning leads to greater power savings for comb lasers based links (Fig. 5.14).

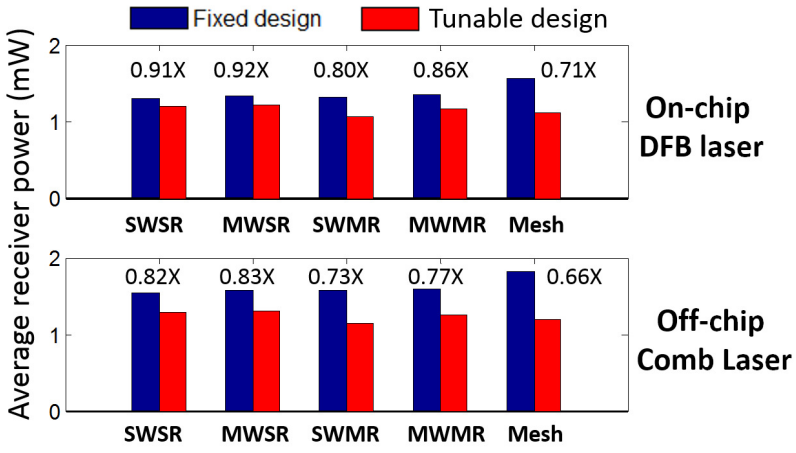


Figure 5.14: The average receiver power consumption for different laser types and for different link structures. The numbers denote the ratios of the average receiver power by the tunable design to the fixed design.

In summary, the adaptive tuning approach scales well with the process variation, the thermal variation, and the number of clusters, especially for comb lasers based links and for link structures with non-uniform path lengths.

5.6 Summary

Microring resonator based nanophotonic interconnects are very sensitive to process and thermal variations. In this work, we model the microring based photonic devices and their variation effects using the measured data. Taking into account the process and thermal variation effects, our simulations show that the BER of optical links has significant variation. Since the worst-case based fixed design consumes much excessive power, we propose a novel power-efficient adaptive tuning approach. The proposed approach could

tune each link individually and allocate just enough power to meet the BER requirement. This approach offers good power efficiency with reasonable area and time overhead. Our simulation and analysis demonstrate that the proposed adaptive tuning approach scales well with respect to different process variations, thermal variations, numbers of clusters, and laser types. Particularly, the adaptive tuning could save more power for link structures with non-uniform communication path lengths and/or using comb lasers.

Chapter 6

Optimal Pairing of Microring-based Optical Transceivers

In this chapter, we will first introduce the schematic and the tuning scheme of the microring-based transceiver. The optimal assignment and pairing algorithms are designed to mix-and-match microring-based transceivers to minimize the overall tuning power consumption. The optimization algorithms demonstrates effective power saving on both realistic and synthetic data sets.

6.1 Introduction

Silicon microring-based optical transmitters and receivers are very attractive due to its compact footprint, low energy consumption, and MUX-free WDM implementation [21, 95, 96]. Microring resonators are highly wavelength selective and can modulate or route optical signals [13, 24]. However, the microring resonators are very sensitive to fabrication process variations. The geometry variations of the fabricated microrings could lead to a variation of the microring resonance wavelength as large as 5 nm. In

contrast, the microring modulator and filter usually have a high Q factor and a small passband (0.1∼0.2 nm). Consequently, the resonance wavelength of a microring needs to be tuned to align with the carrier wavelength.

In microring-based optical interconnects, the tuning power accounts for a non-trivial portion of the total power budget [69]. It is desirable to design a scheme to effectively reduce the tuning power. Zheng et al. proposed several techniques to reduce the average tuning power. However, some of its assumptions were not valid for realistic devices and their proposed techniques were not tested on realistic data sets [84]. In this work, we study the assignment and pairing problem of fabricated microring-based WDM transceivers. The problem we attempt to address is formulated based on real fabricated WDM transceivers: a batch of microring-based devices that are subject to process variations could be optimally mix-and-matched to form transmitter-receiver pairs with the objective of minimized tuning power. A Hungarian method and a simulated annealing-based algorithms are designed to tackle the problem in two cases, naming as separable and inseparable transmitters and receivers. Our proposed algorithms are tested on both measurement data from batches of fabricated devices and well established synthetic data sets, both of which show excellent results of power saving and algorithm scalability w.r.t. the device count for pairing.

6.2 Background

In this section, we introduce the schematic of our objective microring-based transceiver. Then its process variations and thermal tuning are illustrated. A model of the wavelength process variation in multi-microring transceiver is also developed here in order to generate synthetic data sets to test our optimization algorithms in Sections 6.3 and 6.4.

6.2.1 Overview of the Optical Transceiver

The WDM optical transceiver in this study is based on microring modulators and filters as illustrated in Fig. 6.1. The transmitter (Tx) and the receiver (Rx) are fabricated side-by-side on 200 mm SOI wafers at CEA Leti. Corresponding Tx and Rx CMOS circuits on electrical dies will be bonded to the optical die. The microring modulators and filters have 10 µm diameters and 13.9 nm free spectral ranges (FSR).

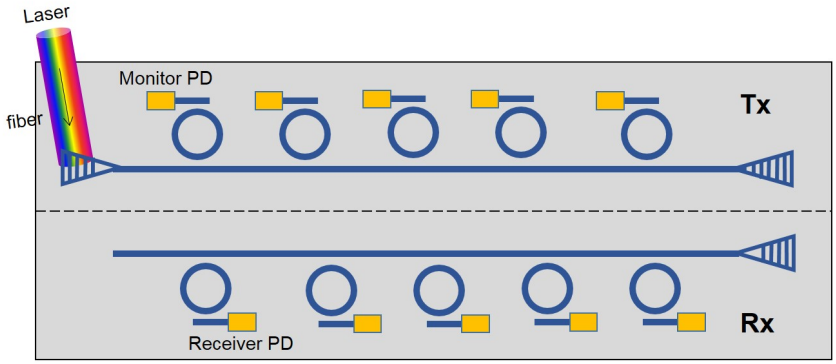


Figure 6.1: Schematic of the WDM optical transceiver.

In the optical Tx, light is generated by a multi-wavelength off-chip laser (e.g. a WDM comb laser [21]), and then coupled onto the optical die by a silicon grating coupler. The light is modulated by the silicon microring modulator at a certain wavelength. Local heaters based on doped silicon are placed inside the microrings in order to tune the wavelength aligning with the laser wavelength grid through thermal tuning. In the Tx microring modulators, monitor photodetectors (PD) at the drop waveguide are used to detect the resonance wavelength during thermal tuning. At the output of the Tx, light is coupled out through a grating coupler to optical fibers or on-board polymer waveguide depending on the applications [97]. In the optical Rx, light at a certain wavelength is routed to the drop waveguide of the microring filter. The light is further detected by a high-speed PD.

A 200 mm SOI wafer consists 49 dies as shown in Fig. 6.2. The microring Each die has 9 transceivers where 5 of them have 80 GHz channel spacing and 4 of them have 160 GHz channel spacing. 9 representative locations of the wafer, highlighted in the Fig. 6.2, were tested, while the lower Rx data was not correctly measured for one of the 9 locations. As a result, we have 40 valid transceiver devices data with 80 GHz channel spacing, and 31 valid transceiver devices data with 160 GHz channel spacing due to the lack of clear resonance dips in one transceiver data.

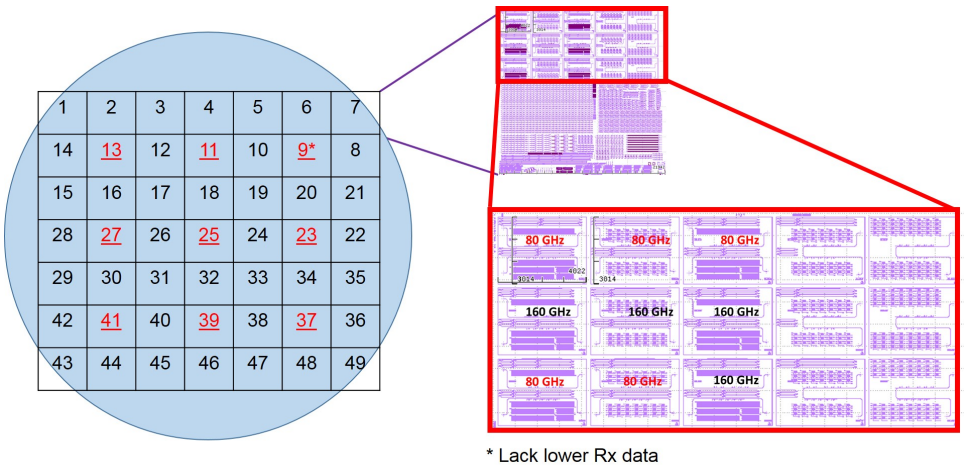


Figure 6.2: The silicon photonic transceiver wafer.

6.2.2 Process Variations and Tuning

Due to inevitable fabrication process variations, the actual resonance wavelengths would deviate from the nominal values. Fig. 6.3 shows our measured optical spectra of a Tx and an Rx in a transceiver block. The resonance wavelengths of Tx and Rx need to be tuned to align with each other, as well as to match the WDM grid with certain channel spacing. In this work, the channel spacing of the off-chip comb laser is 80 GHz. The comb laser's absolute wavelengths could be shifted by controlling its temperature, and the laser's tuning power is not counted toward the on-chip tuning power budget.

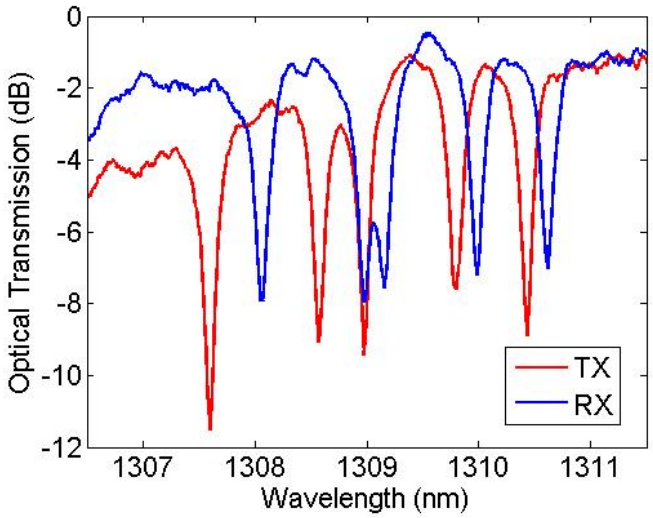


Figure 6.3: Measured optical spectrum of a transceiver

Fig. 6.4 shows the resonance wavelengths before tuning (the red and blue solid dots) and after tuning (the dashed vertical lines) of a transceiver. The absolute wavelengths of the WDM grid are chosen so that the total tuning distance is minimized, and each wavelength is only red shifted. Only thermal tuning is applied in this work, because electrical tuning (biasing the microring p-i-n junction) would make it difficult to achieve optical high-speed driving conditions [63] [1].

Depending on the design and fabrication details, the Tx and Rx in one transceiver block would either be separated and individually packaged, or not be separated and be packaged as a whole transceiver. The overall thermal tuning distance and power could be minimized by optimally assigning a Tx to an Rx, or optimally selecting transceiver pairs for point-to-point links. These two cases are discussed in the following two sections.

[1]The choice of tuning type only affects the tuning cost matrix and does not change the following optimization algorithms.

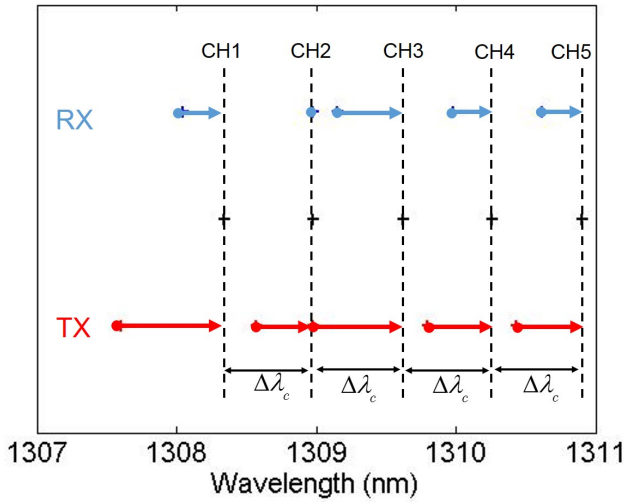


Figure 6.4: Illustration of the thermal tuning of 10 microrings in a transceiver, where $\Delta\lambda_c = 0.64$ nm.

6.2.3 Process Variation Model

In order to characterize the process variations in multi-microring transceivers, we propose a model for the resonance wavelengths of transceivers. From a number of measured transceiver spectra (Fig. 6.3 and others), we observe that the transceiver wavelengths are subject to both a large inter-transceiver global variation (GV) and a small intra-transceiver local variation (LV). Also, within one transceiver, the Rx wavelengths have an obvious offset from Tx wavelengths, which is described by a Tx-Rx variation ($TRxV$) term. Taking into account these factors, we express the wavelength of transceiver #i's channel #j, $\lambda_{TX/RX}(i,j)$, in Eq. (6.1), where i is the transceiver index, j is the channel index ($j = 1 \sim 5$ for the data in this study), λ_0 is the average wavelength of channel #1, $\Delta\lambda_c$ is the channel spacing (0.64 or 1.28 nm in this work).

$$\begin{aligned} \lambda_{TX}(i,j) &= \lambda_0 + GV_i + (j-1)\Delta\lambda_c + LV_j \\ \lambda_{RX}(i,j) &= \lambda_0 + GV_i + TRxV_i + (j-1)\Delta\lambda_c + LV_j \end{aligned} \tag{6.1}$$

We use the measured wavelength data to validate the model in Eq. (6.1), and to extract the variation components (GV, LV, and $TRxV$). Firstly, each wavelength is shifted based on its channel index to be nominally aligned with channel #1: $\lambda'(i,j) = \lambda(i,j) - (j-1)\Delta\lambda_c$. Then the variances of GV and LV are computed based on Eq. (6.2), which essentially describes the inter-transceiver and intra-transceiver variations respectively.

$$\begin{aligned} \mathrm{var}(GV) &= \mathop{\mathrm{var}}_{i}\left\{\mathop{\mathrm{mean}}_{j}\left(\lambda'(i,j)\right)\right\} \\ \mathrm{var}(LV) &= \mathop{\mathrm{mean}}_{i}\left\{\mathop{\mathrm{var}}_{j}\left(\lambda'(i,j)\right)\right\} \end{aligned} \tag{6.2}$$

The random variables of GV and LV are visualized in Fig. 6.5. The histograms show that both of GV and LV follow normal distributions with zero mean. The variance of GV is much larger than that of LV, which in turn confirms our model based on separable GV and LV. The $GV \gg LV$ is also consistent with the conclusion that wavelength mismatch between devices is linearly dependent on their physical distance in [98].

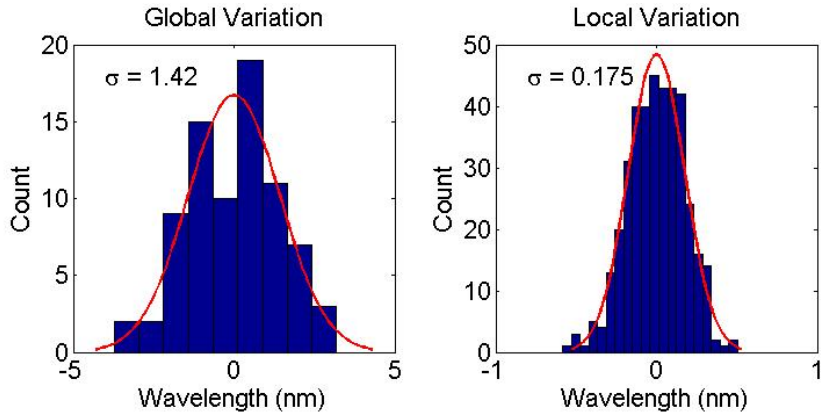


Figure 6.5: The distribution of random variables of global and local variations for our 80 GHz data set.

To quantify the variance of $TRxV$, we calculate the difference of the two equations in Eq. (6.1), and obtain Eq. (6.3). The random variable of $\lambda_{RX}(i,j) - \lambda_{TX}(i,j)$ is visualized

in Fig. 6.6 which demonstrates a normal distribution shape with zero mean. Therefore, the distribution of $TRxV$ is also regarded as a normal distribution with zero mean. The variance of $TRxV$ can be obtained from Eq. (6.3).

$$\text{var}(TRxV) + 2\text{var}(LV) = \underset{i,j}{\text{var}}\{\lambda_{RX}(i,j) - \lambda_{TX}(i,j)\} \tag{6.3}$$

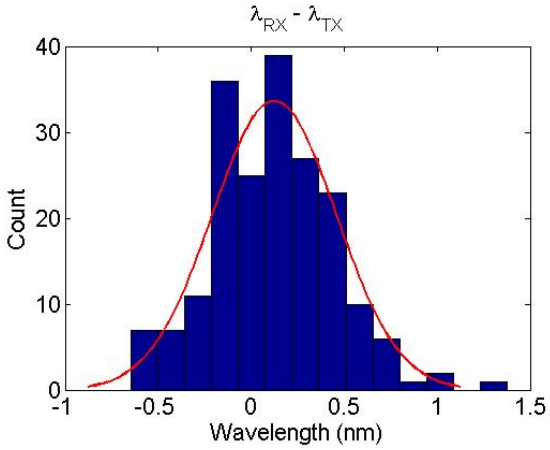


Figure 6.6: The distribution of random variables of $\lambda_{RX} - \lambda_{TX}$ for our 80 GHz data set.

The analysis of the measured data set with 160 GHz channel spacing reached similar results. In summary, our model well characterizes the process variation of the wavelengths. The statistics of the random components in the model can be extracted from the wavelength data.

6.3 Optimal Assignment of Transmitters and Receivers

When the Tx and Rx in a transceiver are diced and separately packaged, Tx and Rx originally from different transceiver blocks could be matched to minimize the overall tuning power. Fig. 6.7 shows the schematic of separately packaged Tx and Rx connected

by an an off-chip fiber [2]. The five microrings in the Tx and the five microrings in the Rx need to be tuned as illustrated in Figs. 6.3 and 6.4. Due to fabrication process variations, the actual resonance wavelength of the microrings are random. Among a pool of fabricated Tx's and Rx's, we could optimally assign Tx to Rx to minimize the microring tuning power consumption.

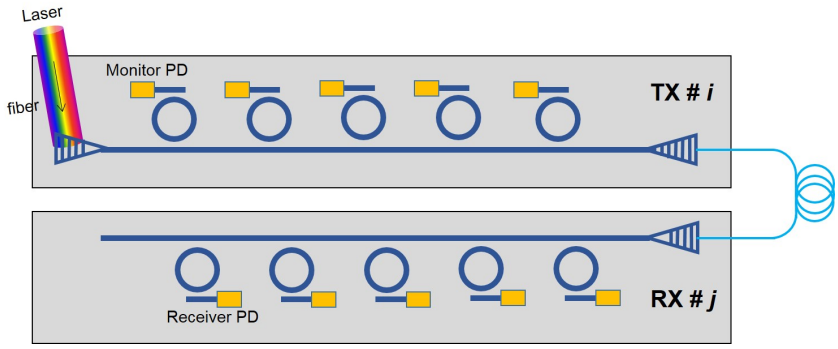


Figure 6.7: A schematic of an individual Tx connected to an individual Rx.

The optimal assignment procedure of Tx and Rx devices is as follows: the resonance wavelengths of Tx and Rx devices are measured after their fabrication. Then we construct a tuning cost matrix for a pool of n Tx devices and n Rx devices. The cost matrix element c_{ij} is the tuning cost of matching Tx $\#i$ with Rx $\#j$ that can be easily calculated from Fig. 6.4. In this way, this problem is formulated as a classical assignment problem and could be solved by Hungarian algorithm in $O(n^3)$ time.

This optimal assignment algorithm is tested on two batches of measured data sets. The optimal assignment results are shown in Table 6.1, assuming a heater efficiency of 0.15 nm/mW. The optimal assignment algorithm can gain some power savings compared to the local assignment scheme where each Tx is assigned to the local Rx in the same original transceiver.

We also test our assignment algorithm based on synthetic data sets. The synthetic

[2]could also be a polymer waveguide on board.

Table 6.1: Optimal Assignment of Tx to Rx using Realistic Data

Channel spacing (GHz)	Average tuning power per pair (mW) Local assignment	Average tuning power per pair (mW) Optimal assignment	Power saving (%)
80	25.7	24.1	6.2
160	24.7	21.3	13.8

data sets are randomly generated based on the established process variation model in Section 6.2.3. Table 6.2 summarizes the experimental results w.r.t various Tx and Rx numbers to be assigned. The power saving is calculated by comparing the optimal and local assignment results. Due to the random nature of the synthetic data sets, a number of synthetic data sets are tested for each configuration to achieve converged values of average power saving. Table 6.2 shows that the algorithm has comparable power saving on the synthetic data sets with the same number of devices as the realistic data sets. It also shows that greater power saving can be achieved when there are more devices.

Table 6.2: Optimal Assignment of Tx to Rx using Synthetic Data

Channel spacing (GHz)	Number of Tx and Rx	Power saving (%)
80	40	11.2
80	400	23.2
80	1000	25.8
160	31	14.4
160	301	27.1
160	1001	30.2

6.4 Optimal Pairing of Transceivers

When the fabricated transceiver block is inseparable and is packaged as a whole, there also exists optimization problem of forming transceiver pairs for optical links to minimize the overall tuning power. Here we consider the point-to-point (P2P) optical link as a

simple case. In a P2P link, two transceivers (# i and j) are paired as shown in Fig. 6.8, where the Tx in the transceiver # i (or j) is connected to the Rx in the transceiver # j (or i). The transceivers from a pool could be optimally paired to minimize the overall tuning power.

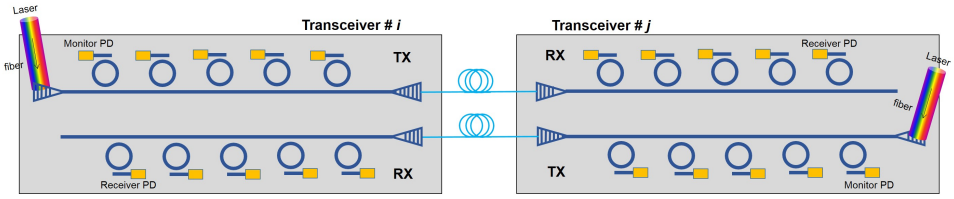


Figure 6.8: A schematic of two connected transceivers in a P2P link.

Different from the classical assignment problem, it is hard to find a polynomial time exact algorithm for this pairing problem. There is a dynamic programming algorithm based on the following equation: $d(S) = \min\{|T_iT_j| + d(S - \{T_i\} - \{T_j\})\}$, where $d(S)$ is the minimum total tuning power for the transceiver set S, and $|T_iT_j|$ is the tuning power for transceiver pair # (i, j). However, this dynamic programming algorithm fully explores the state space of $O(2^n)$, so its time complexity is also $O(2^n)$. Here we use

simulated annealing (SA) algorithm to tackle this problem as illustrated in Algorithm 1.

Algorithm 1: Simulated annealing algorithm for transceiver pairing

```
1  Construct the cost matrix based on the tuning cost for transceiver pair (i, j), i ≠ j
   in O(n^2) ;
2  Run greedy pairing algorithm: iteratively select the transceiver pair with the
   minimum tuning cost (O(n^3));
3  Use the greedy algorithm result as the initial pairing of the simulated annealing;
4  //Begin simulated annealing algorithm;
5  Set some SA algorithm parameters: initial and final temperature, cooling rate,
   number of loops per temperature;
6  temperature ← initialTemperature;
7  while temperature ≥ finalTemperature do
8      for i = 0 to loopNumPerTemperature do
9          Randomly select two pairs and shuffle the four transceivers;
10         Compute ΔE, the change of cost due to the shuffle;
11         if ΔE < 0 then
12             Accept the new pairing;
13         else
14             Accept the new pairing with probability of exp(−ΔE/kT);
15         end
16     end
17     temperature ← temperature × coolingRate;
18 end
19 Return the pairing with the minimum cost during the whole SA process;
```

In our experiments, we observed that the greedy algorithm could provide a fairly good pairing result, so the greedy algorithm result is used as the starting point for the

SA algorithm to shorten the execution time. However, the tuning power of the transceiver pairs in the greedy algorithm results tend to have large variances (shown by blue lines in Fig. 6.9). Since uniform product performance and power consumptions are desirable for industrial productions, we include the standard deviation of the transceiver pair tuning power in the cost function:

$$E = \mu(A) + \lambda_1 \sigma(A) \tag{6.4}$$

Where A is the vector of the tuning power of the transceiver pairs, and λ_1 is a weight coefficient for the standard deviation of the tuning power.

We run this SA-based algorithm on the two realistic data sets with the weight coefficient λ_1 swept from 0 to 2. The results are compared with the greedy algorithm as plotted in Fig. 6.9. The statistics of the algorithm results are summarized in Table 6.3, where the baseline, the nearest pairing scheme, naively pairs transceiver $\#(i, i+1)$ $(i = 1, 3, 5...)$ together. The results show that the SA algorithm greatly reduces the mean and variance of the tuning power compared to the naive nearest pairing scheme. In the SA algorithm, a larger weight λ_1 could result in a smaller tuning power variance at the cost of sacrificing the tuning power mean a little.

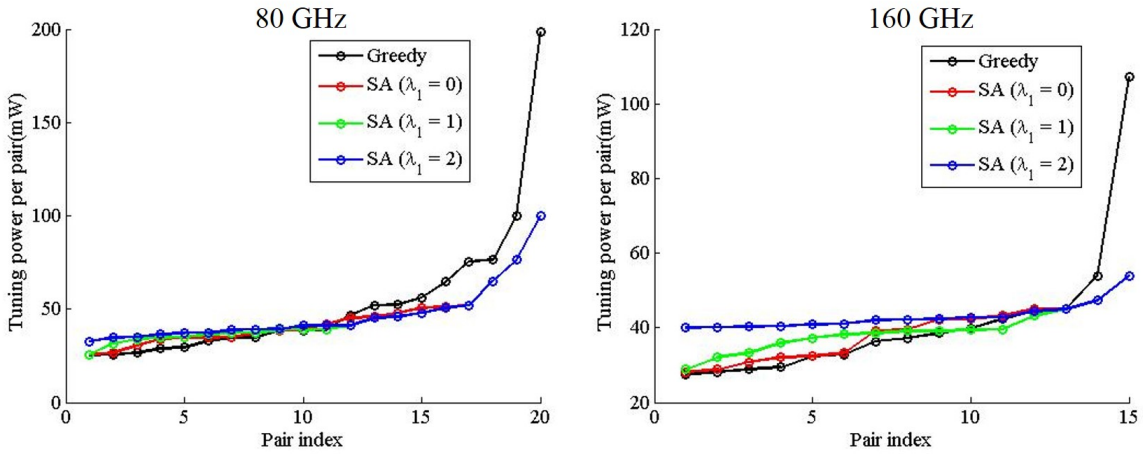


Figure 6.9: The results of SA and greedy algorithm on two realistic data sets.

Table 6.3: Optimal Pairing of Transceivers using Realistic Data

Channel spacing (GHz)	Algorithm & configuration	Power saving (%)	Std. Reduction (%)
80	Nearest pairing	0	0
80	Greedy	52.2	28.3
80	SA with $\lambda_1 = 0$	59.5	67.7
80	SA with $\lambda_1 = 1$	59.5	68.7
80	SA with $\lambda_1 = 2$	58.4	70.3
160	Nearest pairing	0	0
160	Greedy	55.1	70.0
160	SA with $\lambda_1 = 0$	58.1	88.3
160	SA with $\lambda_1 = 1$	57.5	90.5
160	SA with $\lambda_1 = 2$	53.6	94.5

The relative power savings here in Table 6.3 are much larger than the Tx/Rx assignment case in Table 6.1 in Section 6.3. This is because the baseline here, the scheme of pairing nearest transceiver block, involves inter-transceiver global variation. The pairs in the baseline scheme here are less spatially correlated than the baseline assignments in Section 6.3. Intuitively, the baseline here is expected to have worse performance than in Section 6.3, resulting in larger relative power savings.

The SA-based optimal pairing algorithm is also tested on synthetic data sets. The weight $\lambda_1 = 1$ in the SA algorithm. The device counts of 301 and 1001 are chosen to test the cases with odd device counts. The results are shown in Table 6.4, where the mean tuning power saving and power standard deviation reduction are calculated by comparing the SA and the nearest pairing results. Similar to the assignment algorithm for Tx and Rx, the TRx pairing algorithm also demonstrates better power saving with more devices. Also, the optimal pairing algorithm offers significant reduction in tuning power variance, yielding uniform power consumption of the transceiver products.

Table 6.4: Optimal Pairing of Transceivers using Synthetic Data

Channel spacing (GHz)	Number of TRx	Power saving (%)	Std. Reduction (%)
80	40	66.1	81.7
80	400	72.7	90.3
80	1000	75.4	77.1
160	31	60.8	78.8
160	301	66.3	87.1
160	1001	72.9	84.0

6.5 Summary

The resonance wavelengths of fabricated microrings would deviate from their nominal values due to process variations, which requires proper tuning to realign the wavelengths in an optical link. In this work, we have proposed optimal assignment and pairing algorithms for microring-based optical transceivers to minimize the tuning power. For the separable Tx and Rx case, the Hungarian algorithm finds the optimal assignment of Tx with Rx to minimize the tuning distance and power. For the case of inseparable transceiver-based P2P link, a simulated annealing-based algorithm is applied to achieve transceiver pairs with low and uniform tuning power. The two algorithms are tested on both measured data from batches of fabricated devices, and synthetic data sets based on well established models. The results of the algorithms show significant power saving compared to the nearest assignment or pairing scheme, and demonstrate excellent scalability w.r.t. the device count.

Chapter 7

Spatial Pattern Analysis of Process Variations in Silicon Microring Modulators

In this chapter, the measured wafer-scale process variation data of microring modulators are decomposed and analyzed, which provides useful insights for locating the process variation sources.

7.1 Introduction

As the dimensions of silicon photonic devices dive into submicron era, the device performance suffers from significant fabrication process variations. In order to better understand and further control and manage the process variations in fabrication process level, device design level and system design level, the process variations need to be systematically modeled.

The process variations have been studied in many previous work such as [98, 99],

which, however, did not systematically analyze the spatial patterns in the process variations. In this work, we quantitatively analyze the spatial patterns in the wafer-scale variations of microring modulators performance and local heaters resistance. The wafer-scale measured data is decomposed into two spatial pattern components, which are very valuable in analyzing the process variation sources and improving the fabrication steps.

7.2 Spatial Pattern Decomposition and Analysis

We first measure and then decompose the wafer-scale device characteristics. Though the resonance wavelength is a good fingerprint of the microring modulator, it requires additional efforts to track a specific resonance wavelength when the resonance wavelength drifts over one free spectral range (FSR) across the wafer. Therefore, as a proof of concept, we choose the electrical characteristics of the microring modulator that can be measured accurately and efficiently. We perform S11 test at 1 mA bias of the modulators. Then the S11 test data is fit into the small signal model in Fig. 2.11 with high accuracy to extract the model parameters, among which the R_D is plotted in Fig. 7.1.

The wafer-scale measured values are decomposed into the leveling component $ax+by$ and the radial component $c_1\sqrt{x^2+y^2}+c_2(x^2+y^2)$ as described by the following equation:

$$z_m(x,y) = ax + by + c_1\sqrt{x^2+y^2} + c_2(x^2+y^2) + d + \epsilon(x,y) \tag{7.1}$$

Where z_m is the measured value; x and y are the coordinates of the device-under-test (DUT) on the wafer with the wafer center as the origin; d is a constant representing the DC part in the measured value, which is included in the leveling component in the wafer-scale maps; ϵ is fitting error or the residual component. The weights of different components are evaluated by the variance of the component divided by the variance of the

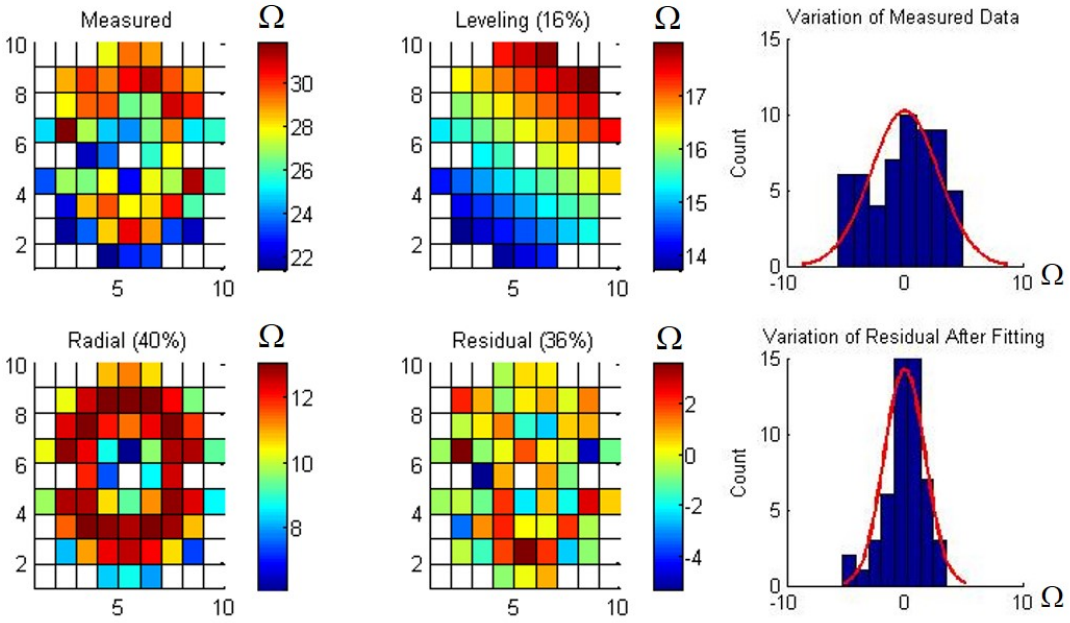


Figure 7.1: Measured value and decomposition results of the diode resistance R_D. The center die is burnt. The radial component is not rotationally symmetric with respect to the wafer center since the DUT deviates from the die center.

measured values. It should be noted that the sum of the weights of all the components is not necessarily one, because the leveling and radial components are not orthogonal basis.

Using the decomposition approach above, all the extracted model parameters in the small-signal model are well explained by the two spatial components. Here we plot R_D in 7.1 as a representative due to space limitation, which shows significant leveling and radial components.

The RC-limited 3dB bandwidth of the microring modulator is calculated based on the small signal model parameters [64], as plotted in Fig. 7.2, which shows significant radial component and some leveling component.

We measure the local heater resistance by I-V test across the same wafer as shown in Fig. 7.3, where three outlier dies are eliminated. Good probe contact is confirmed by repeated measurements with repeating error less than 1 Ω. The decomposition of heater resistance data shows a large radial component and a trivial leveling component.

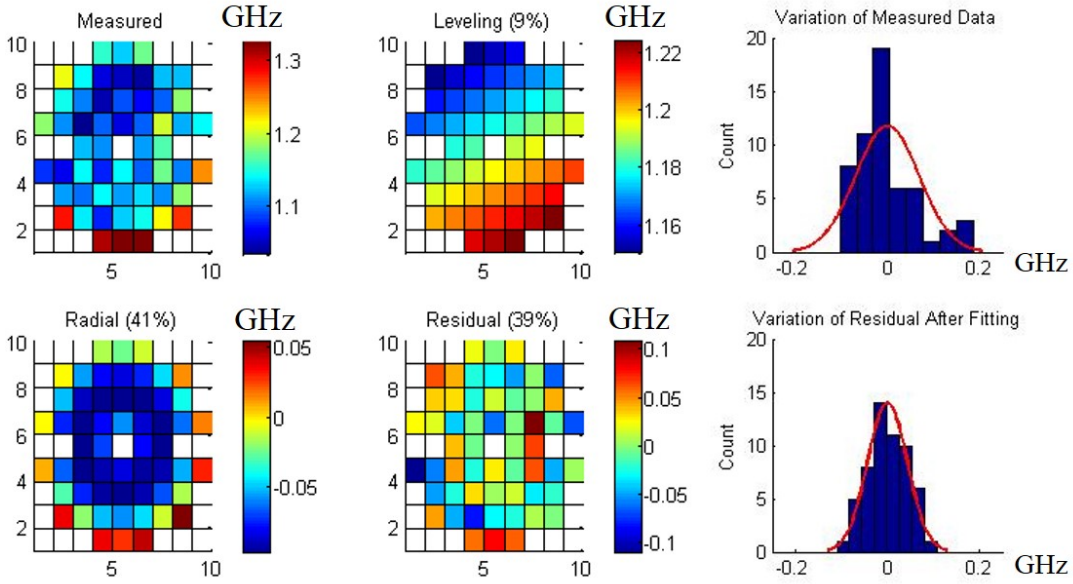


Figure 7.2: Measured value and decomposition results of the wafer-scale RC-limited bandwidth.

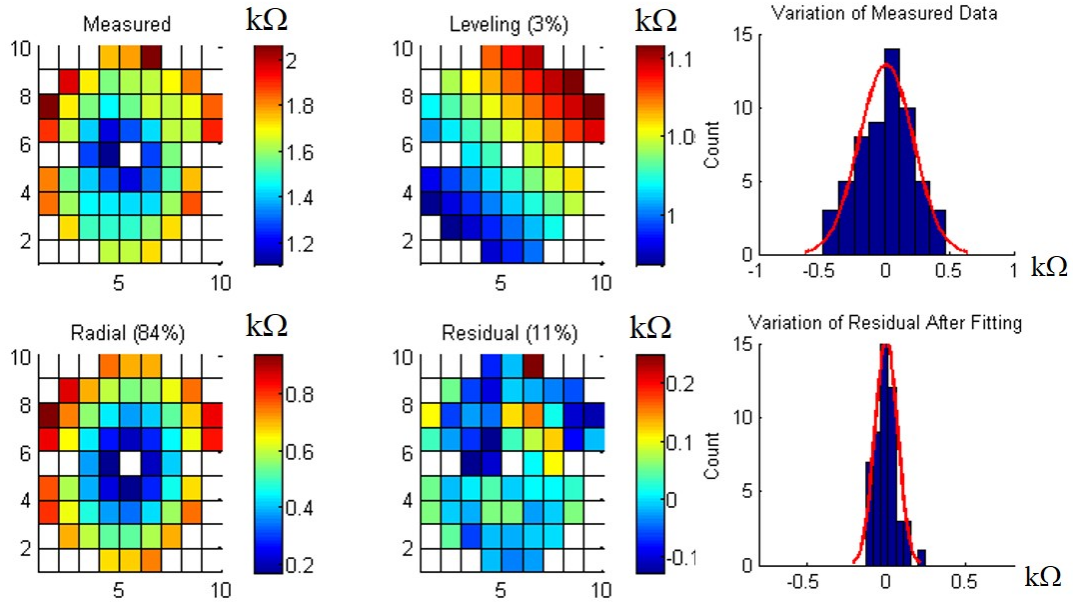


Figure 7.3: Measured value and decomposition results of the wafer-scale heater resistance.

7.3 Implications on Fabrication Process Steps

The variation decomposition results show that the leveling component in C_D and R_D are respectively 15% and 16%, which are much larger than that in the local heater resistance (3%). Comparing to the local heater with simpler geometry, the modulators PIN junction has additional dependencies such as the waveguide width (Fig. 1 ab). Therefore, the unique leveling component in the PIN junctions C_D and R_D is mainly introduced by the waveguide width variation, which is caused the imperfect leveling of silicon waveguide photomask during the lithography step.

Both the PIN junctions R_D and the heater resistance show significant radial pattern with higher resistance at the wafer edge. Additionally, the foundry measured SOI wafer thickness shows a radial pattern with 8 nm thicker at the wafer edge. Therefore, other contributors of the radial pattern, such as the silicon dry etch step and contact via etch step, also play important roles. Meanwhile, by noticing the weight percentages in Fig. 2, the contribution of the wafer thickness and the dry etch depth to the R_Ds total variation effect is about 2.5 times (40% : 16%) as large as that of the leveling of the silicon waveguide photomask.

7.4 Summary

We have decomposed the wafer-scale process variation data of microring modulators and local heaters into two spatial pattern components (leveling and radial). The electrical characteristics of the modulators PIN junction demonstrate both radial and leveling patterns, while the local heater resistances are dominated by radial pattern. The spatial pattern analysis implicates variation sources of waveguide photomask leveling, SOI thickness, and the dry etch depth.

This work is limited to wafer-scale global variations due to the small number of DUTs on a wafer. With more dedicated test structures in future fabrication runs, and optical spectrum measurements, we can expect more accurate and informative analysis of both global and local variations using this approach.

Chapter 8

Conclusions and Future Work

This thesis documents the efforts of compact modeling, circuit simulation, and variation management of nanophotonic interconnects. The key contributions and findings are as follows.

Microring modulators are extensively studied and modeled in various aspects including its device design space, electrical and optical properties, and its dynamic behavior. The models for various aspects are compiled into a comprehensive model, which is then used in circuit-level simulations. Components in a heterogeneous silicon optical NoC are also compactly modeled. We have performed circuit-level simulations of a microring-based transceiver and a heterogeneous optical link in Cadence. The simulation results show excellent agreement with measurements, and demonstrate the electro-optical co-simulations and photonics-aware design space explorations.

Observing the significant process variations of Q factor and extinction ratios in microrings, the adaptive tuning technique has been proposed to allocate just enough power for the fabricated links. The adaptive tuning saves the receiver power consumption and scales well w.r.t variation ranges, NoC sizes, and laser types. We have also designed optimization algorithms to mix-and-match the microring-based devices to minimize the

tuning distance and power in each link. The optimal pairing algorithms demonstrate good performance and scalability on both measured and synthetic wavelength data sets. To characterize the spatial patterns of the process variations, we have decomposed the wafer-scale process variation data of microring modulators. The resulting spatial patterns are explained by certain fabrication process steps, which is helpful in process debugging and improvement.

The future work can include:

- Enrich and improve the photonics device model library: model more types of photonic components; include the device design parameters in the model to facilitate early state design space explorations of PICs; add more photonics-specific information to the model description (e.g., phase, noise, chirp, etc.)

- Co-simulate the photonic device models with realistic CMOS circuits: simulate realistic CMOS driver circuits with photonic devices to study their interactions and co-optimizations.

- Study the device mix-and-match problem in more complex situations: consider the tuning of not only transmitters and receivers but lasers; optimally arrange optical devices in network architectures with optical switches.

- Perform more variation-aware system-level and architectural study of optical interconnects and NoC based on the well established compact device models and variation models.

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