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Low-Temperature Growth of Tellurium for Electronic

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Low-Temperature Growth of Tellurium for Electronics

By
Chunsong Zhao

A dissertation submitted in partial satisfaction of the
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Professor Felix Fischer

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Abstract of the dissertation

Low-Temperature Growth of Tellurium for Electronics

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Chunsong Zhao

Doctor of Philosophy in Materials Science and Engineering

University of California, Berkeley

Professor Ali Javey, Jie Yao (Co-chairs)

Large-scale growth of high-quality semiconductors forms the basis of the modern electronics. Growth of high-quality semiconductors such as Si typically requires a high processing temperature, which cannot meet the fabrication thermal budget for the emerging circuit architectures and applications such as three-dimensional (3D) monolithic integration and flexible electronics. Great effort has been devoted to exploration of low temperature material systems with sufficient mobility in last decades. Although low-temperature grown n-type films such as indium gallium zinc oxide (IGZO) with respectable electron mobility have been shown, the development of their p-type thin-film counterpart with sufficiently high hole mobility is still limited. In this report, we identify the elemental p-type semiconductor-Tellurium (Te) as a promising candidate due to its high hole mobility, low processing temperature and possibility for wafer-scale production.

Specifically, the wafer-scale growth of Te thin films was realized through thermally evaporated at cryogenic temperatures, field effect transistors (FETs) based on which exhibited respectable electrical properties. 3D monolithic circuits and devices on flexible substrates were fabricated using the evaporated Te thin films, demonstrating that Te is a promising p-type semiconductor processed at low temperatures.

After that, we systemically studied the growth mechanism of the thermally evaporated Te thin films, which has an intriguing amorphous to crystalline phase transition at near-ambient temperature. We visualized and modeled the kinetics and dynamics of the crystallization of thermally evaporated Te films and achieved the growth of Te thin films with large grains and patterned Te single crystal arrays by optimizing the crystallization temperature, which possess an enhanced crystallinity and electrical properties.

Additionally, orientated growth of ultrathin tellurium was investigated, as Te has attractive orientated and thickness-dependent properties. Two-dimensional (2D) formed Te and SeTe alloys were realized on the three-fold symmetric transition metal dichalcogenides substrates (WSe_2, WS_2, $MoSe_2$ and MoS_2) by van der Waals epitaxy, forming a one-dimensional/2D moiré superlattice, where the chains were aligned to the armchair directions. Further, growth of single-crystal-textured Te film was demonstrated on the low-symmetric surface of WTe_2.

Finally, we investigated the thermal stability of Te based devices, which is a major drawback for their practical applications. Two failure mechanisms related to the sublimation of Te channel and the degradation of the contacts were raised. To address these issues, we applied graphene contact and SiO_x encapsulation, which is able to keep the contacted stable and channel intact at high temperatures. Such devices have the similar effective mobility comparing to the traditional metal contacted ones', but with an improved thermal stability.

To my family

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Chapter 4 is a slightly modified version of "Orientated Growth of Ultrathin Tellurium by van der Waals Epitaxy" which is still under review at the time of submission.

Chapter 5 is a slightly modified version of "Thermal stability for Te-based devices" published in Applied Physics Letters (2020). Reproduced from (Zhao, C., Hurtado, L. and Javey, A., 2020. Thermal stability for Te-based devices. Applied Physics Letters, 117(19), p.192104.), with the permission of AIP Publishing.

CHAPTER 1

Introduction

1.1 Need for low-temperature processed semiconductors

Silicon (Si), the most widely used elemental semiconductor, has been the foundation of the modern electronics since 1950's. However, the current traditional material (Si) system and its corresponding manufacturing process are not fully compatible with some emerging chip architectures or application areas such as monolithic three-dimensional (3D) complementary metal-oxide-semiconductor (CMOS), and transparent/flexible electronics. One of the major challenges is that the processing temperature for conventional materials exceed the thermal budget of the substrates. Specifically, the processing temperature for constructing monolithic 3D CMOS, where multiple active circuit layers are stacked on top of each other, needs to be maintained below 300-400 ℃ to prevent degradation of the underlying devices and interconnects. The thermal budget needs to be even lower (below 200 ℃ or even less) for flexible electronics due to low glass transition temperatures of polymer substrates (for example, the maximum stable temperature of polyethylene terephthalate (PET) is around 150 ^{o}C)[1-3]. However, for the wafer-scale growth of high-quality semiconductors, the processing temperatures are typically over 600 ^{o}C; and the materials grown at low-temperature cannot maintain their inherent electrical properties, which largely limits their application space. Therefore, exploring low-temperature (400 ^{o}C or lower) processed semiconductors with high device performance is critical and challenging for the semiconductor industry.

Part of the following subchapter has been previously published in a similar format in: Zhao, C., Tan, C., Lien, D.H., Song, X., Amani, M., Hettick, M., Nyein, H.Y.Y., Yuan, Z., Li, L., Scott, M.C. and Javey, A., 2020. Evaporated tellurium thin films for p-type field-effect transistors and circuits. *Nature nanotechnology*, 15(1), pp.53-58.

1.2 Status of the current low-temperature processed semiconductors

Great effort has been devoted in exploring any promising material system in the past decades. Multiple *n*-type material systems with respectable electron mobility on the order of 10 $cm^2V^{-1}s^{-1}$ such as *a*-IGZO, *a*-ZnO, ITO, InO_x, CdS and CdSe[4-8], have been identified, but the development in their *p*-type counterparts has been still limited despite many years of efforts. Widely explored low-temperature processing *p*-type thin films are amorphous Si, metal oxides (e.g. CuO_x, NiO_x and SnO_x), organic compounds/polymers and polycrystalline germanium (Ge)[9-12]. Among them, amorphous Si, metal oxides and organic compounds/polymers normally exhibit low hole mobilities on the order of 1 $cm^2V^{-1}s^{-1}$ or even less[2, 9, 10, 13, 14]. Vapor phase-deposited polycrystalline Ge films give high hole mobility up to 110 $cm^2V^{-1}s^{-1}$. However, its application is limited by the need of sequential annealing and/or metal catalysts to induce the crystallization[11]. Alternatively, carbon nanotubes (CNTs) have been explored as a promising *p*-type nanomaterial and solution-processed CNT-based networks exhibit hole mobility of up to tens of $cm^2V^{-1}s^{-1}$. However, their nanoscale processing remains a concern[3, 15-18]. In addition, layer transfer of high-

temperature grown materials such as chemical vapor deposition (CVD)-grown CNT arrays and III-V has also been explored, but their large-scale processing is still a challenge[1, 19, 20].

In summary, several n-type materials with acceptable electrical properties, which can be grown at low temperature in wafer scale, has been raised, but a promising p-type counterpart is still lacking due to the limitation in electrical performance and/or large-scale processing. Therefore, exploring a promising p-type material system with respective electrical properties and developing its corresponding low-temperature and wafer-scaled fabrication method is critical.

Part of the following subchapter has been previously published in a similar format in: Tellurium Single-Crystal Arrays by Low-Temperature Evaporation and Crystallization; Zhao, C., Hurtado, L. and Javey, A., 2020. Thermal stability for Te-based devices. *Applied Physics Letters*, 117(19), p.192104.

1.3 Tellurium as a promising candidate

Te is composed of covalently-bonded atoms sequenced in a helical chain along a single axis, with chains packed in a hexagonal array *via* van der Waals force (Fig. 1a). It is an intrinsically *p*-type semiconductor due to the native defects like vacancies. Recently, solution grown single-crystalline tellurium (Te) nanosheets exhibit high device performance with hole mobilities up to hundreds $cm^2V^{-1}s^{-1}$ and the on/off current ratio over 10^4. On the other hand, large-scale polycrystalline Te thin films with tens of nanometer thickness prepared by thermal evaporation were studied in 1960-70s, but the device performance especially on/off current ratio was poor. Accordingly, we identify Te is a promising candidate as a low-temperature grown semiconductor for large-scale high-performance *p*-type transistor applications, since its single crystals exhibit high device performance and crystalline films could be grown at near ambient temperature. Such advantages of tellurium drive us to develop a strategy for Te film growth and device fabrication to realize low-temperature grown high-performance transistors.

Bulk Te has a narrow bandgap of 0.31 eV, which determines the high off-state carrier concentration at room temperature and causes the low on/off current ratio, which was the main issue of evaporated Te based transistors. The weak electrostatic gate control for thick Te films could also cause a large off-state leakage current. Large carrier concentration created by the high defect and impurity densities could decrease both mobility and on/off current ratio. Accordingly, (1) enlarging the bandgap, (2) increasing electrostatic gate control (3) improving the quality of the materials are the directions for optimizing the evaporated Te films to improve the device performance. It is well known that the bandgap of semiconductors can be tuned by tuning geometry of the materials due to the quantum confinement effect, which is observed in many material systems. The thickness-dependent bandgap for tellurium is also calculated in recent studies, which tell us that the bandgap of tellurium could be enlarged from 0.31 eV to 1.0 eV by decreasing the thickness from bulk to monolayer. Additionally, as the thickness of Te is thinner, the leakage current path will be less, which suppresses the off-current level and improves the switching performance further. Theoretically, it is possible to realize high performance Te devices with acceptable on/off current ratio by making ultrathin Te films, since thinner Te films have the larger bandgap and stronger electrostatic gate control. Therefore, in chapter two, I will fabricate wafer-

scale ultrathin Te thin films by a low temperature thermal evaporation method, and demonstrate the respective device performance of Te and its broad application potential in 3D monolithic integrated circuits and flexible electronics.

Film quality has a critical influence on the electrical properties, for example, the amorphous semiconductors always have a significant lower device performance comparing to the crystalline ones. The imperfects inside the crystalline materials like impurities, defects and grain boundaries could largely affect the carrier mobility and switching performance. Te thin films with tens of nanometer thickness prepared by thermal evaporation were studied in 1960-70s[21-23]. Polycrystalline Te films were deposited, and material quality (*i.e.*, grain size) and transport properties (*i.e.*, carrier mobility) of the evaporated Te films could be tuned by substrate temperature[22], nucleation layer[24, 25] and deposition rate[24, 25]. Specifically, the grain size strongly depends on the deposition temperature with the maximum size obtained at cryogenic temperatures[22]. Optimized evaporated Te films have shown high Hall mobility (up to a few hundred $cm^2V^{-1}s^{-1}$)[21, 22]. Although the grain size and mobility of the evaporated Te films were optimized by controlling the deposition temperature, the underlying mechanism has not been fully investigated and understood. Thermally evaporated tellurium has an intriguing crystallization behavior, where an amorphous to crystalline phase transition happens at near-ambient temperature. However, a comprehensive understanding and delicate control of the crystallization process for the evaporated Te films is lacking. In chapter three, we visualize and model the kinetics and dynamics of the crystallization of thermally evaporated Te films. The understanding so obtained is then used to fabricate large grain Te films (average grain area of 150 μm^2) with preferred (100) out-of-plane orientation at low temperatures. Te single crystal arrays (lateral dimension as large as 6 μm) were also realized on various substrates by patterned thermal evaporation and low-temperature crystallization.

Te also has intriguing anisotropic physical properties owing to its inherent one-dimensional crystal structure. Although tellurium nanosheets and ultrathin films with high crystallinity and electronic properties have been achieved, the in-plane orientation of the domains on the substrate was random, which impedes the utilization of the anisotropic properties of Te. In chapter four, we systemically investigated the van der Waals epitaxy growth of Te on the surface of transition metal dichalcogenides. Orientated growth of two-dimensional Te with a thickness down to 5 nm was realized on the three-fold symmetric substrates (WSe_2, WS_2, $MoSe_2$ and MoS_2), where the atomic chains of Te are aligned with the armchair directions of substrates. This method was extended to the growth of SeTe alloys, providing flexibility for band alignment of Te based heterostructures. Growth of single-crystal-textured Te film has been demonstrated on the low-symmetric surface of WTe_2.

Lastly, in chapter five, I will be focusing on the thermal stability of Te based devices. Although Te is attractive semiconducting material for a wide range of electronic and optoelectronic applications, thermal instability of Te-based devices introduces major drawback for their practical applications. Therefore, in chapter five, we will explore the influence of annealing temperatures on Te transistors and their two failure mechanisms, related to the sublimation of Te channel and

the degradation of the contacts. To overcome these challenges, we fabricated a Te device which is graphene-contacted and SiO_x-encapsulated such that the Te channel and the contacts remain intact and stable at high temperatures, making it suitable for practical usage.

1.4 References

[1] M. M. Shulaker, G. Hills, R. S. Park, R. T. Howe, K. Saraswat, H.-S. P. Wong, S. Mitra, *Nature* **2017**, 547, 74.

[2] J. Kwon, Y. Takeda, R. Shiwaku, S. Tokito, K. Cho, S. Jung, *Nature Communications* **2019**, 10, 54.

[3] H. Chen, Y. Cao, J. Zhang, C. Zhou, *Nature Communications* **2014**, 5, 4097.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, 432, 488.

[5] T. Rembert, C. Battaglia, A. Anders, A. Javey, *Advanced Materials* **2015**, 27, 6090.

[6] H.-I. Yeom, J. B. Ko, G. Mun, S.-H. K. Park, *Journal of Materials Chemistry C* **2016**, 4, 6873.

[7] V. H. Martinez-Landeros, N. Hernandez-Como, G. Gutierrez-Heredia, R. Ramírez-Bon, M. Quevedo-Lopez, F. S. A. Tostado, *Semiconductor Science and Technology* **2018**.

[8] F. S. Stinner, Y. Lai, D. B. Straus, B. T. Diroll, D. K. Kim, C. B. Murray, C. R. Kagan, *Nano letters* **2015**, 15, 7155.

[9] Z. Wang, P. K. Nayak, J. A. Caraveo-Frescas, H. N. Alshareef, *Advanced Materials* **2016**, 28, 3831.

[10] H. Sirringhaus, *Advanced Materials* **2014**, 26, 1319.

[11] D. Shahrjerdi, B. Hekmatshoar, S. Mohajerzadeh, A. Khakifirooz, M. Robertson, *Journal of Electronic Materials* **2004**, 33, 353.

[12] M.-G. Kim, M. G. Kanatzidis, A. Facchetti, T. J. Marks, *Nature Materials* **2011**, 10, 382.

[13] E. Fortunato, P. Barquinha, R. Martins, *Advanced Materials* **2012**, 24, 2945.

[14] M. J. Powell, *IEEE Transactions on Electron Devices* **1989**, 36, 2753.

[15] M. L. Geier, J. J. McMorrow, W. Xu, J. Zhu, C. H. Kim, T. J. Marks, M. C. Hersam, *Nature Nanotechnology* **2015**, 10, 944.

[16] H. Park, A. Afzali, S.-J. Han, G. S. Tulevski, A. D. Franklin, J. Tersoff, J. B. Hannon, W. Haensch, *Nature Nanotechnology* **2012**, 7, 787.

[17] B. Chen, P. Zhang, L. Ding, J. Han, S. Qiu, Q. Li, Z. Zhang, L.-M. Peng, *Nano Letters* **2016**, 16, 5120.

[18] Q. Cao, S.-j. Han, G. S. Tulevski, Y. Zhu, D. D. Lu, W. Haensch, *Nature Nanotechnology* **2013**, 8, 180.

[19] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, *Nature* **2010**, 468, 286.

[20] J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, J. A. Rogers, *Science* **2006**, 314, 1754.

[21] R. W. Dutton, R. S. Muller, *Proceedings of the IEEE* **1971**, 59, 1511.

[22] K. Okuyama, Y. Kumagai, *Journal of Applied Physics* **1975**, 46, 1473.

[23] P. Weimer, *Proceedings of the IEEE* **1964**, 52, 608.

[24] K. Okuyama, H. Yamamoto, Y. Kumagai, *Journal of Applied Physics* **1975**, 46, 105.

[25] R. Dutton, R. Muller, *Thin Solid Films* **1972**, 11, 229.

CHAPTER 2

Thermally Evaporated Tellurium Thin Films for p-Type Field Effect Transistors and Circuits

2.1 Introduction

Recently, single-crystalline tellurium (Te) nanostructures with a bandgap E_g = 0.31 eV have been shown to exhibit high hole mobilities up to 707 $cm^2V^{-1}s^{-1}$, but their large-scale processing is challenging, hence limiting their applications[1, 2]. On the other hand, large-scale polycrystalline Te thin films with tens of nanometer thickness prepared by thermal evaporation were studied in 1960-70s[3-5]. Optimized evaporated Te films have shown high Hall mobility (up to a few hundred $cm^2V^{-1}s^{-1}$)[3, 4]. However, the device performances were very poor (I_{on}/I_{off} of ~8 times on/off current ratio) with poor subthreshold swing (Figure R1). As a result, the research in the field stopped and the material became largely forgotten and obsolete. The reason for the poor on/off current ratio in previous studies is that they focused on thick films (tens of nanometers to few micrometers), whose bandgap is small (Eg = 0.31 eV) and electrostatic control from the gate is weak. Here, by making the Te films very thin (thus enlarging the bandgap and improving the gate coupling to reduce the off-state current leakage paths), by optimizing the processing conditions of Te evaporation (including deposition temperature and rate), and by incorporating ALD high-k gate dielectrics, we demonstrate for the first time transistors with performances (effective hole mobility of ~35 $cm^2V^{-1}s^{-1}$, on/off current ratio of ~10^4 and subthreshold swing of 108 $mVdec^{-1}$) that meet many application criteria, including for flexible/glass electronics and possibly for 3D monolithic CMOS. Based on the low temperature processed high-performance Te, we demonstrate the fabrication of various logic gates and circuits, with proof-of-concept demonstrations of monolithic 3D integration and mechanically flexible devices. This work addresses the issues of the forgotten material, evaporated tellurium film, and shows the evaporated Te film can potentially be a good candidate for low temperature p-type semiconductors.

2.2 Te thin film synthesis and characterization

Te is composed of covalently-bonded atoms sequenced in a helical chain along a single axis, with chains packed in a hexagonal array via van der Waals force (Figure 2.2.1a). Te thin films were deposited in an Edwards Coating System (E306A thermal evaporator system) with a base pressure about 1.5×10^{-6} mbar. Te pellets (99.999%, Sigma-Aldrich) were used as the thermal evaporation source. When the pressure reached 2×10^{-6} mbar, the substrate temperature was reduced to -80 ℃ by cooled nitrogen gas flow prior to the evaporation. The evaporation rate was controlled to be around 10 $Å s^{-1}$ for all the evaporations. The thickness of Te thin film was monitored by during deposition. After evaporation, the samples were taken out after the substrate temperature recovered to room temperature. All the Te thin films studied were prepared under these conditions except Te thin films evaporated at different substrate temperatures.

Domains with different contrast were observed under polarized light microscopy (Figure 2.2.1b and Figure 2.2.2). The domains correspond to the arrays of aligned Te molecular chains, acting like wire grid polarizers, with absorption dependent on the angle between the light polarization and the array. To further confirm the crystal structure of different domains, TEM was performed (Figure 2.2.1c). The selected-area electron diffraction (SAED) patterns of two regions with different contrast show single-crystalline diffraction spots with different orientations, suggesting that both regions are single-crystal-like domains (Figure 2.2.1d). The high-resolution transmission electron microscopy (HRTEM) image clearly shows the grain boundary of the two domains (Figure 2.2.1e). Note that defects can be observed from the HRTEM image (Figure 2.2.3), suggesting that domains are not perfect single crystals.

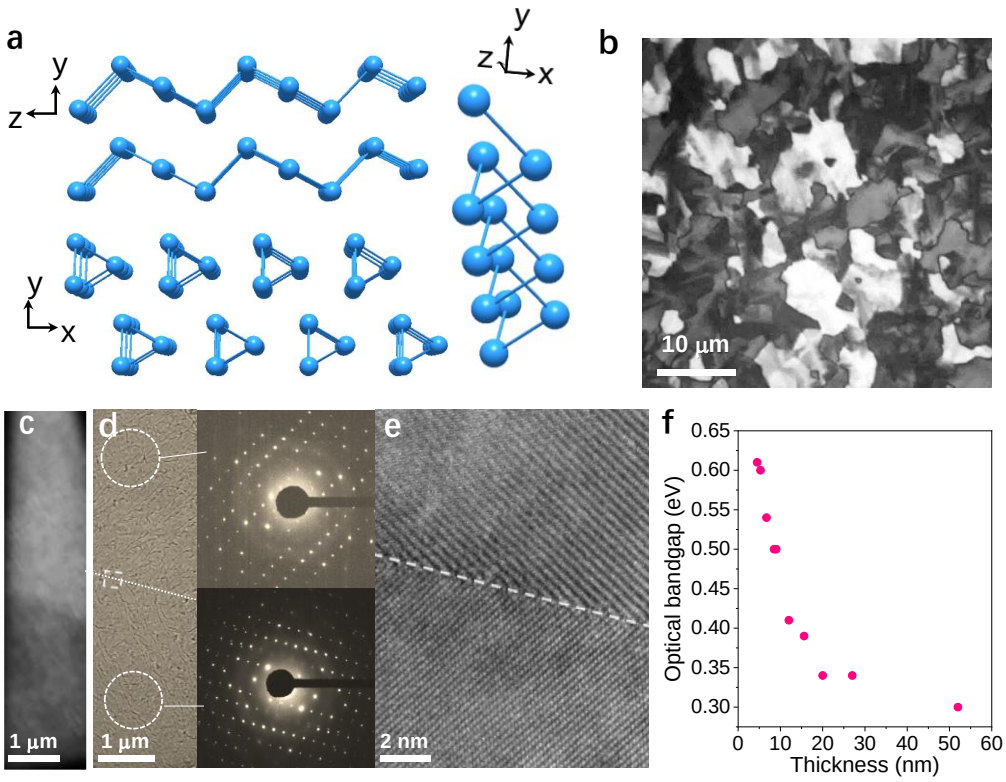


Figure 2.2.1 | Characterization of Te thin films evaporated with a substrate temperature of -80 ºC. a, Crystal structure of Te. **b**, Polarized light microscopy image of a Te film (9 nm). **c,** Zoom-in optical image of a Te film (9 nm) on SiO_2 TEM grid, depicting a grain boundary. **d**, The low magnification TEM image of the Te film (9 nm) in **c**. The dash line indicates the grain boundary. Insets are the corresponding SAED patterns of selected areas. **e**, HRTEM image of the same film at the boundary area. **f**, Thickness-dependent optical bandgap of Te thin films.

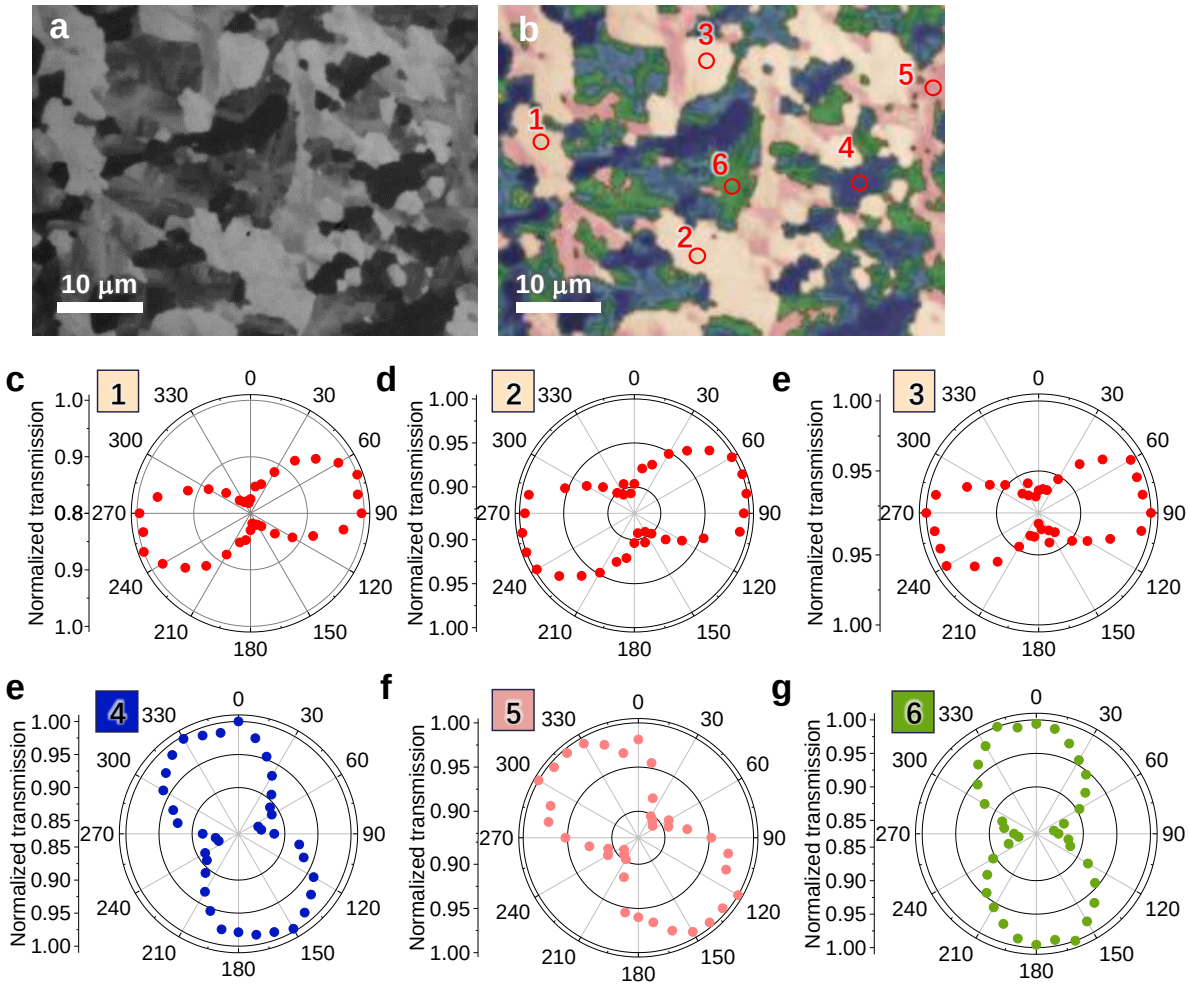


Figure 2.2.2 | **a**, The polarized light microscopy image of 9 nm Te film on quartz evaporated with a substrate temperature of -80 ºC. **b**, The corresponding false-color polarized light microscopy image of **a**. **c-e**, The polar plots of normalized polarization-resolved transmission intensity at 550 nm from the labelled domains in **b**. **e-f**, The polar plots of normalized polarization-resolved transmission intensity at 550 nm from domains with the corresponding color in **b**. **Note**: Figure 2.2.2 shows a polarized light microscopy image of 9 nm Te film with a smooth surface on quartz evaporated with a substrate temperature of -80 ºC. Supplementary Fig. 1b shows the corresponding false- color polarized light microscopy image in a, in which the domains with different labeled with different colors. Supplementary Fig. 1c shows polar plots of normalized polarization-resolved transmission intensity at 550 nm from domains with the same color in b, which clearly presents that they have almost the same orientations. Supplementary Fig. 1d-f show the polar plots of polarization-resolved transmission intensity at 550 nm from with the corresponding color in e, which clearly presents that the domains with different colors have the different crystal orientations. The polarization-resolved transmission analysis can support that the contrast differences observed in polarized light microscopy images come from the gains with different crystal orientations.

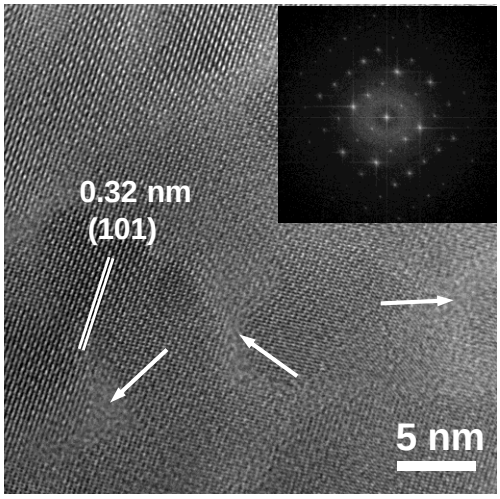


Figure 2.2.3│ HRTEM image of a Te thin film (9 nm) evaporated with a substrate temperature of -80 ºC. Inset is the corresponding Fourier transform. The measured lattice distance is 0.32 nm, corresponding to the (101) planes of Te crystal.

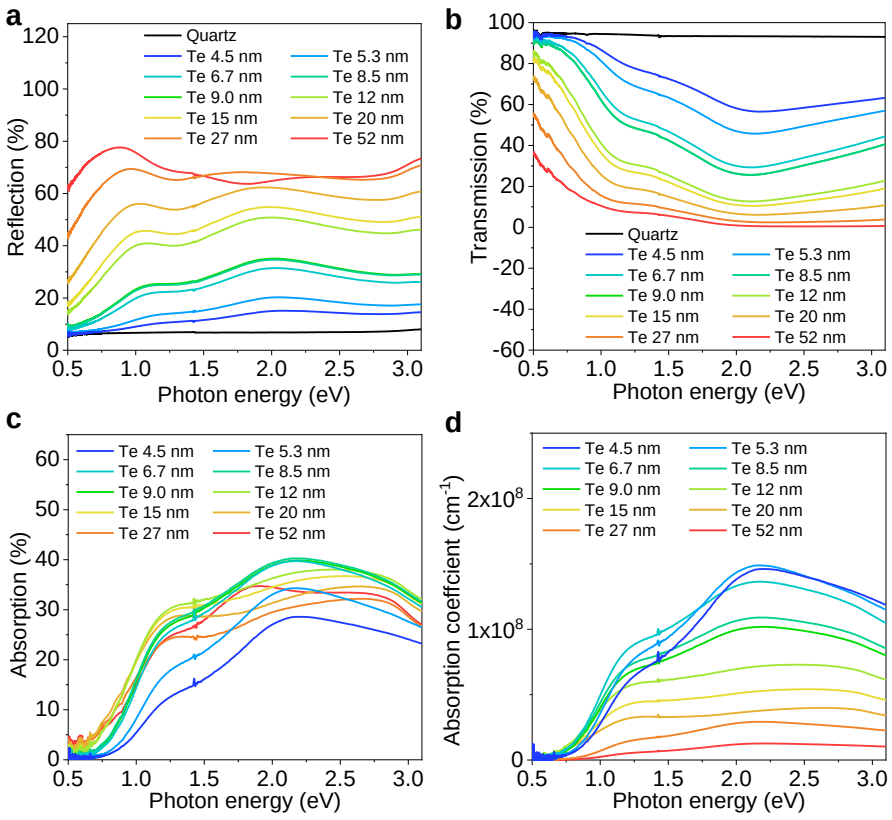


Figure 2.2.4│ **Thickness-dependent optical properties of Te thin films evaporated with a substrate temperature of -80 ºC. a-c**, Reflection (**a**), transmission (**b**) and absorption (calculated as 100%-R-T) (**c**) of the evaporated Te films with varying thickness. **d,** Thickness-dependent absorption coefficient of evaporated Te films calculated from the data shown in panel **c**. The thicknesses are measured by AFM.

We first investigate the thickness effect on the domain size of Te films evaporated with a substrate temperature of -80 ºC. Te films with thickness varying from 8 to 30 nm were analyzed using the polarized light microscope. We observed minimal thickness dependence for the domain size for the studied thickness of 8 to 30 nm. The extracted optical bandgap from the absorption measurements shows a thickness-dependent behavior, from 0.3 eV for bulk to 0.6 eV for 4.5 nm-thick evaporated Te films (Figure 2.2.1f and Figure 2.2.4) due to quantum confinement effect. Our results are consistent with the previously reported calculations [6] and experimental results on single-crystalline Te layers [7].

We also found that the substrate temperature for evaporation has significant impact on the Te film quality. When the substrate temperature decreases from -10 ºC to -60 ºC, the average area of domains monotonically increases from ~3 μm^2 to ~25 μm^2 (Figure 2.2.5-2.2.7). Below -60 ºC, the domain size does not change with further decrease of temperature. At room temperature (the substrate temperature of 25 ºC), the film is not continuous and instead consists of small nanoparticles (Figure 2.2.8).

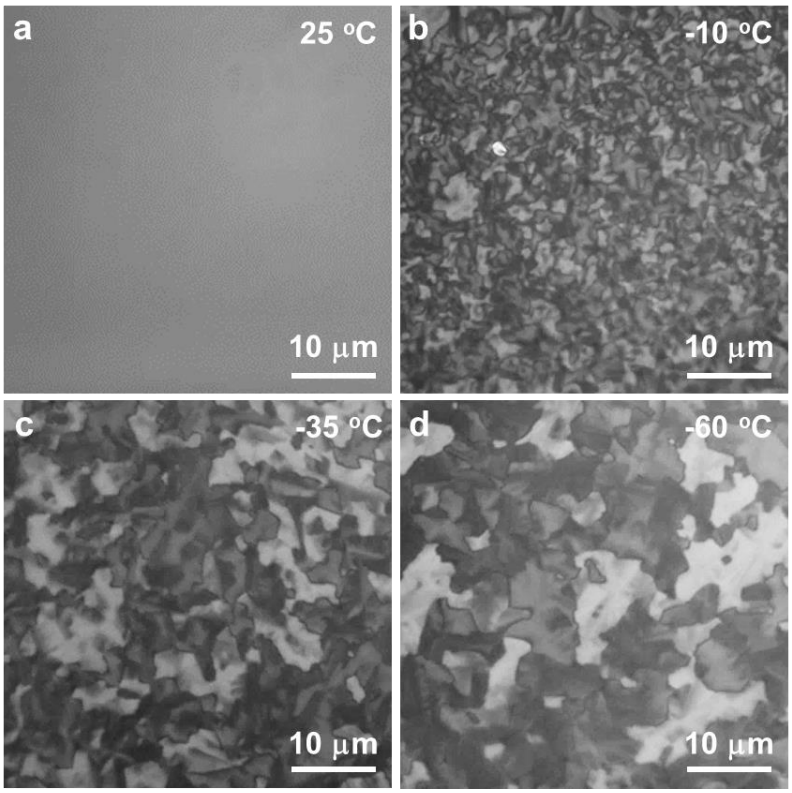


Figure 2.2.5│ Polarized light microscopy images of Te films (9 nm) evaporated with different substrate temperatures: **a**, 25 ºC; **b**, -10 ºC; **c**, -35 ºC; **d**, -60 ºC.

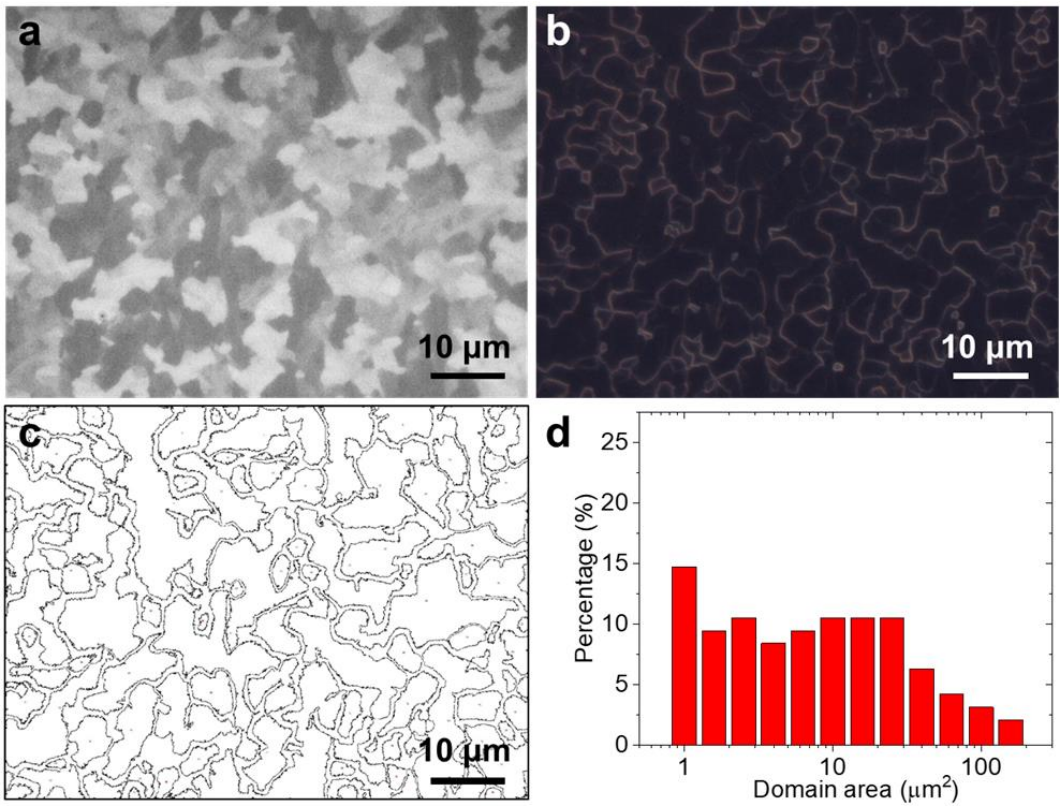


Figure 2.2.6 | **a**, The optical microscopy image of Te film (9 nm) evaporated with a substrate temperature of -80 °C. **b**, The corresponding dark-field optical microscopy image of **a**. **c**, The extracted domains from the dark field optical microscopy image in **b**. **d**, The histogram profile of the domains area calculated from **c**.

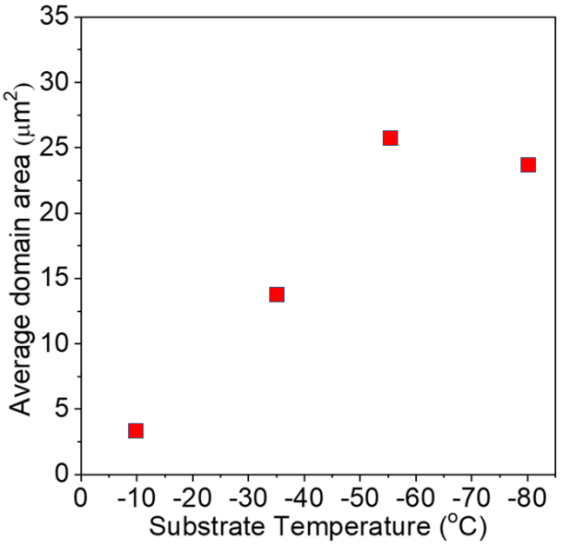


Figure 2.2.7 | The calculated average domain areas of Te films (8 nm) evaporated with different substrate temperatures.

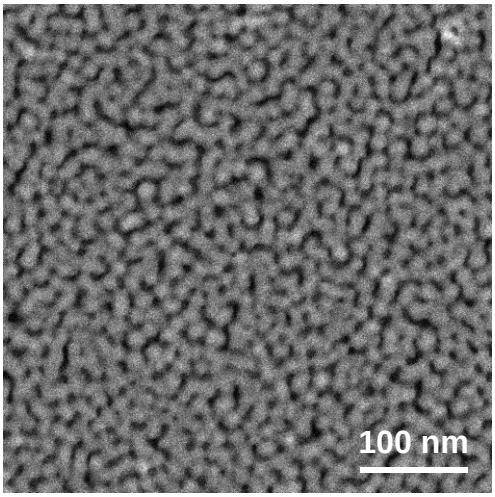


Figure 2.2.8 | The STEM image of Te film (9 nm) evaporated on a room temperature substrate.

2.3 Electrical characterization of Te field-effect transistors

The evaporation temperature effect on the device performance of Te FETs is explored given its significant impact on the domain size. We fabricate FETs based on Te films (8 nm) evaporated at different temperatures from 25 °C to -80 °C. The device structure consists of a Ti/Au local bottom gate, a 5-nm ZrO_2 ($\varepsilon \approx 16$) gate dielectric (Figure 2.3.1a), and Ni as source/drain metal contacts. The effective mobility decreases from 35 to 10 $cm^2V^{-1}s^{-1}$ with the increase of the substrate temperature (Figure 2.3.2). The higher mobility for FETs based on Te thin film evaporated at -80 °C can be mainly attributed to larger domain size as compared to those deposited at higher temperatures[4]. To this end, we use Te films evaporated with a substrate temperature of -80 °C for subsequent device and circuit fabrication.

Uniform Te FETs can be easily fabricated at wafer scale given the simplicity of the Te deposition (Figure 2.3.1b). Te FET shows a typical *p*-type characteristic as shown in Figure 2.3.1b and c. A hysteresis in the voltage sweep measurement is observed which is a common behavior for a thin film device without encapsulation. The transistor exhibits an effective hole mobility of ~35 $cm^2V^{-1}s^{-1}$, on/off current ratio of ~10^4 and subthreshold swing (SS) of 108 $mVdec^{-1}$ at room temperature (Figure 2.3.1d and e). To study the uniformity of Te FETs, we randomly measured 60 devices on a wafer. The devices exhibit a narrow distribution in performance with standard deviation of 32±7 $cm^2V^{-1}s^{-1}$ in mobility, 9491±4765 in on/off current ratio, and 114±9 $mVdec^{-1}$ in SS (Figure 2.3.1f-h), Importantly, the performance of Te FET did not show obvious degradation after leaving the device in ambient air without any encapsulation for 30 days (Figure 2.3.1i). Temperature-dependent I_d-V_g transfer curves are measured to investigate the carrier scattering mechanisms (Figure 2.3.3a). The effective mobility is nearly independent of temperature from 77 K to 300 K (Figure 2.3.3b), suggesting that the mobility is limited by the grain boundary and surface roughness scattering[2, 8]. In the future, it is possible to further improve the mobility by increasing the domain size and reducing the surface roughness by optimizing the evaporation process.

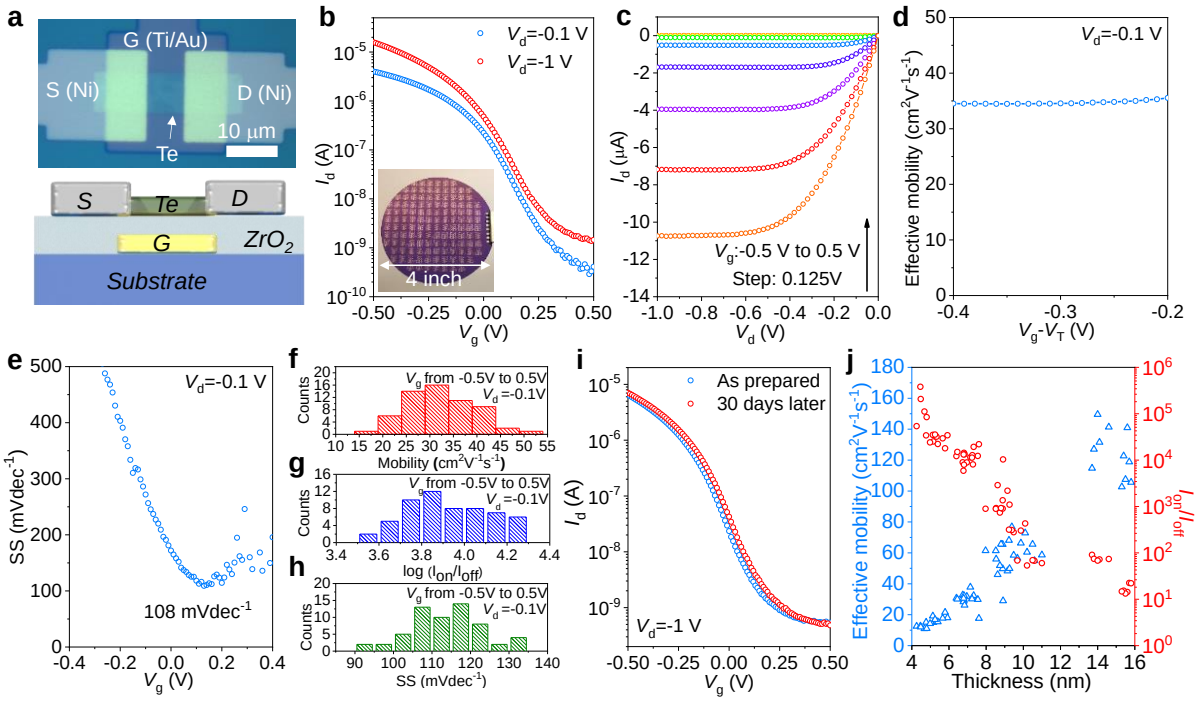


Figure 2.3.1 | Field-effect transistors based on Te evaporated with a substrate temperature of -80 ºC. a, Optical image of a typical Te FET and schematic diagram of the device structure. **b**, I_d-V_g transfer curves of the Te transistor (8 nm) in **a**. Inset, photograph of wafer-scale (4 inch) Te FETs. **c**, I_d-V_d output characteristics of the same device as shown in **b**. **d-e**, effective mobility (**d**) and SS (**e**) derived from the I_d-V_g shown in **b**. **f-h**, The statistical distribution of effective mobility (**f**), log (I_{on}/I_{off}) (**g**), SS (**h**) for 60 individual transistors from different points on the wafer. **i**, I_d-V_g characteristic of a Te FET measured immediately and thirty days after fabrication. **j**, Thickness-dependent effective mobility (blue) and on/off current ratio (red) for Te FETs. Note that the thicknesses of Te film were measured by AFM.

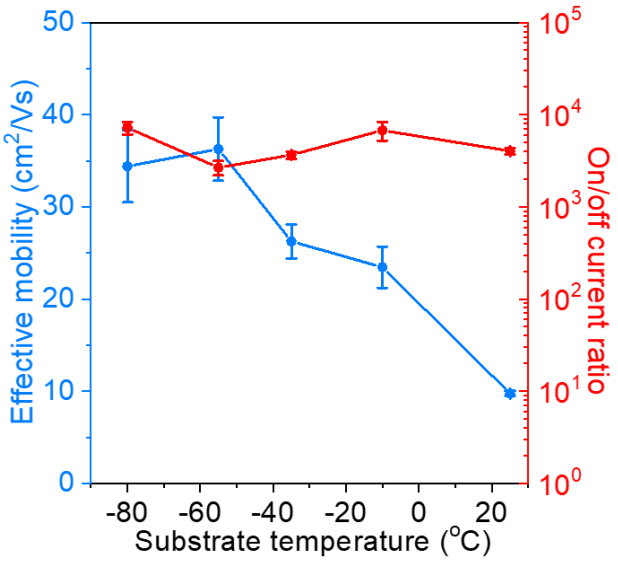


Figure 2.3.2 | Room temperature effective mobility and on/off current ratio of Te FET (8 nm) evaporated with different substrate temperatures (the channel length = 8 μm; the channel width = 8 μm).

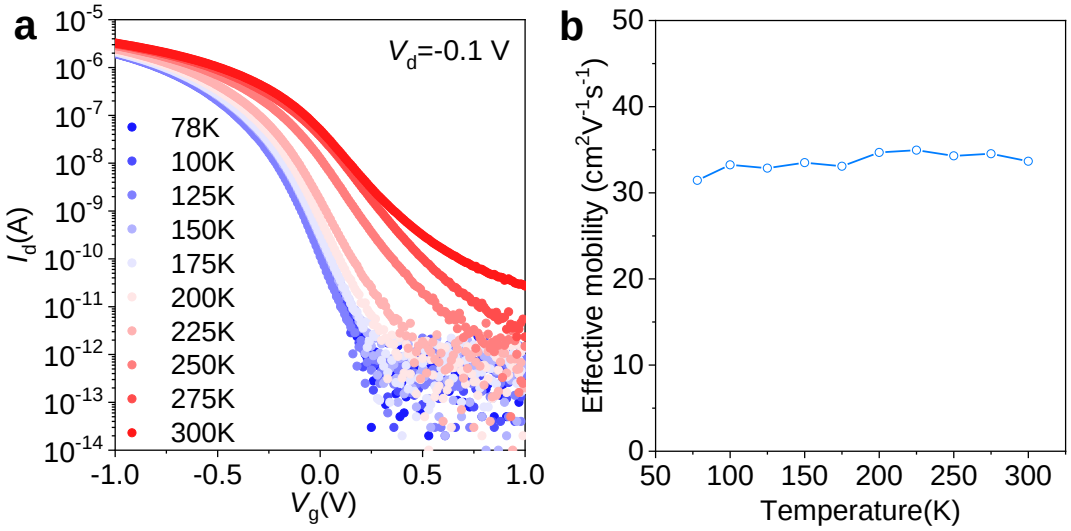


Figure 2.3.3 | **Temperature-dependent Te FET performance. a**, Temperature-dependent I_d-V_g transfer curves of Te FET (~8 nm) measured over a range of 78 K to 300 K. **b**, Temperature-dependent effective mobility derived from the transfer curves in **a**.

We then investigated the thickness-dependent effective mobility and on/off current ratio, the key metrics for transistors (Figure 2.3.1j). Here, we vary the channel thickness from 4 to 16 nm. Te FETs become open circuits at sub-4 nm thickness and the evaporated films were found to be not continuous. The on/off current ratio decreases from ~10^5 (4 nm Te) to ~10 (16 nm Te), which is likely due to the bandgap of Te channel decreases and electrostatic control is reduced as thickness increases. In contrast, the effective mobility increases with thickness monotonically from

10 $cm^2V^{-1}s^{-1}$ to 140 $cm^2V^{-1}s^{-1}$. The monotonically increased mobility along with the film thickness could be attributed to the reduced effect of surface roughness scattering for thicker films, which is often observed in various material systems[9, 10].

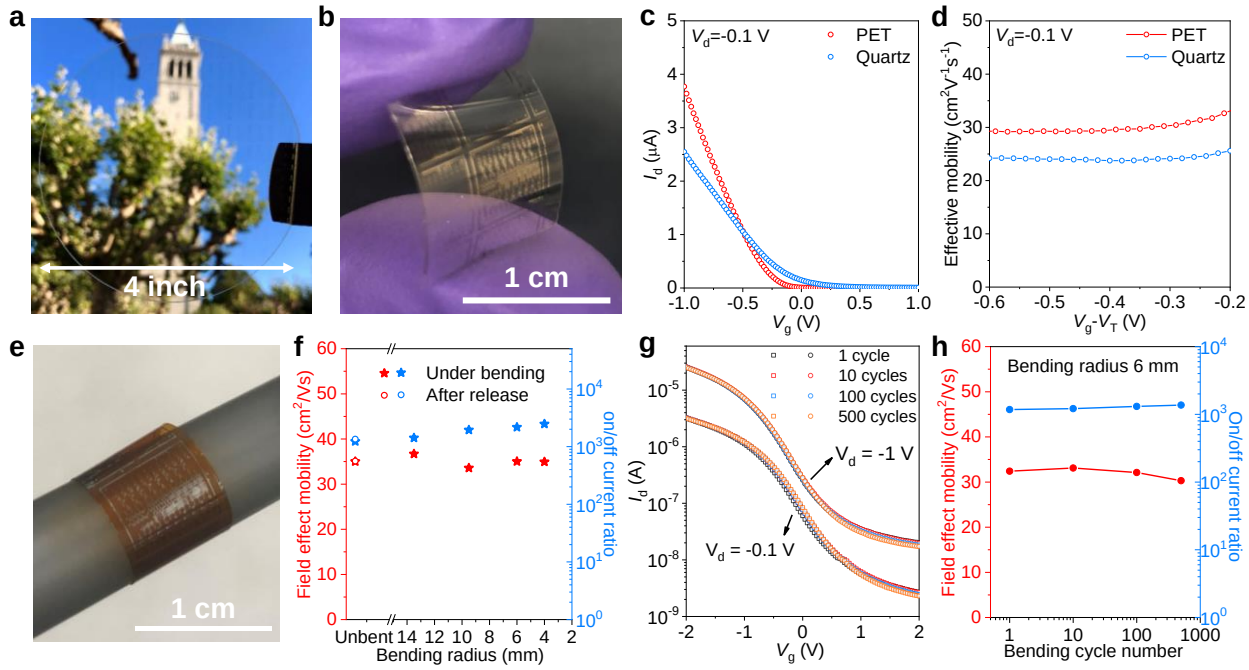


Figure 2.3.4 | Flexible and transparent field-effect transistors based on Te evaporated with a substrate temperature of -80 ºC. a-b, Photograph of Te FETs fabricated on 4-inch quartz wafer (**a**) and PET substrate (**b**). **c**, I_d-V_g transfer curves for evaporated Te FETs on quartz and PET substrates. **d**, Effective mobility of 8-nm-thick Te FETs on quartz and PET substrates. **e**, Photograph of Te FETs on Kapton substrate while bent (thickness of the Kapton substrate is 50 μm). **f**, Effective mobility and on/off current ratio of Te FET (8 nm) on Kapton substrate under different bending radius. **g**, I_d-V_g transfer curves of the Te transistor (8 nm) on PET substrate after different bending cycles. **h**, Effective mobility and on/off current ratio of Te FET (8 nm) on Kapton substrate after different bending cycles.

As a benefit of the low temperature evaporation process, Te can be readily deposited on various substrates such as glass and plastic over large areas (Figure 2.3.4a and b). We fabricated 8-nm-thick Te FETs on 4-inch quartz wafer and polyethylene terephthalate (PET) substrates with the same device structure shown in Figure 2.3.1a. Te FETs on different substrates show similar hole mobilities (in the range of 25-35 $cm^2V^{-1}s^{-1}$) and on-currents (Figure 2.3.4c and d), suggesting that Te FETs can be used in broad applications, such as flexible and transparent electronics and displays[11]. We characterized the mechanical flexibility and operational stability of Te FETs on Kapton substrate. Figure 2.3.4e shows a photograph of Te FETs on Kapton substrate when bent to a radius of 6 mm. The device mobility and on/off current ratio do not significantly change during bending up to a radius of 4 mm, corresponding to a tensile strain of 0.63% (Figure 2.3.4f and Figure 2.3.5). A change in device performance is observed when strain is higher than 0.63%. The

device becomes open circuit when strain reaches 1.5%, which is nonrecoverable (Figure 2.3.5). Furthermore, the electrical properties of the device do not significantly change after multiple cycles (500) of bending at a radius of 6 mm, which corresponds to a strain of 0.42% (Figure 2.3.4g and h).

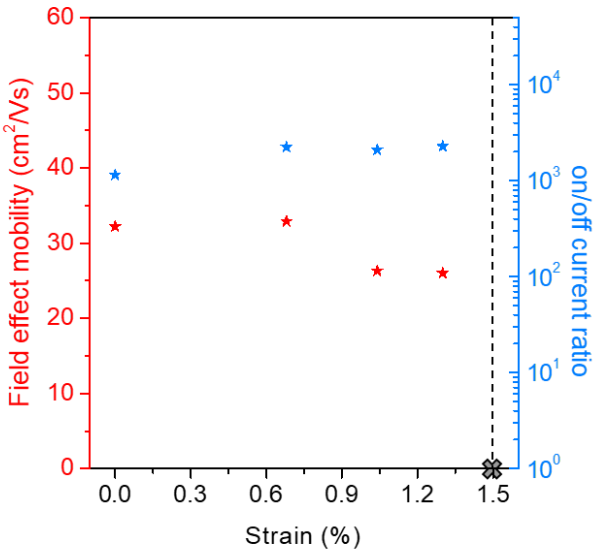


Figure 2.3.5 | Effective mobility and on/off current ratio of Te FET (8 nm) on Kapton substrate under different strain conditions.

2.4 Logic gates and circuits based on Te devices

The high uniformity of Te FETs allows for fabrication of logic gates and computational circuits. Considering the trade-off between on/off current ratio and mobility, 8-nm-thick Te FETs are selected as the building blocks. First, a *p*-MOS inverter, the simplest logic gate, is constructed using two Te devices, acting as the driver and active load, respectively (Figure 2.4.1a inset, and Figure 2.4.2a). Figure 2.4.1a shows typical voltage transfer curves with a gain of 22 and 38 at an operating voltage V_{dd}=1 V and V_{dd}=2 V, respectively. We also fabricated a NAND gate with a logically valid output (Figure 2.4.1b and Figure 2.4.2b). The basic logic gates facilitate the design of more complex circuits. A full-adder is a key component of arithmetic logic units, with myriad applications such as encoders, decoders and binary calculation[12]. Functionally, a full-adder is aimed to add two one-bit numbers (A and B) and one carry number (C_0), producing a two-bit sum (S) and new carry (C_1) as outputs. The Te FET based full-adder, which includes 9 NANDs and 4 inverters that are constructed from a total number of 35 transistors, is fabricated and shown in Figure 2.4.1c. The full-adder functions properly with a maximum output voltage loss of 6% (Figure 2.4.1c and d and Figure 2.4.2c and d). Therefore, we also fabricated a multiplier circuit to realize multiplication functions using 39 transistors. Functionally, 4 input terminals accept two 2-bit factors (A_1A_0 and B_1B_0) and the output is a 4-bit product ($F_3F_2F_1F_0$). The multiplication operation

is achieved with a maximum output voltage loss of 3% (Figure 2.4.1e and f, and Figure 2.4.2e and f).

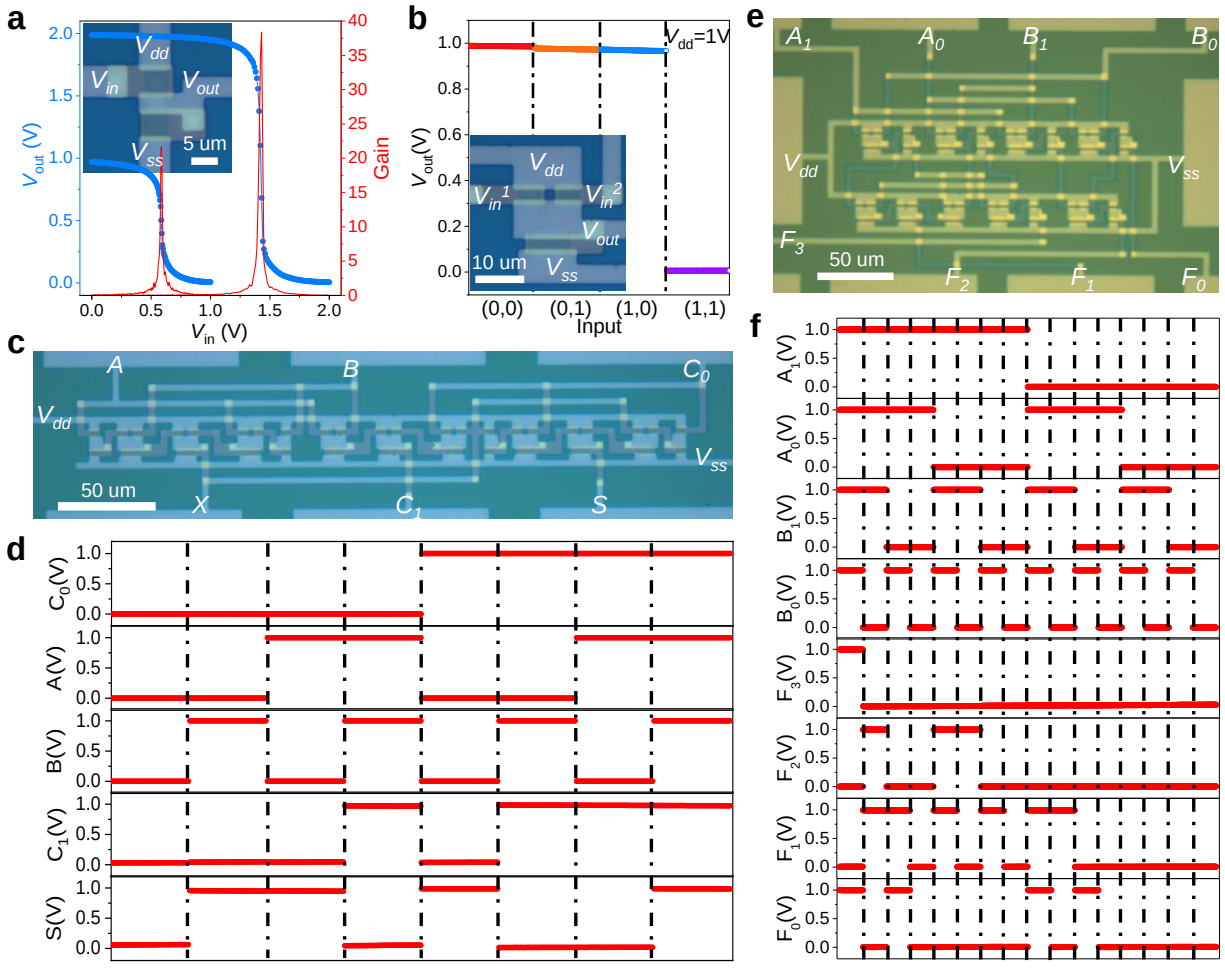
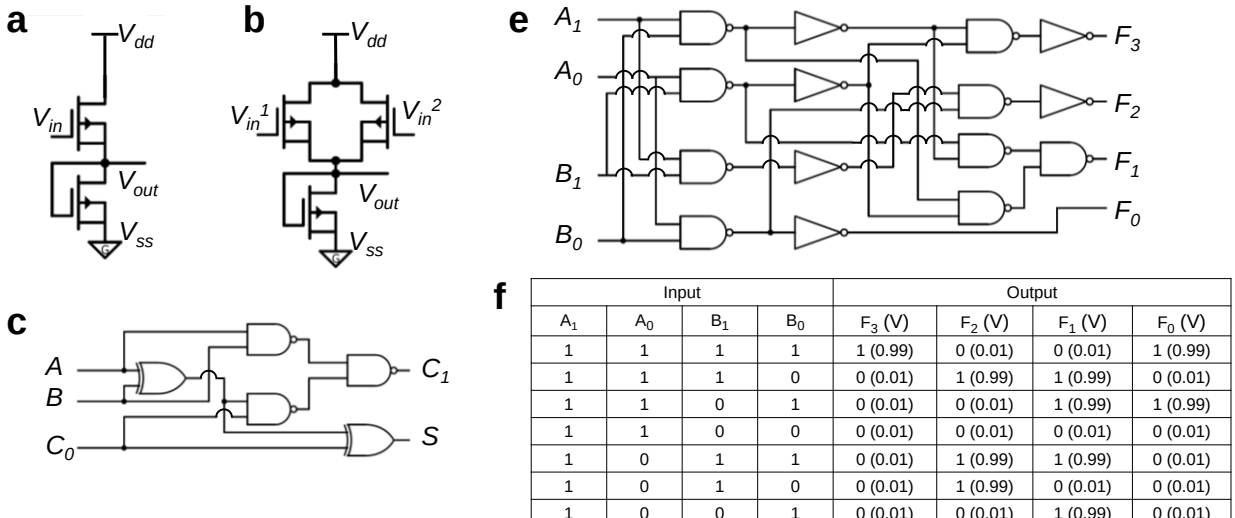


Figure 2.4.1 | Integrated circuits based on Te field effect transistors. a-b, Inverter (**a**) and NAND (**b**) logic gate performance, inset shows an optical image of the device. **c-d**, Optical image (**c**) and output voltage (**d**) of a full adder. **e-f**, Optical image (**e**) and output voltage (**f**) of a 2-bit multiplier. The supply voltage, V_{dd} was 1 V for the NAND gate, full adder, and 2-bit multiplier. Different input and the corresponding output states were separated by black dashed lines in **d** and **f**.



d

Input			Output	
C_0	A	B	C_1 (V)	S (V)
0	0	0	0 (0.03)	0 (0.06)
0	0	1	0 (0.04)	1 (0.95)
0	1	0	0 (0.04)	1 (0.95)
0	1	1	1 (0.97)	0 (0.05)
1	0	0	0 (0.04)	1 (0.99)
1	0	1	1 (0.99)	0 (0.01)
1	1	0	1 (0.98)	0 (0.02)
1	1	1	1 (0.98)	1 (0.99)

f

Input				Output			
A_1	A_0	B_1	B_0	F_3 (V)	F_2 (V)	F_1 (V)	F_0 (V)
1	1	1	1	1 (0.99)	0 (0.01)	0 (0.01)	1 (0.99)
1	1	1	0	0 (0.01)	1 (0.99)	1 (0.99)	0 (0.01)
1	1	0	1	0 (0.01)	0 (0.01)	1 (0.99)	1 (0.99)
1	1	0	0	0 (0.01)	0 (0.01)	0 (0.01)	0 (0.01)
1	0	1	1	0 (0.01)	1 (0.99)	1 (0.99)	0 (0.01)
1	0	1	0	0 (0.01)	1 (0.99)	0 (0.01)	0 (0.01)
1	0	0	1	0 (0.01)	0 (0.01)	1 (0.99)	0 (0.01)
1	0	0	0	0 (0.01)	0 (0.01)	0 (0.01)	0 (0.01)
0	1	1	1	0 (0.02)	0 (0.01)	1 (0.99)	1 (0.99)
0	1	1	0	0 (0.02)	0 (0.01)	1 (0.99)	0 (0.01)
0	1	0	1	0 (0.02)	0 (0.01)	0 (0.01)	1 (0.99)
0	1	0	0	0 (0.02)	0 (0.01)	0 (0.01)	0 (0.01)
0	0	1	1	0 (0.03)	0 (0.01)	0 (0.01)	0 (0.01)
0	0	1	0	0 (0.03)	0 (0.01)	0 (0.01)	0 (0.01)
0	0	0	1	0 (0.03)	0 (0.01)	0 (0.01)	0 (0.01)
0	0	0	0	0 (0.03)	0 (0.01)	0 (0.01)	0 (0.01)

Figure 2.4.2 | Schematic diagram and experimental truth table for Te FETs based ICs. a-b, Schematic diagram of an inverter (**a**) and NAND gates (**b**). **c-d**, Schematic diagram (**c**) and truth table (**d**) for Te FET based full-adder. The voltages indicated correspond to the outputs recorded from the device. **e-f**, Schematic diagram (**e**) and truth table (**f**) for Te FET based 2-bit multiplier. Voltages indicated correspond to the outputs recorded from the device.

2.5 Demonstration of three-dimensional monolithic circuits

The performance of Te *p*-FETs is sufficient to enable the realization of complementary 3D monolithic ICs and back-end-of-line (BEOL) electronics when combined with the existing *n*-FETs such as *a*-IGZO[13, 14]. Therefore, as a proof-of-concept, we fabricated multilayer transistors and logic gates based on Te *p*-FETs. Figure 2.5.1a and b show the two-layer transistors fabricated using an evaporated SiO_x isolation layer. The devices on the 1st and 2nd layers show similar I_d-V_g transfer curves (Figure 2.5.1c). Importantly, the electrical property of the 1st layer does not significantly change after the construction of the top layer given the low processing temperature used for all the fabrication steps (Figure 2.5.2). Note that a small threshold voltage (V_t) shift is observed. This shift is likely caused by fixed charge in the intermediate oxide or at the semiconductor-oxide interface, which can be improved by moving to a more suitable insulation layer or a more optimized deposition technique. A 3D circuit, specifically, a two-layer inverter, is also demonstrated. The upper-layer transistor, acting as an active load, is vertically connected to the bottom-layer transistor acting as the driver (Figure 2.5.1d and f). The 3D inverter accomplishes the desired NOT function with a gain of approximately 12 at a V_{dd}=2 V (Figure 2.5.1f). These results demonstrate the practicality of Te *p*-FETs for monolithic 3D circuits.

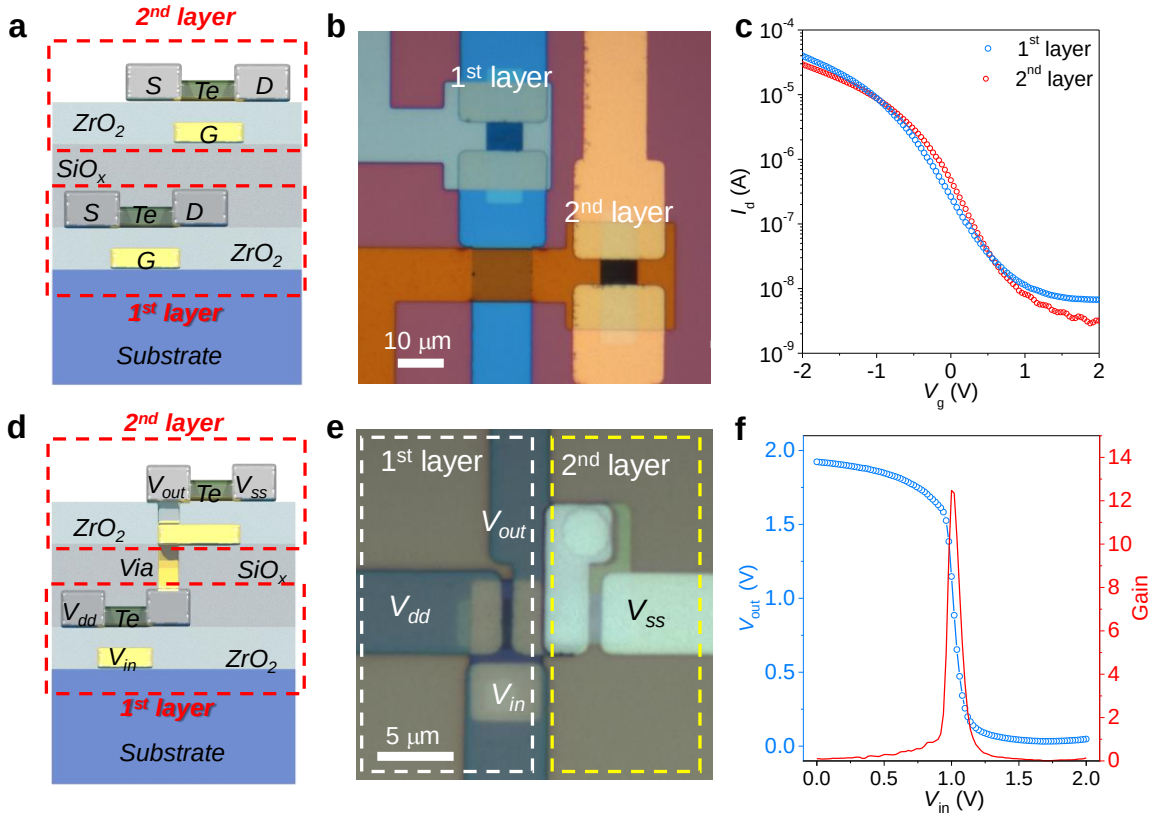


Figure 2.5.1 | Multilayered Te field-effect transistors and 3D inverters. a-c, A schematic diagram (**a**), optical image (**b**) and I_d-V_g transfer curves (V_d = -1 V) (**c**) of the 2-layered transistor. The thickness of Te channels for both layers is 8 nm. **d-f**, A schematic diagram (**d**), optical image (**e**) and voltage transfer characteristic (**f**) of the 3D inverter based on Te FETs (Te channels 8 nm).

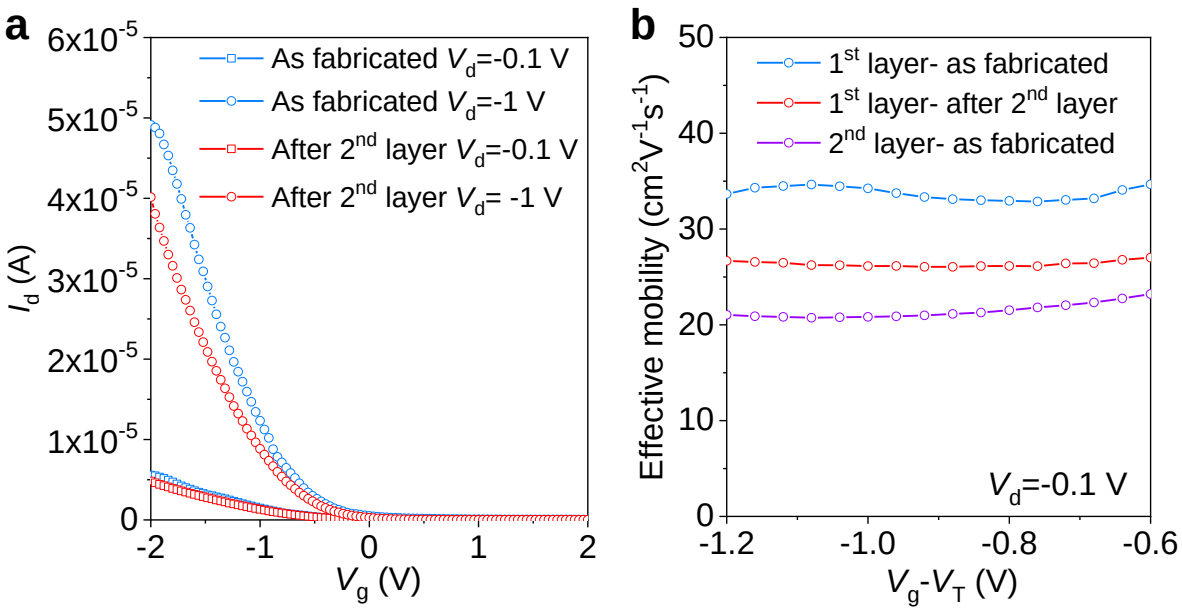


Figure 2.5.2 | Transfer curves for 2-layered transistors. a, I_d-V_g curves measured on the 1st layer Te FET before and after fabrication of the 2nd layer. **b**, Effective mobility of the 1st layer Te FET before and after 2nd layer fabrication and 2nd layer Te FET derived at V_d=-0.1 V (first layer: the channel length = 6 μm; the channel width = 8 μm; second layer: the channel length = 5 μm; the channel width = 8 μm).

2.6 Conclusions

We have demonstrated that evaporated Te thin films are an attractive material for *p*-FETs processed at low temperatures with important practical implications in monolithic 3D circuits, as well as flexible and transparent, and/or large-area electronics. We believe that further improvements in the thin film quality (e.g. purity, crystallinity and surface smoothness) will enhance the device performance of Te FETs. Future integration of Te *p*-FETs with low temperature *n*-type FETs, such as *a*-IGZO, can enable the construction of 3D CMOS circuits. Te *p*-FETs can also be implemented into BEOL electronics with existing Si CMOS circuits to further extend/enhance the system performance.

2.7 Method and Characterizations

Single transistors. Field-effect transistors were fabricated on various substrates by the following photolithography, deposition and lift-off processes. Firstly, gate regions were patterned on the SiO_2/Si, PET, Kapton or quartz substrates and Ti/Au (2 nm/18 nm) gate electrodes were deposited by e-beam evaporation. The ZrO_2 dielectric layer was then deposited by ALD. For single transistors on SiO_2/Si substrates, ZrO_2 was deposited at 200 ℃ with a thickness of 5nm. For transistors on PET, and quartz, ZrO_2 was deposited at 110 ℃ with a thickness of 10 nm. For transistors on Kapton, ZrO_2 was deposited at 110 ℃ with a thickness of 20 nm. Following the gate fabrication, Te channel regions were patterned over the gate area and Te was deposited. After

the lift-off process, source and drain regions were patterned. Ni (30 nm) was deposited by e-beam evaporation as metal contact. For Te FETs on quartz, sputtered ITO was used as gate (20 nm) and contact material (25 nm) to enable device transparency.

Logic gates and circuits. For the logic circuits a 10 nm ZrO_2 was deposited at 200 ℃ by ALD as the dielectric layer. Via regions were etched by buffered HF solution (BHF). Additionally, Ni/Au (20 nm/10 nm) contacts were used to avoid Ni etching by BHF.

Two layered transistors and 3D inverters. The bottom layers were fabricated using the process described above. After the fabrication of the bottom layer, 30 nm SiO_x was deposited on the top as an intermediate insulation layer by e-beam evaporation and then the next layer was built on the top using the same procedure used for the first layer. ZrO_2 (10 nm) was deposited at 110 ℃ by ALD.

Characterizations. Te thin films with varying thickness were deposited on quartz substrates for the optical measurement. The thicknesses of Te thin films for optical bandgap measurements and thickness-dependent device performance were measured by AFM (Dimension ICON AFM microscope (Bruker), operating in tapping mode). All other thickness measurements were based on the crystal quartz monitor. TEM characterization was performed on 9-nm thick Te deposited on SiO_2 support TEM membrane (TED PELLA, INC). The Te film in Figure 1c was patterned and transferred on SiO_2 support TEM membrane. TEM characterization was carried on a FEI Titan 60-300 microscope with an acceleration voltage 200 kV at the National Center for Electron Microscopy at Lawrence Berkeley National Laboratory. The sample for XRD measurement was deposited on glass with a thickness of 50 nm (based on the quartz crystal monitor). XRD measurement was performed on an AXS D8 Discover GADDS, Bruker with a Co Kα X-ray source (λ = 1.7903 Å). A Shimadzu SolidSpec-3700 spectrometer was used to measure the transmission and diffuse reflection of the samples. The polarized-light optical microscopy images of Te thin films were taken by a polarized LV100N optical microscopy (Nikon Inc.). Room-temperature electrical measurements were performed in probe station using 4155C Semiconductor Parameter Analyzer (Agilent Technologies). Temperature-dependent electrical measurements were performed in a cryogenic probe station (LakeShore) with a B1500a Semiconductor Device Analyzer (Keysight). Effective mobility is calculated using: $\mu_{eff} = \frac{dI_d}{dV_d}\frac{L}{WC_{ox}(V_g - V_t)}$ (1), where C_{ox} is the gate oxide capacitance, L is the channel length, W is the device width and V_t is the threshold voltage. I_d was measured at low bias (V_d = -0.1 V). Subthreshold swing (SS) is derived from equation: $SS = (\frac{d(\log I_d)}{dV_g})^{-1}$ (2), at the low bias (V_d = -0.1 V).

2.8 References

[1] M. M. Shulaker, G. Hills, R. S. Park, R. T. Howe, K. Saraswat, H.-S. P. Wong, S. Mitra, *Nature* **2017**, 547, 74.

[2] J. Kwon, Y. Takeda, R. Shiwaku, S. Tokito, K. Cho, S. Jung, *Nature Communications* **2019**, 10, 54.

[3] H. Chen, Y. Cao, J. Zhang, C. Zhou, *Nature Communications* **2014**, 5, 4097.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, 432, 488.
[5] T. Rembert, C. Battaglia, A. Anders, A. Javey, *Advanced Materials* **2015**, 27, 6090.
[6] H.-I. Yeom, J. B. Ko, G. Mun, S.-H. K. Park, *Journal of Materials Chemistry C* **2016**, 4, 6873.
[7] V. H. Martinez-Landeros, N. Hernandez-Como, G. Gutierrez-Heredia, R. Ramírez-Bon, M. Quevedo-Lopez, F. S. A. Tostado, *Semiconductor Science and Technology* **2018**.
[8] F. S. Stinner, Y. Lai, D. B. Straus, B. T. Diroll, D. K. Kim, C. B. Murray, C. R. Kagan, *Nano Letters* **2015**, 15, 7155.
[9] Z. Wang, P. K. Nayak, J. A. Caraveo-Frescas, H. N. Alshareef, *Advanced Materials* **2016**, 28, 3831.
[10] H. Sirringhaus, *Advanced Materials* **2014**, 26, 1319.
[11] D. Shahrjerdi, B. Hekmatshoar, S. Mohajerzadeh, A. Khakifirooz, M. Robertson, *Journal of Electronic Materials* **2004**, 33, 353.
[12] M.-G. Kim, M. G. Kanatzidis, A. Facchetti, T. J. Marks, *Nature Materials* **2011**, 10, 382.
[13] E. Fortunato, P. Barquinha, R. Martins, *Advanced Materials* **2012**, 24, 2945.
[14] M. J. Powell, *IEEE Transactions on Electron Devices* **1989**, 36, 2753.
[15] M. L. Geier, J. J. McMorrow, W. Xu, J. Zhu, C. H. Kim, T. J. Marks, M. C. Hersam, *Nature Nanotechnology* **2015**, 10, 944.
[16] H. Park, A. Afzali, S.-J. Han, G. S. Tulevski, A. D. Franklin, J. Tersoff, J. B. Hannon, W. Haensch, *Nature Nanotechnology* **2012**, 7, 787.
[17] B. Chen, P. Zhang, L. Ding, J. Han, S. Qiu, Q. Li, Z. Zhang, L.-M. Peng, *Nano Letters* **2016**, 16, 5120.
[18] Q. Cao, S.-j. Han, G. S. Tulevski, Y. Zhu, D. D. Lu, W. Haensch, *Nature Nanotechnology* **2013**, 8, 180.
[19] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Plis, H. S. Kim, S.-Y. Chen, *Nature* **2010**, 468, 286.
[20] J.-H. Ahn, H.-S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. Sun, R. G. Nuzzo, J. A. Rogers, *Science* **2006**, 314, 1754.
[21] R. W. Dutton, R. S. Muller, *Proceedings of the IEEE* **1971**, 59, 1511.
[22] K. Okuyama, Y. Kumagai, *Journal of Applied Physics* **1975**, 46, 1473.
[23] P. Weimer, *Proceedings of the IEEE* **1964**, 52, 608.
[24] K. Okuyama, H. Yamamoto, Y. Kumagai, *Journal of Applied Physics* **1975**, 46, 105.
[25] R. Dutton, R. Muller, *Thin Solid Films* **1972**, 11, 229.
[26] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. A. Goddard, M. J. Kim, X. Xu, *Nature Electronics* **2018**, 1, 228.
[27] G. Zhou, R. Addou, Q. Wang, S. Honari, C. R. Cormier, L. Cheng, R. Yue, C. M. Smyth, A. Laturia, J. Kim, *Advanced Materials* **2018**, 30, 1803109.
[28] W. Wu, G. Qiu, Y. Wang, R. Wang, P. Ye, *Chemical Society Reviews* **2018**, 47, 7203.
[29] J. Chen, Y. Dai, Y. Ma, X. Dai, W. Ho, M. Xie, *Nanoscale* **2017**, 9, 15945.
[30] K. Ellmer, R. Mientus, *Thin Solid Films* **2008**, 516, 5829.
[31] C. A. Dimitriadis, P. A. Coxon, L. Dozsa, L. Papadimitriou, N. Economou, *IEEE Transactions on Electron Devices* **1992**, 39, 598.

[32] A. D. Franklin, *Science* **2015**, 349, aab2750.

CHAPTER 3

Tellurium Single-Crystal Arrays by Low-Temperature Evaporation and Crystallization

3.1 Introduction

Large-scale growth of high-quality semiconductors, the active component of devices, is the foundation of modern electronics[1]. Recently, evaporated tellurium (Te) was identified as a promising *p*-type material for flexible electronics due to its appealing electrical properties and potential low-temperature wafer-scale production[2-6]. Material vapor condensed on an unheated substrate typically forms amorphous-phased films, therefore high-temperature post-deposition annealing is required for film crystallization[7]. Interestingly, an amorphous-crystalline phase transition takes place in the evaporated Te films at near-ambient temperature during or immediately after the deposition[8, 9], yielding crystalline Te thin films with respectable electrical properties after optimizing the deposition conditions such as substrate temperature[10], deposition rate[11] or applying nucleation layer[12]. Post-annealing treatments were previously performed on the evaporated Te films in order to further improve crystallinity, decrease the density of grain boundaries and control crystal orientation, but the relatively high vapor pressure of tellurium leads to re-evaporating of films during post-annealing, creating a rough surface and pinholes in films, thus poor electric properties[13-15].

Although deposition and post-treatment optimization were previously investigated to enhance the quality of evaporated Te film[10, 11, 14], control of the amorphous to crystalline phase transformation kinetics has not yet been fully explored. In this work, we characterize and model the kinetics and dynamics of the crystallization of thermally evaporated amorphous Te films. The understanding so obtained is then used to fabricate large grain Te films (average grain area of 150 μm^2) with preferred (100) out-of-plane orientation at low temperatures. Te single crystal arrays (lateral dimension as large as 6 μm) were also realized on various substrates by patterned thermal evaporation and low-temperature crystallization. *P*-type field-effect transistors (FETs) based on the low-temperature crystallized ultrathin Te films (6 nm) are demonstrated, with an average effective mobility of ~100 $cm^2V^{-1}s^{-1}$ and on/off current ratio of ~3×10^4.

3.2 Material synthesis and characterization

Te thin films were deposited on a cold substrate (-80 ^oC) (See methods). X-ray diffraction (XRD) was performed on the as-deposited Te film (see Characterization). The absence of peaks in XRD measurement demonstrates the as-deposited Te film is amorphous (Figure 3.2.1). The amorphous to crystalline phase transformation including nucleation and growth process was observed with optical microscopy at room temperature as shown in Figure 3.2.2. Crystalline nuclei initially appear with variable shapes ranging from faceted to elliptical (Supplementary Figure

3.8.1). The nuclei grow over time, retaining their shape. New crystalline nuclei appear within the non-transformed portions of the sample throughout the transformation process. Eventually, the entire film is transformed into a polycrystalline sample. The phase transformation is confirmed by the occurrence of the intense (100) peak after the crystallization from XRD measurement (Figure 3.2.1).

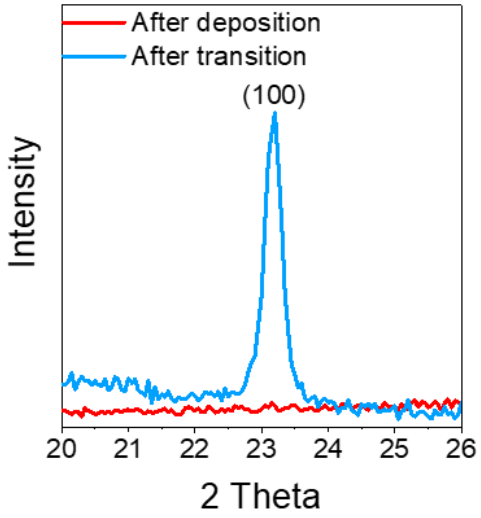


Figure 3.2.1 | XRD patterns of a Te thin film (50 nm) evaporated on cold SiO_2/Si substrate (-80 ^oC) after deposition (red line) and crystallization (blue line).

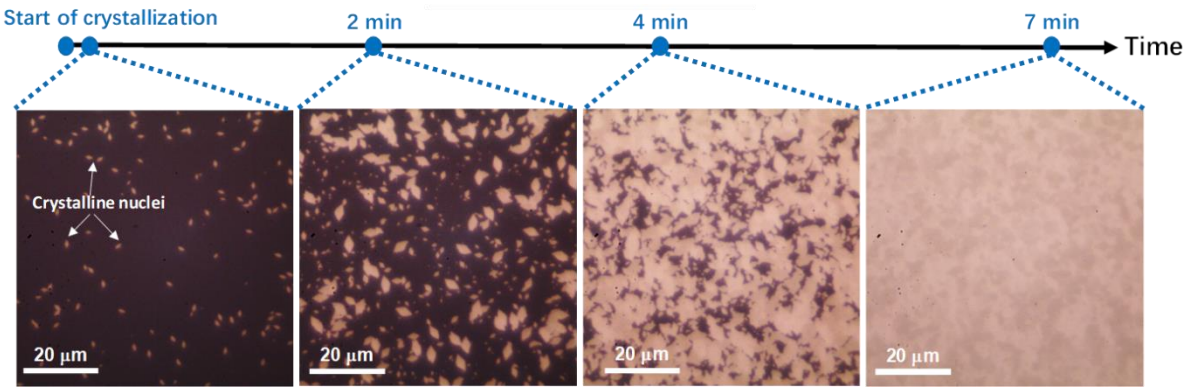


Figure 3.2.2 | The crystallization process for an as-deposited 10-nm-thick Te film at room temperature.

3.3 Kinetics and dynamics of the crystallization of thermally evaporated amorphous Te films

At low temperatures, the crystalline phase is preferred, as it is expected to have a lower Gibbs free energy. The reduction in free energy, then, drives the transformation. In many similar circumstances, however, the thermodynamically favorable phase transformation is impeded by kinetic constraints[16] (Figure 3.3.1a). Amorphous Te films are able to crystallize at low

temperature (ambient temperature or even lower) due to the low activation energy for diffusion of Te atoms or re-arrangement of short chains[9, 17-19]. To explore the kinetics of recrystallization, we conduct experiment to characterize both the nucleation and growth rates as a function of crystallization temperature. Our experiments follow the pathway described using the time temperature transformation (TTT) diagram as a guide (Figure 3.3.1b). Firstly, Te is thermally deposited on a cold substrate (-80 °C) and forms an amorphous film. After deposition, the substrate temperature is quickly increased to a desired temperature, at which the crystallization of the amorphous Te films starts. This substrate temperature is held constant during the whole process until the phase transition is completed (Figure 3.3.1b,c). Lastly, the substrate temperature is recovered back to room temperature after the completion of crystallization.

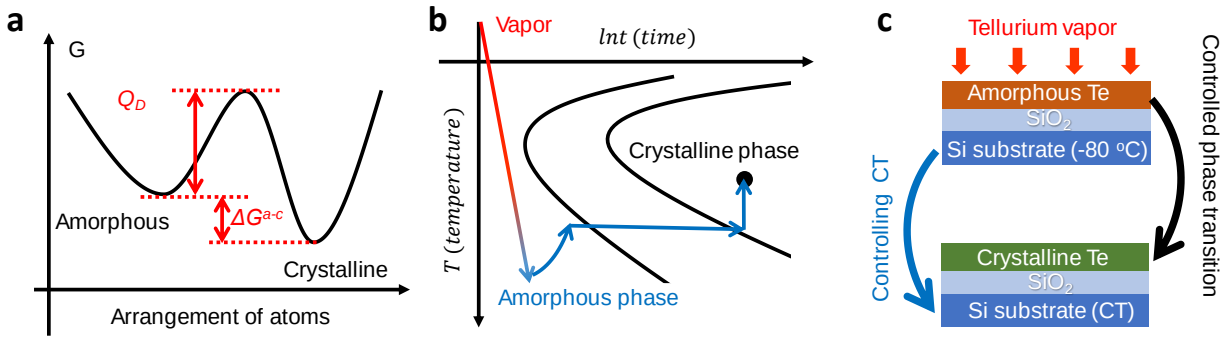


Figure 3.3.1 | Schematic of the crystallization process. a, Gibbs free energy change during amorphous-crystalline phase transition. **b**, TTT diagram showing the heat treatment pathway of evaporated Te films. **c**, Schematic of the controlled phase transition process (CT: crystallization temperature).

The dynamic crystallization processes at different temperatures were captured under an optical microscopy. The videos enable measurement of the fraction of the film transformed as a function of time. Figure 3.3.2a shows the experimentally observed transformation curves (the curves have been shifted in time for clarity). Note that as the temperature is increased, the apparent transformation time decreases quickly starting from over 10 minutes at 10 °C and decreasing to around 30 seconds at 35 °C.

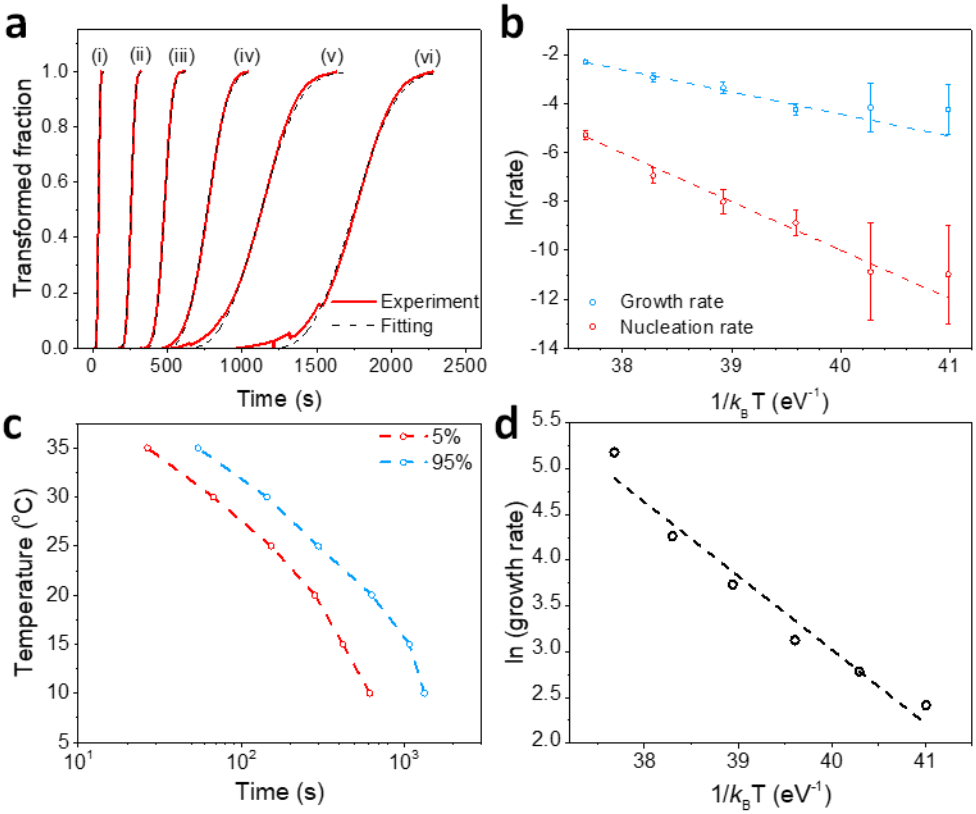


Figure 3.3.2 | Kinetic model for Te crystallization. **a**, The kinetic growth data obtained from analysis of experimental data for (i)…(vii) = 35, 30, 25, 20, 15 and 10 °C, respectively. The solid red curves are the experimental data obtained from the digitized movies, and the black dashed curves represent the fits of the data to Eqn. (1). **b**, The growth and nucleation rates determined by the fitting of Eqn. (1), along with their respective fits to the Arrhenius form. (All lengths are measured in microns, and times in seconds. **c**, TTT for Te films crystallized at different temperatures. 5% and 95% means the coverage of the crystallized Te extracted from videos. **d**, Plot of growth rate as function of temperature. The line represents the fit to the experimental data resulting in Arrhenius equation of $v \propto e^{-0.81/k_B T}$ for grain growth.

To gain a more detailed understanding of the transformation, the data in Figure 3.3.2a can be fitted to a kinetic model. The model chosen here assumes that both the nucleation and growth rates of the crystalline phase in the amorphous phase are constant throughout the transformation process (an isolated growing 2D grain thus appears circular). The nucleation and growth process are modeled as two dimensional, to reflect the aspect ratio of the thin films. Defining the nucleation rate per unit area and linear dimension growth rates to be $\dot{N}$ and v, respectively, and applying the arguments of Johnson and Mehl[20], Avrami[21], and Komolgorov[22], one arrives at the following expression for the transformed fraction, $f \equiv A_c/A$, with A_c the area of the film that has transformed to the crystalline state, and A the total area of the film:

$$f = 1 - \exp\left(-\frac{\pi}{3}\dot{N}v^2t^3\right), \quad (1)$$

where t is the time, measured from the time at which the first nucleus appears. Fitting the experimental data to the form of Eqn. (1) yields an experimental measurement of the product $\dot{N}v^2$. The same model also predicts that the final number density of grains at the completion of the transformation, N, is given by:

$$N = \Gamma\left(\frac{4}{3}\right)\left(\frac{3}{\pi}\right)^{\frac{1}{3}}\left(\frac{\dot{N}}{v}\right)^{\frac{2}{3}}, \quad (2)$$

with $\Gamma(x)$ the Euler gamma function. Eqn. (1) and (2), therefore, provide the means to assess independently the nucleation and growth rates for the crystalline phase.

Figure 3.3.2a shows the fitted curves obtained by using Mathematica's NonlinearModelFit function as compared with the experimental data (as described in the 3.8.1 Supplementary information, Supplementary Figure 3.8.2-4). Eqn. (1) represents the experimental data quite well. This data is combined with the measured grain number densities in the films to obtain the growth velocities and grain nucleation rates. The computed radial growth rates range from around 0.014 μm sec^{-1} to around 0.1 μm sec^{-1}. Assuming that the growth facet is (111), this corresponds to completion of an additional atomic layer approximately every 10^{-4} sec. Figure 3.3.2b displays Arrhenius plots for the growth and nucleation rates. The growth rate corresponds to an energy barrier of $\Delta E_v = 0.91 \pm 0.11$ eV. This, presumably, is the average energy barrier for attachment of an atom to the growing cluster from the amorphous surroundings.

The nucleation rate also obeys an Arrhenius form, but with an energy barrier of $\Delta E_{nucleation} = 1.98 \pm 0.21$ eV. This form can be rationalized using classical nucleation theory. To wit, the nucleation rate is the product of the attachment rate, governed by the same processes as the growth rate, and an exponential term that depends on the free energy of the nucleus:

$$\dot{N} \sim v \exp\left(-\frac{\Delta E_{\dot{N}}}{k_B T}\right) \sim \exp\left(-\frac{\Delta E_v + \Delta E_{\dot{N}}}{k_B T}\right), \quad (3)$$

with k_B Boltzmann's constant, and $\Delta E_{\dot{N}}$ the energy barrier for nucleation. Approximating the nuclei as spherical, we arrive at an expression for $\Delta E_{\dot{N}}$:

$$\Delta E_{\dot{N}} = \frac{16\,\pi\gamma^3}{3\,\Delta G_{c\to a}{}^2}, \quad (4)$$

where γ is the interfacial free energy for the amorphous crystalline interface, and $\Delta G_{c\to a}$ is the free energy increase per unit volume for converting the crystalline to the amorphous phase. Applying Eqn. (3) and (4) along with the experimentally determined values for the activation energies, we conclude that $\Delta E_{\dot{N}} = 1.07 \pm 0.24$ eV. The Materials Project tabulates the air/crystal surface energies for Te and these range from 0.005 to 0.023 $eVÅ^{-2}$.[23] Assuming that the interfacial energy for the crystalline/amorphous interface is approximately equal to 1/2 the smallest of these

energies minimum energy, or 2.5 ± 0.6 meV/ Å^2, one concludes that $\Delta G_{c\to a} = 17 \pm 7$ meV/atom, and the critical nucleus size over the temperature range studied includes roughly 127 atoms.

The growth velocity can also be measured directly from the videos (as described in the 3.8.1 Supplementary information, Supplementary Figure 3.8.5). As temperature is decreased from 35 ^{o}C to 10 ^{o}C, the incubation time, that is the time to 5% transformation, increases from ~30 seconds to more than 10 min due to the suppressed nucleation rate ($\dot{N}$ is dominated by temperature) and crystallization time increases from seconds to hours (Figure 3.3.2c), which is contributed by low nucleation and growth rates. The activation energy for Te crystal growth is extracted directly by measuring growth rate at different crystallization temperatures (Supplementary Figure 3.8.4) and fitting the temperature-dependent growth rate to the Arrhenius equation for grain growth (Figure 3.3.2d). The extracted activation energy extracted directly from measurements of growth is 0.81±0.1 eV in good agreement with the value $\Delta E_v = 0.91 \pm 0.11$ eV extracted from fitting to Eqn. (1). The energy barrier is also much lower than that of Si or Ge (~ 3 eV)[24]. which explains the tendency towards crystallization of the amorphous Te films at the low temperature (-10 ^{o}C or even lower).

Based on the observations above, larger grain size can be obtained by reducing the ratio $\dot{N}/v$, which according to Eqn. (3) has an Arrhenius form with an activation energy barrier equal to $\Delta E_{\dot{N}}$ (Directly fitting the grain density data to an Arrhenius form yields the value $\Delta E_{\dot{N}} = 0.72 \pm 0.21$ eV, which is in reasonable agreement with the value derived above). Consequently, over the range of temperatures modeled here, a lower temperature corresponds to a lower number of grains. Practically, amorphous Te films start rapidly crystallizing during the ramp-up process towards targeted high temperature and re-evaporate in high-temperature range (vapor pressure is 10^{-6} mTorr at temperature of ~220 ^{o}C), yielding small grains and rough surface. Therefore, we crystallize 10-nm-thick amorphous Te films in the temperature range from 100 ^{o}C to -10 ^{o}C (see Methods). When crystallization temperature decreases from 100 ^{o}C to 5 ^{o}C, the average area of the domains increases from sub-μm^2 to ~150 μm^2 (Figure 3.3.3a-d and Supplementary Figure 3.8.6) observed by polarized optical microscopy. The average domain size has no change when we further decrease the crystallization temperature to -10 ^{o}C (Figure 3.3.3e). For higher temperatures (higher than 100 ^{o}C), amorphous Te films start rapidly crystallizing during the ramp-up process towards the targeted high temperature (it just takes seconds to finish the crystallization at 100 ^{o}C), yielding small grains; re-evaporation of Te in high-temperature range (vapor pressure is 10^{-6} mTorr at temperature of ~220 ^{o}C) would cause a rough surface with pinholes, and films became discontinuous after a 5 min annealing at 300 ^{o}C. (Supplementary Figure 3.8.7).

XRD measurements were performed on the crystallized Te to investigate the crystallinity of the films (Figure 3.3.3f and Supplementary Figure 3.8.8). Comparing with the 25 ^{o}C crystallized 50-nm-thick film, where two dominated peaks (100), (101) and two weak peaks (110), (200) were observed (Supplementary Figure 3.8.8a), only two peaks corresponding to (100) and (200) facets were observed for the 0 ^{o}C crystallized 50-nm-thick Te film (Figure 3.3.3f). A layer-by-layer restacked 0 ^{o}C crystallized 8-nm-thick Te sample also exhibits a strong out-of-plane (100) texture

(Supplementary Figure 3.8.8b), indicating that highly crystallized and well orientated Te films ((100) out-of-plane orientation) can be achieved by crystallizing the evaporated amorphous films at low temperature. This preferred orientation is because (100) planes of Te have the lowest surface energy, and the growth rate is low at low temperature, so that the atoms have enough time to find their positions with the minimized energy. Angle-resolved Raman was performed on 4 patterned Te single grains to determine their in-plane orientations (Supplementary Figure 3.8.9). These grains showed 4 different in-plane orientations, which implies that the in-plane orientation for the Te films was random. The mosaicity of the film was characterized by electron back scattering diffraction (EBSD). Based on the EBSD map, (10-10) and (01-10) planes (Miller-Bravais notation) were parallel to the surface, which is consistent with the XRD result (Supplementary Figure 3.8.10). The color in the map showed a minimal variation, indicating a small misorientation.

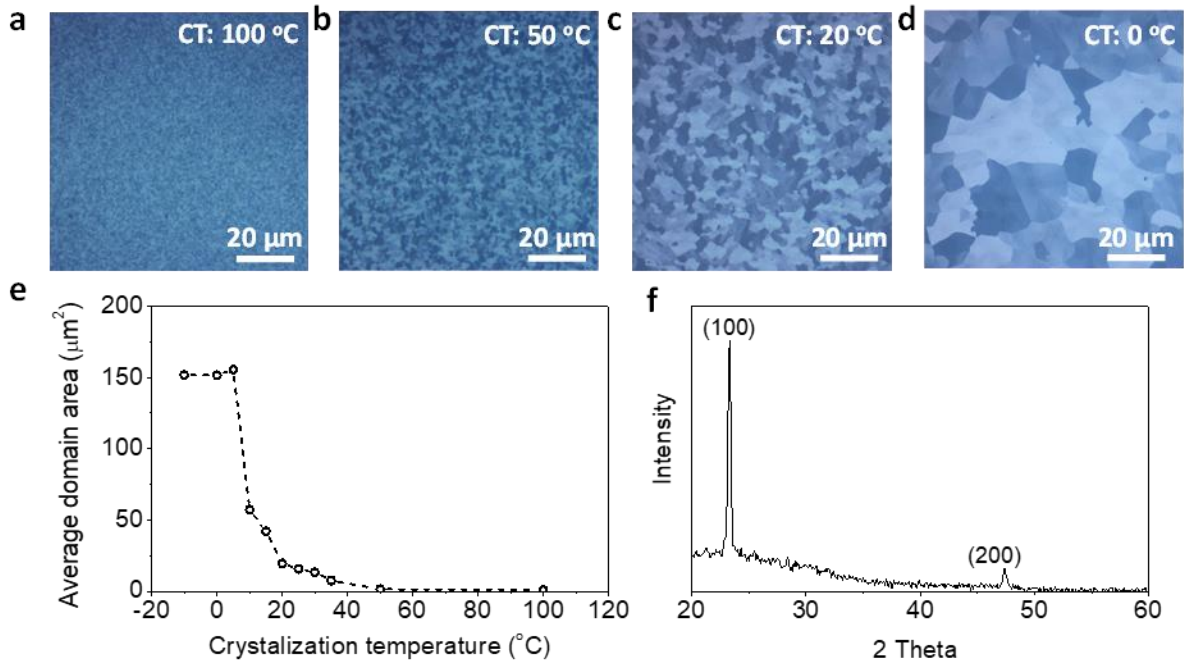


Figure 3.3.3 | Characterization of Te thin films crystallized at different temperatures. a-d, polarized light microscopy image of the Te films (10 nm) crystallized at 100 °C (**a**), 50 °C (**b**), 20 °C (**c**) and 0 °C (**d**). **e**, The calculated average domain areas of Te films (10 nm) crystallized at different temperatures. **f**, XRD pattern of a Te thin film (50 nm) crystallized at 0 °C.

3.4 Growth of patterned Te single crystal arrays

The channel for an ideal device should only have one single grain, since the grain boundaries can decrease the carrier mobility, increase leakage current and cause the threshold voltage shift[25]. Therefore, realization of single-crystalline Te patterns at desired locations is important for electronic and optoelectronic applications. To study the effect of crystallization temperature and feature size on the number of grains, 10 nm Te films were deposited on defined patterns (SiO_2/Si

substrate, see methods) with lateral size varying from 1 μm to 19 μm at -80 °C and crystallized at different temperature (Figure 3.4.1 and Supplementary Fig. 11).

The introduction of edges and small areas has the potential to alter the nucleation problem. Presumably, there are two competing mechanisms for grain nucleation – that for nucleation in the area of the film, and that for edge nucleation. Under these circumstances, it can be difficult to construct an algebraic theory for the number of grains[26]. To explore the effects of the finite size of the lithographic samples, we developed a simulation capable of predicting the number of grains appearing within a sample (for details, see the 3.8.2 Supplementary information). For these simulations, the nucleation rate for the area-based nucleation was taken to be the fitted Arrhenius form obtained from the blank thin film samples. The edge nucleation rate was used as a parameter, and was tuned to get general agreement with experimental observations. At $T = 0$ °C, simulations based on the fitted Arrhenius forms without an enhanced nucleation rate at the edge of the samples are not able to reproduce the experimental data. Increasing the areal nucleation rate by a factor of 2.9 over the extrapolated rate, and decreasing the growth velocity by a factor of 0.54 from its predicted value produces simulation results that are in reasonable agreement with the experimental data (see 3.8.2 Supplementary information). However, the data is better fit by retaining the parameters based on the Arrhenius forms and including an edge nucleation process. The comparison of the simulation predictions to experimental results for $T = 0$ °C is shown in Figure 5. The simulations are based on an area nucleation rate of $\dot{N}_{area} = 3.32 \times 10^{-7}$ sec^{-1} μm^{-2}, a growth velocity of $v = 1.05 \times 10^{-3}$ μm sec^{-1}, and an edge nucleation rate of $\dot{N}_{edge} = 6.8 \times 10^{-6}$ sec^{-1} μm^{-1}. The experimental data is described quite well by the simulations.

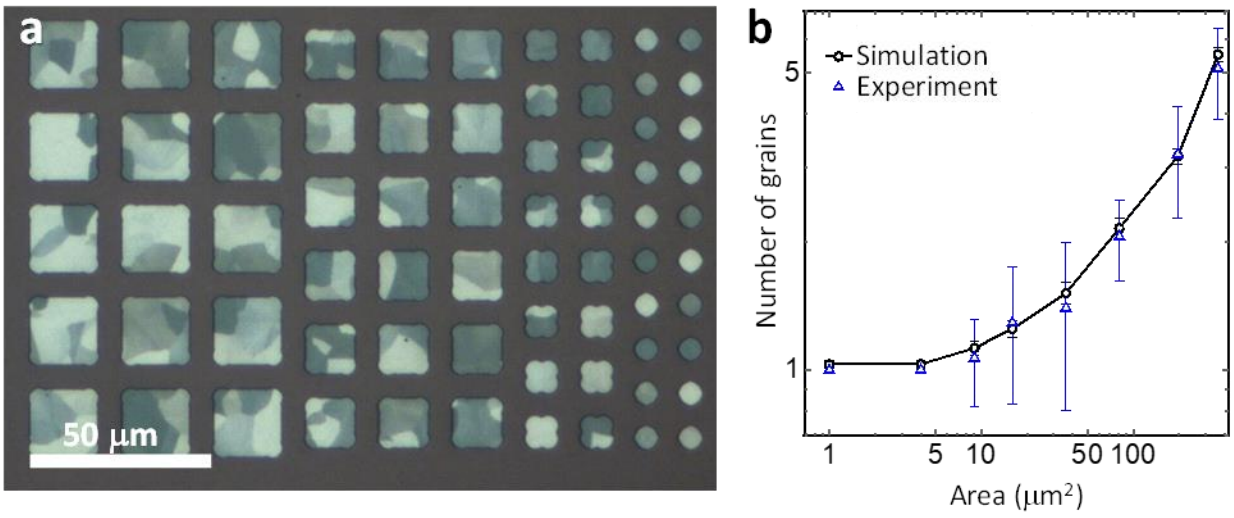


Figure 3.4.1 | 0° C crystallized Te array with different pattern area. a, Polarized light microscopy image of the patterned 0 °C crystallized Te (10 nm) array with lateral dimension ranging from 6 μm to 19 μm. **b,** Log-log plot of number of nuclei as a function of pattern area. Blue triangles are the experimental measurements and black circles are the simulation results.

Growth of highly crystalline Te arrays, which has near-unity average number of grains per pattern with lateral size as large as 6 μm, was realized on an amorphous SiO_2/Si substrate by controlling the crystallization process (Figure 3.4.1a and Supplementary Figure 3.8.11d,e). Transmission electron microscopy (TEM) was performed on a transferred pattern Te film (Supplementary Figure 3.8.15). Selected-area electron diffraction showed a single-crystalline diffraction pattern and high-resolution TEM image exhibited interplanar spacing of 5.9 Å corresponding to (001) planes (Supplementary Fig. 15b,c), confirming the quality of the patterned Te film. Single crystalline Te arrays (lateral size of ~ 6 μm) could also be grown on various substrates including glass and polymer (polyethylene terephthalate (PET) and Kapton) by using the same method (Supplementary Figure 3.8.16), demonstrating the potential of this method for a broad range of application in flexible and transparent electronics.

3.5 Device performance of Te based FETs

FETs were fabricated using Te films as the channel, and SiO_2 (50 nm thick)/p^+-Si as dielectric layer and back-gate to examine the electronic properties of low-temperature crystallized Te as shown in Figure 3.5.1a,b. Ni was used as the contact metal, as it can form near ohmic contact for holes due to the Fermi level pining near valence band for Te. [34,35] Te FETs exhibit a typical *p*-type characteristic due to the native defects (Figure 3.5.1c) with a common hysteresis behavior (Supplementary Figure 3.8.17). The transistor based on a single-grain Te (~6 nm) crystallized at 5 ^oC shows an effective hole mobility of 93 $cm^2V^{-1}s^{-1}$, subthreshold swing of 2.7 V dec^{-1} and on/off current ratio of ~10^5 (Figure 3.5.1c-e) at room temperature in vacuum environment (~10^{-5} mTorr). Statistic distribution of the device performance measured from 30 FETs based on the Te films (7 nm) crystallized at two different temperatures is shown in Figure 6f-g. When the crystallization temperature decreases from 35 ^oC to 5 ^oC, the average effective hole mobility with standard deviation increases from 67±4 $cm^2V^{-1}s^{-1}$ to 100±14 $cm^2V^{-1}s^{-1}$ and average on/off current ratio gets improved by >20 times increasing from 1×10^3 to 3×10^4, which is due to the higher crystallinity and less grain boundaries for 5 ^oC crystallized Te films. For 5 ^oC crystallized Te films, as the grain size was comparable to the channel dimensions, a relatively wider distribution in effective hole mobility was observed, which is caused by the random in-plane crystal orientations along the channel and the anisotropic in-plane electrical transport properties of Te. The 35 ^oC crystallized films had smaller grain size comparing to the 5 ^oC crystallized ones (Supplementary Figure 3.8.6a and f), the device channel based on which contained tens of small grains with random in-plane orientations and grain boundaries. The effective mobility extracted from the 35 ˚C crystallized films is an averaged value from these grains and grain boundaries, which had a smaller fluctuation comparing to the 5 ˚C crystallized one's. We then investigated the thickness-dependent effective mobility and on/off current ratio for the films crystallized at two different temperatures with the thickness ranging from 4 nm to 19 nm. 5 ^oC crystallized Te FETs shows a higher effective mobility and on/off current ratio compared to the 35 ^oC crystallized Te FETs in the measured thickness range, demonstrating electronic properties of the films get improved by optimizing the crystallization process. For 5 ^oC crystallized Te FETs, a maximum effective mobility of 264 $cm^2V^{-1}s^{-1}$ is achieved on a 19 nm thick film (Supplementary Figure 3.8.18) and the average effective

mobility with standard deviation decreases monotonically from 182±42 $cm^2V^{-1}s^{-1}$ (19 nm) to 30±4 $cm^2V^{-1}s^{-1}$ (4 nm) due to the enhanced effect of surface roughness scattering for thicker films (Figure 3.5.1h).[36] On/off current ratio increase from 4.5×10^2 (19 nm) to 6×10^5 (4 nm), which is caused by the larger bandgap and stronger electrostatic control of Te channel for thinner films. We performed Hall measurements on the Te films (lateral dimensions: 5mm x 5 mm) crystallized at 5 ^oC and room temperature (~20 ^oC) with a thickness of ~ 30 nm to estimate the hole concentration and Hall mobility. They showed a similar hole density of ~2.7 x 10^{18} cm^{-3}. The 5 ^oC crystallized Te film exhibited a Hall mobility of 162 $cm^2 V^{-1}s^{-1}$, which is higher than the room temperature crystallized one (102 $cm^2 V^{-1}s^{-1}$). To understand the carrier scattering mechanisms, we measured the temperature-dependent I_d-V_g transfer curves ranging from 77 K to 300 K on an 8-nm-thick 5 ^oC crystallized tellurium FET (Supplementary Figure 3.8.19a). The effective mobility increases as temperature is reduced with maximum value of 197 $cm^2V^{-1}s^{-1}$ at 77 K. The temperature-dependent effective mobility in high-temperature regime (T >175 K) can be fitted with a power law $\mu_{eff} \propto T^{-\gamma}$, where $\gamma = -0.56$, which is consistent with the reported result for a single crystal Te (Supplementary Figure 3.8.19b). [37]

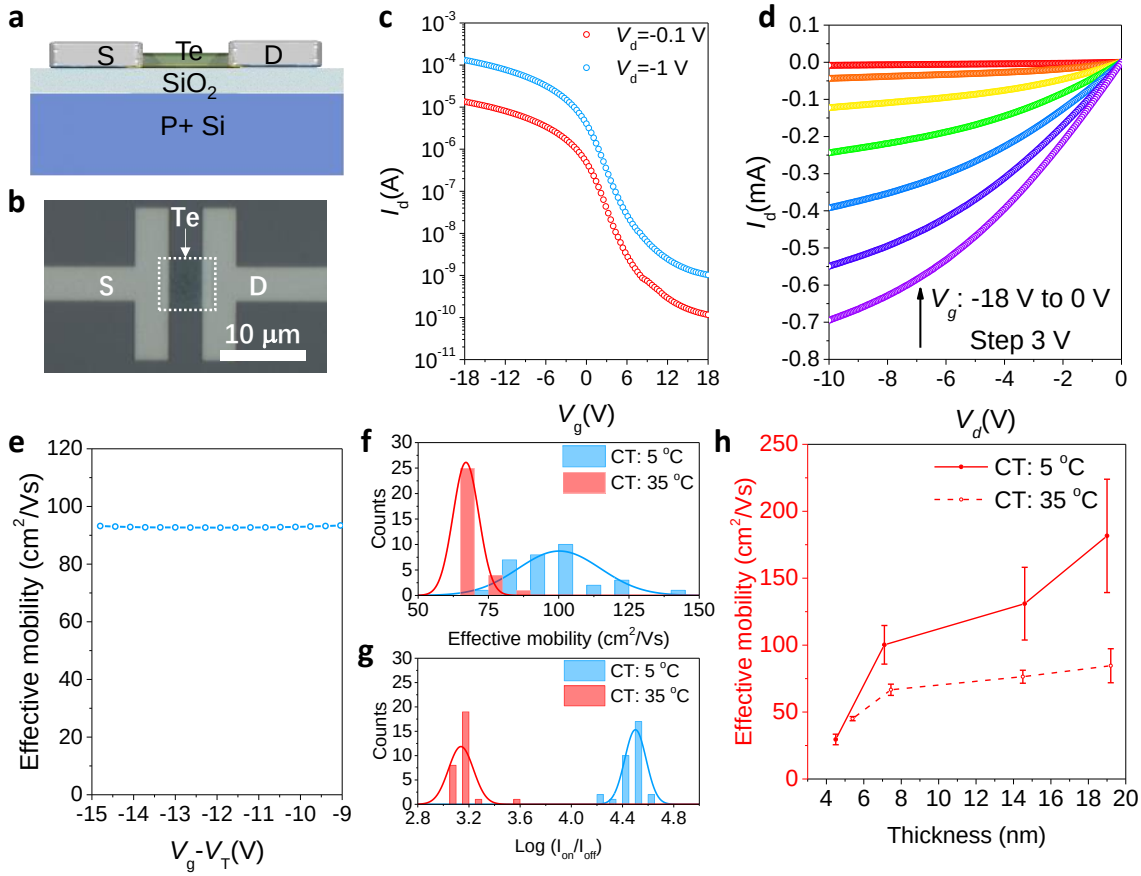


Figure 3.5.1 | Field-effect transistors based on Te films crystallized at different temperatures. **a,** Schematic diagram of the device structure. **b,** Optical image of a typical FET based on the single grain Te film crystallized at 5 °C. **c-e,** I_d-V_g transfer curves (**c**), I_d-V_d output characteristics (**d**) and derived effective mobility (**e**) for the Te transistor (6 nm) shown in **b**. **f-g,** The statistical distribution of effective mobility (**f**) and log (I_{on}/I_{off}) for Te FETs (7 nm) crystallized at different temperatures. **h,** Thickness-dependent effective mobility (blue) and on/off current ratio (red) for Te FETs crystallized at different temperatures.

3.6 Conclusion

In summary, we realize the growth of highly crystalline Te films with a preferred out-of-plane orientation and large grain size (average grain area of ~150 μm^2) and single-crystalline tellurium arrays (lateral size as large as 6 μm). We analyzed the growth kinetics, and using the understanding so obtained to control the crystallization process of thermally evaporated amorphous Te. A typical Te FET based on the low-temperature crystallized Te exhibit high performance in effective hole mobility. This method is compatible with various substrates due to its near-ambient processing temperature. In the future, it is possible to realize the growth of wafer-scale single-crystalline Te

films by further inducing the in-plane orientation of the Te atom chains, since a preferred out-of-plane orientation is achieved.

3.7 Method and Characterizations

Growth method of Te thin films. Te pellets (99.999%, Sigma-Aldrich) were used as the thermal evaporation source. The Te source pellets were loaded in a tungsten boat, which was beneath the substrate. Substrates such as SiO_2/p^+-Si, quartz or polymers were sticked on a steel sample chuck, which can be cooled by cold nitrogen gas flow, using Kapton tape. Bilayer positive photoresist (LOR 5A and S1818 with a thickness of ~ 0.5 μm and 2 μm) was used to define the pattern on the substrate. When the pressure reached $2x10^{-6}$ mbar, a cold nitrogen gas flow was used to cool down the sample chuck to -80 ^oC before deposition. Thermally evaporated Te was deposited on the bare/ patterned cold substrates (-80 ^oC) to form the amorphous-phased Te films/ arrays. The deposition rate (around 10 $Å s^{-1}$) and thickness of Te thin film was controlled during deposition by use of a quartz crystal microbalance. A room-temperature nitrogen gas flow was used to recover the temperature of the chuck after deposition. Samples were taken out from the chamber until the substrate temperature recovered to ~5 ^oC, preventing the condensation of water from ambient air. It took ~10 min for the temperature of the chuck increasing from -80 ^oC to 5 ^oC. As the crystallization process is very slow at low temperature (incubation time is tens of minutes at 5 ^oC), we assume the crystallization has not started, while the samples were unloaded from the evaporator. The amorphous samples were placed onto a thermoelectric module with a controlled constant temperature immediately after unloading for crystallization (thermoelectric module temperature was set to the desired crystallization temperature in advance). Considering silicon substrate is a good heat conductor, the size of the chip is small for the heat source/sink, contact between substrate and thermoelectric module is good, and the temperature difference is small, the Si substrate temperature would stabilize at the desired temperature in seconds. The sample was removed from the thermoelectric module when the crystallization process completed. The atmosphere was not controlled during the crystallization. Note that, the process requires protection from light, especially when the crystallization temperature is below 5 ^oC, since the light has an influence on the crystallization. The crystallization processes were monitored under an optical microscopy, when the crystallization temperature is above 5 ^oC. For the patterned Te samples, photoresist was removed after the crystallization by lift-off process.

Device Fabrication and Measurements. FETs were fabricated on 50 nm SiO_2/p^+-Si substrates. Heavily doped *p*-Si substate was used a global back gate and 50 nm SiO_2 is the dielectric layer. Te channel regions were patterned by electron-beam lithography. Te films were deposited on the -80 ^oC patterned SiO_2/p^+-Si substrates and crystallized at different temperatures as mentioned in growth method of Te thin films. After lift-off process, source and drain regions were patterned by electron-beam lithography. Ni (30 nm) was deposited using e-beam evaporation as metal contact. Room-temperature and temperature-dependent electrical measurements were performed under vacuum in a cryogenic probe station (LakeShore) with a B1500a Semiconductor Device Analyzer (Keysight). Effective mobility is calculated using: $\mu_{eff} = \frac{dI_d}{dV_d}\frac{L}{WC_{ox}(V_g - V_t)}$, where C_{ox} is the gate

oxide capacitance, L is the channel length, W is the device width and V_t is the threshold voltage. I_d was measured at low bias (V_d = -0.1 V).

Hall measurement devices were fabricated in a square configuration with an edge length of 5 mm. 30 nm Ni was used as the contact metal. An Ecopia HMS 300 Hall measurement tool with a ~0.55 T permanent magnet was used to measure the carrier concentration and Hall mobility by van der Pauw method.

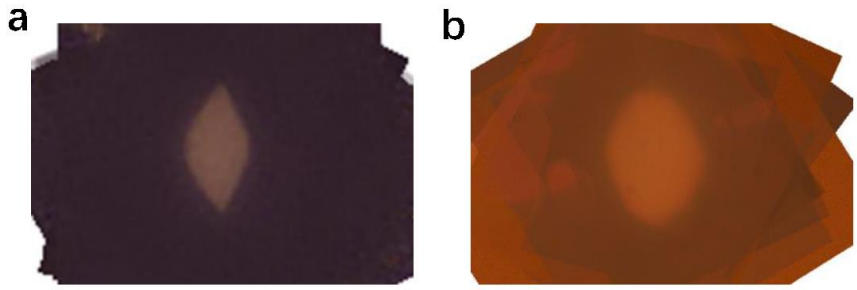
Characterizations. XRD measurement was performed on a Rigaku SmartLab X-ray diffractometer system with a Cu X-ray source (λ = 1.5406 Å). For Figure 3.2.1, as-deposited 50-nm-thick Te samples were kept at ~0 ^{o}C to prevent the crystallization during the XRD measurement. Then we recovered the sample temperature to room temperature for crystallization and performed XRD measurement on the crystallized Te film again. For Supplementary Figure 3.8.8b, we transferred and restacked 0 ^{o}C crystallized 8-nm-thick Te films layer by layer for 7 times using a PDMS stamp to enhance the XRD signal. Raman spectrums were measured on a LabRAM HR Evolution Raman microscope with a excitation line of 532 nm. EBSD measurements were performed using an FEI Quanta field emission gun SEM and an Oxford EBSD detector with a fluorescent screen. TEM characterization was performed on 50-nm thick pattern Te transferred on a SiO_2 support TEM membrane (TED PELLA, INC). TEM characterization was carried on a FEI Titan 60-300 microscope with an acceleration voltage 200 kV at the National Center for Electron Microscopy at Lawrence Berkeley National Laboratory. The optical microscopy images of Te thin films were taken by a homemade polarized optical microscopy.

Video analysis. Images were extracted from the videos and then processed and analyzed using Mathematica.[38] The processing and analysis for each video was done as follows: First, it was observed that the transformation from the amorphous phase to the crystalline phase resulted in an increase in intensity of the image. The fraction transformed was then determined simply as being equal the fraction of the overall intensity change observed over the course of the experiment. (The results so obtained were compared with a more complicated image processing steps involving binarization of the images, as well as computing the intensity change on a per pixel basis. All three methods yielded very similar results, and the differences between the three methods were used to assign uncertainties. See the Supplemental Information for details.) All the fitting was done using Mathematica's NonlinearModelFit. Similarly, the growth rates were obtained by fitting an ellipse to crystals before coalescence using the Component Measurements package and tracking its major and minor axis growth.

Simulation of Nucleation and Growth within a Finite Size Region. The nucleation problem within the defined lithographic regions is based on a kinetic Monte Carlo algorithm. Using the initially available areas and edge lengths, the total rate for nucleation is computed. Assuming that nucleation is a Poisson process, we generate a list of nucleation positions and times for a fixed number of grains using standard kinetic Monte Carlo methods.[39] Following JMAK,[27-29] it is assumed that the growth of the grains is 2D and circular.

The kinetic data for our model was derived from movies of the crystallization process, analyzing one movie for each temperature. The movies captured information from an area of 6912 μm^2, and, for the lowest temperatures, included approximately 60 nuclei. The growth area is then meshed with a regular array of points. The time of arrival for each grain is computed for every grid point (every nuclei is presumed to start a grain at this stage). Each grid point is then labelled by the grain number that arrives at that point first and the time of that first arrival. The time at which the last grid point is transformed is checked to make certain that it is before the last grain nucleation event in the event list. If so, the number of grains and the finish time of the simulation are recorded. If not, the simulation is thrown out, the number of nucleated grains is increased, and the simulation is run again. Results of 64 accepted simulations with meshes of 128x128 points are averaged to produce the data in the plot (see 3.8.2 Supplementary information for details).

3.8 Supplementary information



Supplementary Figure 3.8.1. The average crystal shape for Te nuclei at crystallization temperatures of 25 ºC (a) and 5ºC (b). For getting the average shape, we chose several isolated crystals (18 and 9 crystals for crystallization temperature of 25 ºC and 5ºC). These crystals were normalized, aligned and stacked. Then we average crystal shape using the Stack Mode (Medium) in Photoshop. As shown in the images, crystalline nuclei appear with variable shapes ranging from faceted to elliptical at different crystallization temperatures.

3.8.1 Image and Video Analysis

Transformed fraction

We used three algorithms to extract the information about the transformed fraction from the crystallization videos at different temperatures. In the simplest one, we transformed the video frames to gray scale images and selected two reference frames, one before the transformation has started and another after the system has completely crystallized. The values of the individual pixels of these reference frames are added up and labeled l_0 and l_1, for the amorphous and crystalline references, respectively. Then, the transformed fraction of the frame corresponding to time t is given by:

$$f_1(t) = \frac{l(t)-l_0}{l_1-l_0}, \quad \text{(S1)}$$

where $l(t)$ is the sum of the value of the individual pixels of the frame corresponding to time t. A more sophisticated version of the aforementioned algorithm was also used. In this scheme, the transformed fraction for a pixel i at time t, $p_i(t)$, was computed using the equation:

$$q_i(t) = \frac{p_i(t)-p_{i,0}}{p_{i,1}-p_{i,0}}, \quad \text{(S2)}$$

where $p_{i,0}$and $p_{i,1}$are the values of pixel p_i in the amorphous and crystalline reference frames, respectively. Then, the total transformed fraction for the frame is given by

$$f_2(t) = \sum_i q_i(t). \quad \text{(S3)}$$

In the third and last algorithm that we used, we also worked with the frames extracted from the videos. The frames were then processed as follows: first, they were rescaled to 150 X 113 pixels. A high-pass filter with a cutoff frequency of 0.025 was then applied, and the obtained images were then transformed to gray scale. A background image corresponding to the amorphous state was selected. We define the $N(t)$ matrices as:

$$N(t) = R[M(t) - M_0], \quad \text{(S4)}$$

where $M(t)$and M_0 are the matrix representations of the processed frames corresponding to time t and to the reference state, respectively, and $R[M]$ is a rescaling function that ensures that all the values of the matrix M are between 0 and 1. The entries of the $N(t)$ matrices were then binarized by a function of the form:

$$b_h(N_i(t)) = \begin{cases} if N_i \geq h, 1 \\ if N_1 < h, 0 \end{cases} \quad \text{(S5)}$$

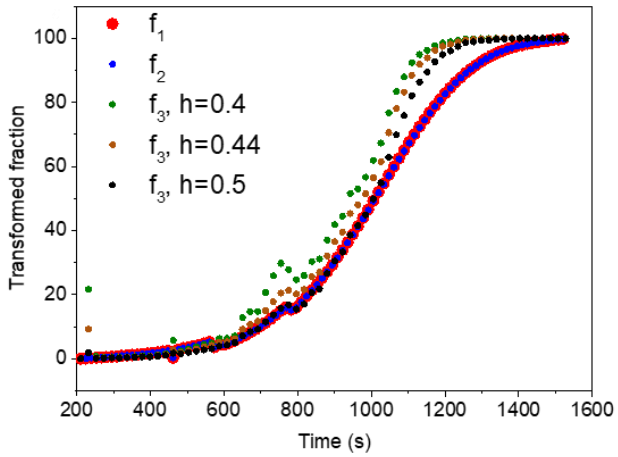
It is important to note that this method depends on the threshold h defined in Equation (S5).

The three methods were applied to the video of the sample held at 10 **°C**. We can see that, even though the same reference images were used, the transformed fraction obtained using the third method, f_3 , differs somewhat significantly from f_1 and f_2, with the difference increasing as the threshold h decreases.

As the first method is the simplest of the three, and it does not have any adjustable parameter besides the selection of the reference frames, results obtained using this method are the ones reported in the main text. In the fitting, we assumed an uncertainty of 0.025 in each of the fractions obtained. A comparison of the results for energy barriers obtained using different methods can be found in Table S1, where we can see that, even though the shapes of transformed fraction curves obtained by using different methods differ for a given temperature (see Supplementary Figure 3.8.2), properties of the system that are obtained by fitting the data of the curves over a range of temperatures, such as those shown in Table S1, yield similar results.

Table S1 A comparison of the results for energy barriers obtained using different methods.

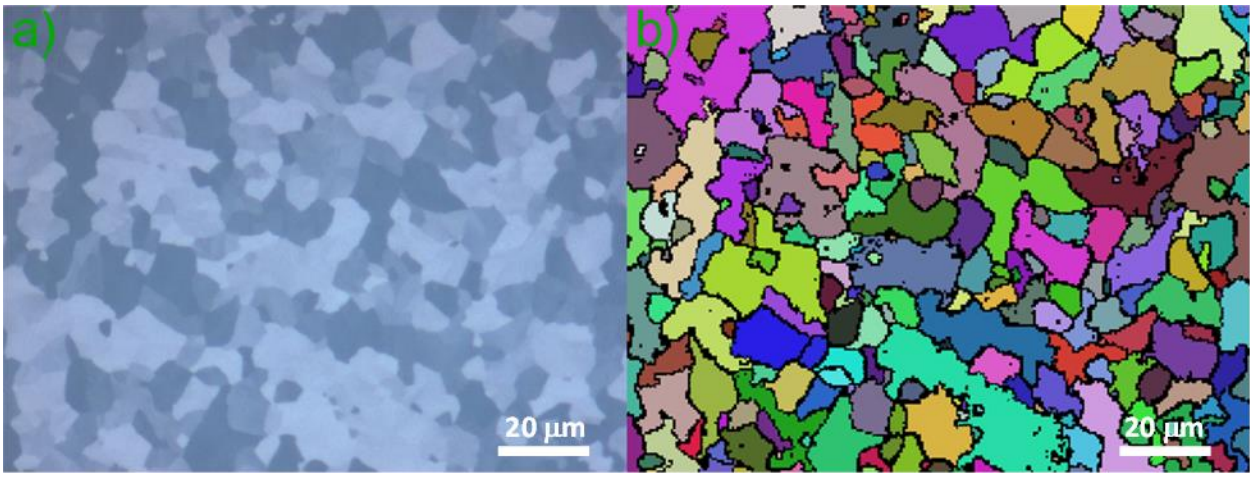
Method	ΔE_v	$\Delta E_{\dot{N}}$
1	0.91 ± 0.11	1.08 ± 0.24
2	0.91 ± 0.11	1.08 ± 0.24
3	0.83 ± 0.23	1.07 ± 0.26



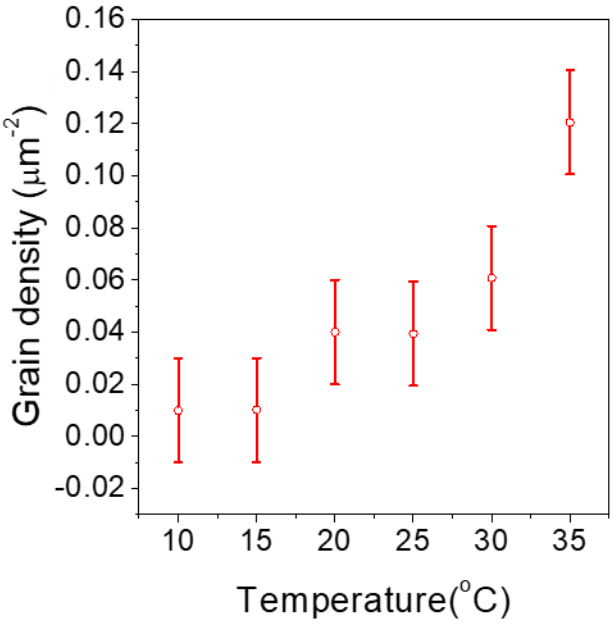
Supplementary Figure 3.8.2. Transformed fraction for the sample held at 10**°C** computed used the three methods with the same reference images.

Grain densities

To obtain the grain density of samples held at different temperatures, images obtained by polarized optical microscopy (Supplementary Figure 3.8.3a) were analyzed. To count the number of grains, we used the Fiji software[27] to process the images as follows: first, contrast was enhanced using histogram stretching and allowing 0.3% of the pixels to saturate; then, the images were transformed from RGB to Luminance; finally, the statistical region merging algorithm[28] with 25 independent random variables per pixel was applied. The output of this process can be found in Supplementary Figure 3.8.3b. From the number of grains, it is straightforward to obtain the nuclei density; these results are shown in Supplementary Figure 3.8.4.



Supplementary Figure 3.8.3. a, Polarized optical microscopy of a sample after the crystallization was completed holding the sample at 15**°C**. **b**, Processed version of (**a**). The image segmentation was done using the statistical region merging algorithm[6] using 25 random variable per pixel. Region colors were assigned just to facilitate differentiation.

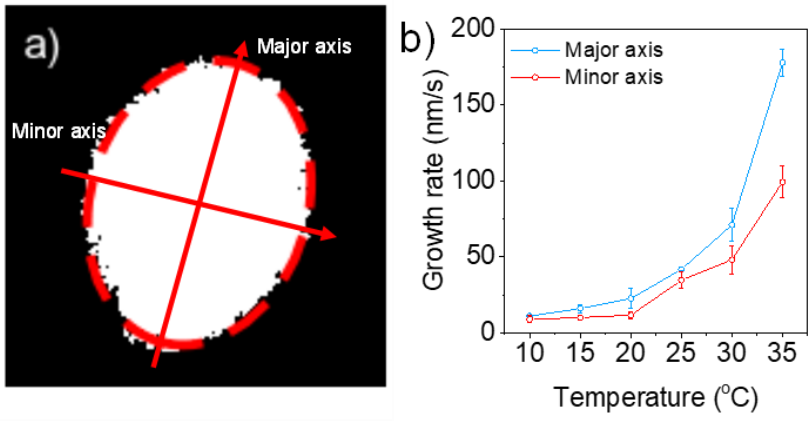


Supplementary Figure 3.8.4. Grain density obtained by segmenting the micrographs of Te samples crystallized at different temperatures. Error bars were set to 0.02 μm^{-2} to account for errors in the digitization of the data.

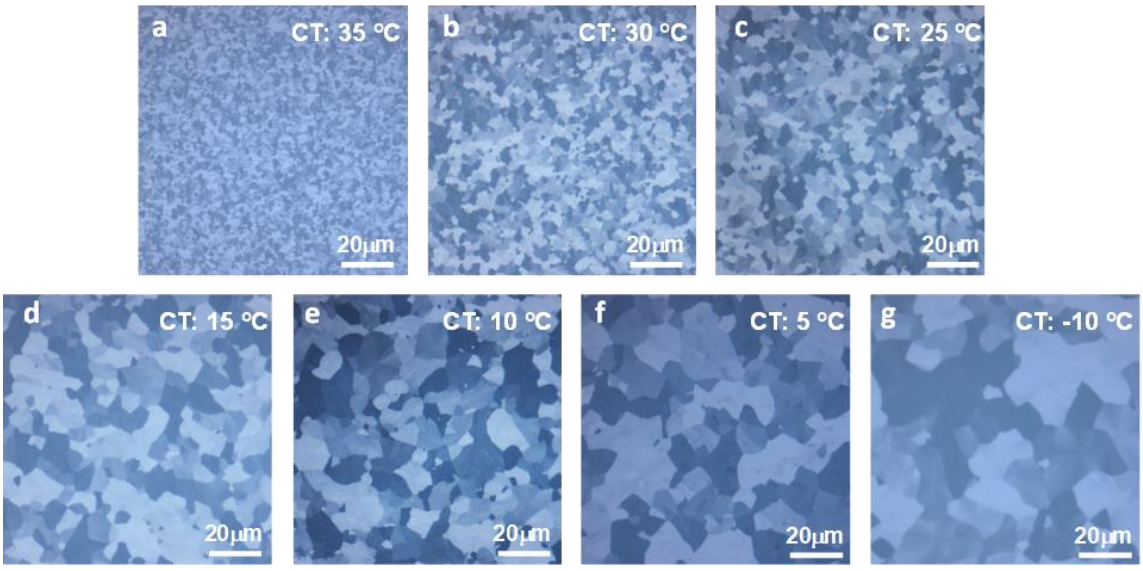
Grain growth

To extract the grain growth velocity from the videos, these were processed and analyzed using Wolfram Mathematica[29]. The processing and analysis for each video frame was done as follows:

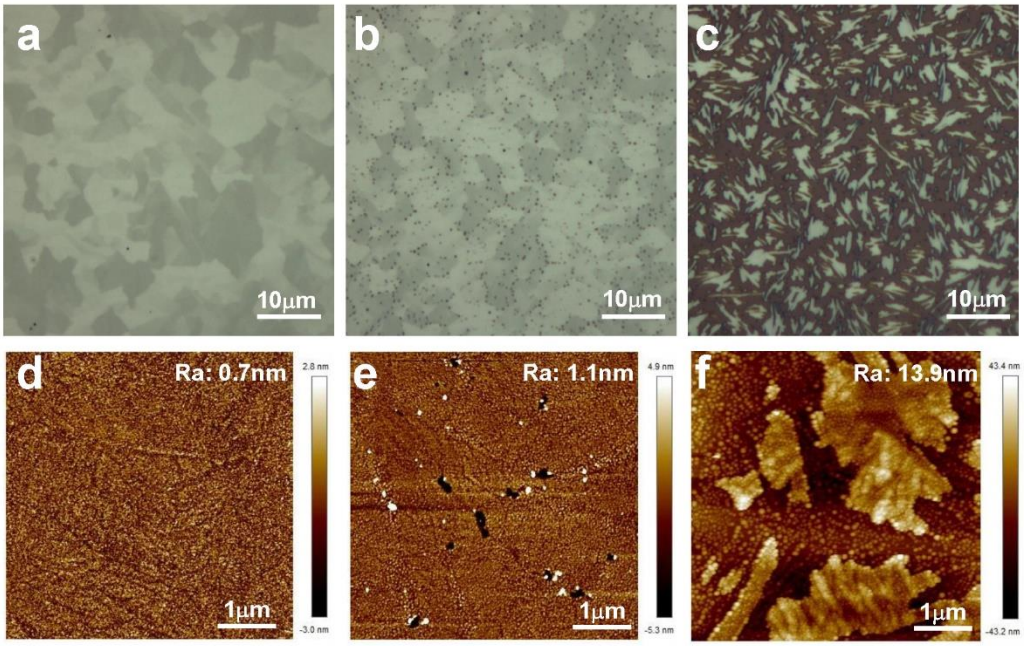
First, all the images were converted to gray scale. Then, a background image was created by averaging all the images corresponding to times previous to crystallization. Second, as the crystals are clearly brighter than the amorphous sections, all the images were binarized by comparing to the background image. Finally, the growth rates were obtained by fitting an ellipse to crystals before coalescence using the ComponentMeasurements package and tracking its major and minor axis growth. An example of the ellipse fit and the results obtained using this method can be found in Supplementary Figure 3.8.5.



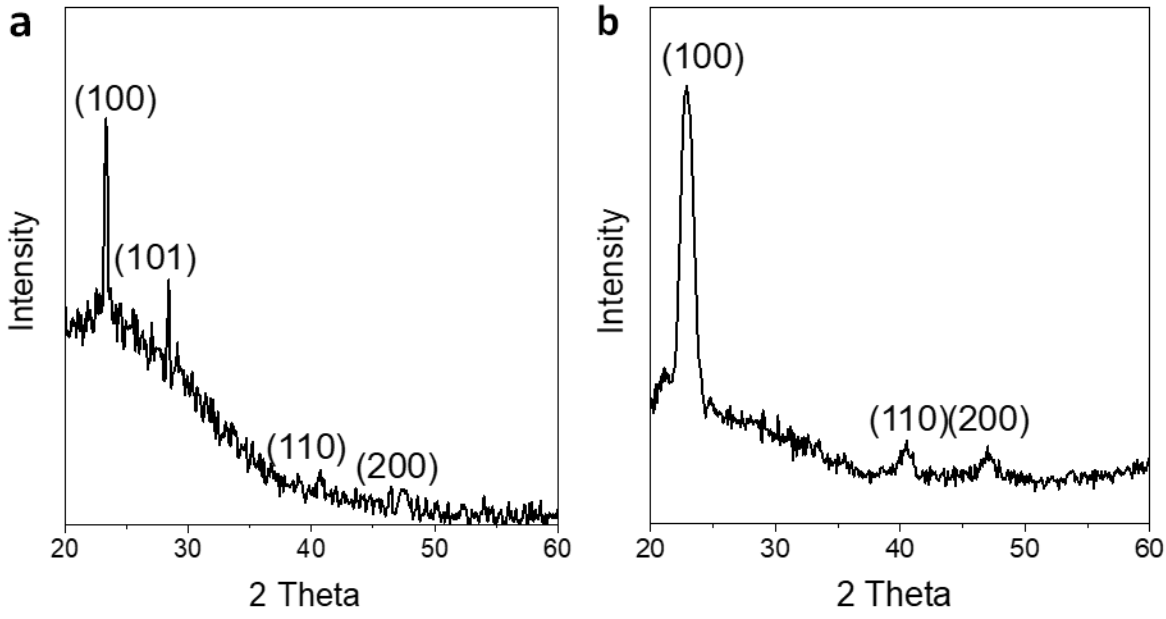
Supplementary Figure 3.8.5. a, Binarized image of a grain and its fitted ellipse. **b**, Growth rate of the major and minor axis of the fitted ellipses for different temperatures. Error bars were obtained as the standard deviation of at least 3 tracked crystals.



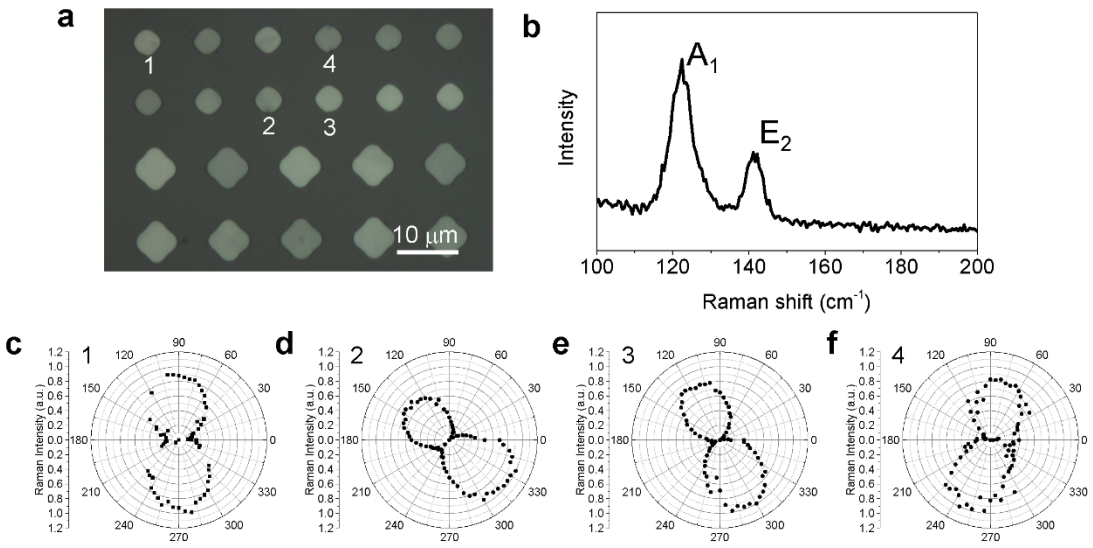
Supplementary Figure 3.8.6. Polarized light microscopy image of the Te films (10 nm) crystallized at different temperature. a, 35 °C, **b,** 30 °C , **c,** 25 °C , **d,** 15 °C , **e,** 10 °C , **f,** 5 °C , **g,** -10 °C .



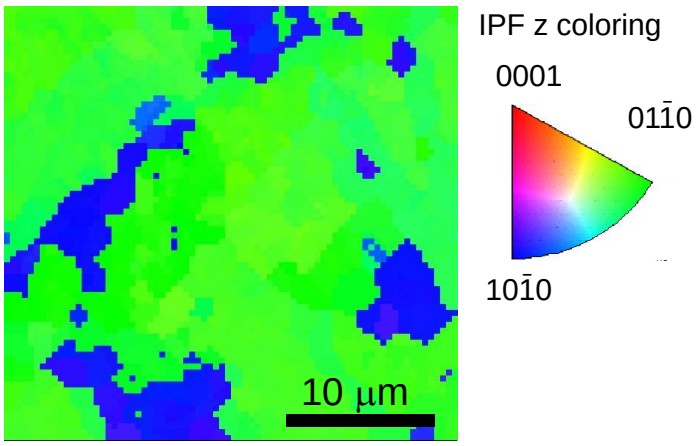
Supplementary Figure 3.8.7. a, Optical (**a-c**) and atomic force microscopy (**d-f**) images of Te films (30 nm) annealed at different temperatures. (**a, d**) As deposited film without annealing, (**b, e**) after annealing at 250 ºC for 5 min, (**d, f**) after annealing at 300 ºC for 5 min. The high temperature annealing creates a rough surface with pinholes. R_a keeps increasing with the temperatures. The film became discontinuous after the 5 min annealing at 300 ºC.



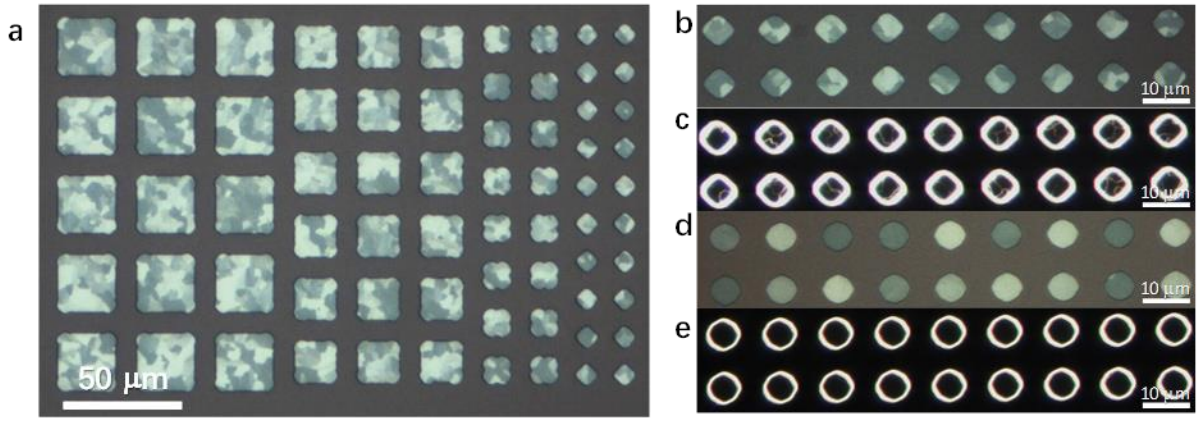
Supplementary Figure 3.8.8. XRD pattern of a 50-nm-thick 25 ºC crystallized Te thin film (**a**) and a transferred and restacked 8-nm-thick 0 ºC crystallized Te thin film (**b**).



Supplementary Figure 3.8.9. a, Optical microscopy image of patterned Te grains. **b**, Ramen spectrum of a Te grain. **c-f**, Angle-resolved Raman spectrum (A_1 mode) was performed on 4 Te grains (as shown in **a**) to determine their in-plane orientations. 4 grains showed us 4 different in-plane orientations, implying the in-plane orientation is random in the films.



Supplementary Figure 3.8.10. EBSD map of a 20 nm thick Te film (crystallized at 5 ^{o}C).



Supplementary Figure 3.8.11. Te arrays crystallized at different temperatures on SiO_2/Si substrate. a, Polarized light microscopy image of the patterned 25 °C crystallized Te (10 nm) array with lateral dimension ranging from 6 μm to 19 μm. **b-c,** High magnification bright-field (**b**) and dark-field (**c**) image of 25 °C crystallized Te (10 nm) array with lateral dimension of 6 μm. **d-e,** High magnificent bright-field (**d**) and dark-field (**e**) image of 0 °C crystallized Te (10 nm) array with lateral dimension of 6 μm.

3.8.2 Kinetic Model for Crystallization for Finite Size Films

The model for nucleation and growth of the crystalline phase within the deposited amorphous phase follows those of Johnson and Mehl[20], Avrami[21] and Komogorov[22] (JMAK). For the infinite (in lateral dimension) film case, nuclei are assumed to form at random locations and random times at a constant rate, and are assumed to grow with a constant velocity. Though our films are not infinitesimally thin, we consider the nucleation and growth process to be 2D. Analysis of the growth process leads to the analytical results presented in the main text.
For a finite film, there is the possibility of nucleation at the edges of the film, and this complicates the problem. Analytical solutions for this geometry are not available. In this case, however, simulation can lend some insight.

The simulations are based on the same assumptions as the analytical model. There are different (but constant) rates of nucleation in the area and at the edges of the film, and growth velocities are taken to be constant. The grains are assumed to grow as circles also at a constant rate. The nucleation rates for the nuclei forming in the area, $\dot{N}_{area}$ are chosen to be those derived from the analysis of the infinite film:

$$\dot{N}_{area} = \dot{N}_o \, exp\left[-\frac{\Delta E_{\dot{N}}+\Delta E_{attach}}{k_B T}\right], \tag{S6}$$

with $\dot{N}_o = 1.13 \times 10^{30}$ μm^{-2} sec^{-1}, $\Delta E_{area} = 1.98$ eV, and k_B Boltzmann's constant. Similarly, the growth velocity is chosen to be that deduced from the infinite films:

$$v = v_o \, exp\left[-\frac{\Delta E_{attach}}{k_B T}\right], \tag{S7}$$

with $v_o = 6.465 \times 10^{15}$ μm sec^{-1}, and $\Delta E_{attach} = 0.91$ eV. The edge nucleation rate is taken to be a parameter used to fit the data.

The simulations are structured as follows. First, the rate of nucleation for the edges and the areas are assigned. The time is set to zero, and a kinetic Monte Carlo process[4] is used to generate the nuclei and the times for nucleation, without regard for whether or not the position of nucleation is already occupied by a crystallized grain. Specifically, the total rate of nucleation is computed as the sum of the edge and area nucleation rates. For a square area of edge length L, the total rate, R, is given by:

$$R = 4\,L\,\dot{N}_{edge} + L^2\,\dot{N}_{area}, \tag{S8}$$

with $\dot{N}_{edge}$ the chosen nucleation rate. The kinetic Monte Carlo begins with the generation of the time increment at which the next event happens. This time increment, Δt is given by:

$$\Delta t = -\tfrac{1}{R}\log p, \tag{S9}$$

with p a random number uniformly distributed between 0 and 1. The total time is incremented by Δt, and a second random number, s, uniformly distributed between 0 and 1, is generated. If $s > 4\,L\,\dot{N}_{edge}/R$, the event is chosen to nucleation within the area, and a random point within the interior of the film region is declared to be the position of the nucleus, which is recorded along with the nucleation time. If $s < 4\,L\,\dot{N}_{edge}/R$, a random point on the edge of the film is chosen as the nucleation site, and the time of nucleation is then recorded. This process is repeated until the desired number of grains have been nucleated.

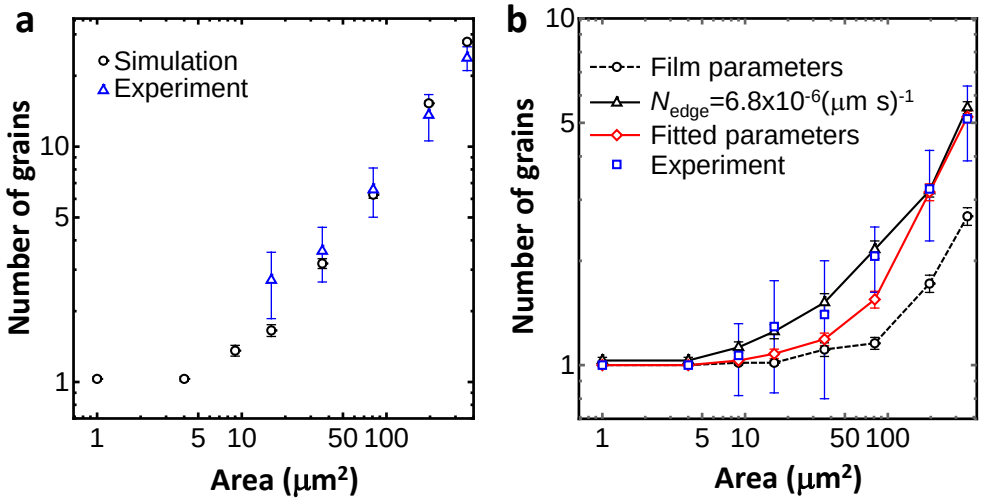
The next step is to construct the microstructure arising from the nuclei. The simulation again follows the assumptions of JMAK in that the grains are all growing unimpeded. The film is divided into a regular array of grid points (e.g. 128×128) and the time at which all the nucleated grains hit each grid point is computed. Each grid point is labeled by the number of the grain that arrives first in time, and the time of the arrival. The maximum arrival time in the grid, then, corresponds to the film growth completion time. This time is compared with the largest nucleation time in the list of grains. If the completion time exceeds the largest nucleation time, the simulation is discarded, the initial number of nucleated grains is increased, and the process is repeated.

While these simulations provide much data, this work is focused on the number of grains within a finite size sample. To make comparison with experiment, 64 simulations at each set of parameters is run to generate the simulated data shown in the plots. The uncertainty in the number of grains arising from the simulation is reported as the square root of the variance in grain numbers divided by the square root of number of simulations. An empirical comparison of experimental data and the simulated results was used to estimate $\dot{N}_{edge}$, which varies with temperature.

Supplementary Figure 3.8.12 compares the results of simulation with the experimental results for $T = 25$ °C and $T = 0$ °C. At 25 °C, the results of the simulation conducted assuming no edge nucleation, and the parameters extrapolated from the fits to nominally infinite films agree well with the experimental data. Based on this agreement, we conclude that the parameters we have deduced from our analysis are reasonable.

For the case of $T = 0$ °C, the simulation predictions using parameters extrapolated from the experimental data underestimates the number of grains. There are at least to explanations for this discrepancy. The first is that the extrapolated parameters are uncertain. To check this, we examined the sum of the squared residuals, and chose a set of parameters that minimized this sum (within the statistical errors). This curve is represented by the red circles in the plot. To obtain this plot, the nucleation rate, $\dot{N}_{area}$ had to be increased by a factor of 2.9, and the velocity, v, decreased to 0.54 times its originally extrapolated value. If we assume that all the uncertainty lies in the energy barriers, both expressions require adjusting the energy barrier by energies of the order of 25 meV. Clearly, these adjustments are within the range of uncertainty for the extrapolated parameters.

Another possibility is that the edges of the finite size samples used serve as special locations for heterogeneous nucleation. (To be clear, one can view all the nucleation within the thin film as heterogeneous. Here, we are referring to nucleation at the edge of the lithographic domain, which presents a different type of heterogeneity.) Through trial and error, we found that for $T = 0$ °C, adding an edge nucleation rate $\dot{N}_{edge} = 6.8 \times 10^{-6}$ μm^{-1} sec^{-1} produced good agreement between experiment and simulation using the parameters extrapolated from the nominally infinite films. (The edge nucleation rate was the only adjustable parameter in simulation, and the sum of the square of the residuals was lower, though within the uncertainty of the sum given the error bars, on the experimental data and on the simulated points.) This should be contrasted with the results at $T = 25$ °C that seem to show no contribution from an enhanced edge nucleation rate.



Supplementary Figure 3.8.12. Comparisons of simulation predictions to those measured experimentally (**a**) $T = 25$ °C and (**b**) $T = 0$ °C. **a**, At 25 °C, the experimental data is described well by the simulation using the parameters obtained by fitting to the Arrhenius forms for the infinite films. **b**, At 0 °C, the experimental data (blue squares) differs from that predicted from the parameters extrapolated from the behavior of the infinite films (black circles). This discrepancy can be attributed to either the uncertainty in the extrapolations, or due to the influences of nucleation from the edge of the lithographically defined regions. The red circles show simulation data for parameters chosen by examining the squares of the residuals (see text for details). The black triangles describe the behavior including edge nucleation. Both descriptions are reasonable and lie within the error bars of the experimental measurements.

To explore whether or not it is reasonable to have edge nucleation be relevant at $T = 0$ °C and not $T = 25$ °C, one can consider two limiting cases for the infinite film: (1) the case in which edge nucleation rate is zero, and (2) the case when the area nucleation rate is zero. For case (1), the number density of grains is already expressed in terms of the nucleation and growth rates by the JMAK result presented in the main text. For the case in which only edge nucleation is active, we consider only the straight edges, and do not account for the fact that the edge in question makes a closed path in the experimental samples. A straightforward calculation of the number density of islands for the edge nucleation case gives:

$$N_{edge} = \sqrt{\frac{\pi \dot{N}_{edge}}{4\, v}} \tag{S10}$$

where the growth velocity is taken to be the same as the growth velocity for grains nucleated in the area. We can then find the sample size at which the number of nuclei expected from edge only nucleation is equal to the number of nuclei from area only nucleation. Samples larger than this size, will be dominated by area nucleation, and samples below this size will be dominated by edge nucleation. Defining this crossover size to be L_c, we have:

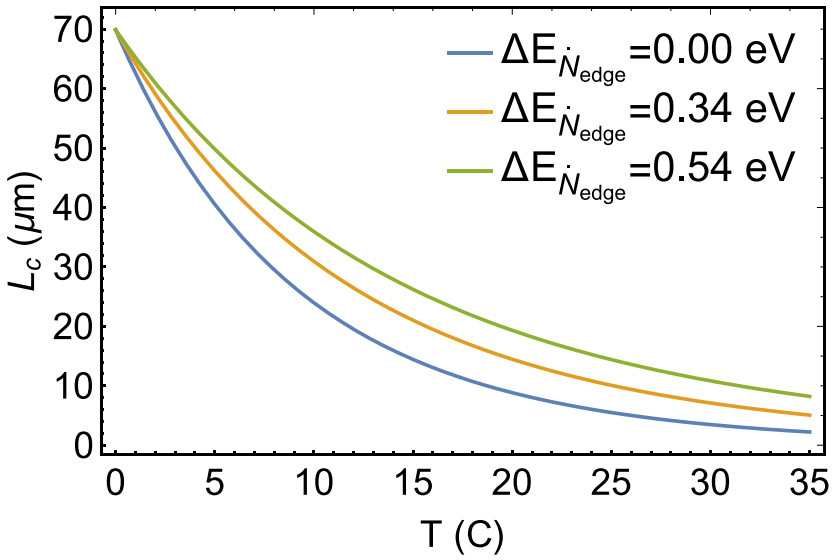
$$L_c = \frac{2\,\pi^{5/6}}{3^{1/3}\Gamma[4/3]} \frac{\dot{N}_{edge}^{1/2}\, v^{1/6}}{\dot{N}_{area}^{2/3}}. \tag{S11}$$

In general, we expect the edge nucleation rate per unit length to have the Arrhenius form:

$$\dot{N}_{edge} \sim exp\left(-\frac{\Delta E_{\dot{N}_{edge}} + \Delta E_{attach}}{k_B T}\right) \quad \text{(S12)}$$

The attachment energy barrier is presumed to remain the same as that for the area-based nucleation events. We expect that $\Delta E_{\dot{N}_{edge}}$ will be smaller than $\Delta E_{\dot{N}}$. Since we do not know *a priori* what might be a good choice for $\Delta E_{\dot{N}_{edge}}$, we plot L_c for a range of $\Delta E_{\dot{N}_{edge}}$ in Supplementary Figure 3.8.13. The prefactor of the Arrhenius form in each case was determined by the fact that at 0 ºC, the edge nucleation rate is $\dot{N}_{edge} = 6.8 \times 10^{-6}$ μm^{-1} sec^{-1}.

The analysis thus predicts that at lower temperatures, edge nucleation will become a more significant contributor. It also predicts that for 25 ºC, the crossover should occur for samples as small as ~30 μm^2, but may in fact occur at larger samples. The data presented in Figure 3.4.1 is consistent with a crossover at 30 μm^2 or so. Given that this analysis is rudimentary, we conclude that it is indeed possible to see the effects of edge nucleation at 0 ºC, while not finding them at 25 ºC (for the size samples we measured).

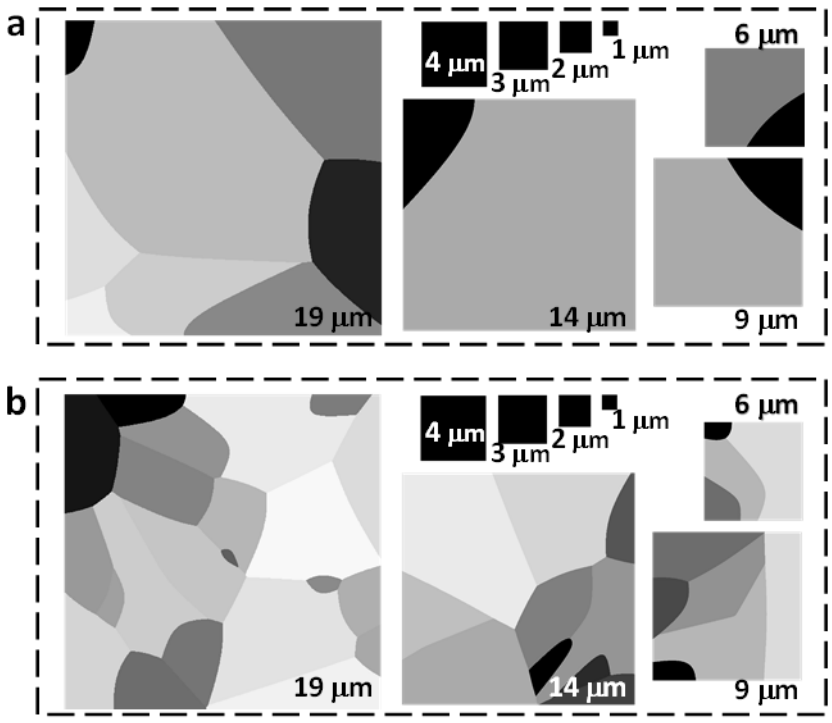


Supplementary Figure 3.8.13. A plot of the crossover length for edge dominated vs. area dominated growth as a function of temperature for various values of $\Delta E_{\dot{N}_{edge}}$. At 25 ºC, the crossover is predicted to fall between samples with edge lengths varying from around 5.5-14 μm. At 0 ºC, the crossover is predicted to appear at a much higher value.

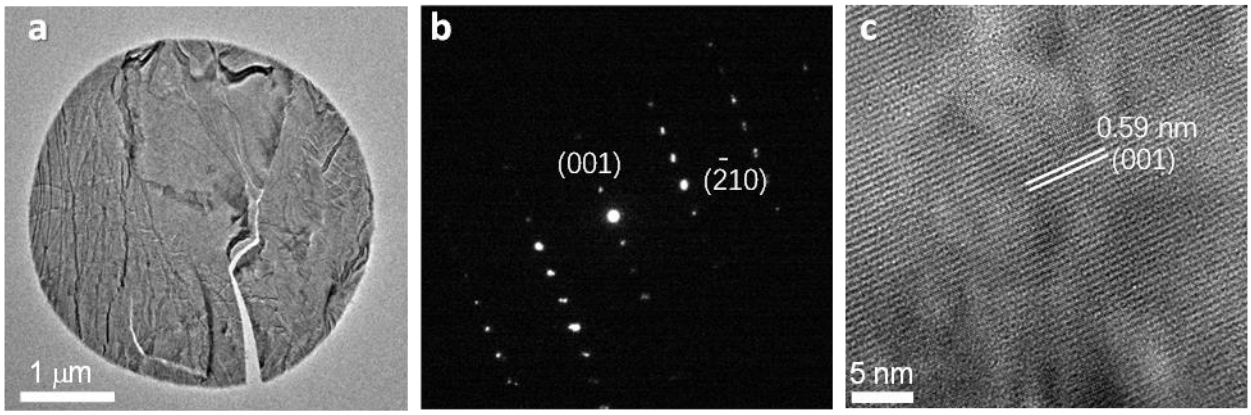
Thus, the two models (adjusted parameters vs. enhanced edge nucleation rate) both describe the experimental data within reason. For now, we note that edge nucleation seems to give a better "fit" (as far as the sum of squared residuals is concerned), and requires fitting only one parameter. For illustrative purposes, we use this model in the main text. We also note that regardless of the

specific model used, this analysis shows that the Arrhenius forms deduced from experiments can describe experiments not used to obtain the parameters.

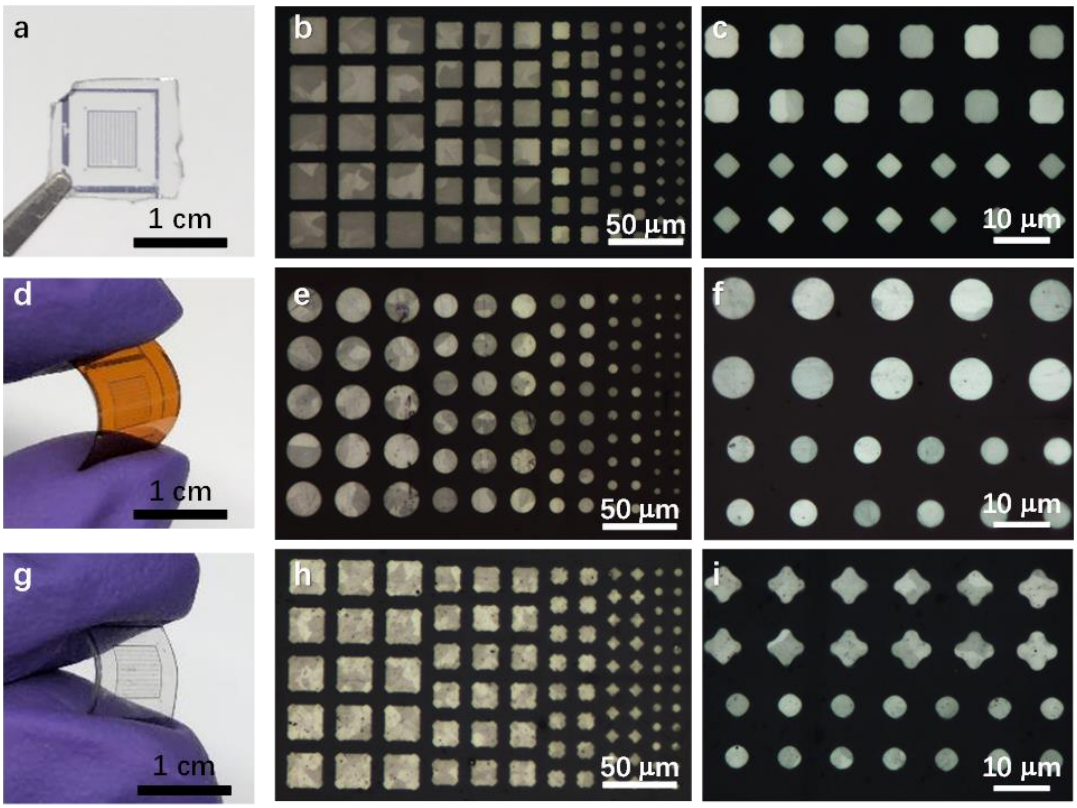
Typical simulated microstructures arising are shown in Supplementary Figure 3.8.14. These grain structures can be compared to those in the main text and in Supplementary Figure 3.8.11. Though the nuclei are different shaped, and the growth velocities are anisotropic when measured directly, the simulations are still able to capture the processes essential to the crystallization process.



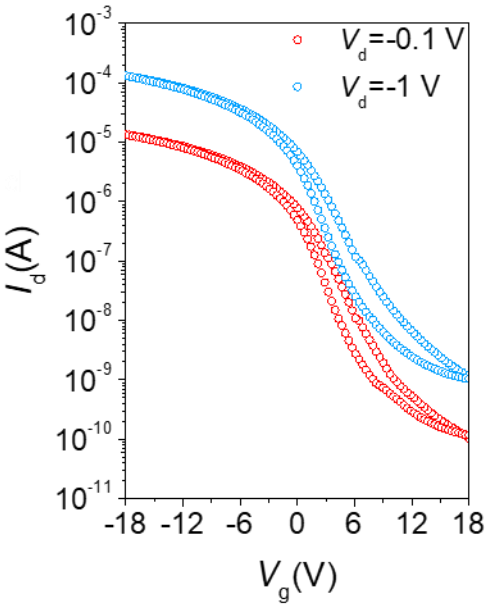
Supplementary Figure 3.8.14. Typical grain structures arising from the simulations for (**a**) T= 0 ºC, and for (**b**) T = 25 ºC. The largest frame in each image is 19×19 μm^2. Each grain is a different shade of gray. Images that are completely black consist of a single grain.



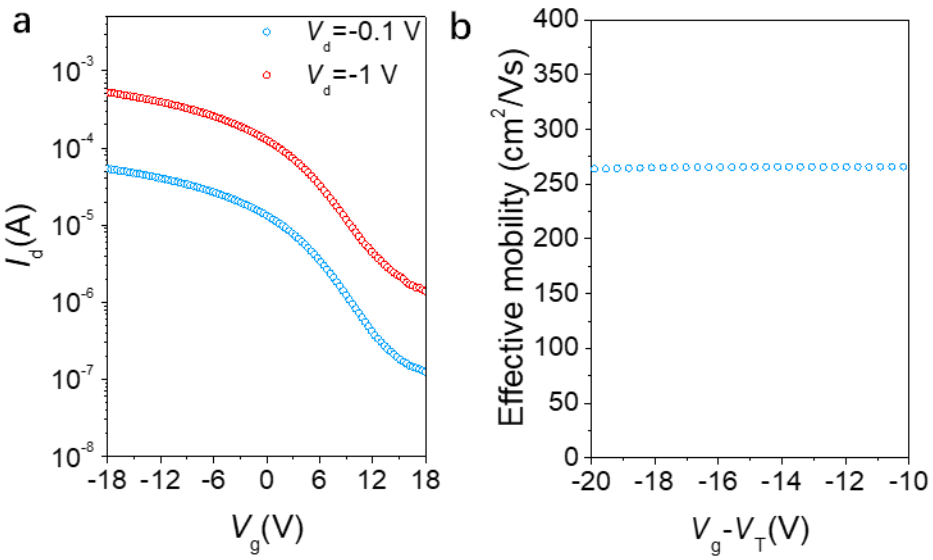
Supplementary Figure 3.8.15. TEM characterization on a transferred 50-nm-thick 0 ºC crystallized Te film. a-c, TEM image (**a**), selective area diffraction pattern (**b**) and high-resolution TEM image of a transferred 50-nm-thick 0 ºC crystallized Te film.



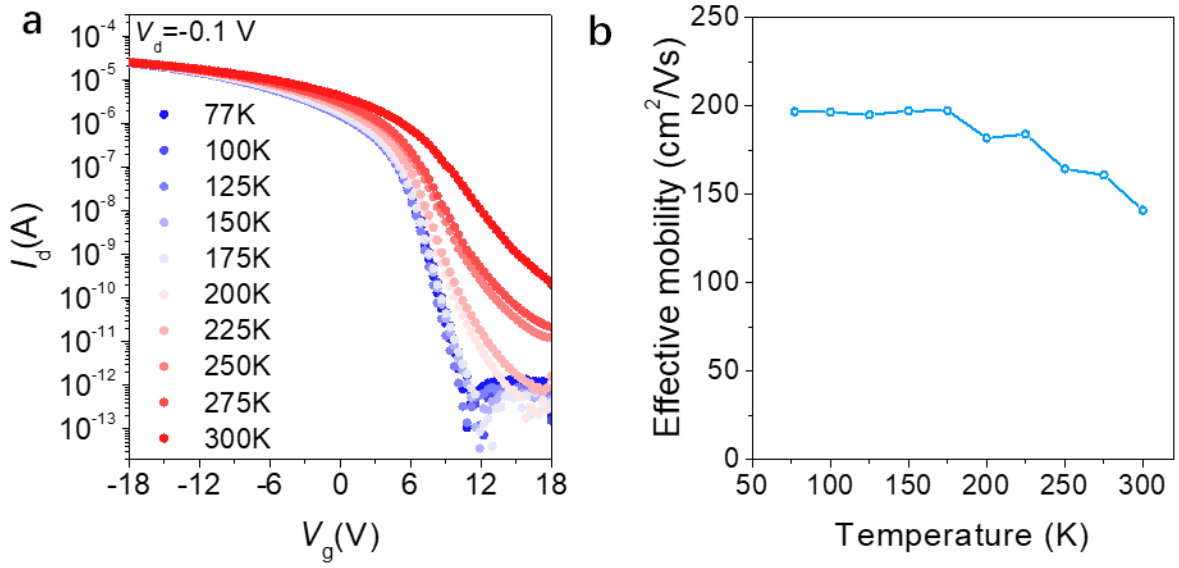
Supplementary Figure 3.8.16. 0 ºC crystallized Te arrays on different substrates. a-c, Photograph (**a**), low (**b**) and high (**c**) magnification polarized light microscopy image of patterned 0 ºC crystallized Te (10 nm) arrays on quartz substrate. **d-f,** Photograph (**d**), low (**e**) and high (**f**) magnification polarized light microscopy image of patterned 0 ºC crystallized Te (10 nm) arrays on Kapton substrate. **g-i,** Photograph (**g**), low (**h**) and high (**i**) magnification polarized light microscopy image of patterned 0 ºC crystallized Te (10 nm) arrays on PET substrate.



Supplementary Figure 3.8.17. I_d-V_g transfer curves of the Te transistor in Figure 6c under forward and reverse sweeping directions.



Supplementary Figure 3.8.18. I_d-V_g transfer curves (a) and derived effective mobility (b) for the transistor based on a 19-nm-thick 0 ºC crystallized Te film.



Supplementary Figure 3.8.19. Temperature-dependent electrical characterization. a, Temperature-dependent I_d-V_g transfer curves of an 8-nm-thick 5 °C crystallized tellurium FET measured over a range of 78 K to 300 K (the channel length = 10 μm; the channel width = 12 μm). **g**, Temperature-dependent effective mobility derived from the transfer curves in **e** (derivation details for effective mobility are introduced in Characterization section).

3.9 References

[1] Y. Taur, T. H. Ning, *Fundamentals of modern VLSI devices*, Cambridge University press, 2013.

[2] C. Zhao, C. Tan, D.-H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, *Nature Nanotechnology* **2020**, 15, 53.

[3] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. A. Goddard, M. J. Kim, X. Xu, *Nature Electronics* **2018**, 1, 228.

[4] M. Amani, C. Tan, G. Zhang, C. Zhao, J. Bullock, X. Song, H. Kim, V. R. Shrestha, Y. Gao, K. B. Crozier, *ACS Nano* **2018**, 12, 7253.

[5] W. Wu, G. Qiu, Y. Wang, R. Wang, P. Ye, *Chemical Society Reviews* **2018**, 47, 7203.

[6] S. Lin, W. Li, Z. Chen, J. Shen, B. Ge, Y. Pei, *Nature Communications* **2016**, 7, 1.

[7] S. Park, B. L. Clark, D. A. Keszler, J. P. Bender, J. F. Wager, T. A. Reynolds, G. S. Herman, *Science* **2002**, 297, 65.

[8] K. Okuyama, M. Chiba, Y. Kumagai, *Japanese Journal of Applied Physics* **1979**, 18, 507.

[9] K. Okuyama, Y. Kumagai, *Thin Solid Films* **1988**, 156, 345.

[10] K. Okuyama, Y. Kumagai, *Journal of Applied Physics* **1975**, 46, 1473.

[11] A. De Vos, J. Aerts, *Thin Solid Films* **1977**, 46, 223.

[12] R. W. Dutton, R. S. Muller, *Proceedings of the IEEE* **1971**, 59, 1511.

[13] R. Dutton, R. Muller, *Thin Solid Films* **1972**, 11, 229.

[14] K. Okuyama, T. Yamashita, M. Chiba, Y. Kumagai, *Japanese Journal of Applied Physics* **1977**, 16, 1571.
[15] M. A. Dinno, M. Schwartz, B. Giammara, *Journal of Applied Physics 1974*, 45, 3328.
[16] J. L. Ericksen, **1992**.
[17] Y.-H. Cheng, S. W. Teitelbaum, F. Y. Gao, K. A. Nelson, *Physical Review B* **2018**, 98, 134112.
[18] T. Ichikawa, *Physica Status Solidi (b)* **1973**, 56, 707.
[19] A. Koma, O. Mizuno, S. Tanaka, *Physica Status Solidi (b)* **1971**, 46, 225.
[20] W. A. Johnson, *Am. Inst. Min. Metal. Petro. Eng.* **1939**, 135, 416.
[21] M. Avrami, *The Journal of Chemical Physics* **1939**, 7, 1103.
[22] A. N. Kolmogorov, Bull. Acad. Sci. USSR, *Math. Ser* **1937**, 1, 355.
[23] A. Jain, S. P. Ong, G. Hautier, W. Chen, W. D. Richards, S. Dacek, S. Cholia, D. Gunter, D. Skinner, G. Ceder, *Apl Materials 2013, 1, 011002.*
[24] N. A. Blum, C. Feldman, *Journal of Non-Crystalline Solids* **1976**, 22, 29.
[25] G. Blatter, F. Greuter, *Physical Review B* **1986**, 33, 3952.
[26] J. W. Cahn, *Acta Metall*. **1956**, 4, 449.
[27] J. Schindelin, I. Arganda-Carreras, E. Frise, V. Kaynig, M. Longair, T. Pietzsch, S. Preibisch, C. Rueden, S. Saalfeld, B. Schmid, *Nature Methods* **2012**, 9, 676.
[28] R. Nock, F. Nielsen, *IEEE Transactions on pattern analysis and machine intelligence* **2004**, 26, 1452.
[29] S. Wolfram, *The MATHEMATICA® book, version 4*, Cambridge University press, 1999.

CHAPTER 4

Orientated Growth of Ultrathin Tellurium by van der Waals Epitaxy

4.1 Introduction

The study of the tellurium (Te) crystal structure, physical properties, and growth techniques can be traced back to the 1950s[1-4]. Recently, Te, as an elemental van der Waals semiconductor, is attracting resurgent interest due to its thickness and orientation dependent electronic and optical properties[5-8], and application potential in electronics[7, 9], optoelectronics[8], sensors[10], modulators[11] and energy harvesting devices[12]. Te possesses a one-dimensional (1D) crystal structure, where atoms are arranged into spiral atomic chains via covalent bonds, and the adjacent atomic chains are packed hexagonally via van der Waals interactions[4]. It exhibits anisotropic carrier mobility[6], thermal conductivity[13], photoresponse[8] and mechanical properties[14] stemming from the unique 1D crystal structure. To exploit the intriguing thickness and orientation dependent properties of Te, fabrication of high-quality ultrathin Te crystals with controlled orientations is critical.

Top-down exfoliation of the bulk is a common strategy to fabricate two-dimensional (2D) materials. However, unlike some van der Waals materials such as graphite[15] and transition metal dichalcogenides (TMDs)[16] that can be mechanically exfoliated to ultrathin layers by tape, 2D formed Te has not been exfoliated from the bulk due to the relatively strong interaction between neighboring chains[17, 18]. Liquid-phase exfoliation approaches such as sonication and electrochemical methods have demonstrated the ability to produce Te nanosheets, but the size, yield and quality of the products need to be further improved[19]. Several bottom-up approaches, such as the hydrothermal method[7], physical vapor deposition (PVD)[9, 20-22] and chemical vapor deposition[23, 24] have been explored to synthesize 2D Te. Although Te nanosheets and ultrathin films with high crystallinity and electronic properties have been achieved by these techniques, the in-plane orientation of the domains on the substrate was random in most of the work, which impedes utilization of the anisotropic properties of Te. Crystalline substrates were used to induce the alignment of the Te atomic chains[20, 25-28]. Te thin films and flakes grown on single crystalline MgO[20] and mica[26] showed a preferred orientation, where the chains are perpendicular to the substrate, so that these films are expected to have isotropic in-plane properties. Epitaxial growth of Te was observed on single crystalline KBr substrate[27], 2D crystals such as GaS and GaSe[28], and uniaxially-orientated polyethylene[25]. Due to its inherent crystalline anisotropy, Te favors a 1D formed structure and island growth mode, leading to needle-like crystals with a large thickness (tens to hundreds of nanometers) and poor surface coverage[21]. Therefore, oriented growth of ultrathin Te flakes and films is still challenging and lacking.

Here, we systematically investigate the van der Waals epitaxial growth of Te on the surface of TMDs by PVD. Ultrathin Te crystalline films with controlled in-plane orientation have been

demonstrated on several substrates with three-fold symmetric surface such as WSe_2, WS_2, $MoSe_2$, MoS_2. The morphology of Te can be controlled from wires to flakes, or even films by tuning the growth conditions such as substrate pre-treatment and growth temperatures. The preferred growth orientation was determined by TEM, which showed the atomic chains were aligned along the armchair directions of these substrates. In addition, diffraction spots corresponding to the moiré structure were observed. Recently, moiré superlattice formed by stacking 2D materials showed unique physical phenomenon and properties[29, 30], however, there are few reports about 1D/2D moirés heterostructures. Orientated growth of SeTe alloys is also demonstrated on WSe_2, the tunable bandgap of which provides the flexibility for band alignment with other materials. The substrate system is extended from the mentioned 3-folded symmetric surfaces to lower symmetry surfaces to realize unidirectional growth of Te chains. We have achieved the growth of textured Te films on WTe_2, where all the Te grains are well aligned in all the directions and c-axis of Te is perpendicular to the tungsten chain direction of WTe_2.

4.2 Growth of Te and SeTe alloys on 3-fold symmetric surface of TMDs

Ultrathin Tellurium was grown by the PVD method using a two-heating zone oven as shown in the schematic diagram (Fig. 4.2.1a). Te powders were used as the precursor and placed in zone 1 at 450 ^oC. Pure Ar gas was employed as the carrier gas to deliver precursor vapor with a flow rate of 50 sccm and pressure of 1.5 Torrs. TMDs flakes were exfoliated onto SiO_2/Si substrates by tape, serving as the epitaxy templates to induce the orientated growth of Te. Substrates were loaded in the downstream region (zone 2) with controlled temperatures ranging from 100 ^oC to 170 ^oC. Pre-annealing of the substrates and the growth temperature have critical influence on the growth (see 4.5 Method). WSe_2 was used as a model TMD substrate to investigate the effect of these mentioned growth conditions.

Fig. 4.2.1b and 4.2.1c show the optical microscopy and scanning electron microscopy (SEM) images, respectively, of the grown Te on WSe_2 surface (WSe_2 substrate was pre-annealed at 300 ^oC, and substrate growth temperature was 100 ^oC). Unlike the 1D needle-shaped crystals in most of the published results[21, 25], Te grown on WSe_2 surface exhibits a 2D form with a lateral dimension of several micrometers. The nanosheets are able to merge the adjacent flakes, which tend to form a continuous film. The thickness of the flakes was determined by atomic force microscopy (AFM). Te flakes have smooth surface and uniform thickness of about 7 nm as shown in Fig. 4.2.1d. In addition, these flakes are well orientated on the WSe_2 surface with a peak distribution at every 60 ^{o} (statistic result from 79 flakes in Fig. 4.2.2). Given consideration to the *C3v* symmetry of the WSe_2 surface, Te atomic chains are well aligned along the specific directions of WSe_2, indicating a van der Waals epitaxial growth.

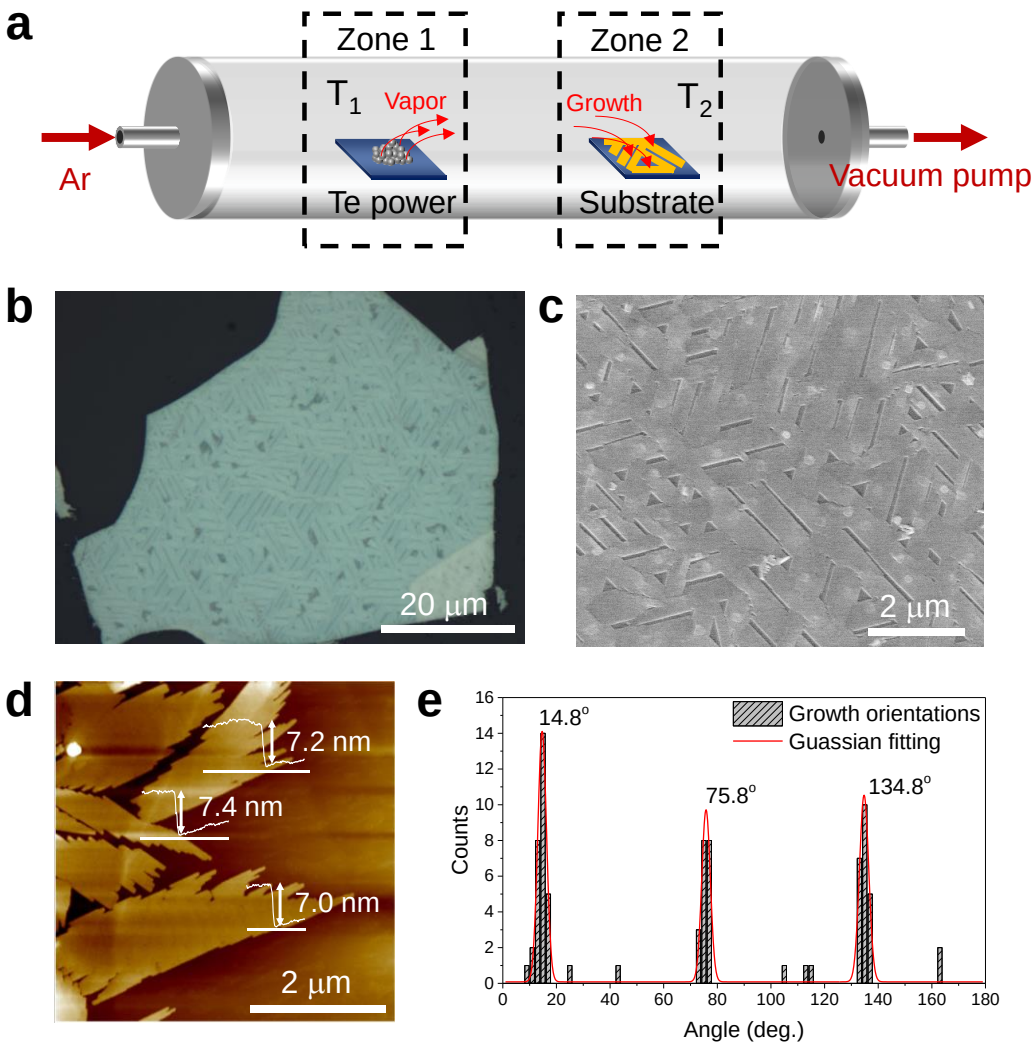


Figure 4.2.1 | Characterization of Te grown on WSe_2 substrate. a, Schematic of the growth system. **b-c,** Optical **(b)** and SEM **(c)** images of the orientated ultrathin Te on WSe_2 substrate. **d,** Tapping mode AFM and the corresponding height image of the grown Te flakes. **e,** Statistical distribution of the orientation angle of Te in Fig. S, which is fitted by Gaussian fitting.

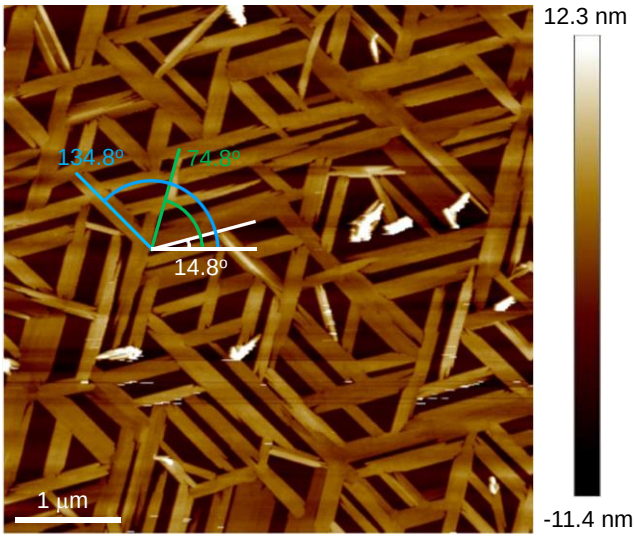


Figure 4.2.2 | AFM image of the orientated ultrathin Te on WSe_2 substrate.

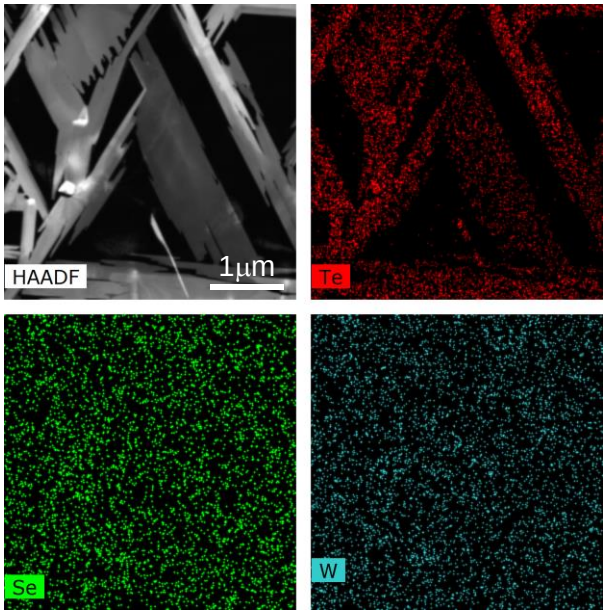


Figure 4.2.3 | EDS maps of the orientated ultrathin Te on WSe_2 substrate.

The grown Te/WSe_2 heterostructure were transferred onto a carbon coated transmission electron microscopy (TEM) grid. Energy dispersive x-ray spectroscopy (EDS) maps demonstrated the flakes were Te (Fig. 4.2.3). TEM was performed on the flakes to investigate the crystallinity of the Te nanosheets and the preferred growth orientations (Fig. 4.2.4a). Firstly, we collected selected area electron diffraction (SAED) pattern from the WSe_2 substrate in region 1 to determine its orientation as shown in Fig. 4.2.5. Then, SAED was performed on the Te flake in region 2. Two sets of diffraction patterns from Te and WSe_2 were observed in the SAED image as shown in Fig. 4.2.4b, indicating the single crystalline nature of the grown Te flakes. The spots in red circles are from WSe_2 substrate, which are consistent with the data collected from region 1(Fig. 4.2.5). The

Te signal has been labeled and indexed in blue. The nearest blue spots from the center correspond to the (0001) and (1-210) planes of Te, which are supported by lattice observed in the high-resolution TEM. The preferred growth direction is identified by the relative orientation between the two sets of diffraction patterns of Te and WSe_2, where the Te atomic chains are aligned along the armchair direction of WSe_2 as shown in Fig. 4.2.4d. Additional weak spots, which are not from each individual layer, were observed in the diffraction pattern, and labelled in green in Figure 2b. These spots imply a periodic structure along the [1-210] direction of Te with a length of 0.67 nm (Fig. 4.2.4c). These diffraction patterns are caused by the moirés structure formed at the 1D (Te)/2D (WSe_2) van der Waals interface based on the lattice parameters of bulk WSe_2 (a = 0.330 nm) and Te (a = 0.445 nm) along the [1-210] direction of Te as shown in the Fig. 4.2.4d. Rich physics has been discovered in the moiré structures formed by twisting and/or stacking 2D materials[29, 30], however, there are few reports about the construction or properties of 1D/2D van der Waals moirés superlattices. The structure grown here can be an interesting platform for the fundamental study of the 1D/2D moirés structure. We characterized two more flakes in region 3 and 4 (Fig. 4.2.5), which showed the same preferred growth orientation and moiré diffraction patterns. These results demonstrate the orientated growth of crystalline ultrathin Te on WSe_2 by van der Waals epitaxy.

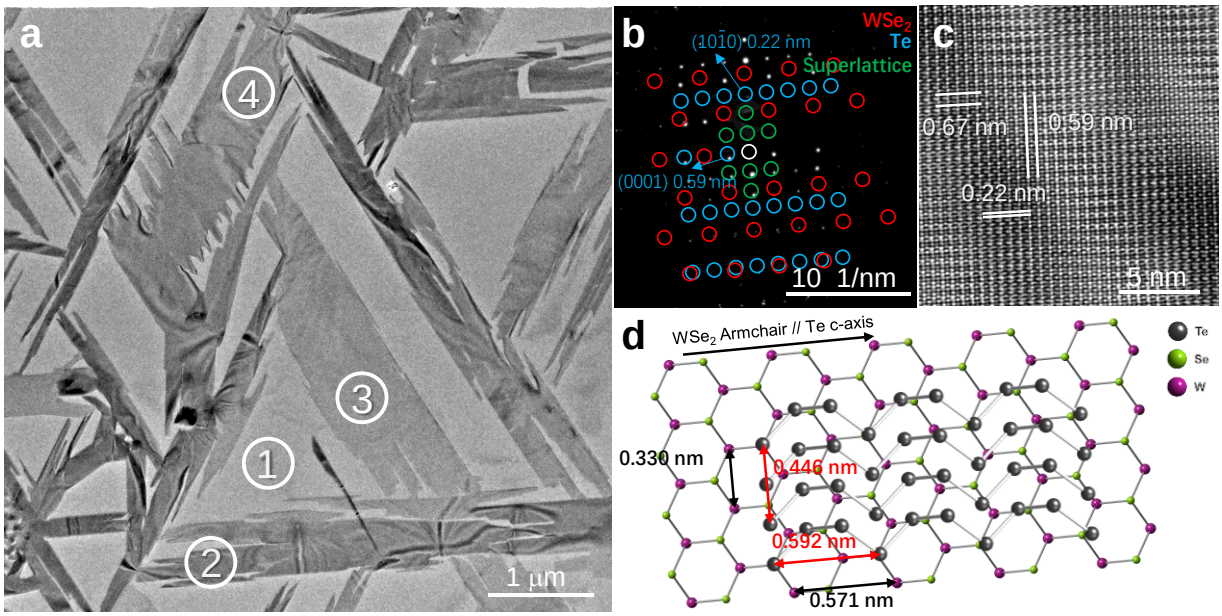


Figure 4.2.4 | TEM characterization of the grown Te/WSe_2 heterostructure. a, TEM image of the Te/WSe_2 heterostructure. Electron diffraction patterns were collected from region 1 (pristine WSe_2 substrate) and regions 2-4 (Te/WSe_2 heterostructure). **b-c,** Electron diffraction pattern (**b**) and Fourier-filtered HRTEM image (**c**) from region 2. **d**, Schematic of the alignment between Te atomic chains and WSe_2 surface based on **b** and **c**, where the c-axis of Te is parallel to the armchair direction of WSe_2.

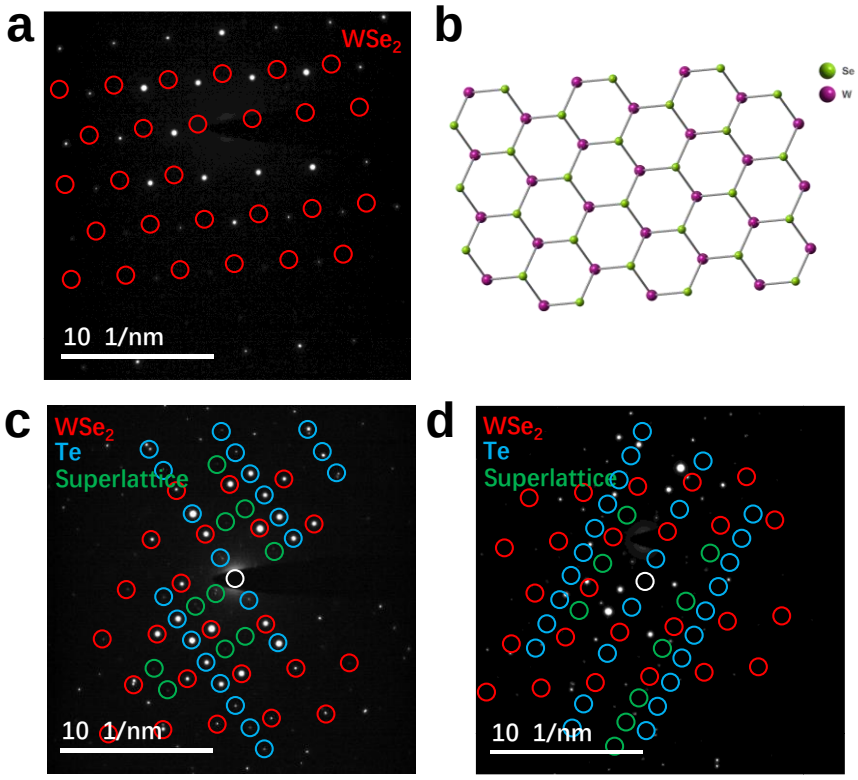


Figure 4.2.5 | TEM characterization of the grown Te/WSe_2 heterostructure. a-b, SAED pattern (**a**) collected from region 1 (WSe_2 substrate) and the corresponding crystal orientation (**b**). **c-d**, SAED patterns collected from regions 3 (**c**) and 4 (**d**).

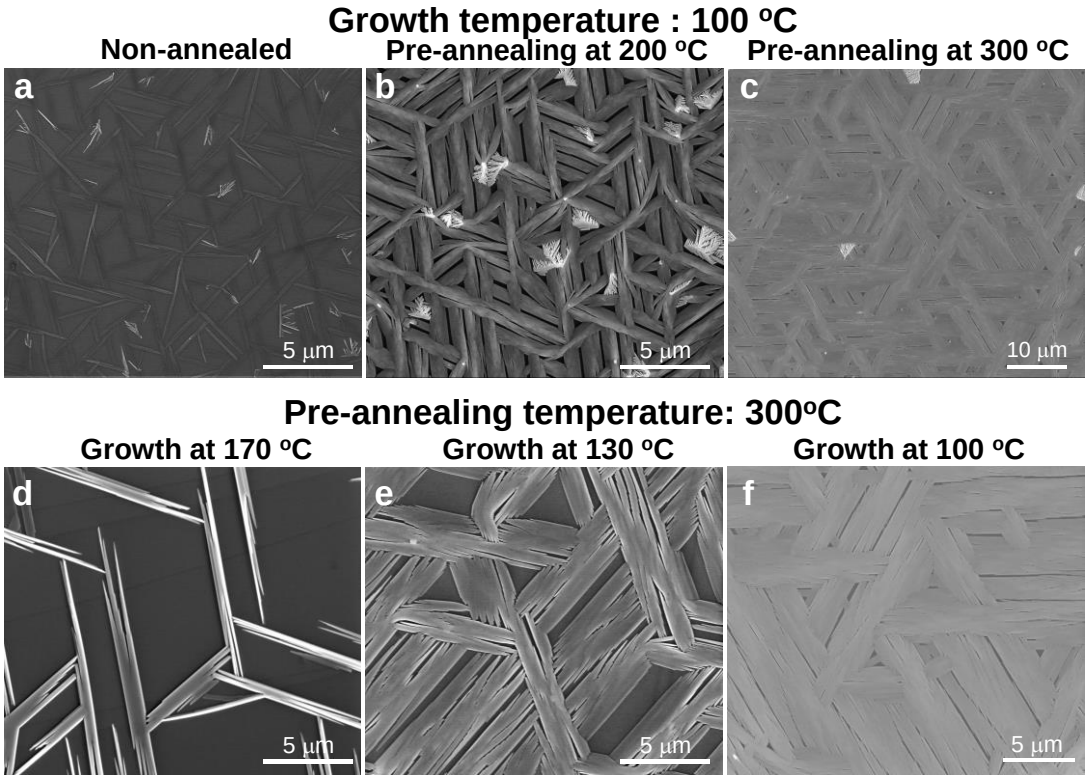


Figure 4.2.6 | Morphology of Te grown on WSe_2 under different conditions. a-c, Te grown at 100 ºC on the non-annealed (**a**), 200 ºC (**b**) and 300 ºC (**c**) annealed WSe_2 substrates. **d-f**, Te grown at temperatures of 170 ºC (**d**), 130 ºC (**e**) and 100 ºC (**f**) on the 300 ºC pre-annealed WSe_2 substrates.

The morphology of the grown Te can be significantly influenced by the pretreatment of the substrate (see Methods). As shown in Fig. 4.2.6a, Te showed a 1D needle-like structure on the untreated, as-exfoliated WSe_2 flakes. 79 % of the flakes exhibited preferred growth orientation along the armchair directions, while the other 21% flakes grew along the zigzag directions. Te grown on the annealed substrates tends to form 2D structures as shown in Fig. 4.2.6b and c. The yield of armchair orientated flakes increases to 93% after a pre-annealing of WSe_2 substrate at 200 ºC (Fig. 4.2.6b). The flakes, retaining the orientated nature, grow and merge into a film with a surface coverage of 95% on the WSe_2 substrate pre-annealed at 300 ºC. Fig. 4.2.6a-c indicate that the films are more uniform after pre-annealing. We further investigate the influence of substrate temperature on the growth. Te was grown on the annealed WSe_2 flakes (annealing temperature was 300 ºC) at temperatures ranging from 170 ºC to 100 ºC. As shown in the Fig. 4.2.6d-f, the morphology of Te changes from 1D needle-like structure to 2D form with the growth temperature decreasing at fixed substrate preparation conditions.

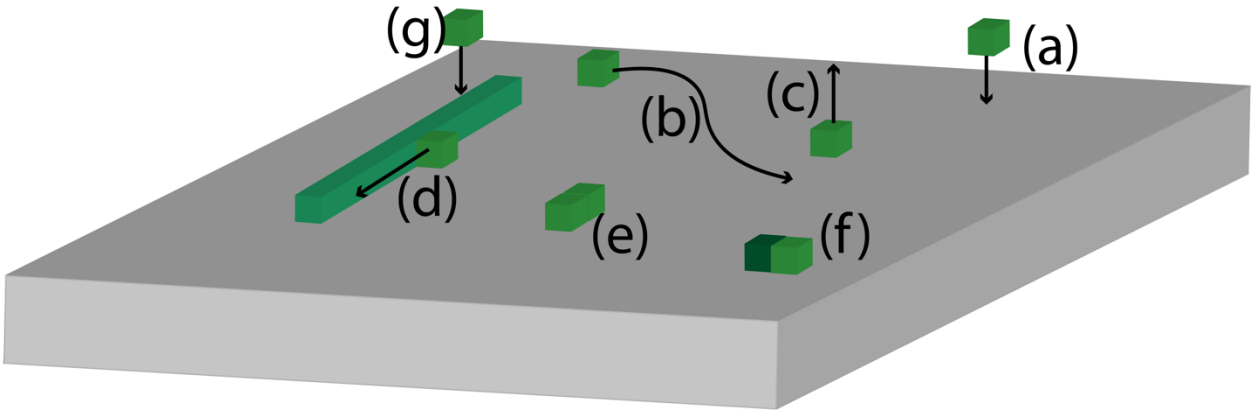


Figure 4.2.7 | Kinetic Processes Affecting Morphology. a, Atoms arrive at the surface from the vapor. **b,** Atoms diffuse on the surface and **c,** may desorb from the surface if they do not encounter a trapping site. **d,** Existing nuclei can serve as a trapping site. Once an atom encounters a wire, it is loosely bound and diffuses along the edge of the wire rapidly until it encounters the end of the wire, where it covalently bonds to the chain. **e,** Other atoms may also serve as trapping sites, leading, through standard nucleation kinetics, to homogeneous nucleation. **f,** Pre-existing defects can also serve as trapping sites, and can lead to heterogeneous nucleation. (Here the defect is shown as a darker atom.) **g,** After growth has progressed for some time, atoms will attach directly to nucleated clusters, and multilayer growth can ensue.

The observed patterns of growth can be rationalized within a simple model. Fig.4.2.7 highlights the kinetic processes that appear to be relevant to the growth mechanism. Te atoms are deposited on the surface, diffuse on that surface, and can desorb from the surface (Fig.4.2.7a-c). Note that diffusion of adatoms on a substrate with 3-fold symmetry is expected to be isotropic. The diffusing atoms can encounter trapping sites before desorption. In the case that the trapping site is another diffusing atom, a nuclei may begin to form, growing through the attachment of additional diffusing atoms (Fig.4.2.7e). Alternatively, the trapping site might be a surface defect, such as a Se vacancy in the substrate, or a Te substitutional defect in the substrate (Fig.4.2.7f). Finally, an adatom can encounter a stable cluster of Te atoms, and begin to diffuse along its edge (Fig.4.2.7d). At later stages of growth, atoms can attach directly to existing Te islands, and thus thicken the films (Fig.4.2.7g).

These processes can be used to understand the morphology of the growth. First and foremost, the growth shape of the crystals is determined by the relative rates of diffusion along the wire, vs. diffusion at its ends. Since the Te interchain bonds are primarily of van der Waals character, one expects that edge diffusion (Fig.4.2.7d) will be very rapid relative to the diffusion of Te atoms on a pristine (0001) surface because those Te are covalently bonded to the chains. These relative rates explain the aspect ratio of the growing wires, as well as the fact that the (0001) facets of the growing plates are very rough, and perhaps even display a fingering instability [31].

The potential for desorption helps to explain the fact that the growth rate of the films depends upon temperature and pre-annealing conditions. First, density functional theory (DFT) total energy calculations suggest that the binding energy of the Te film to the substrate is quite weak, 10 mJ/m^2,

which is consistent with a high probability for desorption of diffusing Te atoms. (See Methods for a description of the DFT calculations.) With no pre-annealing, the number of surface trapping sites (Fig.4.2.7f) is at a minimum. The potential for an atom to be bound to a trapping site is low, and the average desorption rate of the deposited Te atoms is maximized. Pre-annealing leads to the production of Se vacancies in substrate [32, 33], and DFT predicts that these will trap a Te atom with a binding energy of 4.9 eV. Thus, one expects that the vacancies will become substitutional Te defects. The substrate Te substitutional defects then act as a trapping site for additional Te atoms. DFT predicts that this binding energy is 1.6 eV, which is greater than that computed for a Te atom binding in a pristine substrate by 95 meV. So, on average, a Te atom has a longer residence time on the substrate for a pre-annealed sample.

The nucleation rate of clusters is probably a combination of heterogeneous and homogeneous nucleation. Consider the growth morphologies of Fig.4.2.6a-c. Clearly, pre-annealing at 200 ^{o}C leads to a higher nucleation rate than that without pre-annealing. This is most likely due to heterogeneous nucleation (Fig.4.2.7f). However, it appears that as the pre-annealing temperature is increased to 300 ^{o}C, the nucleation rate decreases. A possible explanation for this is that the vacancies produced in the substrate begin to cluster. DFT predicts that the Se divacancy in WSe_2 is bound by 105 meV. If true, as the vacancies form, the number of clusters depends on the ratio of the diffusion coefficient to the rate of production of vacancies [34]. If this ratio increases rapidly with temperature, then the number of clusters in the 300 ^{o}C pre-annealing case will be reduced relative to the 200 ^{o}C pre-annealing treatment, and the heterogeneous nucleation rate will be, accordingly, decreased.

Once the clusters are nucleated, they grow through the aggregation of atoms, both from the vapor and from the surface. Occasionally, if two atoms bound to the edge of a wire encounter one another, they can nucleate and adjacent wire, and the width of the flake increases. Alternatively, a Te atom diffusing along the edge of a wire may encounter and bind to a Te substitutional defect in the substrate. This bound atom would start a new chain that would align with the original. In this manner, the growing needles can expand to become a film.

The orientation of the wires (armchair vs. zigzag) are determined by both kinetics and thermodynamics. Though the films are not strongly bound to the substrate, the symmetry of the substrate clearly impacts the growth morphology. Empirically, the chains aligned along the armchair direction seemed favored, but it is difficult to assess the relative binding energies of the two configurations using DFT because the size of the cells necessary to obtaining a low stress configuration are prohibitive.

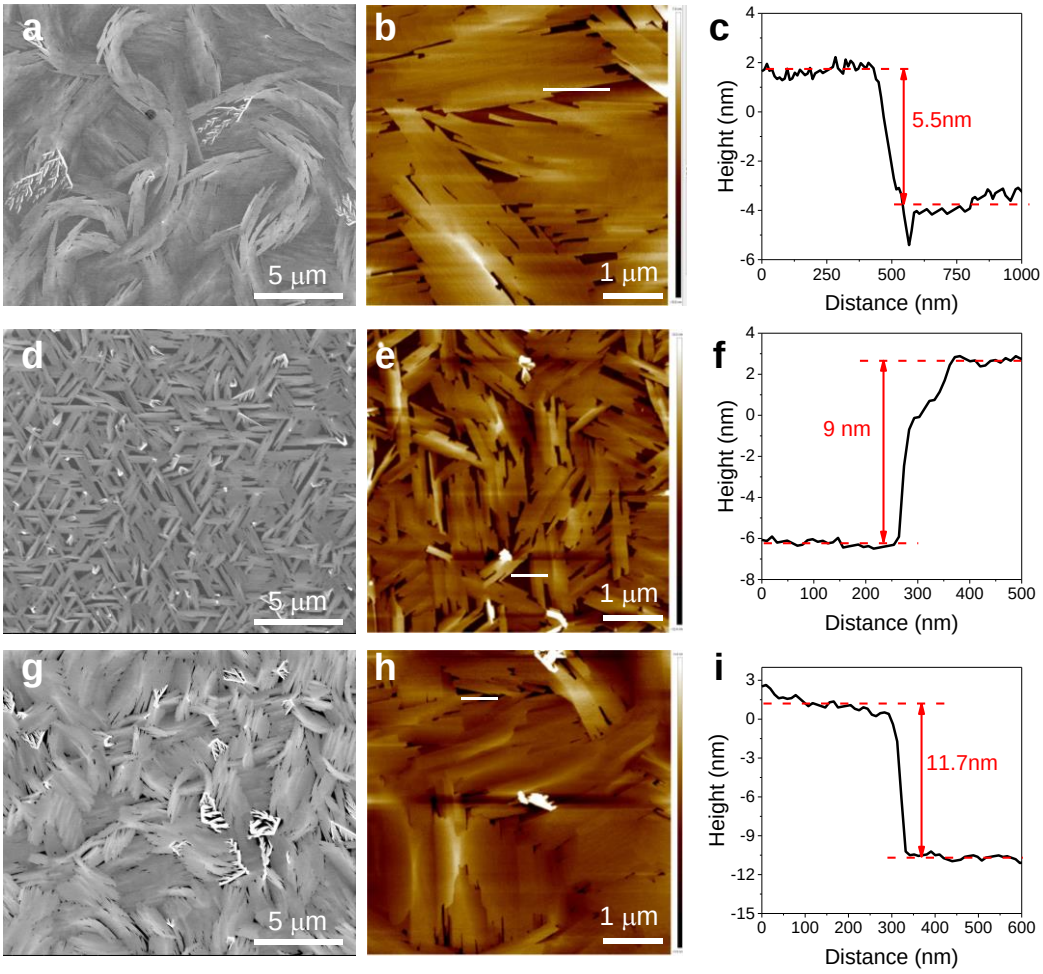


Figure 4.2.8 | Orientated growth of Te on the different TMDs with three-fold symmetric surface. a-c, SEM (**a**), AFM (**b**) images and the corresponding height profile (**c**) of Te grown on WS_2. **d-f,** SEM (**d**), AFM (**e**) images and the corresponding height profile (**f**) of Te grown on $MoSe_2$. **g-i,** SEM (**f**), AFM (**h**) images and the corresponding height profile (**i**) of Te grown on MoS_2.

We investigated the growth of Te on other TMDs with a similar three-fold symmetric surface structure (Fig. 4.2.8). By employing the same method (substrate pre-annealing at 300 ^{o}C and growth at 100 ^{o}C), orientated growth of ultrathin tellurium flakes with the thickness down to 5 nm, is achieved on these 2D surfaces, indicating the possibility to build different Te based heterostructures by van der Waals epitaxy. The size of the flakes on MoS_2 and $MoSe_2$ is relatively small compared to the ones on WS_2 and WSe_2, which can be further improved by optimizing the growth conditions.

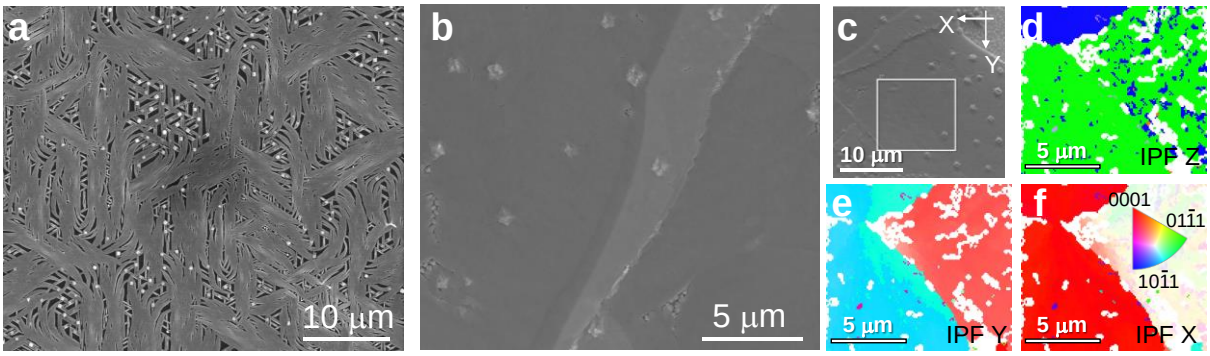


Figure 4.2.9 | Orientation growth of SeTe alloy on WSe_2 surface. a-b, SEM of the orientated grown $Se_{0.3}Te_{0.7}$ (**a**) and $Se_{0.5}Te_{0.5}$ (**b**) alloys on WSe_2. **c-f,** SEM image (**c**) and the corresponding EBSD IPF Z (**d**), Y (**e**), X (**f**) maps of $Se_{0.5}Te_{0.5}$ Te grown on WSe_2.

Selenium (Se) is also composed of 1D helical atomic chains, the same crystal structure as Te. It is able to be alloyed with Te to form the solid solutions for any concentration[24, 35]. These alloys have tunable bandgaps ranging from 0.3 eV to 1.9 eV and broad applications such as photodetectors or solar cells[24, 35]. The tunable band gap of SeTe alloys provides flexibility for band alignment with the 2D materials, allowing the growth of functional 1D/2D heterostructures. Hence, we explored the growth of SeTe alloys on 2D surface. WSe_2 and WS_2 flakes were used as the substrates and SeTe powders with different compositions were applied as the precursor (see Method). As shown in Fig. 4.2.9a, orientated grown $Se_{0.3}Te_{0.7}$ crystals are achieved on the WSe_2 surface by using a $Se_{0.22}Te_{0.78}$ powders as the precursor. When the Se content of the source increases to 40 % in the source, continuous $Se_{0.5}Te_{0.5}$ films are grown (Fig. 4.2.9b). Electron backscatter diffraction (EBSD) results show that the $Se_{0.5}Te_{0.5}$ film is polycrystalline and the misorientation between grains was ~60 ° (Fig. 4.2.9c-f), indicating the growth mode is still van der Waals epitaxy for the alloys.

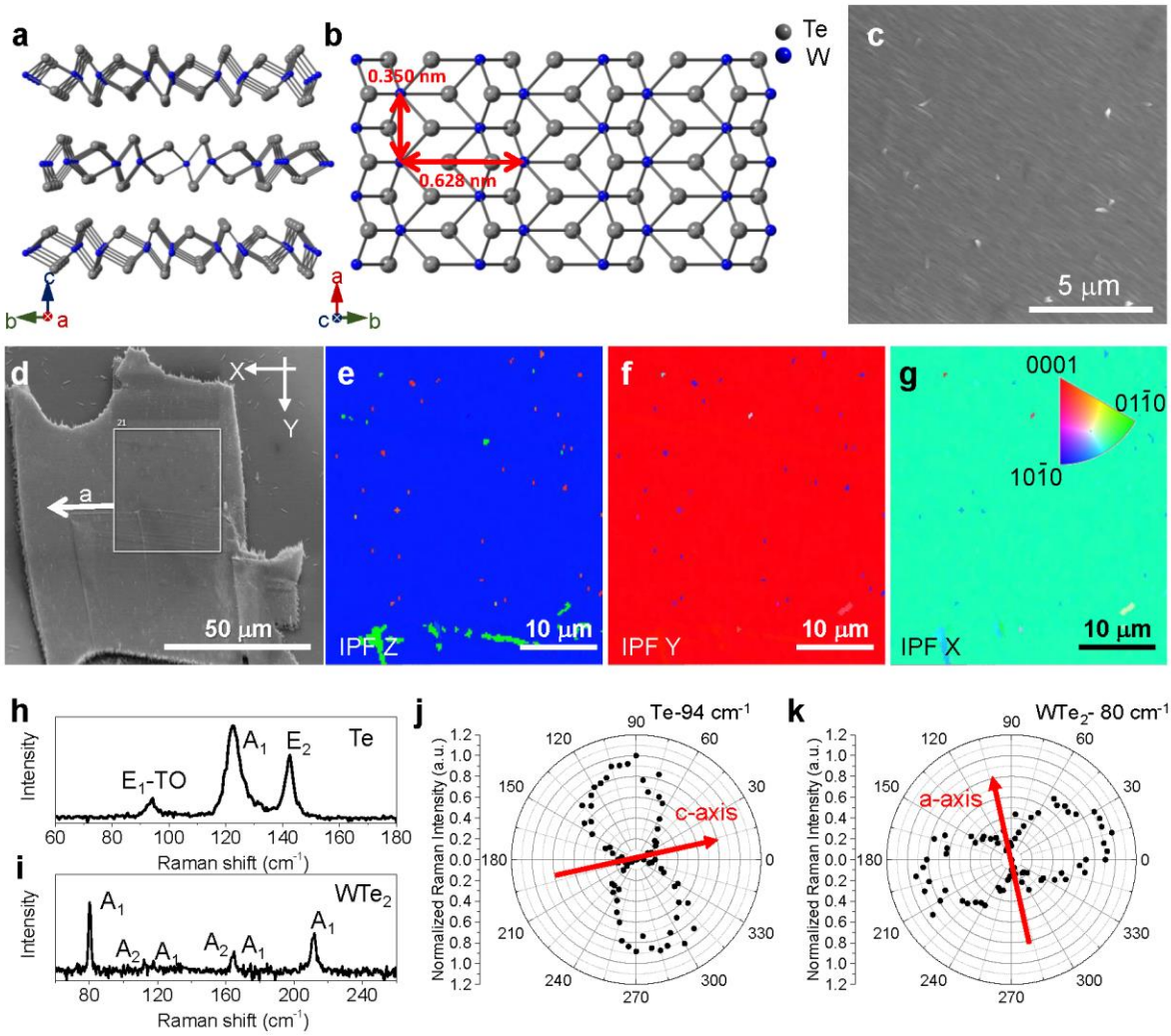


Figure 4.3.1 | Unidirectional growth of Te on WTe_2 surface. a-b, Crystal structure of WTe_2 along a-axis (**a**) and c-axis (**b**). **c,** SEM image of Te grown on WTe_2 surface, where the uniaxial features can be observed. **d-g**, SEM image (**d**) and the corresponding EBSD IPF Z (**e**), Y (**f**), X (**g**) maps of Te grown on WTe_2, indicating Te atomic chains are well aligned along any directions. **h-i**, Raman spectrum of the grown Te (**h**) and the uncovered WTe_2 part (**i**) in the same flakes. **j-k**, Angle-resolved polarized Raman intensities of the peaks at 94 cm^{-1} for Te (**j**) and 80 cm^{-1} for WTe_2 (**k**). The red arrows indicate the orientations of the c-axis of Te and a-axis of WTe_2.

4.3 Growth of single-crystal like Te on WTe_2

Although orientated growth of Te and SeTe crystals have been demonstrated on the above mentioned TMDs, it is hard to achieve single orientation thin films on them due to the three-fold symmetry of those TMD surfaces. However, unidirectional alignment of Te atomic chains is critical for the growth of films with properties that reflect the anisotropic nature of crystalline Te. Therefore, WTe_2 substrates, which have a relatively low-symmetry surface, were used to grow Te with a uniaxial, in-plane texture. WTe_2 has an AB stacked layered structure, where the adjacent layers are rotated 180 ^{o} with respect to each other (Fig. 4.3.1a). The surface crystal structure (ab-

plane) has only mirror symmetry and one-fold rotational symmetry (Fig. 4.3.1b) and the lattice parameters are a= 0.350 nm and b= 0.628 nm (Fig. 4.3.1b), where the mismatch between c-aixs of Te and b-axis of WTe_2 is relatively small, which is in favor of the unidirectional alignment of Te atoms. WTe_2 was exfoliated onto SiO_2/Si substrates. We can determine the crystal orientation of WTe_2 flakes from their configurations, as it has the tendency to fracture along the a-axis during exfoliation[36]. Te was grown on the annealed WTe_2 flakes at 130 ^oC (pre-annealing temperature was 300 ^oC). As shown in the Fig. 4.3.1c, we observed the growth of a continuous film with uniaxial features perpendicular to the a-axis of WTe_2 substrates. EBSD was performed on the Te/WTe_2 structure to determine its crystallinity and growth orientation. As shown in Fig. 4.3.1d-g, the inverse pole figure (IPF) maps show constant color in all directions, indicating single-crystal-like texture of the grown Te on the WTe_2 surface. C-axis of Te is aligned perpendicularly to the a-axis of WTe_2 (tungsten atomic chains), and (10-10) planes are paralleled to the surface based on the EBSD results. Te film with (01-10) planes parallel to the surface were observed in another flake. The different out-of-plane orientations of Te on different WTe_2 flakes is likely caused by the nature of the exposed surface of AB stacked WTe_2 substates. Further investigation is needed for the underlying growth mechanism. Angle-resolved polarized Raman was performed on the Te and uncovered WTe_2 surface on the same flakes as shown in Fig. 4.3.1h-k. The relative crystal orientation between Te and WTe_2 can be identified based on the angle-dependent intensities of the E_1-TO mode (~94 cm^{-1}) for Te[7] and A_1 mode (~80 cm^{-1}) for WTe_2[36] (Fig. 4.3.1j and k). The c-axis of Te is perpendicular to the a-axis of WTe_2 (Figure S8), further confirming the previous results. It is possible to achieve single crystalline Te films over large area by further post-annealing to eliminate the grain boundaries of the current films.

4.4 Conclusion

In summary, we realized orientated growth of ultrathin Te on 2D surfaces via van der Waals epitaxy. 2D Te flakes with thickness down to 5 nm were grown on the WSe_2, WS_2, $MoSe_2$, MoS_2 flakes, where the c-axis of Te is aligned with the armchair direction of the substrates. Moiré superlattice was achieved and observed on the Te/WSe_2 heterostructure. This method can be extended to the growth of SeTe alloys. Finally, we achieved the growth of single-crystal textured Te on WTe_2, where the c-axis of Te is aligned perpendicular to the tungsten chains of WTe_2. The orientated grown Te can exploit its anisotropic behaviors. In addition, this method enables the construction of Te based heterostructure, the 1D/2D moiré superlattice of which can be a novel platform for further investigation. In the future, it is possible to realize the growth of single crystalline Te films by post-annealing the Te/WTe_2 to eliminate the grain boundaries, since the Te atomic chains are well aligned in any directions. Exploring some other substrates with low-symmetric surface is another route to achieve single crystalline Te films.

4.5 Method

Materials growth. WSe_2, WS_2, $MoSe_2$, MoS_2, WTe_2 flakes were exfoliated onto SiO_2/Si chips as the growth substrates. The exfoliation of WTe_2 was operated in a N_2 glove box. Te pellets (99.999%, Sigma-Aldrich) or SeTe alloy crystals ($Se_{0.22}Te_{0.78}$ and $Se_{0.4}Te_{0.6}$ alloys) were grounded into powders as the precursor. Growth was done in a two-zone hot wall quartz tube furnace

(Daepoong Industry, 50602). An alumina boat containing precursor powders (20 mg) was loaded into the zone 1 of the furnace and substrates were placed in the downstream region (zone 2). Prior to the growth, the furnace was evacuated, and Ar flow was introduced at 50 sccm, at which the pressure of the system was about 1.5 Torr. Once the system is purged of air, substrates were pre-annealed at desired temperatures for 15 min. The annealing temperature was typically 300 ^{o}C. Non-annealed or 200 ^{o}C annealed substrates were used to investigated the effect of the pre-treatment in Fig. 3. The furnace was open to cool down the system after pre-annealing, Ar flow and pressure were kept constant in the whole process. After pre-treatment, the substate temperature was set to the growth temperatures (100 ^{o}C without specific notification, 130 ^{o}C for the growth of Te on WTe_2). When the substrate temperature stabilized at the target temperature, the precursor was heated to 450 ^{o}C. Ar (50 sccm) was applied as the carrier gas. The growth process last for 10-15 min. The furnace was open to cool down the system after growth.

Characterization. TEM characterization was performed on a Te/WS_2 sample. The flakes were transferred on a carbon coated transmission electron microscopy (TEM) grid by dry transfer method. TEM characterization was carried on a FEI Titan 60-300 microscope with an acceleration voltage 200 kV at the National Center for Electron Microscopy at Lawrence Berkeley National Laboratory. SEM and EBSD measurements were performed on a FEI Quanta field emission gun SEM and Oxford EBSD detector. In the analysis of the composition of SeTe alloy, we grew SeTe on WSe_2 and WS_2 flakes in the same batch, and estimated the element ratio of Se and Te by doing EDS on the alloy grown on WS_2 substrates. performed AFM (tapping mode) was carried on a Dimension ICON AFM (Bruker, Germany). Raman spectrums were measured on a LabRAM HR Evolution Raman microscope with a excitation line of 532 nm.

Density Functional Theory Based Total Energy Calculations

DFT computations were run using the Vienna Ab Initio Simulation Package[19] version 5.4.4. The projected-augmented-wave method was used to model the core electrons[19b], and the exchange-correlation energy was estimated using Perdew-Burke-Ernzehof[20]. All the simulations were run using a 600eV cutoff energy for the plane-wave (PW) basis set, a minimum spacing for the *k*-points of 0.25 Å^{-1}, and convergence criteria of 10^{-5} eV for the electronic self-consistent cycle (SCC). Also, a dipole correction was used in the direction perpendicular to the substrate to reduce spurious interaction with its periodic image.

To compute the binding energies of Te atoms to WSe_2 substrates with and without Se vacancies, a 5x5 substrate supercell was used with a 30, and the atomic positions and volume of the supercell were relaxed until the forces on all atoms were less than 10^{-3} eVÅ^{-1}. Lastly, the binding energies were computed using the usual equation, $E_b = E_{Te/WSe_2} - \left(E_{WSe_2} + E_{Te}\right)$, where E_{Te} is the energy of a single Te atom (obtained using a single *k*-point and the above mentioned parameters), and $E_{Te/WSe_2}, E_{WSe_2}$ are the energies of Te plus substrate and substrate systems, respectively.

The binding energy of a Te slab was computed using a supercell containing 1x4 and 1x3 substrate and Te unit cells, respectively, and strains of ε_{33}=-3.6% and $\varepsilon\varepsilon_{11}$=-2.0% were imposed on the Te slab. The bonding energy was obtained using the equation

$$E_b = \frac{E_{Te/WSe_2} - E_{WSe_2} - E_{Te}}{A} \quad (1)$$

where $E_{WSe_2}, E_{Te}, E_{Te/WSe_2}$ are the energies of the systems consisting of just the substrate, the Te slab, and the substrate plus the slab; and A is the area perpendicular to the substrate normal.

4.6 References

[1] R. S. Caldwell, H. Fan, *Physical Review* **1959**, 114, 664.
[2] J. R. Reitz, *Physical Review* **1957**, 105, 1233.
[3] R. W. Dutton, R. S. Muller, *Proceedings of the IEEE* **1971**, 59, 1511.
[4] A. Koma, S. Tanaka, *Physica Status Solidi (b)* **1970**, 40, 239.
[5] W. Wu, G. Qiu, Y. Wang, R. Wang, P. Ye, *Chemical Society Reviews* **2018**, 47, 7203.
[6] Z. Shi, R. Cao, K. Khan, A. K. Tareen, X. Liu, W. Liang, Y. Zhang, C. Ma, Z. Guo, X. Luo, *Nano-Micro Letters* **2020**, 12, 1.
[7] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. A. Goddard, M. J. Kim, X. Xu, *Nature Electronics* **2018**, 1, 228.
[8] M. Amani, C. Tan, G. Zhang, C. Zhao, J. Bullock, X. Song, H. Kim, V. R. Shrestha, Y. Gao, K. B. Crozier, *ACS Nano* **2018**, 12, 7253.
[9] C. Zhao, C. Tan, D.-H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, *Nature Nanotechnology* **2020**, 15, 53.
[10] S. Sen, K. Muthe, N. Joshi, S. Gadkari, S. Gupta, M. Roy, S. Deshpande, J. Yakhmi, *Sensors and Actuators B: Chemical* **2004**, 98, 154.
[11] L. Wu, W. Huang, Y. Wang, J. Zhao, D. Ma, Y. Xiang, J. Li, J. S. Ponraj, S. C. Dhanabalan, H. Zhang, *Advanced Functional Materials* **2019**, 29, 1806346.
[12] T. I. Lee, S. Lee, E. Lee, S. Sohn, Y. Lee, S. Lee, G. Moon, D. Kim, Y. S. Kim, J. M. Myoung, *Advanced Materials* **2013**, 25, 2920.
[13] S. Huang, M. Segovia, X. Yang, Y. R. Koh, Y. Wang, D. Y. Peide, W. Wu, A. Shakouri, X. Ruan, X. Xu, *2D Materials* **2019**, 7, 015008.
[14] S. Ran, T. S. Glen, B. Li, T. Zheng, I.-S. Choi, S. T. Boles, *The Journal of Physical Chemistry* C **2019**, 123, 22578.
[15] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science* **2004**, 306, 666.
[16] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nature Nanotechnology* **2011**, 6, 147.
[17] H. O. Churchill, G. J. Salamo, S.-Q. Yu, T. Hironaka, X. Hu, J. Stacy, I. Shih, *Nanoscale Research Letters* **2017**, 12, 1.
[18] S. Yi, Z. Zhu, X. Cai, Y. Jia, J.-H. Cho, *Inorganic Chemistry* **2018**, 57, 5083.
[19] V. Nicolosi, M. Chhowalla, M. G. Kanatzidis, M. S. Strano, J. N. Coleman, *Science* **2013**, 340.
[20] E. Bianco, R. Rao, M. Snure, T. Back, N. R. Glavin, M. E. McConney, P. Ajayan, E. Ringe, *Nanoscale* **2020**, 12, 12613.
[21] G. Zhou, R. Addou, Q. Wang, S. Honari, C. R. Cormier, L. Cheng, R. Yue, C. M. Smyth, A. Laturia, J. Kim, *Advanced Materials* **2018**, 30, 1803109.

[22] A. Apte, E. Bianco, A. Krishnamoorthy, S. Yazdi, R. Rao, N. Glavin, H. Kumazoe, V. Varshney, A. Roy, F. Shimojo, *2D Materials* **2018**, 6, 015013.
[23] X. Zhang, J. Jiang, A. A. Suleiman, B. Jin, X. Hu, X. Zhou, T. Zhai, *Advanced Functional Materials* **2019**, 29, 1906585.
[24] C. Tan, M. Amani, C. Zhao, M. Hettick, X. Song, D. H. Lien, H. Li, M. Yeh, V. R. Shrestha, K. B. Crozier, *Advanced Materials* **2020**, 32, 2001329.
[25] F. Katzenberg, I. Lieberwirth, J. Petermann, *Journal of Materials Science* **1998**, 33, 4787.
[26] Q. Wang, M. Safdar, K. Xu, M. Mirza, Z. Wang, J. He, *ACS nano* **2014**, 8, 7497.
[27] M. Capers, M. White, *Thin Solid Films* **1971**, 8, 317.
[28] S. Yang, B. Chen, Y. Qin, Y. Zhou, L. Liu, M. Durso, H. Zhuang, Y. Shen, S. Tongay, *Physical Review Materials* **2018**, 2, 104002.
[29] Y. Cao, V. Fatemi, A. Demir, S. Fang, S. L. Tomarken, J. Y. Luo, J. D. Sanchez-Yamagishi, K. Watanabe, T. Taniguchi, E. Kaxiras, *Nature* **2018**, 556, 80.
[30] C. Zhang, C.-P. Chuu, X. Ren, M.-Y. Li, L.-J. Li, C. Jin, M.-Y. Chou, C.-K. Shih, *Science Advances* **2017**, 3, e1601459.
[31] G. Bales, A. Zangwill, *Physical Review B* **1990**, 41, 5500.
[32] M. Donarelli, F. Bisti, F. Perrozzi, L. Ottaviano, *Chemical Physics Letters* **2013**, 588, 198.
[33] S. Tongay, J. Suh, C. Ataca, W. Fan, A. Luce, J. S. Kang, J. Liu, C. Ko, R. Raghunathanan, J. Zhou, *Scientific Reports* **2013**, 3, 1.
[34] G. Bales, D. Chrzan, *Physical Review B* **1994**, 50, 6057.
[35] I. Hadar, X. Hu, Z.-Z. Luo, V. P. Dravid, M. G. Kanatzidis, *ACS Energy Letters* **2019**, 4, 2137.
[36] Q. Song, X. Pan, H. Wang, K. Zhang, Q. Tan, P. Li, Y. Wan, Y. Wang, X. Xu, M. Lin, *Scientific Reports* **2016**, 6, 1.

CHAPTER 5

Thermal stability for Te-based devices

5.1 Introduction

Tellurium can provide high hole mobility with low processing temperature, and wafer-scale production; therefore, it has been demonstrated as a promising candidate for flexible/transparent electronics and three-dimensional integration circuits[1]. Although various properties and applications of Te have been reported[1-7], detailed study of the thermal stability of the Te based devices, which is a major concern for the practical use, is still lacking. Te-based transistors suffer from device degradation after exposure to high temperatures because (1) the high vapor pressure of Te induces sublimation of the channel[8, 9], and (2) interdiffusion/reactivity between the Te and the electrodes causes contact degradation. This can critically limit its practical utility. Thus, a method to mitigate such effect on Te-based devices is necessary.

In this study, we investigated the effect of temperature on the evaporated Te-based devices and demonstrated a graphene-contacted and SiO_x-encapsulated Te transistor with improved thermal stability. Our device suppresses the sublimation of the Te channel by applying an encapsulation layer such that the Te film remains intact for hours at temperatures up to 250 ^oC in N_2 environment. The integration of graphene as a contact with Te also eliminates the interdiffusion/reactivity between Te and the electrodes even after repeated annealing at 250 ^oC in N_2. Our Te transistor showed a device performance with a hole mobility of ~ 50 $cm^2\ V^{-1}\ s^{-1}$ after contact annealing, which was similar to a Ni-contacted Te device with the same channel thickness. While typical metal-contacted Te devices show performance degradation with increasing temperatures and failure at temperatures > 200 ^oC, our device can maintain its electrical performance under repeated annealing processes at temperatures up to 250 ^oC.

5.2 Two failure mechanisms of Te-based devices

The vapor pressure of Te is ~10^{-7} Torr at 200 ^oC and reaches ~10^{-5} Torr at 250 ^oC[8]. The high vapor pressure results in sublimation of the Te film when it is exposed to a high-temperature environment, significantly deteriorating the electrical properties of Te. Encapsulation is an effective method to stabilize the chemically or thermally sensitive materials such as organic semiconductors and black phosphorus[10-12]. Therefore, we firstly investigated the effect of the encapsulation layer on the thermal stability of Te films. Patterned crystalline Te films with a thickness of 6 nm were prepared on the cold SiO_2/Si substrates (-80 ^oC) by thermal evaporation as reported previously[1] (Fig. 5.2.1a and b), the average grain size of which was ~25 μm^2. 30 nm SiO_x was subsequently deposited on the substrates by e-beam evaporation to fully encapsulate the Te films on the bottom (Fig. 5.2.1c and d). The Te films with and without the SiO_x encapsulation layer were annealed at 250 ^oC in N_2 atmosphere for 1 hour to assess their thermal stability. For the uncapped sample, the Te films fully sublimed after the annealing process as shown in Fig. 5.2.1b). In contrast, the encapsulated films did not show surface morphology changes, including the

sublimation or the movement of grain boundaries after annealing at 250 °C(Fig. 5.2.1d). When the annealing temperature was further increased to 300 °C, re-evaporation of Te was observed on the encapsulated sample (Figure 5.2.2). The voids observed on the encapsulated Te films are likely caused by the pinholes or cracks in the evaporated SiO_x capping layer, which are formed or enlarged during the high-temperature annealing process.

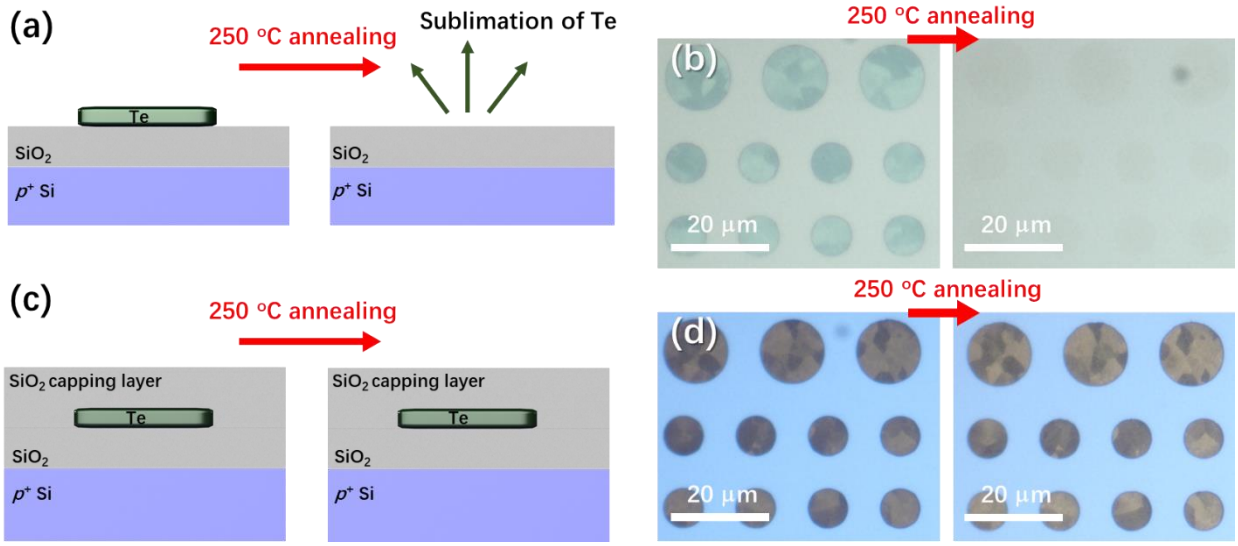


Figure 5.2.1 | (a)-(b) Schematic diagram (a) and optical microscopy images (b) of the Te films before (left) and after (right) annealing in N_2 atmosphere. (c)-(d) Schematic diagram (c) and optical microscopy images (d) of the SiO_x encapsulated Te films before (left) and after (right) annealing in N_2 atmosphere. The thickness for Te films is ~ 6 nm and the thickness for the SiO_x capping layer is ~ 30 nm. Each annealing process mentioned above lasts for 1 h.

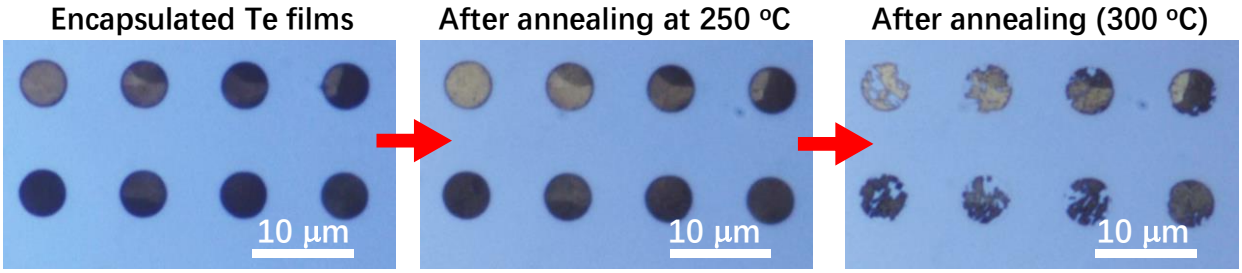


Figure 5.2.2 | Surface morphology change for the SiO_x encapsulated Te films after annealing at different temperatures. The thickness for Te films is ~ 6 nm and the thickness for the SiO_x capping layer is ~ 30 nm. Each annealing process mentioned above lasts for 1 h.

Next, field-effect transistors (FETs) were fabricated to further examine the thermal stability of Te at the device level. Te FETs with different metal contacts (Pd, Ni and Au) were fabricated on the SiO_2 (50 nm)/ p^+ Si substrates, which serve as a dielectric layer and a global back gate respectively (Figure 5.2.3a). These devices were annealed at 250 °C in N_2 atmosphere for 30 min. For the Pd-contacted FET, significant change in the channel region was observed after annealing due to the diffusion of Pd atoms into the Te channel (Figure 5.2.4a and b). The diffused Pd

metallized the Te channel, which was confirmed by the I_d-V_g transfer curves for the Pd-contacted FET (Figure 5.2.5). A similar behavior between Au and Te was also observed after annealing (Figure 5.2.4c and d). These interactions between the metal contact and the Te channel lead to the device deterioration. Among the investigated metal contacts, Ni contact was considered most stable (Figure 5.2.4e and f). Therefore, we further fabricated Ni-contacted and SiO_x-encapsulated Te device (Figure 5.2.3a and b) to evaluate its thermal stability. The device was annealed in the N_2 atmosphere repeatedly with annealing temperature increasing from 100 ^oC to 250 ^oC (Figure 5.2.3b-f). Each annealing process lasted an hour, and the electrical measurements were performed on the device immediately after each annealing process. Figure 5.2.3g shows the I_d-V_g transfer curves for the device before and after annealing. The effective mobility, which was extracted from the I_d-V_g transfer curves, decreases slightly from 57 $cm^2\,V^{-1}\,s^{-1}$ to 38 $cm^2\,V^{-1}\,s^{-1}$ as the annealing temperature increases to 150 ^oC. When the annealing temperature was further raised to 200 ^oC, the device performance drops dramatically with ~3 orders of magnitude lower effective mobility (~0.05 $cm^2\,V^{-1}\,s^{-1}$) and subthreshold swing increases from 2.3 V dec^{-1} (as-fabricated) to 8.6 V dec^{-1}. The device becomes an open circuit after annealing at 250 ^oC. We also measured the device performance of encapsulated Ni-contacted Te devices, which contain random lattice orientation along the channel, after annealing at different temperatures (Figure 5.2.6). The effective mobility decreases from 26.1 ± 8.6 cm^2/Vs to 11.8 ± 1.8 cm^2/Vs as the annealing temperature increases to 150 ^oC. When the annealing temperature reached 200 ^oC, half of the devices became open circuits, and the rest showed a low effective mobility of ~ 0.1 $cm^2\,V^{-1}\,s^{-1}$. The degradation in performance above 150 ^oC is mainly related to the loss of Te around the contact regions. At these locations, re-evaporation/diffusion of Te is easy because the shadowing effect causes poor step coverage and the Te and the contact metal can possibly react with each other[13, 14]. This explanation is supported by the observable disconnection around the contact regions after annealing at 250 ^oC (Figure 5.2.3f).

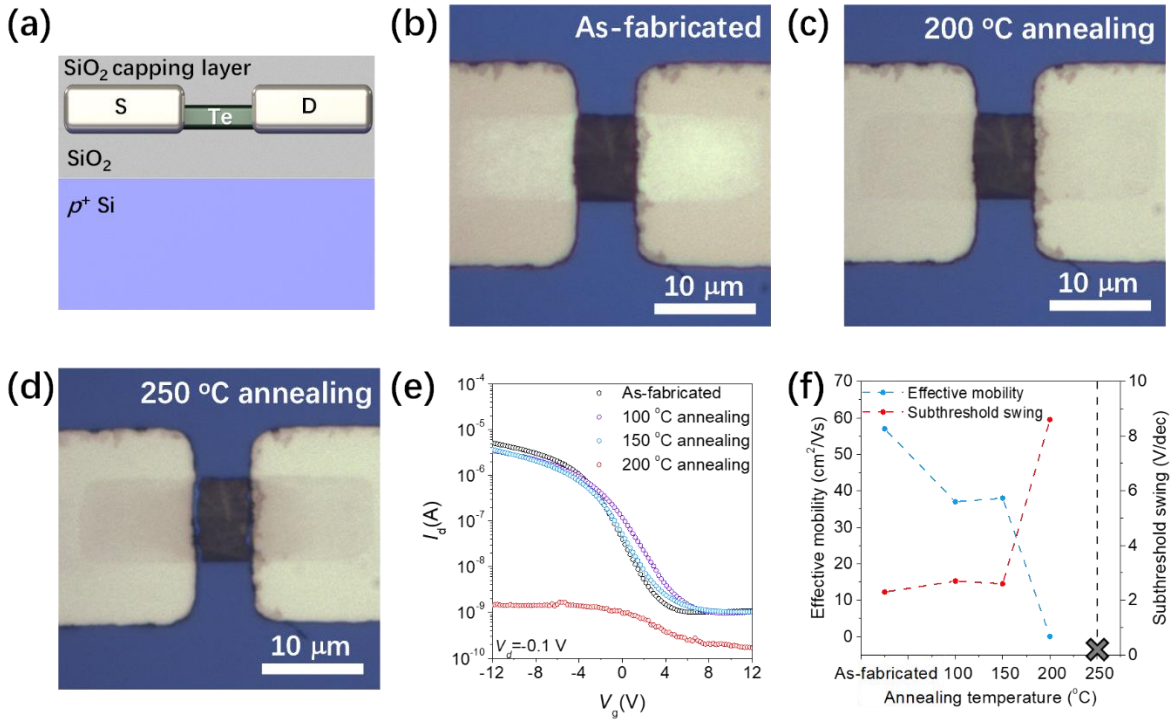


Figure 5.2.3 | (a) Schematic diagram of the device structure for a metal-contacted Te device encapsulated with evaporated SiO_x layer. (b)-(d) A Ni-contacted SiO_x-encapsulated Te device before (b) and after (c)-(d) annealing in N_2 atmosphere at different temperatures. (e) I_d-V_g transfer curves change for the Ni-contacted SiO_x-encapsulated Te device before and after annealing processes. (f) Effective mobility change extracted from (e). Effective mobility is calculated using: $\mu_{eff} = \frac{dI_d}{dV_d}\frac{L}{WC_{ox}(V_g - V_t)}$, where C_{ox} is the gate oxide capacitance, L is the channel length, W is the device width, and V_t is the threshold voltage. The thickness for the Te channel is ~7 nm and the thickness for the SiO_x-capping layer is ~ 30 nm. Each annealing process mentioned above lasts for 1 h.

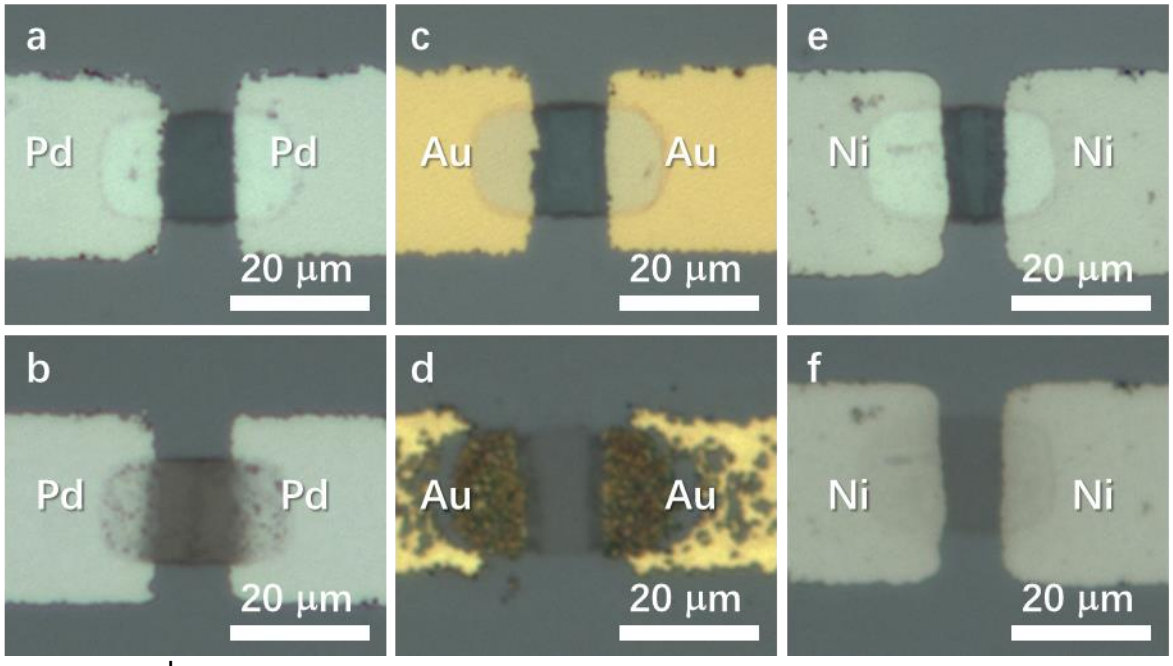


Figure 5.2.4 | **a-b**, Pd-contacted Te before (**a**) and after (**b**) a 250 °C annealing in N_2 atmosphere. **c-d**, Ni-contacted Te before (**c**) and after (**d**) a 250 °C annealing in N_2 atmosphere. **e-f**, Au-contacted Te before (**e**) and after (**f**) a 250 °C annealing in N_2 atmosphere. Each annealing last for 30 min.

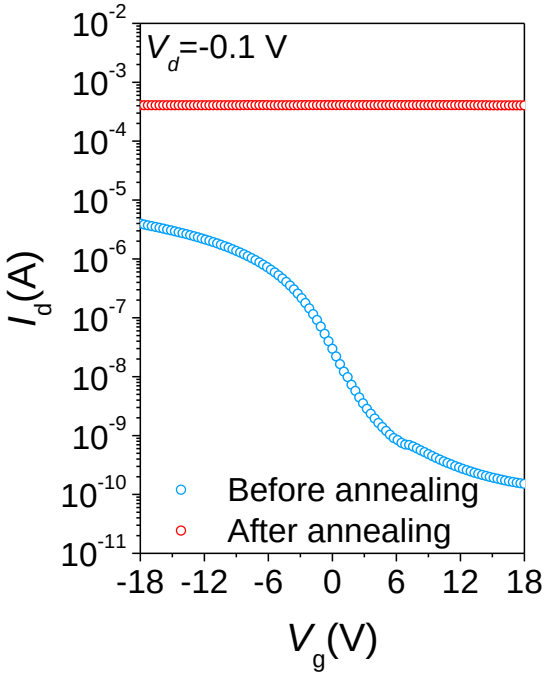


Figure 5.2.5 | I_d-V_g transfer curves for the Pd-contacted Te transistor before and after the 250 °C annealing in N_2 atmosphere.

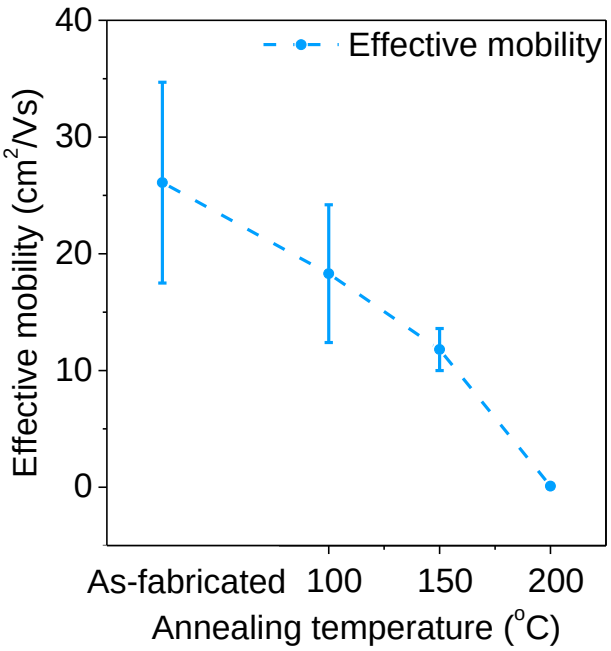


Figure 5.2.6 | Effective mobility change of encapsulated Ni-contacted devices with random lattice orientation along the channel after annealing in N_2 atmosphere (the results are collected from 8 individual devices). Each annealing process lasts for 1 h.

5.3 Graphene-contacted, SiOx-encapsulated Te transistors with improved thermal stability

To address these challenges, we applied a thin and chemically inert contact material to replace the thick and active metal such that the thermal stability of Te devices can be enhanced. Graphene is considered to be a promising candidate owing to the following reasons. First, the electrical conductivity of graphene is sufficiently high [15, 16]. Second, graphene is chemically inert due to large delocalized π electrons, circumventing the interdiffusion/reaction at the interface of the contact at high temperatures [17, 18]. In addition, the atomically thin graphene electrodes eliminate the shadowing effect during the capping layer deposition [12], hence fully encapsulating the Te device to prevent the sublimation.

Graphene-contact and SiO_x-encapsulated Te FETs were fabricated as shown in Figure 5.3.1a and b. Chemical vapor deposition (CVD) grown bilayer graphene film was transferred onto the SiO_2 (50 nm)/ p^+ Si substrate through a wet transfer method[19], followed by lithography and O_2 plasma etching processes to define the electrodes. Te film was deposited as a channel connecting the source and drain graphene electrodes. Metal Ni probe pad was deposited far away from the source/drain contact regions. Fabrication was completed with capping the whole device with 30 nm evaporated SiO_x layer and opening windows on top of Ni pads for probing. The as-fabricated graphene-contacted and SiO_x-encapsulated Te device shows a poor electrical performance (Figure 5.3.1c) with the effective mobility of 3.5 $cm^2\ V^{-1}\ s^{-1}$, which is much lower than the effective mobility of the Ni-contacted devices (57 $cm^2\ V^{-1}\ s^{-1}$). Post-annealing has significant effect on the

electrical performance of the graphene-contacted Te device (Figure 5.3.1c-e) because the high temperature treatment facilitates removal of residues at the interface and adhesion between Te and graphene[20, 21], yielding an improved contact. The highest contact annealing temperature was 250 °C since the Te device may deteriorate due to the degradation of the encapsulation layer at higher temperatures (>250 °C). As shown in Figure 5.3.1e, the effective mobility is enhanced from 3.5 $cm^2 V^{-1} s^{-1}$ to 15.1 $cm^2 V^{-1} s^{-1}$ after the contact annealing at 200 °C in N_2. The mobility further increases to 50.4 $cm^2 V^{-1} s^{-1}$ when the annealing temperature is raised to 250 °C. The ON-current level is enhanced by over an order of magnitude after the 250 °C annealing process as shown in the I_d-V_g transfer curves (Figure 5.3.1c). The electrical performance of the annealed graphene-contacted and SiO_x encapsulated Te device is comparable to that of Ni-contacted device without annealing. It needs to be noted that the annealing temperature (250 °C) for the graphene-contacted devices is even higher than the failure temperature for metal-contacted ones, demonstrating the advantages of the ultrathin and chemically inert electrodes. We believe the thermal stability of Te based devices could be further improved by a more suitable encapsulation layer or a more optimized deposition technique such as low temperature atomic layered deposition or sputtering.

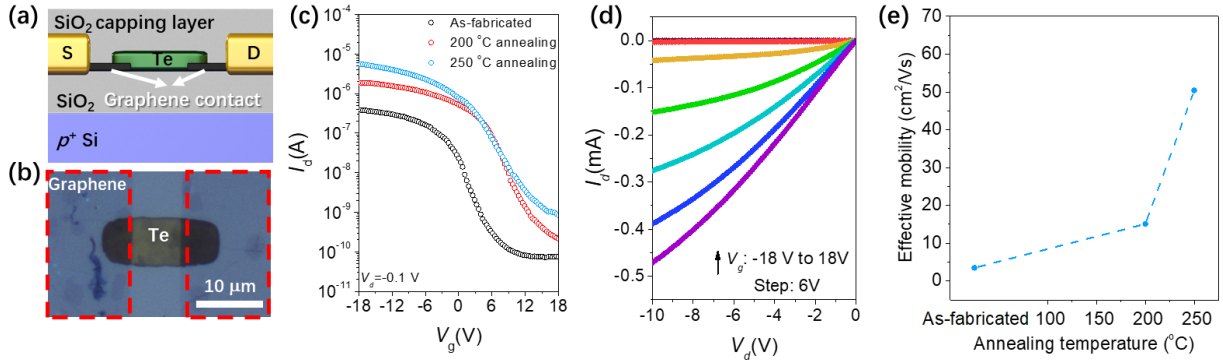


Figure 5.3.1 | (a) Schematic diagram of the device structure for a graphene contacted Te device encapsulated with evaporated SiO_x layer. (b) Optical image of a typical graphene-contacted encapsulated Te device. (c) I_d-V_g transfer curves of a graphene-contacted SiO_x-encapsulated Te device before and after contact annealing at different temperatures in N_2 atmosphere. (d) I_d-V_d output characteristics of the graphene-contacted SiO_x-encapsulated Te device after a contact annealing at 250 °C in N_2 atmosphere. (e) Effective mobility change extracted from (b). The thickness for the Te channel is ~7 nm and the thickness for the SiO_x capping layer is ~ 30 nm. Each annealing process mentioned above lasts for 1 h.

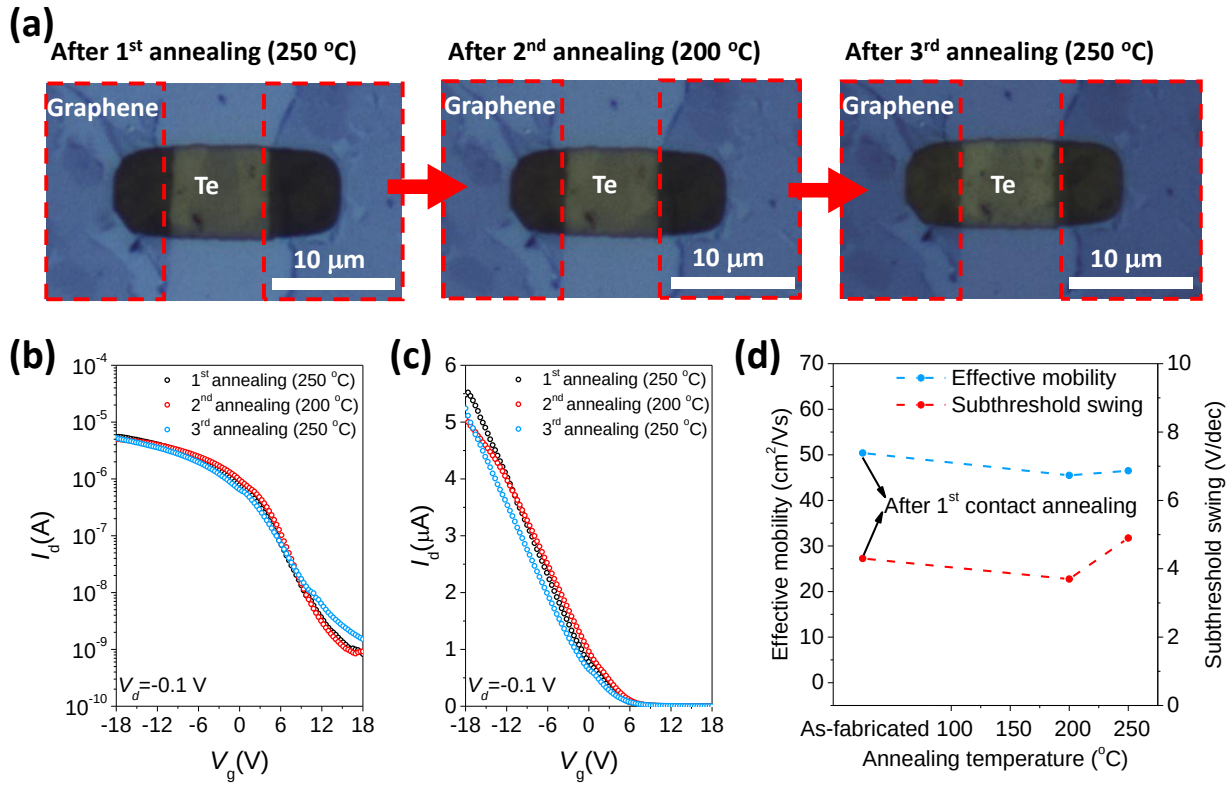


Figure 5.3.2 | (a) Optical microscopy images of a graphene-contacted SiO_x-encapsulated Te device after repeated annealing processes. (b)-(c) Semi-log (b) and liner (c) I_d-V_g transfer curves of a graphene-contacted SiO_x-encapsulated Te device after repeated high temperature annealing processes in N_2 atmosphere. (d) Effective mobility and subthreshold swing change (extracted from (b)) after repeated high temperature annealing processes in N_2 atmosphere. The thickness for the Te channel is ~7 nm and the thickness for the SiO_x capping layer is ~ 30 nm. Each annealing process mentioned above lasts for 1 h.

We further investigated the thermal stability of the graphene-contacted and SiO_x encapsulated Te device by tracking its changes in electrical performance after repeated high-temperature annealing processes. The as-fabricated graphene-contacted Te device was first annealed at 250 °C for an hour and was cooled down to room temperature, followed by the electrical measurements. The same annealing procedures and the measurement were performed on the same sample two more times at annealing temperatures 200 °C and 250 °C. Each annealing process mentioned above lasts for 1 h. As shown in Figure 5.3.2a, no prominent morphology changes were observed on the device after the repeated high-temperature annealing processes. The semi-log and liner I_d-V_g transfer curves measured after each annealing process are exhibited in Figure 5.3.2b and c. No significant device performance degradation was observed. As apparent from these figures, the device shows a similar I_d-V_g curve after each annealing process. The OFF-current slightly increases from 0.83 nA to 1.5 nA, which is probably due to the quenched-in defects[22], as Te devices were rapidly cooled from annealing temperatures to room temperature. Subthreshold swing increase from 4.3 V dec^{-1} to 4.9 V dec^{-1} and a small fluctuation in threshold voltage is observed after

annealing. The effective mobility of the graphene-contacted and SiO_x-encapsulated Te device remains approximately constant at ~47 $cm^2 V^{-1} s^{-1}$ after repeated thermal treatments with highest annealing temperature of 250 ^oC (Figure 5.3.2d). The changes in subthreshold swing and threshold voltage are likely caused by the charges trapped inside the oxide layer or at the interface[23, 24], which could also induce an OFF-current increase. The changes of defects or trapped charges in the Te devices must be small, otherwise, an obvious mobility drop would take place due to the scattering. Figure 5.3.3 showed the effective mobility of 10 individual devices with random lattice orientation along the channel on the same chip after the repeated annealing procedures. The devices exhibited an average effective mobility of 48.1 ± 9.7 cm^2/Vs. The sustained excellent electrical performance and the long-term thermal stability demonstrate the potential of the graphene-contacted and SiO_x-encapsulated Te device.

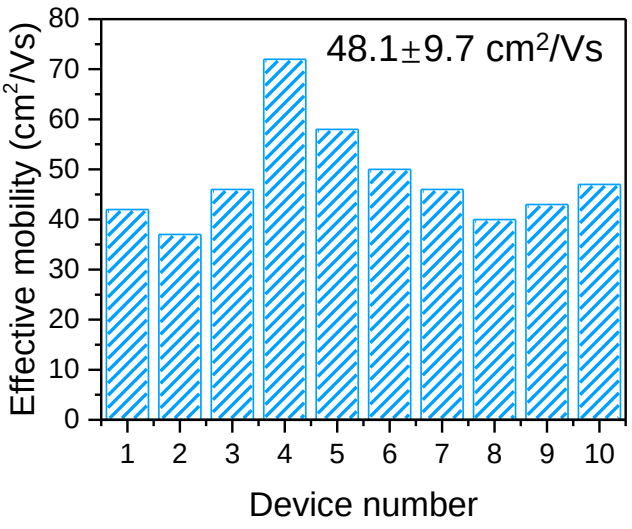


Figure 5.3.3 | Effective mobility of encapsulated graphene-contacted devices with random lattice orientations along the channel after repeated high temperature annealing processes in N_2 atmosphere. The average effective mobility is 48.2±9.7 cm^2/Vs.

5.4 Conclusion

In conclusion, this work explores the thermal stability of Te films and devices. To address the thermal instability of Te, we fabricated a graphene-contacted and SiO_x-encapsulated device. The chemically-inert graphene provides a thermally stable interface with Te, and the ultrathin nature of graphene allows a fully sealed encapsulation layer on the Te channel. Such a device structure increases the temperature tolerance of the Te-based devices to up to 250 ^oC. Further enhancement in thermal stability may be possible by improving the encapsulation layer through providing a conformal coating, suppressing pinholes or cracks formation, and matching the thermal expansion coefficients between the encapsulation layer and the Te film. Exploration of a proper electrode, which is inert to tellurium at high temperature and compatible to the conventional fabrication process, is needed.

5.5 References

[1] C. Zhao, C. Tan, D.-H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, *Nature Nanotechnology* **2020**, 15, 53.

[2] Y. Wang, G. Qiu, R. Wang, S. Huang, Q. Wang, Y. Liu, Y. Du, W. A. Goddard, M. J. Kim, X. Xu, *Nature Electronics* **2018**, 1, 228.

[3] S. Lin, W. Li, Z. Chen, J. Shen, B. Ge, Y. Pei, *Nature Communications* **2016**, 7, 1.

[4] M. Amani, C. Tan, G. Zhang, C. Zhao, J. Bullock, X. Song, H. Kim, V. R. Shrestha, Y. Gao, K. B. Crozier, *ACS Nano* **2018**, 12, 7253.

[5] W. Wu, G. Qiu, Y. Wang, R. Wang, P. Ye, *Chemical Society Reviews* **2018**, 47, 7203.

[6] Y. Du, G. Qiu, Y. Wang, M. Si, X. Xu, W. Wu, P. D. Ye, *Nano Letters* **2017**, 17, 3965.

[7] Y. Liu, W. Wu, W. A. Goddard III, *Journal of the American Chemical Society* **2018**, 140, 550.

[8] R. Honig, D. Kramer, *RCA Laboratories* **1968**.

[9] R. Dutton, R. Muller, *Thin Solid Films* **1972**, 11, 229.

[10] K. Kuribara, H. Wang, N. Uchiyama, K. Fukuda, T. Yokota, U. Zschieschang, C. Jaye, D. Fischer, H. Klauk, T. Yamamoto, *Nature Communications* **2012**, 3, 1.

[11] G.-H. Lee, X. Cui, Y. D. Kim, G. Arefe, X. Zhang, C.-H. Lee, F. Ye, K. Watanabe, T. Taniguchi, P. Kim, *ACS Nano* **2015**, 9, 7019.

[12] A. Avsar, I. J. Vera-Marun, J. Y. Tan, K. Watanabe, T. Taniguchi, A. H. Castro Neto, B. Ozyilmaz, *ACS Nano* **2015**, 9, 4138.

[13] T. Karabacak, T.-M. Lu, *Journal of Applied Physics* **2005**, 97, 124504.

[14] S. Arscott, Journal of Vacuum Science & Technology B, *Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **2019**, 37, 011602.

[15] C. a. Di, D. Wei, G. Yu, Y. Liu, Y. Guo, D. Zhu, *Advanced Materials* **2008**, 20, 3289.

[16] M. J. Allen, V. C. Tung, R. B. Kaner, *Chemical Reviews* **2010**, 110, 132.

[17] L. Liao, H. Peng, Z. Liu, *Journal of the American Chemical Society* **2014**, 136, 12194.

[18] J. Eun Lee, B. K. Sharma, S.-K. Lee, H. Jeon, B. Hee Hong, H.-J. Lee, J.-H. Ahn, *Applied Physics Letters* **2013**, 102, 113112.

[19] J. W. Suk, A. Kitt, C. W. Magnuson, Y. Hao, S. Ahmed, J. An, A. K. Swan, B. B. Goldberg, R. S. Ruoff, *ACS Nano* **2011**, 5, 6916.

[20] J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos, C. W. Magnuson, R. S. Ruoff, L. Colombo, R. M. Wallace, E. M. Vogel, *ACS Nano* **2012**, 6, 3224.

[21] A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. Magnuson, S. McDonnell, L. Colombo, E. Vogel, R. Ruoff, R. Wallace, *Applied Physics Letters* **2011**, 99, 122108.

[22] F. Bassani, *Encyclopedia of condensed matter physics*, Elsevier acad. press, 2005.

[23] D. Fleetwood, *Applied Physics Letters* **1992**, 60, 2883.

[24] Y. Y. Illarionov, G. Rzepa, M. Waltl, T. Knobloch, A. Grill, M. M. Furchi, T. Mueller, T. Grasser, *2D Materials* **2016**, 3, 035004.