Low-Power, Scalable Platforms for Implantable Neural Interfaces

By
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ABSTRACT

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Clinically viable and minimally invasive neural interfaces stand to revolutionize disease care for patients with neurological conditions. For example, recent research in Brain-Machine Interfaces has shown success in using electronic signals from the motor cortex of the brain to control artificial limbs, providing hope for patients with spinal cord injuries. Currently, neural interfaces are large, wired and require open-skull operation. Future, less invasive interfaces with increased numbers of electrodes, signal processing and wireless capability will enable prosthetics, disease control and completely new user-computer interfaces.

The first part of this thesis presents a signal-acquisition front end for neural recording that uses a digitally intensive architecture to reduce system area and enable operation from a 0.5V supply. The entire front-end occupies only 0.013mm^2 while including "per-pixel" digitization, and enables simultaneous recording of LFP and action potentials for the first time. The second part presents the development of a minimally invasive yet scalable wireless platform for electrocorticography (ECoG), an electrophysiological technique where electrical potentials are recorded from the surface of the cerebral cortex, greatly reducing cortical scarring and improving implant longevity. A high-density flexible MEMS electrode array is tightly integrated with active circuits and a power-receiving antenna to realize a fully implantable system in a very small footprint. Building on the previously developed digitally intensive architecture, an order of magnitude in circuit area reduction is realized with 3x improvement in power efficiency over state-of-the-art enabling a scalable platform for 64-channel recording and beyond.

Dedicated to my father, Joseph Muller

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LIST OF ACRONYMS

AC	Alternating Current
ACF	Anisotropic Conductive Film
ADC	Analog to Digital Converter
AP	Action Potential
ASIC	Application Specific Integrated Circuit
BER	Bit-error Rate
BJT	Bipolar Junction Transistor
BMI	Brain-Machine Interface
BPF	Band-Pass Filter
BRAIN	Brain Research through Advancing Innovative Neurotechnologies
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
COB	Chip-on-Board
DAC	Digital to Analog Converter
DC	Direct Current
DBS	Deep-Brain Stimulator
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
ΔΣ	Delta-Sigma
ECoG	Electrocorticography
EEG	Electroencephalography
EPSP	Excitatory Post-Synaptic Potential
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
FPGA	Field Programmable Gate Array
FSK	Frequency Shift Keying
IC	Integrated Circuit
ICMS	Intracortical Microstimulation
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Nonlinearity
INV	Logical Inversion
LDO	Low Dropout Regulator

LFP	Local Field Potential
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MA	Moving Average
MEMS	Micro-Electromechanical Systems
MICS	Medical Implant Communication Service
MIM	Metal-Insulator-Metal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NAND	Logical Negated And
NEF	Noise Efficiency Factor
NMOS	N-type Metal-Oxide-Semiconductor
NTF	Noise Transfer Function
OSR	Oversample Ratio
OTA	Operational Transconductance Amplifier
PBS	Phosphate Buffered Saline
PCB	Printed Circuit Board
PEF	Power Efficiency Factor
PMOS	P-type Metal-Oxide-Semiconductor
PMU	Power Management Unit
PSRR	Power-Supply Rejection Ratio
RF	Radio Frequency
RFID	Radio Frequency Identification
Rx	Wireless Receiver
SAR	Specific Absorption Rate
SAR ADC	Successive Approximation Register ADC
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SPI	Serial-to-Parallel Interface
THD	Total Harmonic Distortion
Tx	Wireless Transmitter
UWB	Ultra-Wideband
VCO	Voltage Controlled Oscillator
XOR	Logical Exclusive Or

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CHAPTER 1: INTRODUCTION

1.1 The Need for Neural Recording

The question of how electrical activity in a group of neurons ultimately results in perception, consciousness, and personality has intrigued the neuroscience community since the discovery of bioelectricity by Galvani in the 18th century. In spite of this effort, many fundamental questions remain unanswered, and we still lack a cohesive theoretical framework in which clinically observable high-level processes can be interpreted mechanistically in terms of underlying neural activity. Developing a comprehensive theory of the brain remains one of the last great frontiers of human discovery; a base of knowledge that would not only enable new diagnostic and treatment tools for a variety of neurological and psychiatric diseases but also hold the potential to redefine our view of the human condition.

In the last ten years, this question has attracted unprecedented attention from both private philanthropists (e.g. Paul Allen donating $500M to the Allen Institute for Brain Science) and governments (e.g. the EU spends $1.3B on developing a computer simulation of the brain), which culminated in the announcement of the multi-billion dollar Brain Research through Advancing Innovative Neurotechnologies (BRAIN) initiative by the Obama Administration in February 2013. The goal of this project is to develop a map of the brain at all levels in order to gain an understanding of the function of every neuron in the brain as well as the high-level organization in the brain. The 2013 Kavli Futures Symposium on the subject reports, "We anticipate that the advent of technology that allows a million neurons to be accessed simultaneously and continuously will produce not just a quantitative change in the way that we design experiments and analyze data, but a qualitative shift in the types of questions that can be asked and answered." This view is consistent with the observation that many great advances in science follow on the heels of advances in experimental techniques and instrumentation, a trend that is pronounced in the history of neuroscience: the Golgi stain and electron microscopy showed us neuronal

structure, microstimulation and optogenetics allowed us to write information to neural circuits, and recently, electrocorticography has started to uncover how self-organization and long-range communication may be emerging on the cerebral cortex. The development of new and less invasive neural recording technologies is cornerstone to achieving this vision.

In addition to its impact on fundamental neuroscientific research, clinically viable and minimally invasive neural interfaces stand to revolutionize disease care for patients of neurological conditions. Advancing our ability to interface technology with biological environments will enable patients to be monitored and receive treatment at home, and in the long term, have electronic devices chronically implanted. For example, recent research in Brain-Machine Interfaces (BMI) has shown success in using electronic signals from the motor cortex of the brain to control artificial limbs, providing hope for patients with spinal cord injuries [LEB] [GAN] [HOC2]. Currently, neural interfaces are large, wired and require open-skull operation, leaving the patient at risk of infection and unable to move. Future, less invasive interfaces with increased numbers of electrodes, signal processing and wireless capability will enable prosthetics, disease control and completely new user-computer interfaces. In this section, emerging applications including two applications with a current need for a clinically viable neural interface are studied: motor prosthetics and epilepsy localization.

1.1.1 *Motor Prosthetics*

Hitzig and Fritsch first discovered the motor cortex in 1870 [FRI], although the best-known experimental mapping of the motor cortex dates back to Penfield's experiments in 1937 [PEN] using electrical stimulation to activate muscle groups in patients undergoing surgery for epilepsy. It wasn't until the 1980s, over 100 years since the discovery of the motor cortex, that population coding [GEO] was proposed and thus the beginnings of decoding neural signals in the motor cortex into their corresponding motor function.

In 1998 the first human was implanted with a brain-machine interface (BMI) of high enough quality to simulate movement and demonstrated 2-dimensional control of a mouse cursor [KEN]. Since then, there has been an explosion of demonstrations of motor prosthetic control of computer cursors and robotic arms by both primates and humans. In the last year, the same group demonstrated 4-degree of freedom robotic arm control in a tetraplegic patient [HOC2]. These demonstrations mark a significant step in bringing BMIs from the research arena to viable medical devices. However, a number of technological hurdles must still be overcome to make this a reality.

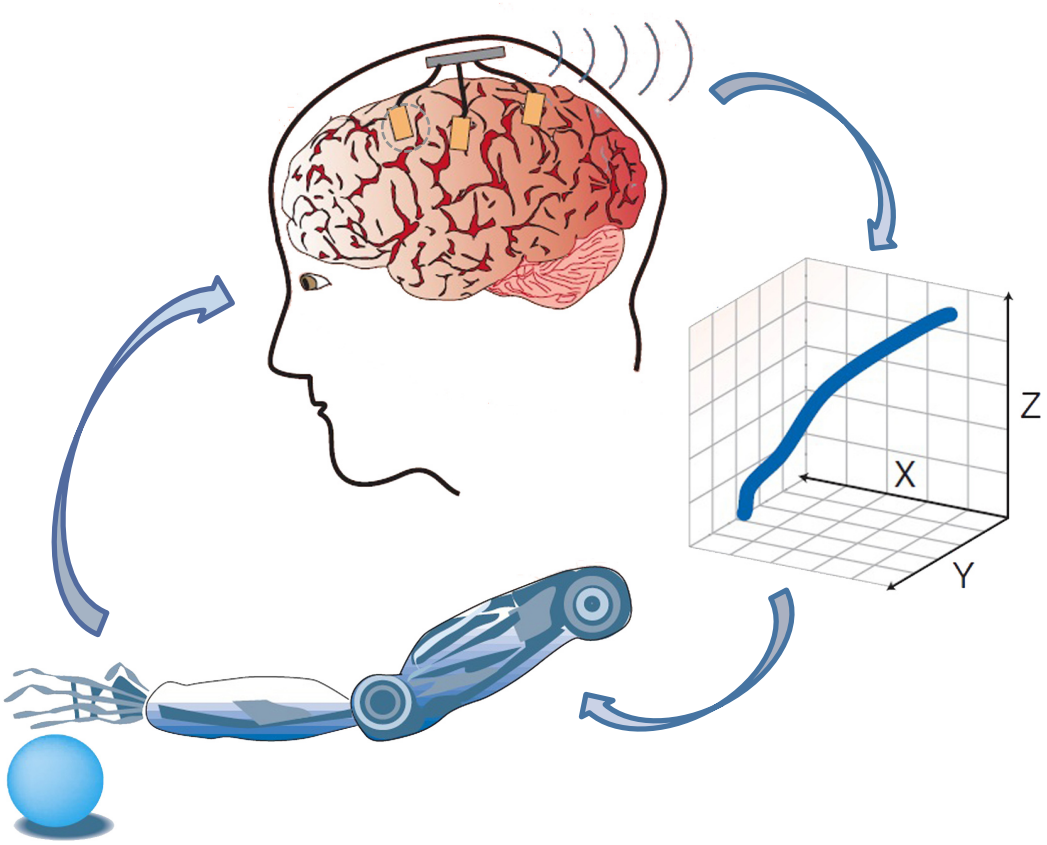


Figure 1-1: Brain-Machine Interface Model, modified from [NIC]

A simplified diagram of a BMI system is exemplified in Figure 1-1. A full BMI system involves a recording device to take signals directly from the motor cortex. This recording device could be an intracortical implant, an extracortical implant, or even external to the body. The signals are then relayed to a computing element, which decodes the signals and uses an algorithm [LI] to trace a trajectory in 3-D space, which is then used to control a prosthetic such as a robotic arm. Location and sensory feedback can be done either through existing intact sensory systems such as vision or through cortical microstimulation [VEN2] enabled by true bidirectional communication with the brain.

While there have been BMIs built using Electroencepahlography (EEG) which is external to the body and therefore non-invasive, the signal resolution is poor and insufficient for most motor tasks. The invasive nature of the electrical contact with the brain is a major hurdle in building BMIs for long-term use in humans. Large, penetrating implants cause cortical scarring, gliosis, and degrade the neural signal on the timescale of months [TUR]. The goal of the BMI implant is to be so minimally invasive that it can be implanted in healthy humans and to make the implant so robust that it can last for decades. This vision is exemplified in Figure 1-2.

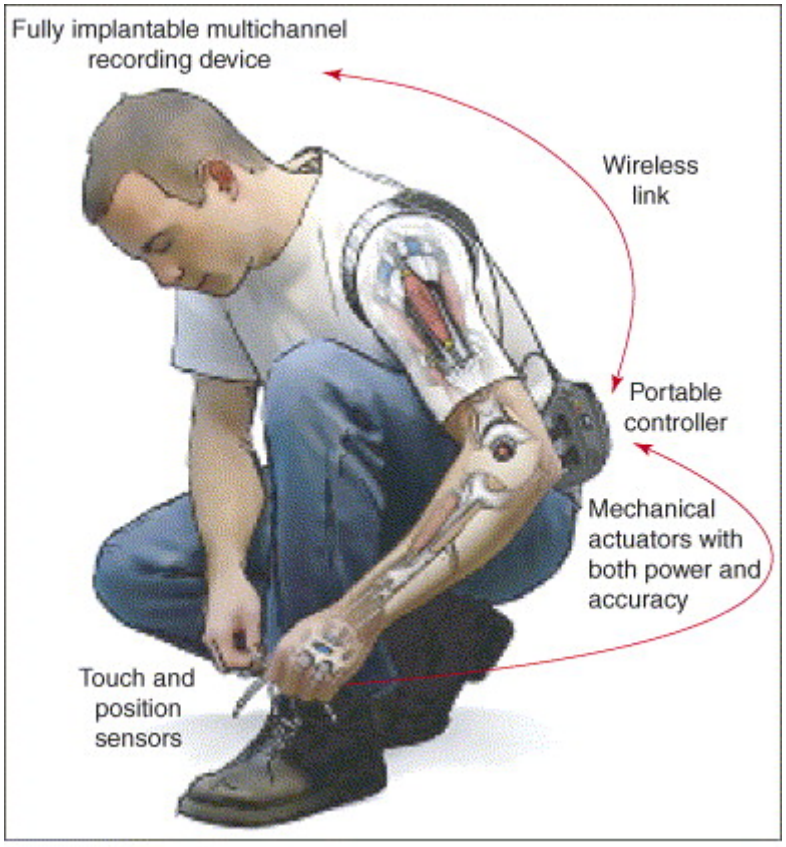


Figure 1-2: Future vision of Brain-Machine Interfaces, from [LEB]

1.1.2 *Epilepsy*

Epilepsy is the most common neurological disease, affecting 65 million people worldwide. One third of patients are unresponsive to any medication and are diagnosed with intractable epilepsy. People with epilepsy experience higher rates of mortality from sudden death, and also live in constant fear of injuring themselves (e.g. falling and drowning), cannot drive, and are excluded from many occupations. In the United States alone, the number of hospitalizations for refractory epilepsy has more than doubled in the past 20 years, representing a major growing medical burden of disease [ENG].

Currently, surgery is the only effective treatment option for intractable epilepsy. While surgical resection has shown promising and even curative results, the outcome is limited due to difficulties in identifying the seizure onset zone. Thus, making precise localization essential. Additionally, the pre-resection diagnostics work-up is an invasive neurosurgical procedure where wires are tunneled out through the skin for weeks, posing significant

infection risks. Such risks cause many to avoid treatment altogether, and therefore many patients are living with uncontrolled seizures when there are potentially curative therapeutic options available. Up to 300,000 patients with intractable epilepsy in United States are potential candidates for epilepsy surgery.

Figure 1-3: Photo from a human craniotomy showing the state-of-the-art use of Electrocorticography for seizure focus localization

Electrocortical (ECoG) grids such as the one shown in Figure 1-3 are used in the clinic to localize the seizure focus for resection. These grids spatially under-sample the brain and are severely limited in the total number of recording channels because they are made by hand. The readout requires wired connectivity and consists of large external amplifiers connected to a computer. Consequently, such devices can only be implanted for a period of less than 30 days to limit the risk of infection.

1.1.3 *Emerging applications for neural recording*

In addition to motor-prosthetics, researchers are exploring other cortical regions for a variety of clinical applications.

Neural recording in disease therapies, which are based on stimulation, are increasing in popularity. The deep brain stimulator (DBS) for example, initially used to treat Parkinson's disease, is now in use also in patients with essential tremor as well as dystonia, and acts as a "pacemaker" for the brain, keeping uncontrolled oscillations of neural activity in check. DBS has also shown efficacy in treating chronic pain, major depression and Tourette syndrome. Recently, the neuromodulation group at Medtronic has published a research prototype for a bidirectional neural interface, which *monitors* brain activity with neural recording circuitry and provide disease therapy only when needed [AVE]. In this work, spectral content is used to determine when a tremor was occurring in the patient and delivered therapy only during those times. This approach improves power efficiency as well as device longevity and minimizes neural damage.

Having the ability to record and process data locally can enable disease therapies which rely on short time scales such as tremor-triggered deep brain stimulation, but can extend to other applications such as inducing activity dependent plasticity. In a 2006 study [JAC] it was proposed that connections severed by lesions or stroke can be strengthened with the use of a neural implant. This study utilized an electronic system to invoke the basic neuroscientific principle of Hebbian plasticity in the brain and demonstrated a potential need for implantable microsystem which has the capability of recording and stimulating. A recent article by the same group [PAI] demonstrated a similar principle, but for brain-to-brain communication by recording from one rat and stimulating in another.

Pasley et al. at the University of California at Berkeley published a study in 2012 [PAS] that showed for the first time he ability to reconstruct speech from the human auditory cortex. The study showed that ECoG readout of the auditory cortex allowed direct identification of individual words through speech spectrogram reconstruction. Showing the capability to identify words directly from brain signals is a key enabler to building a speech prosthetic for patients with certain types of aphasia, a condition that impairs or inhibits speech. Aphasia is most often a result of stroke but can be caused by cancer, traumatic brain injury or neurodegenerative disease.

While each of the above examples is still in the early stages of research, they demonstrate an emerging need for robust and viable neural recording technology and indicate an explosion of the neuroengineering field in the decades to come.

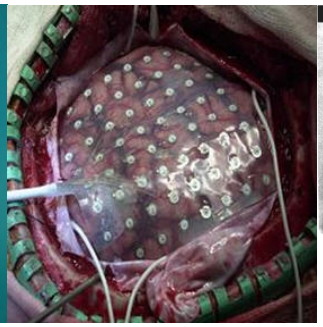
1.2 Clinical viability

In order to realize the vision of fully autonomous, highly integrated neural interface systems it is important to understand the limitations of today's devices coupled with the demands of tomorrow. Devices should not only be effective, but should also meet clinical constraints such as ease of implantation, longevity and ease of patient use. Table 1-1 shows the tradeoffs in neural recording modalities, particularly highlighting issues that affect clinical viability and information content relevant to the design of neural prosthetics.

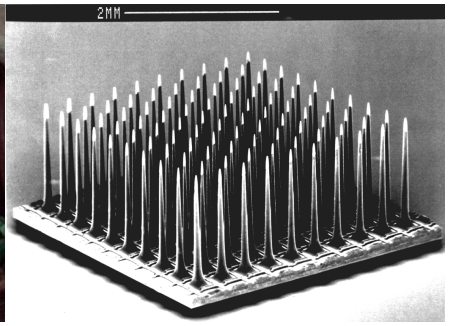
Table 1-1: Neural signal comparison

EEG

ECOG (LFP)



Penetrating (LFP+AP)



	EEG	ECoG	LFP	AP
Bandwidth	0.5-50Hz	0.5-500Hz	0.5-500Hz	250-10kHz
Amplitude	1-10µV	1-100µV	10µ -1mV	10µ -1mV
Spacing	3cm	0.2-10mm	0.1-1mm	0.1-1mm
Invasive	No	Craniotomy, no neural damage	Craniotomy, neural damage	Craniotomy, neural damage
Area Coverage	Whole Brain	~ cm^2 , whole brain	~ mm^2	~ mm^2
Stability	Decades	Decades	Years	Months

Until recently, the neuroscience community has largely focused on action potential (AP) recording as the recording modality of choice for neural prosthetics. Today AP recording remains the highest resolution recording modality but comes at the price of tissue scarring in the brain resulting in signal degradation over the course of several months [TUR]. As such, it is worth exploring techniques to reduce cortical scarring and improve longevity.

Shrinking the size of the implant [SEY] and giving it free-floating, wireless capability [BEI] have both been proposed as potential solutions. In order to enable micron-scale, free-floating wireless sensor nodes, a drastic reduction in implant size and power are required.

While the least invasive solution, electroencephalography (EEG), does not provide sufficient resolution for most BMI applications; less invasive recording techniques, such as ECoG, are gaining popularity in a variety of applications because of their superior longevity. Electrocorticography (ECoG), an electrophysiological technique where electrical potentials are recorded from the surface of the cerebral cortex, has excellent prospects to become the technology of choice for clinically relevant BMI [SCH] since the implant does not pierce the cortex and has much longer signal stability than AP recording, but provides a higher resolution signal than EEG. Using high-density, polymer-based grids [LED] can lead to high-resolution recording at the surface of the cortex and approach the signal quality found in the more invasive LFP recording.

1.3 Neural Signals

1.3.1 *Intracortical signals*

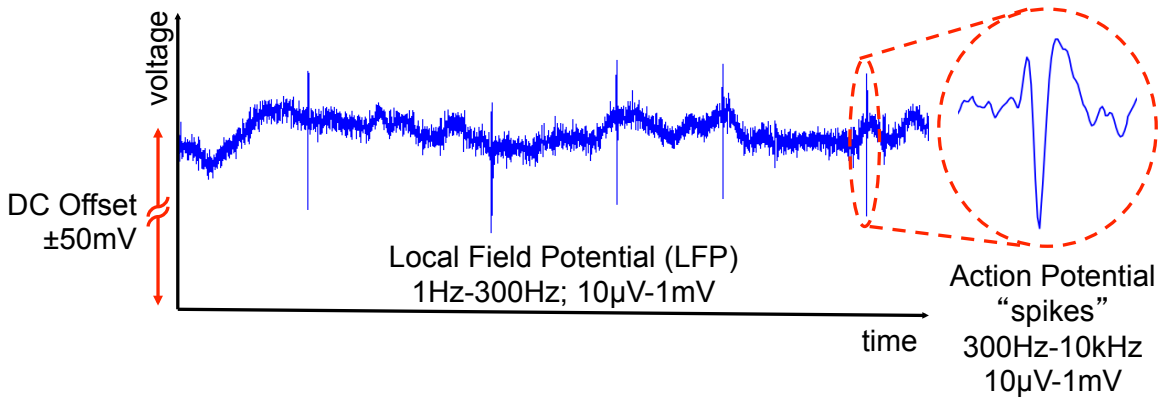


Figure 1-4 Representative neural signal at the electrode/circuit interface.

The key challenge in the design of a neural signal acquisition chain is in separating the μV level desired signal from large offsets and low-frequency disturbances. In neural recording, a DC offset as large as 50mV is associated with the electrodes. Superimposed on the offset, the information-bearing signal is composed of two components. The first is a

slowly varying (<300Hz) Local Field Potential (LFP), representing a spatial average of neural activity in the neighborhood of the electrode. The second component is the higher frequency (300-10kHz) Action Potential or "Spike" events, associated with the firing of individual neurons in the immediate proximity of the electrode as shown in Figure 1-4.

An action potential (AP) is a burst of electrical potential caused by ionic movement across a cell membrane and plays a key roll in cell-to-cell and cell-to-muscle communication [KAN]. The AP is caused by influx and efflux of sodium (Na+) and potassium (K+) ions across the cell membrane and serves a multitude of functions from signal propagation to information encoded in their firing frequency and pattern. In a neuron, APs are triggered when excitatory pre-synaptic potentials (EPSP) pass a threshold triggering Na+ ion channels to open. During this time the membrane potential typically goes through a 100mV-150mV potential change. In extracellular recordings the potential change observed is variable and often on the order of 100s of microvolts. This is because the ions diffuse through the extracellular medium causing rapid drop-off of observable potential. Thus the amplitude of a recorded AP is a result of both the type of cell and the distance of the electrode to that cell. The high-frequency "noise" that appears superimposed on the LFP and between the large spikes is simply the spiking of the thousands of neurons that are far from the electrode and thus have small amplitude. The fact that they are caused by APs makes them difficult to filter since they have similar frequency content and waveform shape to the signal of interest.

The complete neural signal observed is a result of the cumulative electrical signals in a "listening sphere" of the electrode, including action potentials and synaptic potentials, of all local neurons. The local averaging of these signals appears as the LFP, which contains information about the population of neurons in the sphere of the electrode. The LFP relates well to sub-threshold integrative processes in dendrites and may reflect the synaptic activity. It has also been shown to encode movement and movement intention in the motor cortex [SCH1] [HEL]. Information in the LFP is processed differently from the information in the AP where waveform shape and timing are important. The LFP is observed in time-frequency space where it is normalized to a baseline activity to account for its $1/f^n$ power spectrum [VEN]. These decoding methods were developed primarily for EEG and ECoG signals and are discussed in the next section.

1.3.2 *Electrocorticographic signals*

Richard Caton first published observations of electrical phenomena of the exposed cerebral hemispheres of monkeys and rabbits in 1875 [CAT]. German physiologist Hans Berger recorded the first human EEG in 1924 [BER] and invented the

electroencephalogram, expanding on the work previously conducted on animals. In 1934 EEG was first used to observe electrical patterns of seizures. Since then EEG has been widely used to detect and monitor synchronous neuronal behavior that is observable at low frequency such as sleep patterns, levels of consciousness and seizures.

Electrocorticography, also known as intraoperative EEG (iEEG) was pioneered in the early 1950s by Penfield and Jasper [PEN2] and developed as a tool to identify epileptogenic zones for surgical resection. They further used the technique to map the critical functional brain areas. As discussed in Section 1.1.2, it is largely used to this day for the same purpose it was invented for. Recently, ECoG has seen a surge in popularity as a tool for neuroscience researchers to perform experiments in a clinical setting.

What separates ECoG from EEG is the proximity to the neuronal signal source. ECoG signals are 1-2 orders of magnitude higher signal power, contain broader spectral content, and provide higher spatial resolution. These advantages come from three main sources:

1. Signals are not as heavily filtered through approximately 1.5 centimeters of additional skull and tissue.
2. Geometrical constraints only allow for EEG electrodes to be spaced 1-2cm apart, while ECoG electrodes can be spaced much closer together enabling a higher spatial resolution. Spatial resolutions down to 100s of microns have been reported [LED] [VIV]. As electrodes become more closely spaced they begin to overlap cortical columns and can thus produce highly redundant information, therefore finding an optimal electrode pitch remains an active area of research [SLU].
3. Electrode surface area scales down with electrode pitch resulting in a higher signal bandwidth. Since a large electrode will effectively average the signal from sources underneath it, a smaller electrode will average a smaller area of the cortex. This means that less synchrony is required in order to produce a signal in a particular spectral band and high-frequency signals, which tend to be incoherent, are averaged to a lesser degree.

Until the last decade, the spectral content of EEG and ECoG was limited to 60Hz. This is largely because researchers low-pass filtered the signals at 60Hz to eliminate line noise and since the EEG spectrum is negligible at higher frequencies. It was only in the last decade that researchers began to explore the high gamma band above 60Hz in ECoG [CRO] [EDW]. The ECoG spectrum is divided into frequency bands whose modulation of power has been correlated to various brain states as show in Figure 1-5 and Table 1-2.

A representative plot of an ECoG signal is shown in Figure 1-6. Unless specific oscillations are present, the time-domain waveform is not discernable from electronic 1/f noise; therefore ECoG is commonly analyzed in the frequency domain. ECoG signals are

similar to LFP that is recorded from the top layers of the cortex and averaged over a broader area. Like the LFP, ECoG signals have a $1/f^n$ spectrum where $1 < n < 2$. Increases and decreases of spectral bandpower are analyzed as deviations from a baseline of neural activity. In order to observe spectral changes over time, time-frequency spectrograms and wavelet transforms are commonly used.

Table 1-2: Table of brain waves and associated functions

δ	Anesthesia, sleep
θ	Arousal, drowsiness
α	Relaxation, eye closing
β	Waking consciousness
Low γ	Alertness, perception
High γ	Sensorimotor function

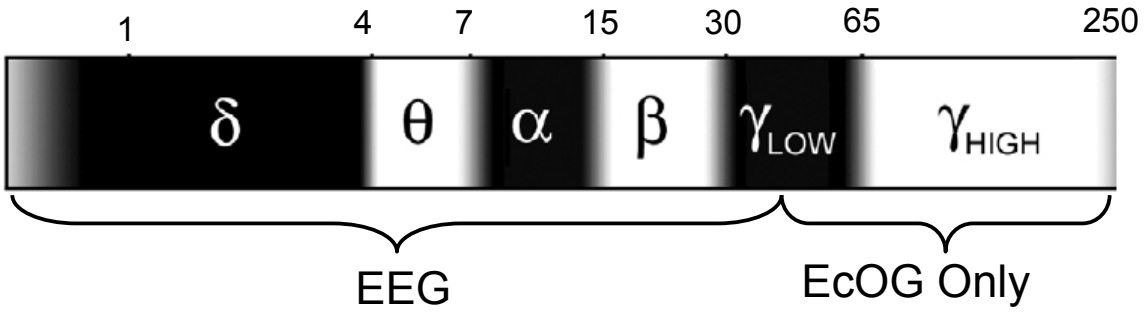


Figure 1-5: Frequency bands of extracortical neural signals

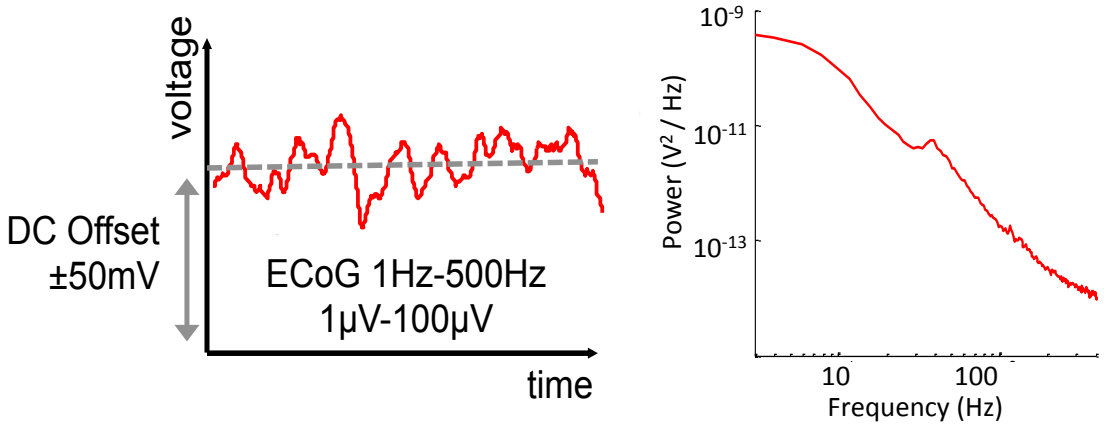


Figure 1-6: Representative ECoG time-domain (L) and frequency domain (R) signal.

1.4 Implantable System

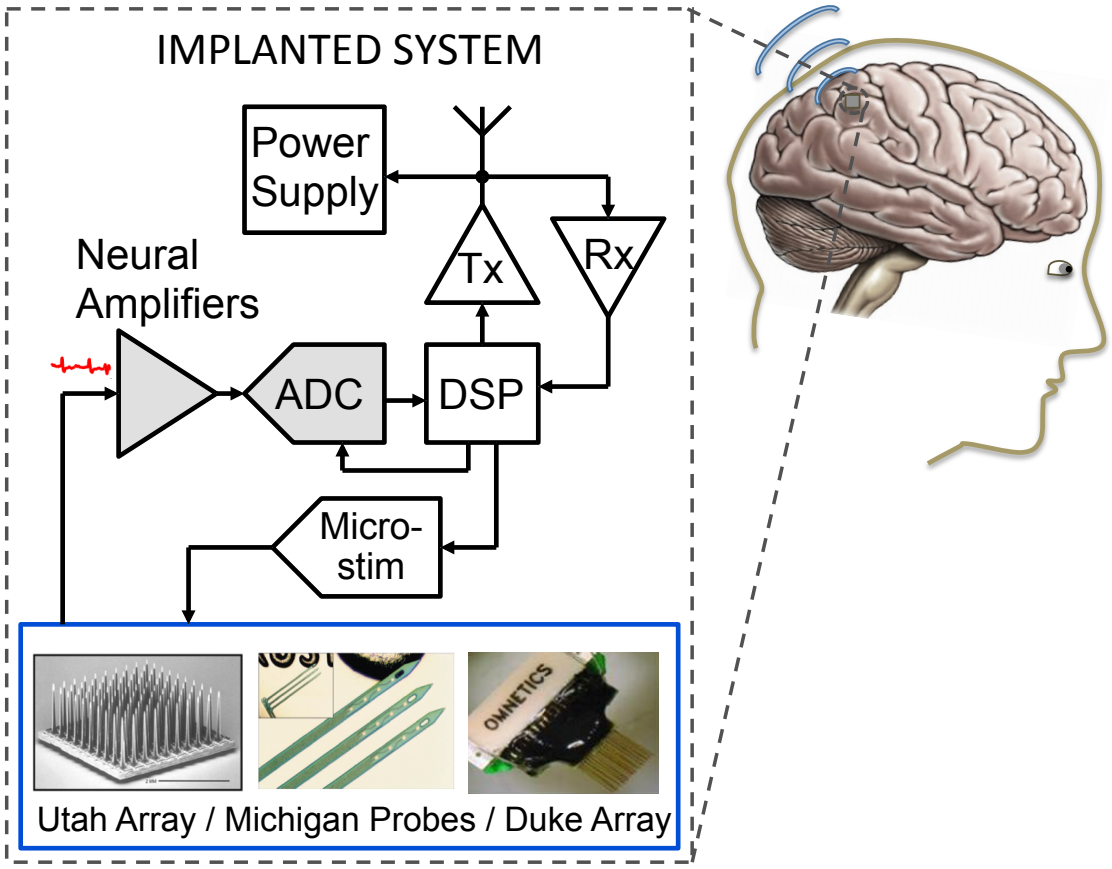


Figure 1-7: Block diagram of an integrated circuit for an implantable neural recording system. The inset at the bottom of figure shows examples of commonly used electrodes.

Figure 1-7 shows the components required for any generic fully implantable wireless neural recording system. Battery-less operation requires wireless power coupling, while wireless data transmission eliminates wires, allowing the surgeon to close the surgical site, thus restoring mobility and lessening the risk of infection. A mixed-signal front-end is required to digitize the signals from each electrode. To record from multiple sites simultaneously, one front-end is required per active electrode, thus the implanted chip may have hundreds of arrayed data acquisition channels, which dominate the chip area and power in current implementations [AZI] [HAR]. Future electrode arrays with greater number and density of recording sites will only increase the power and area constraints placed on these front-ends.

The key to transitioning these interfaces to be safely used in humans is three-fold:

1. Shrink the size of the implant to minimize cortical scarring, immune response, and gliosis in addition to simplifying surgical implantation.
2. Add wireless capability so that the surgical site can be closed, drastically reducing the risk of infection and restoring mobility and autonomy to the patient.
3. Design the implant electronics for low-power operation in order to stay within IEEE safety guidelines [IEE] for human body RF exposure.

1.4.1 *Electrodes*

Several types of electrodes are used currently in research systems. For action-potential recording, platinum-Iridium (Pt-Ir) microwire arrays [PAL] [NIC2] and micro-fabricated silicon arrays [CAM] with a single recording site per electrode are common today and widely used by neuroscientists. Michigan style probes [OLS] [BLA], featuring multiple recording sites along the depth of a microfabricated electrode are also relatively widespread and are used when depth, high-density, or three-dimensional recordings are required. Current state-of-the art electrode systems have a typical pitch of 400μm and a typical impedance of 100kΩ at 1kHz, necessitating small and high-impedance interfaces. Recent implementations of electrodes with multiple electrodes on a single shaft have pitches down to tens of microns [SEI] [LOP], necessitating highly miniaturized neural circuitry.

Electrodes at the surface of the brain average the electric fields in the fluid over their contact area. As a result larger electrodes are used in non-penetrating recording such as ECoG, where lower frequency fields are of interest. For a typical ECoG grid, 1mm diameter circular metal electrodes with a 5mm pitch are used, resulting in a typical impedance of 10kΩ at 1kHz. Microfabricated ECoG grids have been recently proposed [LED] [VIV] [RUB], offering a tradeoff between smaller electrode size and pitch (down to 200μm and 500μm) with increased impedance and higher signal spectral content.

Finally, it is important to remember that all electrode systems are inherently non-linear because of the possibility for ionic transport of the electrode material into the solution. While AC currents, such as stimulation currents, are often high amplitude, to prevent long-term electrochemical effects, DC currents through the electrodes should be kept below 50nA.

1.4.2 *Powering and communicating with neural implants*

Battery-assisted wireless systems require perilous and expensive surgeries for replacing the discharged batteries. In [RAB] power densities of various sources were compared and concluded that electromagnetic power transfer can provide 2-3 orders of magnitude higher power to an implant. Thus, achieving fully wireless and battery-free operation is presently a major focus in the research on BMI hardware. State of the art work on implantable antennas for BMIs has been focused on antenna miniaturization [ODR] [MAR1] in order to minimize tissue scarring and immune response to the implant. However, this extreme miniaturization has been at the expense of link power efficiency, which drops sharply as the implant size is reduced below a few millimeters [RAB].

For a 2mm by 2mm implant size (corresponding to approximately to a 25-electrode array), and a transmitter meeting both FCC and IEEE regulations, the available power is the order of 140μW [ODR2] or approximately 5.8μW/electrode. Allocating 10% of this power budget to the radio, and noting that a typical AP front-end produces 160kBps/channel, the radio energy efficiency and aggregate data rate should be approximately 3.6pJ/bit and 4Mbps, both of which can be achieved through backscattering [SARP]. Assuming there is little explicit digital signal processing, this leaves 5.2μW for acquisition, making the baseband design challenging.

Since the number of channels scales linearly with the implant area, but the available power has a super-linear dependence, larger arrays have larger power budgets available to each channel. In this case, the challenge becomes achieving the increasing data-rate (i.e. 16Mbps for 100 channels). Conversely, trying to make highly miniaturized implants that are 1mm x 1mm [MAR1] or smaller can put extreme demands on the system power dissipation, requiring all circuits to consume less than 5μW.

Data communication throughput also scales linearly with the number of sensor sites and therefore scales with implant area unless there is compression done locally on the implant integrated circuit. To understand the datarates required, let us take two extreme scenarios. A small ECoG grid that has four sensor sites that are each digitized with 10 bits of resolution at 500Hz would require 20kbps. On the other hand, a 256-channel intracortical neural interface for AP sensing digitized at 10 bits and 20kbps would require 51Mbps. For most existing implantable neural recording systems [CHAE] [LEE] [SOD] [HAR] [BEI] the data-rates required range from 20kbps - 25Mbps.

Three primary categories of transmitter architectures have been proposed for implantable medical systems: narrowband systems at the 400MHz medical implant communications service (MICS) band, ultra-wideband (UWB) technologies, or passive backscattering transmitters such as those used in radio frequency identification (RFID) tags. Early work

on neural implants proposed frequency shift keying (FSK) transmitters [HAR] [RAI] with power consumptions on the order of mW, making them an unattractive choice for highly scale, power-constrained implants. UWB transmitters have been explored in the context of neural implants [CHAE] and extensively explored for ultra-low-power wireless sensor networks [GAM] [MERC]. UWB has been demonstrated to be power efficient, trading off a simpler transmit architecture for a more complex receiver architecture. UWB radios typically dissipate power on the order of 10s to 100s of microwatts for short-range communication data rates of tens of Mbps but are best suited for systems that are locally or battery powered rather than remotely powered since they require up-conversion.

For remotely powered systems, backscattering is the most power efficient strategy since it does not require carrier generation, power amplification, or an on-chip frequency reference [BEI]. While the carrier is downconverted to DC to provide power to the implant, reflecting the incident signal back to the external transmitter mitigates the added step of upconverting the energy to generate a high-frequency carrier. There are several major drawback to this technique: it suffers from two-way propagation loss necessitating high power from the transmitter, the reflected signal is at the same frequency as the incident signal resulting in high carrier leakage, and finally it is difficult to realize at datarates in the range of Mbps and above, therefore scaling to higher data-rates remains an active area of research.

1.5 Neural Amplifiers and Front-Ends

Many of the same basic challenges exist for all neural front-ends whether they are intracortical or extracortical. In particular, implantable electronics suffer the consequences of both an extremely space-constrained and an extremely power-constrained environment. The following list of characteristics contains the goals of all neural signal acquisition front-ends:

- Low-power dissipation: this constraint is required for all power sources such as battery, wireless power coupling or energy scavenging.
- Low input-referred noise: all neural signals are extremely small, on the scale of μV and therefore require low-noise electronics. The noise requirements become more and more difficult to meet as the sensor gets farther away from the neuron.
- Offset rejection: all recording electrodes suffer from mismatch that leads to DC voltage offsets at their terminals, which must be rejected.
- High CMRR and PSRR: large interfering signals such as 60Hz ambient noise or artifacts from stimulation may appear on the power supply or input electrodes.

The above constraints will be discussed in the following subsections together with additional considerations which are specific to the recording modality.

1.5.1 *Action Potential Front-Ends*

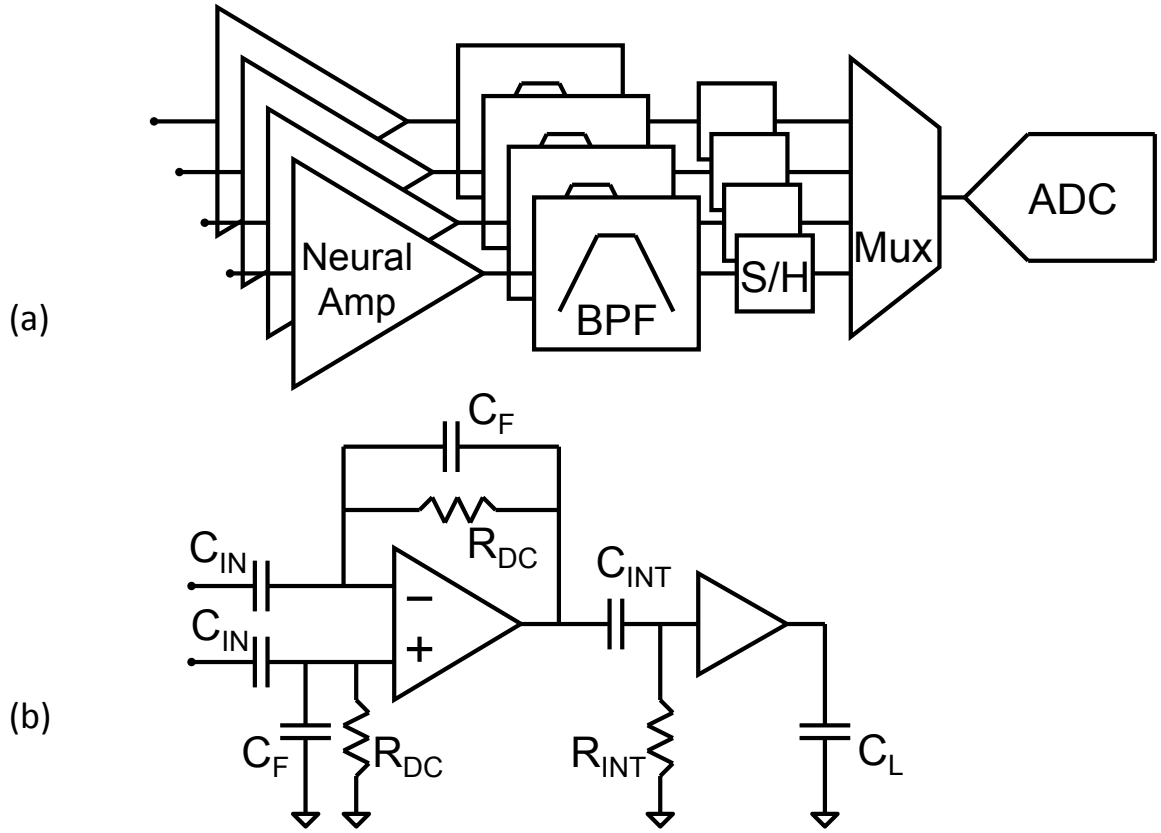


Figure 1-8: (a) State-of-the-art multi-channel signal acquisition chain and (b) neural amplifier and band-pass filter.

Both LFPs and Spikes are relevant in prosthetics and neuroscience [AVE] [AZI] [HAR] [WAT]; it is therefore optimal to digitize both signals simultaneously. The relative magnitude of these signals depends on the location of the recording electrode and its proximity to the neurons. In a worst-case condition, spikes with amplitudes of the order of 10s of μV can appear simultaneously with LFPs with amplitudes of 1mV. Assuming a minimum signal to thermal noise ratio requirement of 10dB for Spike digitization, an input referred noise on the order of 5μVrms is required. The total dynamic range required by the acquisition chain is approximately 50dB after offset removal, and >80dB including the offset. Therefore if all signals were digitized together using a single ADC, resolution in excess of 14 bits would be required. Even for a 0.1pJ/step figure of merit, this ADC

would consume over 30μW when sampling that data at 20kHz. Therefore, signal conditioning prior to A-to-D conversion is necessary in order to obtain a compact and power-efficient solution.

State-of-the-art neural signal acquisition systems [AVE] [AZI] [HAR] [WAT] typically employ an acquisition chain such as the one shown in Figure 1-8 (a), consisting of a low-noise amplifier (LNA), a band-pass filter to filter either the spike or LFP bands, an analog sample-and-hold, and a multiplexer which serializes multiple channels into a single high sample rate ADC. These designs have relied heavily on analog techniques to implement the LNA and band-pass filter by using AC-coupled instrumentation amplifiers with capacitive feedback followed by analog filtering (Figure 1-8 (b)).

Most implementations use a capacitive feedback topology to simultaneously reject the offset and obtain stable gain for the signal. The design is driven by the need to acquire both local-field potentials and action potentials, requiring a high-pass cutoff of the order of 10Hz.

The values of capacitance required by C_{IN} and C_F are determined by the time constants required for offset and LFP separation as well by the maximum resistor values that can be implemented. For typical values of a 10Hz high-pass pole, $R_{DC} = 100G\,\Omega$ and $C_{IN}/C_F = 100$, we find $C_F = 0.15pF$ and $C_{IN} = 15pF$. In a standard process, even if linear capacitors with density of $2fF/\mu m^2$ were available, the area occupied by C_{IN} alone would be $0.015mm^2$. A literature survey [JOC] confirms that it is difficult to scale the area of a complete neural acquisition chain utilizing AC coupling below $0.04mm^2$. From a system standpoint, since current AP electrodes have a 400um pitch, a total acquisition chain area below $0.16mm^2$ is acceptable. While the figures above seem well in range, obtaining 100G resistors in a repeatable manner is challenging, and the high-pass pole location could vary by as much as 10x for typical implementations. As a result, smaller recording amplifiers with stable high-pass poles still require development.

At the core of the closed-loop amplifier topology is a low-noise, high-gain operational transconductance amplifier (OTA). High gain is employed in the OTA leading to traditional topology choices, which include but are not limited to: folded cascode [WAT] [HAR], telescopic cascode [AZI] [SHA], current mirror [GOS], common source [HOL] and two-stage [CHAE2]. Some of the tradeoffs of these amplifier topologies are discussed in the following paragraphs.

Well-known analog design considerations apply to this problem: simultaneously obtaining low noise and low power consumption requires maximizing the transconductance of the input differential pair, while minimizing the number of noise

contributing devices by topology choice and their transconductance by biasing. As the signals swings are <100mV in this context, aggressive supply reduction can be utilized at no costs in current consumption [WAT]. As expected, using a single common-source stage is noise efficient since it has the fewest number of devices, but is not a practical topology since it has extremely poor power supply rejection. Similarly, telescopic amplifiers perform better than folded and current-mirror amplifiers.

Current reuse input stages [CHAE2] also double the transconductance and hence reduce noise. The recently proposed orthogonal current reuse [JOH] also reduces the total input-referred noise while consuming the same current as a traditional differential pair and can provide even larger benefits than current reuse. From a system perspective, the reported amplifier power and performance is finally catching up to the requirements of wireless powering. However, increasing the recording density further increases the demands on area and power efficiency, leaving this an active area of research.

Filtering and digitization have received less attention from the research community than low noise amplifiers and have less impact on system performance, but they still contribute significantly to area occupation and system complexity. State of the art employs Gm-C [HAR] or switched capacitor filtering [WAL] to separate action potentials and LFP signals in the analog domain, so that area occupation is again dictated by capacitance density. Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) are used for digitization and often the ADC is shared amongst multiple recording sites, necessitating in-channel sample and hold amplifiers to ensure simultaneous acquisition. In [WAL] for example the in-pixel ADC occupies approximately 40% of the pixel area of 0.26mm^2.

1.5.2 *ECoG and EEG Front-Ends*

As discussed in Section 1.2, penetrating electrodes have a limited lifetime due to scarring, and future long-term neural interfaces are likely to employ ECoG or micro-ECoG recordings [SCH]. While much of the same considerations discussed in the previous sub-chapter apply to these implant systems as well, some major differences exist:

1. ECoG grids, even in their miniaturized incarnations, are larger than micro-electrode arrays. This implies a larger antenna can be used, so that more power is available at the implant side.
2. ECoG signals have a maximum frequency content of 500Hz. As a result the wireless transmission data-rate per channel is reduced to approximately 12kbps per channel.

3. ECoG signals are measured further from the neurons and can be smaller than AP signals, so that a lower noise floor of approximately 1μV is required. In addition, while 1/f noise can be mitigated through sizing in AP recordings, the low bandwidth of ECoG signals demands 1/f noise mitigation techniques to be used in the front-end. This is particularly difficult as it must be achieved while maintaining a high input impedance and low-offset.

The most common and simple 1/f noise reduction technique is to employ chopper stabilization. This technique up-modulates the signal by multiplying it with a square wave with an amplitude pattern of +1, -1, allowing the signal to be amplified at a higher frequency mitigating low-frequency interferers such as 1/f noise and amplifier offset. The signal must then be down-modulated and filtered in order to recover the original signal.

The consequences of consideration 3 above are illuminated by analyzing the tradeoff between noise and amplifier input impedance when chopper stabilization is employed. The noise power spectral density of a chopper amplifier is derived in [ENZ]. An approximation is given by

$$S_N \approx S_{nO}\left(1+\frac{17f_k}{2\pi^2 f_{chop}}\right) \tag{1-1}$$

where S_{n0} is the thermal noise power spectral density, f_k is the 1/f noise corner frequency and f_{chop} is the chopper stabilization clock frequency. From this approximation alone, maximizing f_{chop} seems optimal to minimize noise. In reality, a high f_{chop} will lead to low input impedance, therefore an optimal value, which balances these two constraints, must be found. A good tradeoff can be found by selecting chopper frequency is where f_{chop} is at least $2f_k$ making the second term of Equation 1-1 contribute only 20% or less to the total voltage noise.

Consider the state-of-the-art design pictured in Figure 1-9. Using a simplified model of the input chopper switches, the input capacitance of the amplifier at each positive and negative input is approximately C_i since the summing nodes of the amplifier can be approximated as virtual grounds. When switched at f_{chop}, the differential input impedance of the amplifier can be shown to be

$$Z_{in}=\frac{1}{2f_{chop}C_i}. \tag{1-2}$$

Since a high f_{chop} will degrade the input impedance it is important to consider both simultaneously. In [DEN] the value for C_i is 15pF while in [FAN] the value of C_i is 12pF. Chopping at moderate frequencies between 5-20kHz yields input impedances that range 2MΩ-6MΩ. While these impedances are high enough to pass the ECoG signal for most standard electrodes, micro-electrodes can reach impedances in the MΩs, therefore higher input impedance is desirable.

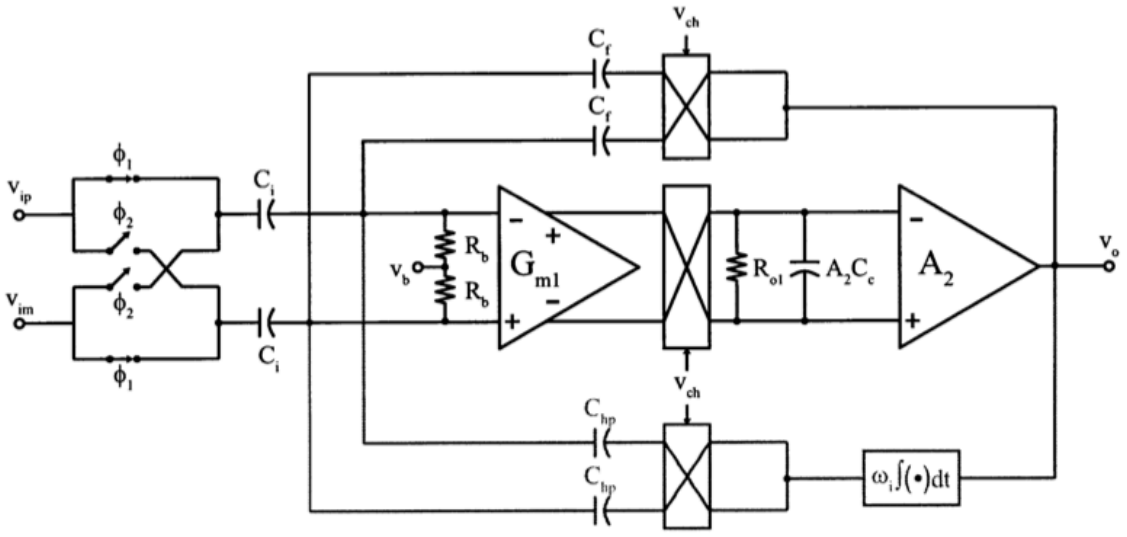


Figure 1-9: State-of-the-art high-precision neural amplifier architecture, from [DEN]

Since there is a large offset associated with the electrode interface the offset is upmodulated together with the signal and is therefore not blocked by the input capacitors. Without explicit offset cancellation the amplifier will saturate, mandating a feedback loop dedicated to cancelling the offset in the up-modulated domain. State-of-the-art utilizes a switched-capacitor integrator in the feedback path to track the DC signal and is then chopped to provide cancellation in the upmodulated domain. These high-precision, sensor interfacing instrumentation amplifiers suffer from the integration of large passive components at an even greater extent than their action-potential counterparts. The necessity of this filter can lead to areas that are an order of magnitude larger than action potential amplifiers.

An alternative solution has been proposed [VER] where chopper switches are implemented at the summing junction of the amplifier after input AC-coupling capacitors. In this implementation the chopper switches create a switched capacitor resistance with the parasitic capacitance on the summing node of the amplifier. In the case of [VER] this resistance is 1GΩ. The caveat is that this resistance creates a high-pass filter pole together with the input capacitors; therefore in order to keep the pole below 1Hz, an input capacitance of at least 100pF is required making the implementation impractical. In [VER], 1nF off-chip capacitors were used to provide a pole at 0.1Hz.

To date the largest array of ECoG or EEG front-ends on a single die is 8 [YAZ], and occupies a staggering 3.6mm^2 of die area for the amplifiers alone. Considering this bottleneck, designing highly scaled, miniaturized platforms is critical to enabling the

integration of hundreds of front-ends in a practical silicon area and lead to devices that can be used in humans without cortical scarring.

1.6 Scope of this Thesis

This introduction discussed the need for minimally invasive, wireless, implantable neural recording devices. An overview of current state-of-the-art devices and their requirements was also given. The majority of this thesis is focused on one key element to shrinking the footprint and power consumption of the implant: the neural signal acquisition front-end. The remainder of this thesis is organized as follows. In chapter 2 a neural signal acquisition front-end for AP and LFP recording is described. A digitally intensive architecture is used to reduce the footprint by more than 3x, the supply voltage more than 2x, and maintain or improve power efficiency when compared to state-of-the-art designs. Measurement results including *in-vivo* measurements are given. Chapter 3 describes a neural signal acquisition front-end for ECoG which builds on the principles described in Chapter 2 and transitions them to lower frequency and higher precision. The ECoG front-end achieves an order of magnitude improvement in area occupation and over 3x improvement in power efficiency over state-of-the-art designs. The advantages of the small power-efficient front-end culminate in a 64-channel fully integrated implantable wireless ECoG platform that is described in chapter 4. The components of the system are described together with measurements of the 64-channel front-end array and *in-vivo* measurements in a rat. Finally, conclusions and future directions are discussed in Chapter 5.

CHAPTER 2: ACTION POTENTIAL SIGNAL ACQUISITION

In order to address the challenges of low-power low-area neural recording, this chapter describes a complete neural signal acquisition channel in 65nm CMOS and operating at a 0.5V supply that obtains state-of-the-art performance in a silicon area over three times smaller than the smallest neural amplifier previously reported [AZI]. A compact solution is obtained by using a system architecture tailored to an advanced process that avoids on-chip passives and takes advantage of high-density logic and aggressive process voltage scaling to reduce power and area.

This area-efficient neural signal-acquisition system uses a digitally intensive architecture to reduce system area and enable operation from a 0.5V supply. The architecture replaces AC coupling capacitors and analog filters with a dual mixed-signal servo loop, which allows simultaneous digitization of the Action and Local Field Potentials. A noise-efficient DAC topology and a compact, boxcar sampling ADC are used to cancel input offset and prevent noise folding while enabling "per-pixel" digitization, alleviating system-level complexity. Implemented in a 65nm CMOS process, the prototype occupies 0.013mm^2 while consuming 5μW and achieving 4.9μVrms of input-referred noise in a 10kHz bandwidth.

2.1 Action Potential Front-End

2.1.1 *Front-end architecture selection*

In order to scale the die area occupied by the signal acquisition chain below this mark and to enable simultaneous LFP and spike digitization, we employ the architecture shown in Figure 2-1 [MUL1] [MUL2]. The AC coupling capacitors are removed, and the offset is mitigated using a mixed-signal feedback loop. The forward path is composed of a

broadband instrumentation amplifier that is DC-coupled to the electrodes and an ADC, while the feedback path, comprised of a DAC and a digital low-pass filter H(z), realizes a servo-loop that suppresses the offset and the LFP. Feedback forces the output of the digital low-pass filter to reproduce the sum of the low-frequency components, reducing the dynamic range requirement of the instrumentation amplifier and ADC cascade. Therefore, the ADC outputs a digitized version of the "high frequency" spike band. In addition, the output of the digital filter provides a digitized version of the low-frequency components and becomes the LFP output. Both LFP and spike bands are thus digitized simultaneously using the same hardware. The large time constants necessary to effectively separate the two components are realized in a compact footprint by H(z) using digital gates.

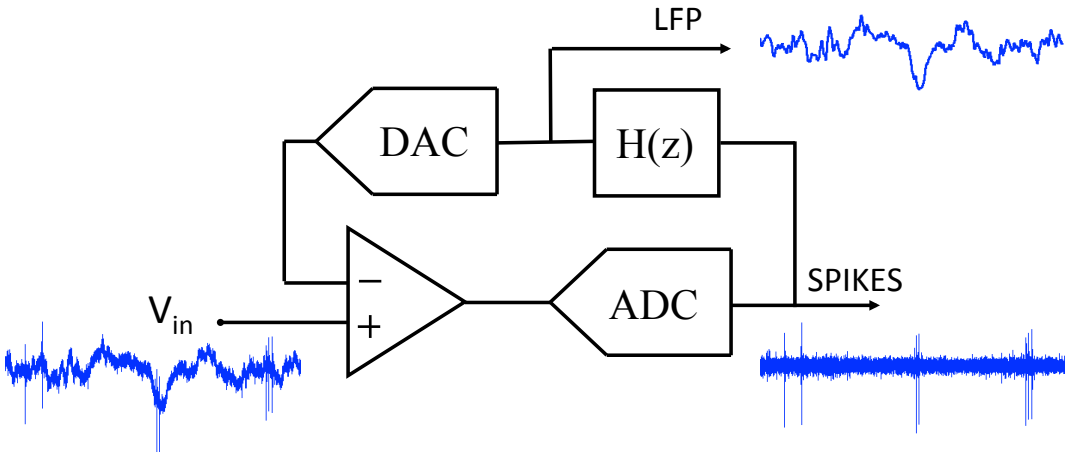


Figure 2-1: Mixed-signal feedback architecture.

When realized in a 65nm process, the architecture in Figure 2-1 has several advantages over traditional solutions such as low area, programmability and "per-pixel" digitization, which replace the complicated routing of analog signals at the top level. The efficient realization of the architecture presents a few challenges that are discussed in detail in the following sub-sections.

2.1.2 *Electrode interface and safety*

Since the integrated circuit makes direct contact with the electrodes it is important to make sure that safe current levels are maintained in both normal operation and when there is an electrostatic discharge (ESD) failure. At the same time, the on-chip common-mode voltage must be stabilized. A string of diode-connected sub-threshold MOSFETs is used to stabilize the DC common mode voltage in a method similar to [MOH] to 4/5 V_{DD}

or 400mV (Figure 2-2). The small signal DC resistance of the on-chip bias network is approximately 1GΩ. Constraints on accuracy and matching of the resistors are relaxed since the offset is cancelled and the refresh rate can be programmed to cancel drift in electrode offset and DC characteristics.

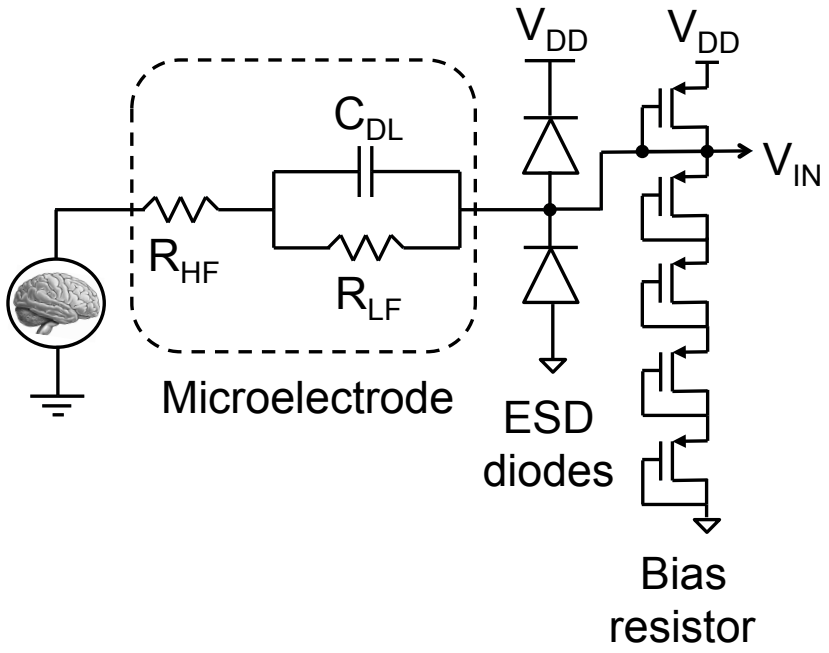


Figure 2-2: Microelectrode small signal model and IC interface

Ideally the circuit can interface with a variety of microelectrodes such as those shown in Figure 1-7. A simplified small-signal model of an electrode is shown in Figure 2-2. The DC resistance of the electrodes R_{LF} given by the equilibrium exchange current is very high; for example, a platinum microelectrode with an area of 1000μm^2 has >30GΩ of DC resistance [FRA].

Figure 2-3 confirms that Utah-style microelectrodes with platinum tips have a resistance >30GΩ in their linear range. In parallel to this resistor, a capacitor C_{DL} (formed by the electrical double layer at the metal-tissue interface) dominates the impedance in the signal band. A more accurate model for C_{DL} is a constant phase element whose capacitance changes with frequency and is on the order of 1-3nF at 1Hz. The chosen 1GΩ bias network impedance stabilizes the DC operating point while setting (together with C_{DL}) a high-pass filter pole below the 1Hz signal bandwidth. As a result, thermal noise generated by the bias network in either the LFP or the spike band is shunted by C_{DL} and does not impact the system noise floor.

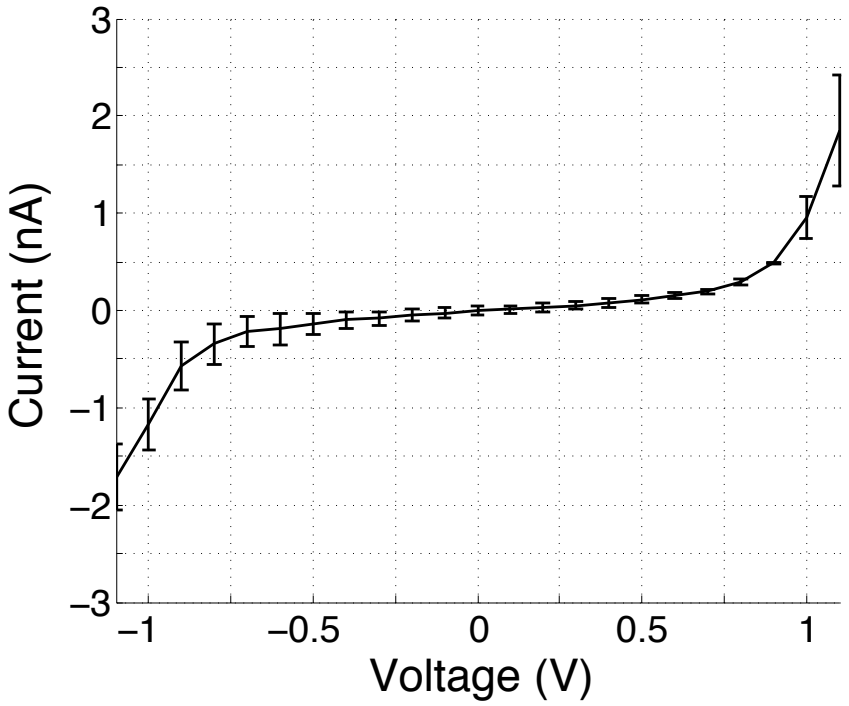


Figure 2-3: Average and standard deviation I-V curves of "Utah-style" microelectrodes from a single array. The measurement is made differentially across two electrodes.

Figure 2-3 shows measured I-V curves for the current between two electrodes of a Utah-style polysilicon microelectrode array from Blackrock Microsystems measured in Phosphate Buffered Saline (PBS). In the event of an ESD failure, a worst-case voltage equal to the on-chip power supply voltage of 0.5V is applied across the electrodes and a worst-case current of approximately 200pA results, well within safe levels of operation [MERR]. In comparison, an IC with a V_{DD} = 1V would suffer currents 10 times larger due to the non-linearity of the I-V relationship. Bubbles in the PBS/electrode interface are visually observed at approximately $\Delta V \geq 3.8V_{DC}$.

2.1.3 *Gain and offset correction range allocation*

Open-circuit potential measurements of the electrodes show that offsets can be on the order of 100s of mV. Because of the large value of R_{LF}, even if there is an open-circuit potential of 1V, the offset seen at the chip input will be attenuated by the on-chip resistor to 30mV, and the DC current flowing through those electrodes will be 15pA, well below electrolysis-inducing current levels. In this implementation, an offset range of ±50mV was chosen, however this range could be extended as will be discussed in section IV. For typical values of offset (up to ±50mV) and assuming a maximum input-referred noise floor of 5μVrms, the DAC in Figure 2-1 requires a resolution of 16 bits to suppress

quantization noise well below the thermal noise floor. To mitigate the DAC resolution requirements, the offset and LFP cancellation is split into a dual-loop architecture that uses a coarse-fine approach, as shown in Figure 2-4. First, a 7-bit DAC performs coarse offset cancellation, reducing the total offset processed by the acquisition chain from +/-50mV down to 1mV. The noise and common-mode rejection requirements of this DAC are critical and require the use of special circuit techniques described in the next section. The second, fine loop has a DAC resolution of 9 bits, which is necessary to suppress the residual offset as well as the LFP signals without degrading the SNDR in the spike band. The time scales of the coarse and the fine offset loops are separated: coarse offset cancellation is performed at slow rates (programmable between 0 and 1 Hz) using a binary search; while the fine loop is closed through a linear filter H(z) and has bandwidth comparable to the LFP.

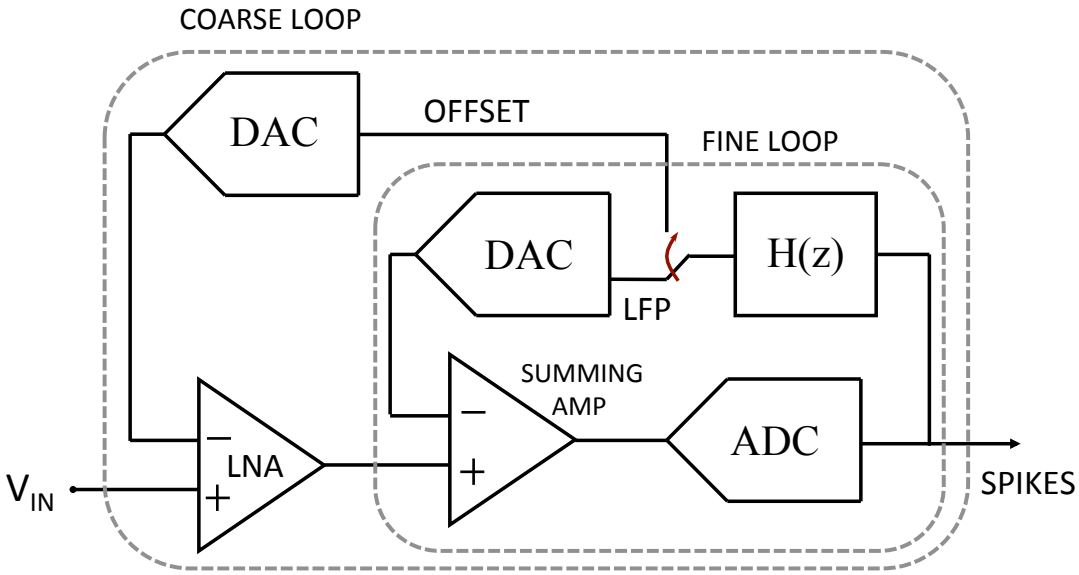


Figure 2-4: Split dual-loop architecture: coarse loop cancels offset, while fine loop cancels LFP with residual offset.

2.1.4 *Noise Folding*

Since the forward path is broadband compared to the signal bandwidth, sampling its output without an anti-aliasing filter before digitization would lead to out-of-band noise aliasing, reducing power efficiency. For example, a 1MHz overall forward path bandwidth sampled at 20kS/s would incur a 50x noise folding penalty. To prevent this penalty, and to avoid the added area of having an explicit analog filter for anti-aliasing, we chose to use a boxcar sampling ADC [EZE] running at the 20kS/s Nyquist rate.

2.2 Filter Design

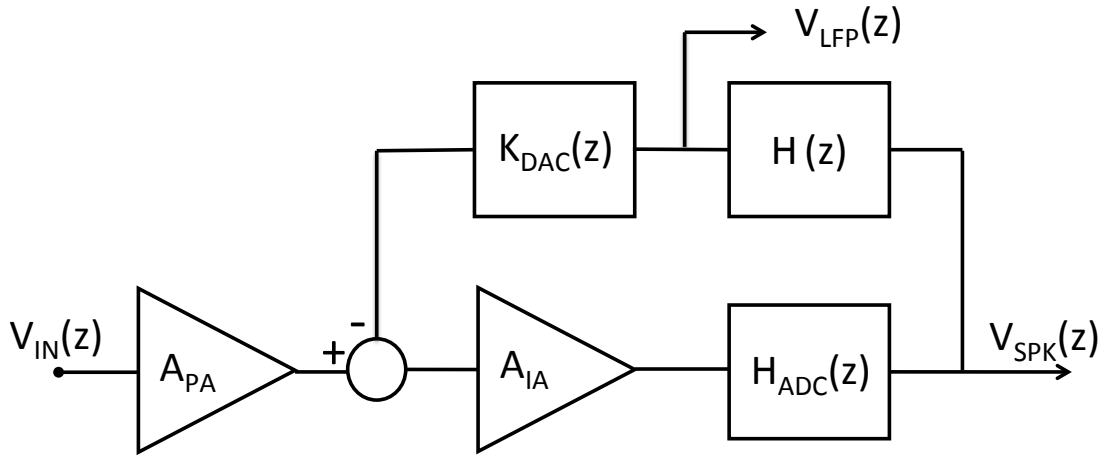


Figure 2-5: Feedback block diagram representation of neural signal acquisition chain.

A high-pass transfer function (G_{SPK}) is required in order to remove the LFP and residual offset from the spike output. The use of feedback introduces a tradeoff between the choice of loop filter and loop stability. With reference to the block-diagram in Figure 2-5, defining H(z) as the transfer function of the digital low-pass filter in the feedback path, the transfer function from the electrodes to the ADC output is

$$G_{SPK}(z) = \frac{V_{SPK}(z)}{V_{IN}(z)} = \frac{A_{PA}A_{IA}H_{ADC}(z)}{(1+A_{IA}H_{ADC}(z)K_{DAC}(z)H(z))}, \quad (2\text{-}1)$$

where A_{PA} is pre-amplification gain outside the feedback loop, A_{IA} is the instrumentation amplifier gain, $K_{DAC}(z)$ is the DAC gain and $H_{ADC}(z)$ is the transfer function of the ADC. Thus, the transfer function from the electrode to the low-pass filter output is simply

$$G_{LFP}(z) = \frac{V_{LFP}(z)}{V_{IN}(z)} = \frac{A_{PA}A_{IA}H_{ADC}(z)H(z)}{(1+A_{IA}H_{ADC}(z)K_{DAC}(z)H(z))}. \quad (2\text{-}2)$$

H(z) can be designed by starting with a closed-loop prototype $G_{SPK}(z)$. Assuming known A_{IA}, $K_{DAC}(z)$, and $H_{ADC}(z)$ (which can be obtained through calibration), one obtains:

$$H(z) = \frac{A_{PA}A_{IA}H_{ADC}(z)-G_{SPK}(z)}{A_{IA}H_{ADC}(z)K_{DAC}(z)G_{SPK}(z)} \quad (2\text{-}3)$$

If we assume for the sake of illustration that $K_{DAC}(z) = H_{ADC}(z) = A_{PA} = A_{IA} = 1$, any invertible prototype $G_{SPK}(z) = N_{SPK}(z)/D_{SPK}(z)$ can be realized by setting $H(z) = (D_{SPK}(z)-N_{SPK}(z))/N_{SPK}(z)$. In this case, if $G_{SPK}(z)$ = z-1/(0.99z-1) (first order high-pass with 200Hz lower cutoff), we find H(z)=.01z/(z-1) and $G_{LFP}(z)$=-.010z/(z-1.01). These transfer functions are shown in Figure 2-6.

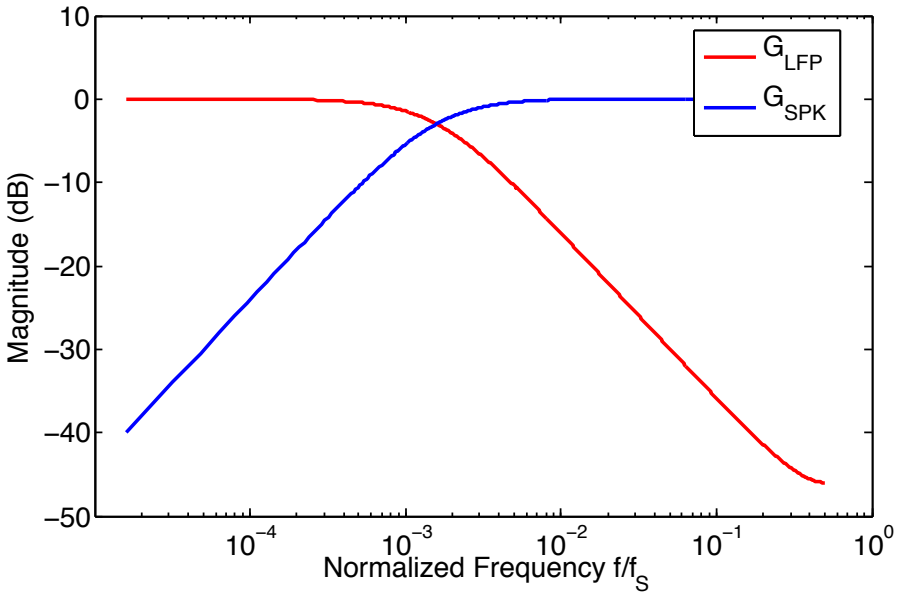


Figure 2-6: Example transfer functions for G_{SPK} and G_{LFP}

In practice the ADC and DAC typically introduce additional delays. For the more general case of $H_{ADC}(z) = z^{-N}$, $K_{DAC}(z) = z^{-M}$ we find

$$H(z) = \frac{z^N D_{SPK}(z) - z^{M+N} N_{SPK}(z)}{N_{SPK}(z)}. \quad (2\text{-}4)$$

This H(z) is causal for all open loop prototypes whose $\deg(D_{SPK}) = \deg(N_{SPK})+M$ where the M+N leading terms of $N_{SPK}(z)$ and $D_{SPK}(z)$ are equal. Furthermore, the roots of $N_{SPK}(z)$ are still required to lie within the unit circle to ensure stability. If the loop is closed on-chip, $K_{DAC}(z) = K_{ADC}(z) = z^{-1}$ can be achieved, and in this case it is relatively straightforward to find an H(z) that will result in the desired closed-loop transfer function.

For larger values of M and/or N it becomes increasingly difficult to find an open-loop prototype satisfying the above constraints. In this case, the feedback filter can be designed by guaranteeing that there is sufficient phase margin at the unity-gain frequency of the loop. If there is insufficient phase margin to design a second-order filter, a stable first order high-pass filter can be built using integrative feedback. The first-order closed-loop transfer function still provides dynamic range reduction in the spike path, and if additional filtering is needed, it can be provided outside the feedback loop in order to preserve stability.

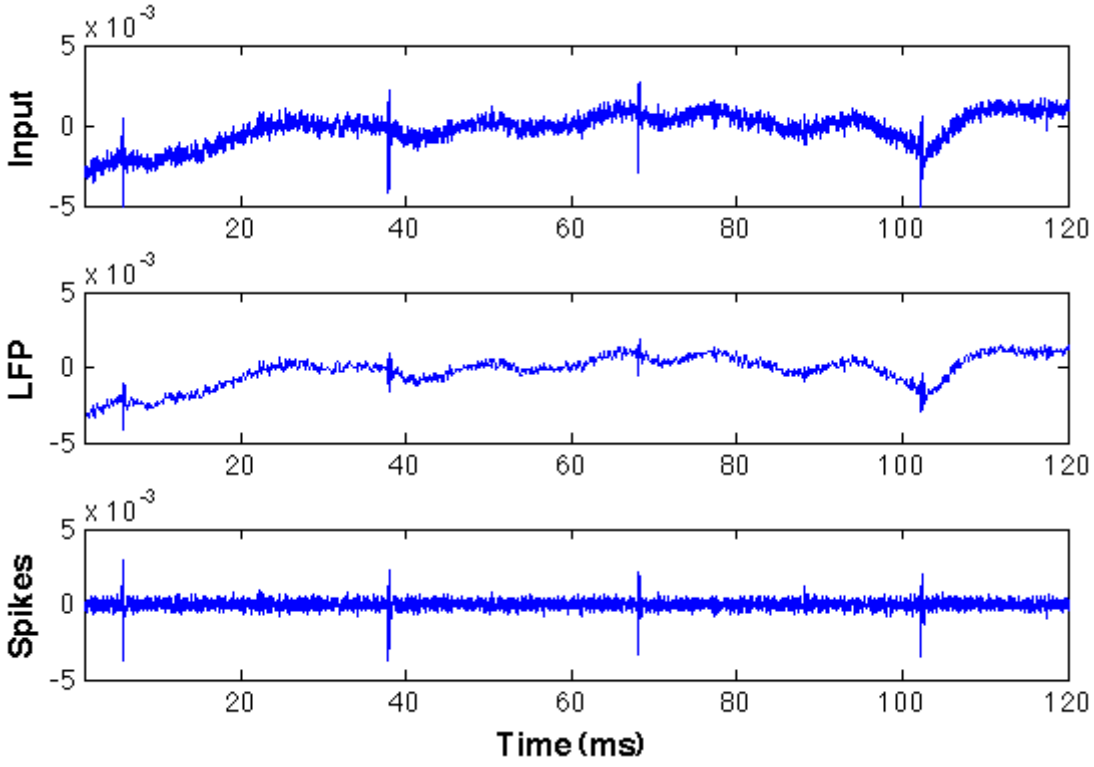


Figure 2-7: System behavioral simulation performed on pre-recorded signals from rat neocortex.

Behavioral simulations were performed of the mixed-signal closed-loop system, including digital filter. Appropriate quantization and gain levels were incorporated in the model. The results are shown in Figure 2-7. The simulation was performed on pre-recorded signals from a rat neocortex. With a pole placed at 500Hz, the results show clearly separated Action Potential (Spike) and LFP bands. The small spike that appear in the LFP are a result of a high pole frequency selection and a single-pole roll-off.

2.3 Circuit design

The neural implant environment is battery free, and as a result, the supply voltage for the implant becomes a design parameter that is chosen based on tradeoffs in the power-transfer, digital, and analog sections. Given the low clock speed and fine line process adopted, a low supply voltage is preferred for the digital section. For the power transfer section, reducing the required output V_{DD} reduces the number of rectification stages,

leading to overall lower area [ODR]. It is therefore highly desirable for the analog circuits to operate from a low supply as well.

Although designing low power, high dynamic-range circuits at low supply voltages is generally very challenging, these difficulties are mitigated in this context by two facts. First, since neural signals have a fixed low-amplitude input swing, amplifier swings can be reduced together with the supply. Because current consumption is determined by an absolute thermal noise specification, analog power consumption is reduced with decreased V_{DD}. Second, the proposed architecture employs global mixed-signal feedback to reduce the dynamic range of each individual gain stage, and enables the use of open-loop circuit techniques that scale more gracefully to a low-supply environment. Based on these considerations, we designed the acquisition chain to operate from a 0.5V supply. Despite the architectural optimizations, circuit-level techniques are still required to enable state-of-the-art performance and power consumption at low supply voltage. These techniques will be described in the remainder of this section.

2.3.1 *Low-noise offset cancellation*

A key challenge in the design of this DC coupled acquisition chain is to accommodate the large input offset without degrading common-rejection ratio or noise/power efficiency. In order to understand the tradeoffs between offset rejection, common mode rejection and noise performance, consider the simple differential amplifier of Figure 2-8. Input offset voltage (V_{IO}) coming from the electrodes changes the relative transconductance (Δg_m) and the relative drain current (ΔI_D) of the left and right halves of the circuit resulting in $\Delta g_m/g_m = \Delta I_D/I_D = V_{IO}g_m/I_D$. Assuming that all devices are matched and that the product $V_{IO}g_m/I_D$ is small, it can be shown that in the presence of input offset

$$CMRR = \frac{g_m}{\Delta g_m/(1+2g_mR_{tail})} = \frac{1+2g_mR_{tail}}{V_{IO}g_m/I_D}. \quad (2\text{-}5)$$

For low supply voltages the achievable g_mR_{tail} product is limited, and thus the product $V_{IO}g_m/I_D$ must be minimized. This optimization would lead to a design which must use a small amplifier g_m/I_D and would hence degrade the amplifier's noise/power tradeoff. The tight constraints on input-referred noise and leakage current flowing toward the electrode prevents the use of offset cancellation at the input of the instrumentation through a G_m-based servo loop. Canceling the offset at the output of the amplifier as shown in Figure 2-9(a) does not solve this problem. Under these conditions the transconducting stage still processes both signal and offset, and additional noise is introduced by the offset suppression circuitry. It is therefore highly desirable to find an alternative means of offset cancellation.

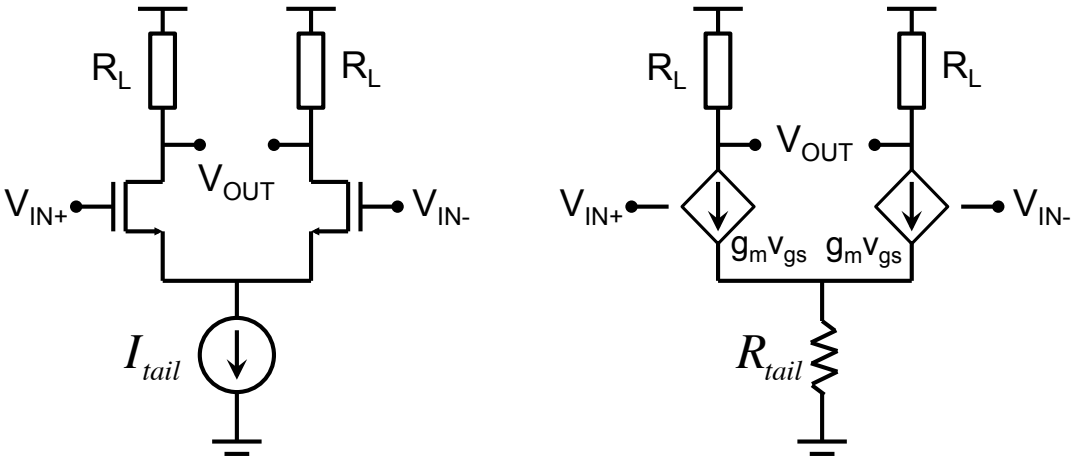


Figure 2-8: Resistively loaded differential pair (left) and corresponding small-signal model (right).

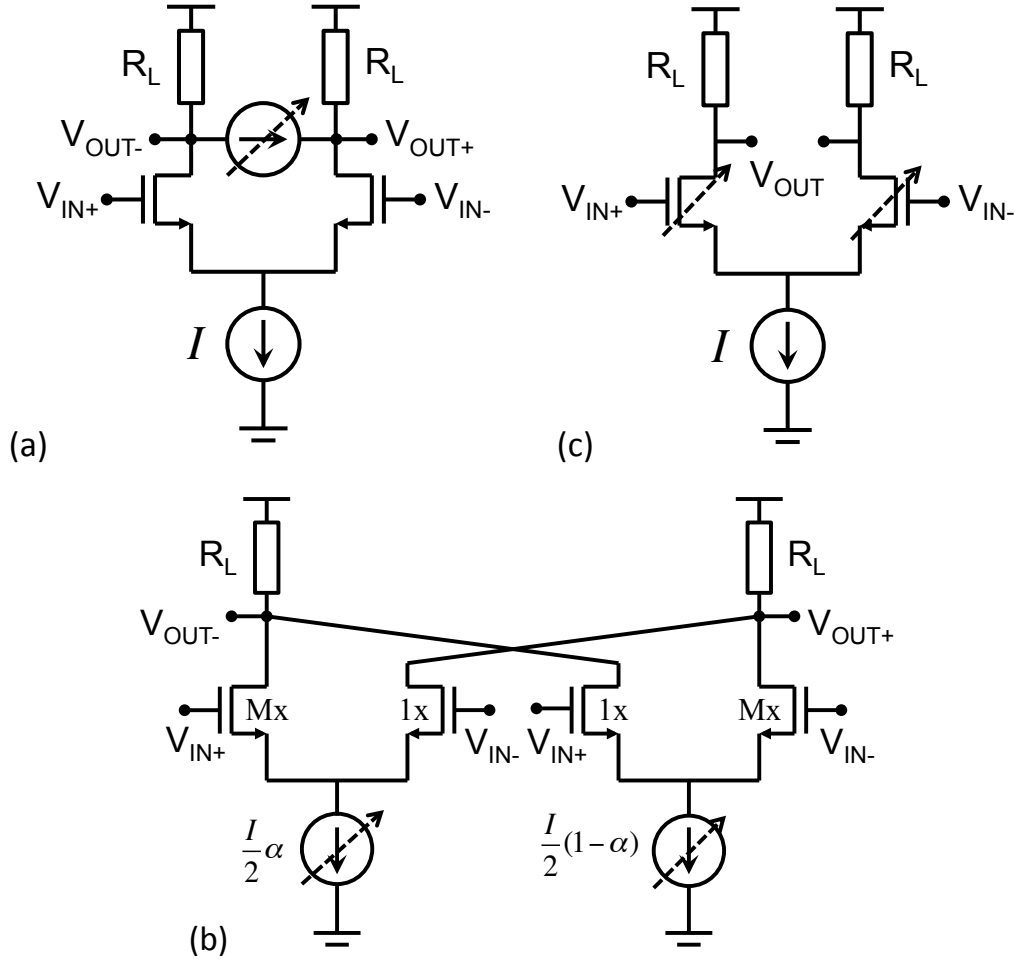


Figure 2-9: (a-c) DACs used for offset cancellation

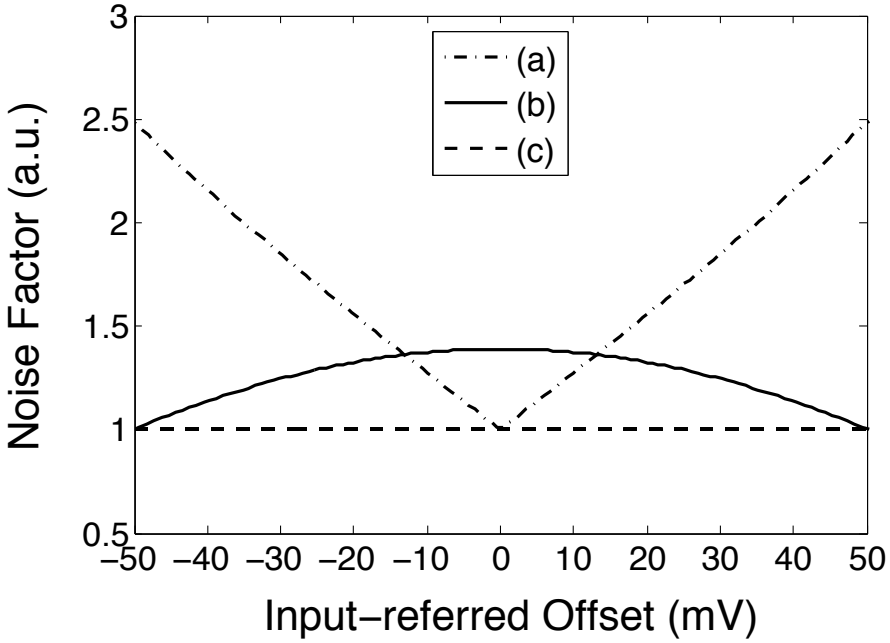


Figure 2-10: A comparison of noise factor vs. input-referred offset for the DACs shown in Figure 2-9.

In order to arrive at such a solution, consider the offset cancellation scheme originally introduced in [CAS] and shown in Figure 2-9(b). In this design the offset is cancelled by varying the tail current ratios between two asymmetrically sized differential pairs. In utilizing this topology, we incur a noise penalty associated with offset cancellation from the tail current devices whose noise current travels in asymmetric paths to the output, increasing the total noise.

Figure 2-9(c) shows an alternative solution based on a single-differential pair with transistors of programmable widths biased in sub-threshold. This amplifier has an input-referred offset of

$$V_{off,in} = n\frac{kT}{q} ln\left(\frac{W_{M1}}{W_{M2}}\right) \tag{2-1}$$

where kT/q is the thermal voltage, $n = 1+C_{dep}/C_{ox}$ is the subthreshold slope multiplier, and W_{M1} and W_{M2} are the widths of the input devices M_1 and M_2. A feedback loop can then change the relative size of the two transistors comprising the differential pair until the offset introduced by the asymmetry is equal and opposite to the electrode offset. At this point, the tail current and its associated noise current is split equally between transistors M_1 and M_2, $I_{D1} = I_{D2} = I_{tail}/2$, and because of sub-threshold operation, $g_{m1} = g_{m2} = I_{tail}q/(2nkT)$. In order to verify the improved noise performance of the proposed offset

cancellation scheme, the input referred noise density of the three offset cancellation solutions in Figure 2-9 are compared in Figure 2-9(d). To first order, the solution of Figure 2-9(c) cancels the input offset without any penalty in thermal noise or common mode rejection, and was hence adopted in this work. We now proceed to analyze the design in detail for this solution, which we will refer to as a merged amplifier-DAC.

2.3.2 *Transfer characteristic linearization*

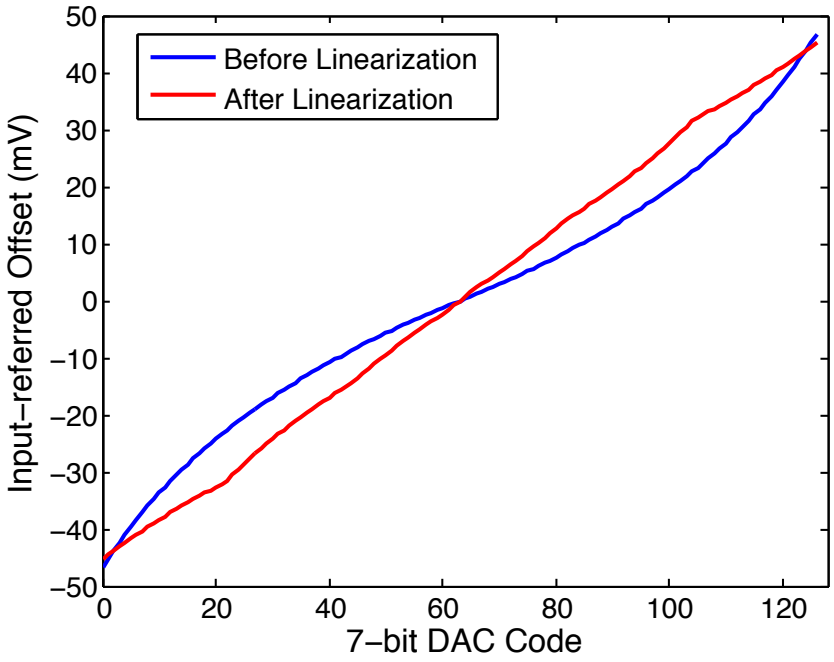


Figure 2-11: Offset DAC Transfer Function

To cancel ±50mV of input-referred offset, a W_{M1}/W_{M2} ratio of 4 is required. A linear transfer function of input-referred offset vs. DAC code results in a 7-bit DAC requirement to cancel the offset down to sub-1mV levels. However, if the DAC is thermometer coded, the transfer function is defined by Eq. 6 and is thus nonlinear. If W_{M1}/W_{M2} increase linearly, the input-referred offset will change with a steeper slope at the center codes than it will towards the edges the transfer curve, requiring higher DAC resolution for a given LSB size. To decrease the resolution requirement a non-linear coding scheme is employed. Ideal linearization can be achieved by coding the elements with exponentially increasing size. Since this sizing would result in an impractical layout, the elements were instead coded with increasing unit size in groups. Such an implementation results in a linearized transfer function with built-in DNL, which was

designed to be less than 0.25LSB, corresponding to a maximum input-referred offset of 1mV and reduced the resulting resolution by 1 bit. The transfer curve from DAC code to input-referred offset is shown in Figure 2-11.

Since nonlinear coding lead to a transfer curve that is not perfectly linear even without mismatch, there is some DNL built into the DAC by design. The sizing of the unit elements was designed such that the built-in DNL was well below 0.5LSB. Figure 2-12 shows the simulated DNL across 100 monte-carlo trials for mismatch. The lower plot shows the built-in DNL plus 3 sigma of random mismatch DNL. The worst-case simulated performance results in 0.8LSB of DNL. A 7-bit DAC cancelling a 100mV range of offset results in an LSB size of 0.78mV, therefore the worst-case input-referred offset should be 1.4mV. Subsequent stages will be designed to handle this residual offset.

The transfer characteristic exhibits linear temperature dependence; however, since the power consumption of an implanted IC must be very low and since the human body is a relatively temperature stable environment, even if a 5^{o} change were observed, then $\Delta T/T$ = 5K/310K, resulting in only a 1.6% change in LSB size of the DAC. The unit-element sized transfer function and the resulting linearized transfer function are plotted together in Figure 2-11. The breakpoints of the nonlinear groupings are clearly visible in the figure where the DNL systematically changes. To extend the offset cancellation range beyond ±50mV a larger ratio of W_{M1}/W_{M2} may be employed.

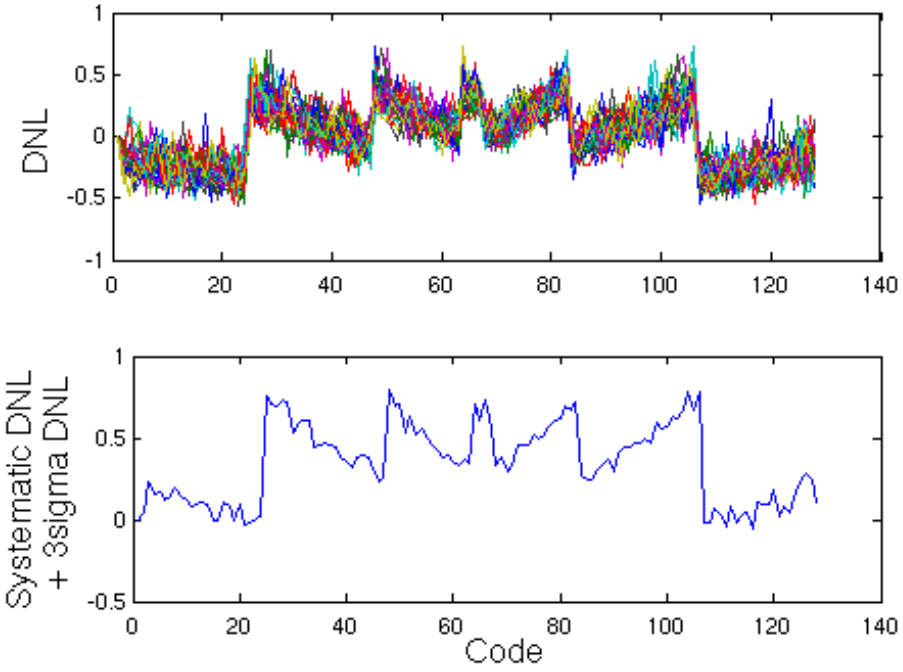


Figure 2-12: Mismatch simulation of DNL in the offset-cancellation DAC.

2.3.3 *Residual CMRR*

The first order analysis presented above assumes that the electrodes contribute the entire input-referred offset of the system. In reality, the devices comprising the amplifier also contribute offset. Threshold voltage mismatch from the differential pair devices, typically much smaller than the electrode offset, appears in series with the electrode offset and is therefore cancelled by the feedback DAC. However, load resistor mismatch cannot be neglected. For a relative load resistor mismatch $\Delta R/R$, nulling the total input-referred offset requires differential pair currents to be imbalanced an amount $\Delta I/I = -\Delta R/R$ leading to an increase in Δg_m. Even in the absence of random mismatch, the device subthreshold slope factor n also depends on bias point [TSI], leading to an additional increase in Δg_m of the input devices after offset cancellation. The variation of n can be decreased by decreasing the inversion coefficient (by increasing W/L) of these devices at the cost of increased area and gate leakage. Lastly, since offset cancellation is performed with finite resolution, there is a residual input referred offset due to the minimum quantization step V_{LSB}. The CMRR expression from Eq. 5 including all these effects becomes

$$CMRR = \frac{1+2g_m R_{tail}}{\frac{\Delta R}{R}+\frac{\Delta n}{n}+\frac{V_{LSB} g_m}{I_D}}. \quad (2\text{-}2)$$

While the first and third terms of the denominator are random in nature, the $|\Delta n/n|$ term is deterministic and increases with offset value. CMRR is therefore maximum at V_{IO}~0 and progressively degrades as larger values of offset are canceled.

2.3.4 *Offset-dependent 1/f noise*

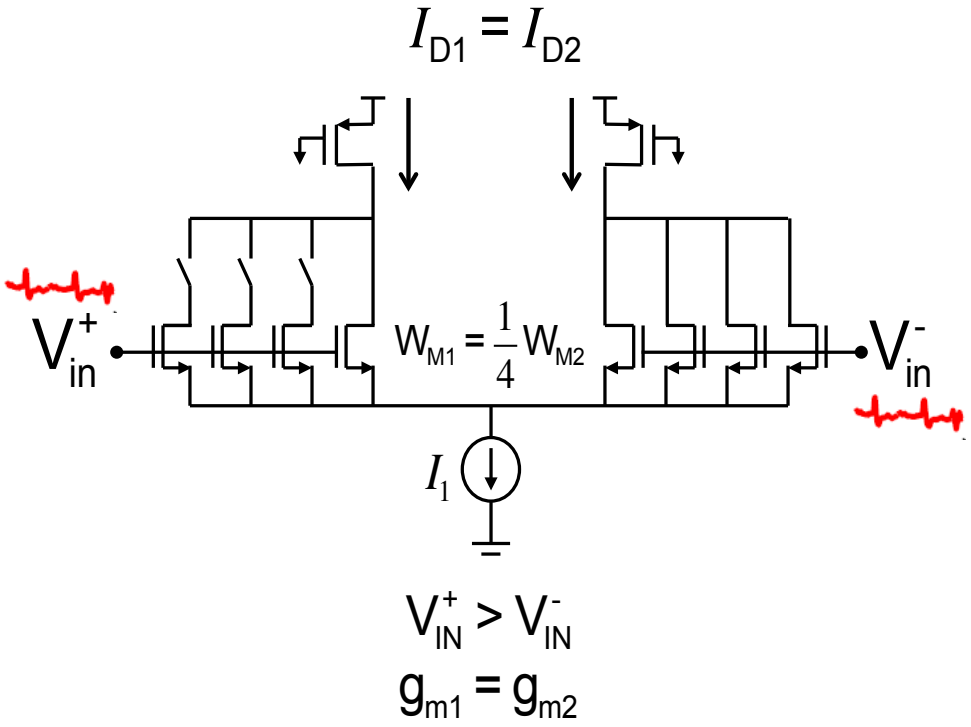


Figure 2-13: Operation of the offset cancellation amplifier-DAC in the presence of a large positive input offset.

While the chosen amplifier-DAC topology achieves offset-independent thermal noise, the 1/f noise corner is modulated as the effective device width and inversion level of the input pair is changed. Consider the merged amplifier-DAC circuit of Figure 2-13 in the presence of a positive offset voltage V_{IO} and in the absence of any resistor mismatch. After offset cancellation, we have $NW_{M1} = W_{M2}$ where $N = \exp[|V_{IO}|/(nkT/q)]$. If we call i_{n1}, and i_{n2} the noise generators associated with M_1 and M_2 respectively, then the differential noise current power spectral density can be calculated to be $i_{no} = i_{n1}+i_{n2}$. Since the flicker noise corner of M_1 is N times larger than that of M_2, the flicker noise corner of i_{no} becomes (N+1)/2 times larger than that associated with M_1 alone. Expressing the trade-off in terms of V_{IO}, we find that the 1/f noise corner frequency (f_k) becomes

$$f_k = \frac{f_{k0}}{2}\left(1 + \exp\left(\frac{|V_{IO}|}{nkT/q}\right)\right), \tag{2-3}$$

where f_{k0} is the flicker noise corner at zero input offset. For a maximum offset of 50mV, the 1/f corner frequency of the input devices is increased by 2.5 times. This increase was accounted for in this design by correspondingly over-designing the device size and the increase in input capacitance was found to have no effect at the frequencies of interest.

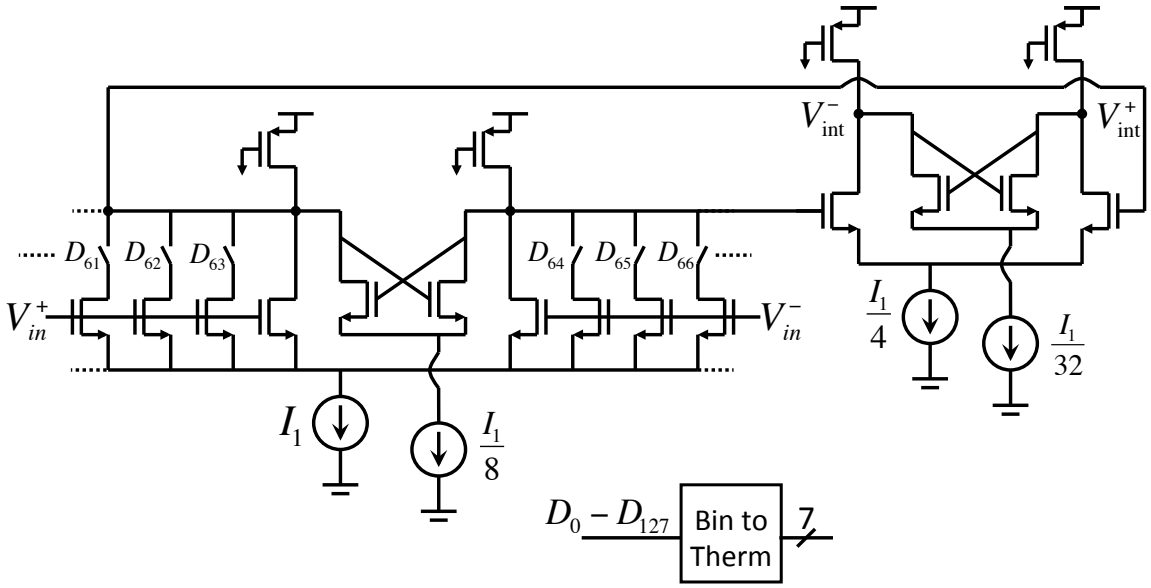


Figure 2-14: Complete circuit implementation of merged amplifier-DAC.

The circuit schematic of the designed merged DAC-amplifier is shown in Figure 2-14. A two-stage open loop topology is used to achieve power-efficient gain at low supply voltage. A bias current of 6.4μA is used in the first stage to meet the thermal noise specification. Input device channel length is set to 0.25μm for improved output resistance, while the total widths of the input devices are set to 336um to keep the |Δn/n| factor below 5%. The second stage is scaled to ¼ the power dissipation of the first stage to save power since noise constraints are relaxed. Both stages employ weak cross-coupled pairs to boost the gain [CHAT] of each stage to 16dB to give a total LNA gain of 32dB. The total noise spectral density of the amplifier-DAC referred to the electrodes at an input offset $V_{IO} = 0$, is 48nVrms/√Hz, with a 6kHz 1/f corner.

2.3.5 *Summing amplifier and DAC*

A complete schematic of the second summing amplifier is shown in Figure 2-15(a). This stage subtracts the feedback signal from the output of the first stage, which contains an amplified version of the spikes, LFPs and residual offset. Because of the preceding 30dB of gain, linearity in this stage is a more pressing concern than noise. A differential amplifier with a differentially connected degeneration resistor and triode transistor loads realizes the amplification stage. Feedback signal subtraction is performed at the output of the amplifier in the current domain by a current-steering DAC. This 9-bit DAC is realized as a 100x oversampled ($f_{ck} = 100f_s = 2$MHz, where f_s is the ADC sample clock frequency), 4-bit structure with first order Delta-Sigma encoding. A thermometer coding

scheme and unit element sizing are used to achieve 9-bit linearity. While using 4 physical bits results in an area penalty compared to a 1-bit implementation, it reduces the input voltage range to the ADC without having to implement an explicit low-pass filter in the analog domain.

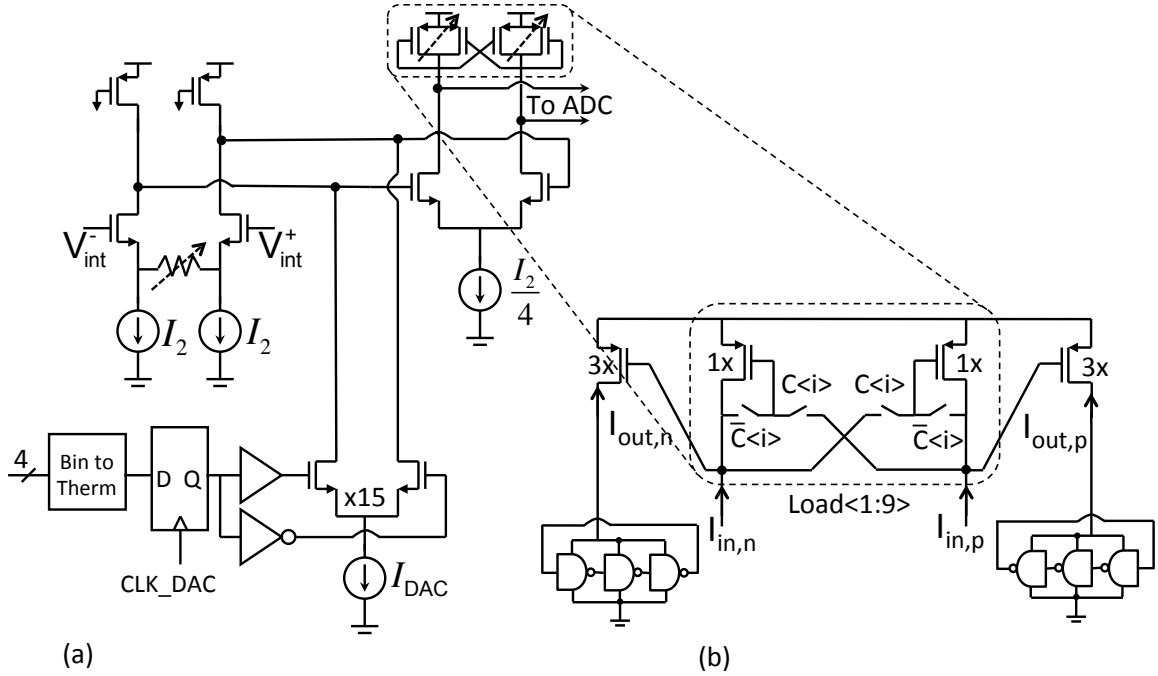


Figure 2-15: (a) Circuit diagram of current-feedback DAC and amplifier. (b) ADC driver current mirror with adjustable gain.

The system employs a current-driven, ring oscillator based ADC [HOV] [XIA1] whose linearity requirements are relaxed since it handles only the signal after LFP subtraction. The driver consists of a differential-pair V-I converter cascaded with a current-mode programmable gain block (Figure 2-15(b)). The V/I converter load is comprised of nine pairs of unit PMOS devices that can be individually connected either as cross-coupled pairs or as diode-connected devices. When N devices are cross-coupled, the differential mode load impedance seen by the V/I converter equals $1/(9\text{-}N)/g_{mp}$ (N<5 to maintain stability). The outputs of this block are connected to the gates of 3 matched unit PMOS devices. Changing N can therefore program the differential mode current gain without changing the power dissipation, enabling ease of compensation for varying input amplitudes, which are associated with the distance between the neuron and electrode.

The total noise spectral density of the summing amplifier and the ADC driver, referred to the electrodes, is 5nVrms/√Hz, with a 5kHz 1/f corner at a bias current of 1.25μA (800nA summing amplifier, 200nA ADC driver, 250nA feedback DAC).

2.3.6 *Analog-to-digital converter*

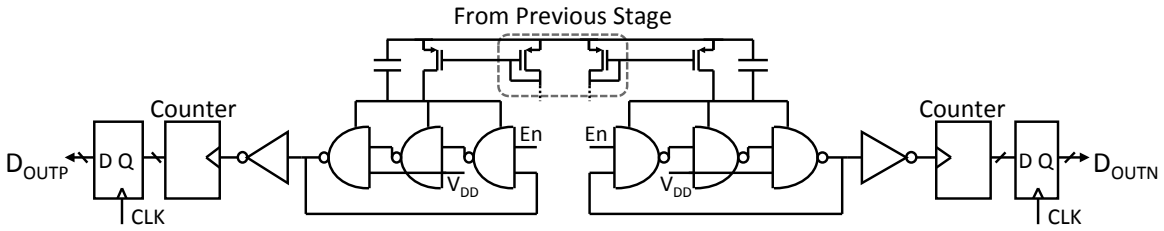


Figure 2-16: Circuit diagram of ring-oscillator based ADC.

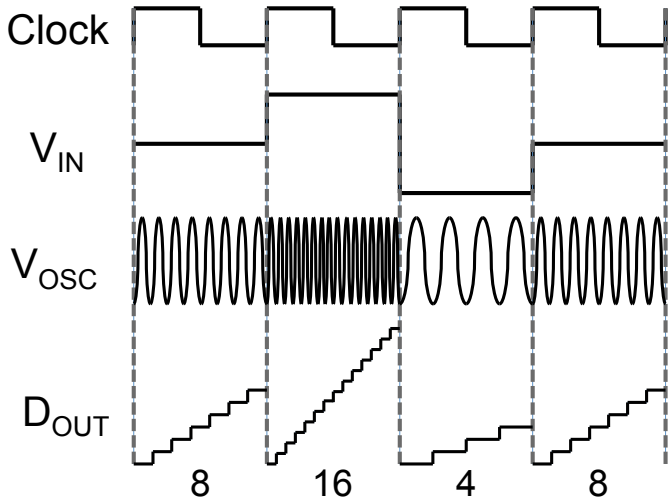


Figure 2-17: Ring-oscillator based ADC operation

In order to keep the quantization noise well below the thermal noise floor an ADC resolution of at least 8 bits is required. The ADC employs a pseudo-differential, VCO-based architecture shown in Figure 2-16. The positive and negative driver output currents are used as the bias for two single-ended, three-stage CMOS ring oscillators realized with NAND gates, which feed the clock inputs of 9-bit digital counters. The basic operation is illustrated in Figure 2-17 where an input voltage V_{IN} is used to modulate the oscillation frequency of a ring-oscillator. The number of cycles in a clock period are then quantized by a digital counter. In this implementation the counters are not reset but allowed to wrap causing first-order noise shaping of the quantization noise as described in [STR].

Power and area are minimized by the use of simple CMOS rings while supply and common-mode disturbances are suppressed by the differential operation of the circuit.

Driving the ADC in the current-domain through a PMOS current mirror further improves PSRR and soft-rail operation maintains good linearity through the full dynamic range [WIS]. While extra resolution can be obtained by sampling all of the oscillator phases [STR], the intrinsic speed of the 65nm CMOS technology used is such that the desired 8-bit, 20kS/s is easily achieved with a single-phase measurement. Each oscillator is designed such that the minimum and maximum oscillation frequencies f_{min} and f_{max} satisfy $|f_{max}-f_{min}| > 2^8 f_s$ with f_s = 20kHz, therefore each differential output results in an 8-bit dynamic range for a total of 9-bits of quantization.

The counter output represents the average oscillator frequency over a period, corresponding to integration in the time domain and a sinc transfer function in the frequency domain. Thus the converter provides the desired boxcar sampling response, preventing aliasing of the wideband noise from the instrumentation amplifier. Sinc filters have been used as anti-aliasing filters in this context [BOH] but with large-area analog implementation; this work merges this anti-aliasing filter into the ADC in a compact form factor. The box-car sampling characteristic introduces a second key benefit in this system, as it suppresses the shaped quantization noise from the Delta-Sigma (ΔΣ) DAC employed for LFP cancellation. Because of the harmonic relation between the ΔΣ clock and the ADC clock, and the integrating nature of the ADC, the transfer between quantization noise and ADC output $NTF_Q(z)$ expressed in the 2MHz clock domain is given by the modulator NTF cascaded with that of a 100 tap moving average (MA) filter. For a ΔΣ noise transfer function of $NTF(z) = 1-z^{-1}$, and

$$NTF_Q(z) = NTF(z)MA(z) = \frac{1-z^{-100}}{100}. \quad (2\text{-}4)$$

Essentially, the integrating characteristic of the ADC averages the DAC output bit-stream while performing the conversion, acting as first stage of decimation. As a result, the high-frequency quantization noise from the ΔΣ modulator is greatly attenuated at the output port and does not degrade the overall system SNR.

2.4 Measurement Results

The chip was fabricated in a 65nm 1P7M LP CMOS process from ST Microelectronics. A chip microphotograph is shown in Figure 2-18. The chip contained two channels and one stand-alone ADC test block. The inset shows the detailed layout of a single channel. The total chip area is pad-limited to 1.2mm x 1.2mm, while the core channel area is 80μm x 170μm. The chip power consumption was measured to be 5.04μW. Electrical characterization of the chip was performed by housing the die in a 48-pin 7mm x 7mm metal lead frame package connected a PCB through a test socket. The digital filters,

which form the feedback path for LFP separation, were implemented off-chip on an FPGA. Figure 2-19 shows a complete diagram of the implementation and Table 2-1 shows the area and power breakdown by block. The total area of the channel includes the 0.0017mm^2 required to synthesize the off-chip digital filters. All measurements were performed through the full acquisition channel including the on-chip ADC. Post-processing of the digital outputs was performed using MATLAB. Differential sine wave inputs were produced using a Stanford Research Systems DS360 low-distortion signal generator and attenuated to proper input levels at the acquisition channel input.

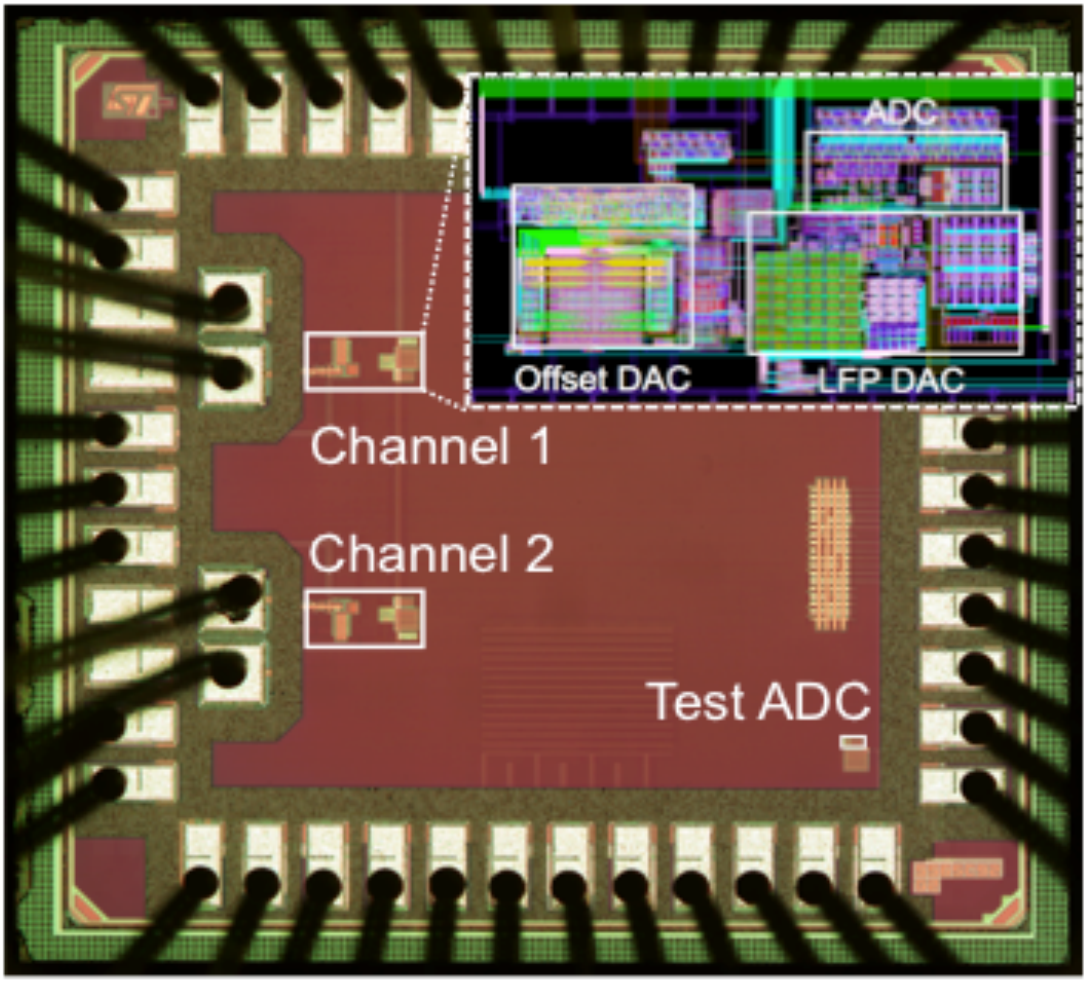


Figure 2-18: Action Potential Front-end Chip Microphotograph and Layout (inset).

The measured closed-loop transfer functions of the IC from the input to the spike and LFP outputs are shown in Figure 2-20. The transfer function of the spike band shows a 300Hz high-pass cut-off, set by the digitally programmable feedback loop. The full-scale voltage of the spike transfer function is programmable between 870μV and 3.5mV. The high-frequency roll-off is due to the sinc transfer function of the ADC. This droop is

deterministic and can be compensated for in DSP if needed. The loop filter order was limited to be first-order by the latency introduced by implementing the filters off-chip. Further filtering the two signals outside the feedback loop will enhance signal band isolation. If the digital signal processing were integrated on-chip, higher filter order could also be implemented inside the feedback loop.

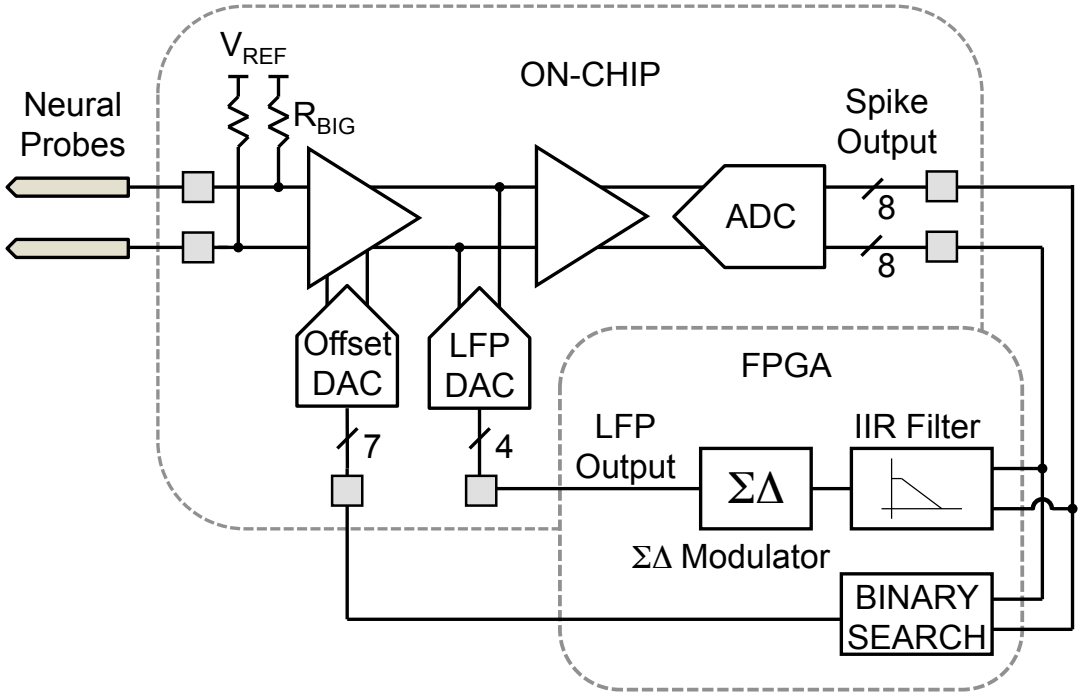


Figure 2-19: Implemented system diagram.

Table 2-1: Power and area breakdown by block.

	Power	**Area**
Merged Amplifier-DAC	4.13μW	0.0037mm^2
Summing Amplifier & DAC	0.66μW	0.0045mm^2
ADC	0.24μW	0.0018mm^2
Digital Filters	0.1μW*	0.0017mm^2

*estimated

The measured input-referred noise is shown in Figure 2-21 over the same bandwidth. The measured integrated noise in the spike band is 4.9μVrms in a 10kHz bandwidth, while the LFP band has a noise floor of 4.3μVrms in a 300Hz bandwidth. At low frequency, both neural signals and transistors exhibit a 1/f power spectrum; therefore the

low-frequency LFP band can absorb larger noise spectral density while maintaining SNR [VEN]. ΔΣ quantization noise was not observed and is therefore suppressed below thermal noise levels.

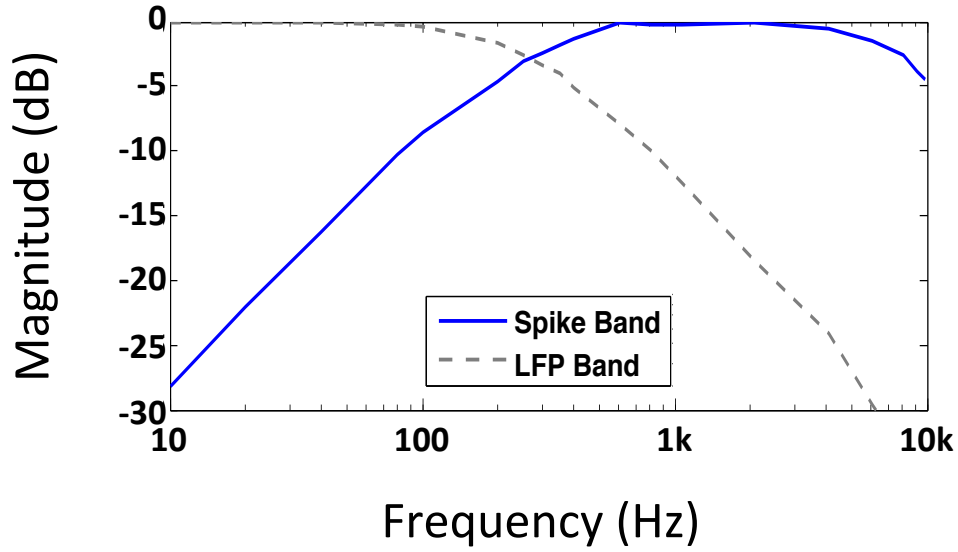


Figure 2-20: Normalized magnitude plot of closed-loop system.

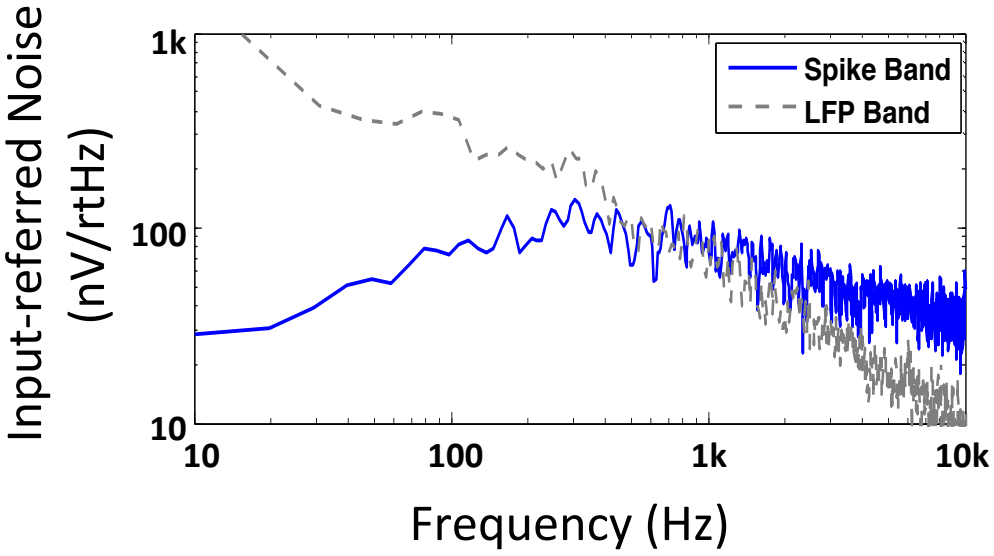


Figure 2-21: Input-referred noise spectral density in Spike and LFP bands.

Figure 2-22 shows the measured performance of the offset-cancellation amplifier-DAC. The top shows the measured transfer curve between digital code and input-referred offset. This curve closely matches that predicted by Eq. 6. DNL is plotted at the bottom of

Figure 2-22. Since the maximum measured DNL and LSB sizes are 0.55LSB and 0.8mV respectively, the maximum input referred offset after the first stage of cancellation is 1.2mV. Excess DNL was observed at the lower extreme of offset cancellation and was found to be systematic across multiple chips due to asymmetry in the layout.

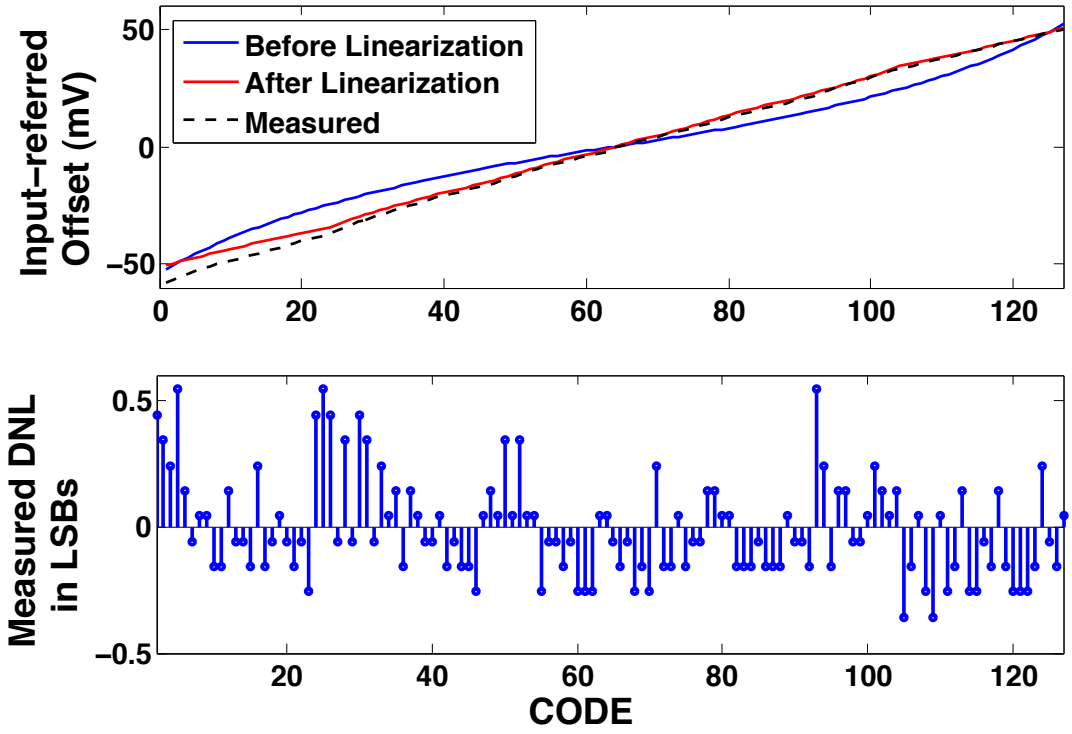


Figure 2-22: Merged amplifier-DAC transfer curve (top) and DNL (bottom).

Figure 2-23 shows the measured and simulated CMRR (top) and PSRR (center). Input-referred noise (bottom) is plotted together with calculated values. Each is plotted as a function of the initial input offset after rebalancing the amplifier. Values remain above 50dB for both CMRR and PSRR for all values of offset. Peak PSRR is shifted from the center due to sensitivity to mismatch in the second stage of amplification, while the input differential pair dominates CMRR. The noise is measured through the on-chip ADC and therefore includes quantization noise. Input-referred noise stays below 6μVrms for all conditions and below 5μVrms for ±20mV of offset. Acute in-vivo measurements showed that offsets were rarely above 20mV, although long-term studies have yet to be done. Note that since the simulated g_mR_{tail} product for this amplifier is only 26dB, a solution employing output offset cancellation would require an impractical $g_m/I_D = 1.6$ to achieve the same worst-case CMRR.

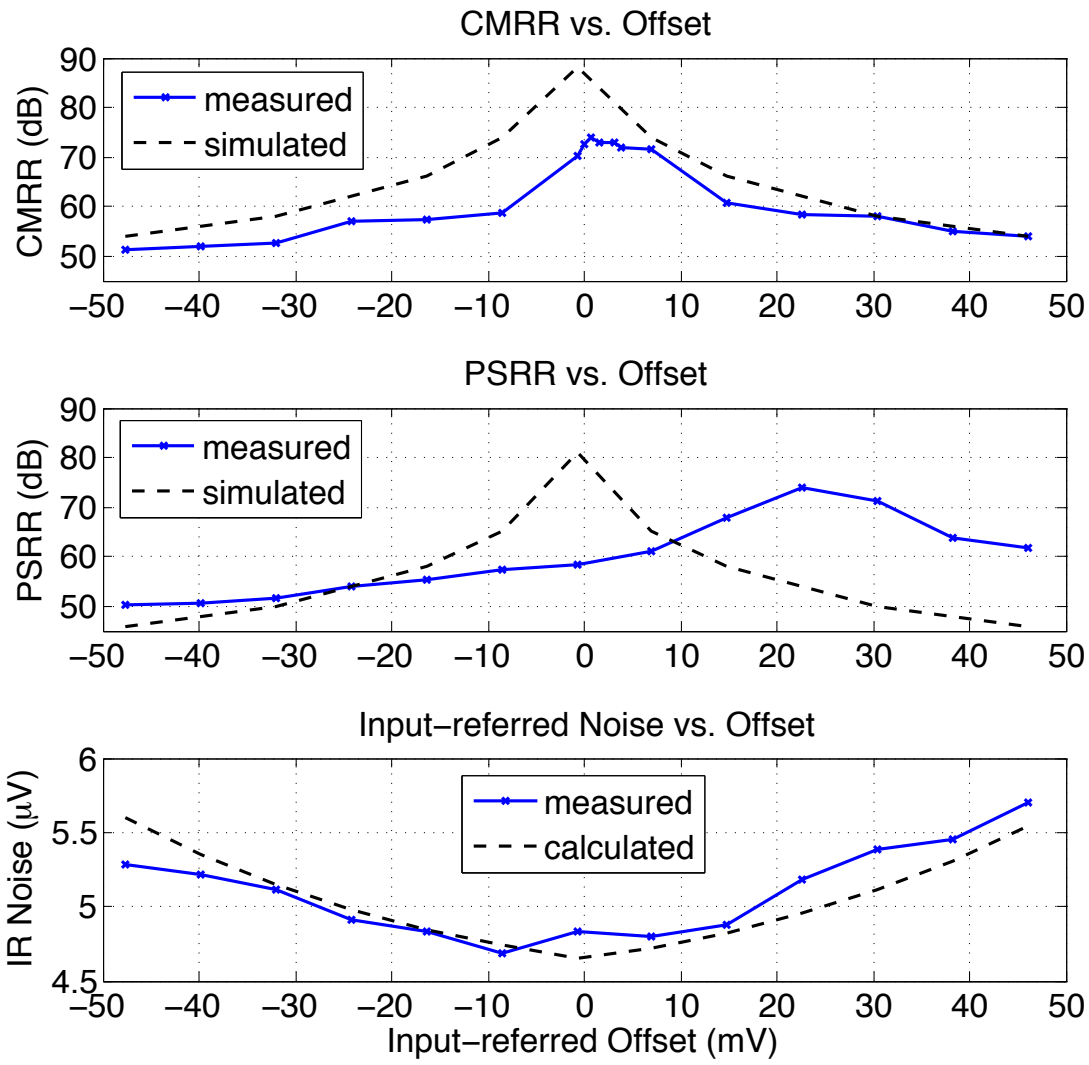


Figure 2-23: CMRR (top), PSRR (center) and Input-referred integrated noise (bottom) vs. input-referred offset.

Figure 2-24 shows the measured output spectrum of the acquisition system for a 2kHz, 200μVrms input sine wave. 2% total harmonic distortion (THD) is observed for the entire channel at the maximum system gain. Figure 2-25 shows the measured output spectrum of the stand-alone ADC test structure with a 1kHz sinusoidal input. The spectrum shows an SNDR of 45dB and an SFDR of 58dB, a linearity that is sufficient for 9-bit operation. The converter consumes 240nW, which corresponds to a figure of merit of 84fJ per conversion step. First order quantization noise shaping is observed.

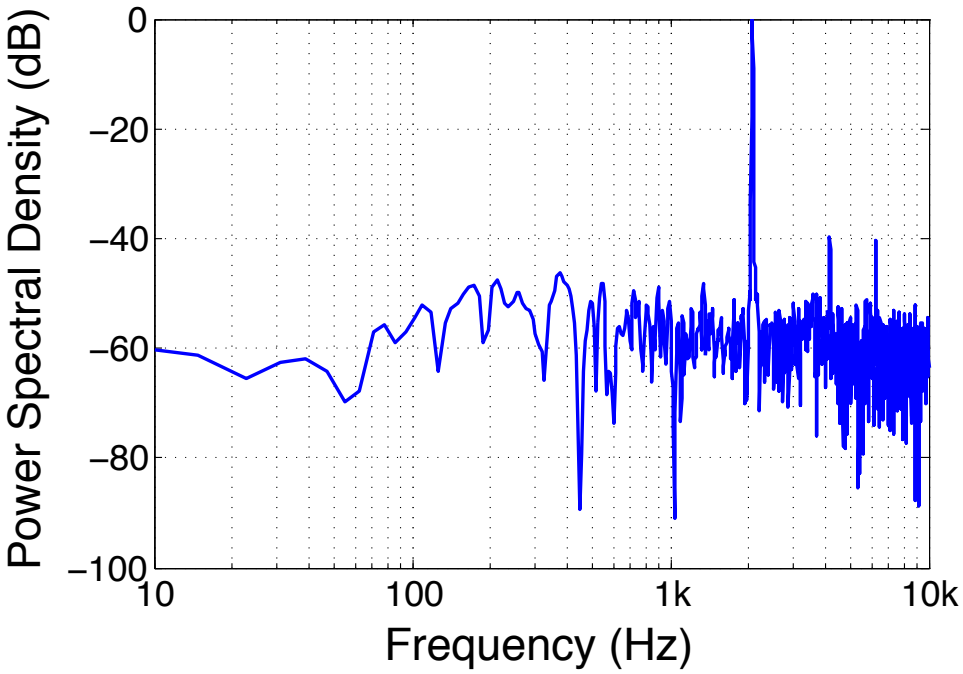


Figure 2-24: Power spectral density of system with a 200μVrms, 2kHz sine wave input.

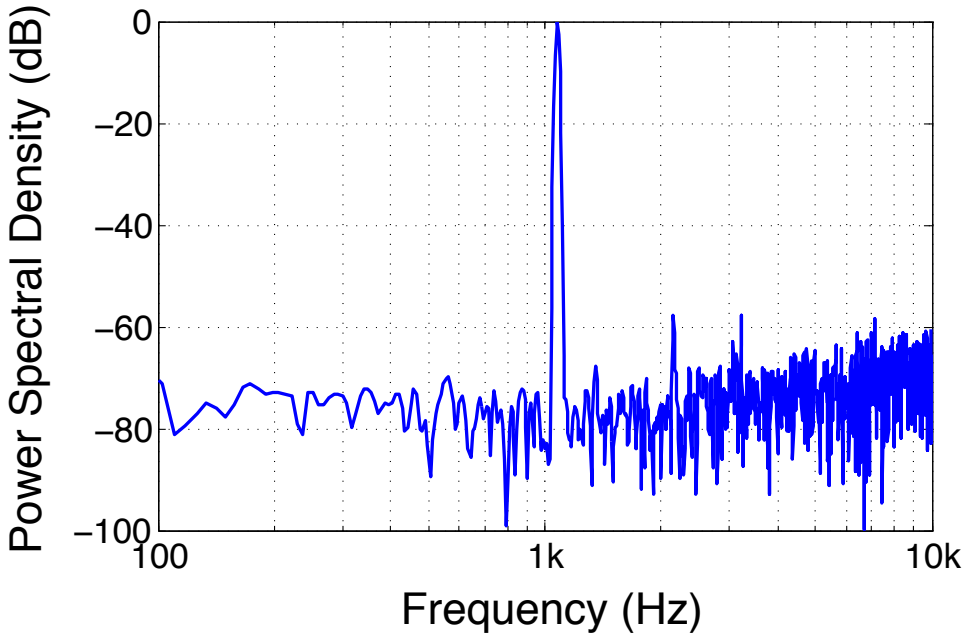


Figure 2-25: Power spectral density of ADC with 1kHz sine wave input at full scale.

2.4.1 *In-vivo Measurements*

The system was further verified through in-vivo measurement. The inputs of the chip were connected to a microelectrode array implanted near the motor cortex of a live, awake, free-moving rodent two months prior to recording. Figure 2-26 shows a detailed photo the rat, with two 16-channel Platinum-Iridium microwire arrays from Plexon held in place with dental cement. One array is implanted in the motor cortex while the other is in the striatum. The implant locations were determined for a separate behavioral experiment and only the implant in the motor cortex was used for this work.

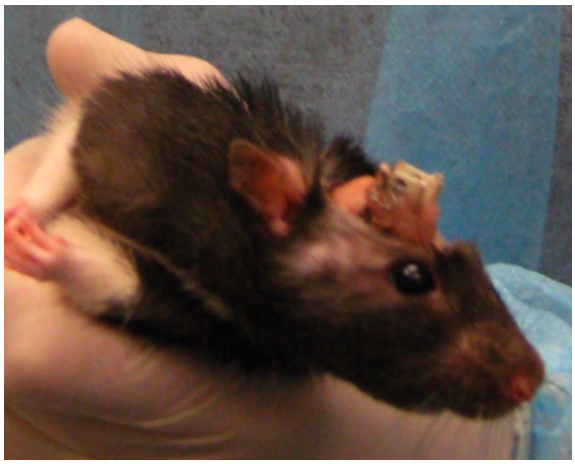


Figure 2-26: Photo of rat electrode implants

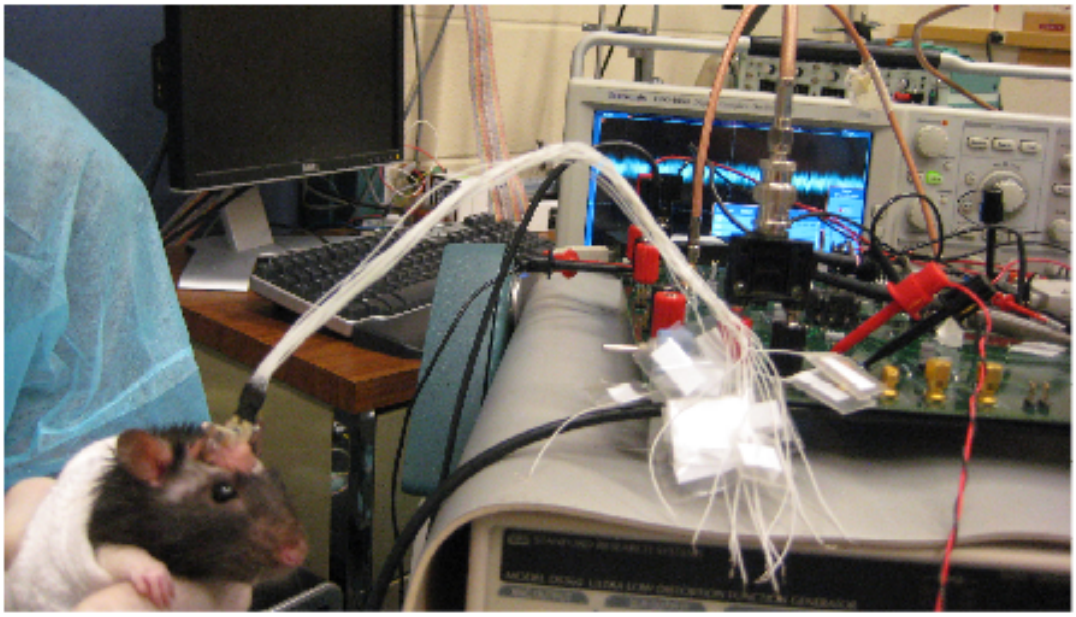


Figure 2-27: In-vivo recording test setup

Figure 2-27 shows the in-vivo recording setup. The electronic test board was connected through a custom wire connector to the implanted microarray. Due to their length, he wires were wound together as a twisted pair to mitigate 60Hz noise and the recordings were taken fully differential. All inactive electrodes and the body of the rat were tied to a low-impedance reference voltage. No other precautions were taken for 60Hz noise mitigation; there was no observable need for shielding or for the use of a Faraday cage. Figure 2-28 shows the recorded waveform from one of the trials. The measurements show good quality recordings and indicate that DC coupling the chip to the electrode array does not have significant impact on signal integrity. The finite leakage between LFP and spike band is due to the first-order roll-off of the loop filter.

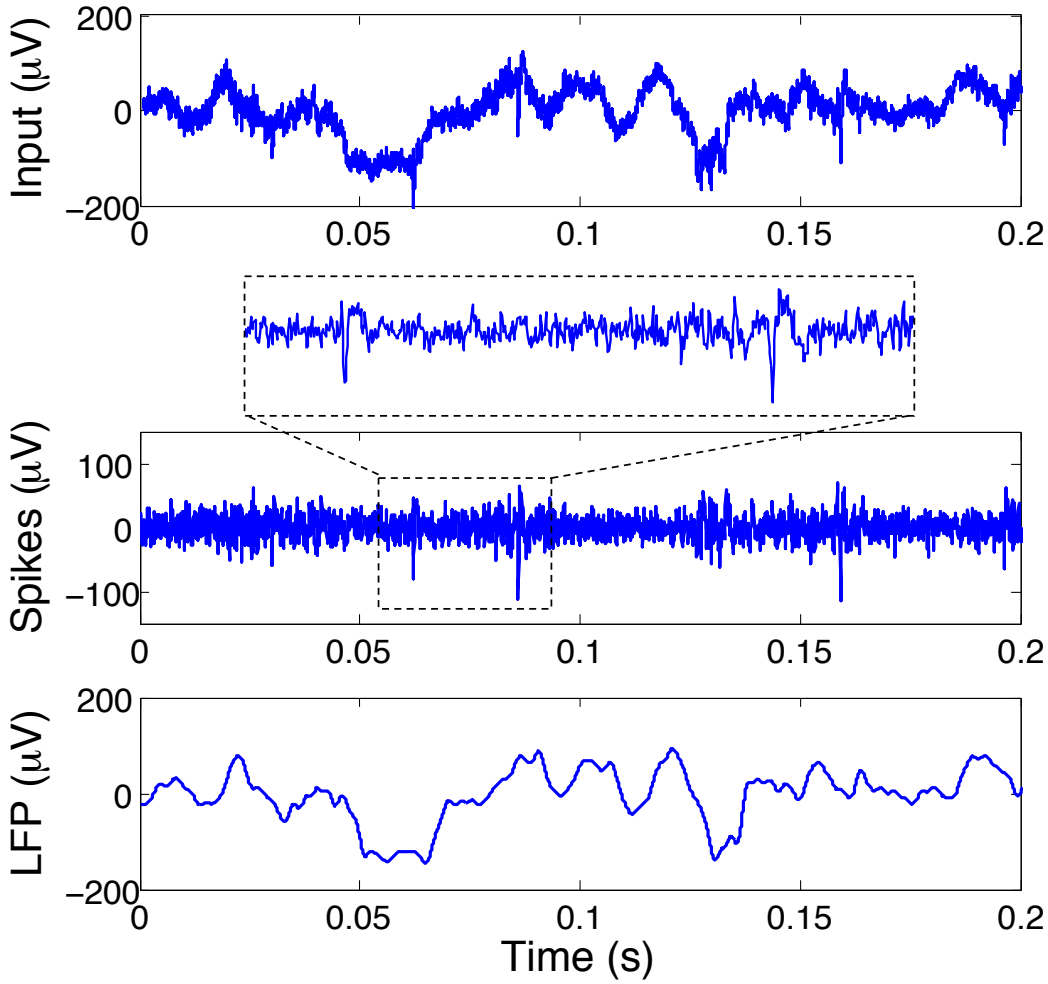


Figure 2-28: In-vivo recordings from live rodent, input waveform (top), Spike output (middle), LFP output (bottom).

Table 2-2 summarizes the performance of this work as compared to state of the art designs from industrial and academic researchers [AZI] [HAR] [WAT] [XIA2] [WAL]. By carefully engineering the system architecture to exploit the strength of deep-submicron processes, and employing low-noise circuit techniques, the area of the entire acquisition chain is reduced to 0.013mm^2, over a factor of 3 smaller than the smallest front-end amplifier reported to date [AZI]. State-of-the art noise, CMRR and PSRR are maintained despite the reduction of the supply to 0.5V.

Table 2-2: Summary of performance metrics for this work and comparison with state-of-the-art. All metrics for this work are given for complete system including ADC.

	[AZI] JSSC '09	[HAR] JSSC '07	[WAT] BioCAS '07	[XIA] ISSCC '10	[WAL] VLSI '11	This Work
Power (μW)	15	42.2	7.56	0.64	43	**5.04**
IRNoise (μV), Spike	7.0	5.1	3.06	14	2.2	**4.9**
Spike Bandwidth	5kHz	5kHz	5.3kHz	6.2kHz	10kHz	**10kHz**
NEF	4.6	9.8	2.67	6.5	5	**5.99**
PEF	63.48	316.9	20	33.8	30	**17.96**
IRNoise (μV), LFP	-	-	1.66*	-	14	**4.3**
LFP Bandwidth	-	-	300Hz*	-	100Hz	**300Hz**
CMRR (dB)	-	-	66	59	-	**75**
PSRR (dB)	-	-	75	71	-	**64**
V_{DD} (V)	3	3.3	2.8	0.8	1.2	**0.5**
Area (mm^2)	0.04	0.16	0.16	0.4**	0.2**	**0.013**
Technology	0.35μm	0.5μm	0.5μm	0.13μm	0.13μm	**65nm**
Blocks included in comparison	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF, ADC	**LNA, BPF, ADC**

*LFP not recorded simultaneously, requires reconfiguration
**estimated

2.4.2 *Power Efficiency Factor*

The 4th and 5th rows of the table compare the measured power-consumption and noise tradeoff achieved by this work to state of the art. This comparison is made using the well-established Noise Efficiency Factor (NEF) [STA] metric, as well as a Power Efficiency Factor metric PEF = NEF^{2}V$_{DD}$. NEF normalizes the input-referred noise of the amplifier to the input-referred noise of a single BJT that dissipates the same total current. A complete derivation of PEF is given in Appendix A. For two circuits with the same supply voltage NEF is a good metric to describe the power/noise tradeoff. However, two amplifiers with the same total current and noise but different V_{DD}s will have equal NEF

but different power dissipation, therefore NEF is insufficient to describe which one is more power efficient. To mitigate this issue a more direct comparison of the total power consumption can be made by the PEF metric, which normalizes the noise power multiplied by the total power by the same factor for an ideal BJT (Eq. 2-5). A complete derivation is provided in appendix A. The resulting metric is dependent on the bandwidth, input-referred noise and power of the circuit rather than the current.

$$PEF = \frac{V_{n,rms}^2 \cdot V_{DD} I_{tot}(myckt)}{V_{n,rms}^2 \cdot V_{DD} I_{tot}(bjt)} = \frac{V_{n,rms}^2 \cdot 2P_{tot}}{\pi \cdot kT/q \cdot 4kT \cdot BW} \quad (2\text{-}5)$$

NEF and PEF numbers for this work were computed using the total input-referred noise and power of the entire signal acquisition chain including the ADC. Typically NEF is computed only for the amplifier, and therefore does not describe the efficiency of the entire system, however the NEF of the merged amplifier-DAC is 5.3 and the PEF is 14. When compared using the NEF metric, the proposed system is comparable to recent state of the art. When comparing systems using the PEF metric, this work is the most power-efficient reported.

CHAPTER 3: ELECTROCORTICOGRAPHIC SIGNAL ACQUISITION

3.1 Electrocorticographic Front-End

As described in Chapter 1, state-of-the-art ECoG and EEG amplifiers occupy a large portion of die area due not only to the input AC coupling capacitors but also to the feedback capacitors that are used to cancel the upmodulated offset at the summing node. While good power efficiencies have been achieved, the resulting die area per amplifier in even the smallest implementations [FAN] makes arrayed implementations beyond approximately 8 amplifiers impractical. Thus it is important to substantially shrink the die area of ECoG neural amplifiers and front-end circuits while maintaining or improving power efficiency.

3.1.1 *Front-end architecture selection*

The key challenge in reducing the area of the ECoG front-end is to efficiently cancel the offset introduced by the electrodes.

Since the DC-coupled Action Potential Front-End of Chapter 2 achieved substantial area reduction and improved power efficiency, let us consider whether same the architecture can be used in ECoG recordings. If no explicit noise-mitigation technique were used, the input referred noise in the ECoG band (1-500Hz) would be approximately 7μV, which is unacceptably large. Since this figure is dominated by 1/f noise of the amplifier, it can be mitigated using well-known 1/f noise reduction techniques such as chopper stabilization [ENZ]. However, simply applying chopper stabilization to the architecture of Figure 3-1 does not give the expected results.

Consider the merged amplifier-DAC pictured in Figure 3-1. When there is no offset, the differential pair devices have equal sizing. The signal is up-modulated to the chopper frequency and harmonics, but since no offset is present, the DAC does not need to be chopped. This means that for a sufficiently high f_{chop}, nearly all of the 1/f noise can be eliminated.

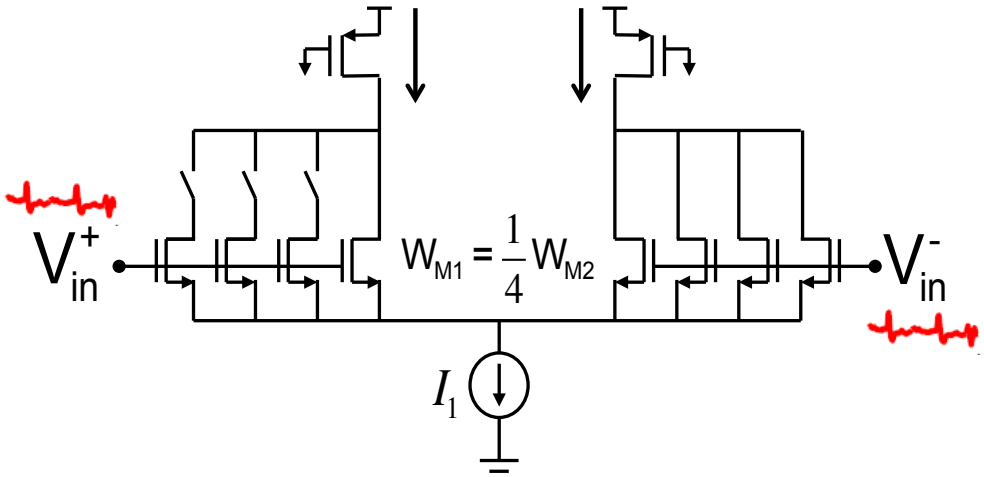


Figure 3-1: Merged Amplifier-DAC Schematic

Next consider the case when the maximum offset is applied and there is a +50mV offset at the input is up-modulated with the neural signal. In order to cancel this offset, the ratio of the widths of the input devices is $W_1/W_2 = 1/4$. When the chopper changes phase, the offset seen at the input of the amplifier changes to -50mV. In order to compensate for this change the polarity of the DAC must change to $W_1/W_2 = 4/1$. Since the sizes of the input devices are changing with a frequency of f_{chop}, their 1/f noise is also changing at that frequency. Thus part of their 1/f noise is being up-modulated with the signal, degrading the effectiveness of the chopper at mitigating 1/f noise. The amount of 1/f noise after chopper stabilization of the DAC from the input devices is

$$S_{\frac{1}{f}chop} = (1 - M)^2 S_{1/f}, \tag{3-1}$$

where M is the ratio W_1/W_2 if $W_2 > W_1$ and W_2/W_1 if $W_1 > W_2$.

In the regime of ECoG recording where the bandwidth of interest lies between 1Hz to 500Hz the noise is dominated by 1/f noise, therefore Equation (3-1) is a reasonable approximation for the total noise of the system after chopper stabilization is employed. Figure 3-2 shows the calculated noise of the amplifier of Figure 3-1. The black line represents the total noise in the 500Hz frequency band without chopper stabilization. The red line represents the thermal noise floor of the circuit and the blue line represents the offset-dependent total noise with chopper stabilization employed. At zero offset, the

circuit has the potential to achieve less than 1μV of input-referred noise, while at 50mV offset the noise increases to over 4μV. The input device sizes used for this simulation are 336/0.2μm.

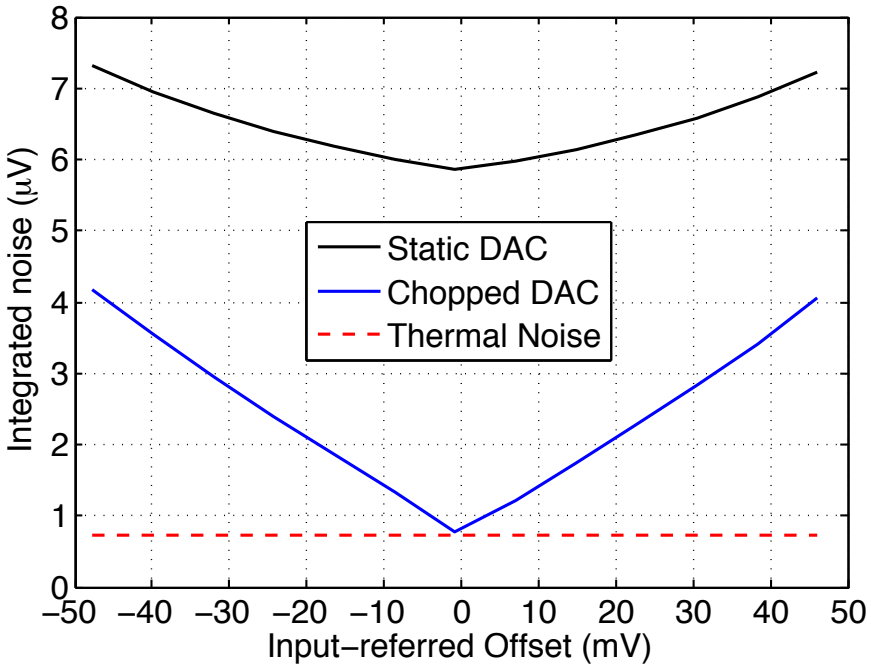


Figure 3-2: ECoG Integrated Noise vs. Input-referred Offset for the Merged Amplifier-DAC

Sizing up the devices to decrease their 1/f noise spectral density can help mitigate this affect but is unattractive for the following reasons.

1. The input capacitance and 1/f noise corner of the amplifier of Figure 3-1 are respectively 1pF and 5kHz. As a result, the input impedance of the front-end after chopper stabilization at 10kHz would be reduced to 25MΩ assuming the input device sizing is held constant.
2. Offset from the sensor is now up-converted to the chopping frequency, and must be canceled prior to demodulation to prevent ripple. This can be achieved by chopping the offset-canceling DAC as discussed above. The 1/f noise corner after chopping could be as large as 1kHz, leading to an integrated noise approximately 4x higher than the thermal noise floor in the band of interest.
3. In order to achieve input-referred noise close to 1μV, the input devices alone would have to be sized up by approximately 40x each leading to >5000μm^2 of active area. In practice, since the DAC is organized in unit elements, the physical layout required could be up to 10x that amount.

4. The increased input device area will substantially increase the input capacitance of the amplifier, degrading the input impedance to sub-MΩ levels.

As a result, implementing chopper stabilization together with the merged amplifier-DAC presents a significant challenge and requires a re-evaluation of the basic system constraints.

The proposed architecture for the ECoG front-end is shown in Figure 3-3 and consists of an open-loop chopper amplifier. To achieve a low 1/f noise the DAC is implemented by passive components as opposed to transistors. The upmodulated offset is mitigated using a mixed-signal feedback loop that uses capacitors on the summing junction to cancel the offset. Capacitor values are substantially reduced since the open-loop architecture allows the capacitors to act as summing rather than pole-setting elements. The capacitor sizes are therefore only limited by layout considerations and parasitic capacitance on the summing node.

The forward path of the proposed architecture is composed of a broadband instrumentation amplifier and a VCO-based ADC. Building on the principles discussed in Chapter 2, the feedback path is comprised of a digital accumulator and a DAC, which realize a servo-loop that suppresses the offset. Feedback forces the output of the digital low-pass filter to track the low-frequency components, reducing the dynamic range requirement of the instrumentation amplifier and ADC cascade. The mixed-signal feedback loop takes the place of an analog integrator, allowing the large time constant necessary to cancel DC to be once again realized in a compact footprint using digital gates.

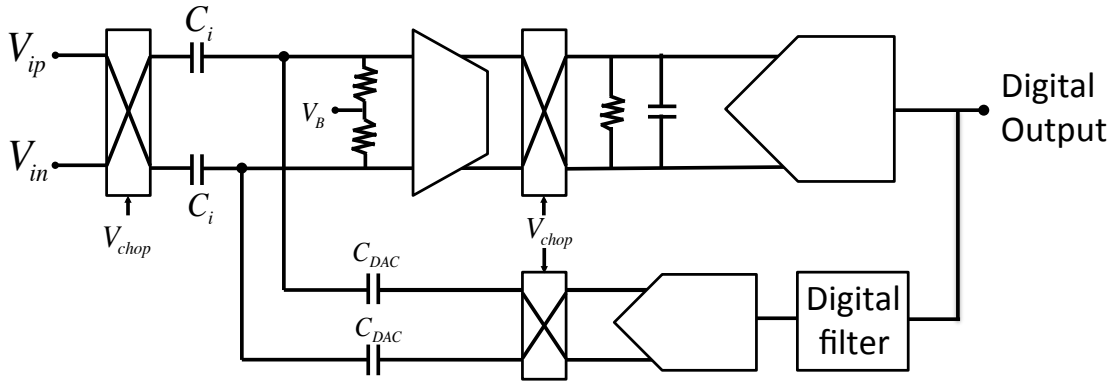


Figure 3-3: ECoG Front-End Block Diagram

The architecture in Figure 3-3 holds many of the same advantages as the action potential architecture of Chapter 2 such as low area, programmability and "per-pixel" digitization, which eliminates the complicated routing of analog signals at the top level. The efficient

realization of this architecture presents a few new challenges that are discussed in detail in the following sub-sections.

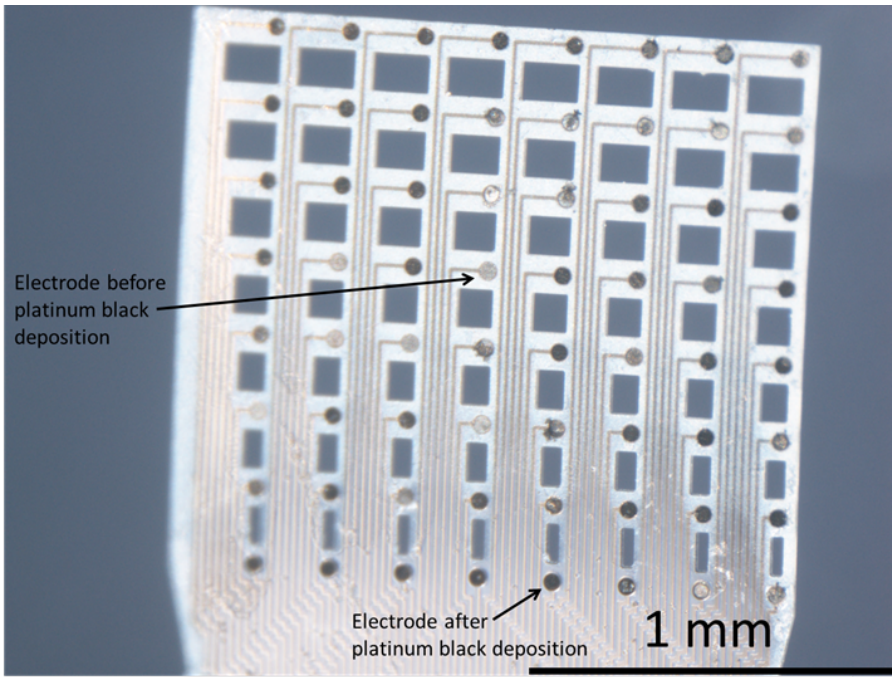
3.1.2 *Input impedance*

This front-end is designed to be used with micro-ECoG electrodes, but should be flexible enough to be use in a system with any ECoG electrodes. The small surface area of the microfabricated ECoG electrodes leads to a high input impedance necessitating a high front-end input impedance, making this interface the most demanding.

High-density microfabricated ECoG electrodes have been demonstrated using standard thin-film processing techniques. The electrodes reported in [LED] yield a resistance of approximately 30MΩ at 1kHz and a resistance of 1-10GΩ at DC. The goal of designing the input impedance of the front-end is to pass the in-band signal without loading the electrodes, whereas loading the electrodes at DC can have a positive effect. In-band input impedances between 10 to 100MΩ would necessitate an input impedance of >1GΩ for the recording electronics making a chopper stabilized implementation impractical. Additionally, long traces of high-impedance electrodes degrade system performance since they contribute thermal noise and are susceptible to crosstalk and coupling from interferers.

In order to improve the electrical coupling to the brain, platinum black is electroplated on the surface of the electrodes [FRA]. Platinum black is a highly porous, conductive material, which effectively increases the surface area of the electrode. For equal diameter, the impedance of platinum black electrodes is more than two orders of magnitude smaller than their platinum counterpart. Figure 3-4 shows a microfabricated ECoG grid with platinum black electroplated to every other electrode. The corresponding impedance of each electrode is plotted at 1kHz showing a 1000x reduction in impedance.

The impedance of the platinum black electrodes at 1Hz is on average approximately 300kΩ. For these electrodes, in order to pass the signal band 1 Hz to 500Hz, the input impedance of the amplifier would ideally be two orders of magnitude higher which is equal 30MΩ, although lower is sufficient. While 30MΩ is more than an order of magnitude lower than the requirement for the action-potential front-end, it nonetheless remains a challenge to meet with a chopper-stabilized front-end since switching capacitance results in very low impedances.



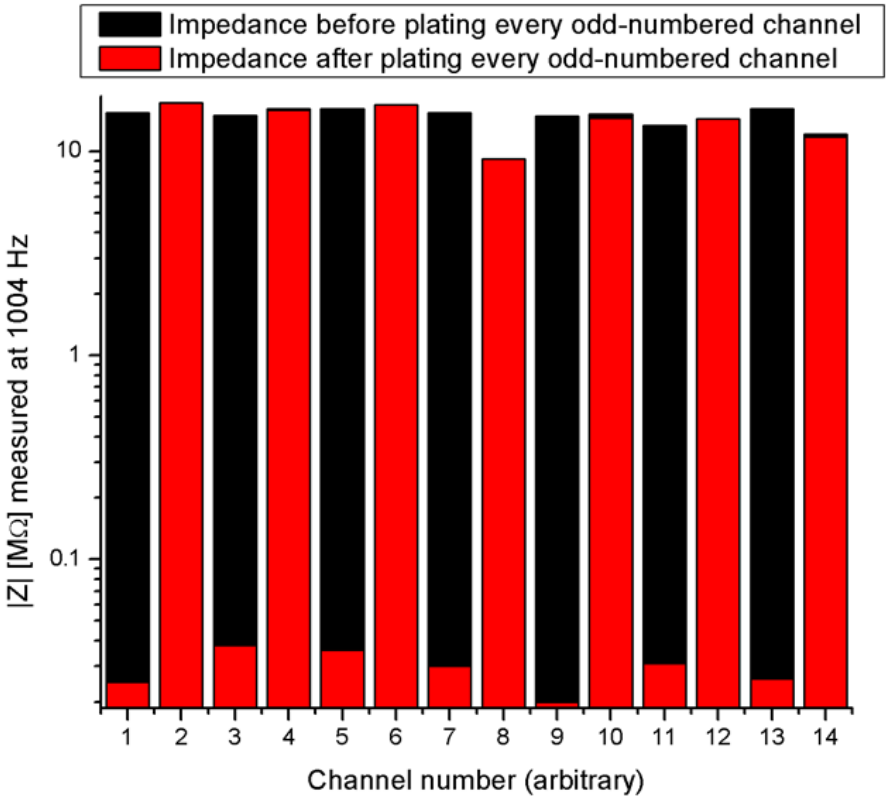


Figure 3-4: (Top) ECoG electrodes with every other electrode electroplated with platinum black. (Bottom) The impedance of the electrodes at 1kHz.

3.2 System and Filter Design

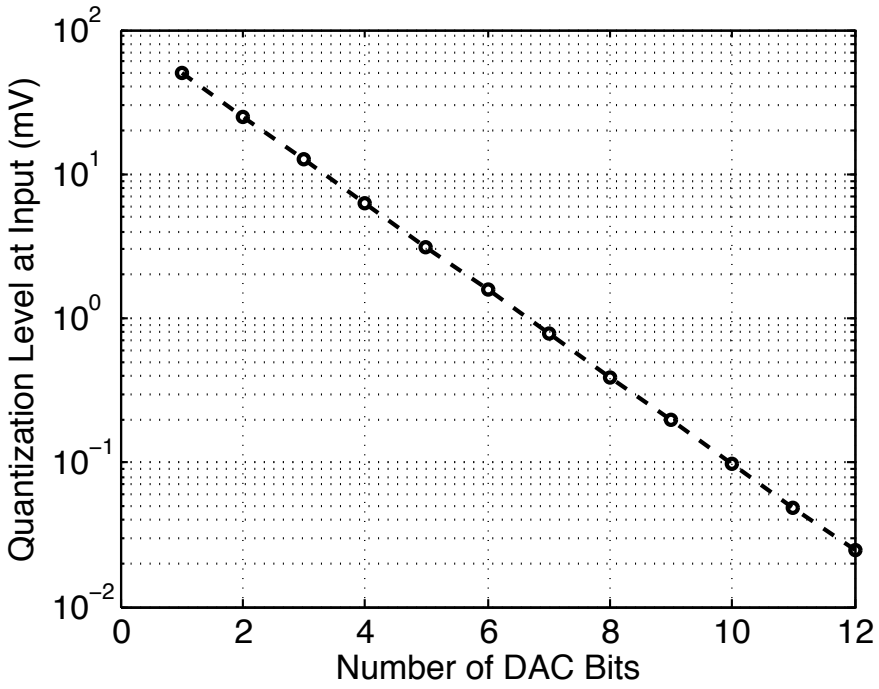


Figure 3-5: Input quantization voltage level vs. Number of DAC bits

Open-circuit potentials in the 100s of mV have been observed for platinum black electrodes in solution [FRA]. The DC resistance of the electrodes are measured and calculated to be on the order of GΩs, therefore an input impedance on the order of 10MΩ will diminish the offset to <10mV. 100mV of offset cancellation range was allocated to the system. Given this full-scale voltage of the DAC it is first important to determine how many bits of resolution are necessary.

To save area and capacitance at the input an oversampled, Delta-Sigma modulated DAC is implemented. In addition to determining the total resolution necessary, the partition between physical bits and oversampled bits must also be determined. Since the DAC feeds back to the input, its quantization noise must be low enough that it does not impact the noise floor of the amplifier. Take for example the quantization noise of a single-bit DAC. Figure 3-5 shows that the amplifier would have to be able to handle swings of ±50mV at its input. Such swings would clearly saturate the forward-path electronics.

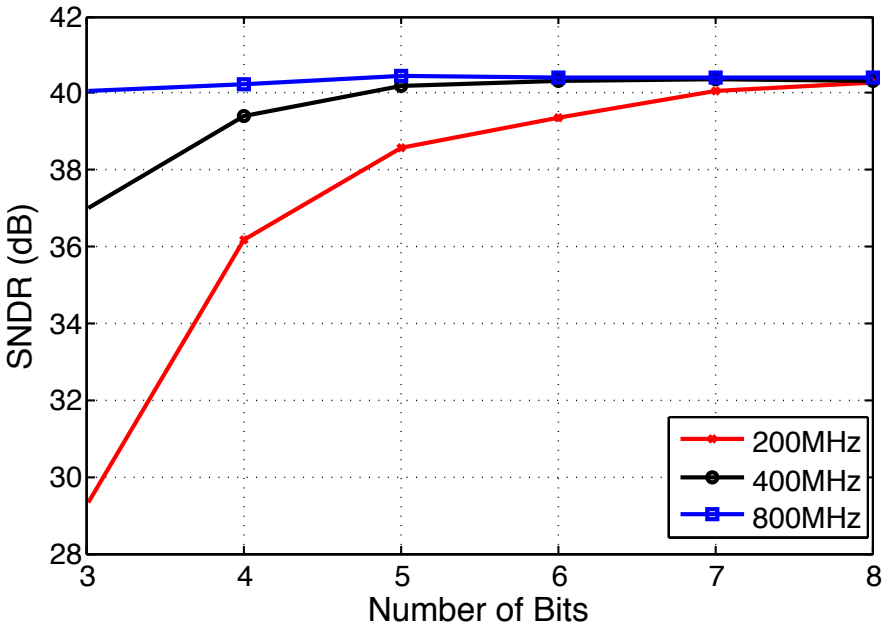


Figure 3-6: SNDR vs. Number of DAC bits for various DAC frequencies in open loop.

Using a behavioral simulation in Simulink, the number of physical DAC bits was swept for various DAC clock frequencies. Figure 3-6 shows an open-loop simulation of the ECoG band SNDR vs. the number of bits in the DAC across several frequencies. A 1μV noise floor and 100μV mid-band signal was used for the simulation. To suppress the DAC quantization noise below the amplifier noise floor a Delta-Sigma clock frequency of at least 800kHz is required. 1MHz was chosen for system simplicity and ease of filtering which will be discussed later in this section.

Since the input of the amplifier is broadband, a square wave can approximate the quantization noise seen at the input. 1MHz square waves of varying amplitude were injected at the input of the amplifier in transistor-level simulation to determine the maximum DAC quantization level before there is a noticeable increase in the amplifier noise floor. This quantity was determined to correspond to 5 bits. A full resolution of nearly 20 bits in the feedback DAC is realized with a 5-bit physical DAC with an OSR of 1000. This corresponds to a quantization level of 0.1μV, small enough to suppress the quantization noise below the thermal noise floor of the front-end.

Figure 3-7 shows the block diagram for the behavioral model of the front-end in closed loop, which was modeled using MATLAB and Simulink. The first low-pass filter in the cascade represents the finite bandwidth of the chopper amplifier. The amplifier must be designed broadband with respect to the DAC clock frequency of 1MHz so that Delta-Sigma noise is allowed to pass through the chopper amplifier. Filtering the Delta-Sigma

signal prior to downconversion will result in noise folding in-band, and therefore must be avoided. The necessity for an explicit low-pass filter implemented after the down-modulation is illustrated in Figure 3-8, which shows that once the system loop is closed, the large quantization noise at high frequency will fold back in-band. Although the quantization noise of the DAC is below the in-band thermal noise floor, putting the system in feedback causes a degradation of the in-band SNDR by folding high-frequency noise back into baseband and degrading the noise floor by more than 4dB for a 5-bit DAC.

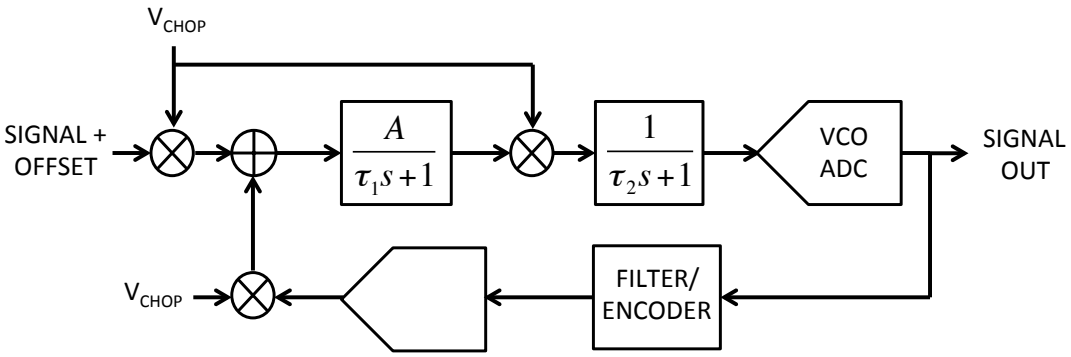


Figure 3-7: Behavioral model of ECoG front-end, modeled in Simulink

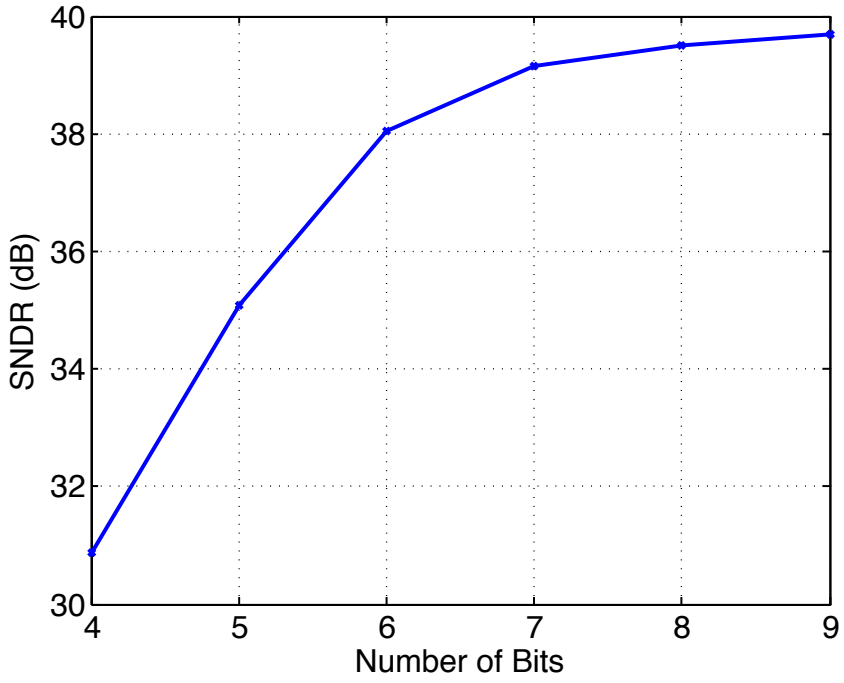


Figure 3-8: SNDR vs. Number of DAC bits in closed-loop

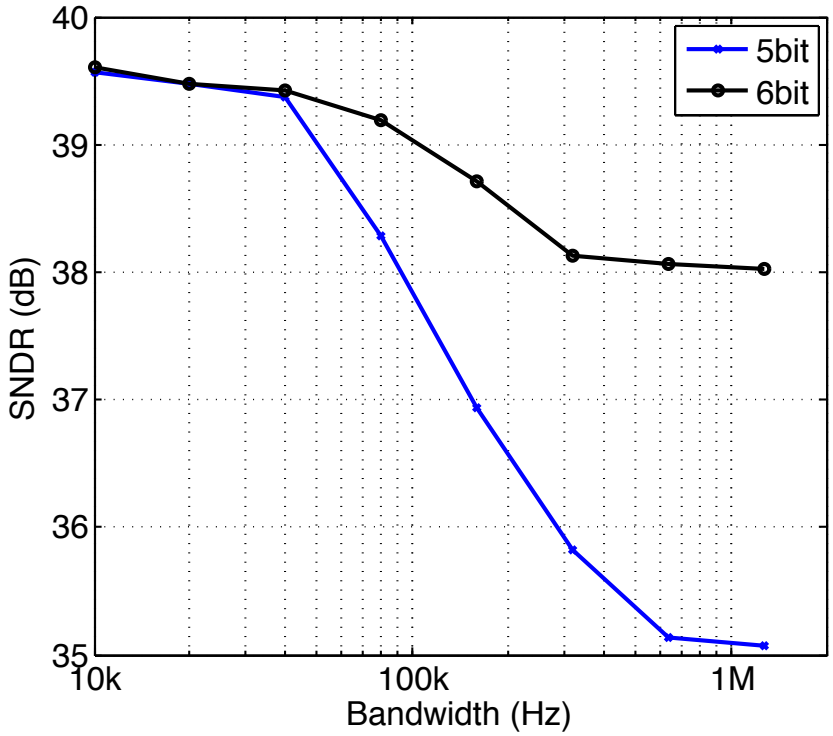


Figure 3-9: SNDR vs. Bandwidth for 5-bit and 6-bit DACs

To overcome the noise folding a single-pole filter is placed in the forward path after the down-conversion chopper to filter the high-frequency quantization noise and improve the phase margin of the loop. In order to determine the required bandwidth for this filter, Figure 3-9 sweeps the bandwidth and shows that the thermal noise floor can be recovered for sufficiently low bandwidths. The noise floor degradation for a 6-bit DAC is less severe even in the absence of this filter since the quantization noise is 3dB lower. To avoid the use of a low-pass filter a 6 or 7 bit DAC can be utilized at the expense of increased die area and lowered input impedance assuming the unit capacitor size is held constant.

3.3 Circuit Design

The ECoG front-end is designed to operate off of a 0.5V supply voltage. The advantages detailed in Chapter 2 for a reduced supply voltage still hold in this environment since it is a fully implantable, remotely powered system. Circuit scalability is of high importance in an ECoG context since cortical coverage is important in cortical mapping applications

and scaled numbers of electrodes are more easily achieved at the surface of the brain if the electrodes are flexible and conformal.

3.3.1 *Feedback DAC*

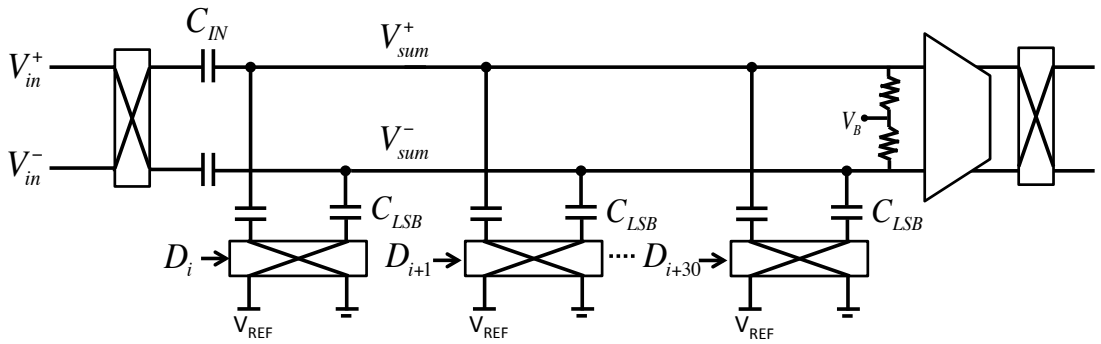


Figure 3-10: Simplified feedback DAC schematic

In order to cancel the up-modulated input offset, a 5-bit charge-distribution feedback DAC is employed. Figure 3-10 shows a simplified schematic of the DAC. To minimize DNL, the DAC is thermometer coded. To minimize area each unit capacitor is minimum sized. The capacitors are implemented as metal-insulator-metal (MIM) capacitors that have relatively large minimum dimensions and 5% relative matching, thus maintaining low DNL. In this implementation, V_{REF} = 0.5V and is tied to V_{DD}. To cancel a full-scale voltage of 100mV, or 50mV on each differential input, $C_{IN} = 10C_{DAC}$, where $C_{DAC} = 31C_{LSB}$, and C_{LSB} = 41fF. The summation nodes are biased (V_B) through a high resistance. The value this resistance must be high enough such that the high-pass filter pole that it produces together with C_{IN} is well below the lowest chopper frequency and thus out of the signal bandwidth.

Each unit cell of the feedback DAC is comprised of two capacitors, C_{LSB}, that are switched in opposite polarity at each phase of the chop clock. Since the chop clock guarantees switching at every cycle, the capacitors do not have to be explicitly reset. Thermometer-coded digital control bits, D, control the polarity of each unit cell modulating the amount of charge that is absorbed by the DAC every time the chop clock changes. For example, if there is no offset present at the input, half of the capacitors on V^+_{sum} would switch low-to-high, and the other half would switch high-to-low. These capacitors would neutralize and thus not cancel any offset from the input. In reality, since there are 31 unit capacitors, one capacitor must dither between the two states in order to realize zero offset cancellation.

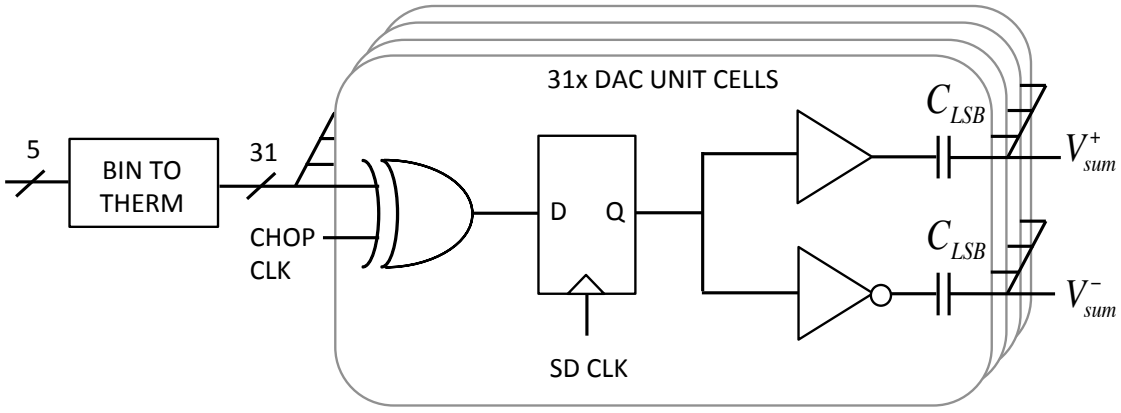


Figure 3-11: DAC unit cell schematic

Figure 3-11 shows a simplified schematic of each unit cell of the DAC. The Delta-Sigma encoder provides a 5-bit output that is thermometer encoded and distributed to the unit cells. An XOR gate inverts the polarity at each phase of the chop clock. Since the logic is combinational, and driven by two inputs, one that is clocked at the Delta-Sigma clock frequency and the other at the chopper clock frequency, the DAC is retimed to the highest clock frequency in order to avoid glitches. To ensure alignment of the DAC chopper to the amplifier chopper, similar retiming is performed for the other chopper signals in the system. The signal is then buffered and inverted to provide an anti-phase signal to the negative input with the two paths designed for matched delay.

The final DAC capacitor driver is referenced to V_{DD}, but a lower voltage can be used at the cost of a reduced full-scale voltage of the DAC. Alternatively a lower ratio of C_{IN}:C_{DAC} may be employed, however, this will cause C_{DAC} to further attenuate the signal at the input of the amplification stage which will degrade noise performance. As designed, the attenuation of the DAC will degrade SNR by less than 0.5dB.

To maximize capacitance density and minimize layout area, metal-insulator-metal (MIM) capacitors were used for both C_{IN} and C_{DAC}. Since MIM capacitors are processed in the upper metal layers of the process, active circuits can be laid out in the lower layers. DAC unit cells are laid out below the C_{DAC} capacitors and all other front-end circuits are laid out below the C_{IN} capacitors. An additional metal layer below the MIM capacitors is used as a ground shield to minimize coupling of the digital circuits to the sensitive analog input.

3.3.2 *Chopper stabilization and input impedance*

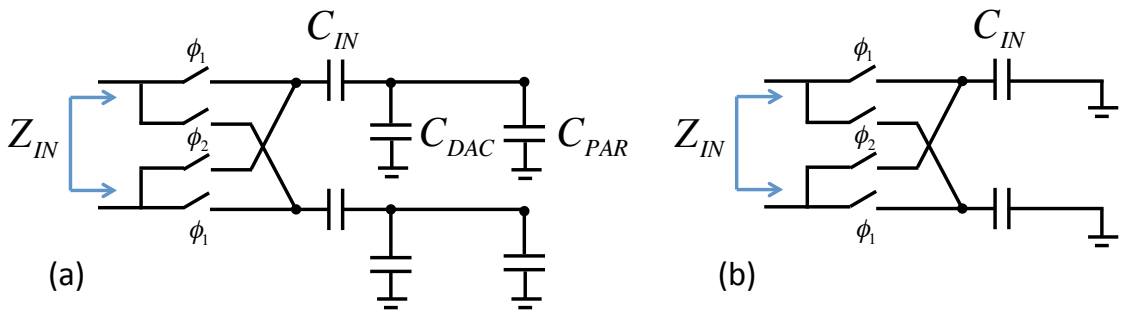


Figure 3-12: Simplified circuit diagram of switched-capacitor resistance of the input chopper (a) in-band and (b) at DC

One drawback to using chopper stabilization is that the switched-capacitor resistance degrades the input impedance of the amplifier. A significant advantage to using an open-loop architecture is that the effective input capacitance is reduced. Take the simplified model of the in-band front-end input shown in Figure 3-12(a). The input capacitance of the amplifier at each positive and negative input to ground is C_{IN} in series with $C_{DAC} + C_{PAR}$, where C_{PAR} is the parasitic capacitance on the summation node and is caused by bottom-plate capacitance, gate capacitance of the input devices and other layout parasitics. Since $C_{IN} >> C_{DAC}$, the differential input resistance of the amplifier can be shown to be approximately

$$|Z_{in}| \approx \frac{1}{4f_{chop}(C_{DAC} + C_{PAR})}. \tag{3-2}$$

Since a high f_{chop} will degrade the input impedance it is important to consider both capacitance and chopper frequency simultaneously. Z_{IN} can be maximized in the following ways:

1. Minimize C_{DAC}. In this implementation the size of C_{DAC} is limited by the minimum sizing of a MIM capacitor, however, C_{DAC} cannot be arbitrarily small and should be significantly larger than C_{PAR} in order to not have its effect diminished. Therefore C_{DAC} is a function of C_{PAR}.
2. Reduce f_{chop}. This can be achieved by selecting a type of amplifier input transistor with low 1/f noise spectral density and by increasing the size of that device.
3. Minimize C_{PAR}. This can be achieved by selecting a type of amplifier input transistor with low gate capacitance and by decreasing the size of that device.

Techniques 2 and 3 are seemingly at odds with each other; therefore in selection and sizing of the amplifier input device, the quotient of the 1/f noise spectral density and capacitance $S_{1/f} \cdot C_{PAR}$ must be minimized. Standard threshold PMOS input devices were chosen in order to minimize this metric.

The input resistance of the front-end is chopper frequency (f_{chop}) dependent. At low frequency, the mixed-signal feedback loop becomes active, changing the impedance characteristics. Figure 3-12(b) shows an equivalent circuit model for the input of the front-end at DC. The feedback loop tracks the DC voltage and cancels it at the summing nodes, creating a virtual ground. In this case, C_{IN} dominates the input impedance characteristics of the front-end and the input impedance becomes

$$|Z_{in}| \approx \frac{1}{2f_{chop}C_{IN}}. \tag{3-3}$$

Since $C_{IN} = 10C_{DAC}$, the DC input resistance will be significantly lower than the impedance in-band. This lower impedance helps to attenuate the DC offset present at the electrodes and stabilize the baseline.

Since the input devices are PMOS, the summing junction and input of the amplifier are biased at a low voltage necessitating NMOS devices for the chopper switches. If the gates of these devices are driven between 0V and V_{DD} (0.5V), their relatively high threshold voltages lead to a small drain-source conductance, which can negatively impact the noise performance of the amplifier. Alternatively, low-threshold devices are a poor option since they cause large leakage currents to flow between the input terminals. Simulations show that the noise contribution of the standard NMOS input switches can be lowered to 2.5% of the total noise if the gate voltages are boosted to 1V in the on state. The voltage is boosted with a switched-capacitor voltage doubler at the system level and distributed to each front-end. This voltage doubler and system design are discussed in Section 4.3.

3.3.3 *Amplifier*

The forward path amplification needs to be broadband compared to the signal, at least 1-2 octaves above the Delta-Sigma modulation frequency. In order to achieve more than 3MHz of bandwidth in approximately 2μW of power dissipation three cascaded low-gain stages were used. Each stage is comprised of a PMOS input differential pair, a PMOS cascode device to extend the bandwidth by decreasing the miller capacitance at each input gate-drain junction, and a resistive load comprised of polysilicon resistors. The polysilicon resistors provide good noise performance and linearity at the cost of die area. Since the amplifier must absorb the large swings of the chopper ripple and Delta-Sigma quantization noise, linearity became a higher priority than die area in this design.

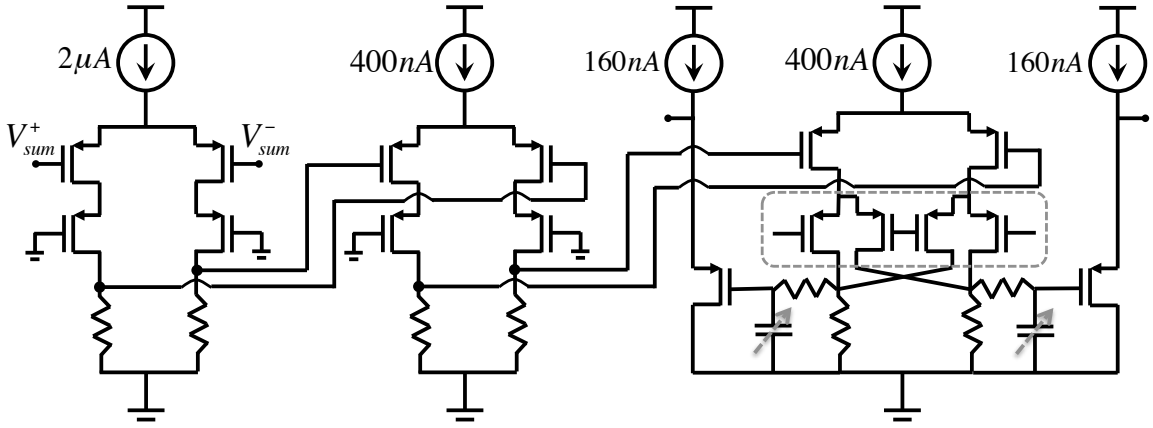


Figure 3-13: Amplifier and low-pass filter schematic. Chopper down-modulation switches are shown in the dashed box.

A tunable single pole filter is realized at the output of the third gain stage with the addition of tunable capacitance in parallel with the resistive load. The capacitors are realized with NMOS devices in depletion so that they remain linear throughout the signal range. Series resistance is added between the load resistor and the capacitor to reduce the low-pass filter pole without affecting the gain and output swing of the stage. The filter is tunable from a broadband 3.3MHz down to 40kHz.

The chopper down-modulation switches are shown in the dashed boxes of Figure 3-13. These devices act simultaneously as cascode devices and current-domain modulation devices. Down-modulating in the current domain is advantageous since chopping at a low impedance node in the current domain will not significantly degrade the gain of the stage; it can however increase the noise floor since the chopper switches are biased in saturation and therefore contribute 1/f noise. This scheme enables the seamless integration of a single-pole filter for filtering the Delta-Sigma noise. If the chopper switches were realized in the voltage domain at the output of the third stage, an additional buffer would be required to prevent the switched-capacitor resistance from affecting the filter pole frequency.

Finally, PMOS emitter-followers are added to level-shift the output. The ADC, largely reused from the Action Potential front-end discussed in Chapter 2 uses an NMOS-input differential pair driver, making DC level shifting from the chopper amplifier to the ADC driver necessary. The level shifters are sized to suppress their thermal and 1/f noise below the noise floor. Since they are single-ended, their current source devices also contribute significantly to their noise and must be sized accordingly. 1/f noise of the level-shifting stage accounts for 7% of the total input-referred noise when the chopper is clocked at

16kHz. Redesigning the ADC and driver with PMOS inputs and eliminating this level-shifting stage can achieve further noise and power reduction.

3.3.4 *ADC Driver*

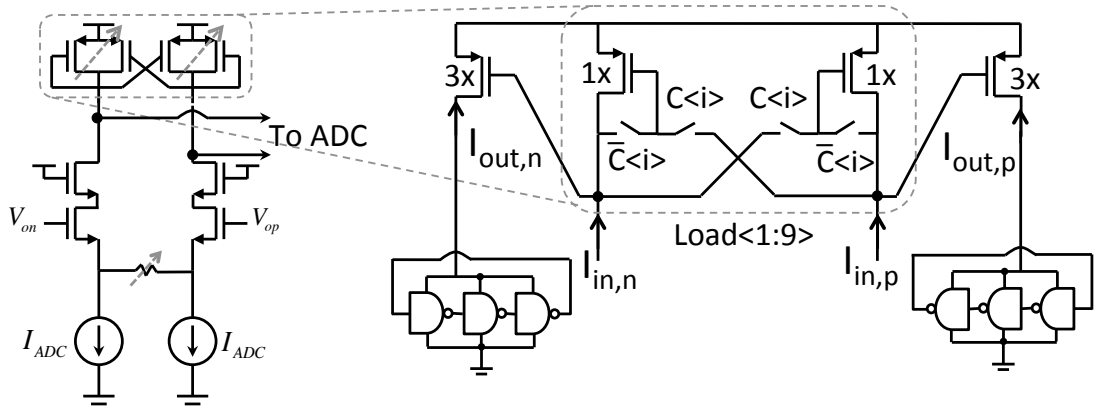


Figure 3-14: Schematic of ADC driver amplifier.

The system employs a similar current-driven, ring oscillator based ADC [HOV] [XIA1] as the Action Potential system [MUL] with a more stringent linearity requirement due to the chopper ripple and ΔΣ quantization noise that must be integrated. The driver consists of a differential-pair V-I converter cascaded with a current-mode programmable gain block as shown in Figure 3-14. The V/I converter operation is explained in section 2.3.5. Cascode devices are used so that the variable load rather than the drain-source conductance of the input device dominates the gain. Variable degeneration resistors are used to further trade-off gain for linearity.

Since the ADC driver stage is cascaded after the chopper amplifier, its 1/f noise can significantly contribute to the 1/f noise of the entire front-end, therefore all devices are designed large for the purpose of suppressing 1/f noise. 1/f noise of the ADC driver accounts for 2% of the total input-referred noise power when chopped at 16kHz, amounting to approximately 8.5nVrms/√Hz across a 500Hz bandwidth.

3.3.5 *ADC and Anti-aliasing*

In order to keep the quantization noise well below the thermal noise floor an ADC resolution of 12 bits is required. The ADC employs the same pseudo-differential, VCO-

based architecture shown back in section 2.3.6, Figure 2-16 and whose basic operation is illustrated in Figure 2-17.

Since the ADC must also quantize the range of the chopper ripple and ΔΣ noise, a full resolution of 14 bits is implemented in each of the counters. A 13-bit linear range is provided by each of the ring oscillators at 1kS/s. Each oscillator is designed such that the minimum and maximum oscillation frequencies f_{min} and f_{max} satisfy $|f_{max}-f_{min}| > 2^{12}f_s$ with f_s = 1kHz, therefore each differential output results in a dynamic range greater than 12 bits. Each counter is expressed as 14 bits to ensure monotonicity such that the counters never over-range twice. The counters are not reset with each clock period and are allowed to wrap. Digital correction is implemented to unwrap the codes prior to subtraction.

The counter output represents the average oscillator frequency over a period, corresponding to integration in the time domain and a sinc transfer function in the frequency domain. Thus the converter provides the desired boxcar sampling response, preventing aliasing of the wideband noise from the instrumentation amplifier. The box-car sampling characteristic introduces a second key benefit in this system, as it suppresses the shaped quantization noise from the ΔΣ DAC employed in the feedback. Because of the harmonic relation between the ΔΣ clock and the ADC clock, and the integrating nature of the ADC, the transfer between quantization noise and ADC output $NTF_Q(z)$ expressed in the 1MHz clock domain is given by the modulator NTF cascaded with that of a 1000-tap moving average (MA) filter. For a ΔΣ noise transfer function of NTF(z) = $1-z^{-1}$, and

$$NTF_Q(z) = NTF(z)MA(z) = \frac{1-z^{-1000}}{1000}. \quad (3\text{-}4)$$

The integrating characteristic of the ADC averages the DAC output bit-stream while performing the conversion, acting as first stage of decimation. Compared to the ΔΣ noise requirement in Section 2.3.5, although this ΔΣ modulator has a 10x higher OSR, its noise must be suppressed below a noise floor more than 10^4 times smaller. As a result, although the high-frequency quantization noise from the ΔΣ modulator is greatly attenuated by the averaging of the ADC, an additional low-pass filter is required for further quantization noise suppression. This filter was described in Section 3.2.

3.3.6 *Digital Feedback*

The digital feedback has the same basic architecture as the one described in Section 2.2. The integrator is clocked at a Nyquist rate of 1kHz while the ΔΣ modulator is clocked at 1MHz. The higher ADC resolution demands higher resolution and word lengths in the digital filter, growing the area occupation.

Since the forward path gain is significantly increased, a greater degree of signal attenuation is required in the feedback path in order to maintain stability. A barrel shifter implements this attenuation with 12-bit tunability in addition to the built-in attenuation of 2^{17}. The attenuation in the feedback path not only serves to stabilize the loop but also to tune the location of the high-pass filter pole.

3.4 Measurement Results

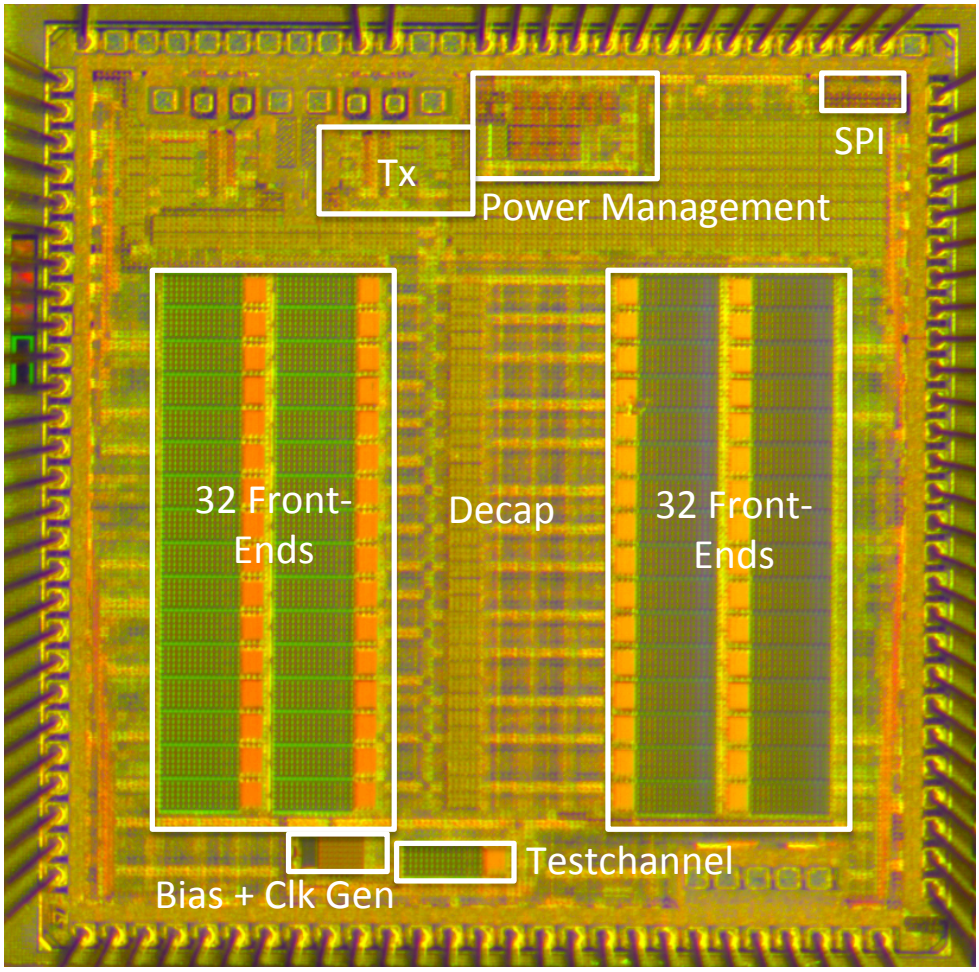


Figure 3-15: 64-channel ECoG Chip Microphotograph

The chip was fabricated in a 65nm 1P7M low-power CMOS process from ST Microelectronics. A chip microphotograph is shown in Figure 3-15. The chip contained 64 integrated front-ends and one stand-alone front-end test block. Power conversion and

management, wireless transmission, clock recovery and division as well as bias circuitry are all integrated on the die. The system details will be described in Chapter 4. The total chip area is pad-limited to 2.4mm x 2.4mm, the area of a single front-end is 0.025mm^2 and the area of the 64 front-end array including routing is 1.6mm^2. The total chip power consumption of the 64 front-ends plus the test-channel was measured to be 150µW, and the power consumed by each front-end is 2.3µW. The power dissipation is higher than designed since the polysilicon resistance was 20% smaller than their simulation value due to process variation, necessitating a higher current consumption in order to recover the lost gain.

Electrical characterization of the front-ends was performed by housing the die in a 124-pin 10mm by 10mm metal lead frame package connected a PCB through a test socket. An Opal Kelly FPGA was used to buffer the serialized digital data stream from the front-end outputs. All measurements were performed through the full acquisition channel including the on-chip ADC. Post-processing of the digital outputs was performed using MATLAB. Differential sine wave inputs were produced using a Stanford Research Systems DS360 low-distortion signal generator and attenuated to proper input levels at the acquisition channel input. Power and input impedance was measured using a Kiethley 2612A source-meter. Test-channel measurement results will be given in the remainder of this chapter, while system-level measurements and in-vivo tests will be detailed in Chapter 4.

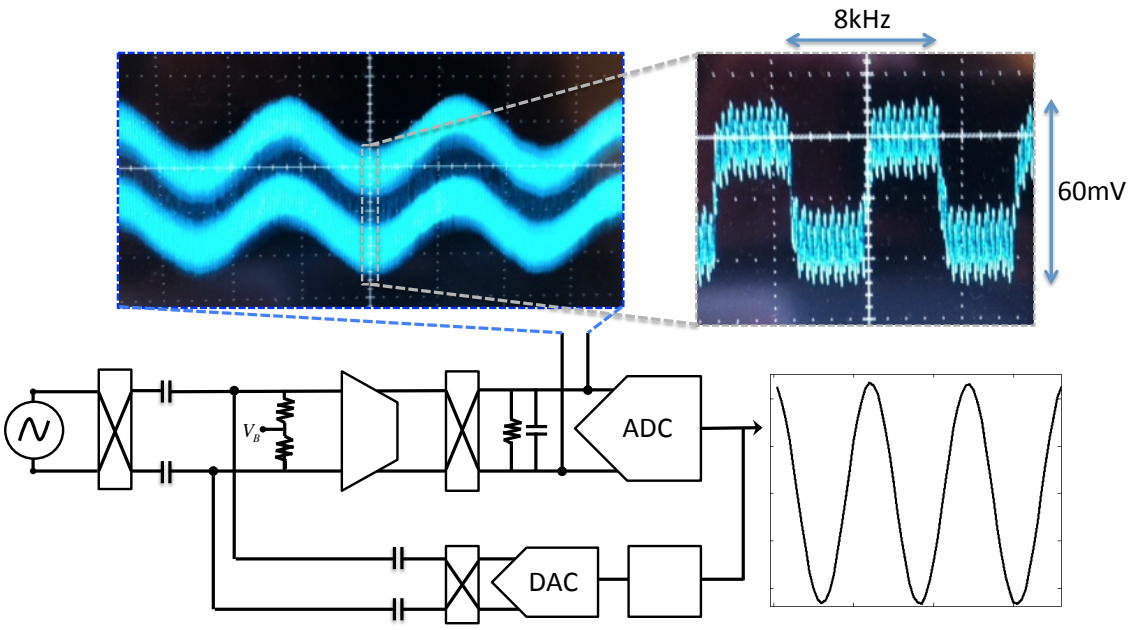


Figure 3-16: Oscilloscope capture of analog input to ADC and corresponding measured output of ADC from a 1mVptp sine-wave stimulus

Figure 3-16 shows oscilloscope captures of the analog output waveform from a 1mVptp stimulus. Analog outputs are first buffered with unity-gain feedback amplifiers on chip, go through additional on-board amplification using AD8429 parts and observed on an Agilent DSO7104A oscilloscope. The front-end chopper frequency is set to 8kHz and zero input offset is presented to the system.

The oscilloscope photos in Figure 3-16 show that the analog output exhibits chopper ripple after down-modulation as a result of amplifier offset. Riding on top of the chopper ripple is the Delta-Sigma modulation noise, which is clearly visible after the low-pass filter. The bandwidth of the filter is set to its lowest frequency and measured to be 50kHz. The total amplitude of the two superimposed signals is 60mV after amplification. The 1mVptp input signal is gained up and adds 30mVptp making the total signal swing at the input to the ADC 90mVptp. The corresponding ADC output waveform is also shown in the figure. It is clear from visual inspection that the ADC is able to filter both the chopper ripple and the Delta-Sigma noise to reproduce the original input sine wave. The remainder of this section will quantify the front-end performance.

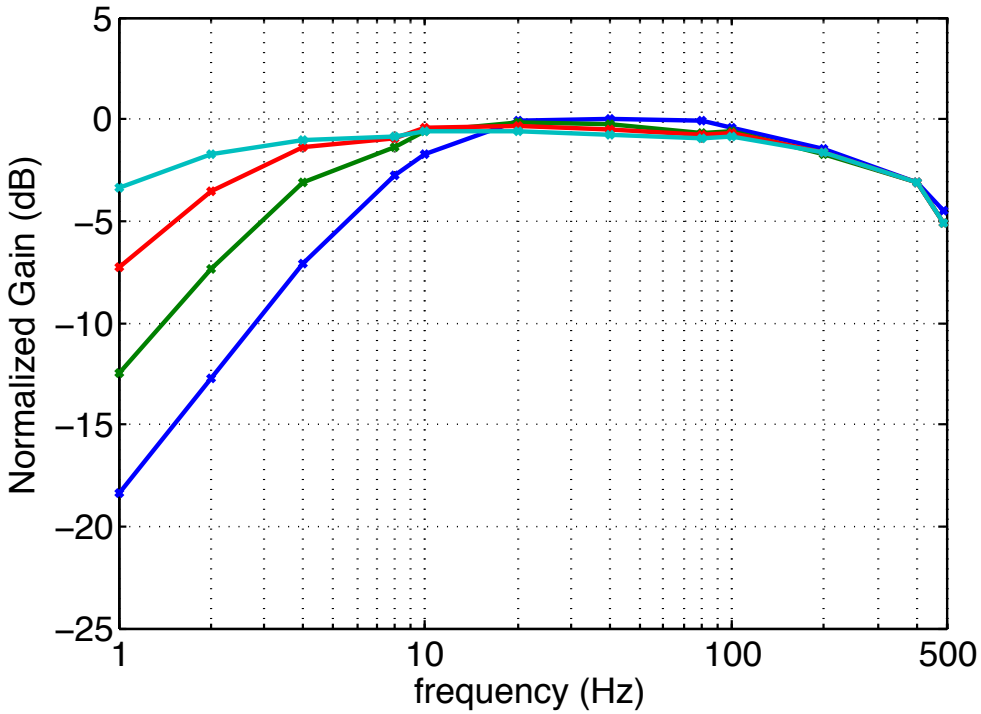


Figure 3-17: Front-end closed-loop transfer function. Digital tuning in the feedback path adjusts the high-pass filter pole.

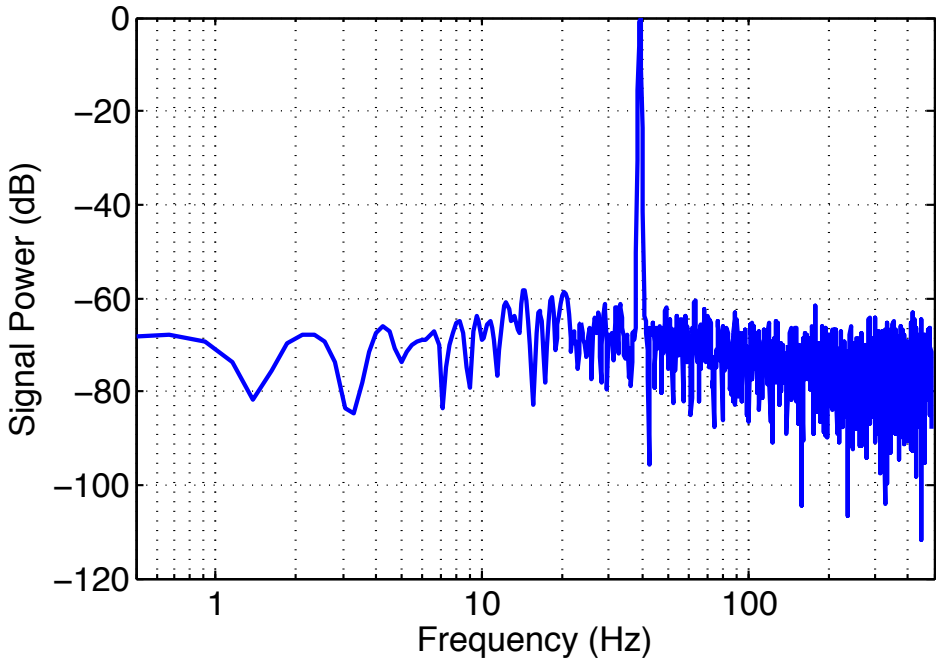


Figure 3-18: Power spectral density of output waveform with 0.5mVptp sinusoidal input stimulus at 40Hz.

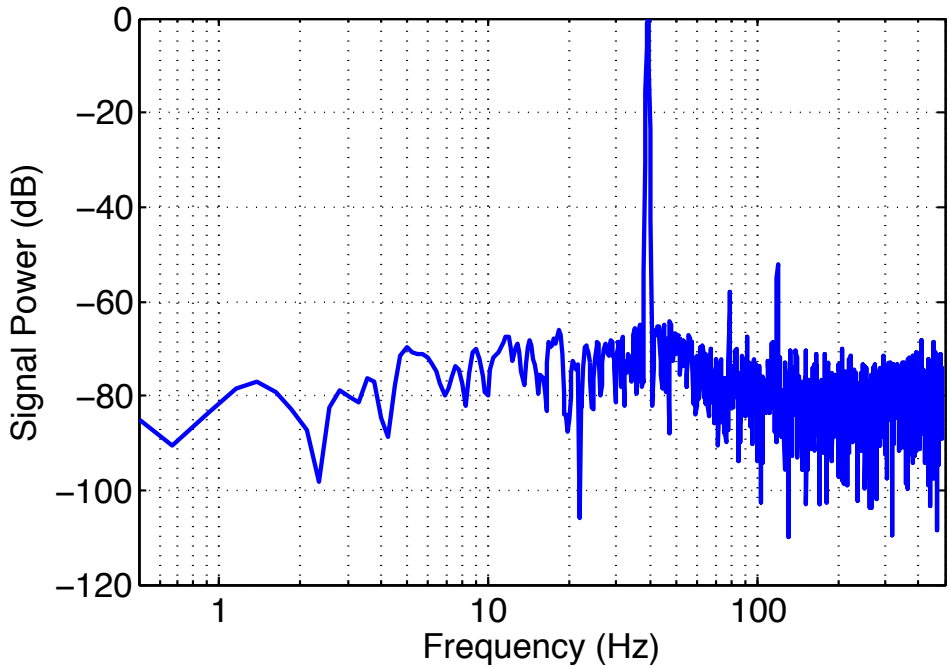


Figure 3-19: Power spectral density of output waveform with 1mVptp sinusoidal input stimulus at 40Hz.

The measured closed-loop transfer functions of the ECoG front-end from the input to the ADC output are shown in Figure 3-17. The transfer function shows a first-order high-pass filter with a pole that is digitally programmable in the feedback loop. Figure 3-17 shows transfer functions for four programmed states with poles at 8Hz, 4Hz, 2Hz and 1Hz. The low-frequency roll-off exhibits a -20dB/decade slope. The high-frequency roll-off is due to the sinc transfer function of the A/D converter that is deterministic and can be compensated for in DSP if needed.

Figure 3-18 shows the measured output spectrum of the acquisition system for a 0.5mVptp input sine wave at 40Hz. The signal power is normalized to the peak power. At this input level no harmonic tones are visible above the noise floor. Figure 3-19 shows the normalized measured output spectrum of the acquisition system for a 1.0mVptp input sine wave. At this input level second and third harmonic tones emerge in the spectrum. The complete system including the ADC exhibits an SFDR of 52dB and a total harmonic distortion (THD) of 0.4%.

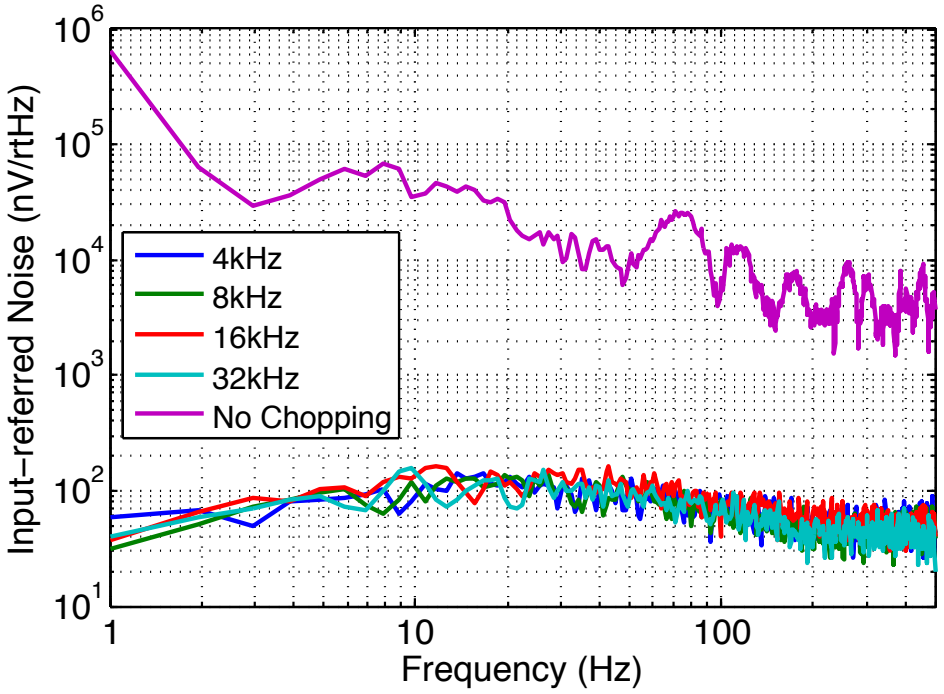


Figure 3-20: Input-referred noise power spectral density across a range of chopper modulation frequencies.

The input-referred noise spectral density is plotted in Figure 3-20. Noise is plotted for a range of chopper frequencies as well as for the open-loop system with chopping disabled. In the absence of chopper stabilization, the noise spectral density of the amplifier is

dominated by 1/f noise that is more than two orders of magnitude larger than the thermal noise floor. Integrated over the bandwidth, the noise of the amplifier without chopper stabilization would be 570μV. This is substantially higher than the noise of the AP front-end integrated over the ECoG bandwidth since small devices are used at the input to avoid parasitic capacitance. In addition, the absence of chopper stabilization makes the system more susceptible to interferers such as 60Hz noise, which impact the measured noise performance.

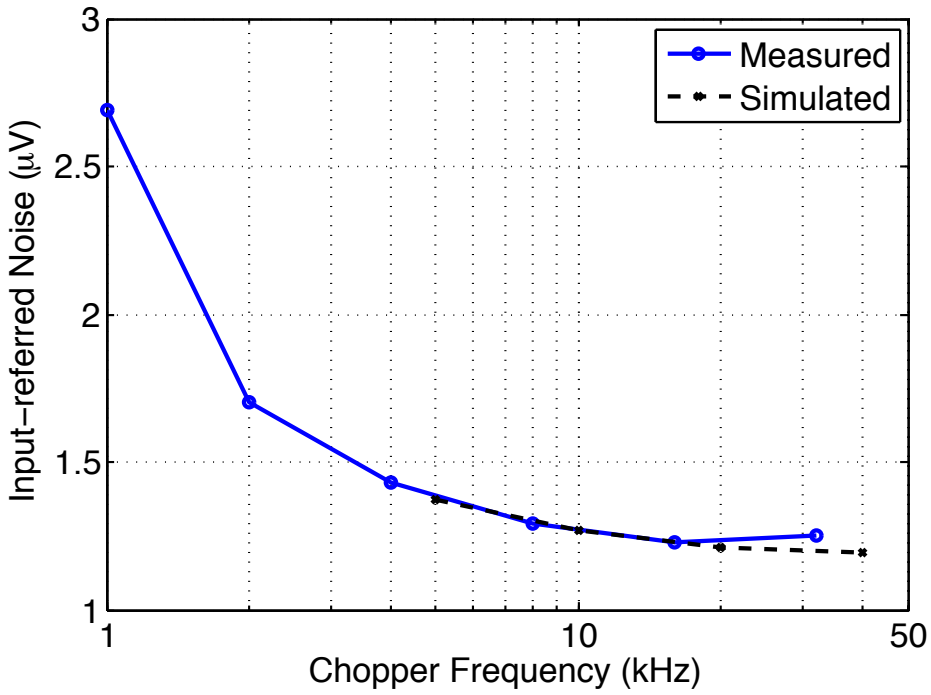


Figure 3-21: Integrated input-referred noise as a function of chopper frequency.

Table 3-1: Table of input-referred noise for several chopper frequencies

Chopper Frequency	Input-referred Noise
4kHz	1.43μV
8kHz	1.29μV
16kHz	1.23μV

The chopper stabilized closed-loop system reduces the 1/f noise corner to 100-200Hz. The input-referred noise integrated over the 500Hz bandwidth is plotted in Figure 3-21. Simulated values are plotted in the figure for comparison and show good agreement with the measured values. Higher chopping frequencies lower the 1/f noise corner frequency and reduce total input-referred noise. Chopping at frequencies beyond the inherent 1/f noise corner results in a diminished return in noise performance. Table 3-1 shows the exact measured values of input-referred noise for several operating frequencies of interest. Since the chopper stabilization frequency affects input impedance adversely it is important to choose the lowest frequency that still meets the required noise performance. Since operating at 16kHz only yields a 5% improvement in noise floor, 8kHz is chosen as the operating point for this system. Should higher input impedance be required, operating at 4kHz will double the input impedance with a 10% penalty in noise performance.

Operating at an 8kHz chopping frequency the NEF of the entire front-end, including power dissipated in the ADC is 4.76 and the corresponding PEF is 11.3. The amplifier alone consumes 1.4μW. Assuming the stand-alone amplifier would have the same noise performance as the full system (in reality the noise would be less), the NEF of the amplifier alone becomes when chopped at 8kHz becomes 3.7 and the corresponding PEF is 6.9. If chopped at 4kHz, the NEF of the complete system rises to 5.28 and the corresponding PEF becomes 13.9.

Input impedance was measured for all possible frequencies of chopper stabilization and plotted in Figure 3-22. The measurements were made at DC and at 100Hz (designated "in-band"). Figure 3-23 plots input resistance vs. input-referred offset for a constant chopper frequency of 8kHz. The calculated input resistances at DC and in-band are 4.9MΩ and 25MΩ respectively. The DC input resistance shows good agreement with calculation and stays constant to within 5% across all offset values. The in-band resistance shows agreement with calculation to within 10% and is constant to within 10% for the full range of input offsets. The capacitance that defines the in-band input impedance is significantly smaller than the capacitance that defines the DC impedance, and is therefore more susceptible to mismatch, although the discrepancy may also be account for by measurement error.

The full-scale range of the DAC was measured and found to be able to cancel a total of 98.6mV. The lowest offset cancelled was -49.1mV and the highest offset cancelled was +49.5mV.

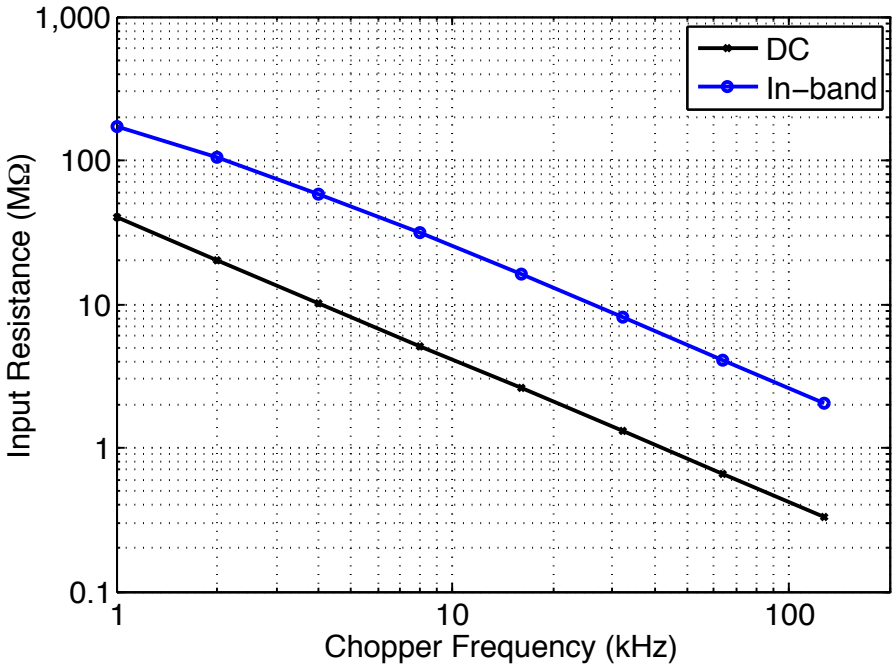


Figure 3-22: Input resistance vs. chopper frequency for DC and in-band signals

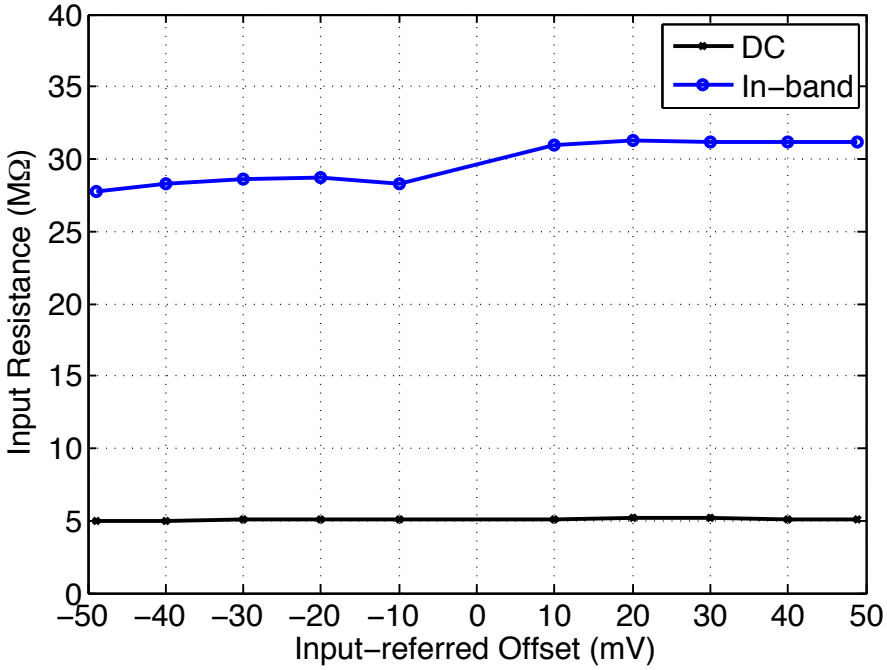


Figure 3-23: Input resistance vs. offset for DC and in-band signals at f_{chop}=8kHz

Finally, CMRR and PSRR were measured for the complete system in feedback with a chopper stabilization frequency of 8kHz. An in-band frequency of 60Hz was chosen for the analysis since it corresponds to a well-known interferer and is well within the bandwidth of the system. CMRR was measured by connecting both inputs to an input sine wave generator, which produced a 50mVptp sine wave at 60Hz. The differential gain was measured through the ADC and determined by taking the spectrum of the output signal and compared to a differential input at 1mVptp. The CMRR was measured to be 88dB.

PSRR was measured in a similar fashion to CMRR with a 10mVptp, 60Hz sine wave with 0.5V mean at the power supply pin. With the inputs grounded the PSRR was measured to be 67dB. The measured PSRR remained stable over a range of DC offsets applied at the input. It is possible to improve the PSRR of the system by decoupling the DAC reference from V_{DD}.

3.4.1 *Comparison with state-of-the-art*

Table 3-2: Performance summary and comparison with state-of-the-art ECoG and EEG front-ends

	[DEN] JSSC '07	[YAZ] JSSC '08	[VER] JSSC '10	[BOH] JSSC '11	[ZHA] TCAS, '11	[FAN] JSSC '11	THIS WORK
V_{DD} (V)	1.8V	3.0V	1.0V	1.5V	1.2V	1.0	**0.5V**
Power (µW/ch)	2	33.3	6.5	1.1	3.24	2.1	**2.3**
IRNoise (nV/rtHz)	100	60	130	340	85	670	**58**
NEF	4.6	4.3	9.37	6.38	5.38	20.94	**4.76**
PEF	38.1	55.5	87.8	61.0	34.7	438.5	**11.3**
R_{IN} (MΩ)	8	1000	700*	--	4	30	**28**
CMRR (dB)	100	120	60	--	80	120**	**88**
PSRR (dB)	--	--	--	--	60	120**	**67**
Area (mm^2/ch)	0.8	0.5	0.6	0.345	0.4	0.2	**0.025**
ADC Resolution	none	11-bit	12-bit	none	none	none	**12-bit**
# of Channels	1	8	1	1	1	1	**64**
Technology	0.8µm	0.5µm	0.18µm	0.18µm	0.13µm	65nm	**65nm**
Blocks included in comparison	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	LNA, BPF	**LNA, BPF, ADC**

*Requires off-chip capacitors
**Measured in different configuration

Table 3-2 summarizes the performance of the ECoG front-end described in this chapter as compared to state of the art designs from industrial and academic researchers [DEN] [YAZ] [VER] [BOH] [ZHA] [FAN]. Limited work has been done in the scope of ECoG, therefore the work is compared also to EEG and high-precision bio-signal acquisition front-ends, which have a similar set of specifications. By employing a digitally-intensive system similar to [MUL], and combining it with 1/f noise cancellation techniques, the area of the entire signal acquisition chain including the ADC is reduced to 0.025mm^2, over an order of magnitude smaller than the smallest ECoG/EEG amplifiers reported to date [BOH] [FAN]. State-of-the art noise efficiency is achieved and together with a reduced power supply this work achieves the best-reported PEF; 3 times lower than state-of-the-art designs [DEN] [ZHA]. The small area enables the highest degree of integration achieved to date in low-frequency high-precision bio-signal acquisition with a 64-channel array in only 1.6mm^2 of active silicon area with no external components required. The low supply voltage and a power-efficient design enable a highly scaled system with power levels easily achieved through wireless power coupling across a human skull, which will be discussed in Chapter 4.

CHAPTER 4: IMPLANTABLE PLATFORM FOR ELECTROCORTICOGRAPHY

4.1 Implantable 64-Channel Wireless µECoG System Description

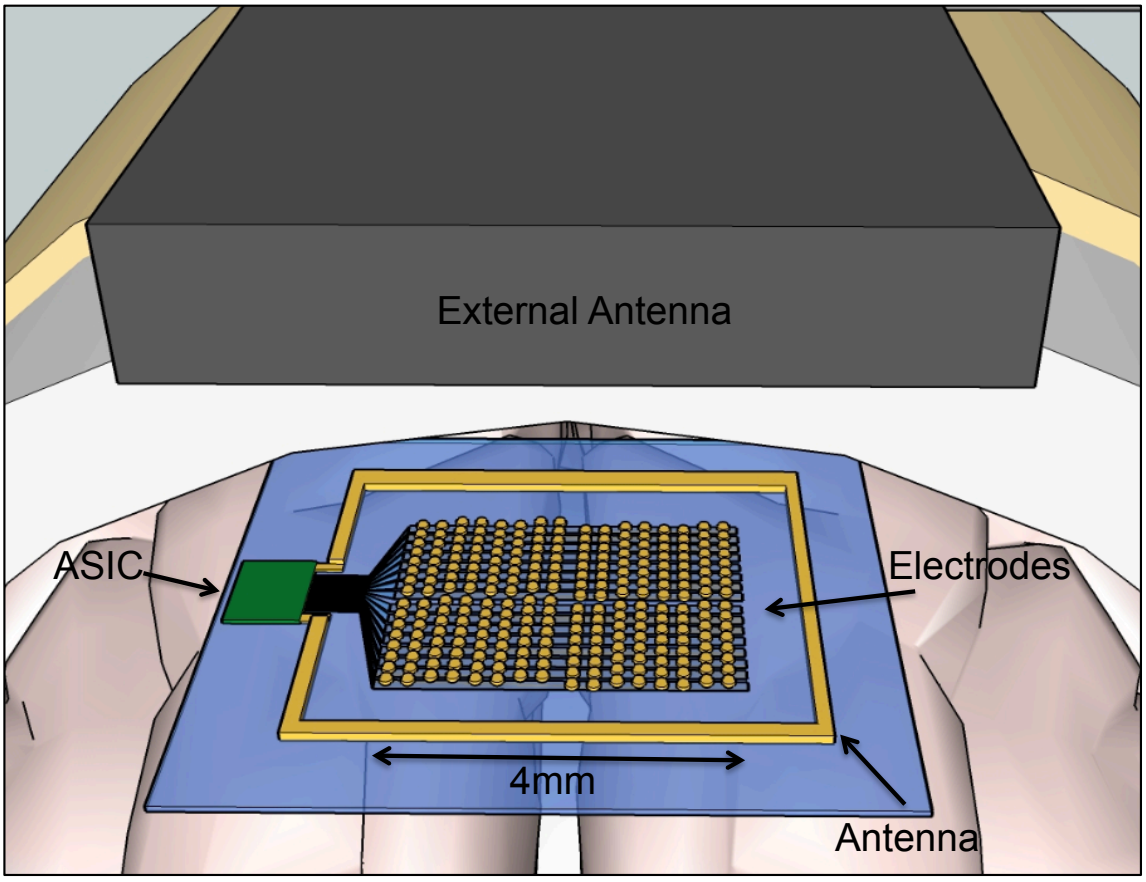


Figure 4-1: Wireless µECoG System Concept

The wireless μECoG device pictured in Figure 4-1 has four main components:

1. A micro-fabricated, sub-mm resolution ECoG grid for neural recordings. The device, designed by Peter Ledochowitsch, is manufactured using only materials that have been approved by the FDA for chronic implantation. Specifically, Parylene-C, which is a class-IV bioimplantable polymer used to insulate pacemaker wires, and platinum, which can be found in deep brain stimulator electrodes. The entire grid is less than 10μm thick and sufficiently flexible to conform to the highly folded cortical surface.
2. An application-specific integrated circuit (ASIC) capable of digitizing the voltage present on the electrodes with power efficiency more than 3x lower and an area more than 10x smaller than current state-of-the-art technologies can provide. The ASIC also integrates circuitry to receive power and to transmit the recorded neural signals wirelessly across the skull, removing the need for percutaneous plugs or ribbon cables.
3. The antenna used to couple wireless power and transmit data wirelessly across the skull is microfabricated together with the sensors in the same custom MEMS process. This allows for an antenna that is sufficiently large to achieve efficient power coupling, flexible enough to conform to the cortical surface.
4. An external reader that provides power to the implant and receives backscattered signals, which are decoded into a data stream.
5. A packaging process involving thermocompression bonding and thermal annealing to directly connect the integrated circuit to the sensor and to provide a highly biocompatible, hermetic seal.

While each part listed above has its own merit and design challenges, all five components must be present to realize a fully integrated platform for chronic neural recording.

The μECoG device takes advantage of recent findings to supersede current commercial and state-of-the-art research prototypes on three different aspects:

1. The wireless functionality of this system will liberate neuroscientists from the need to perform behavioral experiments on tethered animals, and allow them to work with loosely confined animals enabling novel experiments that benefit from continuous neural recordings and unrestricted animal locomotion. Closure of the surgical site will prevent infections and increase the stability of the neural recordings. Translated into the clinic, a wireless device will restore patient autonomy in addition to greatly reducing the risk of infection.
2. The use of non-penetrating ECoG electrodes in this system will substantially reduce the amount of scarring and other forms of tissue immune response, providing stable neural signals for multiple years as opposed to the few months of current practice.

3. The device uses polymer-based micro-fabricated μECoG electrodes that are up to 400 times denser than current state of the art. These electrodes allow researchers to sample neural signals with a spatial resolution comparable to penetrating electrodes, while increasing the longevity by orders of magnitude. The use of a flexible assembly further allows the device to conform to the brain surface.

4.2 Electrode and antenna design

A thin film antenna is monolithically integrated with an array of neural recording electrodes on a flexible polymer substrate. The structure is intended for long-term biometric data and power transfer for electrocorticographic neural recording in a wireless neural recording system. The substrate is comprised of a microfabricated thin-film electrode array and a loop antenna patterned in the same microfabrication process, on the same conductor layer. Fabricating the antenna together with the electrodes provides a small form factor, mechanical flexibility of the structure and minimal cabling to the active circuits enabling seamless integration of all electronic components.

4.2.1 *High-density microfabricated electrodes*

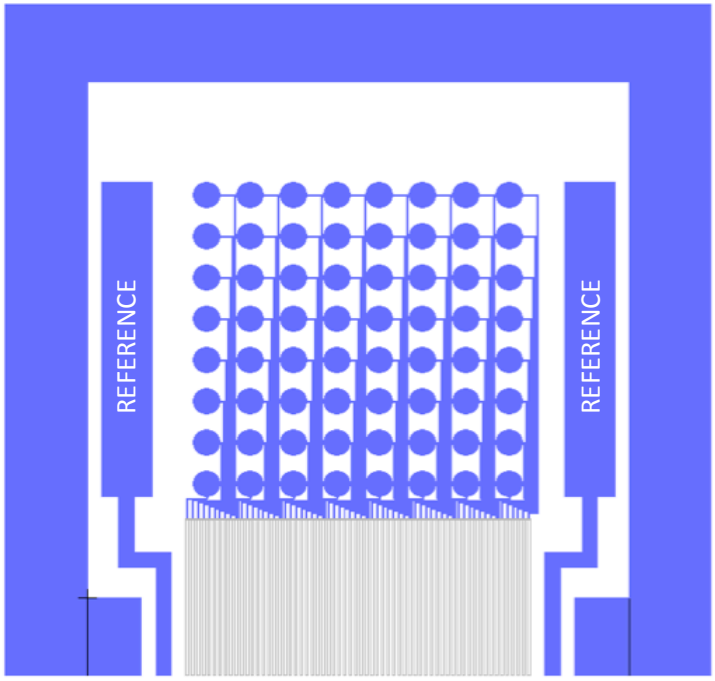


Figure 4-2: Metal mask layout of antenna and electrodes

The electrodes were fabricated in a single metal layer parylene-based process described in [LED]. Microfabricating the electrodes enables a high spatial density. 500μm pitch was chosen for the electrodes since human cortical columns are spaced at an approximate pitch of 500μm [MOU]. Spacing electrodes at much lower pitches will produce highly redundant data although it should be noted that ideal spacing of electrodes is an active area of research and that 500μm is a starting point and not an optimized figure.

A 4mm by 4mm, 64-channel array was chosen in order to cover a significant enough area of the cortex for experimentation. The electrodes have diameter 260μm and an electrode trace spacing of 20μm. The complete layout is shown in Figure 4-2. The electrodes were sized as large as possible, allowing space for routing. Two reference electrodes are patterned on either side of the array. The 64 recording channels each record with respect to this reference, therefore the impedance seen at the reference input is 64 times lower than the impedance seen by each recording channel. In order to balance this impedance the reference electrodes are sized with a total of 64 times the area of a single electrode. Their area is distributed on either side of the array in order to get a good average reference of the cortical area, which helps mitigate 60Hz noise.

4.2.2 *Microfabricated antenna*

The antenna is micropatterned onto a polymer thin-film together with the ECoG electrodes, thus enabling a larger antenna size while eliminating the need to implant a large rigid structure. The nanoscale thickness of the metallization allows the entire structure to be flexible and conformal. State of the art work on implantable antennas for neural interfaces has been focused on antenna miniaturization in order to minimize tissue scarring and immune response to the implant. This extreme miniaturization has been at the expense of link power efficiency, which drops sharply as the implant size is reduced below a few millimeters [RAB]. An alternative approach for miniaturization utilizes a larger diameter for the loop antenna but fabricates it on a thin, flexible polymer such that it conforms to the brain surface, keeping the implant rigid components small [BJO1] [BJO2]. This sub-section will discuss specific issues that arise from microfabricating a flexible thin-film loop antenna rather than general design considerations for implantable antennas, which are discussed in [BJO2], [RAB] and [ODR].

Simulations were conducted by Toni Bjorninen with ANSYS HFSS v13, a full-wave EM field solver, based on the finite element method. The simulation model is illustrated in Figure 4-3. It consists of a layered tissue model of the human head with frequency dependent dielectric properties given in [GAB], a segmented loop transmit antenna

[MAR2], and the single-turn loop antenna enclosing the array of 64 electrodes. To account for additional loss sources, the equivalent series resistance of the segmenting lumped capacitors (50mΩ) in the transmit antenna and the implant antenna bonding resistance (0.3Ω) were included in the simulation. The overall thickness of the Pt-Au-Pt conductor of the simulated and fabricated implant antenna is 200 nm.

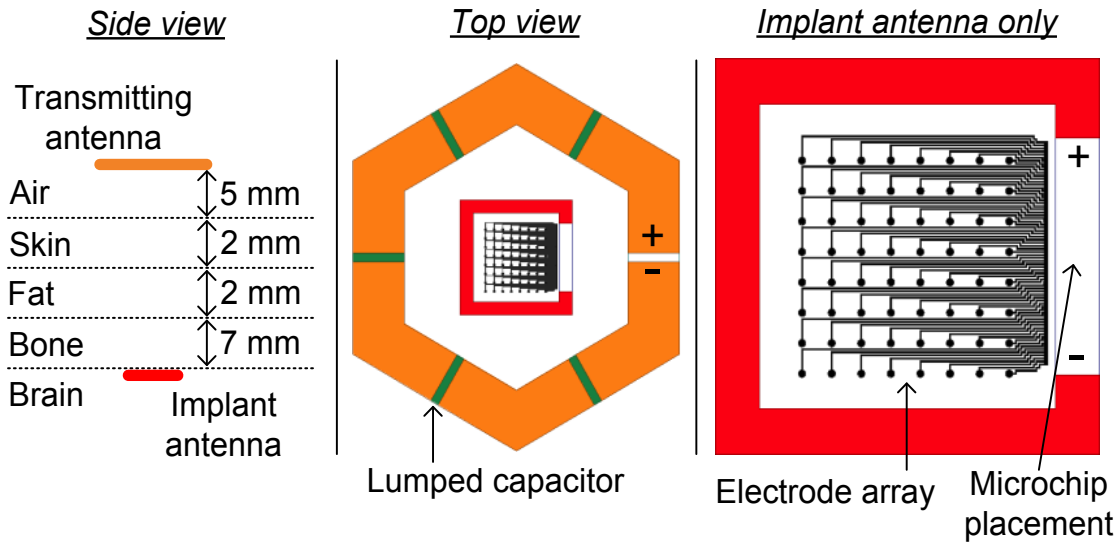


Figure 4-3: Simulation model of the wireless link

A single loop antenna was chosen for the implant geometry for ease of fabrication with the electrodes and simplicity of metallization. Since a single turn yields sufficient power for the implant, a multi-turn geometry was not considered for the device. The electrode dimensions determined the loop inner diameter of 5.5mm since the electrodes sit in the center of the conductor. A large gap is left in the antenna for microchip placement or routing of the electrode leads as shown in Figure 4-3.

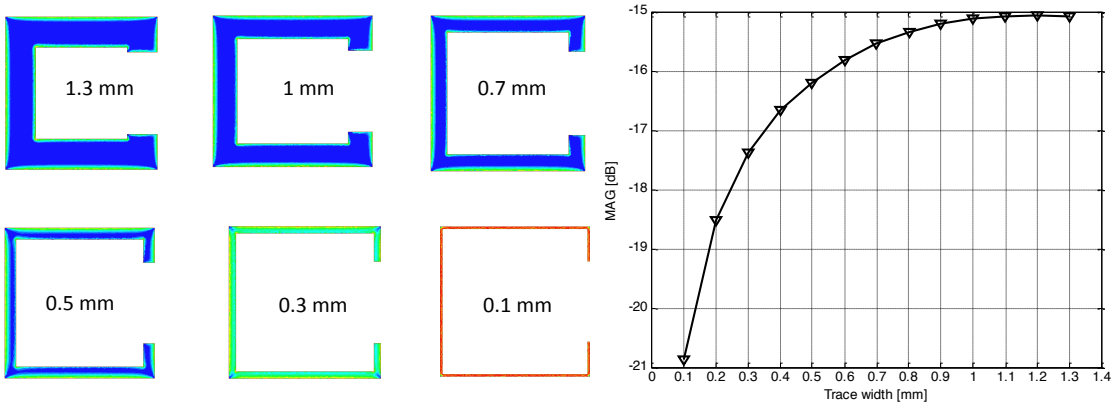


Figure 4-4: The effect of antenna width on link gain; blue=10A/m; green=25A/m; red=50A/m

The geometry of the device was designed to have minimal impact from conductor losses and other non-idealities associated with the implanted device. Careful attention was given to the loop trace width, since current crowding in this sub-skin depth conductor can affect the link gain. Figure 4-4 (left) shows a simulation of the current density profile on the surface of the implant antenna. Since current collects at the edges of the conductor, the minimum loss is incurred when the area of high current density becomes insignificant compared with the majority of the area of the conductor. A width of 0.7mm degrades the link gain by only 0.5dB and was therefore chosen for this design. A loss of 0.1dB can be obtained by increasing the width to 1.2mm at the expense of metallization area. The minor losses incurred illustrate that the benefit of having a large diameter outweigh the losses of the thin-film conductor.

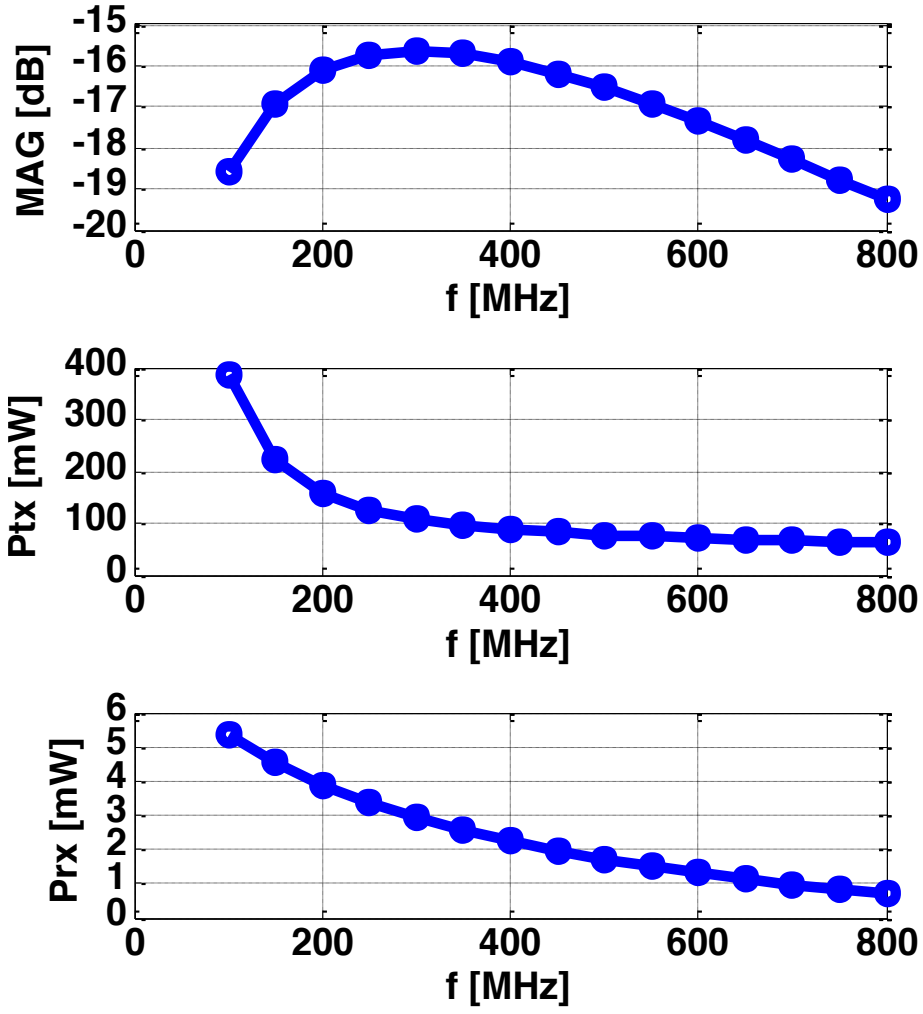


Figure 4-5: Wireless power coupling simulated performance vs. frequency: link gain (top), maximum transmit power (center), maximum receive power (bottom)

The final geometry of the implant antenna was simulated together with the previously described segmented-loop external antenna to determine the maximum possible received power using the human head model. Figure 4-5 shows the results of these simulations. The simulated link gain is shown at the top of the figure with a local maximum at 300MHz corresponding to -15.5dB unidirectional path loss. Since there is a wide local maximum any frequency between 200MHz and 400MHz would provide an energy-efficient operating point. 300MHz was chosen for this design. At 300MHz, the maximum RF power that can be transmitted safely into tissue, shown at the center of the figure, is slightly greater than 100mW, limited by the SAR of tissue and IEEE guidelines. Finally, the corresponding power received at the implant antenna, shown at the bottom of the figure, is 3mW. This received power is an order of magnitude greater than the power demands of the implant, allowing the power transmitted from the external device to be an order of magnitude lower, and thus remain well within safety guidelines.

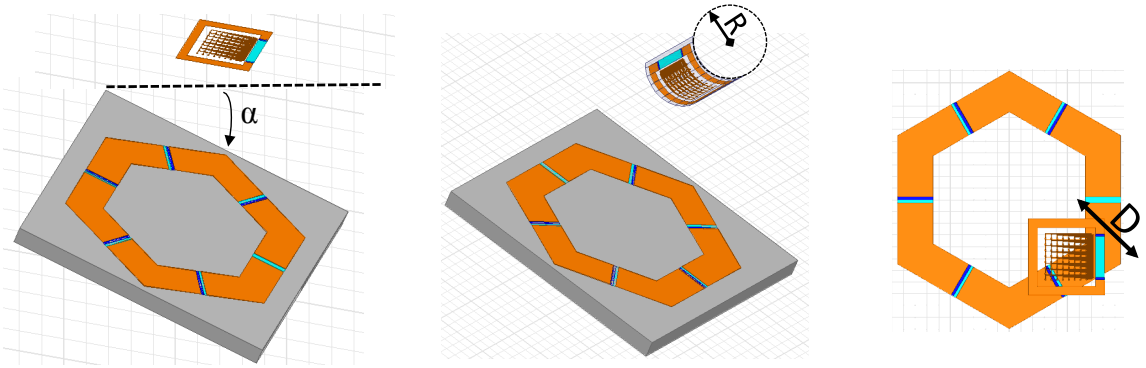


Figure 4-6: Non-idealities associated with patient implantation: tilt (left), curvature (middle), translation (right)

The implant environment creates non-idealities not just from tissue degrading the wireless channel but also from conformations and misalignments of the flexible implant antenna. Three error sources associated with implantation were studied and pictured in Figure 4-6: tilt, curvature and translational misalignment. A 3dB, or quarter-power loss is simulated for a tilt angle α=16 degrees, for a radius of curvature R=3mm and for a translation D=5mm with each error source simulated in the absence of the others. A tilt of 15 or more degrees is easily detectable by visual inspection, as is a 3mm radius of curvature (2mm radius forms a half-cylinder.) Therefore these error sources can be minimized during implantation. A translation of 5mm can be a difficult metric to keep within during implantation. Since the system operates well below maximum allowable RF power, an increase in incident power can be used to compensate for misalignment. To keep the implant from moving after implantation, the device can be sutured to the dura.

4.3 Integrated circuit

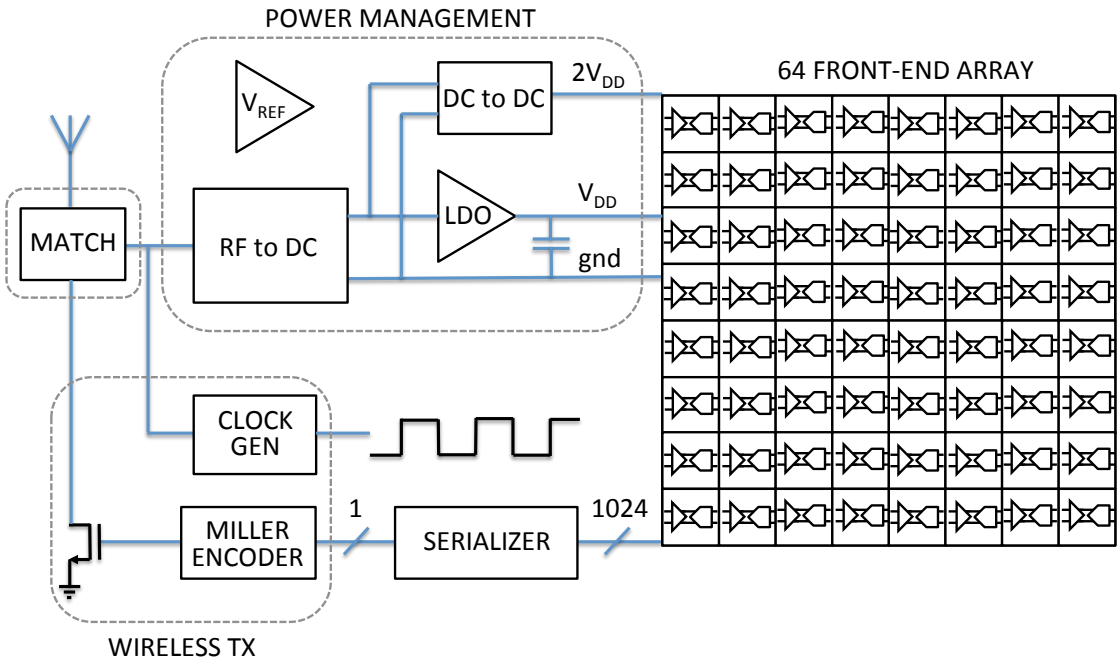


Figure 4-7: ECoG Chip Block Diagram

A block diagram of the integrated circuit is shown in Figure 4-7. The baseband signal acquisition consists of a 64-channel front-end array. 1kS/s, 16-bit digital outputs are serialized into a 1Mbps data stream. A current bias and clock distribution network are also implement on-chip. A wireless backscattering transmitter, designed by Wen Li, consists of a digital miller encoding of the serialized data stream, an antenna matching network and modulation switches. Clock recovery and division is implemented as part of the wireless sub-system. The power management unit, consist of RF-to-DC conversion, a low-dropout linear regulator (LDO) and a DC-to-DC converter that provide 0.5V and 1.0V to the chip respectively.

4.3.1 *Front-end array*

In order to transmit data through backscattering, the front-end outputs of the 64-channel array must be serialized into a single data stream. Although the front-end ADC has 12-bit resolution, each counter is implemented with 14 bits and the final output resolution after unwrapping the counters and subtracting the differential outputs is 16 bits. Therefore

each channel has a 16-bit output that must be serialized. The serializer, shown in Figure 4-8 consists of a shift-register that captures all data from every channel simultaneously each time there is a Pulse signal and sequentially reads it out at the CLK rate. Since 16 bits × 64 channels × 976Hz = 1Mbps, the 1MHz Delta-Sigma clock is used to clock the serializer generating the 1Mbps data stream. A pulse the width of one clock cycle is generated at the start of each sample in order to align the data readout. A timing diagram is shown in Figure 4-9.

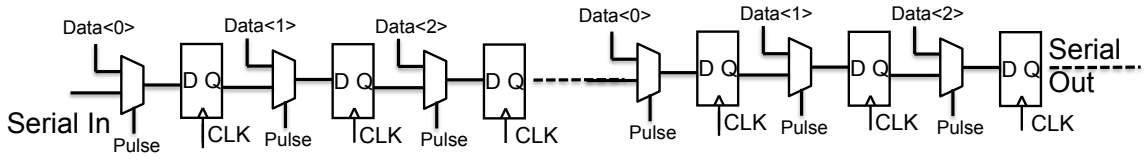


Figure 4-8: Schematic of front-end array serializer.

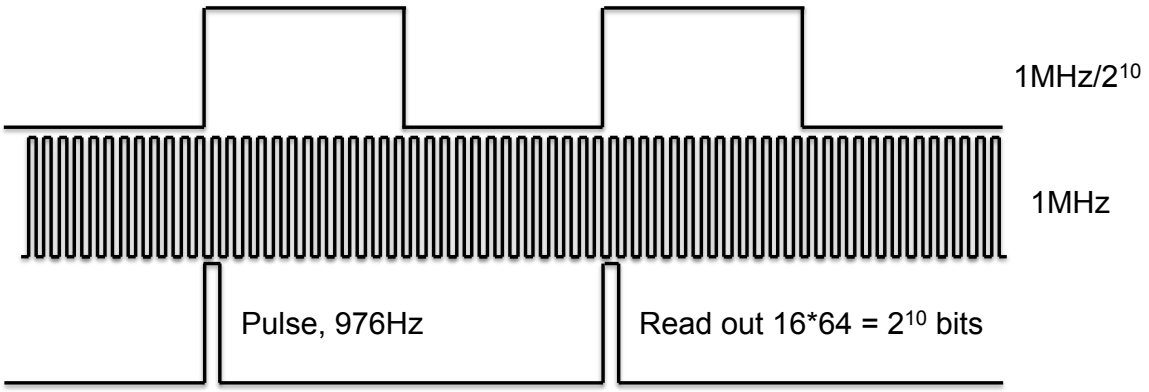


Figure 4-9: Timing diagram for front-end array serializer.

Front-end bias current generation is implemented as a standard CMOS supply-independent current bias circuit pictured in Figure 4-10. The current is referenced to the same unit-sized polysilicon resistance as is used in the front-end amplifiers. A wide tuning range is implemented to cover process variations. A skewed inverter and pull-down switch are used to ensure startup. A 64-channel current mirror distributes a 100nA bias current to each channel. Capacitance is added at to each of these branches to provide additional filtering of the 300MHz supply ripple. Due to the low supply voltage and high thresholds of the devices, the current mirrors are in weak inversion causing a standard deviation of 7% mismatch in these current mirrors. This mismatch contributes to the channel-to-channel gain variation and should be reduced in subsequent designs. The total power consumed by the bias network including current distribution is 3.45µW, adding an effective 53nW per channel.

A counter-based clock divider divides the 1MHz master clock and distributes a 1MHz Delta-Sigma clock, a 1kHz ADC clock and a tunable 1kHz-132kHz chopper clock to all the channels. The clocks are buffered and distributed to each channel using a clock distribution H-tree to balance the delays.

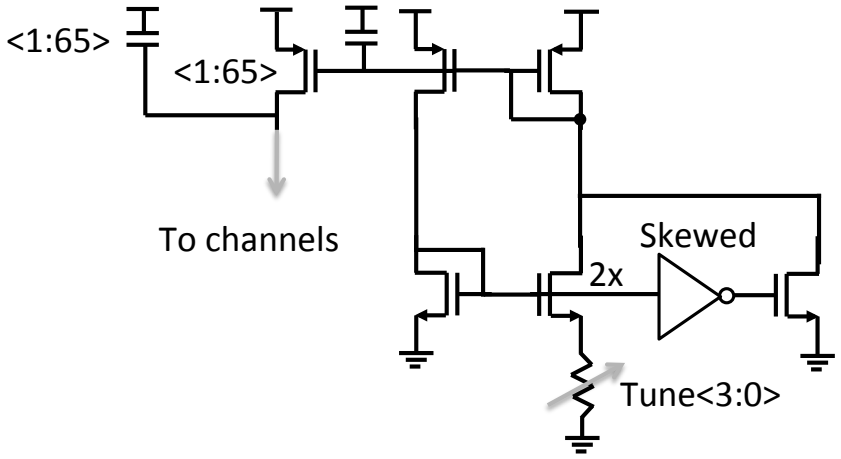


Figure 4-10: Current bias circuit diagram

4.3.2 *Wireless subsystem*

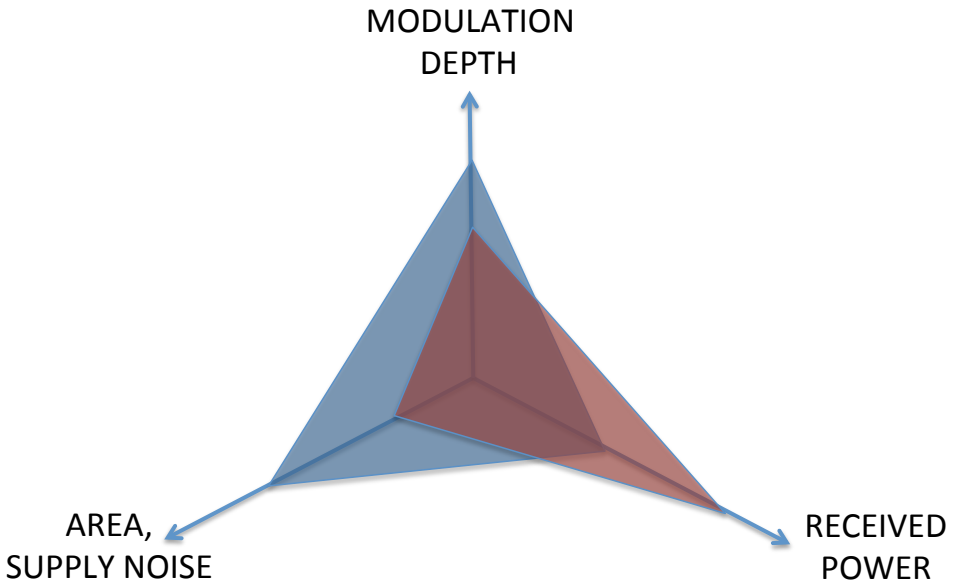


Figure 4-11: Wireless subsystem tradeoffs between duty-cycled data and power delivery (blue), and continuous data and power delivery (red)

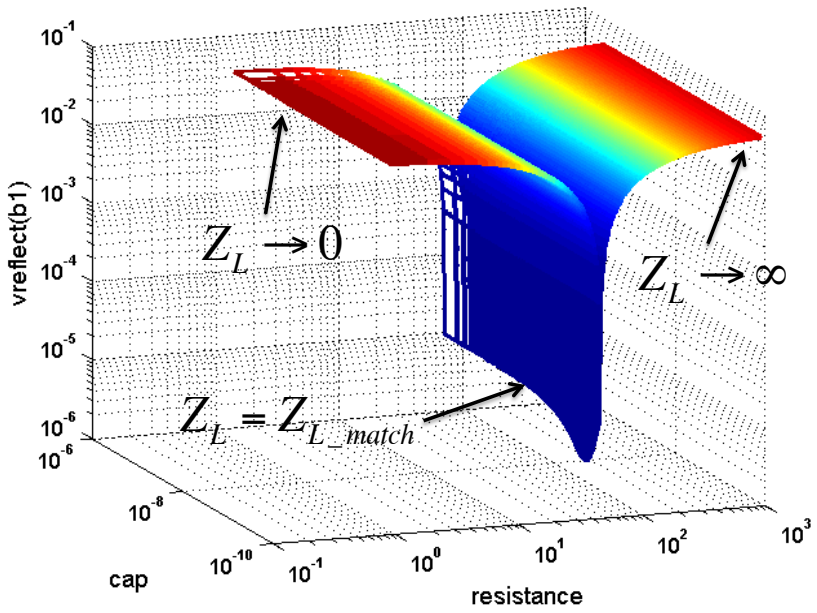


Figure 4-12: Reflection coefficient vs. matching network elements

The wireless sub-system of the μECoG IC shares many commonalities with and can be compared to an implantable RFID tag. An RFID tag uses electromagnetic field backscattering to transmit data in packets. The key difference between this system and an RFID system is that power and data must be delivered across the same link. Rather than using packet-based communication, this system aims to be constantly powered and transmit a continuous stream of data. Architecting the system in this manner avoids the need for large power storage capacitance and the need for on-chip data storage. The trade-off between duty cycling data and power vs. continuous data and power transmission is exemplified in Figure 4-11, where reducing modulation depth increases the received power and lowers the supply noise.

To illustrate this tradeoff, Figure 4-12 shows the amplitude of the reflected wave as a function of the matching network resistance and capacitance. The maximum reflection occurs when the load (Z_L) is either an open circuit or a short circuit while the minimum reflection occurs when the load is matched to the antenna impedance. To maximize modulation depth the matching network impedance can be modulated between a matched condition and an open or short circuit, however, when the antenna is either in an open or short condition power cannot be received and rectified. In order to receive power continuously the impedance of the matching network is modulated between a matched condition and a finite high impedance. While this results in a lower modulation depth, it allows the incident RF to be received on-chip and be rectified, resulting in continuous-wave power transfer with continuous data modulation.

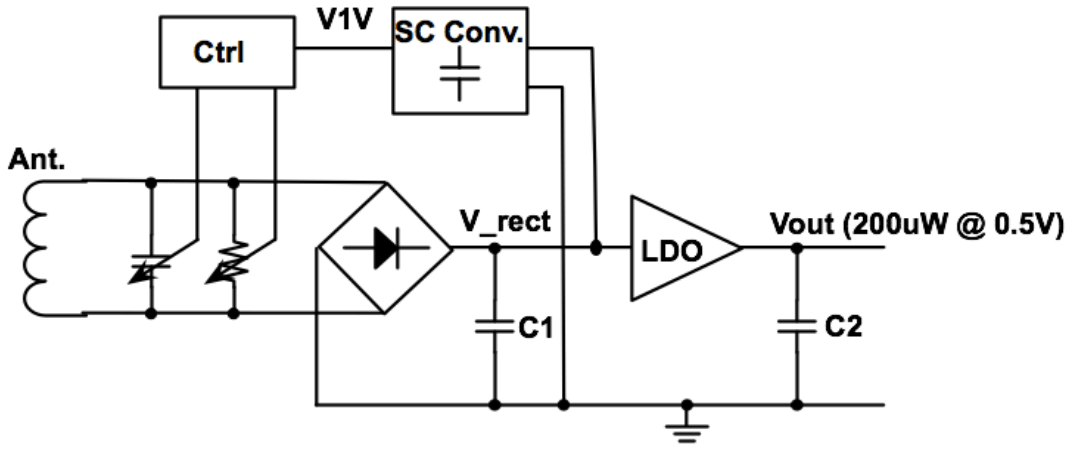


Figure 4-13: Power management unit block diagram

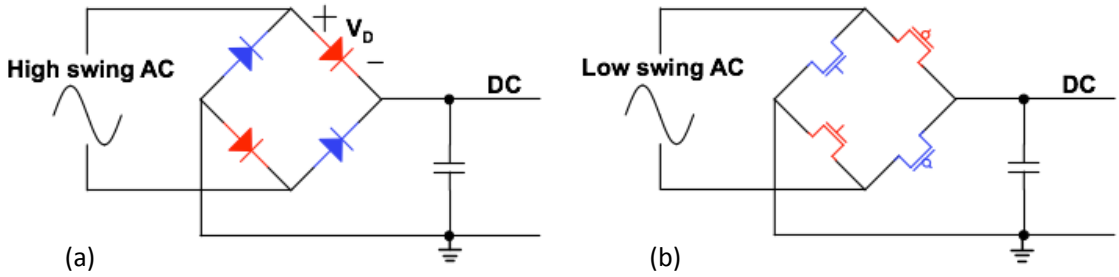


Figure 4-14: RF-to-DC passive rectifier (a) and active rectifier (b)

A block diagram of the power management unit (PMU), designed by Hanh-Phuc Le, is shown in Figure 4-13. An RF-to-DC rectifier, represented by the diode, converts the voltage seen at the antenna and matching network terminals. The output of the rectifier, V_rect, can have high voltage swings that correlate with the modulated matching network impedance, placing stringent constraints on the size of capacitor C1 and the PSRR of the low-dropout (LDO) regulator. The dual-mode rectifier shown in Figure 4-14 is used to mitigate these constraints. When the transmitter (Tx) is transmitting a logic 0, the matching network Z_L=Z_{L_match} and the voltage swing at the input to the rectifier is relatively low. In this condition an active rectifier is used to maximize the power conversion efficiency as shown in Figure 4-14(b). When the Tx is transmitting a logic 1, the resistance of the matching network increases, causing a high voltage swing at the rectifier input as shown in Figure 4-14(a). In order to maintain the same DC voltage at the output of the rectifier a passive mixer is used to drop the excess voltage across the diodes. This technique necessitates a 20x smaller decoupling capacitance than a single-mode rectifier for a supply voltage ripple < 1mVptp.

In order to maintain a good bit-error rate (BER) in the presence of decreased modulation depth, selecting an appropriate data encoding scheme becomes critical. Using standard on-off keying (OOK) places centers the data at the carrier frequency making it compete with carrier leakage caused by the transmitter and degrading system SNR, and thus increasing the number of bit errors. Miller, or Delay encoding [MIL] is a type of binary encoding that modulates the data away from the carrier frequency such that after down-conversion to base-band the finite carrier leakage that exists at DC can be filtered without affecting the data content. This technique is widely used in RFID and backscattering based systems and is preferred over other encoding schemes such as Manchester coding since the signal remains narrowband.

The matching network modulation switches must be able to exhibit a very low on-resistance; therefore a boosted 1V supply is used to drive the gates of these devices. The 1V supply is also used to drive the input switches of the front-ends. To provide this 1V, a switched-capacitor voltage doubler in the style of [LE] is employed. Since this supply provides power to switches, the ripple is a much less critical specification than for the main 0.5V supply. As such, no explicit linear regulation is employed. 20-phase interleaving is used to reduce the output ripple to < 10mVptp. Efficiency is not an important specification for this converter since it supplies < 100nW.

4.4 System integration

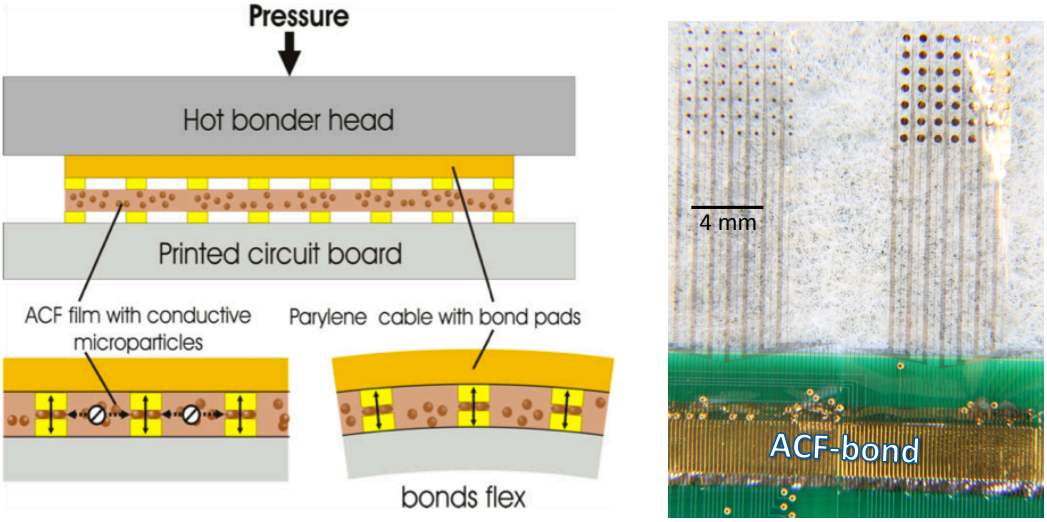


Figure 4-15: ACF bonding procedure, from [NAG] (left) and electrodes ACF bonded to a PCB (right)

Packaging is a key component to any implantable device and one that is often overlooked in an academic setting. For this system, a thermo-compression bonding technique has been adapted. The vision is to flip-chip bond the integrated circuit directly to the parylene substrate, avoiding fragile wire bonds and their encapsulation.

In the current implementation, anisotropic conductive film (ACF) bonding is used to connect the electrodes and antennas to printed circuit boards (PCBs). ACF bonding is commonly used to bond flexible cables in cellular phones, but is underutilized in biomedical applications. Figure 4-15 (left) describes the ACF bonding procedure. Pressure applied to polymer-coated gold microspheres in solution form a flexible conductive bond between electrodes by breaking down the polymer coating. Between the electrode pads, the polymer coating provides electrical isolation. A complete description of the procedure can be found in [LED2]. Bonding the electrodes and antenna to a PCB, rather than directly to the IC, enables full testability of all individual components. This type of bond is pictured in Figure 4-15 (right).

The bondpads that connect the electrodes to the PCB have dimensions 0.1mm by 2.5mm. A large area is used to ensure bondpad yield and robustness. ACF bonding has been demonstrated down to dimensions of 50μm by 50μm, making it compatible with standard integrated circuit bondpad dimensions.

4.5 System measurements

All components were assembled on a PCB for system testing as shown in Figure 4-16. The electrodes and antenna are monolithically integrated and ACF-bonded to a small PCB daughterboard. The daughterboard connects to a PCB testboard that houses the integrated circuit and peripheral testing components. Two versions of the PCB were designed, one with a test socket to test packaged die and another for chip-on-board (COB) direct chip attachment to the PCB to minimize parasitic elements for wireless testing. The antenna link was verified on a separate PCB for 3-point calibration and to further minimize parasitic components.

The chip power dissipation and active area occupation are listed in Table 4-1 with figures broken down by sub-block. The Tx power includes the power of the clock recovery and division while the FE Array power includes the power of the bias circuits and clock distribution. The power dissipation of the PMU indicates 65% power conversion efficiency, which is a result of 75% efficiency when converting in active mode and approximately 50% conversion efficiency in passive mode.

The total area occupied by the circuits is 1.72mm^2, which does not include the pad-ring area and the area utilized for decoupling capacitance and other test circuit structures such as the SPI. Approximately 4nF of 0.5V supply decoupling capacitance are integrated on the die utilizing the unused die area.

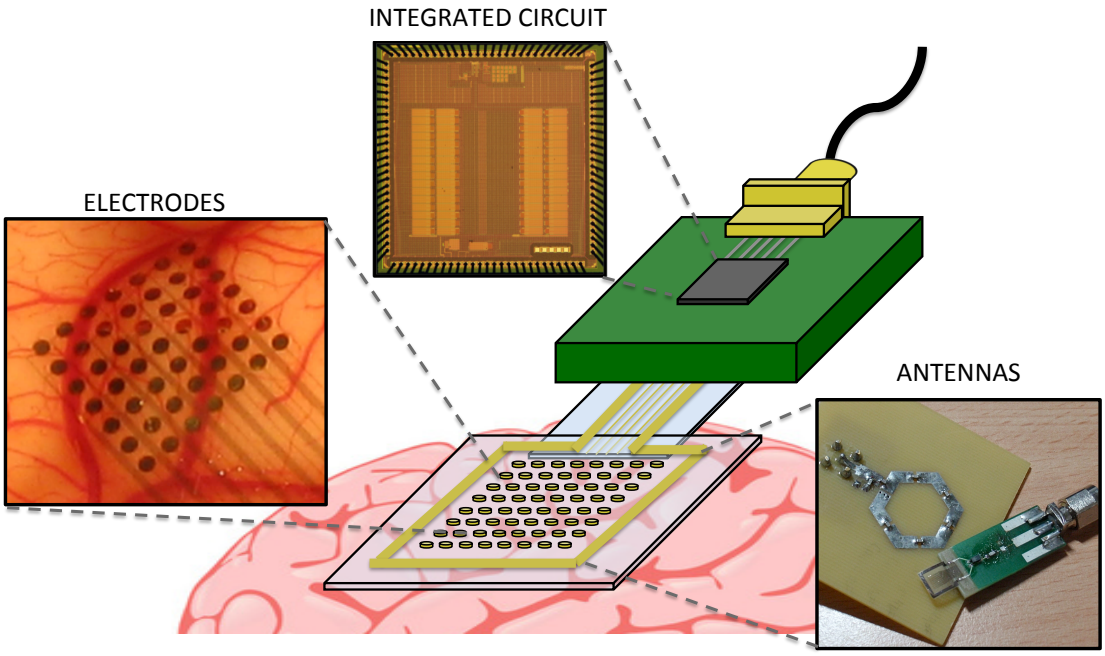


Figure 4-16: Measurement assembly and components

Table 4-1: Chip power dissipation and active area occupation

	Area (mm²)	Power (µW)
FE Array	1.6	147.2
Tx	0.03	13.9
PMU	0.09	51.5
Total	**1.72**	**212.6**

The wireless testing is performed using an Agilent signal generator and directional coupler. BER < 1.7×10^{-6} was measured at a 10mm antenna separation in air. BER < 2.1×10^{-5} was measured with the implant antenna at the surface of a dead chicken brain, covered by a 2mm slice of rat skull and 8mm of air. The measurements are limited by the amount of data content rather than errors and the true BER at these distances are likely to be lower than the previously stated numbers.

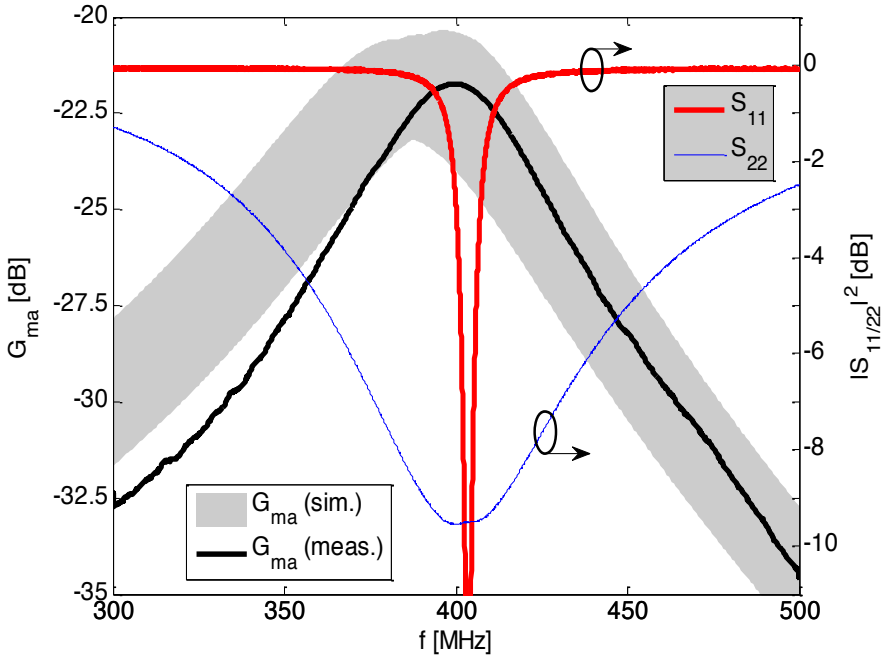


Figure 4-17: Measured and simulated link gain and reflection coefficients in air with a 2cm antenna separation [BJO2]

The measured and simulated link gain, G_{ma}, as well as reflection coefficients in air are shown in Figure 4-17. To fit the models the feeding fixtures were included in the simulation. The grey envelope of the simulation model accounts for the variability in capacitor tolerance, insertion loss of the balun and the implant antenna bonding resistance. Although the system was designed to operate at 300MHz, the antenna pair was matched and verified at 400MHz and showed good agreement at this frequency. The discrepancy at low frequency is related to the finite bandwidth of the transmit antenna matching network.

4.5.1 *Front-end array measurements*

Measurements were performed on the 64-channel array by connecting all inputs to a single signal source. The average forward-path gain of the entire chain to the ADC output was measured to be 1.4×10^6, or 123dB. The standard deviation of the channel-to-channel mismatch was measured to be 14%. The array gain was measured for each chip and mismatch was calibrated out during post-processing.

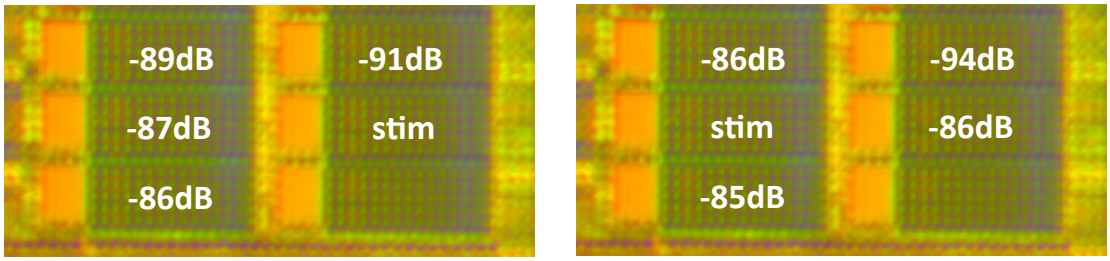


Figure 4-18: Crosstalk measurement configuration and results

Channel-to-channel crosstalk was measured in a group of five co-located channels pictured in Figure 4-18. One channel was stimulated with a 100mV in-band input while the inputs to all other channels were grounded. The measurement was repeated for two separate channels as shown in the figure. A worst-case crosstalk of -85dB was measured at the output of the adjacent channel. The robust channel isolation on chip means that crosstalk is likely to be limited by the electrodes and fabricated traces.

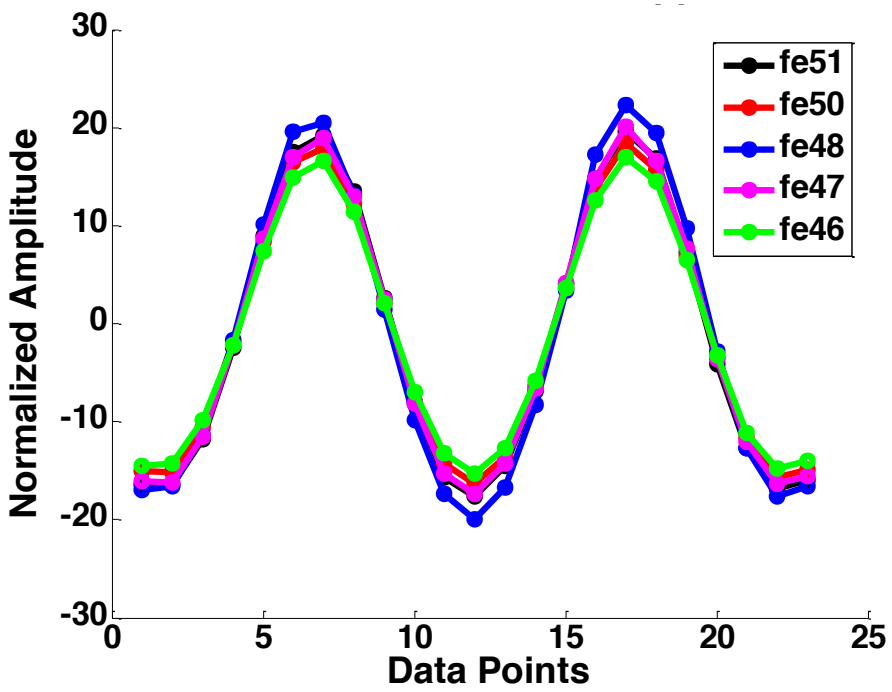


Figure 4-19: 1mVptp, 100Hz sine waves from 5 channels transmitted through wireless link

The front-ends were tested while powered by the PMU and showed no increase in the testchannel noise floor. The front-end circuits were additionally provided a 1MHz clock that was derived from the incident RF. Data from five of the front-end circuits was read out through the wireless link as shown in Figure 4-19. Twenty-five data points sampled

at 1kHz are shown demonstrating the ability to transfer data from the front-ends across the wireless link. The ADC output code is 100x the normalized amplitude plotted in the figure. An inaccurate and noisy signal source was used in this measurement; therefore the absolute amplitude of the signal is not an important component of the demonstration.

4.5.2 *In-vivo experiments*

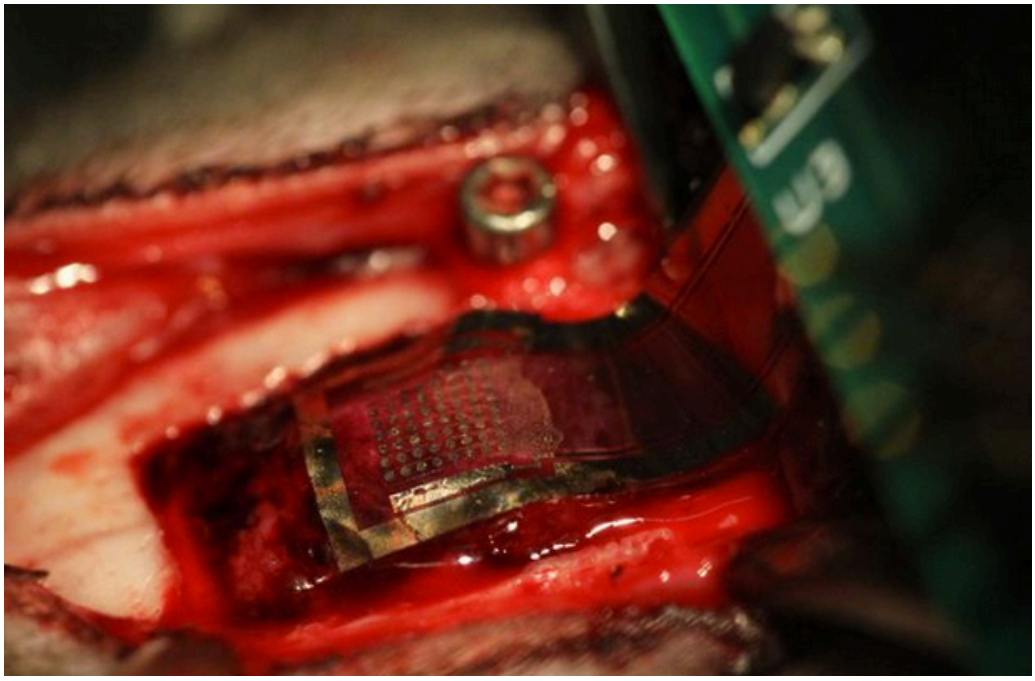


Figure 4-20: Photo of in-vivo measurement setup and grid placement

Data was taken in-vivo from an anesthetized rat. All experiments were performed in compliance with the regulations of the Animal Care and Use Committee at the University of California, Berkeley. Rats were implanted with micro-electrocorticography grids over the left cortical hemisphere. Stereotactic coordinates relative to bregma were used to center the arrays (anteroposterior -6 mm, mediolateral 3 mm). Rodents were anesthetized with Ketamine (50 mg/kg) and Xylazine (5 mg/kg) with supplemental isoflurance gas as needed. Craniotomies (approximately 10 mm x 7 mm) were made on the dorsal surface of the skull and the arrays were gently lowered onto the cortical surface. At the completion of experiments, euthanasia was delivered with an overdose of sodium pentobarbital (150 mg/kg) followed by bilateral thoracotomy.

The ECoG grid was lowered onto the cortical surface using micromanipulators, which suspended the PCB in the air above the head of the rat. The surgical setup is pictured in Figure 4-20. Bulging of the brain outside the incision site is visible and resulted in

substantial curvature of the grid. The excessive curvature resulted in several channels of non-viable recording.

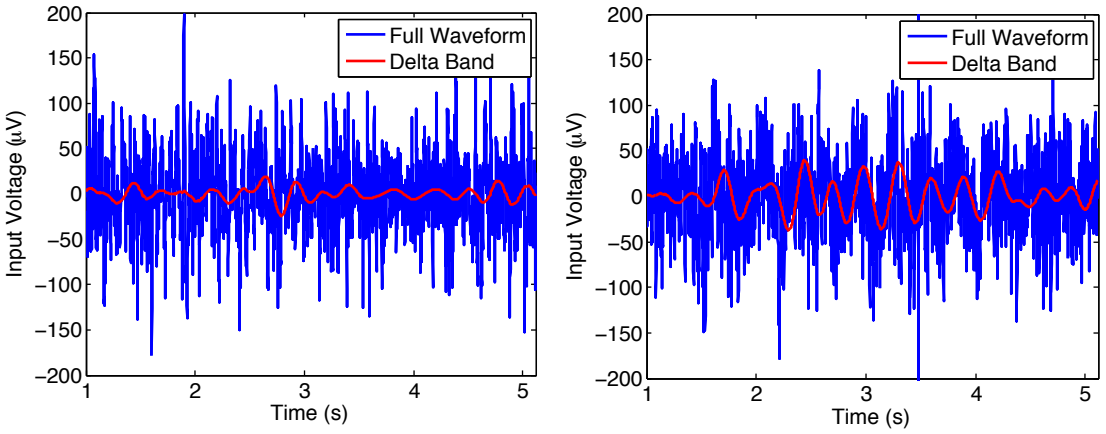


Figure 4-21: In-vivo neural recordings from the rat cortex taken in light anesthesia (left) and heavy anesthesia (right); filtered delta band is shown in red

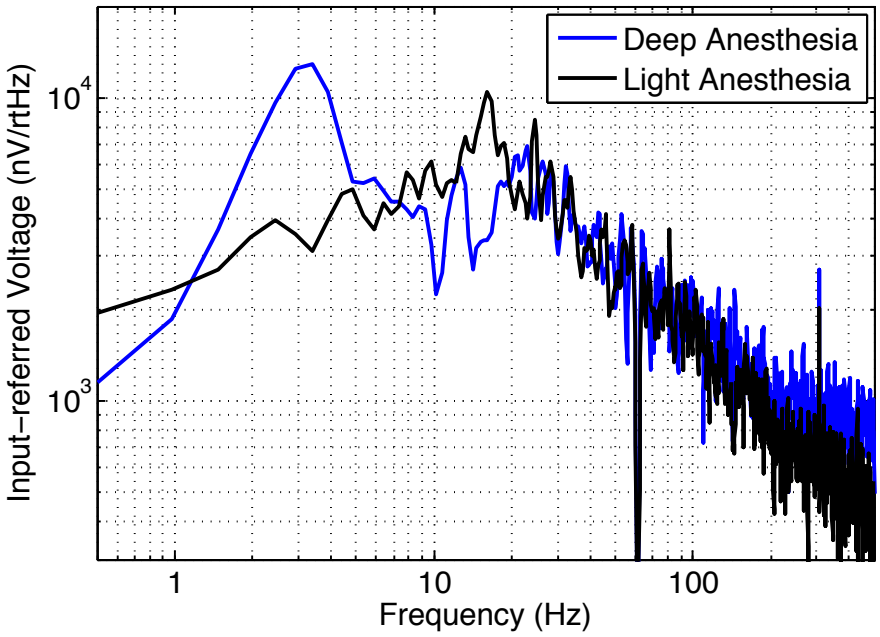


Figure 4-22: In-vivo voltage spectra in deep and light anesthesia

Recordings were taken in five-second increments every minute after an injection of Pentobarbital, an anesthetic. Figure 4-21 shows recordings from a single channel two minutes and twelve minutes after the injection. 60Hz noise, whose peak reaches 4×10^4 nV/rtHz, has been filtered out of both recordings. The full waveform is shown in blue and the bandpass filtered delta band is shown in red. Large amplitude delta oscillations, typical of deep anesthetic states are visible. Voltage spectra of the two recordings are

shown in Figure 4-22. The front-end was configured to have an 8Hz high-pass filter pole. The spectrum of the recordings is shown in the voltage domain to show the power and spectral difference with the noise spectral density shown in Figure 3-20. The delta power increase is over an order of magnitude and there is a decrease in alpha band power between light and deep anesthesia.

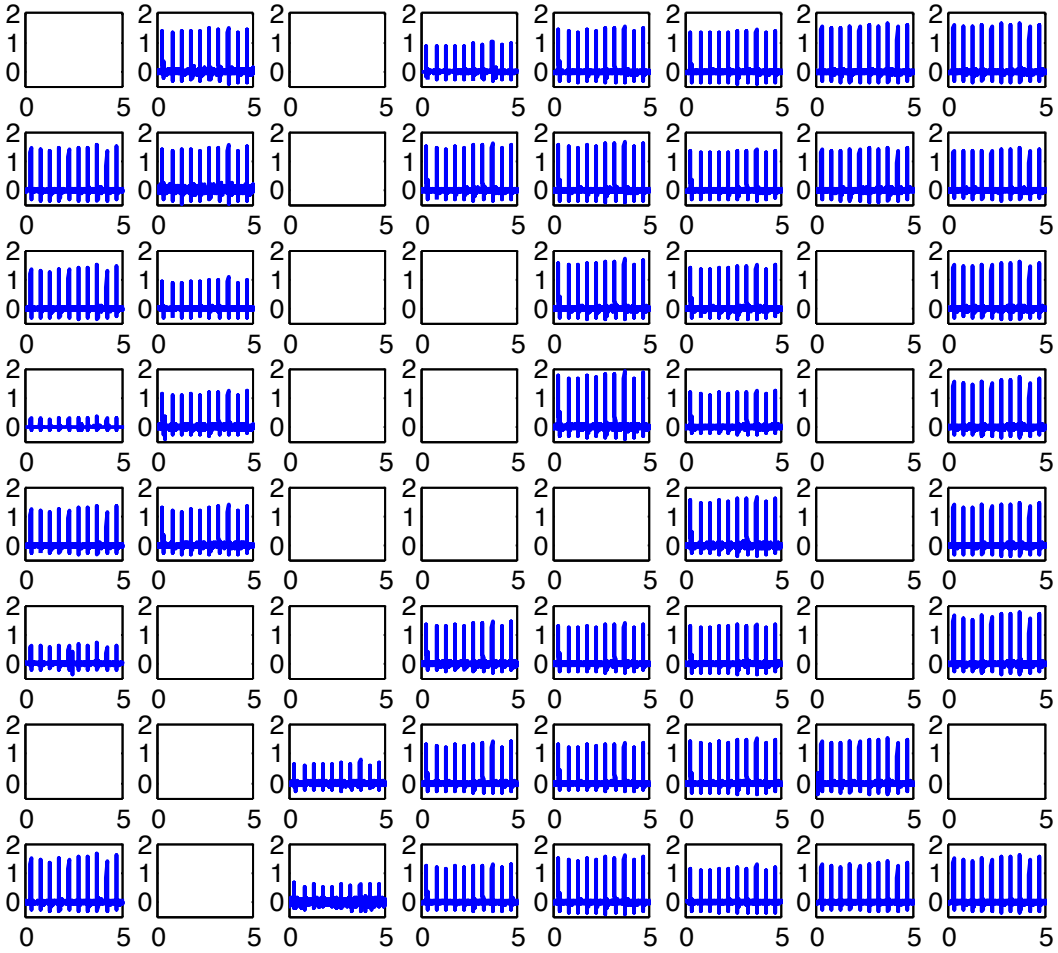


Figure 4-23: 64-channel microstimulation recordings, y-axis is shown in mV, x-axis is shown in seconds.

Prior to the Sodium Pentobarbital injection, intracortical microstimulation (ICMS) was performed. A microwire array was placed in the cortex at the top right corner of the grid with respect to Figure 4-23. 20μA monophasic current stimulation pulses were provided at 2Hz with 250μs pulse-width from a variable amplitude commercial stimulator, A-M Systems 2100. The pulse stimulator was connected to an array of 16 tungsten microelectrodes. Figure 4-23 shows the 64-channel recorded waveforms plotted corresponding to their grid location. Each channel was gain calibrated prior to recording. The channels with no waveform displayed are inactive and did not produce viable

recordings. There are several reasons for the large number of inactive channel: there are five channel inputs that make poor contact with the test socket resulting in an open-circuit input, there are 3 channels whose ACF bond was unsuccessful, and the rest are caused by excessive folding of the μECoG grid which resulted in a number of electrodes that do not make good contact with the cortical surface. The deformation of the grid can be observed in Figure 4-20.

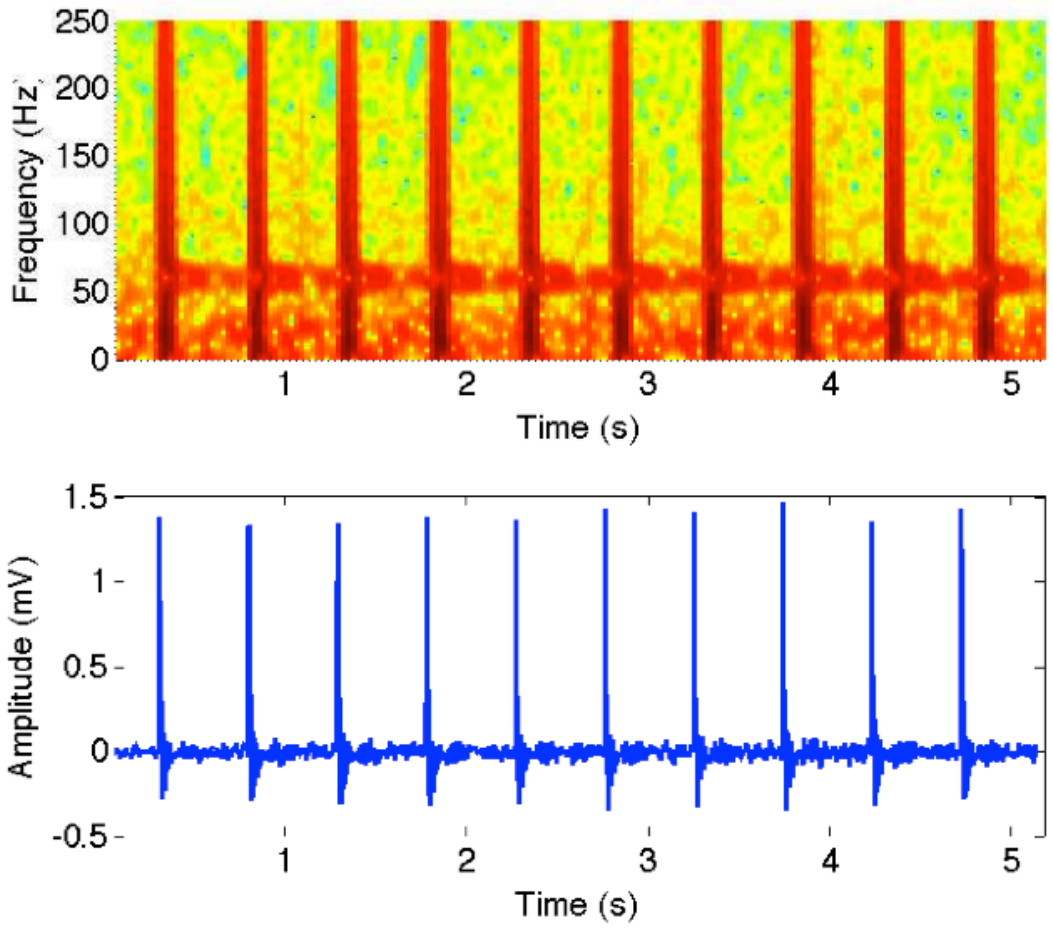


Figure 4-24: In-vivo recording of ICMS response in time-frequency spectrogram (top) and the corresponding voltage waveform (bottom)

The recordings of Figure 4-23 exhibit both stimulation pulse artifacts and a subsequent cortical response in addition to the baseline neural activity. Figure 4-24 shows the recording from one of these channels. The raw waveform is shown in the lower half of the plot while a time-frequency spectrogram is plotted in the upper half. There is a pattern of oscillations clearly visible even in the voltage domain, but which are emphasized as gamma-band oscillations on the time-frequency spectrogram. There is a strong increase of activity between 40-70Hz after each stimulation pulse. Cortical gamma oscillations have been observed as a result of optogenetic stimulation [SOH] and are thought to be a

result of exciting fast-spiking inhibitory interneurons. Since 60Hz is already notch filtered out of the recording, this increase is not a result of line noise and the oscillations were not reproducible in a laboratory environment without recording from the animal. Since oscillations persist for greater than the 0.5s inter-pulse interval, a lower stimulation frequency can be used to confirm the rate of decay of the gamma oscillations.

CHAPTER 5: CONTRIBUTIONS AND FUTURE WORK

Neural recording is a crucial tool for several emerging applications in prosthetics, disease therapies and even new human-computer interfaces which have the potential to completely revolutionize the way people interact with their environment. The design of electronic instrumentation for neural recording has enjoyed significant growth in the last 10 years, and will continue to enjoy similar attention in the years to come, as future cortical recording and stimulation systems will require the design of custom low power ICs incorporating high performance analog, power conversion and RF circuits. Pursuing the power consumption, lifetime and miniaturization challenges highlighted in this thesis and the many other challenges emerging in this field requires an innovative approach in several areas of circuit design. At the same time, these very challenges generate a unique opportunity for electrical engineers to impact the rapidly evolving fields of Neuroscience and Neuroengineering.

Compact neural acquisition systems are an integral part of future wireless brain-machine interfaces. The work described in Chapter 2 of this thesis combines DC-coupled inputs with an architecture that uses mixed-signal feedback for filtering and offset suppression to achieve a compact area, while providing per-pixel digitization and simultaneous LFP and spike recording. The architecture enables noise-efficient offset cancellation, and with a boxcar sampling ADC, to obtain state of the art performance in an energy efficient manner while requiring only a 0.5V supply.

The miniaturization and power efficiency of the action potential front-end architecture has paved two separate paths in the exploration of minimally invasive neural implants. One such avenue is the one described in Chapters 3 and 4 of this thesis: a scaled, wireless, ECoG-based recording system.

The wireless μECoG device will have a tremendous impact on the neuroscience research community. The brain activity mapping effort recently announced by the Obama

administration has a vision to not only advance the understanding of the brain, but to develop the tools required to do functional mapping and treat neurological disorders. This device will enable long-term chronic neural recording from truly freely moving animals and trigger new discoveries in neuroscience. The ability of the μECoG to produce dense electrode grids with long-term stability and wireless communication will accelerate the development of this vision by providing a completely new tool for gathering information relevant to neuronal functional mapping since high-density, untethered recordings from the cortical surface are currently unobtainable.

Beyond the neuroscience laboratory, the understanding of neuronal activity through functional brain mapping coupled with a minimally-invasive recording instrument will lead to numerous disease therapies such as treatments for epilepsy, Alzheimer's disease and ALS, as well as neural prosthetics such as motor and speech prosthetics. Translated into the clinic, the use of non-penetrating ECoG electrodes will substantially reduce the amount of scarring and other forms of tissue immune response, providing stable neural signals for multiple years as opposed to the few months of current practice. A miniaturized, wireless device will restore patient autonomy in addition to greatly reducing size of the craniotomy as well as the risk of infection. With the advantages highlighted above, a wireless μECoG device stands to become *the new standard instrument for chronic neural recordings* in the clinical human market.

The 64-channel module is a first demonstrator of a scalable, autonomous, wireless system for ECoG recording. The future directions to realize the vision of a clinically viable, implantable device are manifold:

1. Packaging: An implantable device must be realized in an autonomous and robust package that is hermetic. An external reader must also be packaged in a compact and lightweight format.

2. Physiological experimentation: Long-term stability of the device must be verified in a realistic environment, starting with long-term implantation in a rodent.

3. Scaling: A single module should be scaled to 100s to 1000s of electrode recording sites. This will initiate a new set of challenges such as how bring large numbers of input signals onto the chip and whether or not to stream out the full recorded waveform or whether to perform data compression to save communication bandwidth.

4. Neuromodulation: To have a complete bi-directional implant we must enable a way to "write in" to the brain. The μECoG implant can serve as a platform for

both electrical and optical stimulation. Additionally, the transparent substrate allows potential combination with optogenetics [DIE], an emerging technique in cortical stimulation, which would allow much higher selectivity of activation.

5. Clinical Translation: All materials must be proven biocompatible. A neurosurgical strategy for implantation, operation, alignment and operation must be developed.

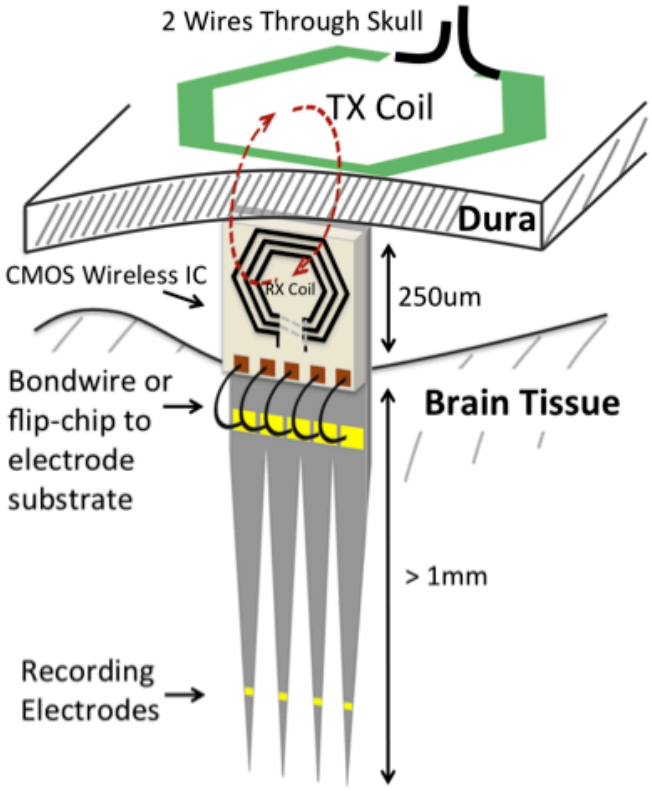


Figure 5-1: Conceptual diagram of a free-floating, miniaturized wireless neural sensor, from [BEI]

A second avenue of exploration in the search for a minimally invasive neural implant is the extreme miniaturization of intracortical recording. As discussed in Chapter 1, current intracortical recording electrodes generate scar-tissue formation and gliosis, which causes signal degradation on the timescale of months. A hypothesis that miniaturized, free-floating electrodes will not elicit the same response has emerged. A first step in proving this hypothesis was taken in [BEI], which demonstrated what is probably the world's smallest autonomous wireless sensor node and is pictured in Figure 5-1.

The entire interface of the miniaturized wireless neural sensor is integrated in 0.125mm^2 and consumes only 10.5µW. The four neural signal acquisition channels could only be

realized by utilizing the front-end architecture of Chapter 2. The entire node is wirelessly powered and employs backscattering communication. One major limitation to such a system is that the extreme miniaturization constrains the antenna into a form factor that is highly inefficient: 50mW are required to power the node at 1mm range in air. This large channel loss over such a small distance makes the required power levels impractical for human implantation.

One potential vision going forward is to combine a flexible platform that sits at the cortical surface with "free-floating" intracortical sensors that are connected through a flexible tether. This vision is exemplified in Figure 5-2.

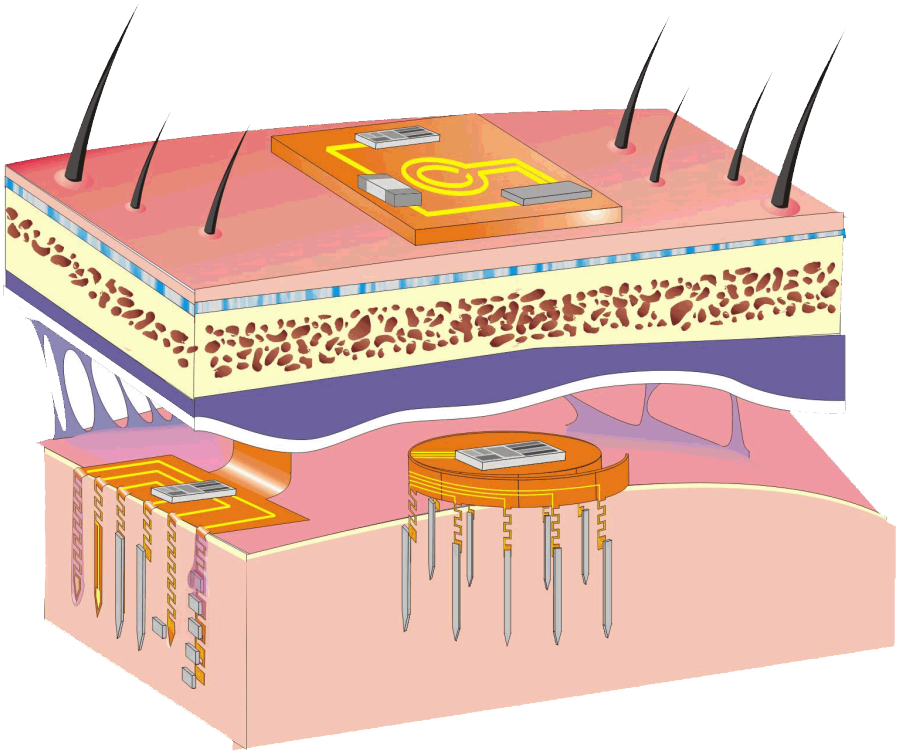


Figure 5-2: Flexible intracortical implant

Looking forward, it is difficult to predict how functional neural readout will evolve. Novel materials and chemical sensors can completely change the form in which the data is acquired while new energy scavenging techniques can enable zero-energy, or energy-neutral sensors. The only thing that is certain today is that Medicine and Engineering are starting to converge on ways to integrate technology with the human body. This slow but inevitable convergence will drastically change the structure of healthcare and even the face of society.

APPENDIX A: POWER EFFICIENCY FACTOR DERIVATION

As first described in [STA], the Noise Efficiency Factor (NEF) describes how many times the noise of a system with the same current drain and bandwidth is higher compared to the ideal case. The ideal case is that of a single ideal Bipolar Junction Transistor (BJT). This work proposes a new metric called the Power Efficiency Factor (PEF) which holds the same variables constant but looks at how many times the noise *and power* of a system are higher than the ideal case, thus taking into account supply voltage scaling.

Ideally both the input-referred noise power ($V^2_{n,rms}$) and the total power consumption (P_{tot}) of the circuit are to be minimized; therefore the metric must take the product of the two values:

$$\min(V_{n,rms}^2 \cdot P_{tot}) . \tag{A-1}$$

The value is then normalized to the noise power times the total power consumption of a single BJT with supply voltage V_{CC} and total current I_C.

$$PEF = \frac{V_{n,rms}^2 \cdot P_{tot}}{V_{n,rms,BJT}^2 \cdot P_{BJT}} \tag{A-2}$$

which can be rewritten as

$$PEF = \frac{V_{n,rms}^2 \cdot V_{DD} I_{tot}}{V_{n,rms,BJT}^2 \cdot V_{CC} I_C} \tag{A-3}$$

Since $I_C = I_{tot}$ the equation is further reduced to

$$PEF = \frac{V_{n,rms}^2 \cdot V_{DD}}{V_{n,rms,BJT}^2 \cdot V_{CC}} . \tag{A-4}$$

Further, V_{CC} can be assumed to be 1V since it is simply a normalization factor and can at most result in a uniform scale error. Therefore it can be shown by definition that

$$PEF = \frac{V_{n,rms}^2 \cdot V_{DD}}{V_{n,rms,BJT}^2} = NEF^2 V_{DD} . \tag{A-5}$$

According to [STA] input-referred noise power of a BJT is defined as

$$V_{rms,in,BJT}^2 = BW \cdot \frac{\pi}{2} \cdot \frac{4kT \cdot kT/q}{I_C} = BW \cdot \frac{\pi}{2} \cdot \frac{4kT \cdot kT/q}{I_{TOT}} . \tag{A-6}$$

Thus the complete definition of PEF becomes

$$PEF = \frac{V_{n,rms}^2 \cdot 2P_{tot}}{\pi \cdot kT/q \cdot 4kT \cdot BW} . \tag{A-7}$$

Note that the metric is now dependent on the total power of the circuit rather than the total current in the circuit.

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