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Publication Date

2023-06-28

DOI

10.1109/compel52896.2023.10221058

IEEE 24th Workshop on Control and Modeling for Power Electronics

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Abstract — Hybrid switched capacitor converter (HSCC) topologies have found use in high-density power delivery applications, such as 48 V to Point-of-Load (PoL). Of this family, Dickson-type converters are recognized as having the lowest Volt-Amp switch stress, indicative of a smaller semiconductor footprint for equivalent performance. However, some of these topologies require a non-conventional clocking scheme — termed "split-phase" switching — to ensure that capacitor-induced hard-charging losses are avoided. A small number of recent works have analyzed split-phase switching with varying degrees of rigor, however, to date no closed-loop active control scheme has been demonstrated. This work presents a hardware implementation of closed-loop split-phase control, eliminating both hard-charging losses and reliance on modelled converter operating points, while providing an increased degree of immunity to component mismatch. Capitalizing on periodic low-noise switching states in which flying capacitors are inactive, a low-cost and high accuracy analog front-end is used to converge on optimal split-phase timing durations while maintaining output voltage regulation, irrespective of load.

I. Introduction

Soft-charged switched-capacitor networks [1], [2] have demonstrated extremely high performance in recent years (e.g. [3]–[11]), owing to both the superior energy density of capacitors versus magnetics [12] and to their circumvention of the slow switching limit (SSL) [13] through elimination of hard-charging losses [1] which have historically thwarted broad adoption of purely capacitor-based designs. Additional analytical techniques, optimization efforts, and improved control methods have further developed this design space in recent years (e.g., [14]–[20]). Subsequently, hybrid switched capacitor converters (HSCC) have found use in direct 48 V to point-of-load (PoL) applications (e.g., data-centers and high-performance computing) where a high-density and conversion ratio converter with regulation enables the retention of high voltage transmission as close to the load as possible — thereby reducing I^2R losses.

Among HSCCs, ladder-type topologies including Cockcroft-Walton and Dickson-type are generally regarded as achieving the best total Volt-Amp (VA) switch stress, ideally resulting in reduced total converter die area and/or losses for equivalent converter performance [13], [17], [18], [21][1]. Use of such structures in PoL applications has therefore received much attention, with both academia and industry further pursuing monolithic integration (e.g., [22], [23]).

[1]As noted in [21], this conclusion relies on near-linear scaling laws of switching devices and may vary with technology.

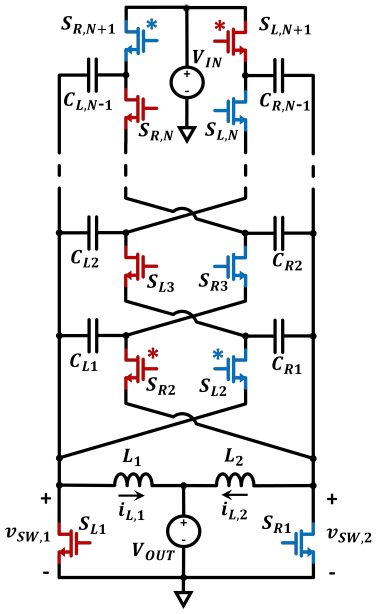


Fig. 1: The Dickson-type symmetric dual inductor hybrid (SDIH) converter [8], [16], [24]. Provided all capacitors are set equal; switches marked with asterisk '*' require split-phase switching [29] to ensure complete soft-charging of all flying capacitors.

One such power converter topology is the symmetric dual inductor hybrid (SDIH) converter introduced in [8], [16], [24] and depicted in Fig. 1. This topology benefits from an inherently interleaved high-side port and a greatly reduced component count when compared with dual interleaved instances of both the series capacitor buck (SCB) converter [25]–[28] and the dual inductor hybrid (DIH) [4] converter, while exhibiting a near identical VA switch stress rating.

However, both DIH and SDIH converters typically require modification to their clocking schemes in order to ensure that capacitor-induced hard-charging loss is avoided. Fortunately, this may be achieved using an established "split-phase" clocking scheme, first introduced in [29] for the Dickson converter, and subsequently discussed in [4], [7] for DIH converters. This technique is depicted in Fig. 2 for the SDIH topology when operated as a step-down converter. Here conventional phases 1 and 3 are each split into sub-intervals A and B. The relative timings of these sub-intervals needs to be controlled as

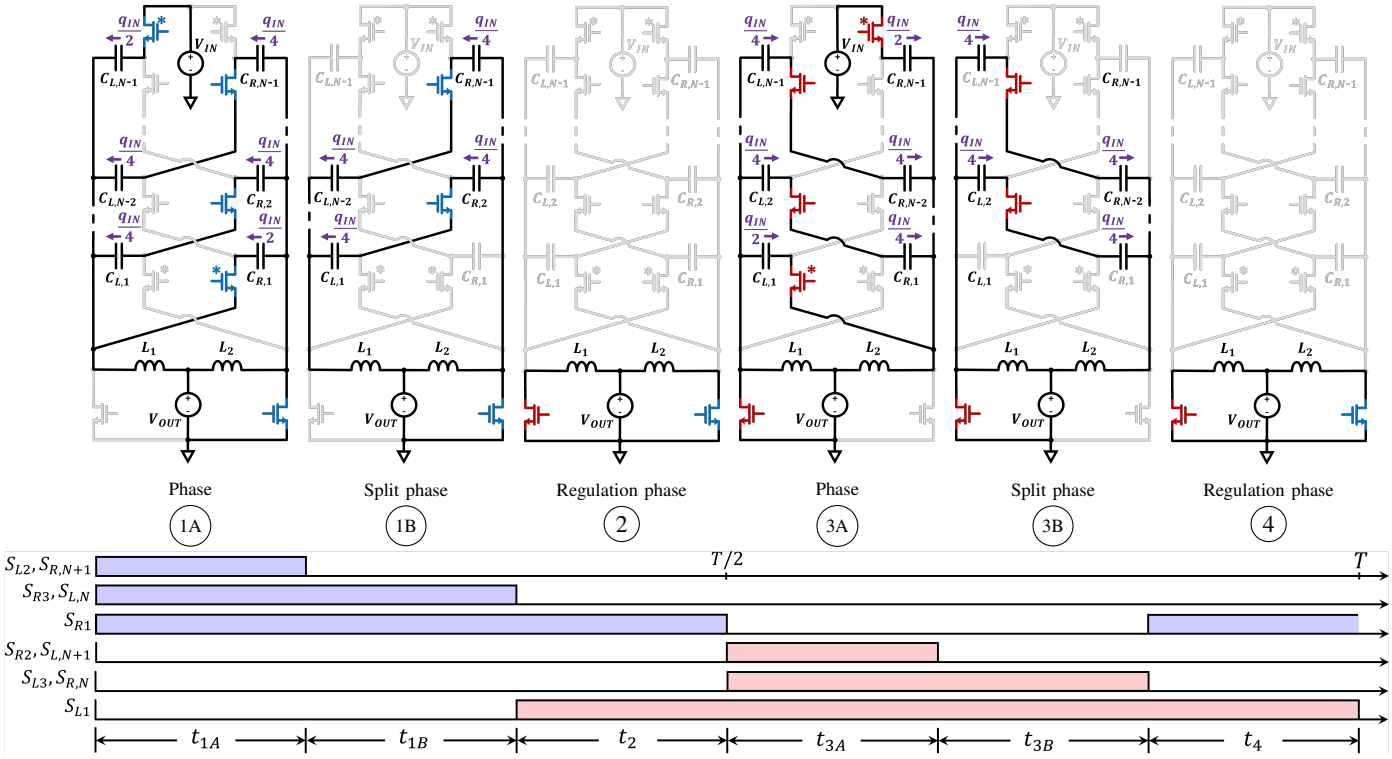


Fig. 2: Periodic phase progression of the SDIH converter (left to right) when optimized for step-down split-phase operation and where all flying capacitors are equal in value. Phases 1 and 3 are split into sub-intervals, A and B, to facilitate split-phase switching [17]. The four switches requiring split-phase operation are marked with an asterisk (*) and reside only at the extreme ends of the switched-capacitor network, for all $N \geq 3$. Charge flow through each flying capacitor is annotated and expressed relative to the total periodic input charge quantity q_{IN} that is admitted during phases 1A and 3A.

a function of load in order to maintain complete soft-charging and elimination of hard-charging losses. Moreover, as shown in Fig. 2, the insertion of phases 2 and 4 (where inductor's switched-nodes are shorted to ground) allows output voltage regulation between 0 V and $V_{IN}/2N$, where N is the order of switched-capacitor network employed. Previous work in [4], [24], [29] provides analytical solutions to split-phase timings with varying degrees of simplifying assumptions. However, in this work, rather than relying on modelled operating points, we instead present a demonstration of active closed-loop split-phase control, allowing automatic convergence on the correct clocking scheme irrespective of load while also preserving output voltage regulation.

The proposed method is applicable to regulating converters where flying capacitor voltage sampling can take place during quiet regulation switching states (e.g., phases 2 and 4 in Fig. 2). During these intervals the flying capacitors are disconnected from the power path and hold a constant voltage, easing sampling bandwidth requirements. Conversely, recent work in [30] has proposed a more involved controller front-end which further enables active split-phase control in resonant topologies where capacitor voltage discontinuities are measured directly using a high-bandwidth slope detect.

The remainder of this paper is organized as follows: Section II describes the conditions necessary to ensure soft-charging with split-phase control and proposes the design of an analog front-end that facilitates appropriate sensing for feedback control. Section III validates the proposed control scheme in hardware, demonstrating results which accurately match theoretical predictions. Section IV concludes this work.

II. Split-Phase Control

Introduced in [29], split-phase operation has been adopted in high performance HSCC topologies (including non-Dickson type, e.g., [31]) where it can ensure complete soft-charging of all flying capacitors while using a minimum number of magnetic components (supported by magnetic scaling laws posed in [32]).

One crucial element to correct split-phase operation — and the elimination of hard-charging loss — is application of the correct relative timing durations within a split phase. That is, while the total duration spanning both phase 1A *and* 1B may remain constant — affecting the converter's conversion ratio — the required relative duration of phase 1A to 1B is instead a function of both load (I_{OUT}) and voltage and current

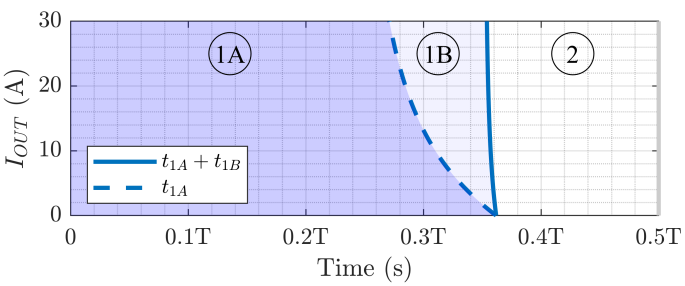


Fig. 3: Calculated split-phase timings as a function of load, expressed as a fraction of the full switching period, T. Phase intervals 3A, 3B, and 4 have identical timings to phases 1A, 1B, and 2, respectively, albeit with a 180° phase shift. $V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, $N = 6$, $f_{SW} = 300$ kHz, $C_0 = 496$ nF, $L_1 = L_2 = 330$ nH.

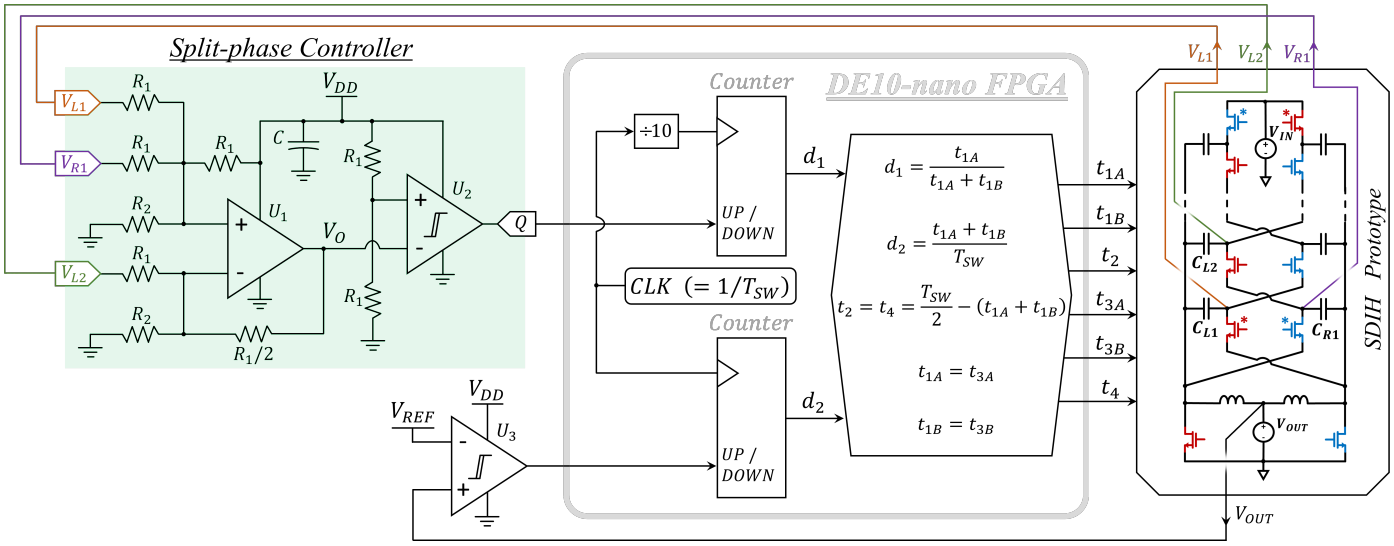


Fig. 4: Diagram of the closed-loop split-phase and regulation control scheme applied to a prototype SDIH converter. The split-phase controller employs a summing/subtraction op-amp, U_1, with subsequent comparator U_2 informing the digital hysteretic controller whether to increase/decrease relative phase durations. An additional comparator is included to facilitate primitive output voltage regulation.

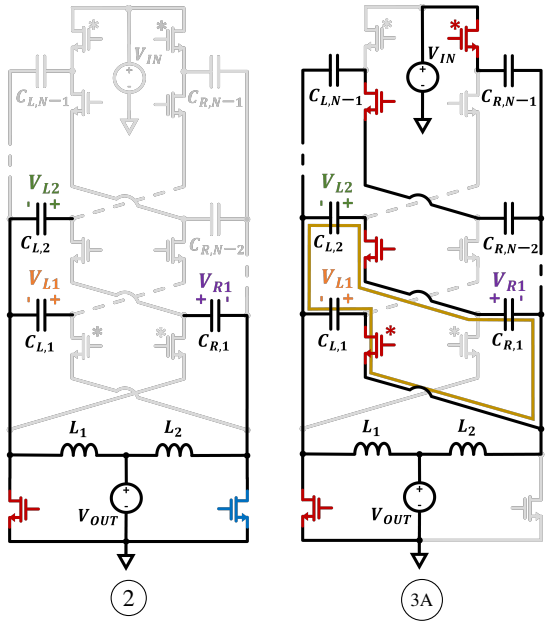


Fig. 5: Capacitor voltages V_{L1}, V_{R1}, and V_{L2} are static and unchanging during phase 2 (left), allowing their measurement using a low-bandwidth analog front-end. These capacitors form a voltage loop (highlighted) upon commencement of phase 3A. Thus; measurements taken during Phase 2 can be used to determine whether KVL will be satisfied come Phase 3A.

ripple on flying capacitors and inductors, respectively. Using the analysis presented in [24], Fig. 3 depicts this timing dependency as a function of load current for a specified set of passive components. While such analysis is useful for design, closed-loop control is desired in practical converter implementations to accommodate component mismatch and derating with age, temperature and bias.

In order to acquire a control input by which this timing scheme can be actively tracked in hardware, it is necessary to consider the source of hard-charging loss in practice. Consider the transition between phases 2 and 3A, depicted separately in Fig. 5. Here capacitors C_{L1}, C_{R1}, and C_{L2} form a KVL loop (highlighted) upon commencement of phase 3A. Correct split-phase control will ensure that this KVL loop is instantaneously satisfied, precluding any transient in-rush currents and hard-charging loss. That is, at the start of phase 3A, capacitor voltages should satisfy

$$V_{L1} + V_{R1} - V_{L2} = 0. \tag{1}$$

We note that these same capacitor voltages are constant during the entirety of the preceding phase 2, with the bottom-plate of all three capacitors referenced to ground. Thus minimal low-bandwidth single-ended sensing circuitry may be employed during phase 2 to evaluate the equality in (1), with the result informing control action on the subsequent clocking cycle.

A. Split-phase controller (Analog front-end)

Figure 4 depicts an example active split-phase control solution, including an analog split-phase controller, where a $V_{DD}/2$ offset is introduced to relax constraints on the common-mode input range of both amplifiers. The op-amp output, V_O, is described by (2), where the second term contains the desired KVL equality:

$$V_0 = \frac{V_{DD}}{2} + \frac{V_{L1} + V_{R1} - V_{L2}}{2} \tag{2}$$

Since capacitor voltages are static during phase 2, a low-bandwidth, low-cost, and/or high-precision op-amp may be used. A comparator evaluates this equality near the end of phase 2, allowing complete set-up during an interval where no switching noise is present. The comparator removes the $V_{DD}/2$ offset, and provides an appropriate up/down command to a 1-bit hysteretic controller. This controller in turn updates the relative duration of A and B phases allowing convergence to optimal split-phase durations in future switching cycles. Further selection of R_1 and R_2 ensures that both op-amp inputs reside within their voltage rails at all times. Note that as a result of forward continuous conduction in L_1 and L_2, phase 2 commences under ZVS conditions — further ensuring signal integrity in the absence of hard switching induced transient settling.

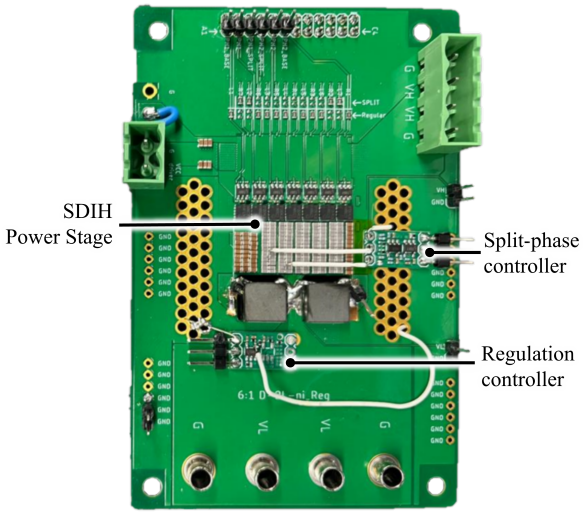


Fig. 6: Photograph of the SDIH power stage and sensing circuitry implemented on two daughterboards; one for active split-phase control, and another for output voltage regulation.

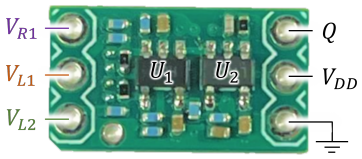


Fig. 7: Photograph of the constructed split-phase controller.

TABLE I: CONTROLLER COMPONENT DETAILS

Component	Details	Part Number
R_1	23.7 kΩ 0.1W 0402	RK73H1ETTP2372F
R_2	4.32 kΩ 1/16 W 0402	CRCW04024K32FKED
C	4.7 μF 10V X5R 0402	CL05A475MP5NRNC
U_1	Low cost op-amp	AD8057ARTZ-REEL7
U_2, U_3	Comparator	LTC6752IS5#TRMPBF

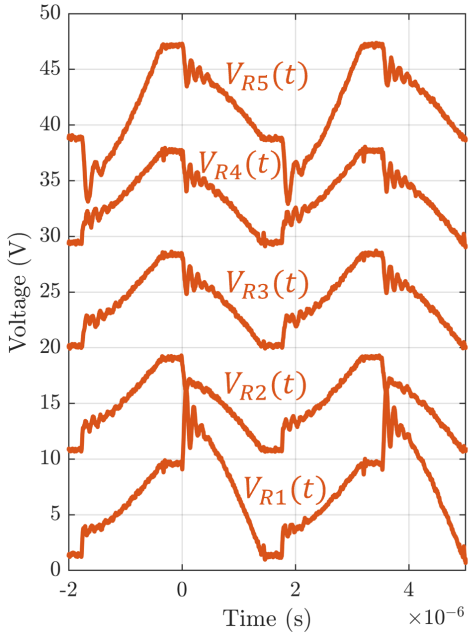
III. EXPERIMENTAL RESULTS

An $N = 6$ SDIH hardware prototype, depicted in Figures 1 and 6, was constructed to validated the proposed closed-loop split-phase control scheme. The split-phase sensing controller in Fig. 7 was connected to the top plates of flying capacitors C_{L1}, C_{R1}, and C_{L2}, thereby enabling closed-loop split-phase control via an FPGA. Also shown in Fig. 6 is a regulation controller, comprising a single comparator where the output voltage is compared to a reference voltage, facilitating basic 1-bit hysteretic voltage control, also implemented on the FPGA. In this way, simultaneous split-phase control and output voltage regulation are achieved, with the controller acting to adjust phase durations by small fixed increments each clock cycle in response to respective comparator outputs. Tables I and II list the components used for the split-phase controller and main power stage, respectively.

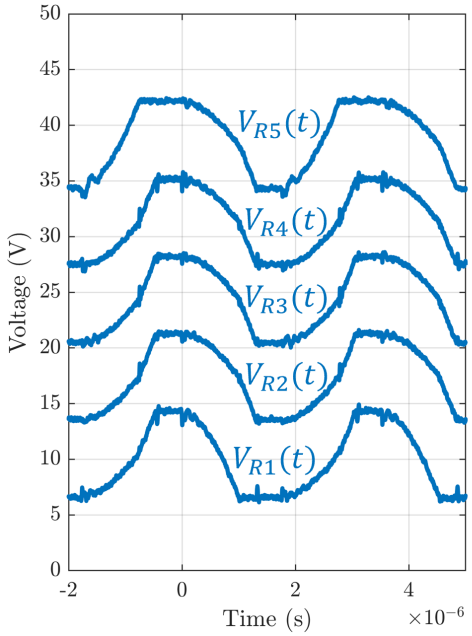
Figs. 8 and 9 depict measured results from the described converter solution. Fig. 8(a) depicts voltage waveforms for flying capacitors C_{R1} to C_{R5} should split-phase switching be removed (i.e., the durations of phases 1B and 3B are set to 0 s). Since capacitor waveforms for C_{LX} and C_{RX} are identical,

TABLE II: SDIH POWER STAGE COMPONENT DETAILS

Component	Details	Part Number
L_1, L_2	330 nH 50 A 0.17 mΩ	PG1712.331HLT
$C_{L,1\text{-}5}$, $C_{R,1\text{-}5}$	28× 18 nF C0G 0603	C1608C0G1V183J080AC
S_{L1}, S_{R1}	0.65 mΩ 25 V	IQE006NE2LM5CGATMA1
$S_{L,2\text{-}7}$, $S_{R,2\text{-}7}$	1.35 mΩ 40 V	IQE013N04LM6CGATMA1
C_{IN}, C_{OUT}	98× 2.2 μF X5R 0603	GRT188R61H225KE13D



(a) Without split-phase control



(b) With split-phase control enabled

Fig. 8: Measured flying capacitor voltages for an $N = 6$ prototype. (a) without split-phase control enabled, i.e. phases 1B and 3B are removed. Abrupt step changes in capacitor voltage indicates hard-charging losses and transient inrush currents. (b) with split-phase control enabled. Smooth continuous voltage waveforms illustrates complete soft-charging with closed-loop split-phase control. For both cases $V_{IN} = 48$ V, $V_{OUT} = 3.3$ V, $f_{SW} = 300$ kHz, $I_{OUT} = 25$ A.

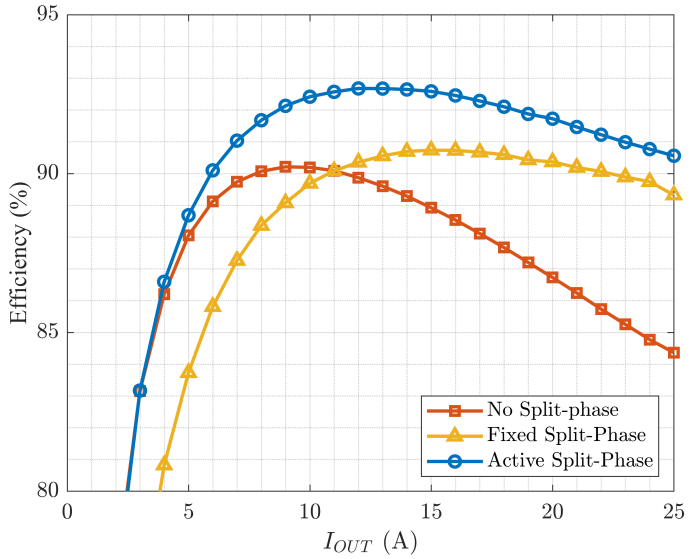


Fig. 9: Measured efficiency curves for the prototype converter with split-phase disabled (red), using calculated split-phase timings in [8], [29] (yellow), with closed-loop split-phase control enabled (blue, **This Work).** $V_{IN} = 48$ **V,** $V_{OUT} = 3.3$ **V,** $f_{SW} = 300$ **kHz.**

bar a 180° phase shift, only one set of waveforms is plotted for conciseness. In this case, abrupt step changes in flying capacitor voltage waveforms is a direct indication of hard-charging losses as instantaneous KVL is not satisfied upon commencement of certain phases. Conversely, Fig. 8(b) depicts smooth and continuous voltage waveforms, indicating complete soft-charging with active split-phase control enabled.

Fig. 9 depicts measured efficiency waveforms, illustrating that closed-loop split-phase control (blue) yields both the highest peak and full load efficiency when compared to clocking regimes in which no split-phase switching is used (red), or one in which the fixed split-phase durations given in [8], [29] are used (yellow). Note that these results are in complete agreement with the theoretical timings portrayed in Fig. 3 and as derived in [24] where both inductor current and capacitor voltage ripple are considered. At zero load, ideal split-phase timings should converge upon $t_{1B} = 0$ s (see Fig. 3). Subsequently in Fig. 9 the efficiency curves for the active split-phase case and no split-phase case converge at light load. Conversely, as load is increased, inductor current ripple becomes small relative to dc; as such, the phase timings of the active split-phase case converge on the timing solution used by the fixed split-phase case as load tends towards infinite — resulting in approaching efficiency curves.

To demonstrate operation of the proposed split-phase controller, Figs. 10 and 11 depict the measured clock signals provided to the SDIH converter under loads of both 5 A and 25 A, respectively. As a result of closed-loop split-phase control Fig. 10 reveals much shorter t_{1B} and t_{3B} intervals while Fig. 11 demonstrates that these intervals are automatically increased at heavier loads. These resulting phase durations are in agreement with the ideal behaviour depicted in Fig. 3, further demonstrating split-phase control's load dependency and the need for active control. The output voltage is regulated to 3.3 V in both cases, as was also the case for all data points plotted in Fig. 9.

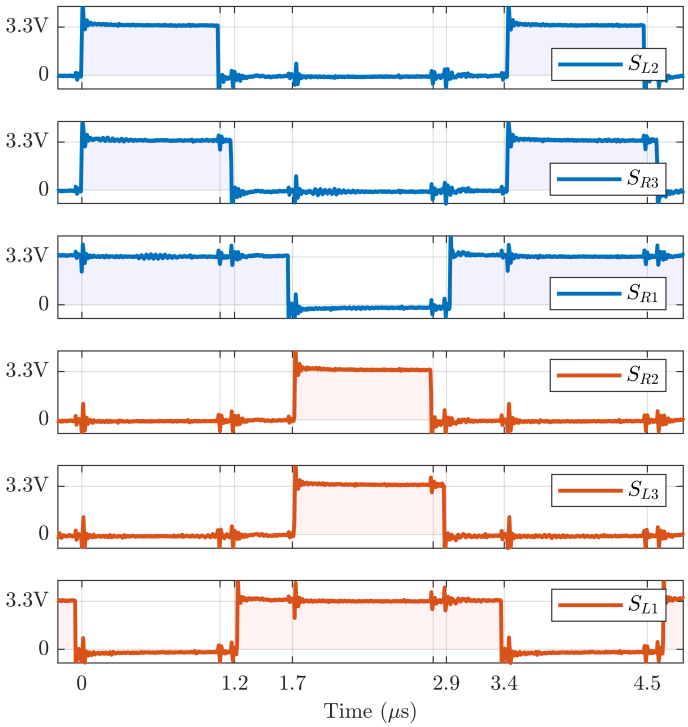


Fig. 10: Measured clock waveforms generated by the closed-loop split-phase controller for $I_{OUT} = 5$ A. Waveforms are depicted in the same order as in Fig. 2. At light load intervals t_{1B} and t_{3B} become short, corroborating the theoretical result depicted in Fig. 3,

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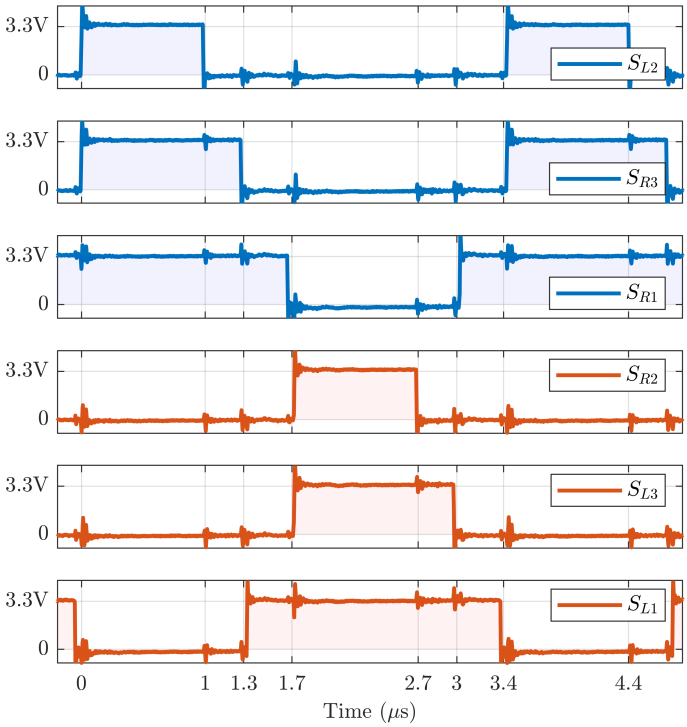

Fig. 11: Measured clock waveforms generated by the closed-loop split-phase controller for $I_{OUT} = 25$ A. As load is increased the closed-loop split-phase controller extends the duration of intervals t_{1B} and t_{3B} to preserve soft-charging.

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IV. Conclusion

This work presents an active closed-loop split-phase control; a clocking scheme required by several high performance HSCC topologies. A straight-forward and appropriate sensing front-end is described, leveraging low-noise phase intervals to perform analog signal processing using low-bandwidth and low-cost components. Measured results validate the superior performance of the split-phase control loop over the full load range compared to control schemes using either calculated or neglected split-phase timing intervals.

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