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IMPROVED POWER CONVERSION FOR LOW VOLTAGE ENERGY HARVESTING APPLICATIONS

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IMPROVED POWER CONVERSION FOR LOW VOLTAGE ENERGY HARVESTING APPLICATIONS

Jiyuan Luan

ABSTRACT

Power conditioning circuit is an essential element for energy harvesting applications. Designed for input rectifying, voltage conversion and output regulation, power conditioning circuit transforms harvested energy from AC to DC and from an unregulated, usually low amplitude input voltage to an application-specific, well-regulated DC output to power the intended load.

Drastically different from conventional power systems, energy harvesting devices usually collect energy from weak power sources and produce low amplitude AC outputs. These devices typically have high output impedance with pronounced reactance in comparison with a regular power supply. The electrical characteristics of the energy harvesting devices make it difficult or even impractical to use existing power conditioning solutions for energy harvesting applications. For example, the forward voltage drop of a typical rectifier diode will prevent those harvested energies with voltage amplitudes below this threshold to be rectified and delivered to their loads. In fact, many recent energy harvesting work are hampered by the lack of adequate power conditioning circuits and fail to prove their practical purposes and values of their energy harvesting techniques.

Inspired by the early work on piezoelectric wind energy harvesting, this research work mainly focuses on low voltage power conditioning circuits for energy harvesting applications. It covers both low voltage rectifier circuits and voltage boosting circuits that are essential for demonstrating the usefulness of energy harvesting techniques. By examining the device physics and operation principles of the existing current rectifying solutions, this work proposes a new low-voltage, high-efficiency hybrid rectifier circuit with low in-line rectifying voltage loss. This new circuit is prototyped and demonstrated to have the highest rectifying efficiency in comparison with other passive rectifier circuits from the literature.

To achieve low-voltage and low-power voltage boosting, this work explored three most representative voltage boosting approaches for energy harvesting applications. It first studied the feasibility of a passive voltage boosting method, which uses the reactive nature of the energy harvesting device to enhance its output voltage. By introducing an inductive load to a capacitive piezoelectric energy harvesting device, this research work studied the feasibility, advantages and limitations of the passive voltage boosting technique via a transformer circuit. It presents bench measurement data for both the voltage conversion ratio and power conversion efficiency.

This work also studied two representative active voltage boosting circuits– charge pump type and inductive boost converter type. Both circuits are bench studied for their minimal input voltage range, voltage boosting capabilities and power conversion efficiencies. Based on these results, a low input voltage power conditioning circuit with hybrid input rectifier is developed and prototyped. Bench test on the prototype

circuit showed that it has high power conversion efficiency around 60% at 10mW and a low start-up voltage of approximately 0.435V V_{RMS} which is better than others work from the literature. This new power conditioning circuit is tested in two energy harvesting applications (thermoelectric and piezoelectric) and both showed great energy harvesting results.

For my parents

CHAPTER 1. INTRODUCTION

Energy harvesting is the process of extracting energy from the ambient and converting it into usable electrical power. Different from conventional power generation, energy harvesting usually chooses its power sources based on their availability rather than energy levels and power densities. In many cases, the power sources used for energy harvesting are considered too weak for commercial power generation. Drastically different approaches are therefore needed to harvest energy from these non-conventional power sources at a relatively low power level which would otherwise be dissipated into the environment[1][2][3].

Table 1-1 Common Energy Sources for Energy Harvesting

Sources	Power Level	Harvesting Approach	Single Unit Output Voltage	Frequency
Solar Energy	0.1~1kw/m^2	Photovoltaic	1.1V	DC
Ambient Light	15μW/cm^2	Photovoltaic	1.1V	DC
Wind Energy	Varies	Turbine	Varies	30~500Hz
Wind Energy	Varies	Piezoelctric	0.6~0.8V	30~120Hz
Vibration	Varies	Piezoelctric	0.1~5V	30~200Hz
Vibration	μW~mW	MEMS	31mV~160mV	30~13.9kHz
Vibration	mW	Electromagnetic	0.3~0.8V	30~490Hz
Heat	μW~mW	Thermoelectric	0.2~3V	DC
Electromagnetic Wave	μW~mW	Antennas	0.1~2V	kHz~MHz

One important motivation for energy harvesting is the abundance of the potential power sources. Energy harvesting technology targets a large variety of energy sources such as mechanical vibration, wind or tidal power, stray electromagnetic field, thermal or heat gradient and many others for energy extraction. Despite the low power nature of these energy sources, the wide availability and high accessibility at the desired locations make them good candidates for energy harvesting exploration.

Table 1-1 shows some of the energy sources that have been recently studied for energy harvesting applications. Although diversified in both harvesting approaches and energy levels, the following few characteristics are common among these energy sources:

(1) Many of the outputs are in Alternating Current (AC) polarities

(2) The amplitudes for the output voltages are typically low, around or below one diode forward voltage drop (0.6V)

(3) Power levels are usually very low, usually in the μW or nW range

These power source characteristics post unique challenges as well as opportunities for developing power conversion solutions specifically designed for energy harvesting applications. As expected, they will be considerately different from the conventional power management solutions used in today's commercial power generation.

1.1.POWER CONDITIONING CIRCUIT FOR ENERGY HARVESTING APPLICATIONS

The first step to enable an electronic load to utilize the harvested energy is to convert the AC output from the energy harvesting devices to Direct Current (DC) in polarity. Many energy harvesting devices extract energy from the kinetic energy of repetitive mechanical motions, the output of these energy harvesting devices are usually AC – electrical signals with their output polarities changed to the opposite polarity periodically. For example, Figure 1 shows a typical output waveform of a polymer

piezoelectric wind energy harvesting device made from polyvinylidene difluoride (PVDF). The output voltage of this device varies between -0.6V and +0.6V in a periodic fashion, and the electrical potential of any of the two output terminals can be either positive or negative depending on the timing within each period.

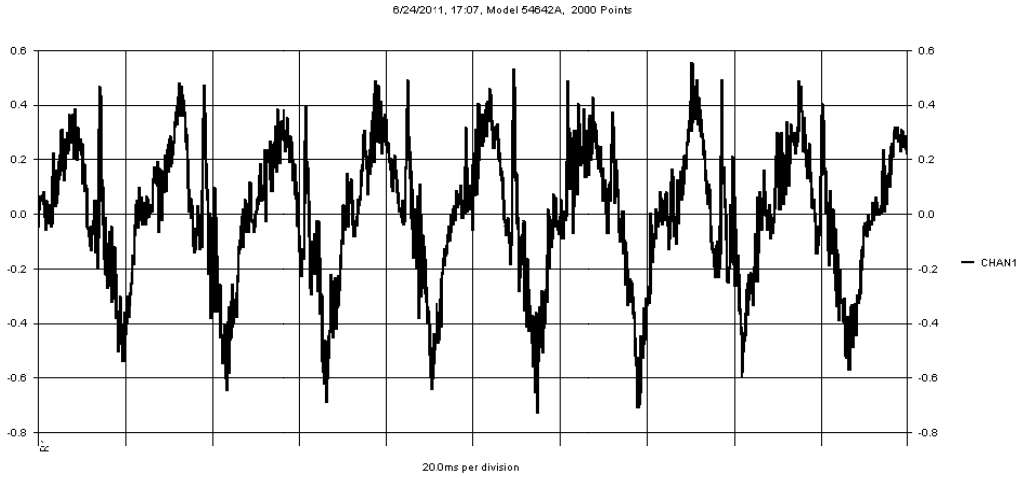

Figure 1 Output of a PVDF Wind Energy Harvesting Device

Similar AC output exists with inductive wireless power transfer application. With the need for more device mobility, portability and safety requirements, inductive power and signal transmission such as Radio-Frequency IDentification (RFID), Radio Frequency (RF) transponder and other inductive-coupled devices have become more and more popular in recent years[4][5]. Figure 2 shows a typical configuration of an inductive power transmission system. The primary coil converts energy from the power supply into an alternating electromagnetic field, the secondary coil in the

receiving end uses an antenna wire loop to intercept the electromagnetic field, inducing an AC current to power the load electronics.

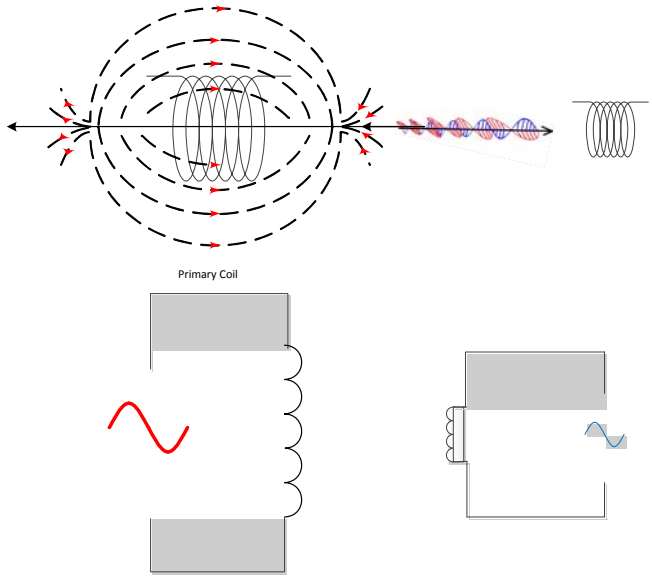

Figure 2 A Typical Inductive Power Transfer Systems

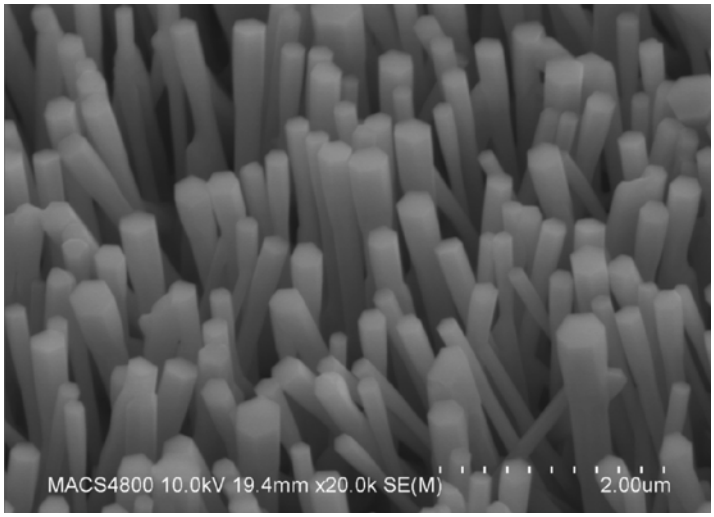

Figure 3 ZnO Nanowires Used for Energy Harvesting

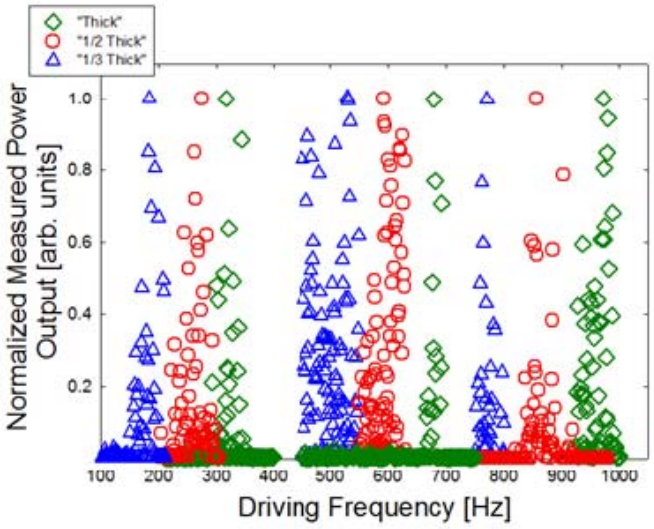

Figure 4 Power Output of ZnO Nanowires with Driving Frequency

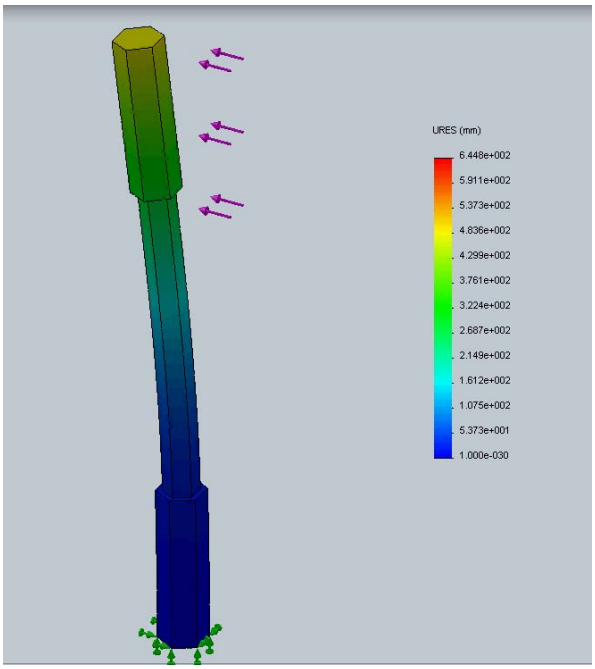

Figure 5 Vibration Energy Harvesting using a ZnO Nanowire

Another example of the AC harvested energy output is the ZnO nanowire vibration energy harvesting[6][7]. ZnO nanowires have piezoelectricity and therefore can be used for vibration energy harvesting. A typical output of the ZnO piezoelectric output has an AC peak voltage of 0.2V with variable frequencies with respect to the sizes and shapes of the ZnO nanowires. Figure 3 shows the Scanning Electron Microscope (SEM) image of a group of ZnO nanowires, Figure 4 shows the normalized power outputs with regard to the mechanical driving frequencies[8]. Figure 5 shows the finite element analysis (FEA) result on the lateral mechanical displacement induced by the mechanical stress applied to a ZnO nanowire.

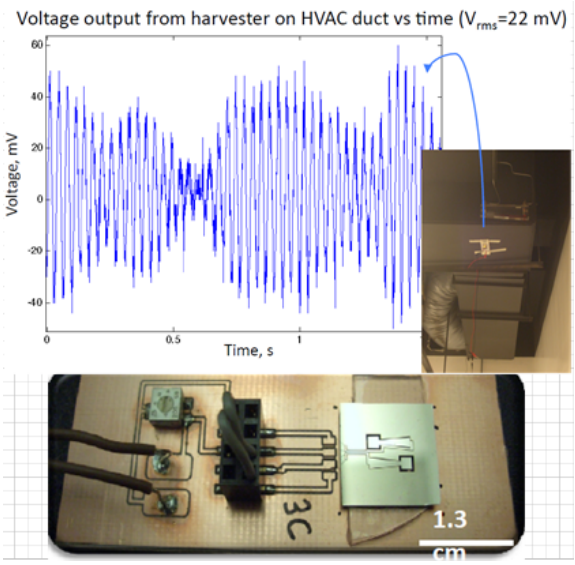

Figure 6 MEMS Vibration Energy Harvesting

AC output voltages are generated not only by piezoelectric and electromagnetic transducers, but also by many other energy harvesting approaches such as Micro-Electro-Mechanical Systems (MEMS). Figure 6 shows the configuration and output

waveform from a MEMS vibration energy harvesting research. An integrated MEMS energy harvester is used to harvest the mechanical vibrations from ambient sources. The output of the MEMS device is an AC signal which can vary between 10mV and 50mV[9][10][11].

All energy harvesting examples above exemplify the necessity of current rectifying as one of the basic requirement of the power management function for energy harvesting applications.

Once the harvested power is rectified to DC, there will be additional power conversion steps to make the voltage level of the harvested energy match its intended load. Modern electronics are usually powered through different supply rails and the voltage specification of these supply rails are determined by the different voltage ratings of the various circuit components connected. In general, the voltage rating for modern electronics is scaled with the advancement of semiconductor technology and best illustrated by the supply voltage vs. technology node relationship. Table 1-2 lists the typical power supply voltages with regard to the different semiconductor technology nodes represented by a leading technology company[12].

From Table 1-2, it can be seen that although the general trend for the system supply voltage is to decrease as the technology node shrinks from generation to generation, the system operating voltage rating asymptotic approaches around 1V because the operation of today's circuit requires the supply voltage to support at least two Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) thresholds. On the other

side, the intrinsic limitation of the drain current on/off ratio of a MOSFET in subthreshold conduction region restricts further decrease of a MOSFET gate threshold[13]. It is therefore necessary for the energy harvesting technology to target an output DC voltage of no less than 1V.

Table 1-2 Major Technology Nodes and its Supply Voltage Scaling

Process Nodes	Release Year	Status	Chip	Vdd
600nm	1994	Production	80486	5.0V
350nm	1995	Production	Pentium Pro	1.5~3.3V
250nm	1997	Production	Pentium II/III	2.25~2.75V
180nm	1999	Production	Celeron	1.2~2.5V
130nm	2002	Production	Pentium 4	1.2~1.5V
90nm	2004	Production	Xeon	1.0~1.2V
65nm	2006	Production	Pentium Core	1.0V
45nm	2008	Production	Intel Core i7	1.2V
32nm	2010	Production	Intel i3/i5/i7	1.35V
22nm	2012	Production	Intel i5/i7	1.0V
14nm	2014	In development		0.9V

Another factor to consider when designating the output voltage for an energy harvesting application is the compatibility with existing energy storage devices. Although capacitive energy storage has made great advancements in recent years, the relative low energy density as well as higher leakage current posts great challenges for its role as the sole energy source for applications such as distributed sensor networks. Batteries, on the other hand, provide better energy density and longer operation lifetime, making them indispensible power sources for applications which can take advantage of them. Depending on the battery chemistry, the required charging voltage becomes another specification for the design of the energy harvesting circuits. For example, a Lithium-Ion (Li-Ion) battery usually requires a

charging voltage around 4.0 V, which would require the output of the energy harvesting device to provide a regulated voltage no less than 4.0V.

Comparing Table 1-1 and Table 1-2, it is obvious that the majority of energy harvesting outputs alone cannot meet the operating voltage requirement of the modern electronic circuits. A voltage boosting circuit is usually required to step-up the harvested low amplitude voltage (rectified if it was AC) to a higher level to match the needs of the electronic loads. Voltage boosting is therefore another essential step for many of the energy harvesting applications.

Table 1-3 Maximum Absolute Voltages for a few Major Technology Nodes

Process Nodes	Chip	Rated Supply Voltage	Absolute Maximum Voltage	Maximum Tolerance of Supply Variation
600nm	80486	5	6.5	1.5
350nm	Pentium Pro	3.3	4.7	1.4
250nm	Pentium II/III	3.3	4	0.7
130nm	Pentium 4	1.35	1.75	0.4
90nm	Xeon	1.2	1.55	0.35
22nm	Intel i5/i7	1	1.25	0.25

Another important but not so obvious aspect from table 2 is that as the supply voltage scales down with the technology nodes, the semiconductor components are more and more susceptible to voltage excursions and fluctuations. The voltage rating at or exceeding a certain level that a semiconductor IC would sustain permanent damage is commonly known as the Absolute Maximum Voltage of the IC. Table 1-3 shows the Absolute Maximum Voltage ratings for a few selected technology nodes. It can be

seen that as the supply voltage scales down, the maximum tolerance for supply voltage variations also scales down and often at a steeper rate. Lower operational supply voltage usually requires a narrower operational voltage range. For an energy harvesting circuit to safely power modern semiconductor devices, a power management circuit which can regulate the output voltage in spite of the supply and load variations is therefore essential.

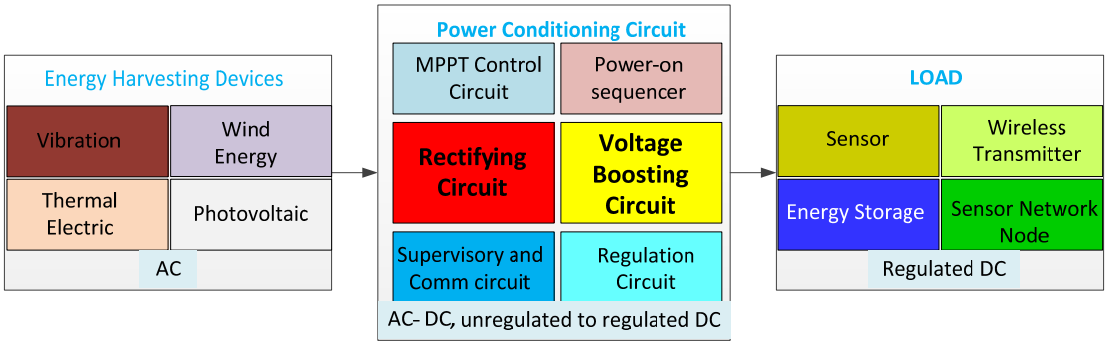

Figure 7 System Block Diagram of an Energy Harvesting System

In the field of power management, the circuits which rectify AC to DC, convert one voltage level to another and regulate the output voltage of a circuit to a specified level are generally under the category of power conditioning circuit. As can be seen from the energy harvesting examples above and Figure 7, power conditioning circuit is an essential part of the overall energy harvesting system. Without an adequate power conditioning circuit, it is difficult or even impossible to utilize the outputs of many harvested energy solutions.

This work is devoted to the power conditioning circuit specifically designed for energy harvesting applications. Since the outputs of energy harvesting devices are

drastically different from conventional power systems, it is difficult or even impossible to use existing power conditioning solutions for energy harvesting applications. For example, a typical house line voltage is 110V AC. This makes the 0.6V forward voltage drop of a rectifier diode insignificant in a rectifier circuit when using the line voltage. However, the same forward voltage drop of a rectifier diode will be significant or even devastating for those energy harvesting applications with output voltages around or below this threshold. It is not uncommon that the lack of adequate power conditioning circuits has prevented some of the energy harvesting technologies from demonstrating and proving their practical values[9]. By developing power conditioning circuits which are specifically designed for low voltage and low power energy harvesting applications, the voltage and energy threshold will be reduced for practical energy harvesting which will help to create more opportunities for energy harvesting applications as well as exploring more potential energy sources.

1.2. DISSERTATION OUTLINE

This dissertation is organized in the following chapters.

Chapter one is the introduction of this dissertation. It outlines the challenges of practical energy harvesting, as well as the power conditioning requirement to bridge up the gap between harvesting energy and making use of the harvested energy. Due to the differences between energy harvesting devices and conventional power

generation, a new type of power conditioning circuit is needed to address the specific application requirement of the energy harvesting applications.

The AC to DC rectifier circuits are analyzed for low power energy harvesting applications in **chapter two**. This chapter reviews various implementations of the rectifier circuits including some of the recent developments in this field. By analyzing the operation principles of different rectifier circuits, the development trend and state-of-the-art in low voltage rectifying circuit design are presented. The power conversion efficiency of different rectifier circuits are compared and used as benchmark to evaluate the newly proposed hybrid rectifier circuit with a virtual junction.

Chapter three reviews the device physics and operation principle of the rectifying devices and their limitations in achieving high efficiency low voltage current rectifying. The physical principle which enables a p-n junction diode to be an effective current rectifier also accounts for the power dissipation in a diode rectifier circuit. The lack of a built-in junction potential in a MOSFET makes it a bi-directional switch which is susceptible to bi-directional current flow. By proposing a new hybrid rectifier circuit with a virtual junction, the advantages of both p-n junction diodes and bi-directional MOSFET switches can be combined and significantly improve the power conversion efficiency of the low voltage rectifier circuit.

Chapter four discusses passive voltage boosting methods. Since many energy harvesting devices are electrically capacitive or inductive, it is therefore possible to

introduce an additional component to make the energy harvesting circuit an oscillatory 2nd order system. The resonant frequency of this oscillating circuit can be adjusted by choosing the proper value of the new component such that this self-oscillating frequency is tuned to the energy source's excitation frequency. At this frequency, the resonating output will be larger than the output at non-resonating conditions, enhancing the energy harvesting output without dissipating additional power. A PVDF wind energy harvesting device and a transformer are used in this chapter to study the passive voltage boosting approach. Test results indicated that although an LC resonant circuit can be developed, it is the tuning of the resonant frequency which posts the challenge of applying this method to wind energy harvesting applications.

Chapter five explores active voltage boosting approaches based on both circuit analysis and bench verification. Depending on the types of energy storage devices used, there are two main categories of active voltage boosting circuits – charge pump type and inductive switching mode converter type. Both approaches are studied, prototyped and bench tested, with their energy conversion efficiency and input voltage range being compared for the suitability of energy harvesting applications.

Chapter six presents an example of a high efficiency power conditioning circuit design for energy harvesting applications. Based on the proposed high efficiency hybrid rectifier circuit, this chapter presents an example on system level design, with bench test results to show its high power conversion efficiency and wide input

operating range. This circuit is further tested in two different energy harvesting applications (thermoelectric and piezoelectric) and both showed great energy harvesting results.

Chapter seven concludes the dissertation with recommendations of the guidelines for high efficiency power conditioning circuit design for energy harvesting applications.

Chapter eight presents some reflections on the overall power conditioning topic for low-voltage, low-power applications, and provides some of the thoughts on future work and improvements.

CHAPTER 2. LOW VOLTAGE RECTIFIER CIRCUIT FOR ENERGY HARVESTING APPLICATIONS

A rectifier circuit is a circuit which converts alternating current (AC) into direct current (DC). Rectifier circuits are needed for those energy harvesting devices which have AC outputs but need to power electronic loads which use DC supplies.

This chapter reviews the operation principle of the rectifier circuits as well as the recent developments in low voltage, high efficiency rectifier circuit design. Since current rectifying is usually the first step to convert AC harvested energy to usable electrical energy, the power conversion efficiency and input voltage range of the rectifier circuit have a huge impact on the overall energy harvesting efficiency. Many new circuits have been recently proposed to reduce the minimal rectifying input requirement as well as to increase the power conversion efficiency of the rectifier circuit itself.

2.1.INTRODUCTION TO RECTIFIER CIRCUITS

Although rectifier circuits are among some of the most common circuits in all modern electronics, they are still being actively studied in recent years for low voltage power conversion including energy harvesting applications. Traditional diode-bridge rectifiers were developed for applications in which the forward voltage drop of the rectifier diode is insignificant in comparison with both the input and output voltages of the rectifier circuit. However, for low-voltage, low-power energy harvesting

applications, the voltage outputs of the energy harvesting devices can be in the same order of magnitude of a forward voltage drop of a rectifier diode, which dramatically reduces the power conversion efficiency of the rectifier circuits. In fact, without a highly efficient rectifier circuit, many low voltage energy harvesting devices would become impractical for energy harvesting because most of their harvested energy is lost in the rectifying stage. It is therefore important to develop new low-voltage rectifier circuits which can maintain high power conversion efficiency even at low input voltage levels.

Another important feature of a good low voltage rectifier circuit is the capability to self-start and sustain operation. Many energy harvesting applications lack the infrastructure for utility power, and may not have an energy storage device to initiate a start-up operation. It is therefore highly desirable for the rectifier circuit to be able to self-start and sustain operation without any external power supply. This simple but important application requirement posts additional challenges on the types of circuits which can be used for energy harvesting applications.

In this dissertation, the basic operation principle of the traditional diode rectifier circuit is reviewed. The operation principles of the diode rectifier circuit serve as the foundation to the more advanced, high-efficiency rectifier circuits presented later on in this dissertation.

A single diode, half-wave rectifier circuit is probably among the simplest circuit for all rectifier circuits. Although it can only use half of the AC input polarity which

restricts the maximum energy conversion efficiency of this rectifier circuit, the low in-line rectifying voltage drop make it useful in applications that have low output voltages. A four-diode, full-wave rectifier can harvest energy from both polarities of the AC input and is the most commonly used rectifier circuit for power generation applications. However, the higher in-line rectifying voltage drop requires higher output voltage amplitude from the energy harvesting devices. The voltage and power conversion efficiencies of both single diode and four-diode rectifier circuit are analyzed in this chapter.

Apart from the p-n junction diodes which are commonly used in rectifier circuits, diode-connected MOSFETs can also be used to improve the voltage and power conversion efficiency because their more flexible gate thresholds are easy to integrate on the integrated circuits (ICs). A thorough analysis of the MOSFET rectifier circuits helps to analyze the pros and cons of diode-connected MOSFETs in comparison with p-n junction diodes.

To overcome the low power conversion efficiency issue due to the diode forward voltage drop or the MOSFET gate threshold drop, a synchronous rectifier circuit was proposed[14]. By introducing a control circuit to turn-on and turn-off the rectifier MOSFETs with regard to the input polarities, the synchronous rectifier circuit can significantly improve the low voltage power conversion efficiency at the cost of higher quiescent power dissipation of the control circuit and the R_{ds} on-resistance of the passing element. For low-power energy harvesting applications, the additional

static power dissipation sometimes outweighs the improvement in the rectifying efficiency, restricting its practical value in low power energy harvesting applications. Synchronous rectifiers also have a maximum operating frequency limitation. The parasitic capacitance of the MOSFETs and the typical low-power design of the synchronous controller limit the maximum switching frequency of the rectifier MOSFETs, preventing the synchronous rectifiers from being used for high switching frequencies.

To reduce the rectifying efficiency loss due to the gate threshold voltage of the rectifier MOSFETs, a full-wave gate cross-coupled rectifier circuit was proposed in 2001[15]. The combination of diode-connected MOSFETs and gate cross-coupled MOSFETs reduce the forward voltage drop for the rectified current, and improving the power conversion efficiency. However, this circuit still suffers one MOSFET gate threshold loss which restricts the maximum power conversion efficiency of this rectifier circuit.

A full-wave fully gate cross-coupled rectifier was introduced in 2005[16]. This circuit was proposed to resolve the rectifying efficiency loss due to the gate threshold voltage drop of the rectifier MOSFET, however, since the MOSFET functions as a bi-directional switch, it was shown that this circuit suffers a current flow-back issue and cannot achieve high rectifying efficiency in actual circuits[17].

Another approach to improve the power conversion efficiency of the MOSFET-based rectifier circuit is the use of a gate threshold cancellation technique[18][19][20]. This

approach uses a capacitor to store energy during the conduction phase and cancels out the gate threshold drop of the MOSFET passing element. However, this method requires the duplication of the threshold voltage of the MOSFET passing element, which is susceptible to device mismatch and process variations.

Another method proposed to improve the power conversion efficiency of the diode-connected MOSFET rectifier circuit is to modulate the threshold voltage of the MOSFET passing element by substrate switching technique[21]. However, this method is not very effective because of the typical low gate threshold sensitivity to the substrate bias voltage. There were also other methods proposed such as using floating gate MOSFET to program the gate threshold of the MOSFET passing elements[22]. However, since programming the floating gate of a MOSFET is usually done by avalanche breakdown and charge tunneling, precise gate threshold adjustment through floating gate programming is difficult to control given the typical process, temperature and voltage variations of the MOSFETs.

Although there are many new rectifier circuits being proposed and studied in recent years, a high efficiency, self-starting rectifier circuit that fit the need of low voltage, low power energy harvesting applications is still highly desirable. In this chapter, the operation principle and the pros and cons of different rectifier circuits are reviewed and analyzed. The insights gained from these existing rectifier circuits are used as the foundation for the new high efficiency hybrid rectifier circuit to be proposed in Chapter 3.

2.1.1 HALF-WAVE RECTIFIER CIRCUIT

A single diode half-wave rectifier circuit is the most simple rectifier circuit available. Compared with a four-diode rectifier circuit which allows the AC current to flow in both input polarities, a single diode rectifier circuit only provides current flow in one of the two possible current directions, hence it is sometimes referred as an half-wave rectifier circuit. Figure 8 shows the basic circuit schematics of two types of half-wave rectifier circuits. Figure 8(a) shows a half-wave rectifier circuit using a rectifier diode. Figure 8(b) shows a similar half-wave rectifier circuit using a diode-connected MOSFET. Both circuits can rectify an AC input to a DC voltage[20][23].

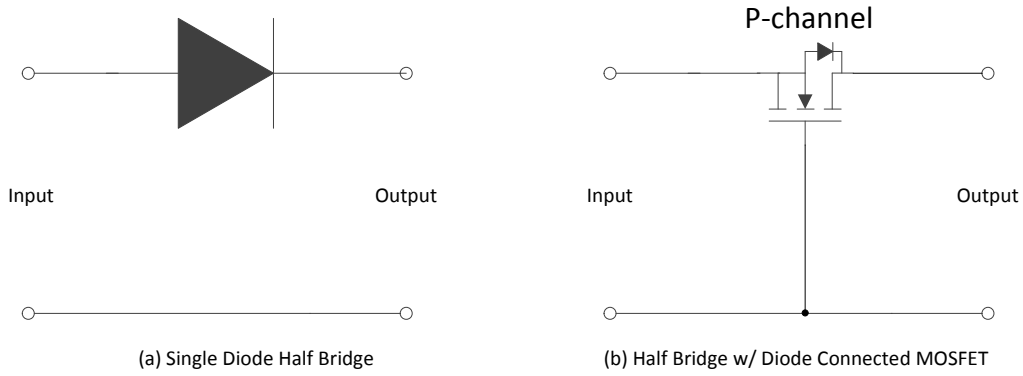

Figure 8 Half-wave Rectifier Circuits

2.1.1.1 PRINCIPLE OF HALF-WAVE RECTIFIER CIRCUITS WITH DIODES

The half-wave rectifier circuit in Figure 8(a) takes advantage of the diode's property that it only allows currents to flow in one direction. The half-wave rectifier circuit in

Figure 8(b) is based on the MOSFET property that it will conduct current only when its gate is properly biased beyond its gate threshold. Although these two circuits are based on very different rectifying mechanisms, they are very similar in output current waveforms as well as their circuit functions.

The diode-based half-wave circuit operates based on the basic p-n junction principle. Figure 9 shows the basic operation principle of a single diode rectifier. Figure 9(a) shows the construction of an abrupt-junction p-n junction diode. The Fermi levels on both p-type and n-type semiconductor materials are illustrated by the E_f levels on both sides of the junctions in the energy band diagrams, with V_b indicating the external bias voltage. At equilibrium condition without any external bias, the alignment of the Fermi level in the p-type and n-type semiconductor materials create a built-in potential V_i:

$$V_i = \frac{kT}{q} \ln\left(\frac{N_P N_N}{N_i^2}\right) \tag{1}$$

In which k is the Boltzmann constant, T is absolute temperature, q is unit electron charge, N_P and N_N are the doping density in the p-type and n-type materials respectively, and N_i is the equilibrium carrier concentration in intrinsic semiconductor material.

Figure 9(b) shows the energy band diagram of a diode under reverse bias condition. When a p-n junction is biased in the reverse direction, the external bias voltage adds on top of the existing built-in junction potential and widens the depletion region which prevents the majority carriers from conducting current. The very low level of

the minority carriers in the semiconductor material forms the leakage current of the diode.

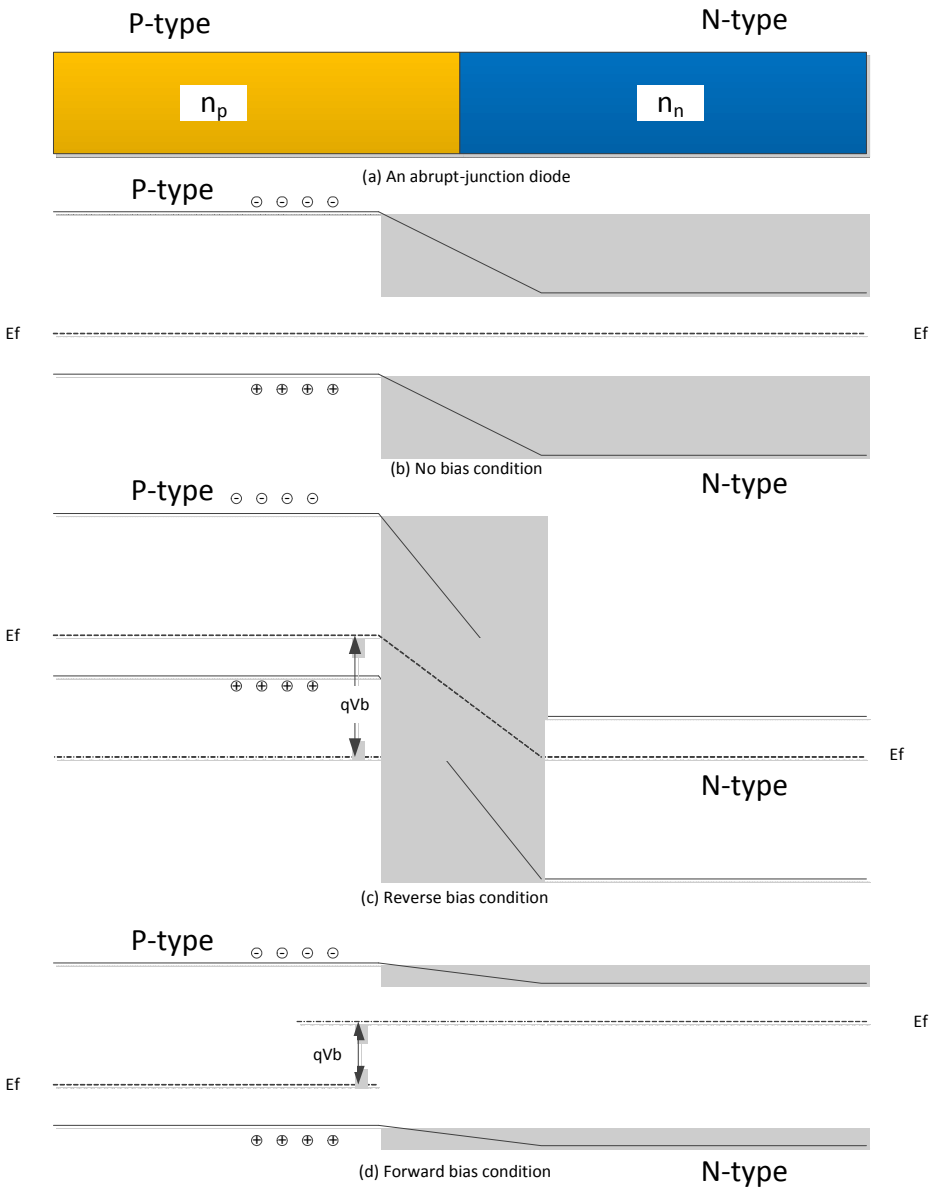

Figure 9 Principles of a p-n Junction Diode and Current Rectifying

Figure 9(c) shows the energy band diagram of a p-n junction diode under forward bias condition. The external bias voltage is in the opposite polarity of the diode built-in junction potential which reduces the width of the depletion region, and cancels out the internal potential barrier. This will allow the majority carriers to create a large forward current.

It can be seen that the p-n junction built-in potential plays a key role for the current rectifying operation the diode. It widens the width of the depletion region when the diode is reverse-based, which prevents the majority carriers in the semiconductor from diffusing across the p-n junction.

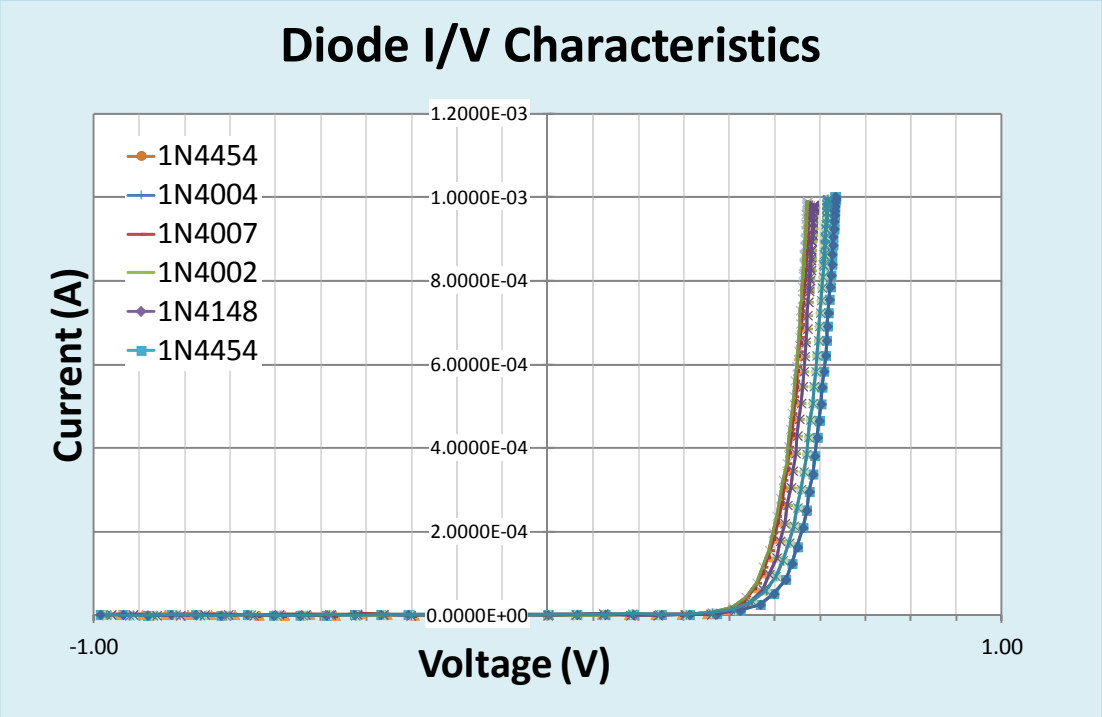

Figure 10 Measured I/V Characteristics of Different Diodes

It is also important point out that the junction built-in potential also accounts for the power loss during the current rectifying process because carriers lose energy while passing this energy gap.

The magnitude of the p-n junction built-in potential is mainly determined by the doping densities of the p-type and n-type semiconductor materials but is generally in the range around 0.6V. Figure 10 shows the measured I/V characteristics of different types of diodes. The x-axis is the forward diode voltage in volts and the y-axis is the diode current in amps. Figure 10 shows most of the diodes have forward voltage drops around 0.6V at 100uA, which accounts for the efficiency loss for passive rectifier circuits with p-n diodes.

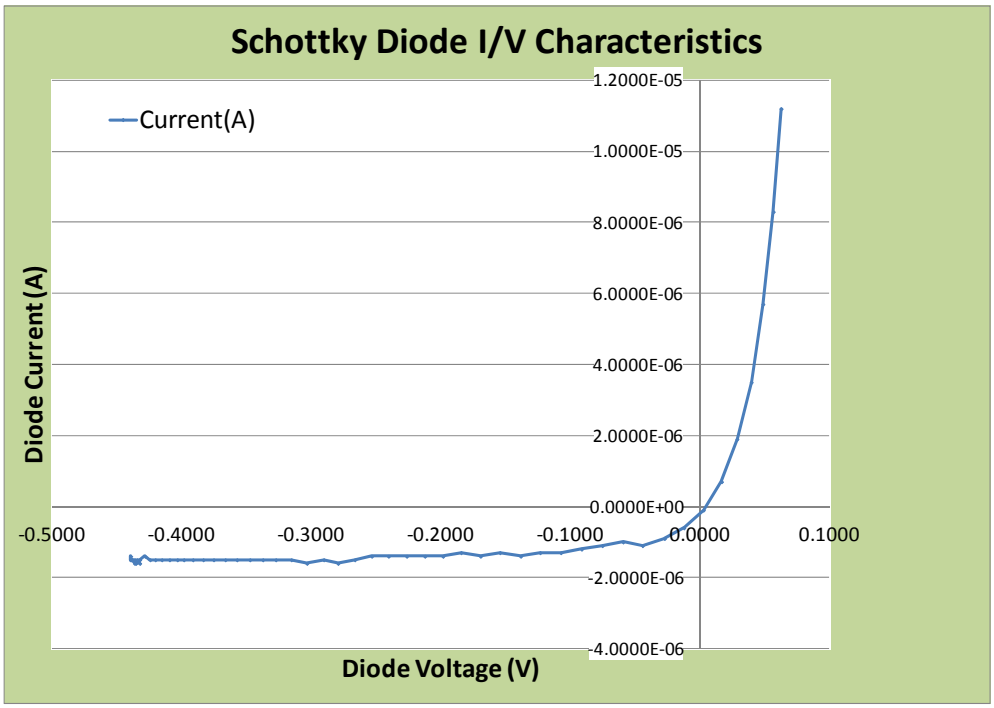

Figure 11 Measured I/V Characteristics of a Schottky Diode

The power dissipation on a rectifier diode with current i_D and forward voltage drop v_D is:

$$P_D = v_D \cdot i_D \tag{2}$$

One way to reduce the power dissipation and increase the rectifier power conversion efficiency is to reduce the forward diode voltage drop v_D by selecting diodes with lower v_D, such as Schottky diodes. However, as shown in Figure 11, Schottky diodes usually have higher reverse leakage current. For example, for the Schottky diode measured in Figure 11, the reverse leakage current is in the μA range at voltages beyond -0.1V, which would significantly degrade the current rectifying effect of the rectifier circuit.

2.1.1.2 PRINCIPLES OF HAVE-WAVE RECTIFIER WITH DIODE-CONNECTED MOSFETS

In order to reduce the power loss due to the diode forward voltage drop of a p-n junction, a diode-connected MOSFET can be used in place of the p-n junction diodes. Since the threshold of the MOSFET can be engineered to target a lower voltage, this is one way to potentially reduce the rectifying power loss associated with the forward voltage drop of a diode.

Figure 12 shows the energy band diagram for a PMOS FET in flat-band condition as well as in diode-connected condition. At flat-band condition, the Fermi level of the P-type polysilicon gate is aligned with the n-doped substrate. When the gate of the

MOSFET is tied to the drain, the input voltage will create a voltage difference between both source-to-drain and gate-to-drain, forward biasing the MOSFET and cause the MOSFET to conducting current. The voltage drop on the MOSFET would be the summation of the threshold of the MOSFET and the IR drop caused by the current flow in the channel of the MOSFET.

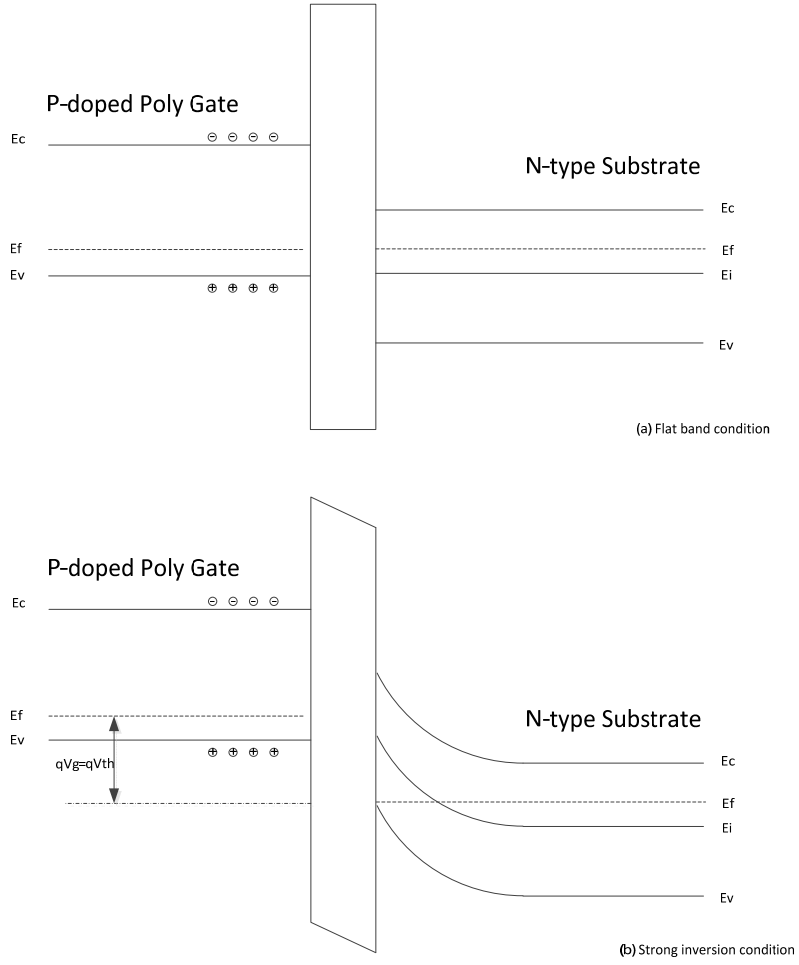

Figure 12 Energy Band Diagram for Diode-connected MOSFET

A unique problem arises when a MOSFET is used as a rectifier diode – substrate effect. The threshold of a MOSFET is defined as the gate potential to induce surface charge with equal and opposite polarity of the substrate:

$$V_T = V_{FB} + V_C + 2\phi_F + \frac{q(N_a - N_d)}{C_{OX}}\sqrt{\frac{2\varepsilon_s 2\phi_F}{q(N_a - N_d)}} \tag{3}$$

Where the flatband voltage V_{FB} is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{OX}} \tag{4}$$

And the bulk potential ϕ_F

$$\phi_F = V_t \ln\frac{P}{N_i} \tag{5}$$

When the substrate of the MOSFET is not tied to ground potential,

$$V_{THB} = V_T + \gamma(\sqrt{|2V_{fp} + V_{SB}|} - \sqrt{|2V_{fp}|} \tag{6}$$

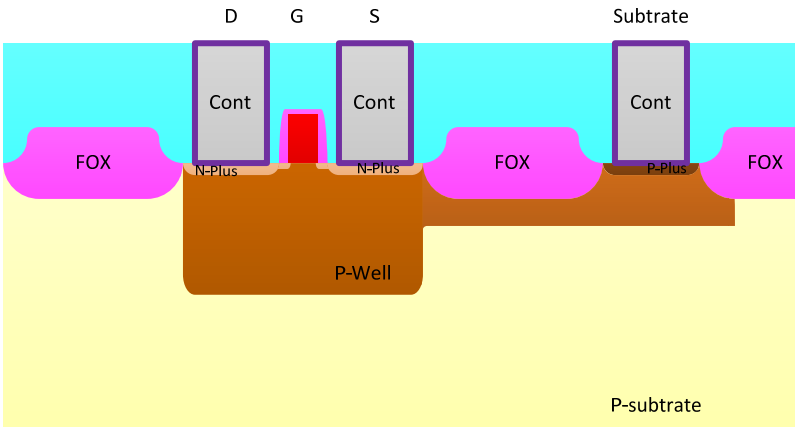

Figure 13 Cross-section of a Typical N-Channel MOSFET

Where the substrate effect coefficient γ is defined as:

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{OX}} \tag{7}$$

The potential of the MOSFET substrate will affect the threshold voltage of the MOSFET and is known as the MOSFET substrate effect.

Due to the MOSFET substrate effect, the selection of the right type of MOSFET is very important for achieving high power conversion efficiency when a diode-connected MOSFET is used for rectifying AC input to DC output. For example, Figure 13 shows the cross-section of a typical NMOS FET and Figure 14 shows this NMOS FET used as a high side pass element of a diode-connected rectifier circuit. The substrate of the NMOS pass element needs to be tied to the lowest potential of the three terminals and in this case, it is the output Vout, and in ideal application

$$V_{IN} = V_{OUT} \tag{8}$$

The substrate of the NMOS therefore is biased to the full output potential and will suffer substrate effect with a higher threshold than nominal condition (w/o substrate effect). When input voltage is at the rated MOSFET threshold voltage, this MOSFET might not be turned-on at all.

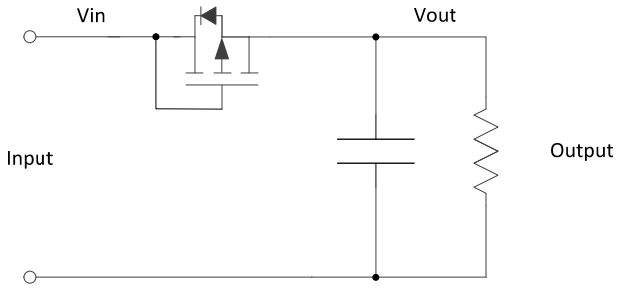

Figure 14 N-channel MOSFET Used as High-side Switch

Similarly, the use of PMOS FETs as low-side switches could also be subjected to MOSFET substrate effect. Care must be taken in selecting the appropriate types of MOSFETs when diode-connected MOSFETs are used in rectifier circuits.

2.1.1.3 EFFICIENCY OF HALF-WAVE RECTIFIER CIRCUITS

The efficiency of a half-wave rectifier is a function of the input voltage V_m as well as the diode forward voltage drop v_d. Figure 15 shows the typical waveform of a half-wave rectifying output with heavy load. Assume the input signal is a sinusoid signal $V_{in}(t)$:

$$V_{in}(t) = V_m \sin(\omega t) \tag{9}$$

$$V_{out}(t) = \begin{cases} V_m \sin(\omega t) - v_d, when V_m \sin(\omega t) > v_d \\ 0, otherwise \end{cases} \tag{10}$$

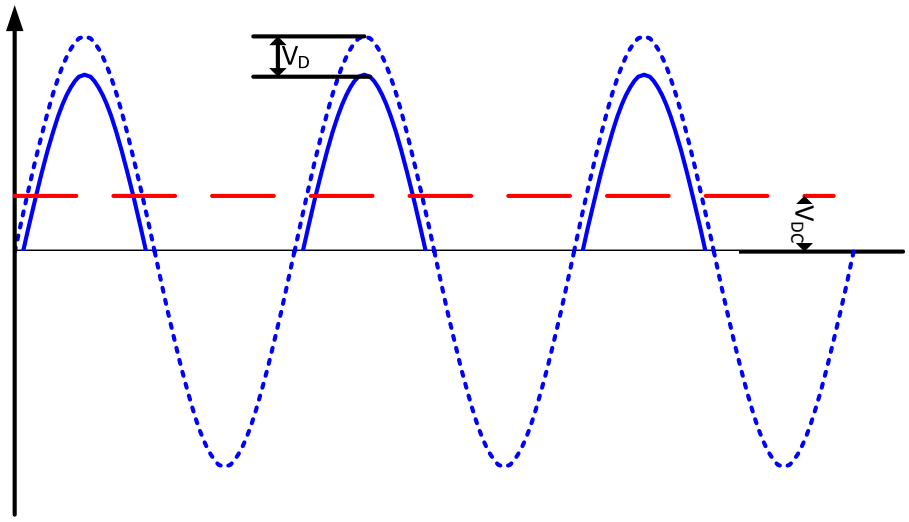

Figure 15 Forward Conduction of a Half-wave Rectifier

The diode conduction on time ωt_{on} and off time ωt_{off}

$$\omega t_{on} = \sin^{-1}(\frac{v_d}{V_m}) \tag{11}$$

$$\omega t_{off} = \pi - \sin^{-1}(\frac{v_d}{V_m}) \tag{12}$$

Therefore the conduction angle θ_c is

$$\theta_c = \omega(t_{off} - t_{on}) = \pi - 2\sin^{-1}(\frac{v_d}{V_m}) \tag{13}$$

The Root-Mean-Square (RMS) DC output of the rectifier output is therefore:

$$\begin{aligned} V_{RMS} &= \frac{1}{T}\int_0^T V_{out}(t)dt = \frac{1}{T}\int_{t_{on}}^{t_{off}} (V_m \sin(\omega t) - v_d)dt \\ &= \sqrt{\frac{1}{4\pi}(V_m^2 + 2v_d^2)[\pi - 2\sin^{-1}(\frac{v_d}{V_M})] - \frac{3v_d V_m}{2\pi}\cdot\sqrt{1-(\frac{v_d}{V_m})^2}} \end{aligned} \tag{14}$$

The rectifying efficiency η of the half-wave rectifier is therefore:

$$\eta = \frac{V_{RMS}^2}{\left(\frac{V_m}{\sqrt{2}}\right)^2} = \frac{1}{2\pi}(1 + \frac{2V_d^2}{V_m^2})[\pi - 2\sin^{-1}(\frac{V_d}{V_m})] - \frac{3}{\pi}\frac{V_d}{V_m}\sqrt{1-(\frac{V_d}{V_m})^2} \tag{15}$$

Figure 16 shows the power conversion efficiency of the half-wave rectifier circuit. As can be seen, the maximum energy conversion efficiency of around 42%. This number is slightly higher than textbook because no approximation is made during the efficiency calculation process.

Apart from circuit simplicity, the half-wave rectifier circuit dissipates only one diode forward voltage drop during the AC to DC conversion process, which could have higher power conversion efficiency when the amplitude of the input voltage is low.

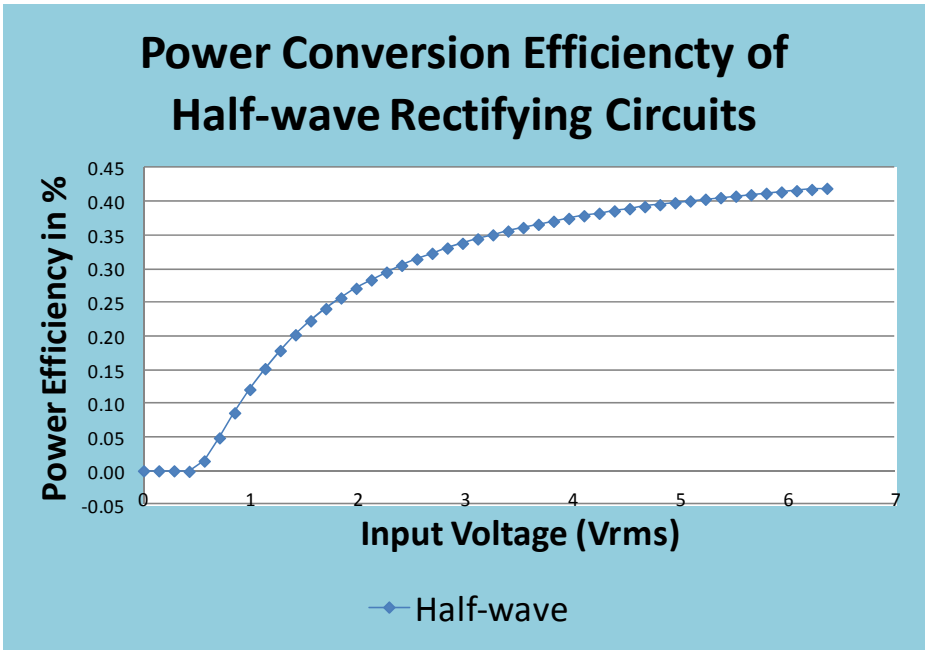

Figure 16 Power Efficiency of Half-wave Rectifier Circuit

2.1.2 FULL-WAVE RECTIFIER CIRCUIT

A single phase full-bridge rectifier circuit is the most common rectifier circuit today. Patented by Karol Pollak, in 1896[24], this circuit is also known as Graetz circuit because it was also being researched by German physicist Leo Graetz. Compared with a single-diode half bridge rectifier circuit, a full-bridge rectifier allows the AC current to flow in both directions to the load, improving the theoretic maximum rectifying efficiency, reducing the output ripple voltage and increasing the reverse voltage breakdown voltage.

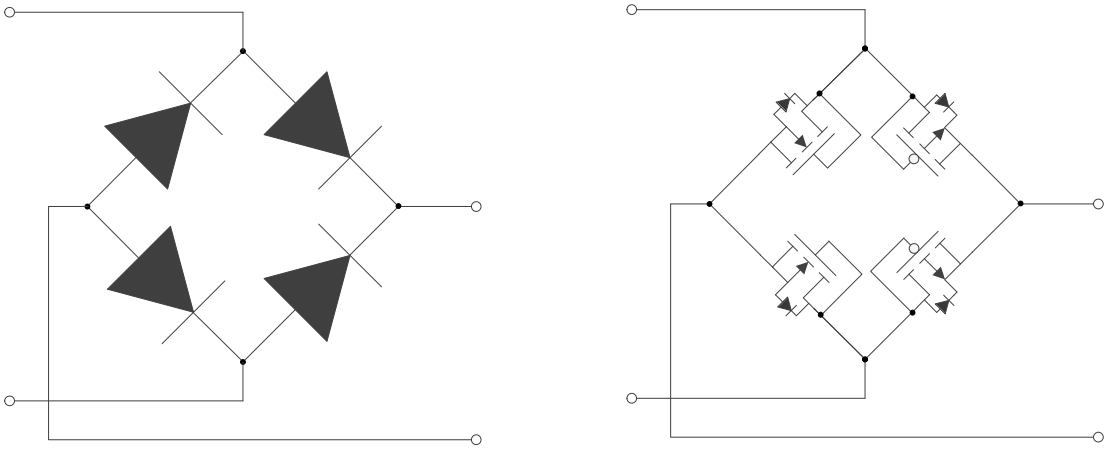

Figure 17 Full-bridge Rectifier Circuit

Figure 17 shows the schematics of the full-bridge rectifier circuit. Figure 17(a) uses four diodes to rectify the AC input current, while Figure 17(b) uses four diode-connected MOSFETs to rectifying the AC input.

2.1.2.1 PRINCIPLE OF FULL-BRIDGE RECTIFIER CIRCUITS

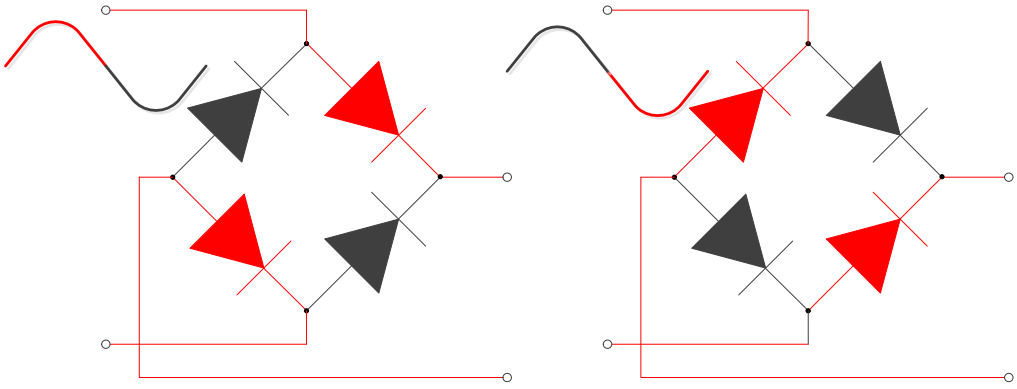

Figure 18 Operation of the Full-bridge Rectifier circuit

The full-bridge rectifier circuit operates very similar to the basic principle of the half-wave rectifier circuit, with the except that the current flows through two diodes instead of one as in the half-wave circuit. Figure 18 shows the current flow directions when the input voltage has different polarities.

2.1.2.2 EFFICIENCY ANALYSIS OF THE FULL-BRIDGE RECTIFIER CIRCUITS

Figure 19 shows the typical waveform of a full-wave rectifying output when its output is heavily loaded. The efficiency of the full-wave rectifier circuit can be analyzed based on the conduction angle of the rectifier circuit:

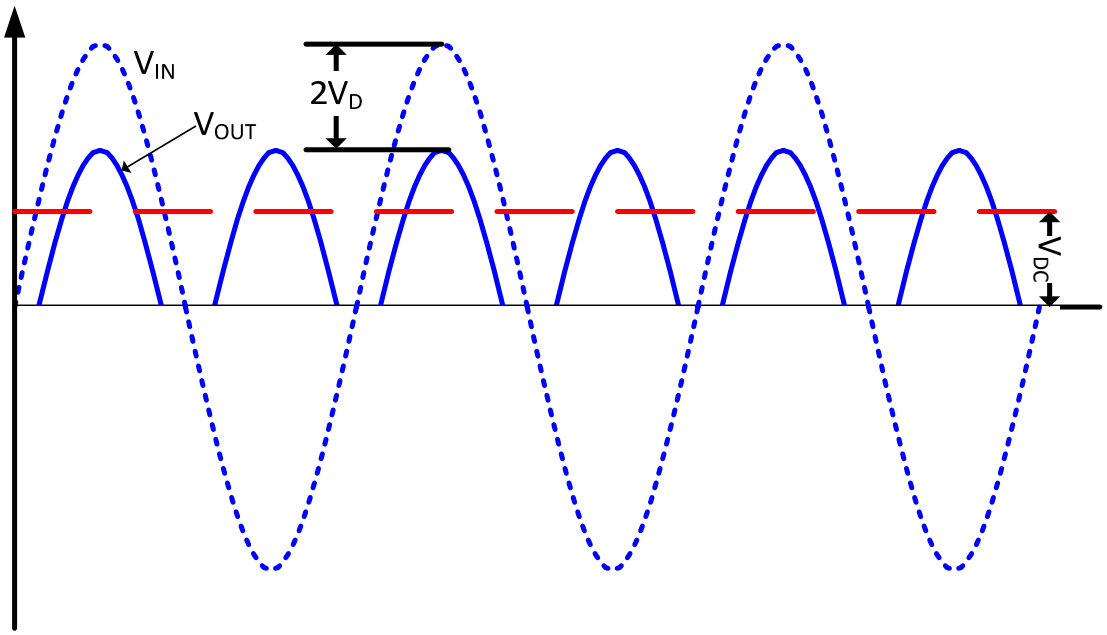

Figure 19 Forward Conduction of a Full-bridge Rectifier

The efficiency of a full-wave rectifier is a function of the input voltage V_m as well as the diode forward voltage drop v_d. Assume the input signal is a sinusoid signal $V_{in}(t)$:

$$V_{in}(t) = V_m \sin(\omega t) \tag{16}$$

$$V_{out}(t) = \begin{cases} V_m \sin(\omega t) - 2v_d, when V_m \sin(\omega t) > 2v_d \\ 0, otherwise \end{cases} \tag{17}$$

The diode conduction on time ωt_{on} and off time ωt_{off}

$$\omega t_{on} = \sin^{-1}(\frac{2v_d}{V_m}) \tag{18}$$

$$\omega t_{off} = \pi - \sin^{-1}(\frac{2v_d}{V_m}) \tag{19}$$

Therefore the conduction angle θ_c is

$$\theta_c = \omega(t_{off} - t_{on}) = \pi - 2\sin^{-1}(\frac{2v_d}{V_m}) \tag{20}$$

The RMS DC output of the rectifier output is therefore:

$$\begin{aligned} V_{RMS} &= \sqrt{\frac{1}{T}\int_0^T V_{out}^2(t)dt} = \sqrt{\frac{2}{T}\int_{t_{on}}^{t_{off}} (V_m \sin(\omega t) - 2v_d)^2 dt} \\ &= \sqrt{\frac{1}{2\pi}(V_m^2 + 8v_d^2)(\pi - 2\sin^{-1}(\frac{2v_d}{V_M}) - \frac{6v_d V_m}{\pi}\sqrt{1-(\frac{2v_d}{V_m})^2}} \end{aligned} \tag{21}$$

The rectifying efficiency η of the full-wave rectifier is therefore:

$$\eta = \frac{V_{RMS}^2}{\left(\frac{V_m}{\sqrt{2}}\right)^2} = \frac{1}{\pi}(1 + \frac{8v_d^2}{V_m^2})[\pi - 2\sin^{-1}(\frac{2v_d}{V_m})] - \frac{12}{\pi}\frac{v_d}{V_m}\sqrt{1-(\frac{2v_d}{V_m})^2} \tag{22}$$

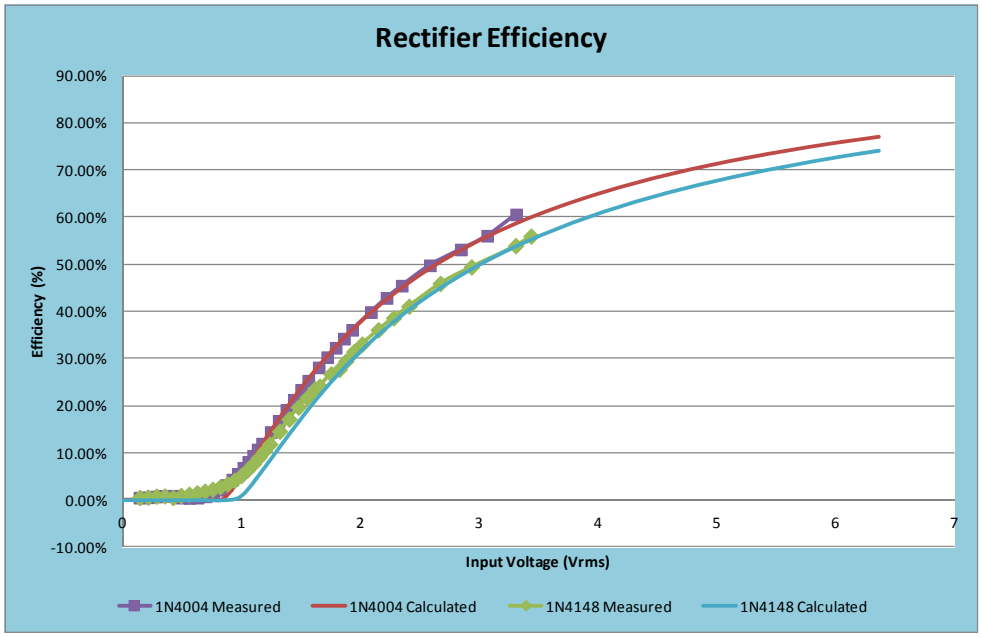

Figure 20 Power Efficiency of Full-bridge Rectifier Circuit

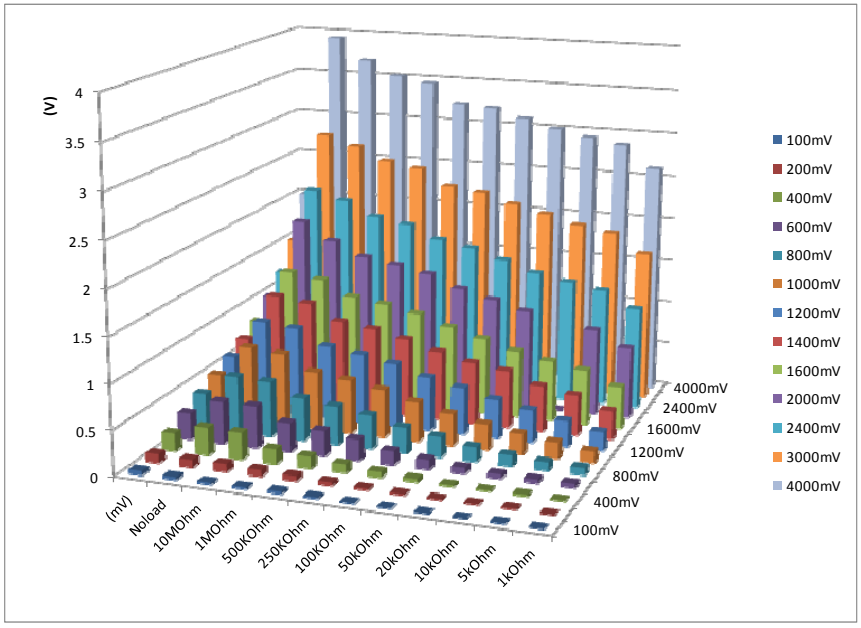

Figure 21 Measured Power Conversion Efficiency for Full-wave 1N4148 Rectifier Circuit

Figure 20 shows the energy conversion efficiency of full-wave rectifier circuit. The full-wave rectifier circuits' power conversion efficiency is calculated and bench tested with the actual diode circuit. Two different kinds of diodes are used for the efficiency measurement with both data fitting well with the calculated efficiency. As shown in Figure 20, the maximum energy conversion efficiency of the full-wave rectifier is 82% but it starts around $2v_d$ input voltage.

Figure 21 shows the actual bench test results for the power conversion efficiency of the full-wave rectifier circuit using 1N4148 signal rectifier diode. The power loss due to the forward voltage drop of the rectifier diode can be easily seen as the output voltage is always lower than the input voltage especially at heavy load conditions.

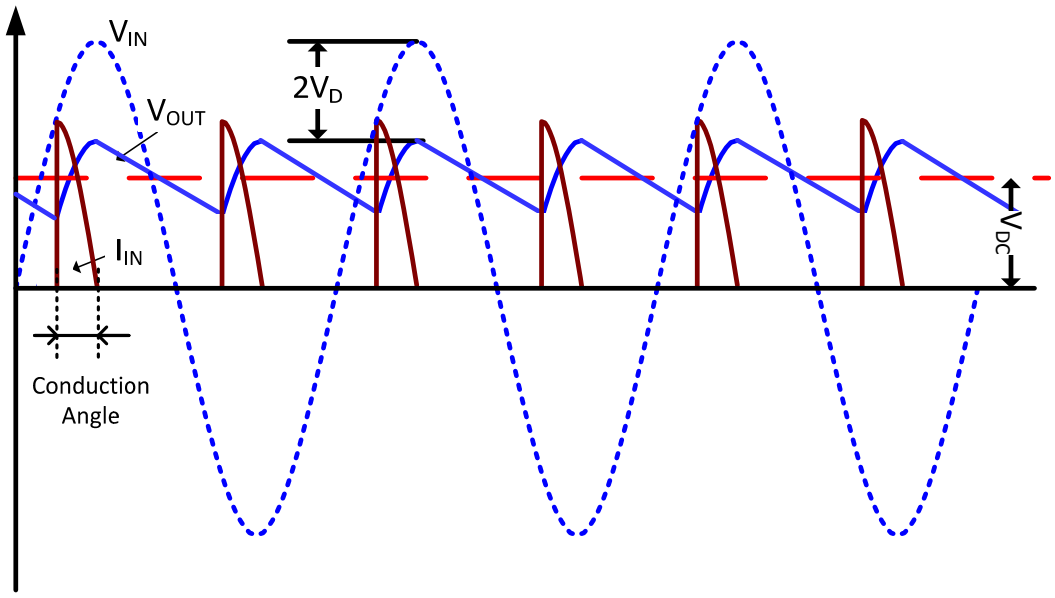

Figure 22 Input Voltage, Input Current and Output Voltage of a Full-wave Rectifier Circuit

Figure 22 shows the input voltage, input current and output voltage waveforms of the full-wave rectifier circuit when its output is connected with an output capacitor and a resistive load. Notice that the output voltage becomes a RC discharging waveform once the input voltage passes it peak voltage. This is due to the reverse bias condition of the rectifier diodes which isolates the input voltage from the output voltage. Also notice that the input current starts conducting when the input voltage is higher than the combined threshold voltages of the rectifier diodes but stops when the rectifier diodes are reverse biased when the input voltage reaches its peak. This low current conduction angle restricts the maximum efficiency of the diode rectifier circuits.

2.2.SYNCHRONOUS RECTIFIER CIRCUIT

A synchronous rectifier is a circuit which uses an active control circuit to time the on and off of switches such as MOSFETs to direct the current flow. Synchronous rectifiers replace diodes with MOSFETs; eliminating the forward voltage drop of the p-n junctions. Instead, the power dissipation of the rectifying switches are mostly dissipated in the internal switch resistance, as well as the circuits which controls the precise timing of the “on”-and-“off” of the active switches. Since most of the active switches are normally-off devices, the operation of the active rectifier requires the control circuit to be functional before any energy from the source can be harvested. Therefore this type of circuit requires a stand-by power supply to keep the control circuit operational before any energy harvesting input can be rectified.

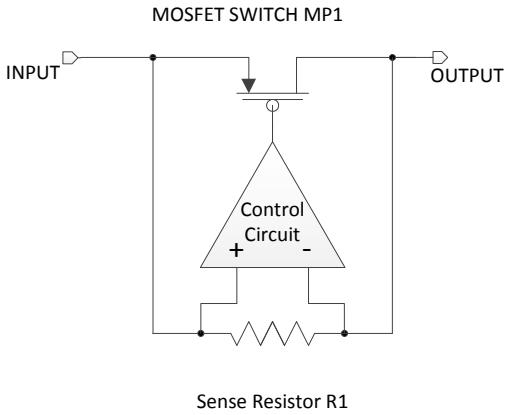

Figure 23 Circuit Diagram for a Synchronous Rectifier

Figure 23 shows a simplified circuit diagram for a current-sensing synchronous rectifier. MOSFET MP1 serves as the main passing element of the harvested energy from input to output. Current sensing resistor R1 senses the current flow and provides the current information to the control circuit. The control circuit turns on or off the passing element to control the current flow. At system power up, the control circuit needs to be “on” to sense the input-output potential difference to turn “on” or “off” the passing element. If the current flow direction is from input to output, the control circuit turns on the passing element. If the current flow direction is from the output to input, the control circuit turns off the main switch.

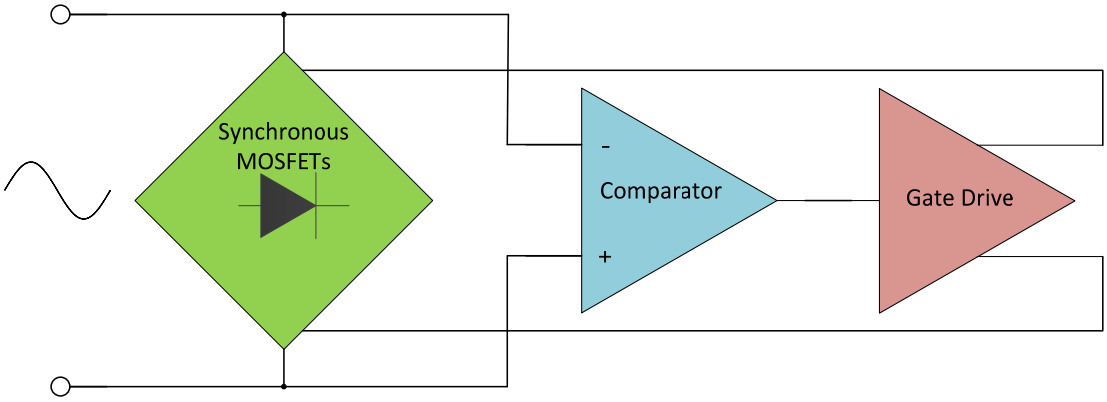

Figure 24 Block Diagram of a Synchronous Rectifier Design

Figure 24 shows a synchronous rectifier circuit designed on a commercial 0.5um CMOS process. Four rectifier MOSFETs are driven by a non-overlapping gate drive circuit, and a low power, high gain comparator circuit senses the polarity of the input voltage which switches on/off the rectifier MOSFETs through the gate drive circuit.

Figure 25 shows the internal connections of the rectifier MOSFET. P-channel MOSFET devices are used for high side switches and N-channel MOSFET devices are used for low side switches to minimize their substrate effects.

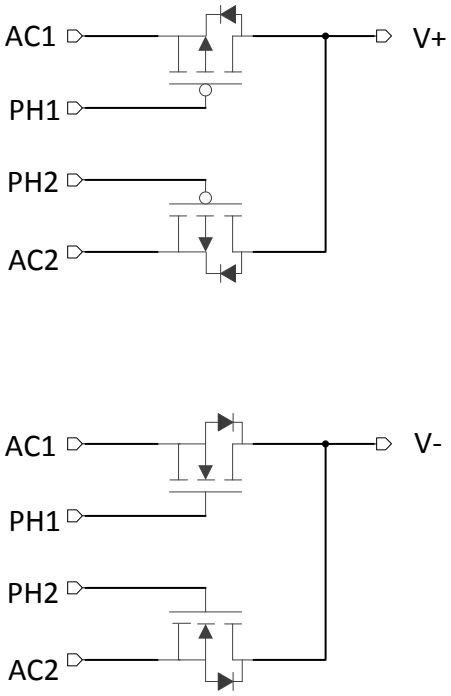

Figure 25 Synchronous Rectifier Diode Bridge

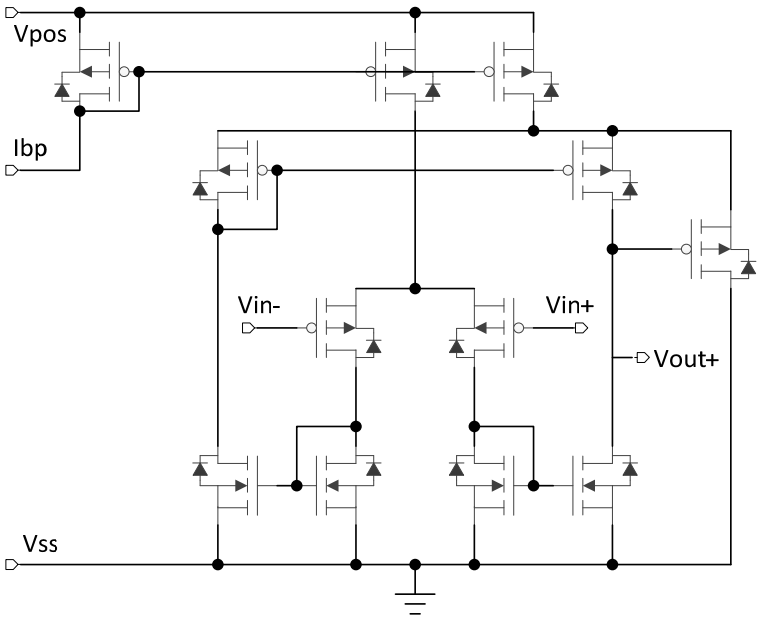

Figure 26 Low Power Voltage Comparator Design

Figure 26 and Figure 27 show the internal circuits of the low power comparator and non-overlap gate drive circuit design. The input voltage polarity is sensed by the low power comparator and the output of the comparator is used to generate a non-overlap gate drive signal to make sure the high side switches and low side switches will never be turned-on simultaneously to avoid a “shoot-through”. The gate drive circuit also helps to increase the turn-on and turn-off of the rectifier diodes to minimize the switching loss.

Figure 28 shows the simulated operation of the synchronous rectifier circuit when there is an auxiliary power supply. The auxiliary power supply provides supply voltage to the synchronous rectifier so the comparator can switch the rectifier diodes with correct timing.

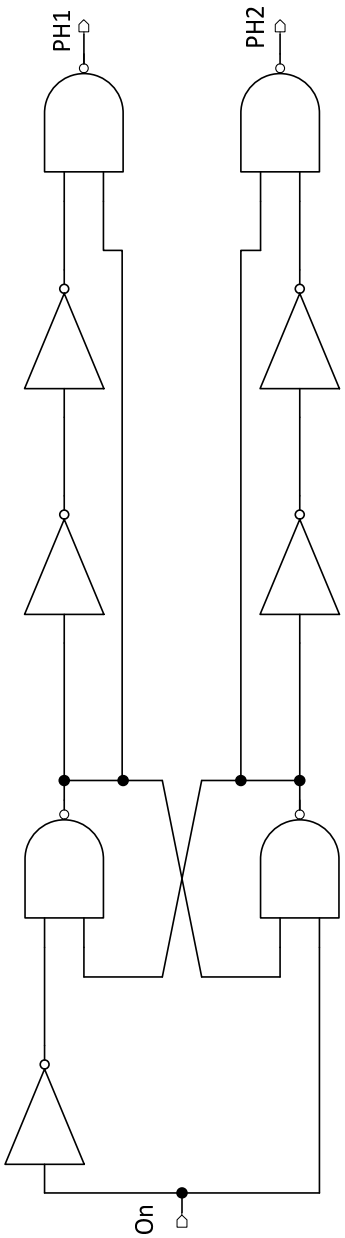

Figure 27 Non-overlap MOSFET Gate Driver Design

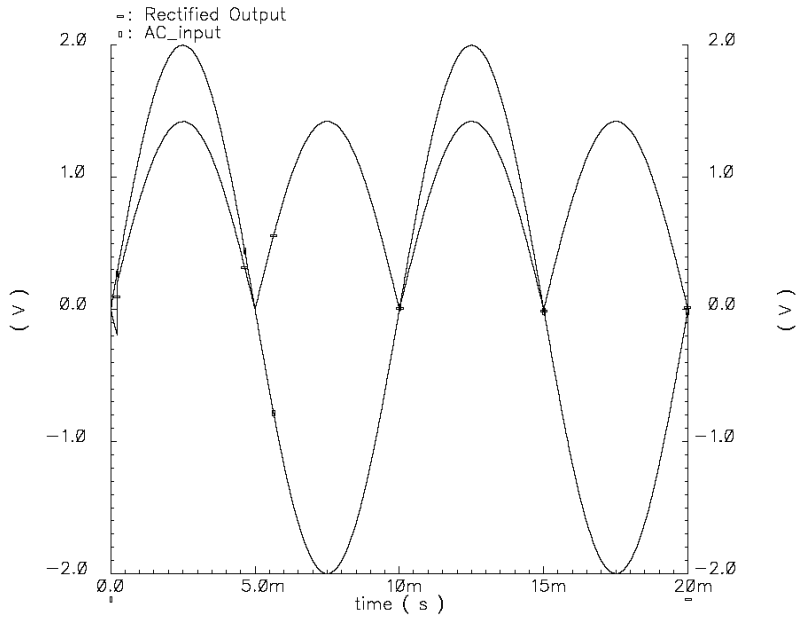

Figure 28 Operation of Synchronous Rectifier with Auxiliary Power Supply

Figure 29 shows the operation of the synchronous rectifier circuit without an auxiliary power supply. Even with the output of the rectifier circuit “boot-strapped” to the synchronous rectifier circuit itself, the random waveform in the rectifier output indicates that without an auxiliary power supply, the comparator circuit cannot reliably initiate the necessary gate drive signal to “self-prime” the synchronous circuit. The lack of ‘cold-start’ capability is one of the important limitations of the synchronous rectifier circuit.

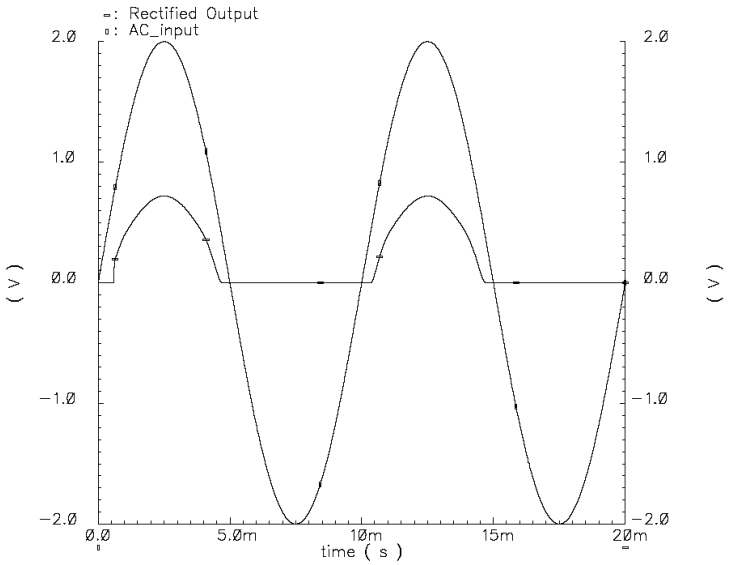

Figure 29 Operation of Synchronous Rectifier w/o Auxiliary Power Supply

The power dissipation of the synchronous rectifier is proportional to the size of the pass element. Assuming the passing element has an R_{dson} of R_s, and the current from the input to the output is $I_{in}=I_{out}=I$ with a resistive load of R_L, the supply voltage of the control circuit is V_c and supply current is I_c. The power conversion efficiency of the synchronous rectifier circuit is therefore:

$$\eta = \frac{I^2 \cdot R_L}{I^2 \cdot (R_L + R_S) + I_C V_C} = \frac{R_L}{R_L + R_S + \frac{I_C}{I^2} V_C} \tag{23}$$

Figure 30 shows the power conversion efficiency of the synchronous circuit. It can be seen that at heavy load conditions, the synchronous rectifier can provide a near ideal power conversion efficiency of 100%, however, this power conversion efficiency drops quickly as the load current drops or the Rdson of the pass element increases. Since many of the energy harvesting devices are low power in nature, the power

consumption of the control circuit could become a large power overhead for the synchronous rectifier circuit and limits its power conversion efficiency.

Another challenge for the synchronous rectifier circuit design is the tradeoff between quiescent power dissipation and the efficiency improvement from the synchronous rectifier circuit. For low power energy harvesting applications, it is therefore important to compare the potential efficiency improvement with the static quiescent power dissipation for the synchronous rectifier controller. The efficiency improvement may not be always justified for the application[25][26][27][28].

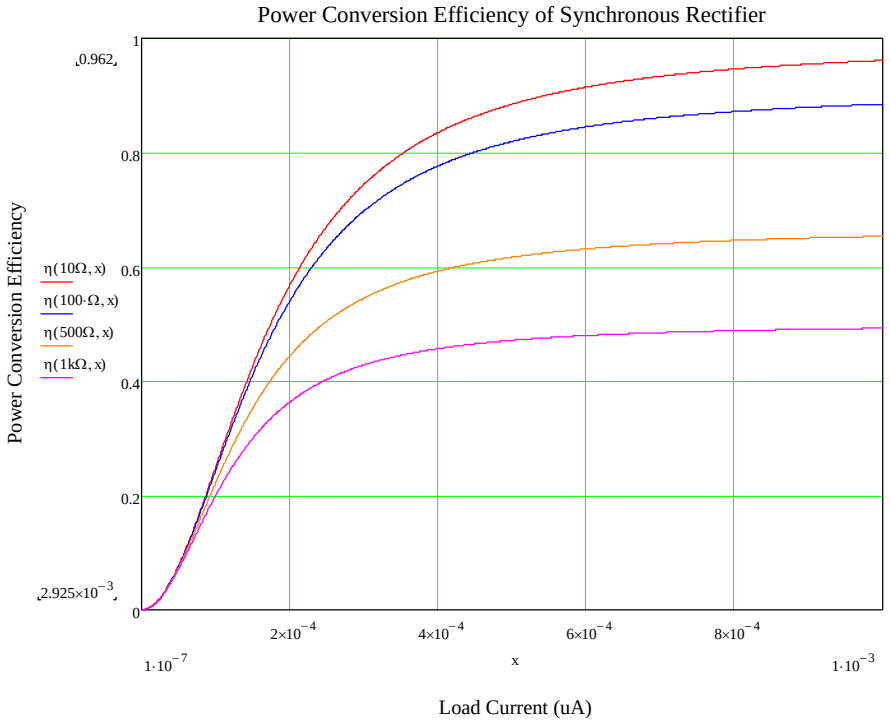

Figure 30 Modeled Power Conversion Efficiency of Synchronous Rectifier Circuit

2.3.FULL-WAVE GATE CROSS-COUPLED RECTIFIER CIRCUIT

A full-wave, gate cross-coupled rectifier uses gate cross-coupled MOSFETs to rectify the AC input to DC output. Figure 31 shows two types of gate cross-coupled rectifier circuits.

In Figure 31(a), MN1 and MN2 are cross-coupled NMOS FETs. One of these two MOSFETs is fully “on” once the input voltage is above its threshold, and the cross-couple connection makes sure only one of these two MOSFETs can be turned on at any given time. MP1 and MP2 are diode-connected MOSFETs which rectify the AC input. Since the input current flows either through MP1 or MP2 to the load, there is always one MOSFET threshold voltage drop in this circuit which limits its power conversion efficiency.

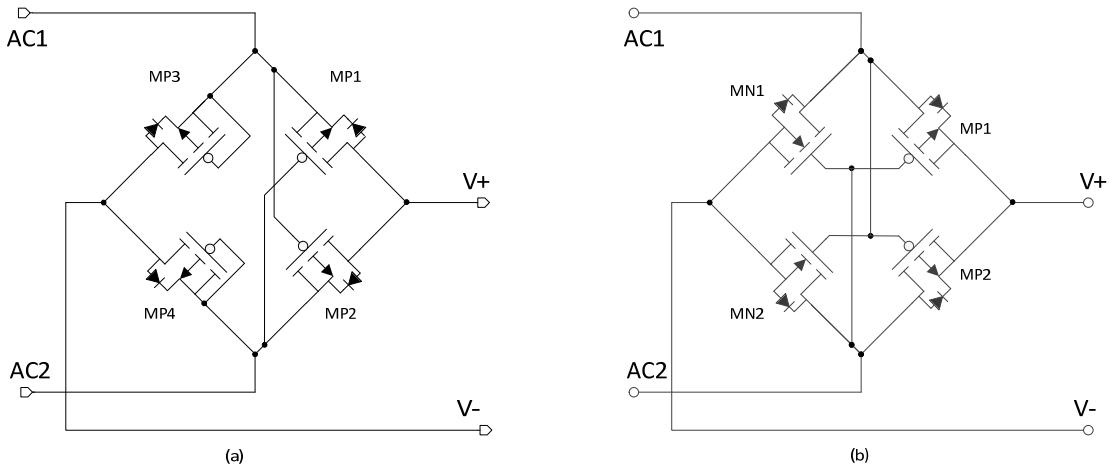

Figure 31 Full-wave Gate Cross-coupled Rectifier Circuit (a) and Full-wave Fully Gate Cross-coupled Rectifier Circuit (b)

In Figure 31(b), all four MOSFETs MP1, MP2 and MN1, MN2 are cross-coupled. Since the turn-on and turn-off the PMOS and NMOS transistors are complementary, the cross-coupling of the P-type and N-type MOSFETs ensures only one of each MOSFET in each connection is in “on” state once the input voltage exceeds the common threshold of the MOSFETs. However, since a MOSFET in its “on” state can conduct current in both directions, this circuit suffers a significant current flow-back issue.

The operation and characteristics of the full-wave, gate cross-coupled rectifier is explained in detail in Figure 32 and Figure 33.

In Figure 32, the AC input is in the positive half cycle. Figure 32(a) shows when the AC input is increasing in amplitude. All MOSFETs are “off” until the gate thresholds are met (assuming PMOS and NMOS have the same gate threshold). Once the input exceeds the threshold voltage of the MOSFETs, in the positive half cycle, MP1 and MN2 conduct and the current from the energy harvesting device starts to charge the load capacitor. Assuming the energy harvesting device has sufficient power to charge up the load capacitor, and the Rdson of the MOSFETs does not significantly reduce the voltage drop between input source and the load capacitor, the output capacitor will be charged to the input peak voltage.

In Figure 32(b), the input voltage starts to drop as the energy harvesting device switching to the negative cycle. During the period when the input voltage is still higher than the gate threshold voltage of the MOSFETs, both MP1 and MN2 are still

on. Since MOSFETs in their “on” states can conduct currents in both directions, the output load capacitor will flow back and charge the energy harvesting device as the input voltage drops to ground potential. This would dissipate the energy harvested during the first quarter cycle and reduce the voltage at the load capacitor to the level of the MOSFET gate threshold.

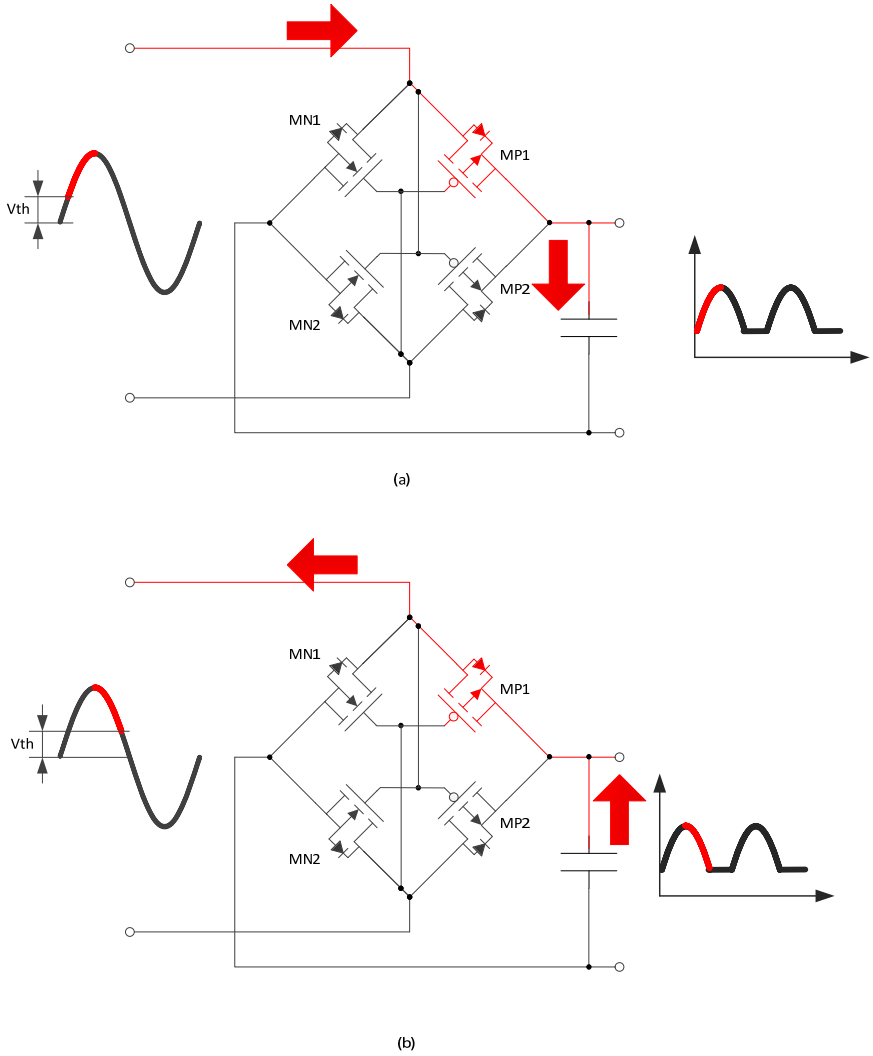

Figure 32 Operational Principle of Full-wave Fully Gate Cross-coupled Rectifier

Figure 33 shows the operation of the same circuit during the negative input cycle. Similarly, the charge built-up during the high input periods will be dissipated when the input voltage swings from the lowest voltage back to zero, leaving the maximum harvested energy on the load capacitor near the threshold voltage of the MOSFETs.

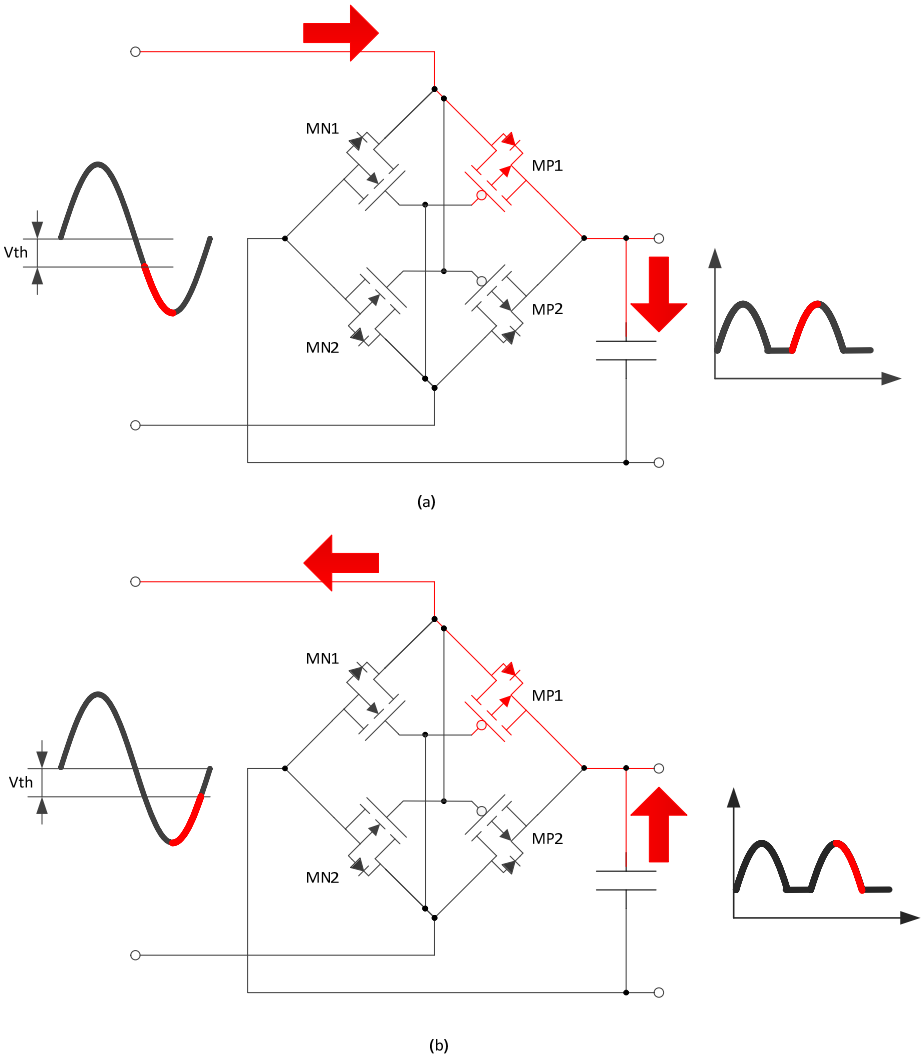

Figure 33 Operational Principal of Full-wave Fully Gate Cross-coupled Rectifier Circuit

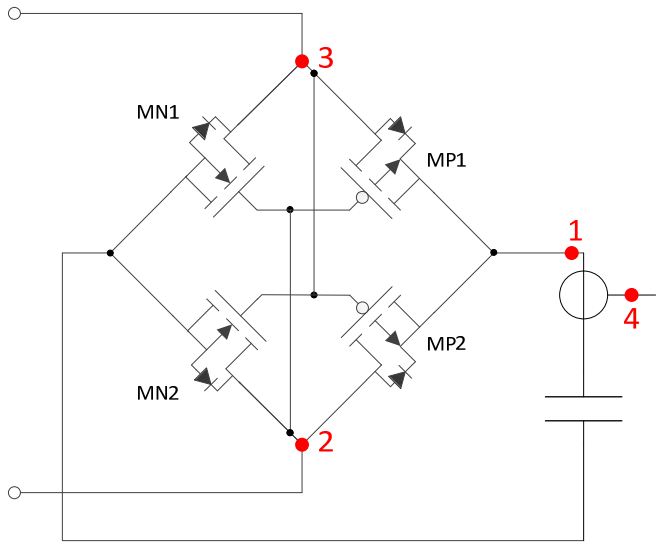

Figure 34 Current "Flow-back" Issue in a Full-wave Fully Gate Cross-coupled Rectifier Circuit, Red Dots Show the Measurement Points

It can be seen that although the gate cross-coupled rectifier can eliminate the gate threshold voltage drop of a diode-connected MOSFET, it cannot prevent the energy back-flow during the period when input voltage drops below the output capacitor. It therefore suffers low power conversion efficiency even without any forward voltage drop from the rectifier MOSFETs.

Figure 34 and Figure 35 show the actual bench measurement of the current back-flow issue in a gate cross-coupled rectifier circuit. Figure 34 shows the different measurement points on the circuit diagram. Node 1 is the output of the rectifier; node 2 and node 3 are the two AC input nodes. Node 4 is the current measurement of the output capacitor. The input of the rectifier is driven by a function generator which

creates a 100Hz 1Vpp sinusoidal wave. The load of this rectifier circuit is a 10uF capacitor.

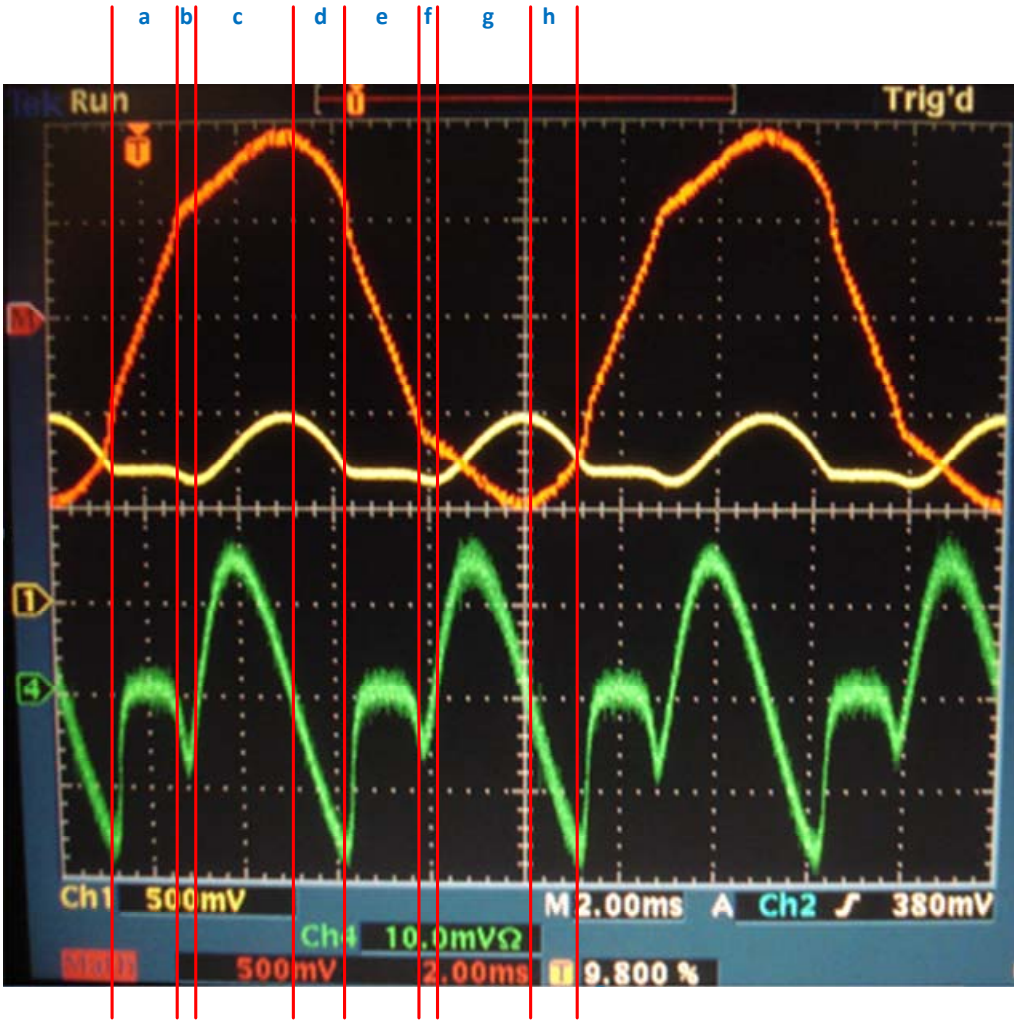

Figure 35 Bench Measurement of the Current Flow-back Issue of the Full-wave Fully Gate Cross-coupled Rectifier Circuit without Virtual Junction

Figure 35 shows the actual measurement result. The orange trace on the top is the actual input voltage between node 3 and node 2. The yellow trace is the voltage

measurement at the output node and the output capacitor. The green trace is the actual current measurement in which the positive direction is charging the output capacitor.

The cyclic waveform can be divided down into 8 segments. During period a, all four MOSFET switches are turn-off due to the AC input voltage of the rectifier circuit being lower than the gate thresholds. There is no load to the function generator therefore the waveform is a segment of a perfect sinusoidal wave. During period b, the voltage of the AC inputs is high enough to turn-on the MOSFET switches. However, the input voltage is lower than the output voltage stored on the output capacitor and the charge stored in the output capacitor back flows into the source, as can be seen by the negative current as well as the dip in the output voltage.

During period c, the input AC voltage exceeds the output capacitor voltage, current starts to charge from the AC input into the capacitor, and the output voltage starts to increase. The waveform is a distorted sinusoidal form due to the limited load-driving capacity of the function generator.

During period d, the input AC voltage starts to decrease but is still above the gate thresholds of the MOSFET switches. The current back flows from the load capacitor to the AC input, dissipating the rectified energy. This can be seen from the negative current flowing out of the capacitor, and the decrease in the output node voltage.

Period e, f, g and h show the similar AC rectifying waveforms when the AC input is in the negative phase.

Figure 35 shows that without a directional current flow, a gate cross-coupled rectifier can rectify the AC input into DC but does not provide good energy converting efficiency. A large portion of the rectified energy commutes back into the energy source during the negative swing of the energy harvesting device, reducing the energy conversion efficiency of this rectifier circuit.

2.4.RECTIFIER WITH V_{TH} CANCELLATION SCHEME

One of the recent developments on improving the power conversion efficiency of rectifier circuits is the MOSFET Vth cancellation circuit. Triet T. Le and Jifeng Han first proposed a reduced diode turn on voltage passive power conversion circuit in 2006[29], Hashemi et al. also proposed a different Vth cancellation circuit in 2012[30].

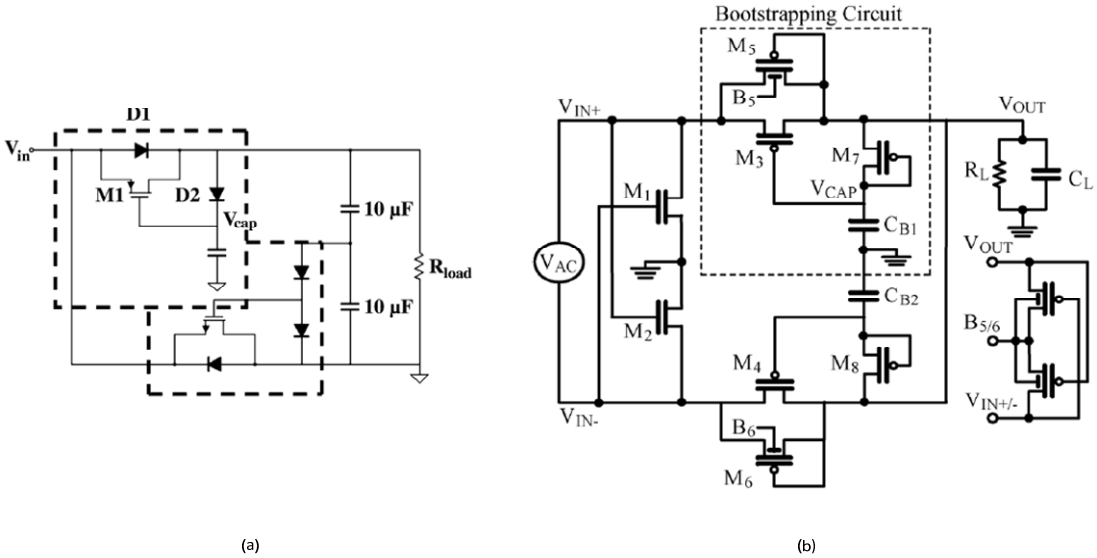

Figure 36 Schematics of MOSFET Rectifiers with Vth Cancellation[18]

Figure 36(a) is the schematic for a passive MOSFET rectifier with Vth cancellation in[20], and Figure 36(b) is another design using diode-connected MOSFETs[18]. The operation principle for both Vth cancellation schemes is similar. The bootstrap caps store charge during the “on” time of the MOSFET, which is used to turn-on the pass element MOSFET in the next “on” cycle.

Vth cancellation schemes can improve the rectifier’s power conversion efficiency by reducing the diode Vth threshold drop if the bootstrap capacitors can be charged to the desired voltage during operation. However, for low voltage low power energy harvesting applications, the duration between each “on” cycle could be longer than the charge holding time of the bootstrap capacitor, making it unpractical for many energy harvesting applications. The energy used to charge the bootstrap capacitor could also be a significant portion of the total energy input, which is dissipated later on as additional power conversion loss.

2.5.SUMMARY

This chapter reviews most of the low voltage current rectifying topologies available today. By examining the circuit operation principle, different circuit characteristics, issues of these rectifier topologies such as p-n junction forward voltage drop, MOSFET substrate effect and the active rectifier’s self-starting issue are discussed. As a summary of this chapter, it is appropriate to compare the power conversion efficiency of the different rectifier circuits presented in this chapter.

Figure 37 summarizes the power conversion efficiency of a few different rectifier circuits from literature and their comparison with ideal half-wave and full-wave rectifier circuits. It can be seen that at very low input voltages (lower than 2.3V), the half-wave diode rectifier has higher power efficiency in comparison with the full-wave rectifier due to less power loss on the forward voltage drop of the rectifier diodes; By introducing Vth cancellation and other techniques, the power conversion efficiencies have been greatly improved especially for low input voltage applications.

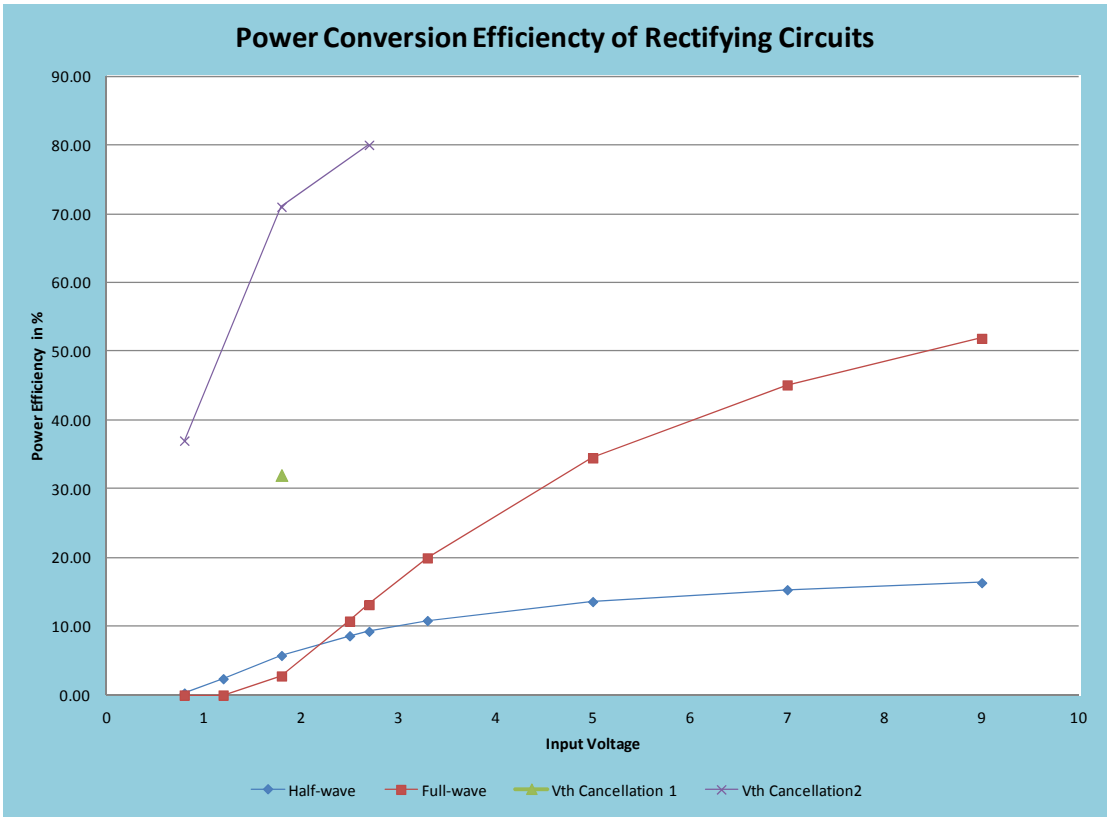

Figure 37 Comparison of the Power Conversion Efficiency of Different Rectifier Circuits

CHAPTER 3. HIGH EFFICIENCY HYBRID RECTIFIER CIRCUIT WITH "VIRTUAL JUNTION"

Although the rectifier circuit is one of the most basic circuits in modern electronics, most of the rectifier circuits today are developed for input voltages high enough that the efficiency loss of the rectifying elements are in-significant. However, since many of the energy harvesting applications are low power and low-energy in nature, traditional rectifier circuits would not able to meet the power conversion efficiency requirement of the applications. In some cases, the majority of the harvested energy would be dissipated in the rectifying stage which makes the energy harvesting in these applications not practical at all. It is therefore very important to develop a high efficiency, self-starting, AC to DC current rectifier circuit for low voltage, low power energy harvesting applications. In this chapter, a new hybrid rectifier circuit using a gate-coupled MOSFET rectifier and a virtual junction is proposed. Different from any of the existing rectifier circuits, this new low power rectifier circuit mitigates many of the limitations of the existing rectifier circuits discussed in the previous chapter. This chapter presents the circuit description, operating principle, and bench measurement result of this new high efficiency rectifier circuit.

3.1.EFFICIENCY LOSS OF THE TRADITIONAL RECTIFIER CIRCUITS

The efficiency losses of traditional rectifier circuits are associated with the principles of the rectifier circuits.

3.1.1 P-N JUNCTION DIODE RECTIFIER CIRCUIT

The operating principle of the diode rectifier circuit is the p-n junction's built-in potential. As shown in figure 6, the built-in potential of a p-n junction prevents the reverse current from commuting across the junction, and it also accounts for the main power loss in the forward direction. The built-in potential of a p-n junction is determined by the doping density and the intrinsic carrier concentration N_i:

$$V_i = \frac{kT}{q} \ln\left(\frac{N_P N_N}{N_i^2}\right) \tag{24}$$

And the intrinsic carrier concentration is a function of the material property

$$N_i = N_s e^{-\frac{E_g}{2kT}} \tag{25}$$

Where N_S is the number per unit volume of effectively available states of the material, E_g is the energy bandgap between the bottom of the conduction band and the top of the valence band. Both are the basic material properties of the semiconductor material. For example, the built-in potential for a silicon p-n junction is around 0.6V. Figure 38 shows the power conversion efficiency for the silicon diodes when the input voltage varies from 0~9V. Due to the fixed diode forward voltage drop built-in to the p-n junction itself, a half bridge circuit has higher power conversion efficiency when input voltage is less than 2.3V. At input voltages higher than 2.3V, a full-wave rectifier circuit would have better power conversion efficiency than the half-wave rectifier circuit. Nevertheless, the low power conversion efficiency significantly

reduces the overall energy harvesting efficiency, making these types of rectifier circuits not suitable for low voltage, low power energy harvesting applications.

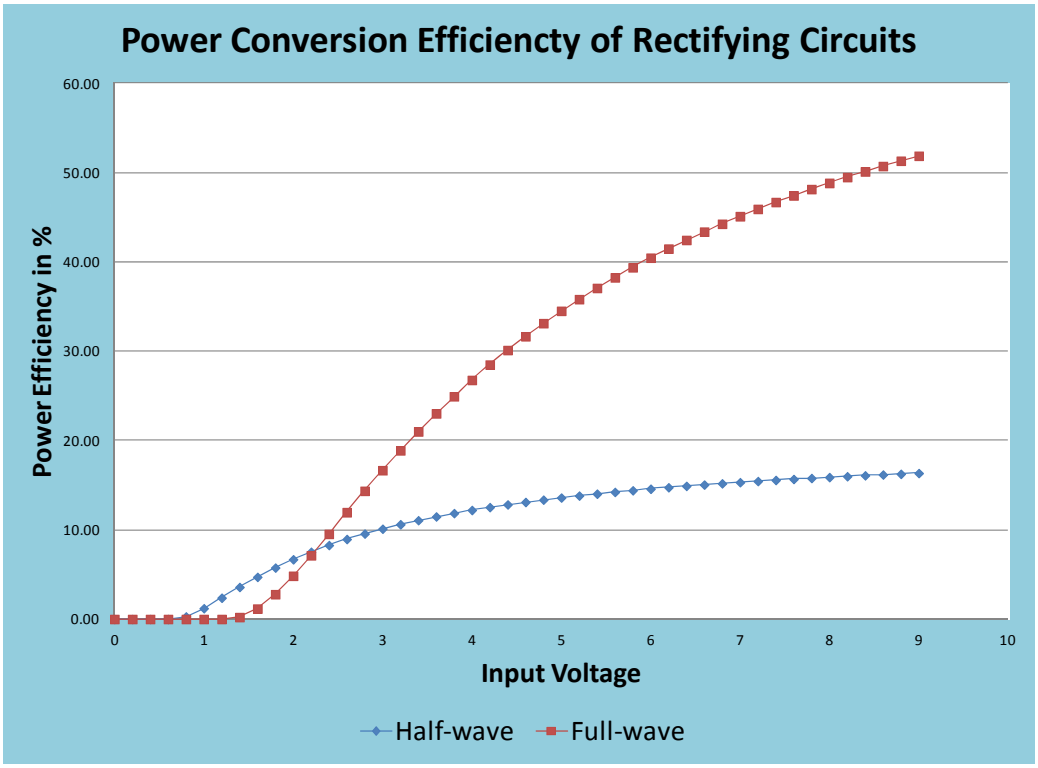

Figure 38 Modeled Power Conversion Efficiencies of Two Different Rectifier Circuits

3.1.2 MOSFET RECTIFIER CIRCUIT

A diode-connected MOSFET can be used to improve the power conversion efficiency of half-wave or full-wave rectifier circuits. Instead of being determined by the basic material property, the forward voltage drop of a diode-connected MOSFET is the gate

threshold, which can be adjusted in the manufacturing process, providing an approach to optimize the system design.

However, in addition to the substrate effect discussed in chapter 2, all practical MOSFETs suffer a sub-threshold conduction issue and a gate threshold variation issue which affect the power conversion efficiency for rectifier circuits using diode-connected MOSFETs.

3.1.2.1 MOSFET GATE THRESHOLD VARIATION ISSUE

The gate threshold of the MOSFET is the function of many process-related parameters as shown in Figure 39.

$$V_T = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \tag{26}$$

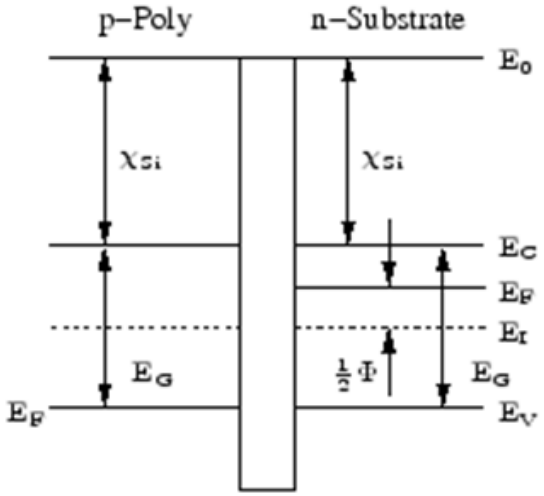

Figure 39 Energy Band Diagram of a P-Poly Gate MOSFET

Φ_{ms} is the work function potential difference of the gate conductor and is determined by the choice of the gate material. ϕ_F is the flat band potential depends on the substrate doping. Q_i is the interfacial charge which can be reduced by the choice of crystal orientation (modern CMOS processes use (100) wafer orientation). Q_d is the charge introduced by threshold adjustment implantation. C_i is the MOS capacitor and depends on the gate oxide thickness and material.

The intrinsic MOSFET threshold voltage fluctuation varies with process technology and a six-sigma of 90mV is considered normal[31]. This restricts the minimal MOSFET threshold voltage required in a rectifier circuit to prevent reverse current flow. For example, the native n-channel MOSFET has a zero or even negative gate threshold. Although a zero-threshold MOSFET would ideally perform like an ideal diode without the forward voltage drop, any gate threshold variation would affect the rectifying performance of the diode-connected device by allowing negative current to flow from the load to the source. This energy "flow-back" would severely impact the rectifying efficiency of the diode-connected rectifier. It is therefore important to specify a minimal range of the MOSFET gate threshold to make sure the diode-connected MOSFETs.

3.1.2.2 MOSFET SUB-THRESHOLD CONDUCTION

Unlike ideal switches, all MOSFETs suffer sub-threshold conduction, the capability for the MOSFET to continue conducting current even when the gate potential of the

MOSFET is below its threshold voltage. Figure 40 illustrates the MOS capacitance when the gate of an N-channel MOSFET is biased below its threshold. Cox is the oxide capacitance between the gate terminal and the channel. C_{dp} is the depletion capacitance. Any voltage applied to the MOSFET gate terminal is divided between these two capacitances and affects the surface potential.

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{ox}}{C_{ox} + C_{dp}} = \frac{1}{\mu} \tag{27}$$

$$\eta = 1 + \frac{C_{dp}}{C_{ox}} \tag{28}$$

Integrating Eq. 30 yields

$$\varphi_s = \frac{V_g}{\eta} + c \tag{29}$$

Where c is a constant.

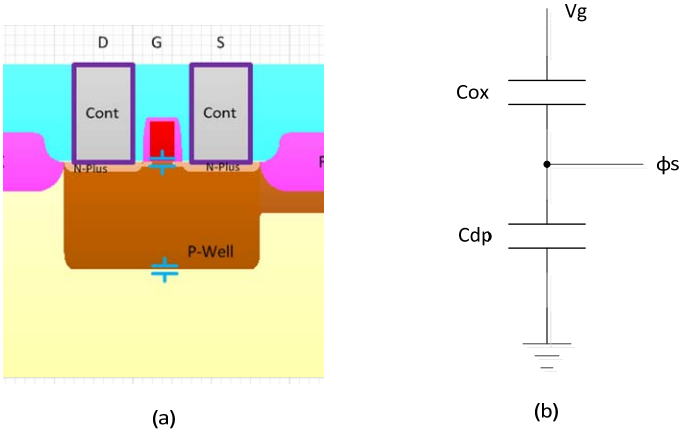

Figure 40 Diagram of the Gate to Substrate Capacitance

The drain to source current can then be expressed as proportional to the surface carrier density Ns

$$I_{ds} = cN_s = ce^{\frac{q\phi_s}{kT}} = ce^{\frac{q(\frac{V_g}{\eta}+c)}{KT}} = ce^{\frac{qV_g}{\eta KT}} \tag{30}$$

Figure 41 shows the current from the drain to the source of a MOSFET when there is a finite gate voltage applied to the MOSFET below its turn-on threshold, alternatively known as subthreshold current. The exponential relationship indicates the channel current decrease linearly with the logarithm of the gate voltage. For practical MOSFETs, their subthreshold currents reduce 10x every 80mV as shown in Figure 41[32].

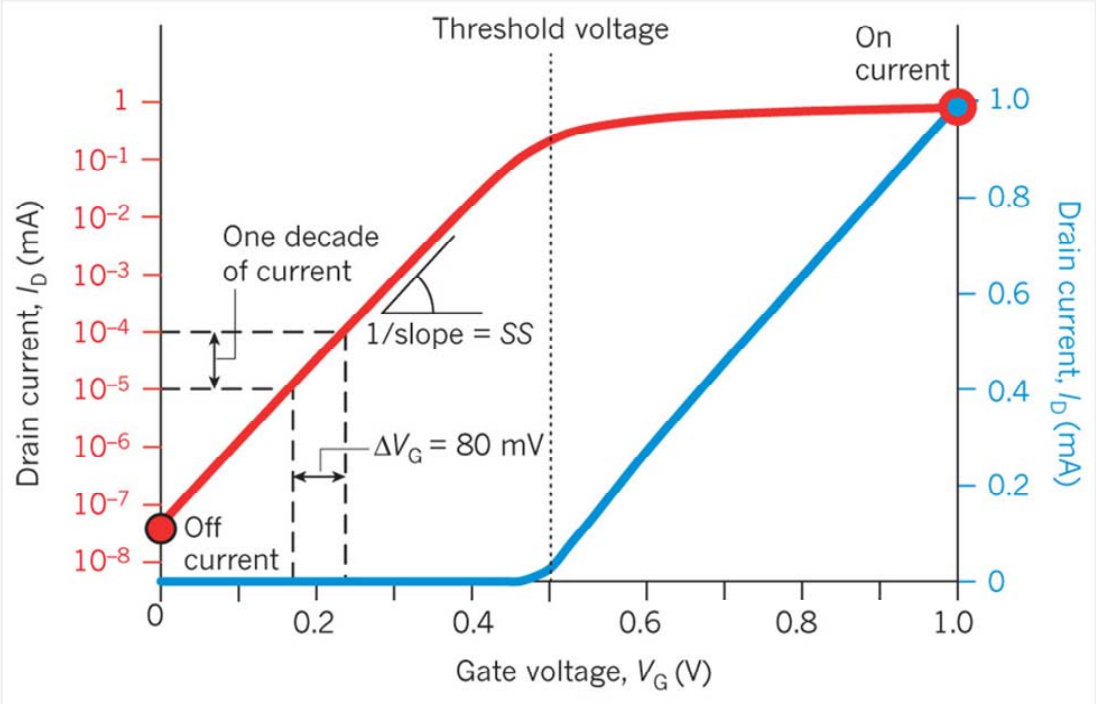

Figure 41 MOSFET Subthreshold Conduction[32]

The MOSFET substrate conduction issue is one important factor to consider in choosing the proper MOSFET gate threshold voltage for low voltage, low power energy harvesting applications. For example, if the subthreshold current reduces 10x every 80mV, which is equivalent to 15.8x every 100mV, a MOSFET needs to have a gate threshold of 400mV to achieve 10^5 on/off current ratio. That means the minimal gate threshold for a MOSFET needs to be around 400mV.

If a MOSFET with a gate threshold voltage lower than 400mV is used as the rectifying element, the high "off" state current is likely to cause excessive leakage when the MOSFET switch is in its "off" state, reducing the power conversion efficiency of the rectifier circuit.

3.1.2.3 THE BIDIRECTIONAL CURRENT FLOW IN MOSFETS

When a MOSFET is biased in its "ON" state, it will be able to pass current from both its drain terminal to its source terminal and its source terminal to its drain terminal. In other words, contrary to a p-n junction diode, a MOSFET will conduct current bi-directionally when it is in its "on" state. The difference of creating directional current flow is caused by the difference in the basic device structures.

Figure 42 shows the difference in the energy band diagrams of diode and P-channel MOSFET in both zero-bias and forward conduction mode. Notice that the symmetric device structure of the MOSFET requires the channel to be inverted for the MOSFET to be in conduction. However, once the channel is inverted, there is no potential

barrier to prevent the majority carrier to flow in either direction. This is the main cause for the power loss in the gate-coupled MOSFET rectifier topology.

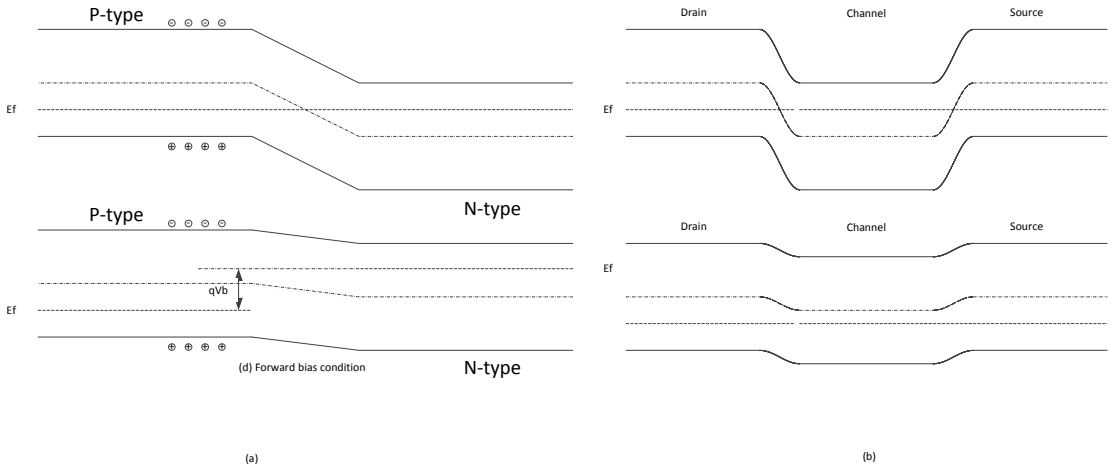

Figure 42 Energy Band Diagram Comparison of Diode and MOSFET both in Zero-Bias and Forward Conduction

In the p-n junction diode structure, on the other hand, the built-in junction potential prevents the majority carriers from flowing back in the reverse direction, which creates a uni-directional current flow. Meanwhile, this built-in junction also accounts for the energy loss for the majority carriers flowing in the forward direction, which is the source of the power loss of a diode rectifier circuit.

3.2.HYBRID RECTIFIER CIRCUIT WITH A PROPOSED "VIRTUAL JUNCTION"

To improve the power conversion efficiency of the rectifier circuit, a new hybrid rectifier circuit with a virtual junction is proposed in this dissertation. This circuit

takes advantage of “input-drive” of the gate-coupled rectifier circuit and the uni-directional current flow of a junction with built-in potential, and eliminates the current “flow-back” issue in a MOSFET switch and high forward power loss on the p-n junction diode. This significantly improves the energy conversion efficiency of the current rectifying process.

Figure 43 shows the energy band diagram of the new hybrid rectifier using a P-channel MOSFET. In this circuit, a fixed potential difference is introduced on the drain side of the P-channel MOSFET, creating an artificial junction which prevents current back-flow. In the meantime, since this junction is developed by an external bias voltage, it can be regulated to a lower potential level which minimizes the unnecessary power loss of the p-n junction. A similar circuit can be used with N-channel MOSFETs, although the substrate effect makes P-channel MOSFETs more suitable for high-side switch applications.

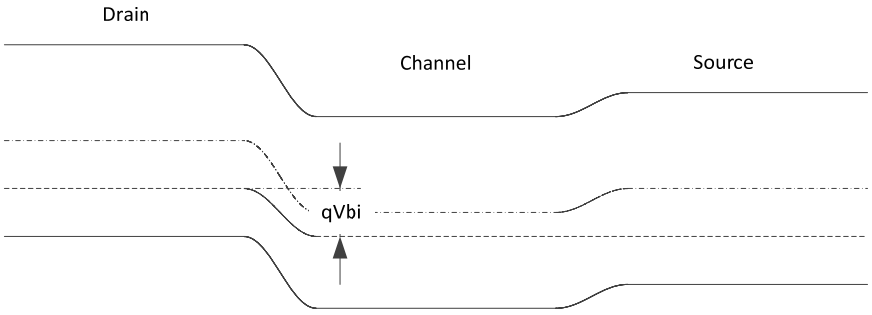

Figure 43 Energy Band Diagram of the Hybrid Rectifier of a P-channel MOSFET with Virtual Junction

Figure 44 shows the typical waveform of a hybrid rectifier circuit. Assuming a v_t=0.35V threshold and MOSFETs are used with a 50mV fixed junction voltage, the efficiency of a hybrid rectifier is a function of the input voltage V_m as well as the artificial junction potential drop v_j. Assume the input signal is a sinusoid $V_{in}(t)$:

$$V_{in}(t) = V_m \sin(\omega t) \tag{31}$$

$$V_{out}(t) = \begin{cases} V_m \sin(\omega t) - v_j, when V_m \sin(\omega t) > v_t \\ 0, otherwise \end{cases} \tag{32}$$

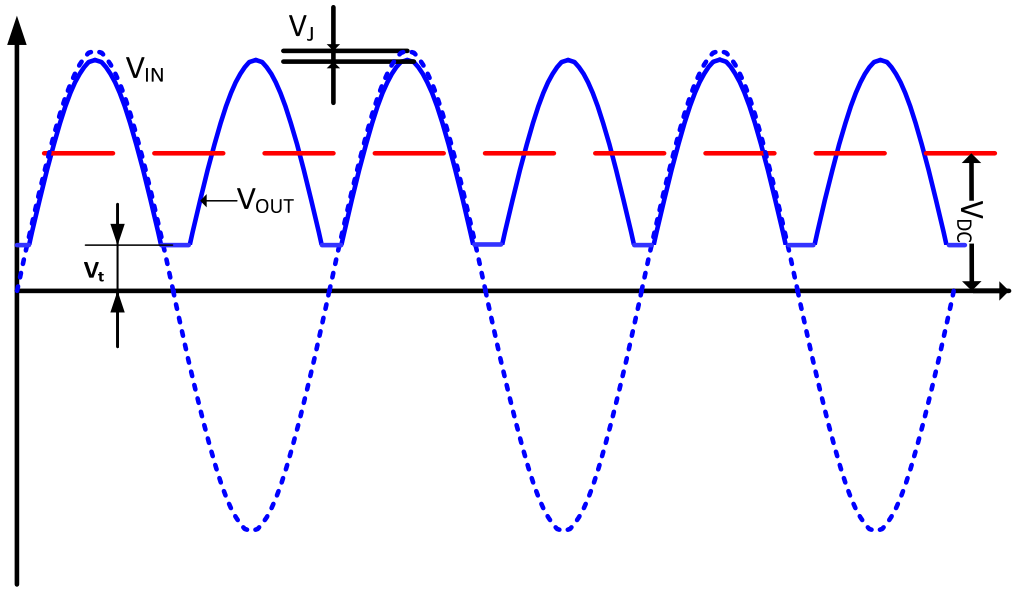

Figure 44 Forward Conduction of a Hybrid Rectifier with Virtual Junction

The diode conduction on time ωt_{on} and off time ωt_{off}

$$\omega t_{on} = \sin^{-1}(\frac{v_t}{V_m}) \tag{33}$$

$$\omega t_{off} = \pi - \sin^{-1}(\frac{v_t}{V_m}) \tag{34}$$

Therefore the conduction angle θ_c is

$$\theta_c = \omega(t_{off} - t_{on}) = \pi - 2\sin^{-1}(\frac{v_t}{V_m}) \tag{35}$$

The average DC output of the rectifier output is therefore:

$$V_{dc} = \frac{1}{T}\int_0^T V_{out}(t)dt = \frac{2}{T}\int_{t_{on}}^{t_{off}}(V_m \sin(\omega t) - v_j)dt = \frac{2V_m}{\pi}[\sqrt{1-\frac{4v_t^2}{V_m^2}} - \frac{\theta_c}{2}\frac{v_j}{V_m}] \tag{36}$$

The RMS voltage of the rectifier output is therefore:

$$V_{rms} = \sqrt{\frac{1}{\pi}((\frac{V_m^2}{2}+v_j)[\pi - 2\sin^{-1}(\frac{v_t}{V_m})] - V_m v_t\sqrt{1-(\frac{v_t}{V_m})^2} - 4V_m v_j\sqrt{1-(\frac{v_t}{V_m})^2}} \tag{37}$$

The rectifying efficiency η of the half-wave rectifier is therefore:

$$\eta = \frac{2}{\pi}\{(\frac{1}{2}+\frac{v_j^2}{V_m^2})[\pi - 2\sin^{-1}(\frac{v_t}{V_m})] - \frac{v_t}{V_m}\sqrt{1-(\frac{v_t}{V_m})^2} - \frac{4v_j}{Vm}\sqrt{1-(\frac{v_t}{V_m})^2}\} \tag{38}$$

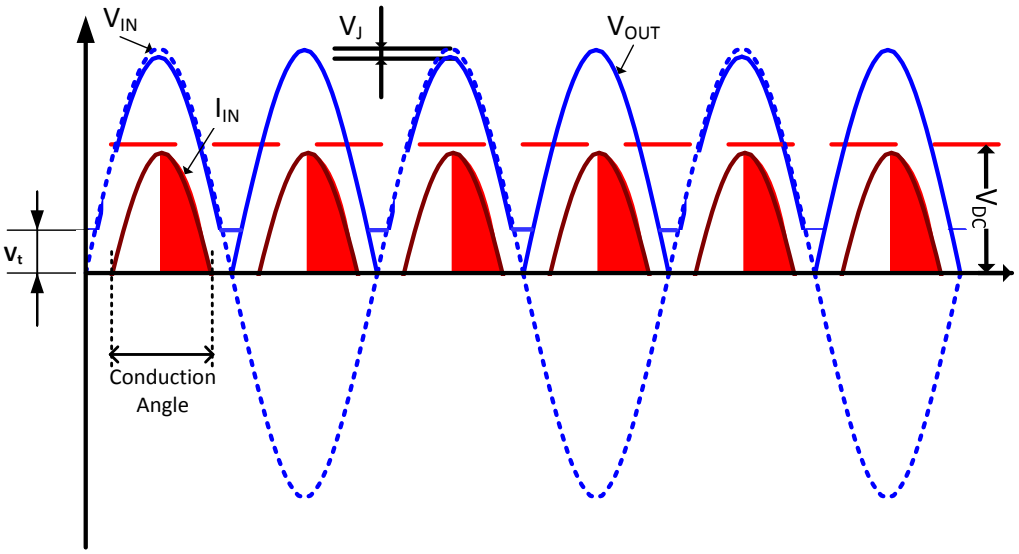

Figure 45 Input Voltage, Input Current and Output Voltage Waveforms of a Hybrid Rectifier Circuit

Figure 45 shows the waveforms of the input voltage, input current and the output voltage of a hybrid rectifying circuit. Notice the current conduction angle is much larger in comparison with the full-wave rectifier circuit shown in Figure 22, which accounts for the higher power conversion efficiency of the hybrid rectifier circuit.

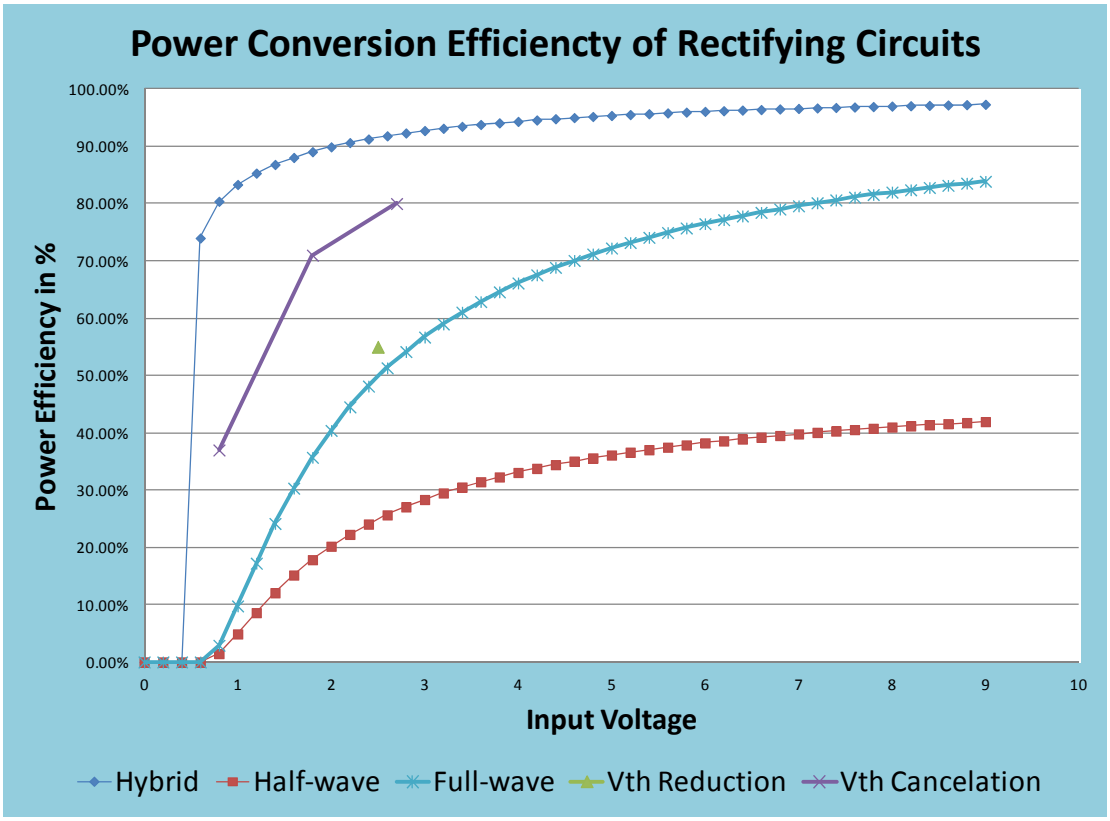

Figure 46 Modeled Efficiency Comparison of the Hybrid Rectifier with Virtual Junction

Figure 46 shows the power conversion efficiency of a few low voltage rectifier circuits. The power conversion efficiency for the hybrid, half-wave and full-wave rectifier circuits are theoretical, while the Vth reduction and Vth cancellation are

reported from literature. It can be see that hybrid rectifier circuit provides the highest rectifying efficiency, especially in the low voltage and low power applications.

3.3.IMPLEMENTATION AND TEST RESULT FOR A HYBRID RECTIFIER CIRCUIT WITH THE “VIRTUAL JUNCTION”

A circuit implementation of the hybrid rectifier circuit with a virtual junction can be implemented as shown in Figure 47.

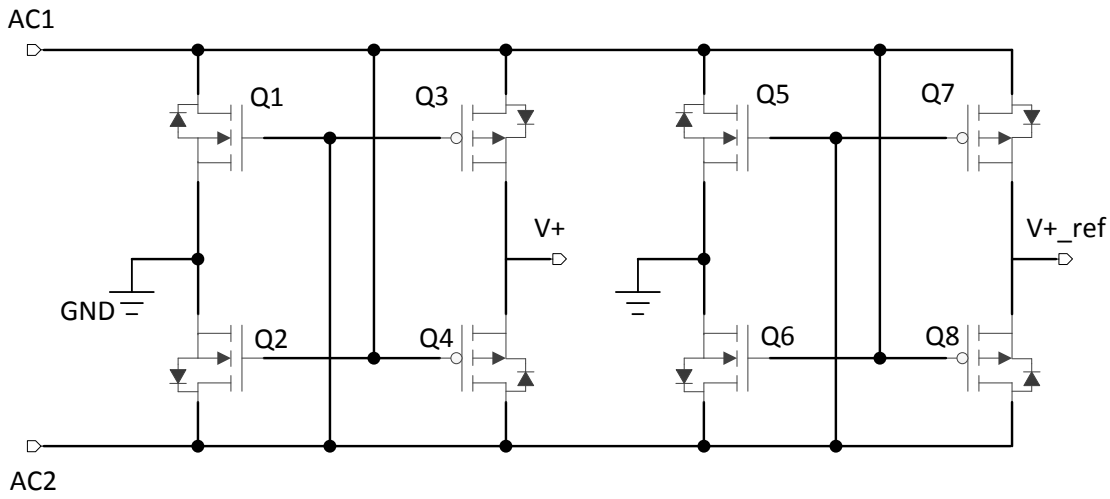

Figure 47 Circuit Implementation of Hybrid Rectifier Circuit with Virtual Junction

In Figure 47, Q1, Q2, Q3 and Q4 comprise a gate cross-coupled rectifier with inputs of AC1 and AC2, and outputs at V+ and GND. A mirror circuit Q5, Q6, Q7 and Q8 duplicates the input and output of the gate cross-coupled rectifier circuit with output

at V+_ref. V+_ref closely tracks V+ except it is not loaded with the rectifying current.

During current rectifying operation, the downstream voltage boosting circuit (shown in Figure 104) uses the reference voltage at V+_ref to calculate a percentage value at which the boost circuit will use to regulate the V+ voltage, for example, 95%. This will create potential differences between the sources and drains of the rectifier MOSFETs Q1, Q2, Q3 and Q4 to form virtual junctions in the current conducting MOSFETs, resulting in the current rectifying with high power conversion efficiency.

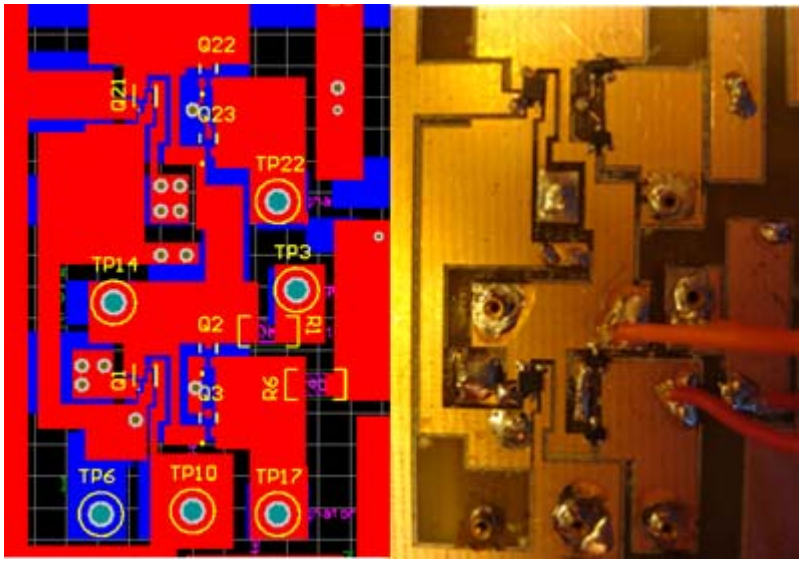

Figure 48 Circuit Layout of Hybrid Rectifier Circuit with Virtual Junction

Figure 48 shows the actual prototyping circuit for measuring the current rectifying efficiency of the hybrid rectifier circuit with virtual junctions.

Figure 49 Input Current Waveform for Hybrid Rectifier Circuit with Virtual Junction

Figure 49 shows the input waveforms for the hybrid rectifier circuit with a virtual junction. Channel 1 (orange trace) shows the input voltage, channel 2 (yellow trace) shows the output voltage of the rectifier. Channel four (green trace) shows the input current. Comparing with Figure 35, it can be seen that the input current flows only in one-direction, and there is no commuting current which flows back to the source.

The efficiency of the hybrid rectifier circuit with virtual junctions is measured using the circuit shown in Figure 47 and Figure 102. When 350mV gate threshold MOSFETs are used with 5% virtual junction voltage and a 19.75Ohm resistive load in parallel with a 4.7uF capacitive load, the measurement result on the rectifying

efficiency matches closely with the theoretical prediction. The rectifier circuit starts up with 10% rectifying efficiency at approximately 350mV (rms) input voltage. At approximately 600mV (rms) input voltage, the hybrid rectifier circuit reaches power conversion efficiency of 63.3%. At this supply voltage, most of the p-n junction diodes are barely conducting. The rectifier circuit's power efficiency reaches 90% for any input voltage which is higher than 900mV.

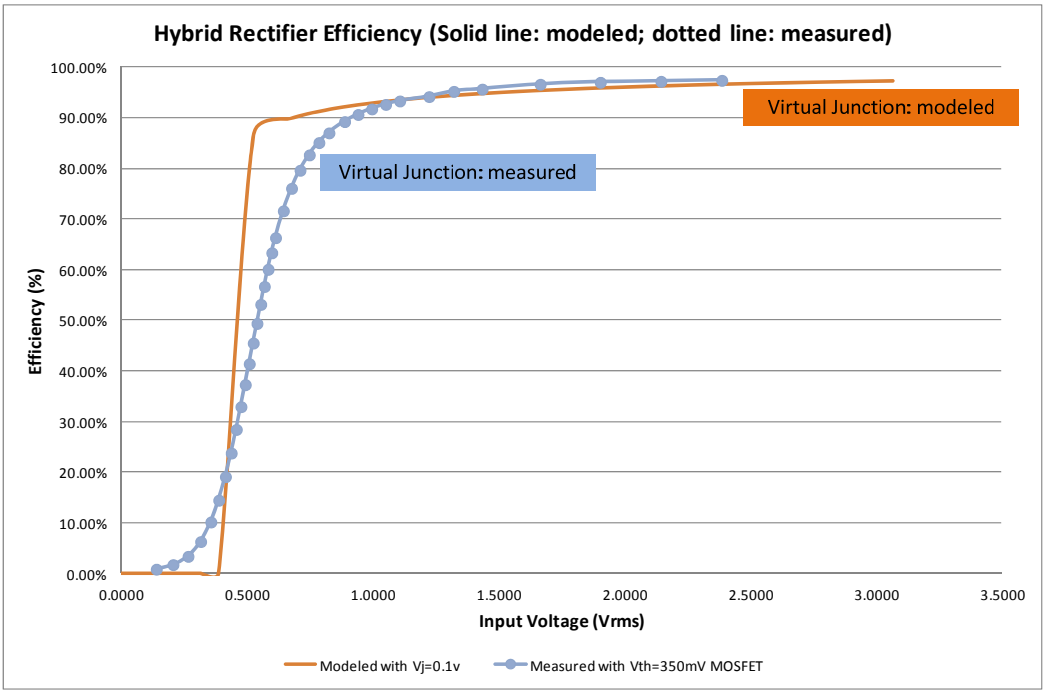

Figure 50 Rectifying Efficiency Measurement of Hybrid Rectifier circuit with Virtual Junctions

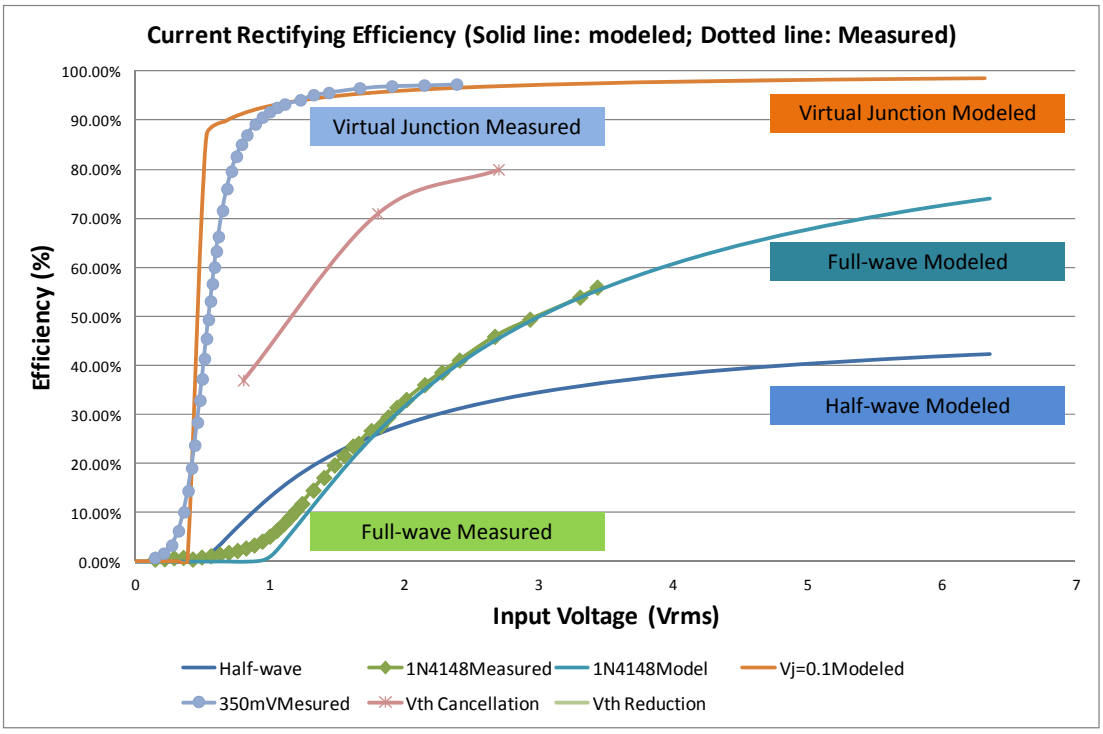

Figure 51 Comparison of Power Conversion Efficiency of Different Rectifier Circuits

Figure 51 shows the comparison of the power conversion efficiencies of different current rectifier circuits. Solid lines are the calculated based on theoretical analysis and dotted lines are actual bench measurement results. The bench measurement results show that the hybrid rectifier circuit has higher current rectifying power conversion efficiency than any other current rectifying approaches from current literature

3.4. SUMMARY

This chapter investigates the main reasons which limit the power conversion efficiency for low power and low voltage applications. Although p-n junction diodes have been widely used for power rectifier circuits, the forward voltage drop of a p-n junction diode is a significant source of power loss in low voltage applications. MOSFETs, on the other hand, provide some improvement to this problem due to the flexibility of gate threshold voltage. However, the device symmetry of a MOSFET makes them intrinsically a bi-directional switch, which leads to power “flow-back” problems. Although many circuit topologies have been proposed in an attempt to mitigate these problems, none of them is able to fundamentally address these problems hence cannot achieve good power conversion efficiency.

To further improve the current rectifier efficiency for low voltage applications, a new rectifier circuit is proposed and implemented in this chapter. This new circuit combines the advantages of both a p-n junction diode and a MOSFET while circumventing the main drawbacks from each of them. By introducing the concept of a virtual junction, a common MOSFET can develop an energy barrier which provides a directional current flow. The height of the energy barrier can be controlled by an external circuit which minimizes the power loss in the rectifying process. Theoretical analysis indicates that this new circuit can provide significant efficiency improvement compared with both diode rectifiers as well as the MOSFET-based rectifiers in the literature. Measurements on the actual implementation closely match the theoretical

analysis and demonstrate the highest current rectifying efficiency compared with all other passive rectifier circuits from the literature.

CHAPTER 4. PASSIVE VOLTAGE BOOSTING FOR ENERGY HARVESTING APPLICATIONS

Voltage boosting is an integral part of the power conditioning circuit for many low voltage, low power energy harvesting applications. Since the output voltages of many energy harvesting devices are low in amplitude as shown in Table 1-1, there will be very little practical application for the harvested energy unless its voltage can be boosted to a level to match the supply requirement of the intended electronic loads. This is especially true for energy harvesting devices which have AC outputs due to the additional in-line rectifying voltage loss.

Depending on whether additional energy is required to step up the voltage, voltage boost circuits can be divided into two main categories: passive voltage boosting and active voltage boosting.

Passive voltage boosting circuits do not need to dissipate more energy than the component power loss in their voltage conversion process. This is usually accomplished by leveraging the cyclic and repetitive feature of the energy source, introducing positive feedback in the system to create oscillating waveform, yielding an output voltage with amplitude higher than its static value. For example: if the energy harvesting device is capacitive, a low loss inductive component can be used to form a high-Q LC resonant circuit. The resonant circuit will produce much higher output if the resonant frequency is tuned in with the AC energy source. Similarly, a capacitor can be introduced to an inductive energy harvesting circuit to boost up the

output voltage if the LC resonant frequency is in tune with the frequency of the excitation.

Passive voltage boosting techniques are attractive to energy harvesting applications for many reasons. First of all, passive voltage boosting does not dissipate static power. It can therefore be more energy-efficient in a lossless system. Secondly, passive voltage boosting circuits only use passive components for circuit implementation. It is therefore more cost effective and reliable in general. Thirdly, there are usually no minimal power requirements for the operation of the passive voltage boosting circuits, and no start-up issues either.

This chapter discusses the approach of passive voltage boosting. Using a piezoelectric energy harvesting device and transformer circuit as an example, this chapter presents the device modeling, energy harvesting application analysis and resonant circuit design methodology.

The electrical characteristics and circuit model of the PVDF energy harvesting device are first developed. Its mechanical properties and application specific mechanical models are also developed and verified with wind tunnel experiments. Based on the weakly-coupled electro-elasto-mechanical model of the energy harvesting application, an inductive load is introduced to create an LC resonant circuit with the objective of matching the LC resonant frequency with the mechanical energy harvesting peak frequency. In this work, the magnetizing inductance of a transformer is used as the inductive component for passive voltage boosting. The resonant

frequency, voltage conversion efficiency and energy conversion efficiency are tested to evaluate the passive voltage boosting and energy conversion efficiency. A DC transformer circuit is also briefly mentioned in this chapter for completeness.

4.1.PVDF FILM ELECTRICAL MODELING

PVDF is a semi-crystalline polymer material which is known to have piezoelectricity[33][34]. Coated with conductive electrodes, PVDF film has the electrical characteristic of a capacitive device. However, unlike a generic film capacitor, a PVDF piezoelectric film is usually more complicated because of the additional model components needed to account for the electro-elasto-mechanical interactions due to the piezoelectric and converse piezoelectric effects. One of the widely used models for analyzing generic piezoelectric device is a two-terminal, four-element model proposed in IEEE standard No. 177-1966[35] (Standard Definitions and Methods of Measurement for Piezoelectric Vibrators) and adopted by IEEE stand No. 176-1987[36] (IEEE Standard on Piezoelectricity). In this model as shown in Figure 52, piezoelectric material is modeled by two capacitors, one resistor and one inductor. C_0 is the shunt capacitance of the piezoelectric material and R_1, C_1 and L_1 are the motional resistance, motional capacitance and motional inductance respectively; additional motional resistance, capacitance and inductance can be added to account for the higher order resonances. C_0, R_1, C_1 and L_1 are derived from a two-

port network model which does not necessarily associate with any actual physical properties of the piezoelectric device.

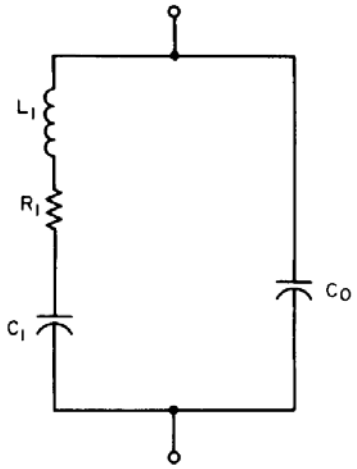

Figure 52 Equivalent Electric Model of a PVDF Piezoelectric Energy Harvesting Device

4.1.1 PVDF EQUIVALENT CIRCUIT MODEL SIMPLIFICATION

The piezoelectric model shown in Figure 52 is accurate enough to represent the impedance measurement of the piezoelectric material up to its first set of resonance frequencies, which are given by:

Parallel resonance frequency

$$f_p = \frac{1}{2\pi\sqrt{L_1 C_1 \cdot \frac{1}{1+\frac{C_1}{C_0}}}} \tag{39}$$

Series resonance frequency

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{40}$$

However, this model is cumbersome when used to model the LC resonant frequency of a passive voltage boost circuit. A simplified PVDF circuit model is much desirable if the IEEE four-element model can be further simplified.

In order to evaluate if any simplification can be made to the IEEE piezoelectric element model, three PVDF films of different thickness are used to evaluate the model parameters. Figure 53 and Figure 54 are the PVDF films' impedance (both magnitude and phase) measurement around their first resonance frequencies for three PVDF films of different thicknesses. The magnitudes of the impedance measurement vary with the film thicknesses prior series resonance frequency at which they all reach their minimum. The phase angles of the impedance measurement start to shift at different frequencies from -90° to +90° prior parallel resonance frequency and they all reach their maximum phase angle at the same parallel resonance frequency. The consistency of the series and parallel frequencies indicates the homogenous origin of the PVDF samples we used.

From the parallel and series resonance frequencies, the ratio of the motional capacitance vs. the shunt capacitance can be calculated as:

$$\frac{C_1}{C_0} = \frac{f_P^2 - f_s^2}{f_s^2} \tag{41}$$

Table 4-1 shows the measured values of $\frac{C_1}{C_0}$ for three PVDF films with different film thicknesses

Table 4-1 Ratio of C1/C0 for PVDF Film

	28μm PVDF Film	52μm PVDF Film	110μm PVDF Film
f_p (MHz)	20.083	20.083	20.083
f_s (MHz)	2.997	3.984	4.987
$\frac{C_1}{C_0}$ ratio	3.94e14	3.87e14	3.78e14

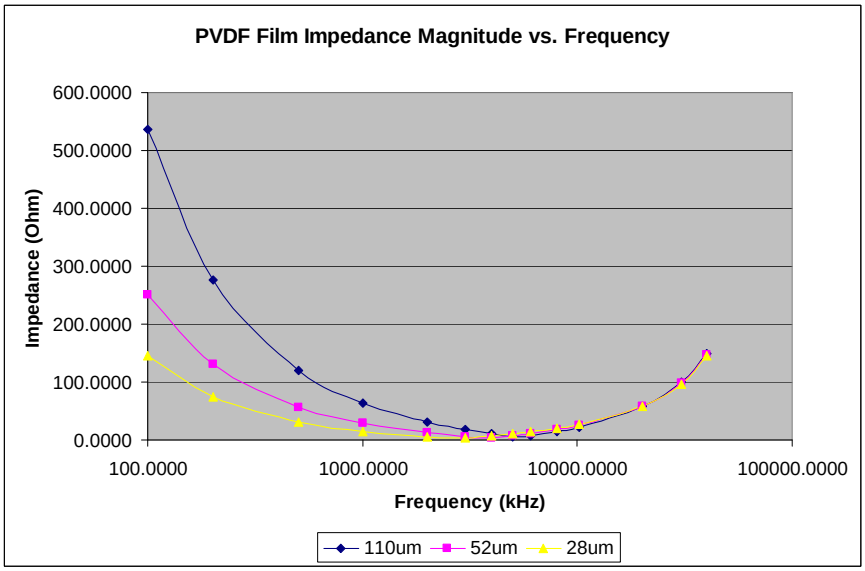

Figure 53 The Magnitude of the PVDF Film Impedance vs. Frequency Sweep

The measured C_1/C_0 ratios shown in Table 4-1 suggests that C_1 is many orders of magnitude larger than C_0, unless for the purpose of calculating high frequency

parallel resonant frequency, we can simplify the four-element PVDF piezoelectric device model by eliminating the shunt capacitor with negligible impact to the measurement results.

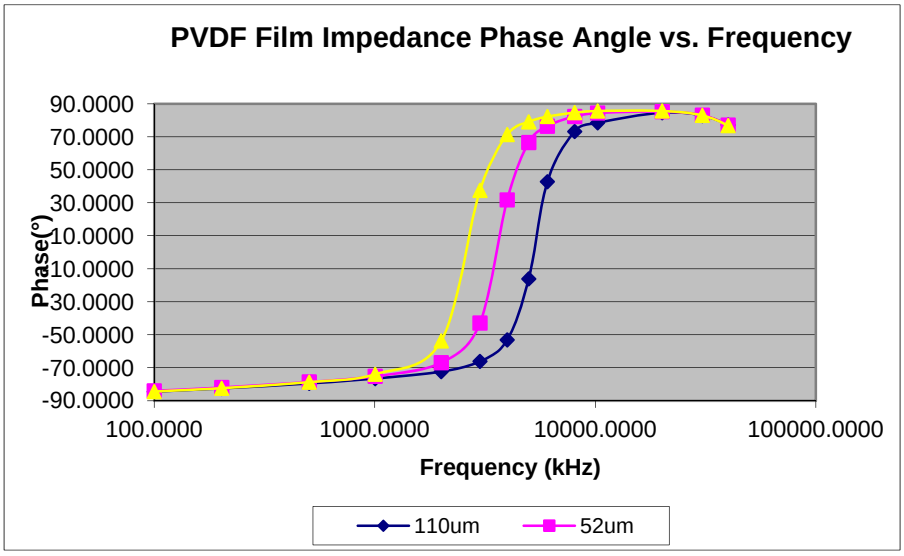

Figure 54 PVDF Film Impedance Phase Angle vs. Frequency Sweep

Table 4-2 Motional Inductances and Its Low Frequency Impedances of Different PVDF Films

	28μm PVDF Film	52μm PVDF Film	110μm PVDF Film
Inductance L (μH)	0.3022	0.221	0.228
Impedance at 100Hz (mOhm)	0.190	0.139	0.143

The motional inductance of the four-element model can be calculated based on the capacitance and the series resonant frequency. Table 4-2 shows the motional inductances and their impedances at 100Hz for three PVDF films of different thicknesses. The impact of the motional inductances can be ignored if the working frequency is significantly lower than the series resonance frequencies.

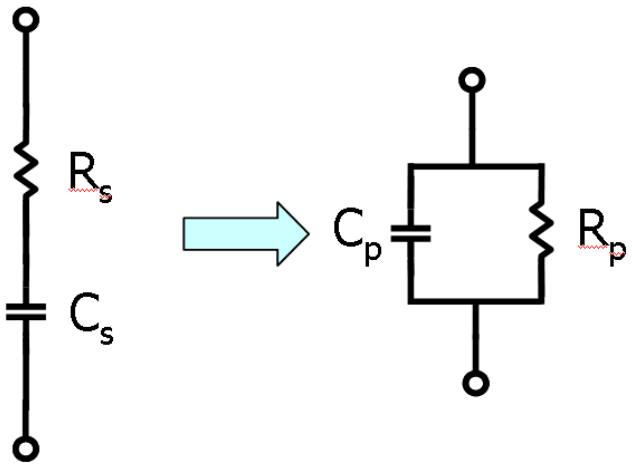

Figure 55 Simplified Circuit Model for Low Frequency PVDF Characterization

Once the two modeling elements C_0 and L are excluded, the low frequency PVDF circuit model can be simplified into the following two-element model as shown in Figure 55.

In this simplified piezoelectric device model, C_s and R_s are the equivalents of the motional capacitance C_1 and motional resistance R_1 in the four-element IEEE model.

In actual capacitance measurement, since a small capacitor has a large reactance, it is advantageous to use a parallel capacitor/resistor model to improve the measurement accuracy. A series-parallel conversion can be done to the simplified series

piezoelectric device model to convert it into a parallel piezoelectric device model. The relationship between the series and parallel model parameters are:

$$R_p = \frac{R_s^2 + X_s^2}{R_s} \tag{42}$$

$$X_p = \frac{R_s^2 + X_s^2}{X_s} \tag{43}$$

$$R_s = \frac{R_p X_p^2}{R_p^2 + X_p^2} \tag{44}$$

$$X_s = \frac{R_p^2 X_s}{R_p^2 + X_p^2} \tag{45}$$

Finally, since the motional resistance R_p is primarily the result of the material's piezoelectric effect, it is more appropriate to represent it with the dissipation factor DP. Dissipation factor (DP) is defined as:

$$DF = \frac{ESR}{|X_c|} = \tan\delta \tag{46}$$

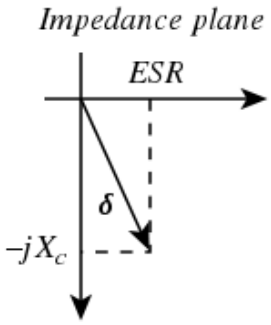

Figure 56 Loss Tangent Definition of a PVDF Film

Where ESR is the equivalent series resistance in Ω, $|X_c|$ is the magnitude of the capacitor reactance in Ω, and δ is the angle between the capacitor's impedance vector and the negative reactive axis as shown in Figure 56.

Comparing with the IEEE four-element model, this new PVDF circuit model greatly simplifies the analysis of LC resonance in a passive voltage boosting circuit.

4.2.PVDF FILM MECHANICAL MODELING

In the wind energy harvesting application, the energy conversion PVDF film undergoes an oscillating motion driven by the wind force. To analyze the PVDF film mechanical deformation and hence its piezoelectric output, it is important to characterize the mechanical property of the PVDF film itself. This section introduces the PVDF film mechanical property characterization procedure based on thin plate theory.

Since the bending of the PVDF film can be analyzed as the bending of a fixed-free cantilever, the film's Young's modulus E can be related with its maximum deflection when one end of the film is firmly clamped by a rigid edge.

The maximum deflection D of a fixed-free cantilever beam with uniform loading ρ is:

$$D = \frac{\rho L^4}{8EI} \tag{47}$$

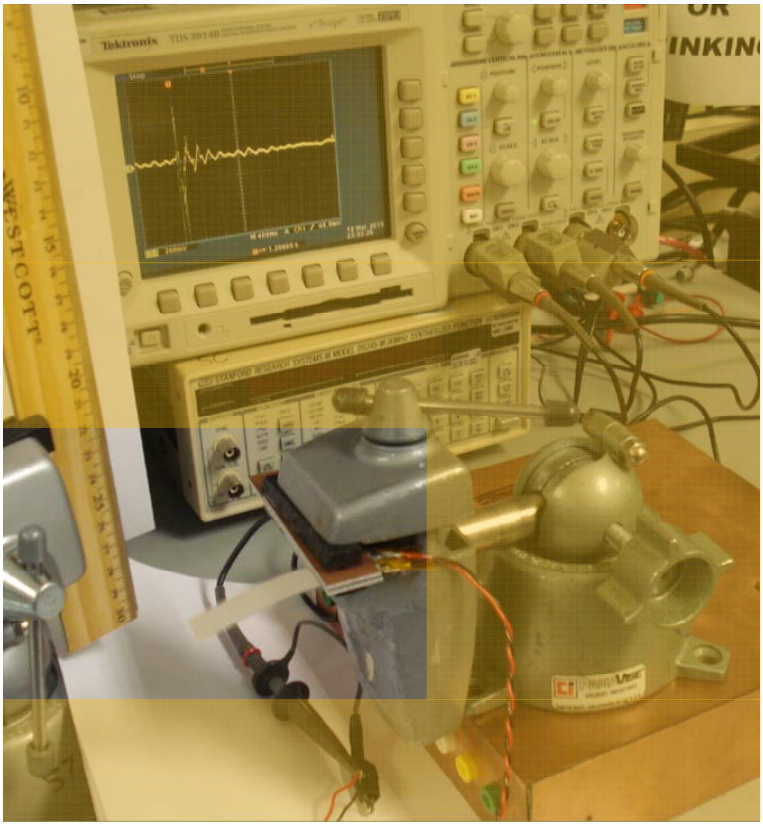

Figure 57 PVDF Film Deflection Distance Measurement in Mechanical Property Characterization

Where L is the length of the beam, and I is the moment of inertia, which is defined as:

$$I = \frac{Wt^3}{12} \tag{48}$$

The PVDF film deflection measurement setup is shown in Figure 57 and the calculated Young's modulus is listed in Table 4-3.

Table 4-3 PVDF Film Deflection Measurement and Young's Modulus Calculation

	Deflection	Young's Modulus
	(m)	(GPa)
52um new film (sq)	0.0154	15.9101
26um new film (sq)	0.0677	22.2447
110um new film (sq)	0.0033	17.2706

The natural frequency of a cantilever beam can therefore be calculated as:

$$\omega_i = (nL)_i^2 \cdot \sqrt{\frac{EI}{\rho L^3}} \tag{49}$$

Where:

E is the Young's Modulus of Elasticity

I is the moment of Inertia,

ρ is the mass of the beam

L is the length of the beam

$(nL)_i$ is the i-th solution of the transcendent equation cos(nL)cosh(nL)=-1

The natural frequency of the PVDF film can also be derived with PVDF film impulse response, in which a short impulse is applied to a piece of PVDF film while one side of the film is clamped by a rigid edge. A typical PVDF film impulse response measurement is shown in Figure 58.

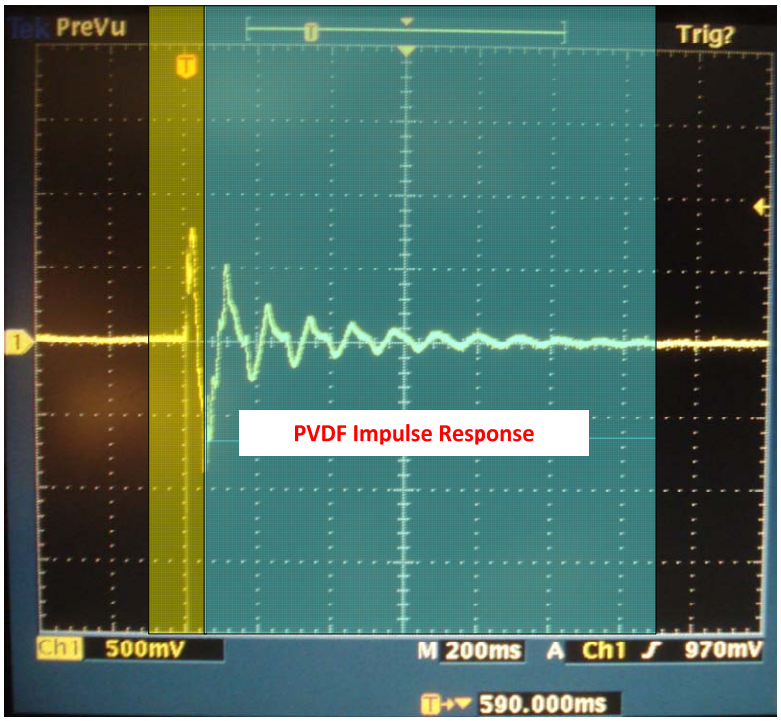

Figure 58 Impulse Test of a PVDF Film under Fixed-Free-Free-Free Condition, X-axis: time in second, Y-axis: PVDF film AC output; Time Duration Shaded in Yellow: Impulse Excitation; Time Duration Shaded in Green: PVDF Film Impulse Response

The frequency of the impulse response of a 2nd order damping system with damping ratio of ζ is[17]:

$$\omega = \omega_n \cdot \sqrt{1-\zeta^2} \tag{50}$$

Where ω is the measured frequency during the impulse test, ω_n is the system natural frequency.

For ζ=0.6, we can plot out the calculated impulse response frequencies based on the PVDF mechanical property measurement and compare them with the actual test data. Figure 59 shows the comparison of the calculated vs. actual PVDF film impulse response frequencies. The two sets of data fit very well especially for the 52μm and 110μm PVDF films.

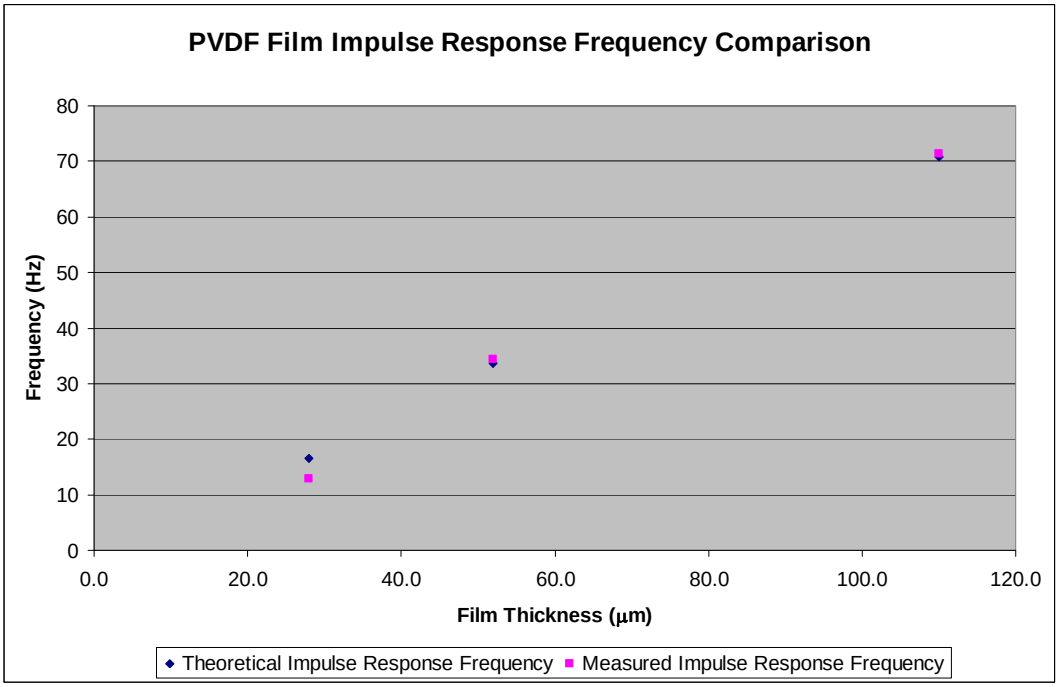

Figure 59 Comparison of Calculated and Measured PVDF Film Impulse Response Frequency

The measured Young' modulus of the PVDF film is higher than the PVDF material Young's modulus given in the literature. This is probably due to the fact that the PVDF film being measured has metallic electrodes. Based on the information provided by the vendor, the PVDF films being characterized were sputtered on with

50nm Chrome and 200nm Au to form each electrode. The two electrodes add a total of 0.5um thick of metal layer which probably accounts for the higher material Young's modulus measured.

4.3.WIND ENERGY HARVESTING EXPERIMENT WITH PVDF FILM

In the NASA/ASL wind energy harvesting setup, the energy transducer PVDF film is actuated by wind energy and undergoes a forced oscillating motion. Part of the PVDF films' kinetic energy is therefore being transformed into electrical energy through the piezoelectric effect. This section will develop the electro-elaso-mechanical model for analyzing the PVDF wind energy harvesting application. The modeling result will be used to design the LC resonant circuit in a passive voltage boosting circuit.

4.3.1 THE WIND LOAD ANALYSIS OF A PVDF FILM

The forced oscillating motion of the PVDF film in the wind field is the result of instability due to the film inertia, bending rigidity, varying tension and the wind loading. This motion resembles the flag fluttering motion in a wind field and is surprisingly complicated and still under active study[37][38][39].

Due to the lack of an analytical solution, an empirical approach is used in this study to characterize the PVDF flapping motion in the wind field. PVDF films of different thicknesses are placed in the wind tunnel and its flapping frequency is analyzed by the piezoelectric output via spectrum analysis. An empirical relationship between

PVDF flapping frequency and wind speed is then established by data interpolation. Figure 60 is a typical piezoelectric voltage output at high wind speed (12.5 MPH) and Figure 61 is the spectrum analysis of the output voltage and the PVDF film flapping frequency is therefore 43 Hz in this condition.

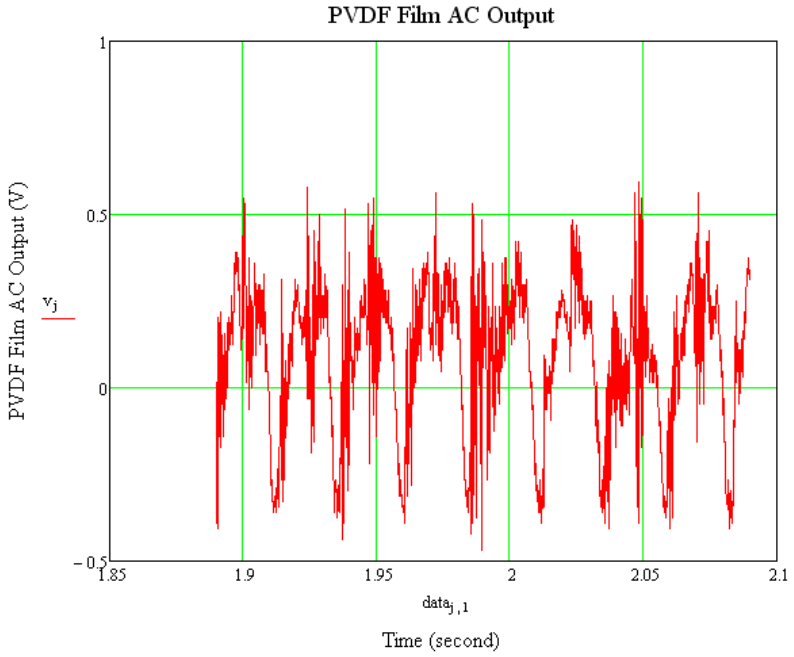

Figure 60 A Typical PVDF Piezoelectric Voltage Output at High Wind Speed, X-axis: Time in second; Y-axis: PVDF Film AC Output in Volts

Figure 62 is the logarithmic interpolation of PVDF film flapping frequency vs. wind speed. The film flapping frequency can therefore be calculated based on the interpolation equations below for a specific wind speed.

For 28μm PVDF film:

$$f(v) = 31.126 \cdot \ln(v) - 28.233 \tag{51}$$

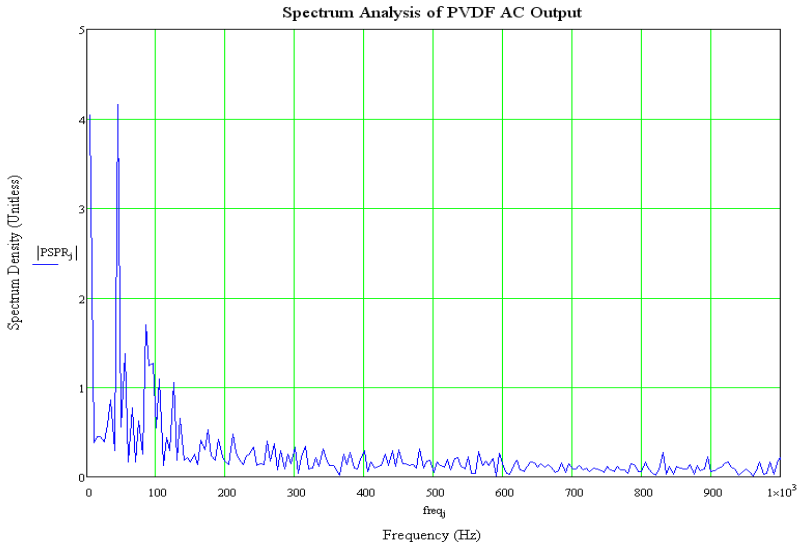

Figure 61 FFT Spectrum Analysis of the Piezoelectric Energy Harvesting Device Output

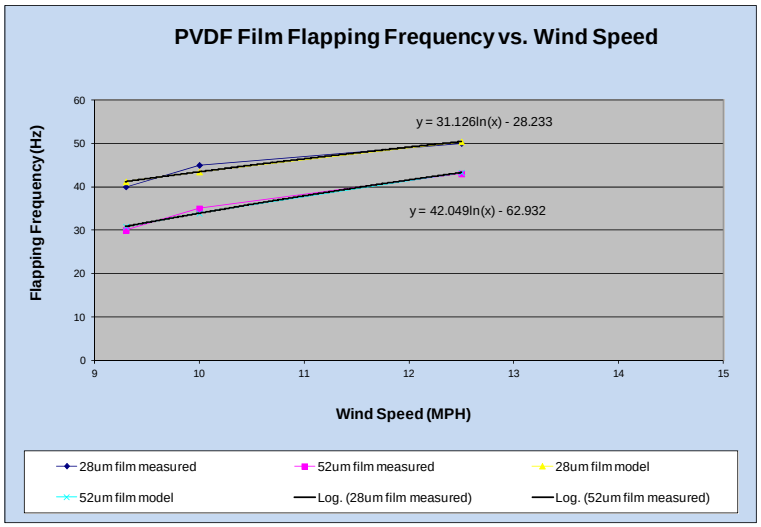

Figure 62 Logarithmic interpolation of PVDF Film Oscillating Frequency vs. Wind Speed

For 52μm PVDF film:

$$f(v) = 42.049 \cdot \ln(v) - 62.932 \tag{52}$$

4.3.2 PVDF FILM OPEN CIRCUIT PIEZOELECTRIC OUTPUT IN THE WIND FIELD

When a PVDF film is placed into a wind field, it will be subjected to wind pressure normal to its surface and a wind drag parallel to its surface. Figure 28 illustrates the force diagram of the PVDF film in a wind field. F_{wn} is the force normal to its surface and f_{wt} is the wind friction force. Notice the net wind force f_w is not balanced by the supporting force at the pivot of the PVDF film, which will cause the PVDF film to bend as shown in Figure 63.

Assume the air behind the PVDF film has negligible speed, the normal force applied to the PVDF film will be

$$f_{wn} = \frac{1}{2}\rho \cdot v^2 \cdot A \cdot \sin\alpha \tag{53}$$

For a 6cmX6cm PVDF film at wind speed of 12.5MPH at 11° angle, the calculated normal force from the wind is approximately 1.9N.

For the same film in a wind tunnel with wind speed of 12.5MPH, the Reynolds number is:

$$\mathrm{Re} = \frac{vL}{\nu} = 21400 \tag{54}$$

Where L is the characteristic length, n is the kinematic viscosity and v is the speed of the wind.

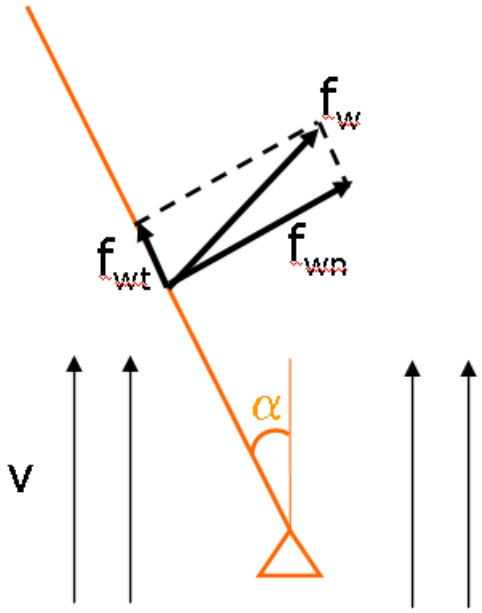

Figure 63 Free Body Diagram Illustrates the Forces Applied by Wind to a PVDF Film

At this Reynolds number, the wind friction force f_{wt} needs to be calculated with the quadratic law, which is:

$$f_{wt} = -\frac{1}{2}\rho A C_d v^2 \tag{55}$$

Where C_d is the drag coefficient. Assuming C_d=0.5, the wind friction force can be calculated to be approximately 0.031N which is 1% of the wind force normal to the PVDF film surface.

Table 4-4 PVDF Film Stress Modes and Piezoelectric Outputs at Wind Speed of 12.5MPH

	Force	Piezoelectric Constant	Voltage output
	(N)	(V/m*N)	(V)
Longitudinal Mode	0.03	0.21	0.01
Thickness Mode	1.90	0.28	0.54

Table 4-4 is a comparison of the PVDF film longitudinal mode and thickness mode piezoelectric outputs at wind speed of 12.5MPH. Since the piezoelectric output of the thickness mode is much higher than the longitudinal mode, the PVDF film in the NASA/ASL wind energy harvesting setup is primarily working in thickness or g_{33} mode and its open circuit output voltage will be given by:

$$V_0 = g_{33} \cdot f_{wn} = g_{33} \cdot \frac{1}{2} \rho \cdot v^2 \cdot A \cdot \sin \alpha \tag{56}$$

This is the PVDF film open circuit voltage output at wind speed of v, cross section area of A and under the fix-free-free-free boundary condition. It can be seen that the PVDF film open circuit voltage output increases with the square of the wind speed and in proportional with the film area.

One typical AC and DC output of the wind energy harvesting system in NASA/ASL is shown in Figure 64. This is a wind tunnel test result done at maximum wind speed with 52μm thick PVDF film. The test was done with a 4.7μF output capacitor and a

1.2MΩ output load resistor. The cyan curve shows the AC output voltage measured at the PVDF film output, and the blue curve shows the DC output at the rectifier bridge. Figure 64 shows at time 0, both the AC and DC outputs are zero apart from the noise, and the baselines of both channels are set at 0 volts.

At approximately 300ms, the wind tunnel is turned on and PVDF starts generating AC output voltage. The rectified DC current starts charging up the output filter capacitor and generating a 0.2V DC output voltage across a 1.2MΩ load resistor. At this time point the DC output power is:

$$P_{DC} = \frac{V^2}{R} = 0.033\mu W \tag{57}$$

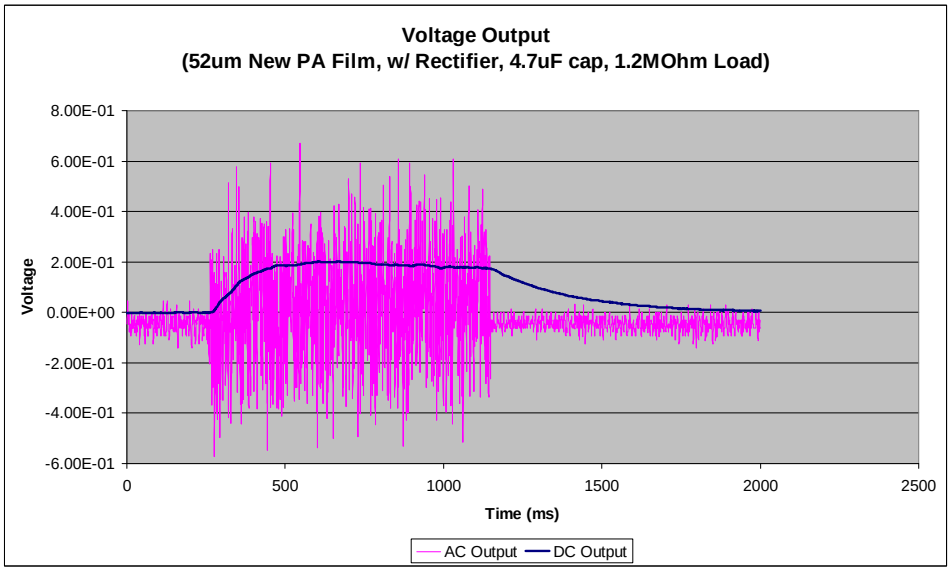

Figure 64 A typical NASA/ASL Wind Energy Harvesting System Output

The AC voltage of the PVDF film output looks choppy because of the oscilloscope timescale is not fine enough to resolve the cycle-per-cycle voltage waveforms.

However, the peak-to-peak AC voltage can be easily read out from the graph as approximately 1.2V. The harvested wind energy is therefore:

$$P_{AC} = \frac{V_{rms}^2}{R} = \frac{1}{2} \cdot \frac{V_{PK}^2}{R} = 0.15\mu W \tag{58}$$

At approximately 1.2s, the wind tunnel is turned off and the PVDF film stops generating AC output voltage. The electrical energy accumulated at the output filter capacitor is gradually dissipated through the load resistor and both channels of the oscilloscope settled back t0 0 volts.

4.3.3 MODEL ANALYSIS OF A WIND ENERGY HARVESTING SYSTEM

To better understand and analyze the NASA/ASL PVDF wind energy harvesting system, a 2nd-order electro-elasto-mechanical model is proposed to characterize the dynamic motion and AC voltage output of the PVDF film in wind field as shown in Figure 65.

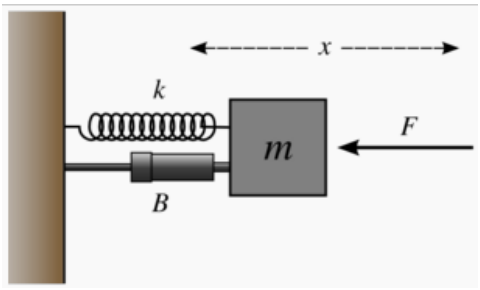

Figure 65 Model of a 2nd Order System: Mass-Spring-Dumping System

$$m\ddot{x} + c\dot{x} + kx + [d^t]\{E\} = F(v,t) \tag{59}$$

Where:

$m\ddot{x}$ is the inertial of the PVDF film

$c\dot{\ddot{x}}$ is the damping of the PVDF film

kx is the spring force of the PVDF film or Hooke's law

$F(v,t)$ is the force applied by the wind at wind speed v

$[d^t]$ ii the matrix for the converse piezoelectric

$E=V_{AC}/d$ is the electric field intensity

This is the full-coupled model for a piezoelectric 2nd order system. The complete analysis of this model will be very difficult because of the piezoelectric term.

In the cases when the electrical field of the piezoelectric device is weak, the piezoelectricity term in the full-coupled model is relatively insignificant. For example, for a 52um thick PVDF film with 0.5V peak voltage, the piezoelectric strain is:

$$dt = t \cdot d_{33} \cdot E = 15 \cdot 10^{-12}\, m = 0.000029\%t \tag{60}$$

It is usually safe to ignore the piezoelectricity term without affecting the effectiveness of the model. Hence a piezoelectric system can be reduced as:

$$m\ddot{x} + c\dot{x} + kx = F(v,t) \tag{61}$$

This is the *weakly-coupled 2nd order system with piezoelectricity*. It resembles a generic 2nd order system at any fixed wind speed v. The following discussion will use

this weakly-coupled 2nd order system to analyze the PVDF film characteristics in the wind field[40].

The characteristic equation of the homogenous 2nd order system is:

$$m\lambda^2 + c\lambda + k = 0 \tag{62}$$

Define natural frequency of the system $\omega_n = \sqrt{\frac{k}{m}}$, damping ratio of the system $\zeta = \frac{c}{2\sqrt{km}}$

The characteristic equation can be re-written as:

$$\frac{1}{\omega_n^2}\lambda^2 + \frac{2\zeta}{\omega_n}\lambda + 1 = 0 \tag{63}$$

The solution of this quadratic equation is:

$$\lambda_1 = -\zeta\omega_n + \omega_n\sqrt{\zeta^2 - 1} \tag{64}$$

$$\lambda_2 = -\zeta\omega_n - \omega_n\sqrt{\zeta^2 - 1} \tag{65}$$

Depending on the value of the damping ratio ζ, there are three different behaviors for the system:

(1) $0<\zeta<1$ (under damped system)

This is an under damped system, which means the system will tend be oscillatory in response to any input excitation, for example, its unit step response will be an exponentially decayed sinusoidal oscillation. The time-domain response for this system in response to a unit step input is:

$$y_h(t) = Ce^{-\zeta\omega_n t}\sin(\omega_n\sqrt{1-\zeta^2}\,t + \Theta) \tag{66}$$

The impulse responses of both the 52μm and 110μm film are oscillatory which suggest that both of them are under damped systems. From Figure 58 and Figure 59, we can determine the system damping ratio ζ for the fixed-free-free-free setup of the 52μm and 110μm thickness PVDF film is ζ=0.6. This is a slightly under-damped system with a dynamic magnification factor or maximum overshoot Mp:

$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} = 1.042 \tag{67}$$

The unit step response of this system is shown in Figure 66.

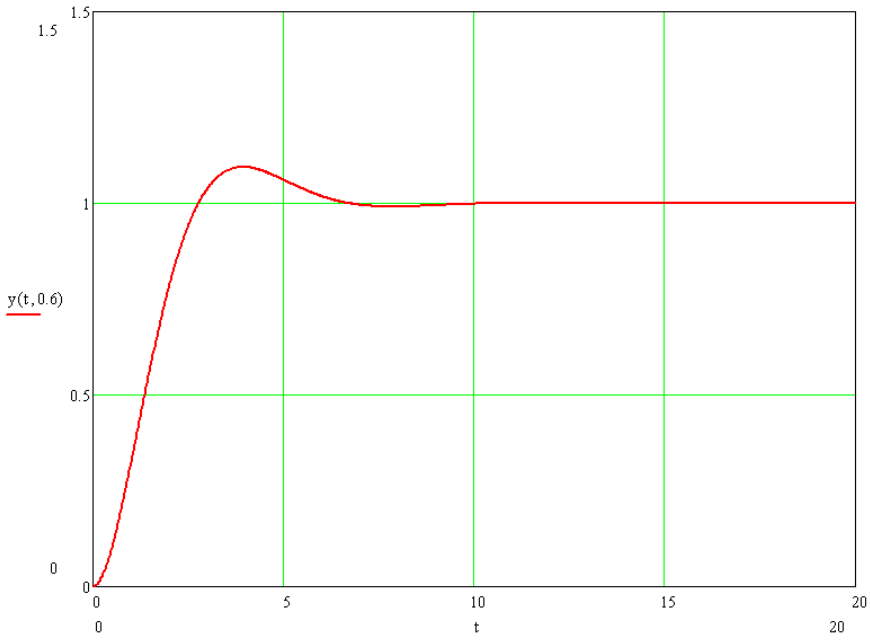

Figure 66 Unit Step Response of the 52μm PVDF Energy Harvesting Device under Fixed-Free-Free-Free Condition

Figure 66 suggested the PVDF film dynamic magnification factor is very low therefore the amplitude magnification of the PVDF film oscillation is very low at the conditions when wind speed induced oscillation frequency matched the PVDF film natural oscillating frequency. This will be discussed further in section §5.2.

(2) ζ=1 (critically damped system)

This is a critically damped system, which means the output will monotonically approach its steady state without overshoot. The time-domain response is:

$$y_h(t) = C_1 e^{\lambda_1 t} + C_2 t e^{\lambda_2 t} \tag{68}$$

(3) ζ>1 (over damped system)

This is an over damped system, which means the output will also monotonically approach its steady state but takes longer time than the critical damping system. The time-domain response is:

$$y_h(t) = C_1 e^{\lambda_1 t} + C_2 e^{\lambda_2 t} \tag{69}$$

Both case (2) and case (3) means the PVDF film will monotonically return to its neutral position once the wind excitation is removed. Since all lab experiment data shows the actual PVDF films oscillate prior to returning to their neutral position, the current NASA/ASL wind energy harvesting system does not fit into any of these two cases.

When the NASA/ASL wind harvesting system is actuated by the wind force F(v,t), the system characteristic equation is a non-homogeneous 2nd order ODE:

$$m\ddot{x} + c\dot{x} + kx = F(v,t) \tag{70}$$

Based on the analysis in chapter 3, the wind force can be approached by a sinusoidal excitation with a linear interpolated oscillation frequency, which can be expressed as:

$$F(v,t) = q \cdot \sin(\omega_w(v) \cdot t) \tag{71}$$

In which $\omega_w(v)$ is the linear interpolation of the oscillation frequency vs. wind speed. For example, for the 52μm PVDF film, $\omega_w(v)$ is:

$$\omega_w(v) = 42.049 \ln(v) - 62.932 \tag{72}$$

In which v is the wind speed.

The maximum wind force q is:

$$q = \frac{1}{2} \cdot \rho \cdot v^2 \tag{73}$$

At given wind speed v, the wind force function is a sinusoidal source:

$$F(v,t) = \frac{1}{2} \cdot \rho \cdot v^2 \cdot \sin(\omega_w(v) \cdot t) \tag{74}$$

The solution of the non-homogenous 2nd order system is:

$$y(t) = y_h(t) + \frac{Kq \sin[w_w(v) \cdot t + \phi(\omega)]}{\sqrt{[1 - (\frac{\omega}{\omega_n})^2]^2 + (2\zeta \cdot \frac{\omega}{\omega_n})^2}} \tag{75}$$

Where the first item is the transient response which will decay to 0 after a few time constants, and the steady state response is:

$$y(t \to \infty) = M(\omega) Kq \sin[w_w(v) \cdot t + \phi(\omega)] \tag{76}$$

Where

$$M(\omega) = \frac{1}{\sqrt{[1-(\frac{\omega}{\omega_n})^2]^2 + (2\zeta \cdot \frac{\omega}{\omega_n})^2}} \tag{77}$$

$$\phi(\omega) = \arctan[-\frac{2\zeta \cdot \frac{\omega}{\omega_n}}{1-(\frac{\omega}{\omega_n})^2}] \tag{78}$$

Figure 67 is the plot of M(ω) vs. the ratio of excitation frequency ω over system natural frequency ω_n. It can be seen that the maximum output magnitude slightly peaks at $\omega=0.6\omega_n$, however, the magnitude gain is very low, which means matching the stimulus frequency will not significantly increase the system output amplitude. In other words, matching the wind-induced oscillation frequency with the PVDF film's mechanical resonance frequency only marginally enhanced the PVDF film's oscillating amplitude and therefore its power output. This limitation is imposed by the existing PVDF film mechanical property, primarily by the PVDF film damping ratio ζ. In the future, this could be one of the film design targets that should be further optimized to improve PVDF wind harvesting efficiency as shown in Figure 39.

Figure 68 shows the effect of reducing PVDF film damping factor ζ on its maximum oscillating magnitude M(ω) under frequency matching conditions. It can be seen that when ζ reduces from 0.6 to 0.3, 0.2 and 0.1, the maximum oscillation amplitudes increase significantly. For example, when ζ=0.1, the maximum oscillation amplitude

is almost 5 times its low frequency oscillation amplitude under frequency matching condition.

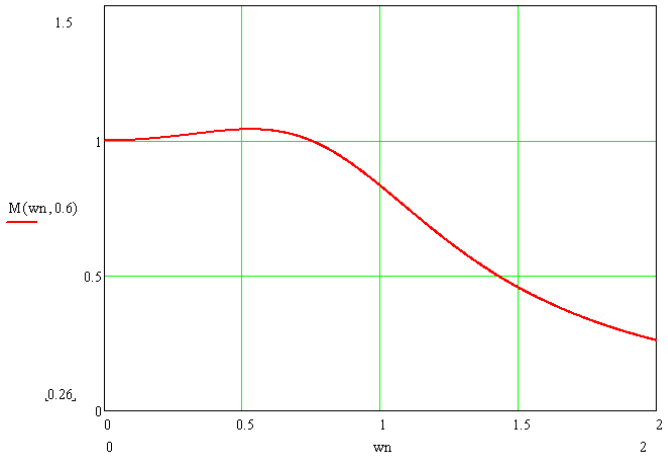

Figure 67 Amplitude Peaking of the 2nd Order System with Stimulus vs. Natural Frequency Ratio

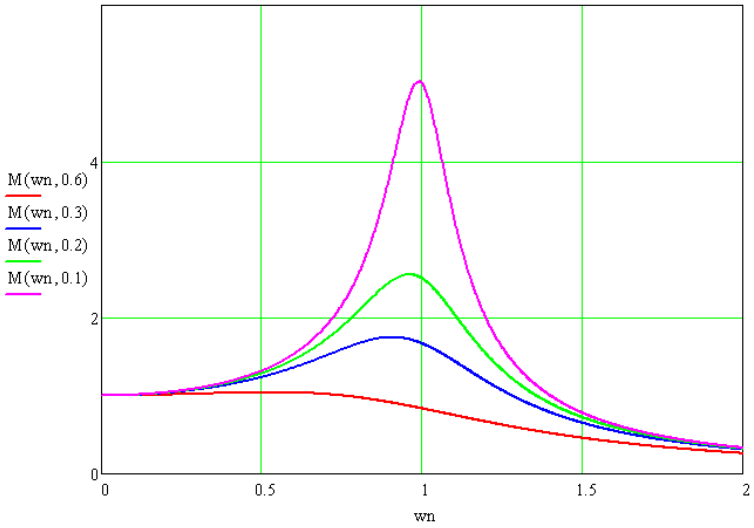

Figure 68 Amplitude Peaking of the 2nd Order System with Different Damping Factors

4.3.4 WIND TUNNEL TEST OF A PIEZOELECTRIC WIND ENERGY HARVESTING SYSTEM

The weakly coupled 2nd order piezoelectric model is used to understand and analyze the NASA/ASL wind energy harvesting setup. A model had been used to calculate the amplitude and the frequency of the PVDF AC voltage output and compared with the actual measurement data collected from wind tunnel test. Figure 69 is a superposition of the model output vs. actual wind tunnel measurement for a 52μm PVDF film at high wind speed. The blue curve is derived from the weakly-coupled 2nd order piezoelectric model. The red curve plots the wind tunnel test data. Only the phase of the blue curve has been adjusted to match the two curves. The strong correlation between the red and blue curves suggests the model fits the bench test data very well.

Figure 70 and Figure 71 are similar plots of the superposition of modeled data vs. actual measurements for the same PVDF film but medium and low wind speed. The weakly coupled 2nd order piezoelectric model predicted the PVDF AC voltage amplitude and frequency with good accuracy.

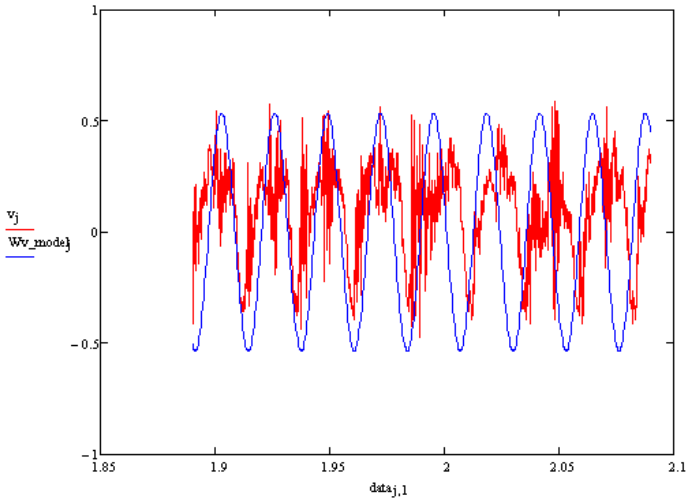

Figure 69 PVDF AC Output Predicted by Model (Blue) and Measured from Wind Tunnel (Red)

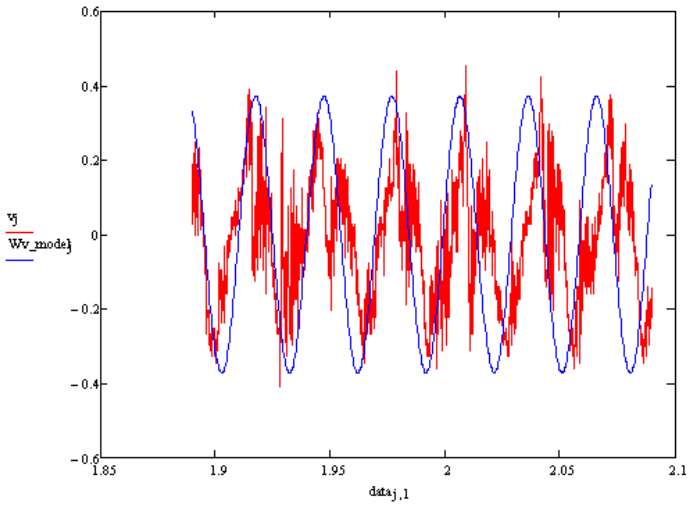

Figure 70 PVDF AC Output Predicted by Model (Blue) and Measured from Wind Tunnel (Red)

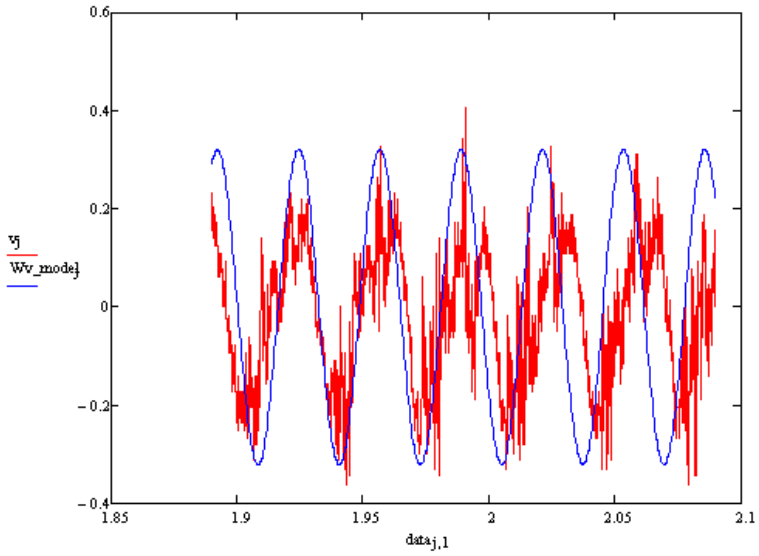

Figure 71 PVDF AC Output Predicted by Model (Blue) and Measured from Wind Tunnel (Red)

Table 4-5 shows the comparison of the weakly-coupled 2nd order piezoelectric modeling result vs. actual wind tunnel data. The high correlation between these two sets of data indicates the proposed 2nd order system is a good model for the actual PVDF wind harvesting system.

Table 4-5 Comparison of 2nd Order Piezoelectric Model vs. Actual Wind Tunnel Data

Wind Speed	AC Output Voltage		Output Frequency	
	Model	Measurement	Model	Measurement
(MPH)	(V)	(V)	(Hz)	(Hz)
12.5	0.535	0.5	43.28	45
10	0.371	0.35	33.7	35
9.3	0.321	0.3	31.02	30

4.4. TRANSFORMER CIRCUIT

The transformer is one of the simplest circuit components in modern electronics. A transformer has two or more magnetically coupled windings which share a common magnetic field. The AC current in the primary winding of the transformer introduces a time-varying magnetic flux in the core of the transformer. It impinges on the secondary winding and induces a varying electromotive force (EMF) or voltage in the secondary winding, and enables the transformer to convert an AC signal from its input to its output according to the turns ratio of the two windings.

Apart from obvious advantages such as circuit simplicity and no active power dissipation, the value of the transformer voltage boosting approach is that being an inductive component, the transformer could potentially form an LC resonate tank with many capacitive energy harvesting devices and enhance their energy harvesting efficiency.

Based on the difference in their AC signal sources, there are two types of transformer circuits which can be used for energy harvesting applications.

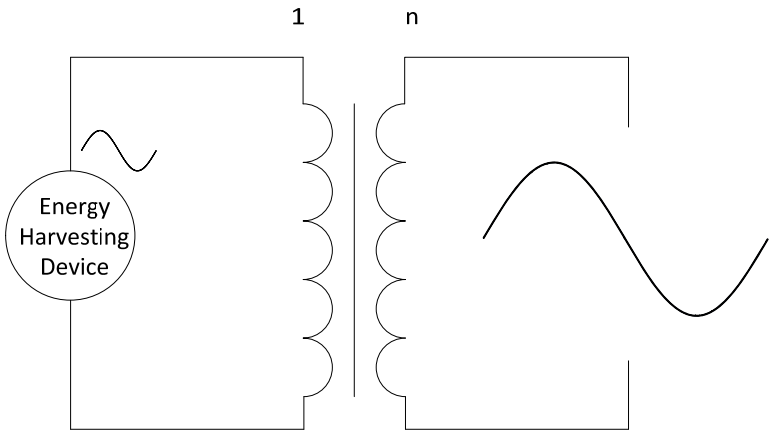

Figure 72 Direct Transformer Voltage Conversion Circuit

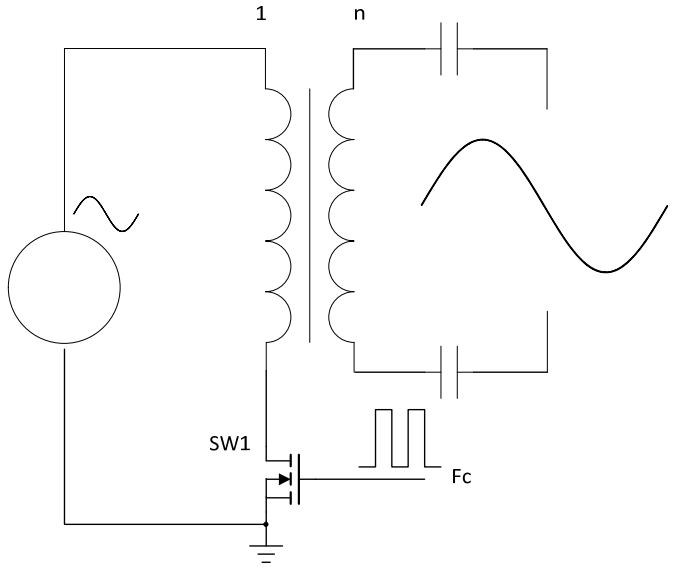

Figure 73 DC Transformer Voltage Conversion Circuit

Figure 72 shows a direct transformer voltage conversion circuit which uses the intrinsic AC output of the energy harvesting device. Figure 73 shows the indirect or DC transformer voltage conversion circuit which uses an external DC switch SW1 to modulate the input voltage to a higher frequency near the DC frequency. Both

transformer circuits can be used to step up the low magnitude signal output from the energy harvesting device.

4.4.1 DIRECT TRANSFORMER VOLTAGE CONVERSION CIRCUIT

A direct transformer voltage conversion circuit transforms the AC output of the energy harvesting device from the primary side to the secondary side without additional signal modulation. The transformer works at the AC signal frequency of the energy harvesting devices themselves.

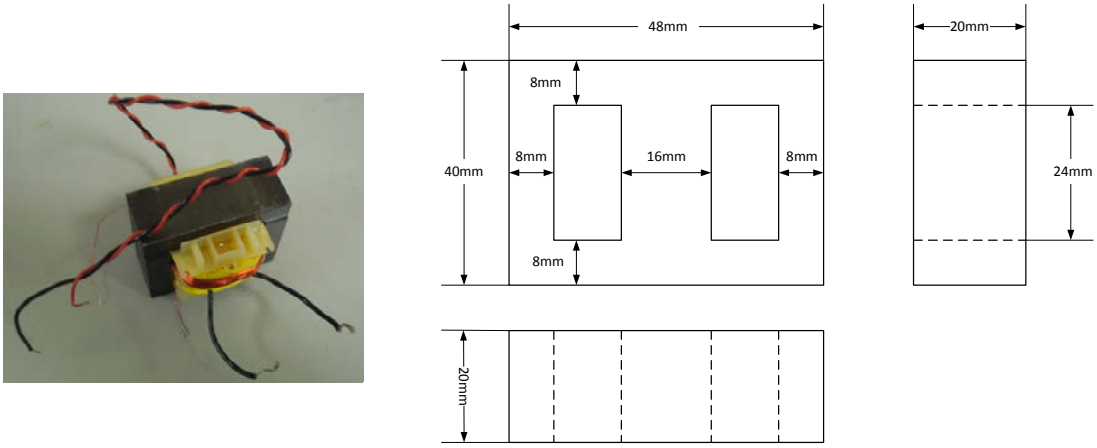

Figure 74 An Iron-core Low Frequency Transformer for Direct Voltage Conversion of Energy Harvesting Applications

Since the majority of the energy harvesting devices generate low frequency signals, i.e., the mechanical vibration signal of a piezoelectric sensor can be as low as tens of Hertz, this type of transformer circuit requires the magnetic components to have high

magnetic permeability at the corresponding low frequencies to maintain its high magnetic coupling efficiency. The most common magnetic materials for this type of transformer circuit are therefore iron-based such as soft iron, silicon steel and silicon alloying iron. Figure 74 shows one example of this type of direct voltage conversion transformers.

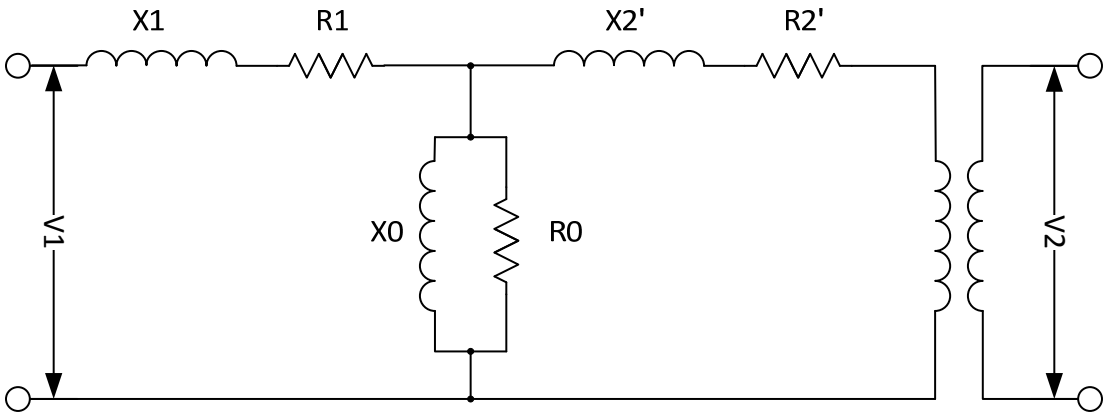

Figure 75 Circuit Model of a Transformer Circuit

Figure 75 shows the most commonly used circuit model of a transformer. X1 and R1 are the leakage reactance and winding resistance of the primary coil, X2’ and R2’ are the leakage reactance and winding resistance of the secondary coil referred to the primary side. X0 and R0 are the components representing the magnetizing reactance and core loss.

4.4.2 VOLTAGE CONVERSION RATIO WITH HIGH OUTPUT IMPEDANCES SOURCE

Using the transformer circuit model shown in Figure 75, the direct voltage conversion transformer circuit can be shown in Figure 76. The orange and blue circuit blocks model the transformer in which the orange block shows the “imperfection” part of the transformer, and the blue block shows an “ideal” transformer. Cp and Rp represent the energy harvesting device.

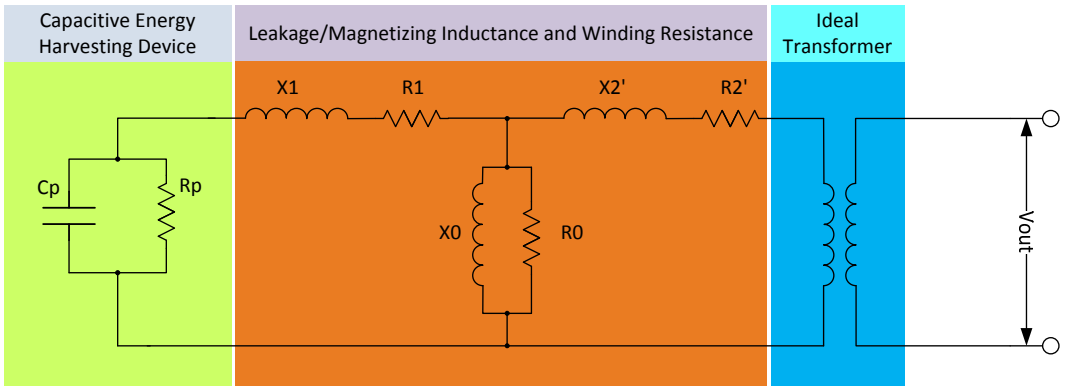

Figure 76 Circuit Model of Passive Voltage Conversion Transformer Circuit

From Figure 76, the current in the primary winding can be calculated as:

$$i_s = \frac{v_s}{Z_{in}} = \frac{v_s}{\sqrt{(R_s + R_1 + R_2^{'} + R_L')^2 + (X_1 + X_2)^2}} \tag{79}$$

Where R_L’ is the load resistance referenced to the primary side of the transformer.

$$R_L' = \frac{n_1^2}{n_2^2} R_L \tag{80}$$

Ignoring core loss and magnetizing inductance, the output voltage on the load resistor is therefore:

$$\frac{v_L}{v_s} = \frac{1}{\sqrt{(\frac{R_s}{R_L'} + \frac{R_1}{R_L'} + \frac{R_2'}{R_L'} + 1)^2 + (\frac{X_1}{R_L'} + \frac{X_2}{R_L'})^2}} \cdot \frac{n_1}{n_2} \tag{81}$$

Comparing with ideal transformer equation, the actual output voltage is reduced by a factor of $\frac{1}{\sqrt{(\frac{R_s}{R_L'} + \frac{R_1}{R_L'} + \frac{R_2'}{R_L'} + 1)^2 + (\frac{X_1}{R_L'} + \frac{X_2}{R_L'})^2}}$.

If the load resistance is large enough, $R_L' >> R_1$, $R_L' >> R_2'$, $R_L' >> X_1$ and $R_L' >> X_2$, this equation can be simplified as:

$$\frac{v_L}{v_s} \approx \frac{1}{\frac{R_s}{R_L'} + 1} \cdot \frac{n_1}{n_2} \tag{82}$$

Equation (82) shows how the source impedance of the energy harvesting device and load impedance of the transformer limit the voltage conversion ratio of a transformer circuit.

For maximum power transfer from the energy harvesting device to the load, the load impedance should be equal to the source impedance. In this case, $Rs = R_L'$, and the voltage conversion ratio is reduced by a factor of two.

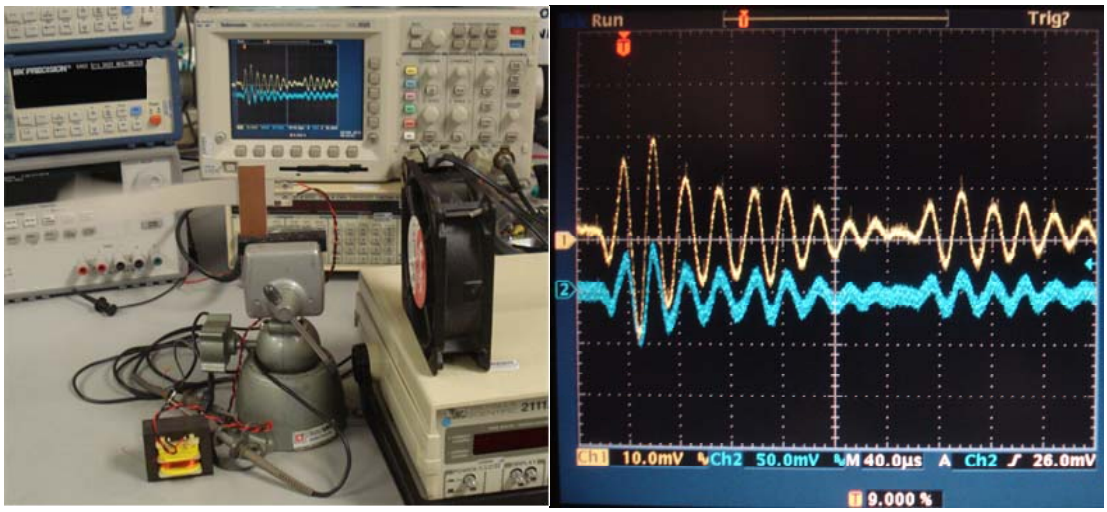

Figure 77 Bench Test with Direct Transformer Voltage Conversion

Figure 84 shows the bench measurement setup and result for direct transformer voltage conversion. The design parameters of the transformer are listed in Table 4-6. The left side of the photo shows the polymer PVDF film is driven by the wind created from a fan. The right side of the photo shows the harvested energy from the PVDF film. The yellow trace on the top indicates the output of the PVDF film, and the blue trace on the bottom indicates the output waveform boosted by a 1:8 direct transformer. Although the primary: secondary turns ratio is 1:8, the actual voltage boosting result can be read from the oscilloscope as 2.5x due to the large output impedance of the PVDF film which is the result of the voltage conversion degradation.

4.4.3 POWER TRANSFOER EFFICIENCY OF PRACTICAL TRANSFORMER CIRCUIT

Practical transformers suffer losses from different sources. For example, the resistances of both the primary and secondary windings introduce copper loss; the hysteresis in the B-H curve of the magnetic core introduces iron loss. High frequency AC signals introduce Eddy currents and skin and proximity effects. While some of these transformer losses can be modeled, the exact transformer efficiency still needs to be measured for practical purposes.

Table 4-6 Design Parameters for a Low Frequency Iron Core Transformer for Energy Harvesting Applications

Core Cross Section Area	A	(m^2)	0.00032
Magnetic Length per turn	Le	(m)	0.096
Primary Coil Wire Thickness		AWG	24
Turns number of Primary Coil	n1	(T)	122
Primary Coil DC Resistance	R1	(Ohm)	12.688
Secondary Coil Wire Thickness		AWG	32
Turns number of Secondary Coil	n2	(T)	976
Secondary Coil DC Resistance	R2	(Ohm)	83.2
AC Frequency	F	(Hz)	100

Table 4-6 shows the key parameters of a low frequency iron core transformer with 1:8 turns ratio for energy harvesting devices. The dimension of this transformer is shown in Figure 74.

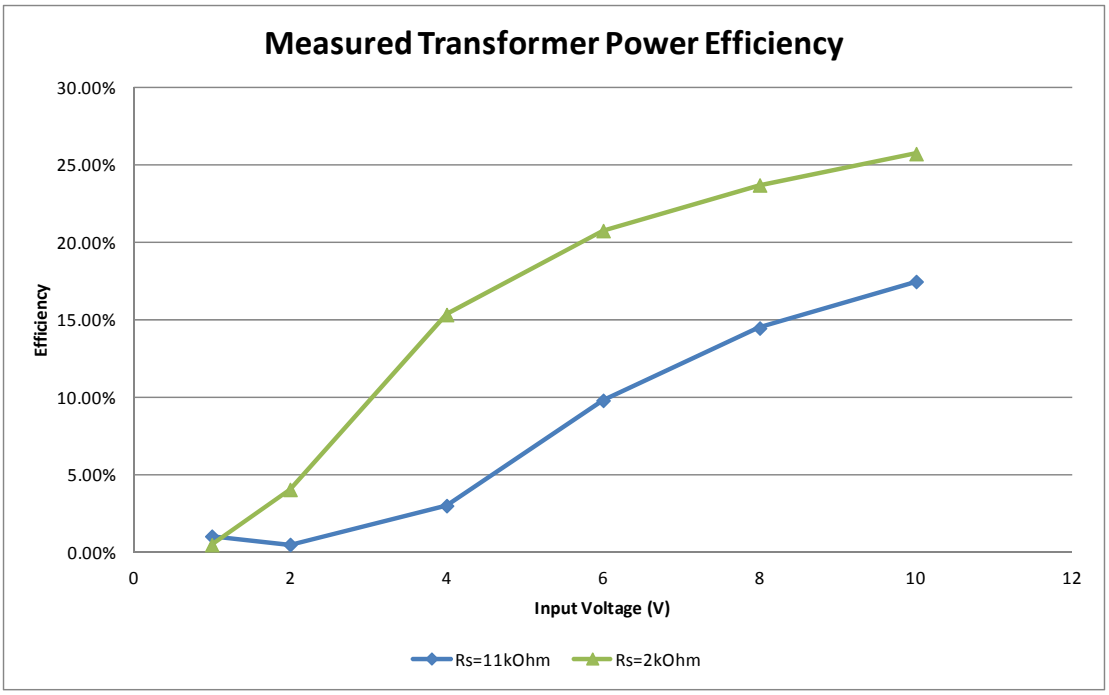

Figure 78 Measured Transformer Power Transfer Efficiency

Figure 78 shows the bench measured power transfer efficiency of the above-mentioned transformer at 100Hz. It can be seen that the power transfer efficiency is significantly impaired by the magnetizing inductance of the actual transformer. As the source impedance increases, the relative percentage of the magnetizing current also increases which decreases the power conversion efficiency of a directly transformer circuit.

4.4.4 POWER CONVERSION EFFICIENCY ENHANCEMENT WITH LC RESONANCE

One important motivation for using a transformer as a voltage boosting element is its potential to be used in an LC resonant circuit with capacitive energy harvesting devices such as piezoelectric transducers to enhance their energy harvesting output voltage. Using the PVDF model developed in section 4.1, two PVDF films were used to bench test the output voltage enhancement using an LC resonant circuit. Two PVDF films are modeled using methods developed in section 4.1.1, and the transformer is modeled using the simplified model in section 4.4.2. Their model parameters are listed in Table 4-7.

Table 4-7 Piezoelectric Energy Harvesting Device and Transformer Model Parameters

Model Element		Unit	Value
Piezoelectric Capacitance	Cp	nF	5.37
Dissipative Resistance	Rp	Ohm	81200
Primary Winding Leakage Inductance	L1	H	2.866
Reflected 1nd Winding Leakage Inductance	L2'	H	0.09628
Magnetizng Inductance	Lm	H	0.083
Turn's ratio	n		8

Figure 79 shows the model analysis based on Table 4-7 and the normalized output amplitude measurement using a function generator and two RMS voltage meters. The modeled LC resonant frequency is around 10000Hz and the measured LC resonant peak is around 9743Hz. There is an additional high frequency resonant peak which is captured in the bench measurement but not shown in the model due to the self-resonance of the PVDF film.

Figure 80 shows the impedance measurement of the PVDF energy harvesting device with a voltage boosting transformer using HP4194A impedance/gain-phase analyzer. The first LC resonant frequency is at 10439Hz which is a good match to the model analysis. The second resonant peak is the PVDF film's self resonant frequency.

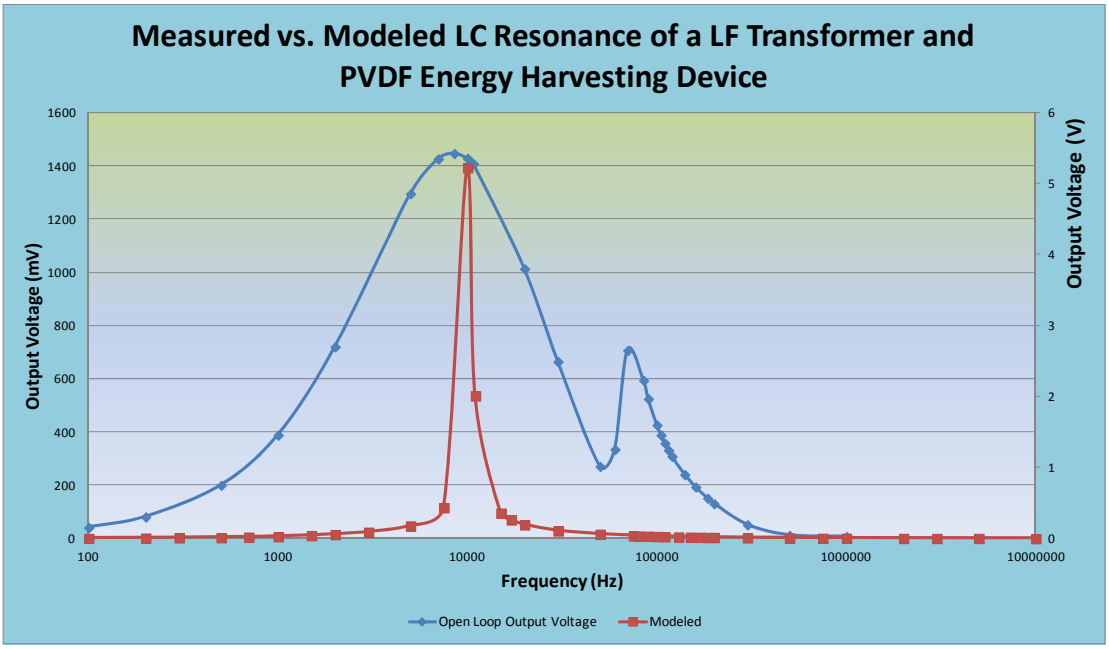

Figure 79 Modeled PVDF and Transformer Resonant Frequency

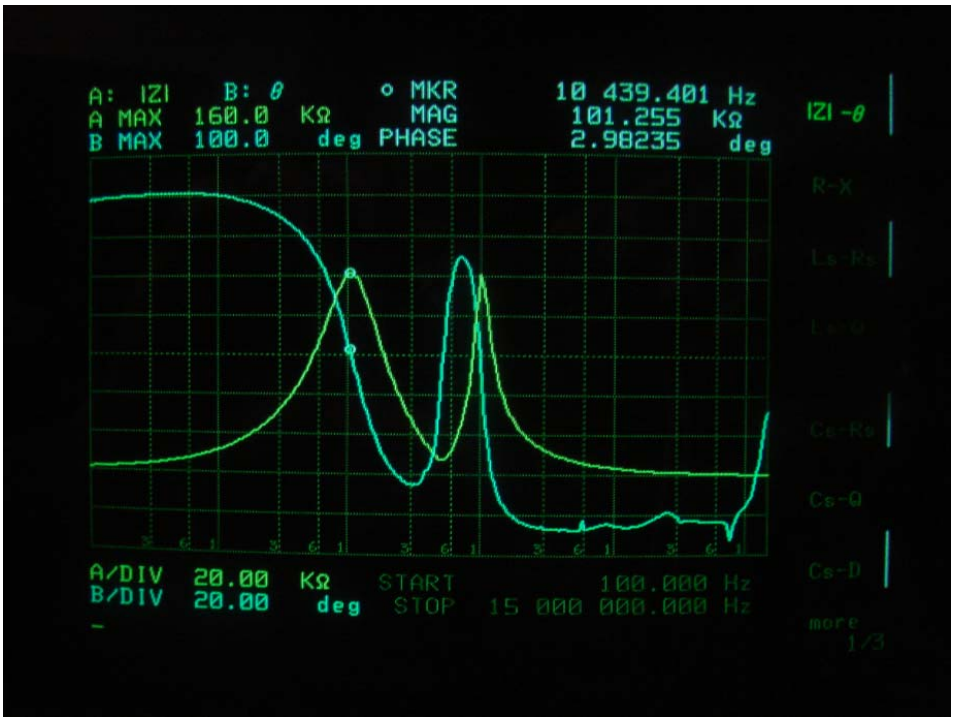

Figure 80 Impedance Measurement on PVDF and Transformer Circuits

4.5.DC TRANSFORMER VOLTAGE CONVERSION CIRCUIT

Although the direct voltage conversion transformer circuit has many advantages such as simple circuit implementation and no static power dissipation, the typical low operating frequency of the energy harvesting devices mandate this kind of transformer to use iron-based core materials which tends to make the transformer both heavy and bulky. A DC transformer circuit as shown in Figure 73 can be used to reduce the size and the weight of the transformer in the energy harvesting applications.

Figure 81 shows the typical voltage waveforms of the DC transformer circuit. A DC signal is used to drive a switch which periodically shorts the input to modulate the DC or low frequency input signal to a higher frequency around the DC frequency. Typically this DC frequency is high enough therefore the transformer can use a light weight high frequency core material. Figure 82 shows one example of the energy harvesting circuit using a DC transformer[41] and Figure 83 shows the input and output waveforms of the DC transformer operation[41].

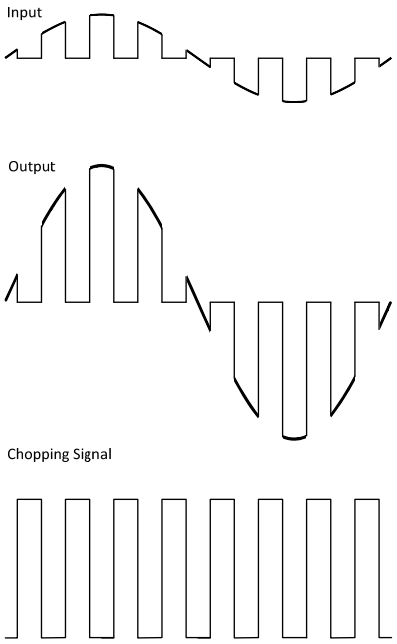

Figure 81 Voltage Waveforms of the DC Transformer Circuit

Although DC transformers can effectively reduce the size and the weight of the transformer components themselves, one of the significant issues with this type of circuit is that it needs an auxiliary power supply to start up and function properly. This is an important limitation for some of the energy harvesting applications.

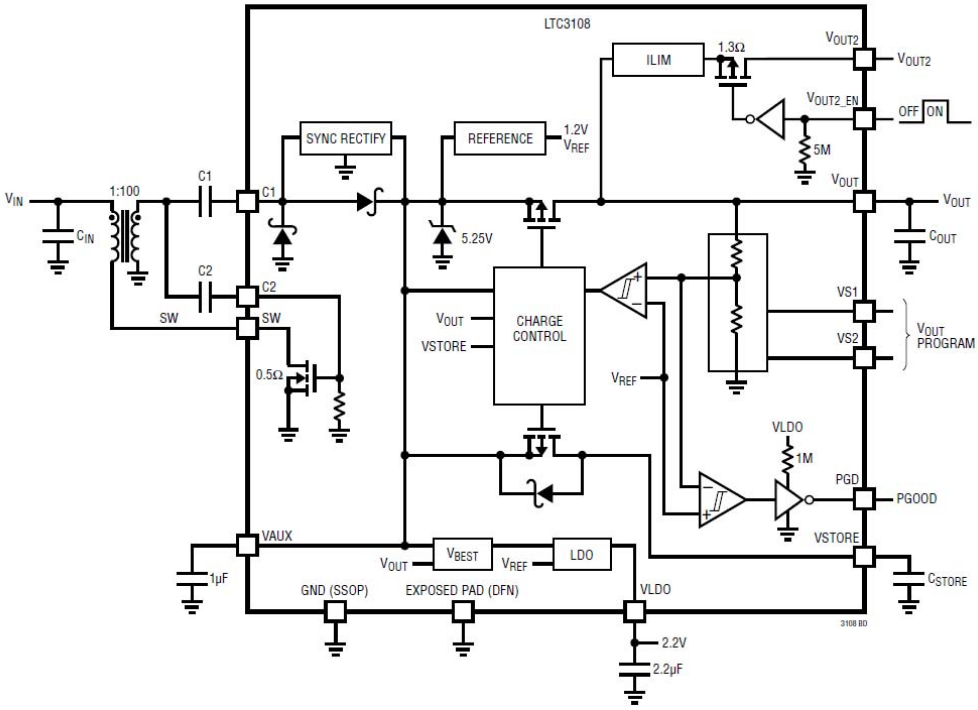

Figure 82 An Energy Harvesting Application Using DC Transformer

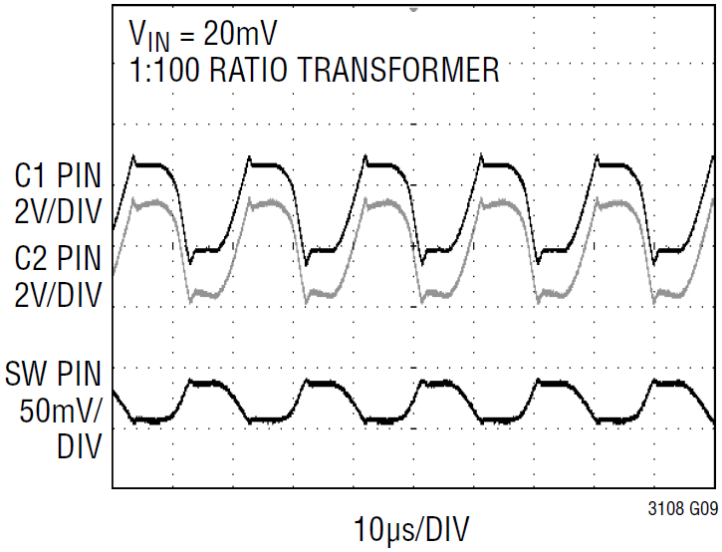

Figure 83 Input/output Waveforms of a DC Transformer[41]

4.6.DYNAMIC RANGE OF THE TRANSFORMER VOLTAGE CONVERSION CIRCUIT

One of the common issues for both direct transformer voltage conversion circuit and the DC voltage conversion transformer circuit is the input dynamic range issue. Since the turns ratio of a given transformer is fixed, this would reduce the output dynamic range of the energy harvesting devices and introduce additional loss. For example, in Figure 82, the input signal to terminal C1 cannot exceed a maximum voltage of 6V to avoid permanent damage to the IC internal circuit. Since the start up voltage of the input is 500mV, the dynamic range for the output of the transformer is therefore 0.5V~6V.

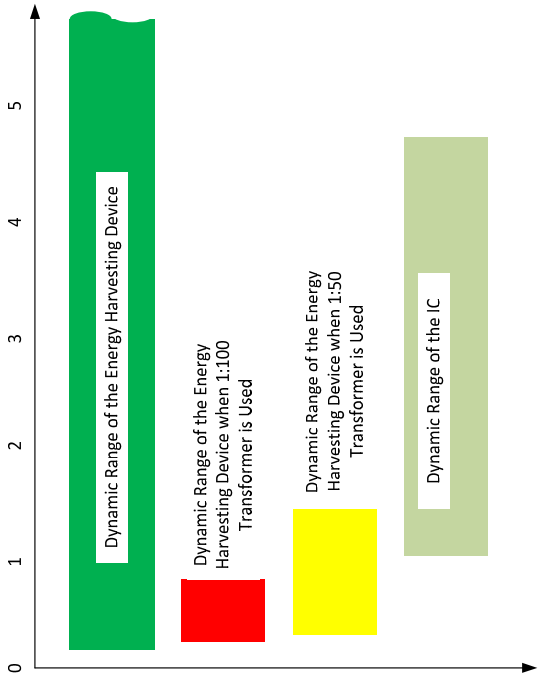

Figure 84 Dynamic Range Limitation of the Transformer Circuits

However, if a 1:100 transformer is used, the input range will be reduced by approximately the turns ratio of the transformer. In this case, the output of the energy harvesting device needs to be restricted between 5mV~60mV before the internal clamp circuit activates and restricts the transformer output. This would introduce additional energy loss because the typical large dynamic range of the energy harvesting devices. Figure 84 illustrates the dynamic range restriction of the transformer voltage conversion circuits.

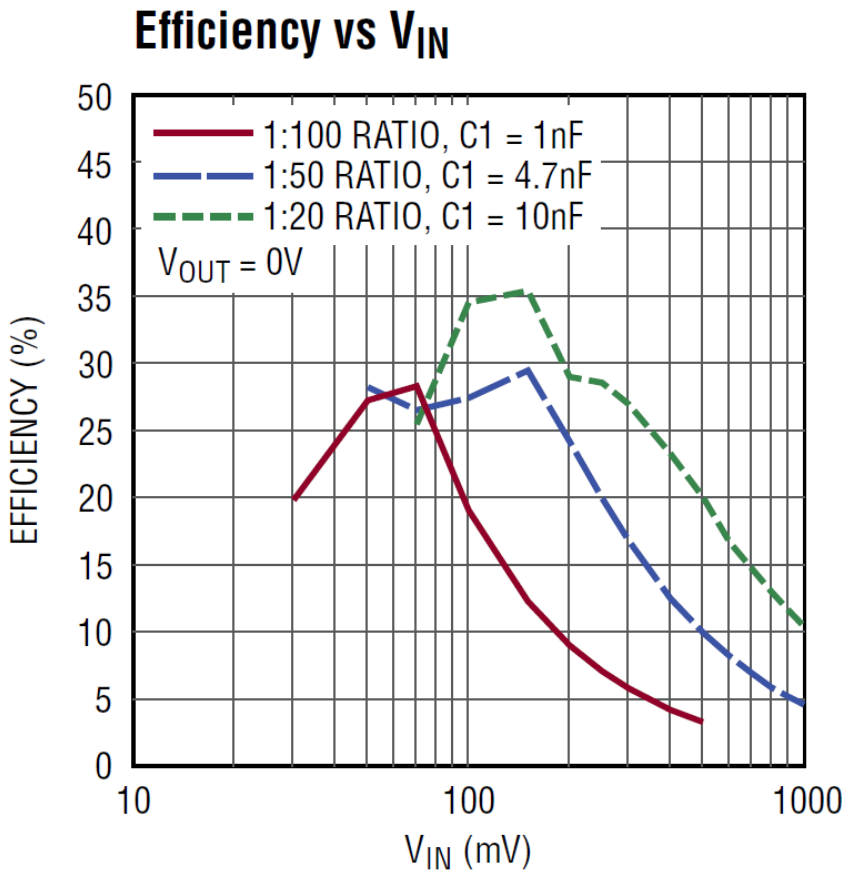

Figure 85 Optimal Input Voltage Range for Transformer Circuit's High Efficiency Operation in Energy Harvesting Applications[41]

4.7.SUMMARY

This chapter presents the passive voltage boosting circuits for energy harvesting applications. Using a PVDF wind energy harvesting application as an example, this chapter demonstrates the process of designing a passive voltage boosting circuit for a capacitive energy harvesting device.

A PVDF piezoelectric energy harvesting device is characterized for both its electrical parameters as well as mechanical properties. A circuit model for the PVDF's electrical property is used to analyze the LC resonant condition of the passive voltage boosting circuit. A device mechanical model and an energy harvesting application model are developed to characterize the energy conversion behavior with regard to the mechanical excitation. By introducing an inductive load to the capacitive energy harvesting device, an LC resonant circuit is developed with its resonant frequency ideally located near or at the high efficiency region of the energy harvesting excitation. However, in this specific example, the extremely low frequency of the system mechanical resonant frequency made it impractical to match the LC electrical resonant frequency. As a result, both the voltage conversion ratio and energy conversion ratio were degraded due to the high source impedance of the energy harvesting device and the relatively high magnetizing inductance of the non-ideal transformer. The lowest LC resonant frequency achieved is in the 9000Hz range which might be useful for other high frequency mechanical vibration energy harvesting applications.

This chapter also discussed the use of DC transformers, which functions as the direct transformer except can be used to boost up DC input.

Both direct and DC transformer circuits have an intrinsic limitation for practical circuits. They usually have a specific input voltage window due to the limitation of the maximum input voltage range of the next circuit stage. Beyond this window, the overall circuit efficiency drops due to the required voltage clamping action for higher amplitude inputs.

CHAPTER 5. VOLTAGE CONVERSION TOPOLOGIES FOR LOW VOLTAGE ENERGY HARVESTING APPLICATIONS

5.1.INTRODUCTION

Voltage conversion is the process of converting electrical energy from one electrical potential level to another to meet the application requirement. Voltage conversion is necessary because the existing electrical components and energy storage devices require minimum supply voltages to function properly. Despite the renewed efforts in the IC technology to keep driving down the IC operating voltages from generation to generation in order to reduce total power dissipation and increase circuit speed, the operating voltages of the modern electronic circuits are almost all above 1.0V to reduce the MOSFET leakage current and standby power dissipation.

On the other hand, the rated operating voltages of the energy storage devices are primarily determined by the battery chemistries and can range from 1.2V to 4.0V. As battery technologies improve, the operating voltages of the batteries are motivated to increase further for higher power and energy densities. This creates a large gap between the voltage outputs of the low power, low voltage energy harvesting devices and their desired applications. A high efficiency voltage conversion circuit is therefore needed to boost the voltage output of the energy harvesting device to a higher voltage level which can drive its intended load.

There are two types of active circuits which can step up the input voltages. Depending on the type of energy storage component used in the voltage boosting circuits, these circuits usually can be divided into charge pump circuits and inductive switching mode converters.

Charge pump circuits use capacitors to store and stack up input voltages to acquire higher output voltage. Although simple to implement, charge pump circuits usually have low load drive capacity due to the limited energy density of the capacitive energy storage device. However, this is usually not an issue for low power energy harvesting applications because the relative low energy available from the source.

Inductive switching mode power converter circuits are a family of versatile voltage conversion circuits. Based on high efficiency switching action, these types of circuits can provide wide voltage conversion ratio with good system efficiency, and the relatively high magnetic energy density of an inductor makes them suitable for a wide range of energy levels.

This chapter will present the circuit analysis and prototype test results of both types of the active voltage boosting circuits.

5.1.CHARGE PUMP CIRCUIT

A charge pump circuit is a kind of DC to DC converter which uses capacitors as energy storage elements. First proposed by Swiss physicist Heinrich Greinacher in 1919, John Douglas Cockcroft and Ernest Thomas Sinton Walton developed on

which can step up the voltage up to 800,000 voltages in their particle accelerator and won the Nobel Prize in 1951.

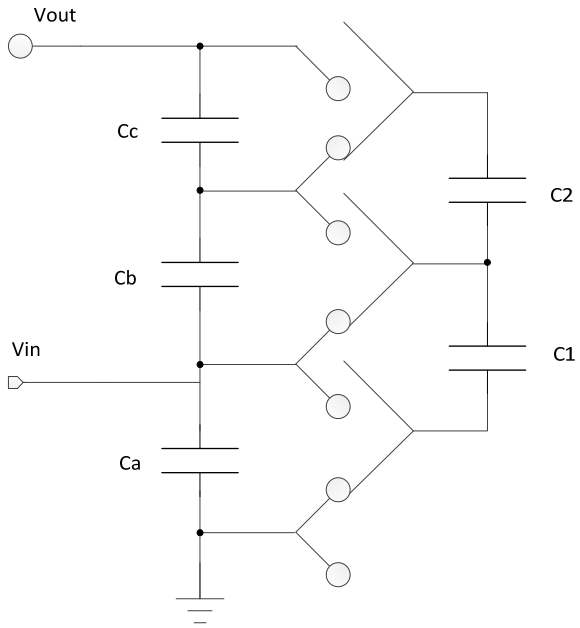

Figure 86 Cockcroft-Walton Multiplying Circuit

Figure 86 shows the circuit schematic of the Cockcroft-Walton multiplying circuit. By mechanically shifting the positions of the switches, Cockcroft and Walton were able to build up a potential up to 800,000 voltages in the Cavendish Laboratory in Cambridge, England, and successfully disintegrated a lithium nucleus into two alpha particles.

Modern charge pumps use diodes instead of the mechanical switches to achieve periodical capacitor charging and voltage multiplying. Figure 87 is one of the circuit diagrams for voltage multiplying with an AC input. Although this circuit is simple, it

is obvious that the use of diodes as reverse current blocking devices prevents this circuit from being used for low voltage applications due to the diode's forward voltage drop. Figure 88 shows the schematic of the improved Dickson charge pump with NMOS switches. The N-channel MOSFETs are used as switches to reduce the fixed forward voltage drop of the diodes.

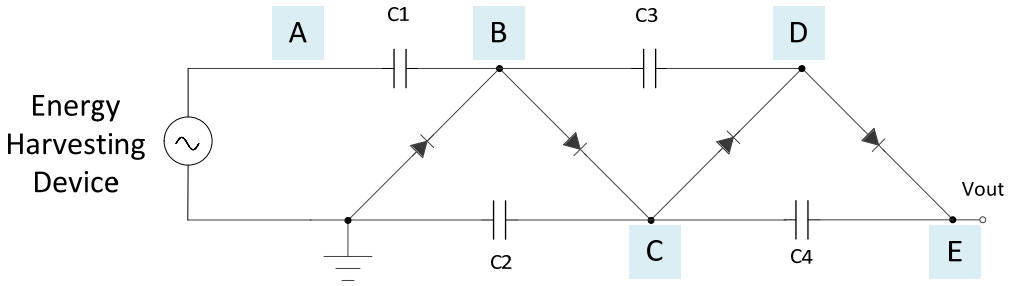

Figure 87 Crockcroft-Walton Multiplying Circuits with Diodes

The output voltage of the charge pump is the sum of the input voltage plus the voltage on the charge transfer capacitor. If we ignore the diode forward voltage drop, the output voltage of a charge pump circuit can be easily calculated. For example, in Figure 87, the maximum voltage in node A is the peak input voltage, and the voltage in node B is the peak of the input voltage in addition to the voltage on capacitor C1, which is 2x the input peak voltage. Similarly, the peak voltage in node C is 3x the input peak voltage, and these voltage stepping stages can be cascaded indefinitely given that the components can withstand the higher voltages during operation. One of the great advantages of the charge pump circuit that at least in theory, the voltage

boosting capability can be increased by simply increasing the stages of the charge pump circuit.

$$v_{out} = n \cdot v_i \tag{83}$$

However, in real charge pump circuits, the voltage boosting efficiency is degraded by the voltage drop of the reverse current blocking diodes. For example, if the diode forward voltage drop is v_d, equation (83) will become:

$$v_{out} = n \cdot (v_i - v_d) \tag{84}$$

Equation (84) shows the relationship of the charge pump output voltage with regard to the diode forward voltage drop. It can be seen that the charge pump's voltage boosting capability is degraded quickly for low voltage applications when the input voltage is comparable with the diode forward voltage drop.

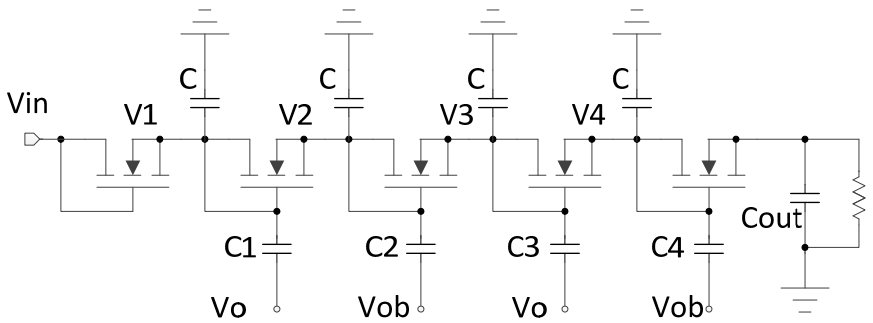

Figure 88 Dickson Charge Pump w/ NMOS Switches

One way to mitigate the diode forward voltage drop impact in charge pumps is to use diode-connected MOSFETs instead of p-n junction diodes as shown in Figure 88. The circuit shown in Figure 88 operates in the same principle as the circuit in Figure 87

except using diode-connected MOSFET for reverse current blocking. The output voltage of the circuit in Figure 88 is therefore:

$$v_{out} = n \cdot (v_i - v_{th}) \tag{85}$$

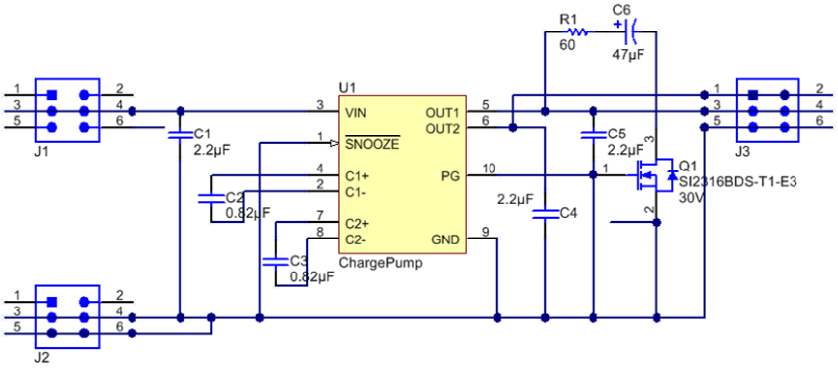

Figure 89 An Integrated 2x Dickson Charge Pump Circuit

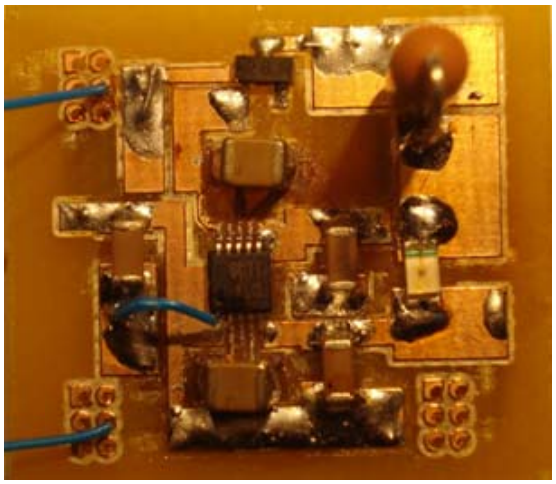

Figure 90 Prototype Circuit of the 2x Dickson Charge Pump

A charge pump circuit with similar circuits shown in Figure 88 is built to evaluate the power conversion efficiency of the Dickson charge pump with diode-connected

MOSFETs. The circuit schematic is shown in Figure 89 and the actual circuit is shown in Figure 90.

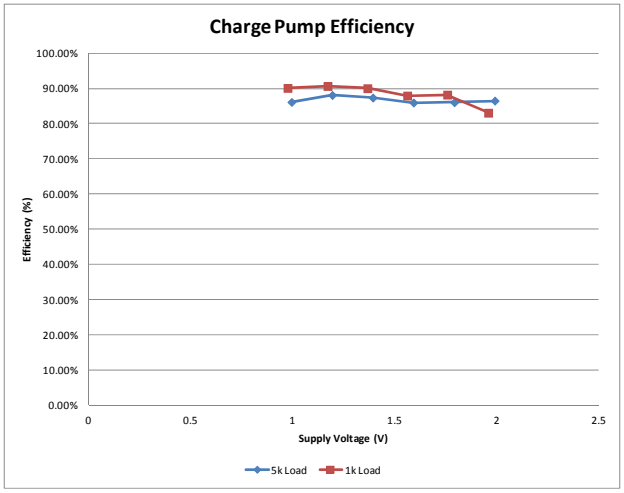

Figure 91 Bench Measured 2x Charge Pump Efficiency

Figure 91 shows the power conversion efficiency of the 2x Dickson charge pump with a diode-connected MOSFET. The efficiency at the operating input voltage range of 0.9V~2.0V is around 90%. However, due to the minimal supply requirement, the charge pump circuits will not able to work below 0.9V. This precludes it to be used for low voltage power conversion applications even though it has respectable power conversion efficiency.

As discussed in chapter 3, MOSFETs suffer from substrate effect in which the biasing of the substrate modulates the MOSFET's gate threshold. This is especially true for the charge pump circuit. As the number of the charge pump stage increases, the charge transfer efficiency quickly diminishes to very low level, preventing the efficient operation of the charge pump circuit. Figure 92 shows the charge transfer

efficiency vs. number of stages in a typical 2-phase charge pump design. As can be seen in this figure, the charge pump's efficiency drops quickly with regards to the number of stages cascaded, limiting the maximum voltage the charge pump circuit can use[42].

Stage	Efficiency (Clock = 3v)
0	100.00%
1	67.00%
2	44.89%
3	30.08%
4	20.15%
5	13.50%
6	9.05%
7	6.06%
8	4.06%
9	2.72%

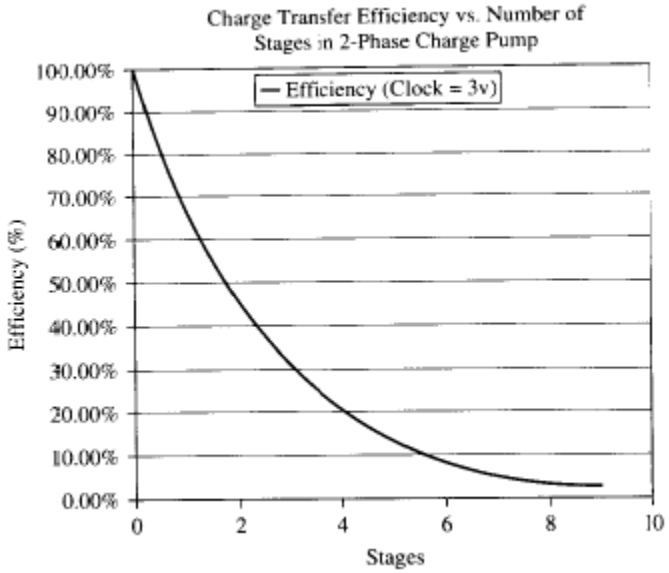

Figure 92 Charge Pump Charge Transfer Efficiency vs. Stages[42]

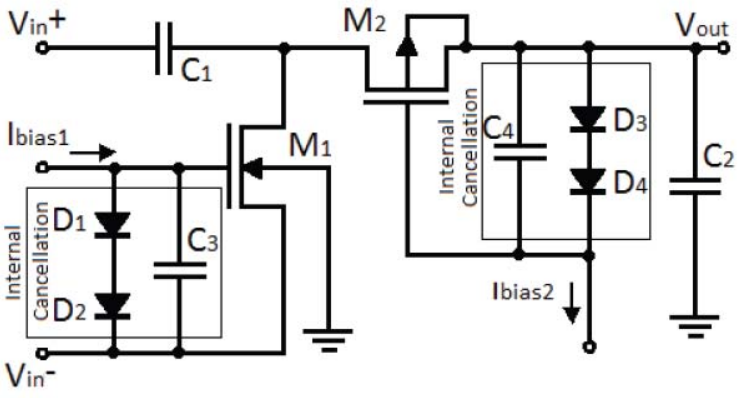

Figure 93 Charge Pump with Vth Cancellation[9]

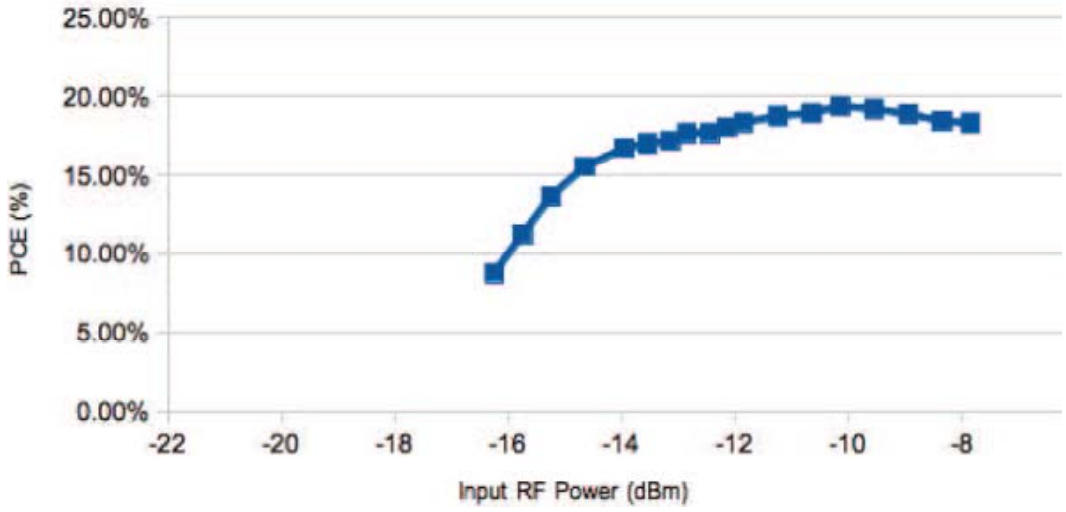

Figure 94 Efficiency Measurement of Charge Pump Circuit[9]

To improve charge-pump operating efficiency in low-voltage, low-power applications, Vth cancellation method was proposed[19]. Figure 93 shows the circuit schematics of a charge pump circuit with a Vth cancellation scheme. Unfortunately even with the Vth cancellation method, the power conversion efficiency is still in the lower 20% as shown in Figure 94.

5.2.SWITCHING MODE POWER CONVERTER CIRCUIT

Switching mode power converters were initially developed in the 1960s when solid state switches are available with the development of semiconductor devices. Initially used for high power density, low size and light weight power supplies, switching mode power converters quickly become the prevailing solutions for high efficiency energy conversion, including DC-DC, AC-DC, DC-AC and AC-AC conversions. For

the low power low voltage energy harvesting applications, a DC-DC voltage step-up topology provides the solution.

The most commonly used DC-DC step up converter is the inductive boost circuit. Figure 95 shows the basic schematic of a boost converter[43]. A boost converter usually has an energy storage inductor L, an active switch SW, a freewheeling diode D and output filter capacitor C. The input to boost converter is DC voltage Vin and the output voltage is also a DC with some ripple component.

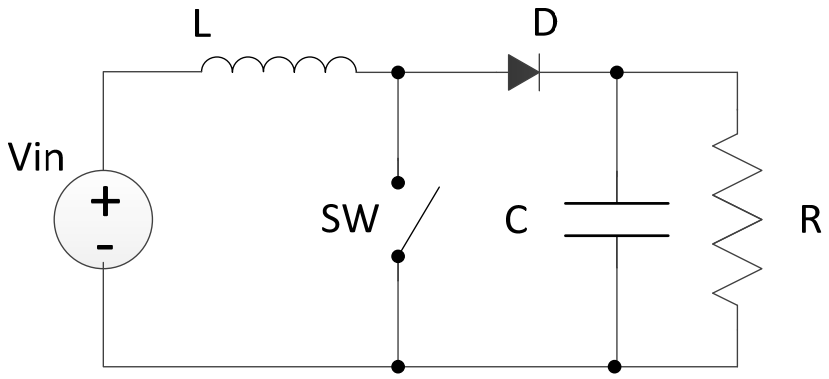

Figure 95 Basic Schematic of a Boost Converter

Figure 96 shows the current and voltage waveforms of the operation of boost converters in continuous current mode (CCM). Every clock cycle of the boost converter has two phases. During time period T1, the switch SW is on, current from the DC supply flows into the inductor and inductor current ramps up. During time period T2, the switch SW is off, the freewheeling inductor current flows through diode D and charges output capacitor as well as provides supply voltage to the load resistor.

During time period T1, the increase of the inductor current can be calculated based on the time duration and the input voltage:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_i}{L} \tag{86}$$

The increase in the inductor current at the end of T1 is therefore:

$$\Delta I_L = \frac{1}{L}\int_0^{DT} V_i dt = \frac{DT}{L} V_i \tag{87}$$

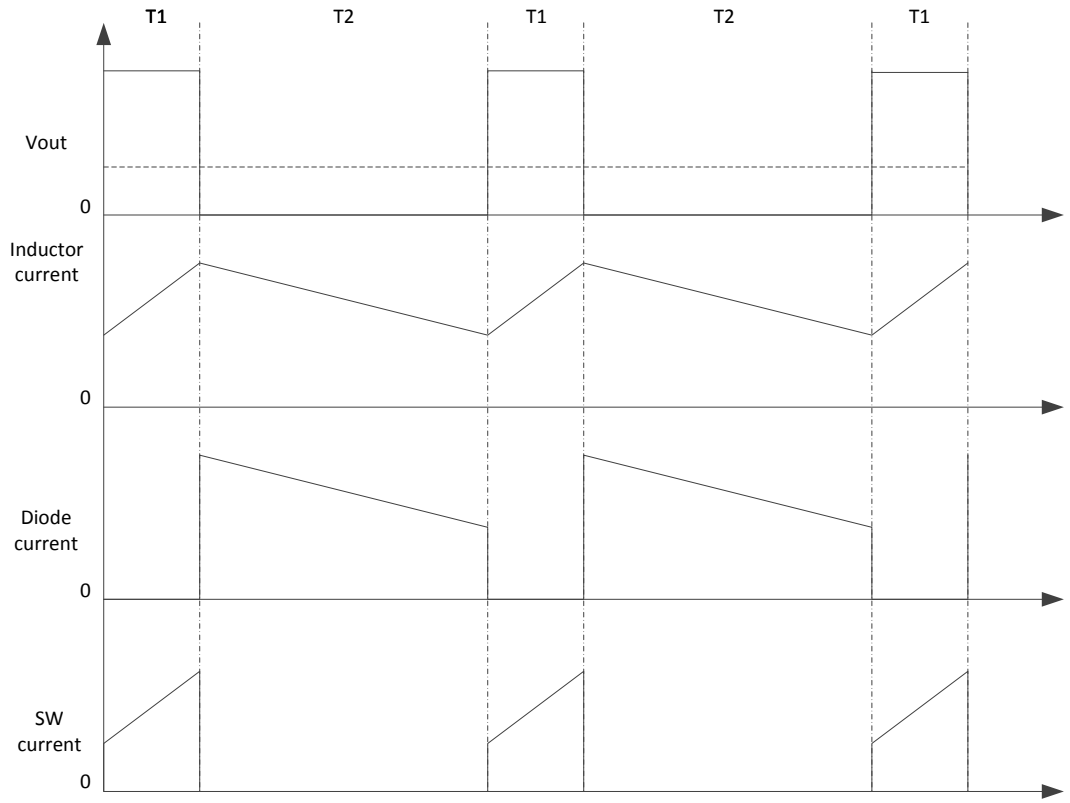

Figure 96 Current Diagram of Boost Converter in CCM Mode

Where D is the duty cycle.

During time T2, SW is off and current from the inductor flows through the load, discharging the inductor. The inductor current is therefore:

$$V_i - V_o = L\frac{dI_L}{dt} \tag{88}$$

The decrease of the inductor current at the end of period T2 is therefore:

$$\Delta I_L = \int_{DT}^{T} \frac{(V_i - V_o)dt}{L} = \frac{(V_i - V_o)(1-D)T}{L} \tag{89}$$

At steady state, the change of the inductor current at each cycle is 0, which leads to:

$$\Delta I_{L\_on} + \Delta I_{L\_off} = 0 \tag{90}$$

$$\frac{DT}{L}V_i + \frac{(V_i - V_o)(1-D)T}{L} = 0 \tag{91}$$

Simplifying this equation, the output voltage of the boost circuit can be calculated as:

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{92}$$

This is the relationship of the boost circuit in CCM mode. Since D is always between 0 and 1, eq. 31 indicates the output of the boost converter is always higher than its input voltage.

As with many other power converters, boost converter can have many different control types based on their PWM control strategy. Figure 97 shows the block diagram of a boost converter with variable frequency control. The input current is sensed for zero-cross and used to turn-on each PWM cycle. The output voltage at the Rload is sensed by a voltage divider of two feedback resistors Rf1 and Rf2. Any output voltage deviation from the set value is compared with a reference voltage Vref

and creates an error voltage. This error voltage is then combined with the PWM external ramp signal and used to turn-off the boost switch.

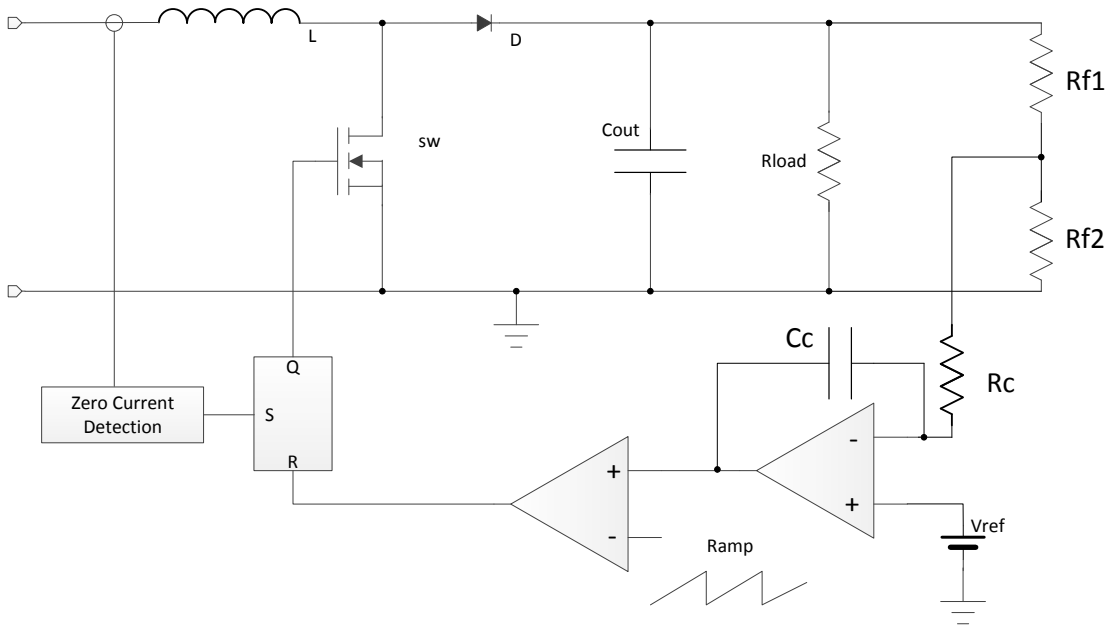

Figure 97 Boost Circuit with Variable Frequency Control

A boost circuit using variable frequency control has lower current stress for its main switch, allowing it to use a switch element which matches with the input/output power rating. However, the variation in the switching frequency makes it difficult to be synchronized with other boost circuits, and the wider frequency range tends to creates broader EMI spectrum which could be an issue for sensor applications.

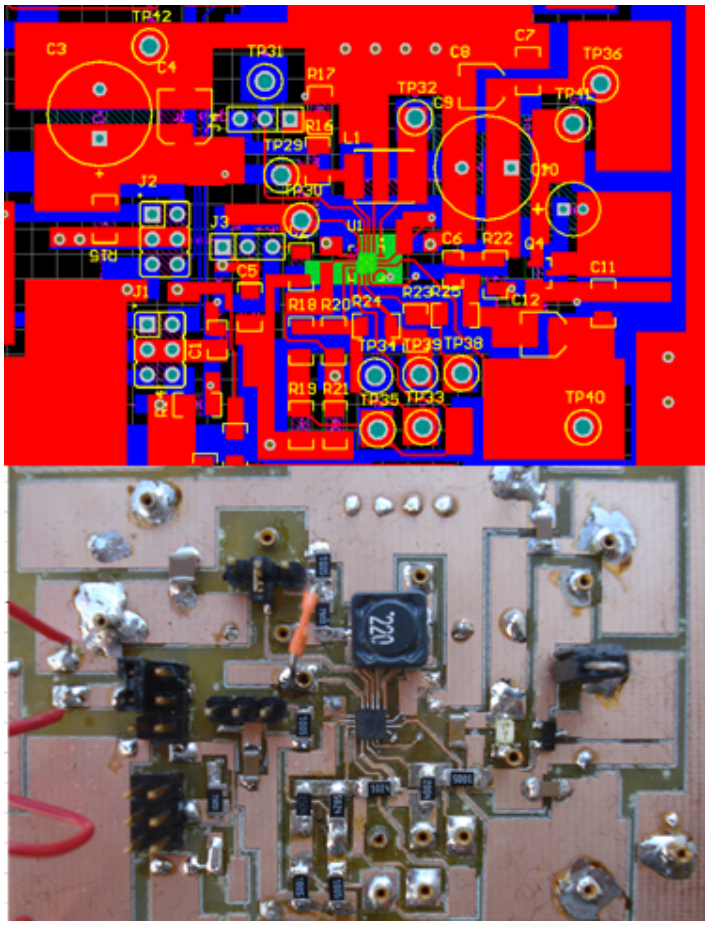

Figure 98 Prototype Circuit for Bench Testing Power Conversion Efficiency of the Boost Circuit

A boost circuit is developed to bench test the power conversion efficiency, the prototype circuit and its layout is shown in Figure 98.

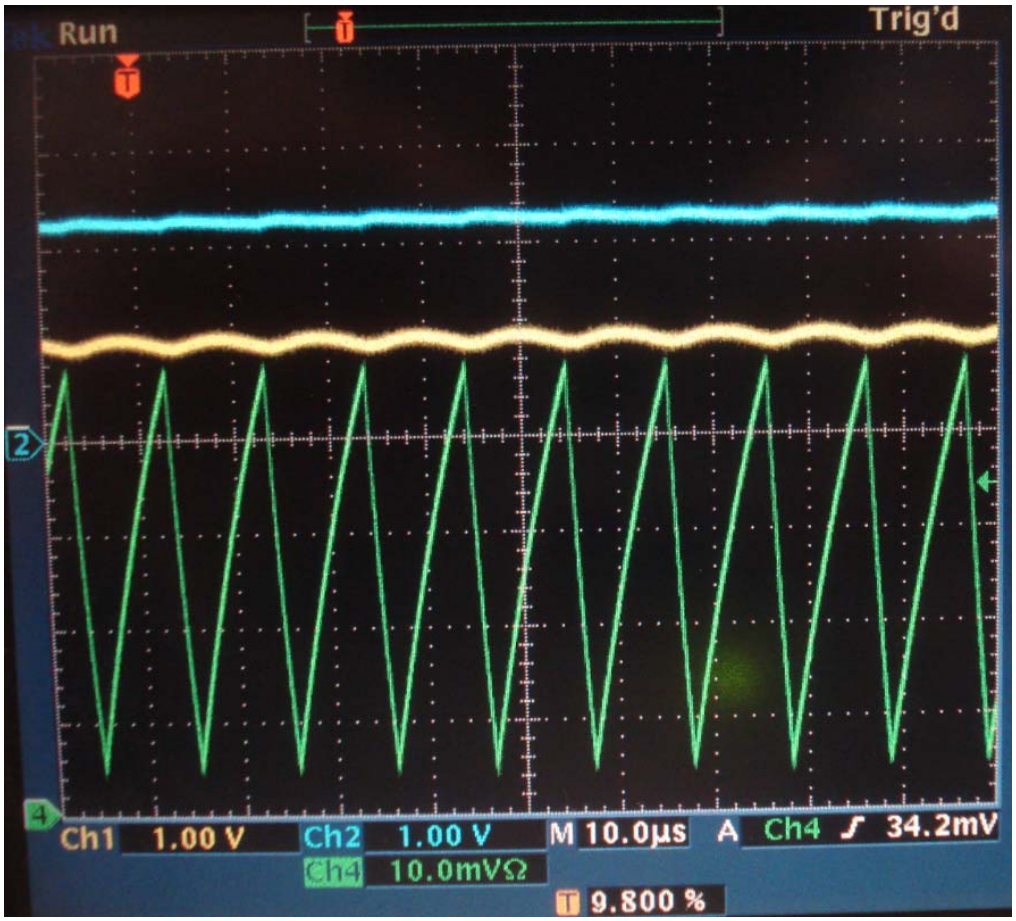

Figure 99 Steady-state Boost Operation Waveform

Figure 99 shows the steady-state waveform of the boost converter. Oscilloscope channel 1 (yellow trace) is the input voltage, channel 2 (blue trace) is the output voltage and channel 4 (green trace) is the inductor current. Channel 1 and channel 2 have the same voltage scale and reference. The higher output voltage on channel 2 shows the voltage step-up result of the boost circuit. The saw-tooth inductor current waveform is the result of variable frequency control in which the inductor current is turned-on once it is near zero.

Figure 100 shows the bench measurement results for the low voltage boost circuit. Notice that the circuit starts around 300mV and the power conversion efficiency quickly increases to 50% around 0.6V, which is below the forward voltage drop of most of the p-n junction diodes.

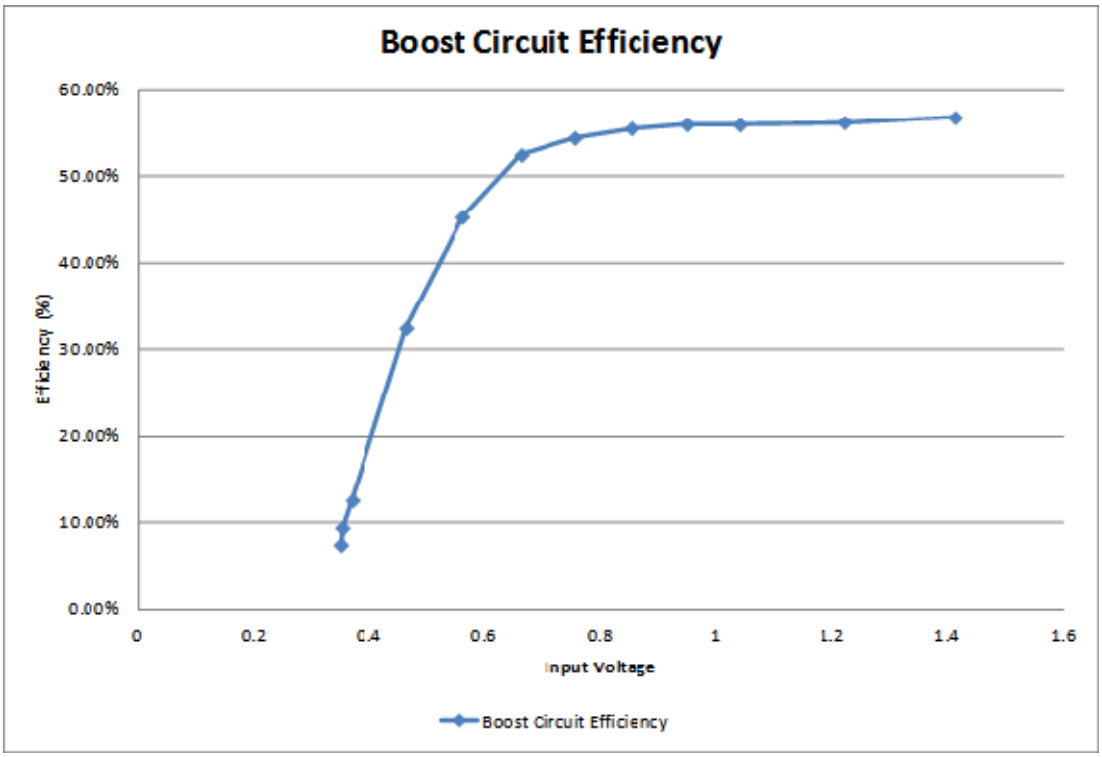

Figure 100 Power Conversion Efficiency of a Low Voltage Boost Circuit

5.3.SUMMARY

This chapter presents the circuit analysis, prototype and measurement results for two active voltage boosting circuits. For charge pump circuits, it can reach good power conversion efficiency when the total number of stages is low. However, since the

voltage conversion ratio is determined by the ratio between the specified load voltage to the available input voltage, this would post a great challenge for charge pump circuits because their power conversion efficiency drops quickly as the number of stages increases.

On the other hand, the inductive switching mode power converter provides a large variety of available circuits and voltage conversion ratios. Unlike the charge pump circuit, the voltage conversion ratio of a switching mode converter can be adjusted continuously instead of multiples of the input voltage, which eases the design of the power regulating circuit. The efficiency of the switching mode power converters can be in the 90% range although for low power applications, this efficiency is usually lower due to the overhead power dissipated in the control circuit of the switching mode controller.

CHAPTER 6. SYSTEM LEVEL DESIGN OF A HIGH EFFICIENCY ENERGY HARVESTING CIRCUIT

6.1.INTRODUCTION

This chapter discusses the system-level power conditioning circuit design for low voltage energy harvesting applications. In general, due to the diversity of the power sources used for energy harvesting, the energy conversion transducers have many different forms and operation principles, resulting in different energy conversion properties and output characteristics. It is therefore not practical to develop a universal power conditioning solution to cover all energy harvesting requirements for these applications. In fact, it is not uncommon to custom design the power conditioning circuit for a specific energy harvesting system to achieve the highest energy conversion efficiency for that application.

However, since many energy harvesting devices produce output signals that share similar electrical characteristics such as low frequency, low voltage amplitude and AC polarity, there will be some circuit functions common to many power conditioning circuits used for these energy harvesting applications. A design example for these types of circuits would be helpful for other design efforts or used as the starting point for more sophisticated designs.

In this chapter, the design objective is to develop a power conditioning circuit for a piezoelectric vibration energy harvesting application. The energy conversion

transducer is a piezoelectric device which harvests environmental vibration energy. A typical energy harvesting waveform is shown by the orange curve in Figure 101. It can be seen that the energy harvesting device output voltage is an AC signal of variable amplitudes between 100mV~1V and intermittent. The targeted load of the energy harvesting device is a green LED with a forward voltage drop of approximately 2.0V DC. The power output of the energy harvesting device is in the μW range, and the duty cycle of the energy harvesting device could be as low as 0.01. The AC frequency is around 100Hz.

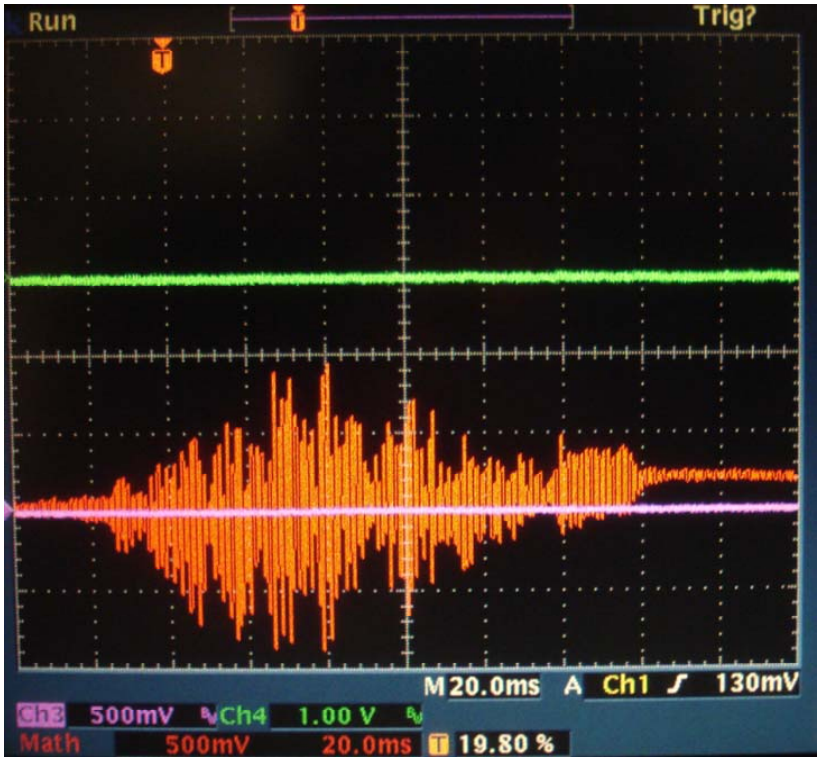

Figure 101 Typical Waveform of the Energy Harvesting Device Output

Based on the energy harvesting input and output requirements, the power conditioning circuit needs to have both a rectifier circuit as well as a voltage boosting circuit to achieve the intended function of using an AC signal with maximum amplitude of 1.0V to a 2.0V DC output.

6.2.DESIGN OUTLINE

Since this energy harvesting application requires an AC to DC rectifier circuit, the choice of the rectifier circuit topology needs to be done based on the input signal characteristics.

(1) Half-wave diode rectifier circuit

Since the input voltage is below 2.35V, a half-wave diode rectifier circuit would have higher power conversion efficiency than the full-wave diode rectifier, and based on Figure 38, a half-wave diode rectifier circuit is expected to have a power conversion efficiency of approximately 6% at 1.0V.

(2) Schottky diode rectifier circuit

Since the input power is around 1μW, which equals to 1uA at Vrms=1.0V. Since the typical reverse leakage current of a Schottky diode is around 10uA, apparently Schottky diode is not a good fit in this application.

(3) Hybrid rectifier circuit

From Figure 51, the power conversion efficiency for a hybrid rectifier circuit with virtual junction is approximately 90%. This is the best current rectifier topology for this application.

For selection of the MOSFET threshold voltage, based on the 0.01 duty ratio, the on/off ratio of the MOSFET switches should be at least 100. To minimize the standby leakage current, we choose 10000:1 MOSFET on/off ratio, which can be achieved with a MOSFET Vth of approximately 80mVx4=320mV based on Figure 41. Four 350mV MOSFETs are selected in this application.

The voltage step-up stage uses a boost converter because the low input voltage.

6.3. CIRCUIT DESIGN AND OPERATING PRINCIPLE

Figure 102 shows the circuit design for the piezoelectric energy harvesting power conversion. A hybrid rectifier circuit is used to rectify the AC input from the energy harvesting device and provide a variable DC voltage to the active voltage boosting circuit. A boost converter is used to step up the low input voltage from the energy harvesting circuit to the voltage required for the load. In this case, an LED is connected to the output to emulate the DC output function of the circuit.

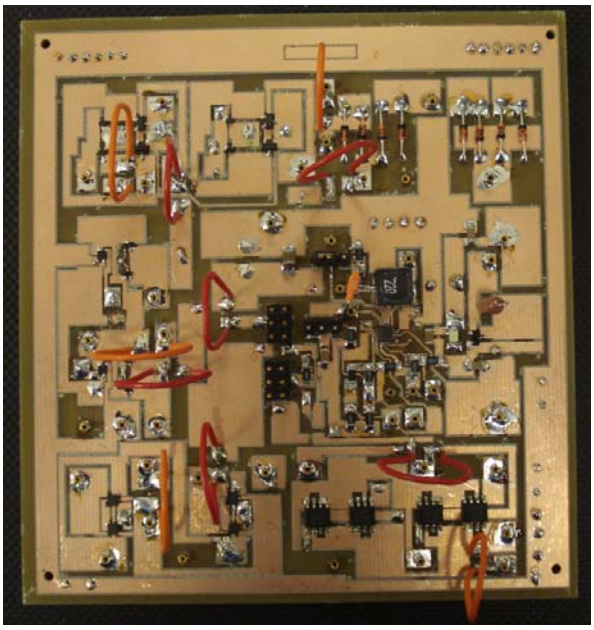

Figure 102 A Low-Voltage, Low-Power Boost Energy Harvesting Circuit

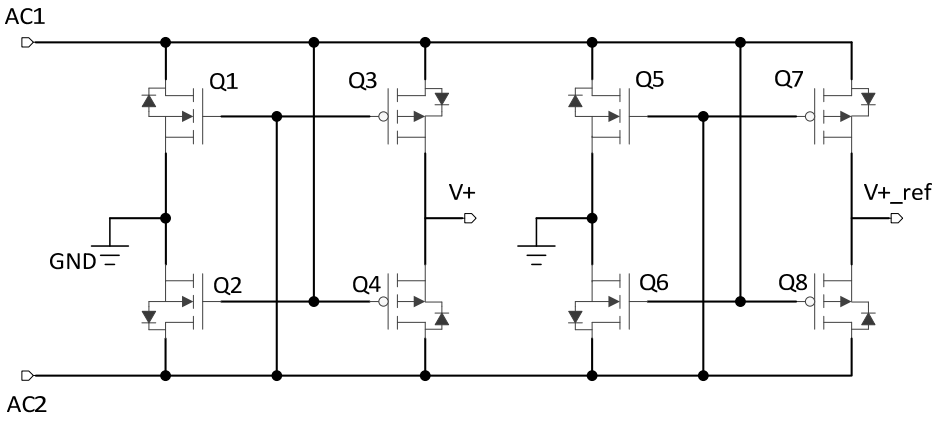

Figure 103 Hybrid Rectifier circuit with Virtual Junction

Figure 103 shows the hybrid rectifier circuit with a virtual junction. Device Q1, Q2, Q3 and Q4 form a hybrid rectifier circuit with output voltage at V+. Q5, Q6, Q7 and

Q8 are identical copies of the first rectifier circuit and are used to create the reference voltage for the virtual junction.

Figure 104 shows the circuit design for the boost power converter. Vin is the main power input from the hybrid rectifier circuit and Vj is the virtual junction reference input. The input of the Vj is connected to a capacitive voltage divider to provide a 95% scaled voltage of the input voltage, which is the virtual junction voltage applied to the rectifier MOSFETs.

The main hybrid rectifying output is feed into the main boost controller through inductor L1. Boost circuit U1 drives L1 and steps up the input voltage at node 15 of Vstor. This voltage can be used to charge energy storage elements such as rechargeable batteries and super capacitors.

A virtual junction is achieved for U1 to regulate its input voltage Vin_DC to the scaled-down Vj voltage. This generates a 5% potential difference between the output node and the input node, preventing the rectified circuit from flowing back into the source.

The capacitive voltage divider can be replaced by a resistive voltage divider with the same function. However, a capacitive voltage divider will consume less input power due to its DC impedance.

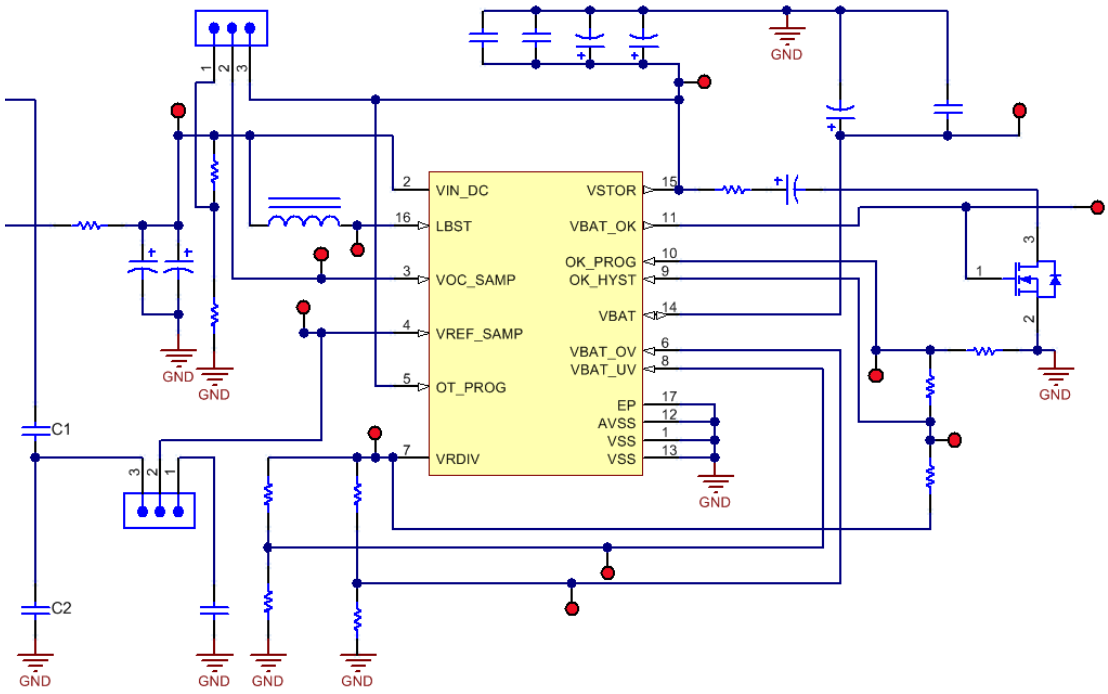

Figure 104 Circuit of the Boost Power Converter

Figure 105 shows the block diagram of the boost converter IC. The boost charge controller uses variable frequency control to generate a PWM waveform for the main converter to step-up input voltage. The MPPT controller circuit is used in this circuit for the virtual junction control. An external capacitive or resistive voltage divider is used to regulate the input voltage at a percentage lower than the Vin voltage, providing an electrical potential to prevent current back-flow in the hybrid rectifier circuit.

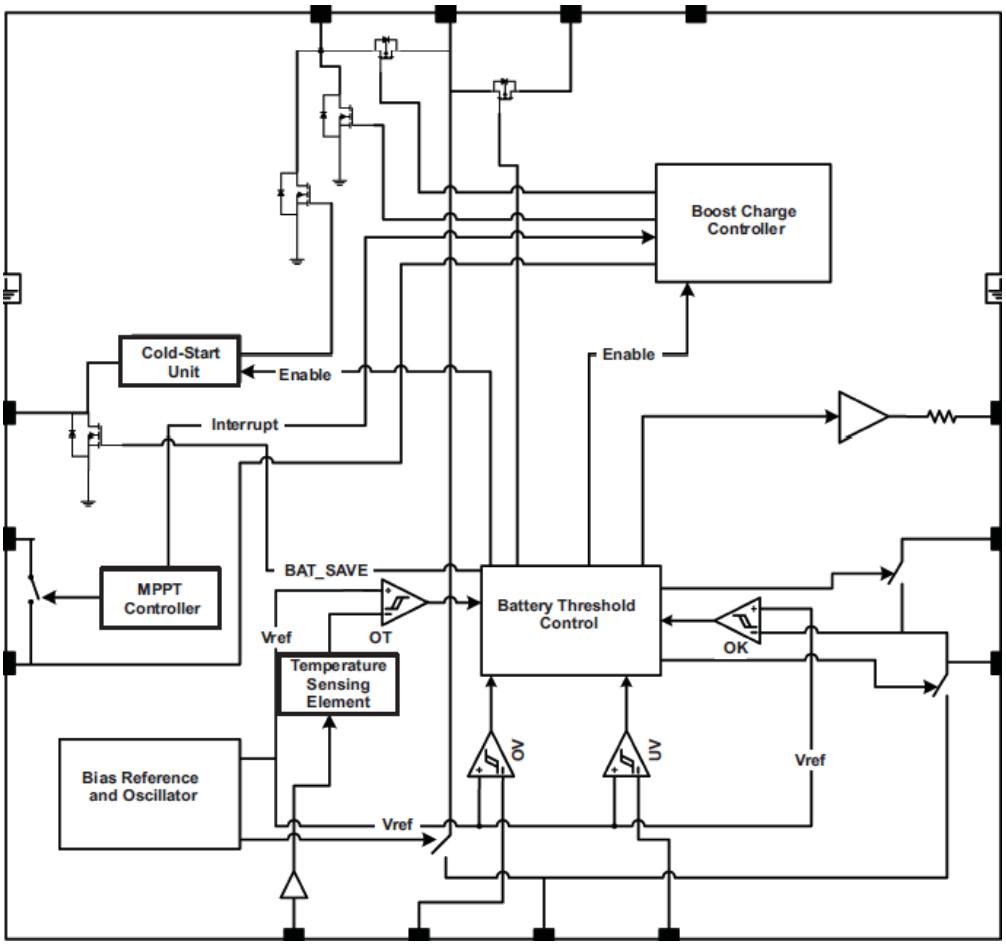

Figure 105 Block Diagram of the Boost Controller

6.4. POWER CONVERSION EFFICIENCY MEASUREMENT AND COMPARISON WITH OTHERS WORK

The low voltage, low power energy harvesting circuit is prototyped and bench tested for both energy harvesting operation and energy harvesting efficiency.

For power conversion efficiency measurement, a SRS function generator is used to provide a stable sinusoidal AC input. A function generator can provide a consistent input signal which helps to accurately measure the overall system efficiency.

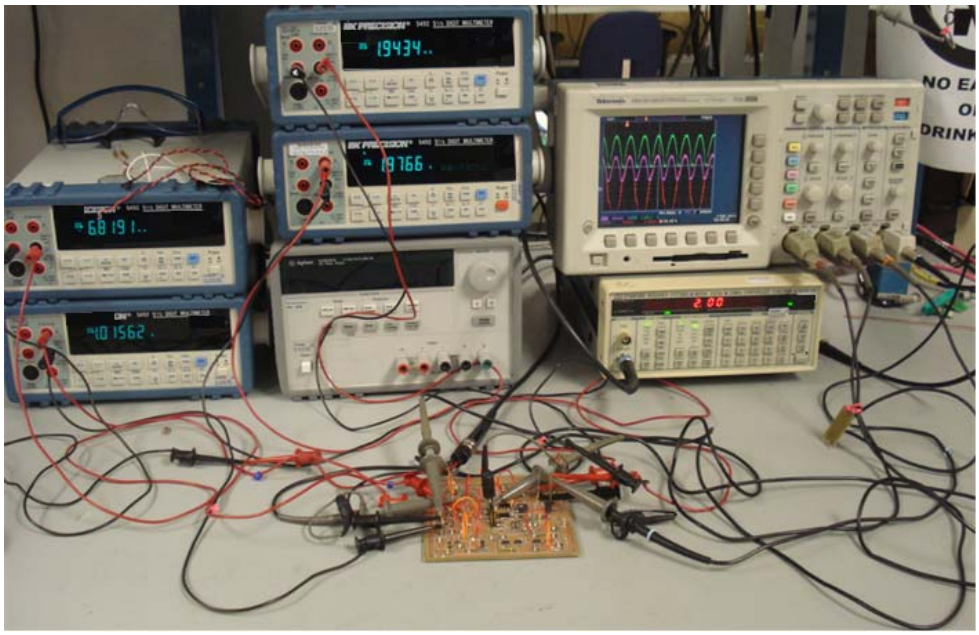

Figure 106 Low Voltage, Low Power Energy Harvesting Circuit Power Conversion Efficiency Measurement Setup

Figure 106 shows the bench setup for measuring the power conversion efficiency of the low voltage, low power energy harvesting circuit. The sinusoidal AC signal is fed

into the input of the hybrid rectifier circuit with virtual junctions and boosted with an inductive boost circuit. The input and output root-mean-square (RMS) currents and voltages are measured with four BK Precision multi-meters which are capable of measurement the true RMS value of signals with both DC and AC components.

For comparison, a benchmark circuit using a full-wave diode rectifier circuit and the same inductive boost circuit is also prototyped for power conversion efficiency measurement. The measurement results are used to compare the performance improvement of the new hybrid rectifier circuit with virtual junctions.

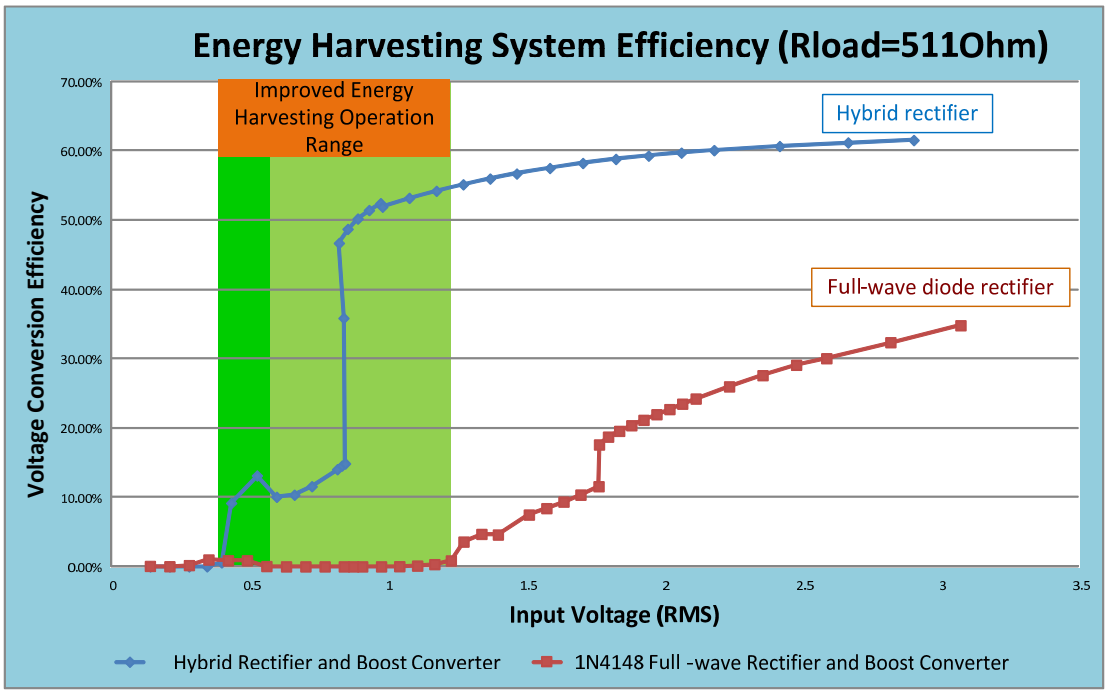

Figure 107 Energy Harvesting System Efficiency Measurement Result (w/ Function Generator and 511 Ohm Load)

Figure 107 shows the bench measurement results of the power conversion efficiencies of the low voltage, low power energy harvesting circuits. The blue curve shows the power conversion efficiency of the proposed low hybrid rectifier circuit with virtual junctions, and the red curve shows the power conversion efficiency of the full-wave p-n junction diode bridge rectifier. It can be seen that the circuit with the hybrid rectifier starts up at 10% power conversion efficiency at a supply voltage as low as 430mV, which is significantly lower than the forward voltage drop of a p-n junction diode. Its power conversion efficiency reaches 50% at around 800mV, and eventually reaches 60% for input voltages above 2Vs. As a comparison, the circuit with a full-wave p-n junction diode bridge does not start energy harvesting until 1.3V, its power conversion efficiency reaches 20% at 1.8V, and peaks at 35% efficiency at 3V.

Compared with a full-wave, p-n junction diode bridge circuit, the hybrid rectifier circuit enables the overall energy harvesting circuit to harvest low voltage, low power energy from 0.4V to 1.2V, and increase the energy harvesting efficiency for input voltages above 1.2V. This is a significant improvement from other circuits both prototyped and from literature.

6.5.LOW VOLTAGE ENERGY HARVESTING APPLICATIONS

The hybrid rectifier circuit and low voltage inductive boost circuits are bench tested with two energy harvesting devices: thermal electric energy harvesting and piezoelectric vibration energy harvesting.

6.5.1 THERMAL ELECTRIC ENERGY HARVESTING

Figure 108 shows the experiment setup for the thermal-electric energy harvesting application. A Peltier device shown in the picture is used to harvest thermal electric energy using the temperature gradient between room temperature and an ice pack. The temperature difference between the two thermal plates of the Peltier generates a thermal electric voltage of approximately 160mV. The energy harvesting circuit shown in Figure 102 converts the thermal electric energy and gets boosted up to approximately 2.2V with sufficient high efficiency to lit up a green LED.

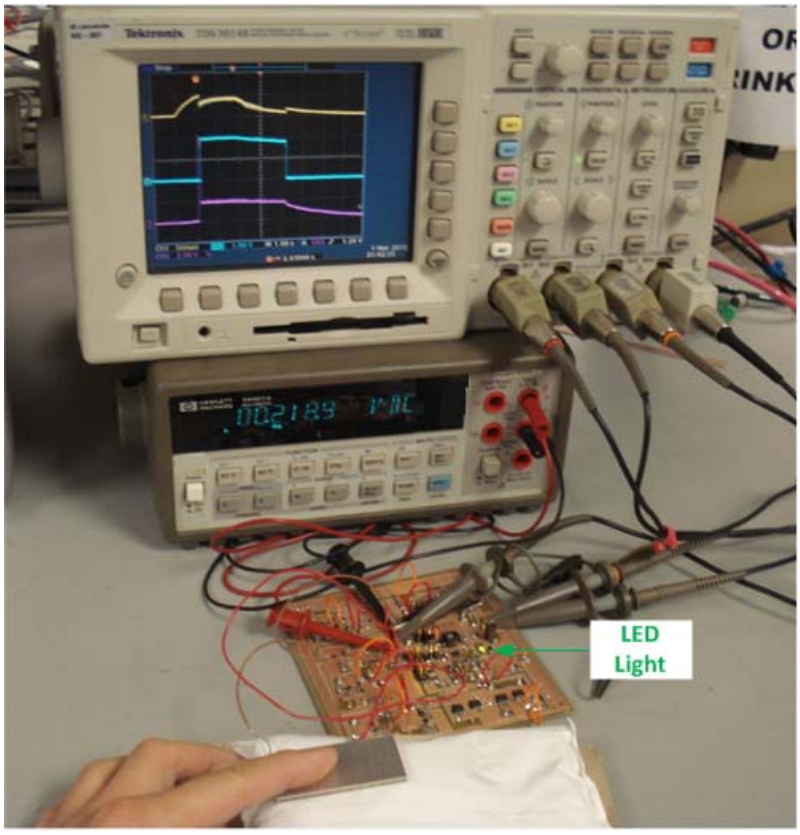

Figure 108 Thermal Electric Energy Harvesting Experiment

Notice the voltage reading of the HP34401 multi-meter which is the output voltage of the Peltier device. The bright green light pointed to on the PCB board was the light of the LED which is solely powered by the harvested thermal electric energy.

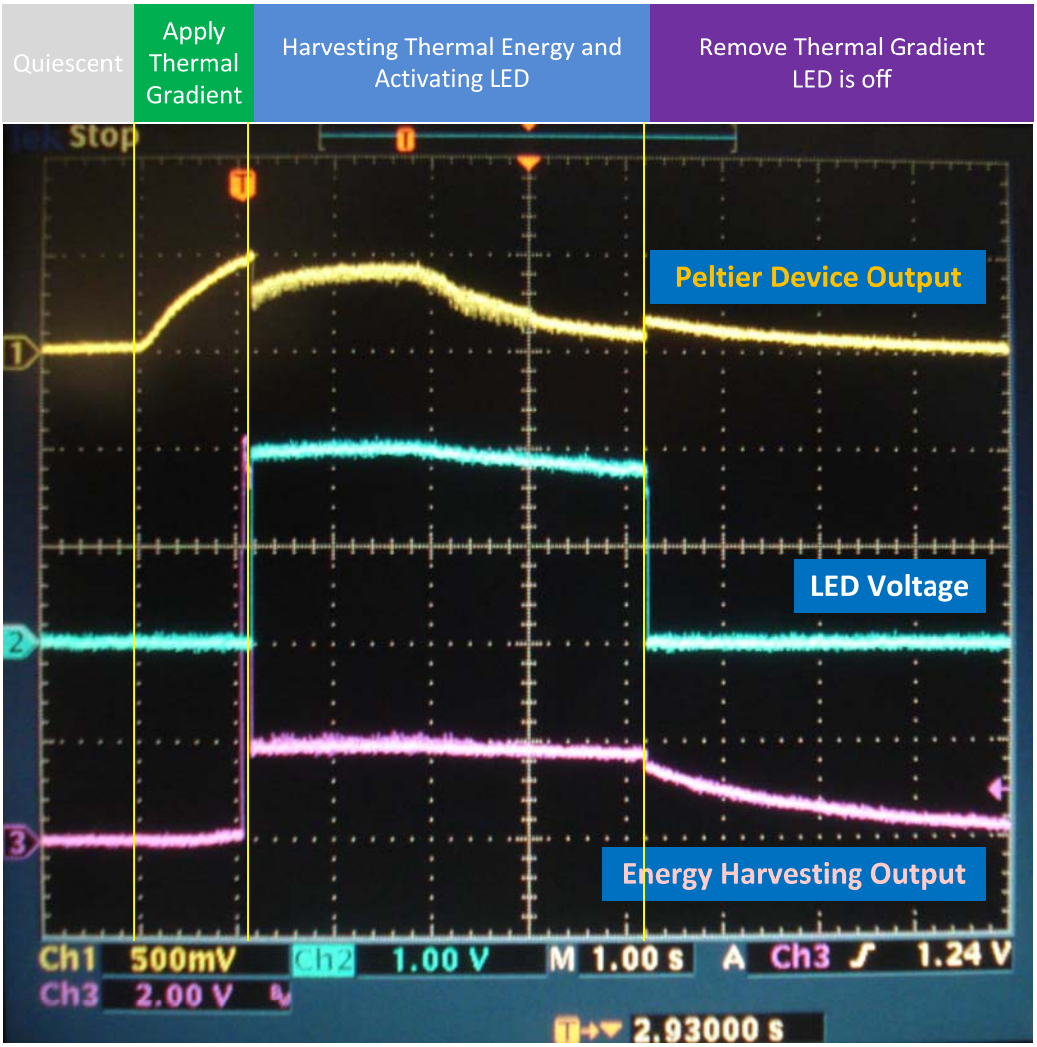

Figure 109 Waveforms for Thermal Electric Energy Harvesting Experiment

Figure 109 shows the waveform of the thermal electric energy harvesting experiment. Oscilloscope channel 1 is the output of the Peltier device which is also the input of

the boost circuit. Channel 2 is the LED drive voltage. Channel 3 is the output of the energy harvesting device. The LED in this circuit will be on around 2V drive voltage. From Figure 109, it can be seen that when the Peltier device output rises to about 500mV, the boost circuit starts up and harvests energy from the Peltier device output. As a result, the output of the Peltier device drops to around 300mV due to its internal impedance. The energy harvesting circuit generates 2V output voltage and turns on the LED. The LED is on until the output of the Peltier device drops to less than 100mV. The energy harvesting circuit turns off by removing the Peltier device away from the temperature gradient source and the output of the boost circuit discharges to ground. This experiment shows the high power conversion efficiency and wide input operating range of this boost circuit. Using direct input instead of a DC transformer, this boost circuit can maintain high power conversion efficiency with a wide input voltage range which is essential for energy harvesting applications.

6.5.2 PIEZOELECTRIC VIBRATION ENERGY HARVESTING

Figure 110 shows the bench test setup for the piezoelectric vibration energy harvesting experiment. A piezoelectric sensor is connected to the low voltage, low power energy harvesting circuit with hybrid rectifier circuit. The AC signal of the piezoelectric device is rectified by the hybrid rectifier circuit and boosted up to a higher voltage to drive a LED light.

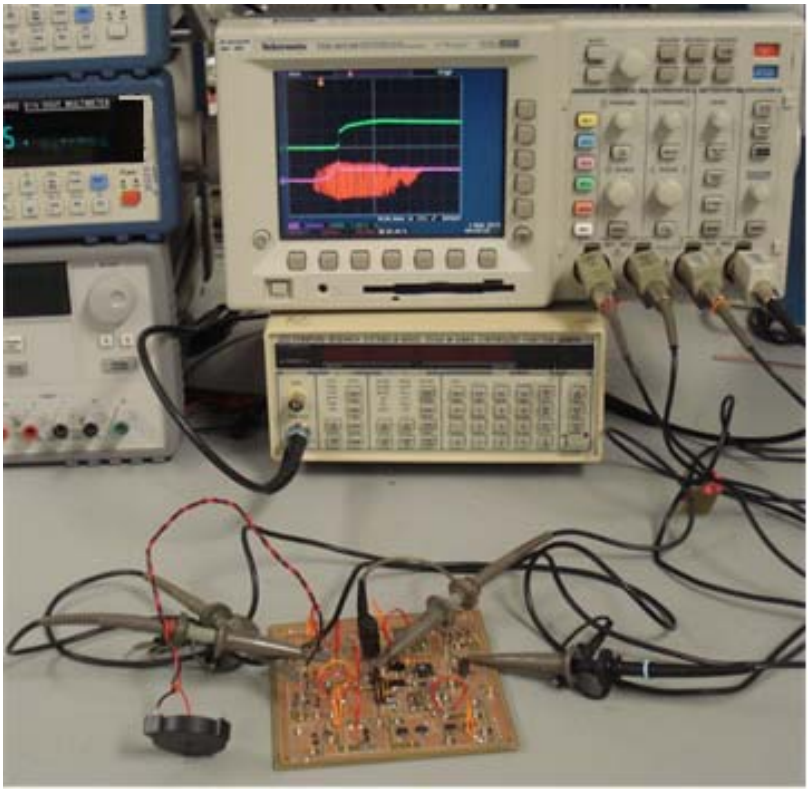

Figure 110 Piezoelectric Vibration Energy Harvesting Setup

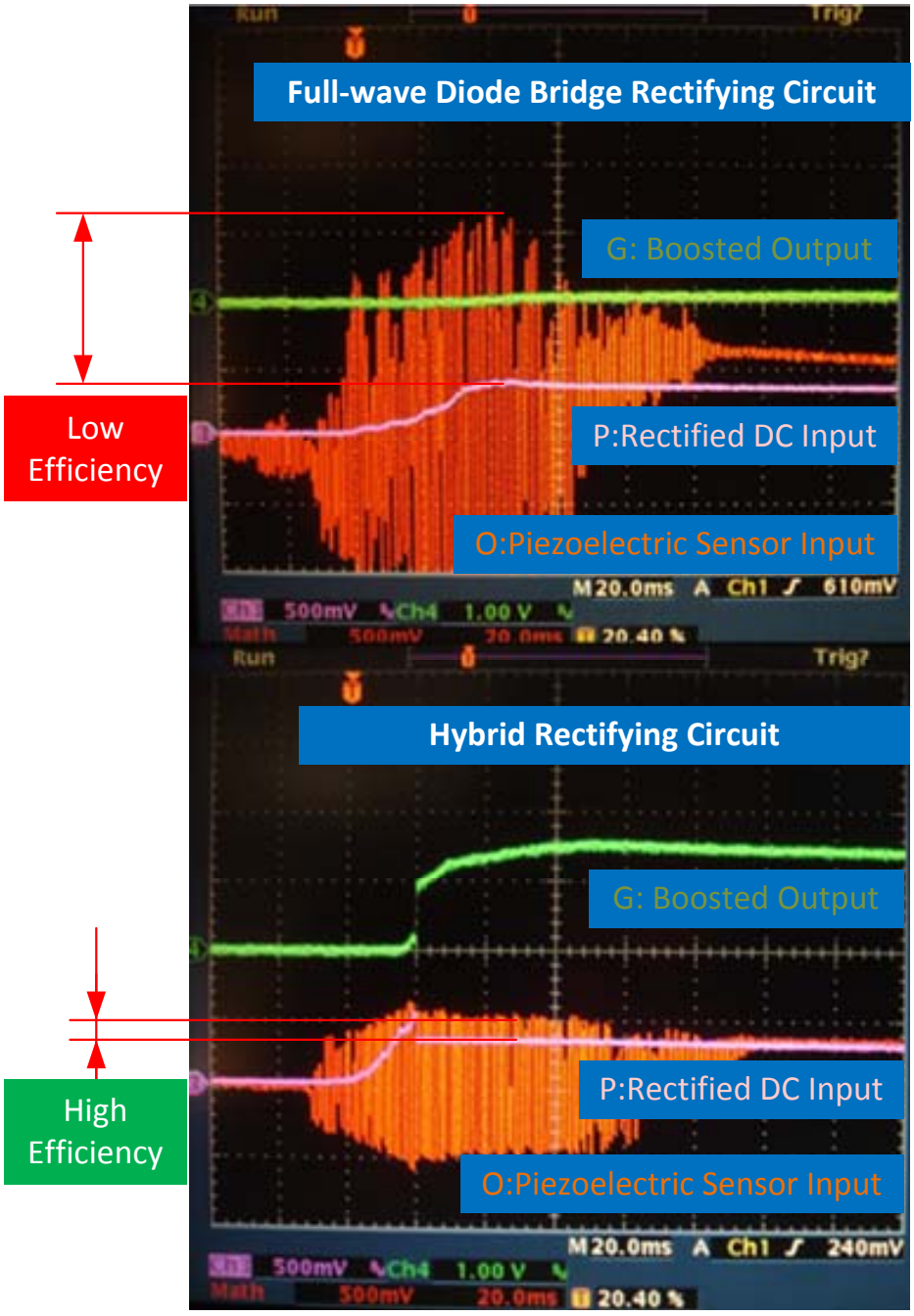

Figure 111 Input and Output Waveform of the Piezoelectric Vibration Energy Harvesting Using Low Voltage Low Power Energy Harvesting Circuit

Figure 111 shows the power conversion efficiency comparison between the hybrid rectifier circuit and a full-wave diode rectifier circuit when used in the low voltage energy harvesting circuit. The top image shows the waveform of the circuit with a full-wave diode rectifier. The bottom image shows the same circuit operating waveform with a hybrid rectifier circuit. The scales and locations of the oscilloscope traces are identical for easy comparison.

The voltage difference between the envelope of the piezoelectric sensor input and the rectified DC input indicates the efficiency of the rectifier circuit. From Figure 111, it can be seen that the hybrid rectifier circuit is much more efficient than the full-wave diode bridge rectifier circuit. It can provide more energy to the boost circuit in the next stage from a weaker input voltage, as can be seen from the difference in the boosted output signals.

6.6.SUMMARY

This chapter presents a complete power conditioning circuit design using the hybrid rectifier circuit with a boost converter for low power, low voltage energy harvesting application. The low voltage rectifier circuit uses a hybrid rectifier circuit to achieve high rectifying efficiency. The virtual junction is formed by regulating the input voltage of the boost controller to avoid the current back-flow problem of the gate-coupled rectifier circuit. Bench results show this circuit can boost a 0.435V input voltage to 2.2V and drive an LED to emulate the charge of a rechargeable battery.

Near ideal rectifying efficiency is achieved by introducing the virtual junction in the rectifier circuit to provide a directional current flow.

Table 6-1 Energy Harvesting Conversion Efficiency and Min. Start-up Voltage Comparison[44][45][46][47][48][49]

	This work	J. Colomer	Hua Yu et al	S.G. Burrow et al	G. K. Ottman et al	Maxim 638	L R Clare et al
	2015	2008	2014	2009	2002	1996	2008
Min Vin (V)	0.435	2.5	1.62	3.5*	22*	2.2	3.0
Efficiency	60%@2V	?	64.95%	-	12%@22V *	85%**	62%~68%
Topology	Hybrid rectifier with boost circuit		Full-wave diode rectifier+boost	Flyback	Buck	Buck	Full-wave diode rectifier+Buck
*: Estimated from graph							
** Not including rectifying circuit							

Table 6-1 is a comparison of the power conversion efficiency and minimum start-up voltage of the work presented in this dissertation and some recent work from the literatures. Notice that the power conversion efficiency is relatively stable over time while the minimal input operating voltage gradually reduces with the development of the low voltage power conditioning circuits. The circuit presented in this work provides the lowest minimal supply voltage based on the literature research.

CHAPTER 7. CONCLUSION

This dissertation presents the power conditioning circuit design for low-voltage, low-power energy harvesting applications. Different from conventional power conditioning circuits, the low input voltage and high output impedance of the energy harvesting devices prove to be a challenge to the existing power conditioning solutions. For example, a 0.6V diode forward voltage drop would cut off any energy harvesting outputs below this threshold voltage. The magnetizing inductance of a transformer which would normally be ignored could account for a majority of the power conversion efficiency loss.

Another challenge for the power conditioning circuit design in low-voltage, low-power energy harvesting applications is the necessity of the voltage step-up circuit. The output voltages of many energy harvesting devices are low in comparison with their intended load. The in-line rectifying voltage loss exacerbates this problem and makes it even more important to have a high efficiency voltage boosting circuit.

This dissertation reviewed the current solutions for the rectifier circuit as well as the recent development for low-voltage rectifier design. From the half-wave diode rectifier to the state-of-the-art MOSFET Vth-cancellation circuit, this dissertation investigated and compared the characteristics of these existing circuits, and proposed a new hybrid rectifier circuit for low voltage applications. By introducing the virtual junction in an otherwise bidirectional MOSFET, a new low voltage, high efficiency rectifier circuit can provide more efficient current rectification for energy harvesting

applications. Bench data indicates this new rectifier circuit has the highest power conversion efficiency in comparison with other passive rectifier circuits from the literature.

Three different voltage boosting circuits are investigated in this work. Although the passive voltage boosting circuit appeared to be an easy solution for energy harvesting devices with AC output, the challenge in matching the resonant frequency with the energy harvesting application has proved to be difficult especially for low frequency energy harvesting applications. The typically high output impedance of the energy harvesting device further degrades the voltage conversion ratio, and the parasitic components such as magnetizing inductance could cause significant power conversion efficiency loss in low power energy harvesting applications.

Charge pump circuits including “voltage doubler” circuits are among many circuits being explored by low-voltage applications. However, the low energy conversion efficiency due to the MOSFET substrate effect restricts their application for energy harvesting applications. The charge pump circuit also has a disadvantage that it usually cannot provide continuous output voltage, which introduces additional power loss in the subsequent voltage regulating circuits.

Inductive switching mode power converters, on the other hand, prove to be an efficient and versatile solution for the voltage step-up needs of the energy harvesting devices. Using a boost PWM circuit as an example, this dissertation provides a low-

voltage, low-power energy harvesting circuit designs to convert a low voltage of 0.5V to 2.0V and beyond with good energy conversion efficiency.

CHAPTER 8. DISCUSSION

Efficient power conditioning for low-voltage, low-power applications has been a challenge for many energy harvesting applications. Without efficient power conversion, many of the energy harvesting devices will have a large portion of their harvested power dissipated in the power conversion process, preventing them to be useful in practical applications.

This work presents the research work on high-efficiency power conditioning circuit design oriented for low-voltage, low power energy harvesting applications. However, due to the diversity of the energy sources and energy-harvesting approaches, there will be situations for which the solution proposed in this dissertation may not be suitable. It is important to evaluate the characteristics of the energy source and explore if there are other ways to provide an energy conversion solution for those applications.

Due to the limited time, some of the experiment and bench verification work used a high output impedance signal generator to emulate an energy harvesting device. However, the system level power conditioning circuits were tested with three different types of actual energy harvesting devices and proved to match the results collected with an emulated energy harvesting source.

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