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High Performance Hybrid Switched-Capacitor Converters for Aerospace Applications

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Abstract

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Innovations within power electronics are necessary to enable future electric aircraft and space exploration. In these aerospace applications, power converters must be light-weight, efficient and reliable. Conventional, inductor-based, power electronics tend to be heavy, and have high switch stress making them difficult to implement in these applications. In this thesis, hybrid switched-capacitor converters are explored as they utilize energy-dense capacitors as the primary energy storage element, and also decrease the voltage stress of the switches. The basics of hybrid switched-capacitor converters are covered, with a focus on why these topologies are suitable for aerospace applications. Next, the losses of the capacitors, the main building block of these converters, are characterized and a model is proposed which allows for simple loss estimation. Then, the design and flight qualification of a hybrid switched-capacitor converter is discussed, showcasing a converter with high efficiency, power density and reliable control. Moreover, the safe control of hybrid switched-capacitor converters during shutdown is described, with a model proposed which allows designers to understand the shutdown of the converter and trade-offs in different shutdown techniques. Hybrid switched-capacitor converters are motivated for their use in harsh space environments, where radiation effects make designing high performance converters challenging. Two different converters designed for space applications are then described, utilizing techniques such as partial power processing to minimize passive component mass. Overall, this thesis showcases the design of several high performance hybrid switched-capacitor converters, but also introduces models and comparison frameworks to allow future designers to better understand the design and operation of hybrid switched-capacitor converters in aerospace applications.

To Chance.

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Chapter 1

Introduction

1.1 Introduction

The need for high performance power converters is growing as there is an increase both in the number of renewable energy sources, such as solar and wind energy and electric loads, such as electric vehicles. It is estimated that by 2030, over 80% of electricity in the United States will flow through at least one power converter [1]. The need for further electrification expands beyond terrestrial applications and into sky and space.

By 2030, the number of aircraft passengers is expected to triple [2]. Hybrid electric, and eventually fully electric aircraft, offer solutions in reduction of maintenance, noise and emissions [3]. However, to enable hybrid electric aircraft, we need innovation within the electric drivetrain, requiring extremely light-weight and efficient power converters [4].

Space exploration has seen a recent surge in interest, both in public and private organizations. With the goal of future human exploration of Mars, we need further technology advancements in robotic exploration, lunar micro-grids and satellites [5]. All of these technologies require high performance power converters which are light-weight and can handle the radiation effects of the harsh space environment.

This thesis focuses on these challenges associated with future electric aircraft and space exploration, where light-weight, efficient and reliable power conversion is crucial. The design of several power converters is described, and for each system the requirements and optimal performance are considered. Moreover, this thesis also tackles fundamental challenges within the design of power converters, such as the losses of key components, the control of converters to ensure safe shutdown procedures and the combination of multiple converters to utilize partial power processing.

1.2 Organization of Thesis

Chapter 2: Fundamentals of Hybrid Switched-Capacitor and Multilevel Converters

Hybrid switched-capacitor converters offer the potential for extremely dense designs, due to their use of energy-dense capacitors as the primary energy storage element. Moreover, hybrid switched-capacitor topologies result in lower voltage stress across the switches, allowing for designs which utilize high performing low voltage devices to achieve higher voltages at the input/output terminals. This chapter presents the motivation for utilizing hybrid switched-capacitor converters in aerospace applications, where light-weight designs are critical for future technology development.

Chapter 3: Characterization and Modeling of Ceramic Capacitor Losses

Recent work on hybrid switched-capacitor converters has demonstrated exceptionally high efficiencies and power densities through the use of multilayer ceramic capacitors (MLCCs). However, when used in such converters as the main energy transfer components, the capacitors experience high voltage and current ripple often under large dc voltage bias. Yet, capacitor characterization is typically done only with small signal excitation and under low or no dc bias, yielding highly inaccurate loss models. This chapter presents a technique for obtaining detailed loss characterizations of MLCCs under more realistic operating conditions through a carefully designed calorimetric setup. Experimental results from several types of MLCCs are presented over a wide range of operating conditions. Finally, a linear model is presented to accurately estimate MLCC losses.

Chapter 4: Flying Capacitor Multilevel Converter for Hybrid Electric Aircraft

Multilevel switched-capacitor converters, such as the flying capacitor multilevel (FCML) converter, offer high energy density and efficiency, over a wide voltage range, making them suitable for applications in electrified aircraft. However, concerns of reliability due to the increased number of active and passive components have limited the use of high-level count converters in aircraft applications. We present detailed component selection and design techniques to achieve this goal, along with a high-performance 28.2 kW/kg, 99.52% efficient high-voltage dc-dc step-up power converter for experimental validation.

Chapter 5: Flight Qualification of Flying Capacitor Multilevel Converter

This chapter addresses the challenges of designing a high-level count converter with the goal of extremely high efficiency and power density, with maintained reliability and flight readiness. Building on the design presented in Chapter 4, the full system design, control and fault tolerance is described, with a focus on robustness. Finally, we demonstrate successful completion of critical flight qualification testing of the hardware prototype, including thermal, shock and vibration.

Chapter 6: Safe Shutdown of Flying Capacitors Multilevel Converters

This chapter explores the dynamic behavior of the flying capacitor multilevel (FCML) converter during unplanned shutdown. A model for a general N-level FCML converter is developed, which captures capacitor non-linearities, component leakage paths, and body diode behavior. This chapter highlights how switch voltage ratings may be exceeded during unplanned shutdown, and proposes several mitigation strategies. Using a ten-level FCML converter hardware prototype, the time-domain behavior of the model is verified, and a successful hardware mitigation strategy is demonstrated which ensures safe and rapid converter shutdown.

Chapter 7: Overview of Converter Requirement in Space Applications

In the harsh environment of space, the design of power converters is particularly challenging. This chapter explains some of the types of radiation experienced in space and how wide-bandgap GaN devices can be utilized to achieve radiation hardened designs. Moreover, hybrid switched-capacitor converters are further motivated for their low switch stress and passive component mass.

Chapter 8: Flying Capacitor Multilevel Converter Designed for Electric Propulsion

Recent work has shown the high efficiency and high power density of multilevel converters in terrestrial applications. This chapter applies the advantages of multilevel converters to space applications by investigating a ten-level flying capacitor multilevel boost converter for compact and efficient high-voltage generation. The converter exploits the low on-state resistance and reduced parasitic capacitance, as well as radiation hardened qualities of GaN power semiconductor switches to achieve high efficiency and power density. Practical challenges such as driving a large number of high-side switches while maintaining high-voltage

creepage and clearance requirements are addressed through innovative cascaded bootstrap techniques for gate driver power, and a new commutation loop design with reduced parasitic inductance. The performance benefits of these techniques are demonstrated in a 1 kW, 100 V to 500 V step-up dc-dc hardware prototype, achieving 99.1% efficiency and a power density of 24 kW/kg.

Chapter 9: Composite Converter Designed for Space Applications

To enable next generation robotic space exploration, innovations in the area of high step-down voltage converters is necessary. This chapter explores the use of multilevel hybrid switched-capacitor power converters which have unique advantages in mass-critical and harsh radiation space environments. A composite converter topology is presented which utilizes two different hybrid switched-capacitor converters in a partial power processing system. First, a fixed-ratio capacitively-isolated resonant Dickson converter is designed for a high step-down conversion ratio and to process the majority of the system power. In addition, a flying capacitor multilevel (FCML) converter is designed to provide regulation over a wide range of input voltages. The optimization of each converter is discussed with careful attention dedicated to the minimization of passive component mass. The hardware results for each converter and the full composite system are presented, showcasing a system efficiency of over 96% for a nominal 15:1 conversion ratio with regulation capability.

Chapter 10: Conclusion

To conclude this thesis, a comparison of hybrid SC topologies is presented. The minimized passive component mass and normalized switch stress are computed which allows for a comparison of different topolgies. The trade-offs for these metrics are discussed, highlighting necessary future work in characterization of losses and converter performance.

Chapter 2

Fundamentals of Hybrid Switched-Capacitor Converters

2.1 Motivation for Hybrid Switched-Capacitor Converters

Passive Component Utilization

Conventional power converters use inductors as the primary energy storage element. For example, the conventional buck converter, shown in Fig. 2.1 is a type of switched-inductor converter which is typically used for step-down conversion. These converters have been historically used due to their uncomplicated control (requiring only one active device in the simplest case) and reliable performance. However, recent advancements in digital control, high-bandgap devices and energy-dense capacitors have opened the possibility for alternative topologies.

Within power converters, the two primary components used for storing and processing energy are capacitors and inductors. While inductors are typically used, commercially available capacitors have the potential for over 1000x higher energy density than inductors [6], as shown in Fig. 2.2. Therefore, motivating the use of capacitors as the primary energy storage element instead of inductors to design compact converters.

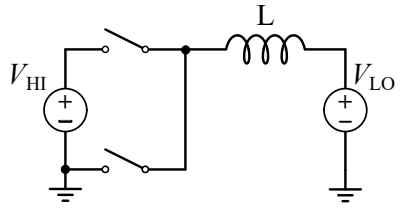

Figure 2.1: Conventional switched-inductor style buck converter.

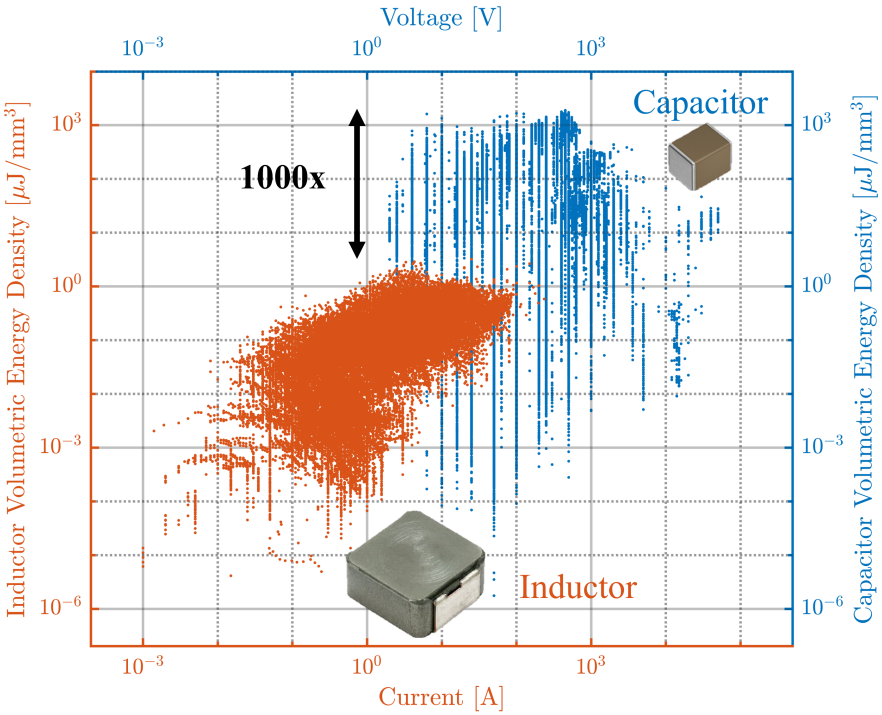

Figure 2.2: Calculated energy density for a survey of commercially available inductors and capacitors [6]. Note, the most energy-dense capacitor has over 1000x higher energy density than the most energy-dense inductor. This difference in component energy density motivates the use of capacitors as the primary energy storage element to design compact converter topologies.

Hybrid switched-capacitor (SC) converters are one family of topologies which use capacitors as the primary energy storage element. The simplest 2-to-1 hybrid SC converter, known commonly as a doubler topology, is shown in Fig. 2.3. The capacitor, C, is known as a flying capacitor as it is not referenced to ground. This flying capacitor is used as the primary energy storage element and the inductor, L, is utilized for filtering and to enable soft-charging of the flying capacitor [7]–[9], thus greatly reducing the required volt-second on the inductor compared to a switched-inductor converter. Note, there are topologies which do not include any inductance. These topologies, pure SC converters, can suffer from large losses due to capacitor charge sharing. Moreover, by adding in the small inductor to a SC converter, the topologies can be operated at-resonance, achieving zero current switching (ZCS), above resonance to reduce converter impedance and component sensitivity and in some cases achieve zero voltage switching (ZVS) and regulation.

In this thesis, two specific converter topologies will be discussed in detail: The flying capacitor multilevel (FCML) converter [10], shown in Fig. 2.4 and the hybrid SC Dickson converter [11], a variant of which is shown in Fig. 2.5.

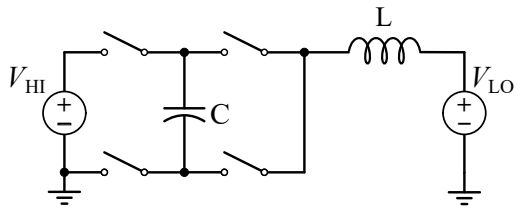

Figure 2.3: A simple 2-to-1 hybrid SC buck converter.

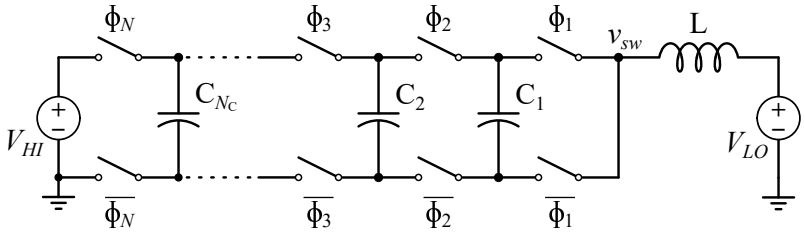

Figure 2.4: An N-level FCML buck converter.

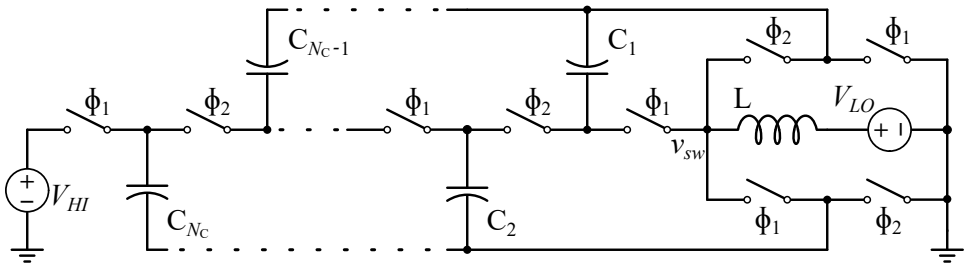

Figure 2.5: An N-level Dickson converter.

Active Component Utilization

As shown in Fig. 2.3, the hybrid SC converter does require additional switches compared to the conventional buck converter. These switches require additional control and advanced gate drive solutions, challenges which will be discussed throughout this thesis. However, in many hybrid SC topologies, the switches only block a fraction of the high-side voltage, instead of the entire high-side voltage, as is the case in the conventional buck converter. This decreased switch stress is due to the flying capacitors which block a portion of the high-side voltage from the switches. As a result, lower voltage switches can be utilized, while still achieving higher voltages at the input/output terminals.

Fig. 2.6 shows a survey of commercially available GaN devices and their blocking voltage versus figure-of-merit. Here the figure-of-merit is defined as the multiplication of the parasitic capacitance (C_{oss}), on-resistance (R_{ds}) and package volume [12]. Therefore, lower figure-of-merit corresponds to lower losses and smaller devices. As shown in Fig. 2.6, the lower

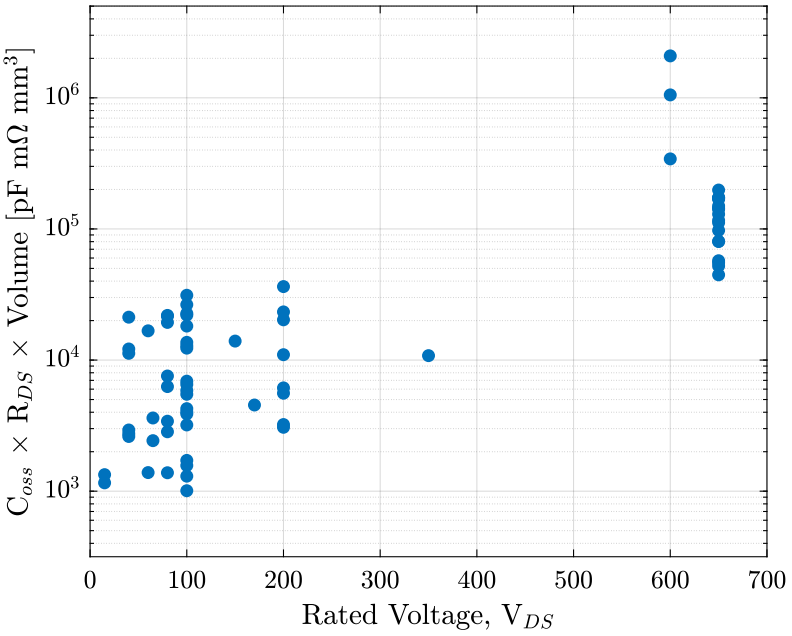

Figure 2.6: A survey of commercially available GaN devices and the corresponding figure-of-merit, where a lower figure-of-merit corresponds to higher performance.

rated voltage devices have significantly lower figure-of-merit compared to higher voltage devices, motivating the use of lower voltage switches to achieve lower losses and smaller converter volume. Across other switch technologies, such as silicon and SiC, the trend of higher performance at lower blocking voltages is also verified [13], [14]. Due to GaN devices demonstrating highest performance at the voltage levels investigated for this thesis (100 V-650 V), GaN is utilized throughout this work. Moreover, as discussed in Chapter 7, GaN devices have higher tolerance to radiation effects [15], making them preferable in space applications.

2.2 Suitability for Aerospace Applications

This thesis focuses on high-performance power converters for aerospace applications. Specifically, Chapters 4-5 demonstrate a design for hybrid electric aircraft and Chapters 7-9 focus on designs with application in space. In both of these applications, light-weight designs are crucial for enabling future technologies.

Designing for minimal mass, opposed to minimal volume, is difficult, since often manufacturers do not include component mass on datasheets. Recent work [6] has provided a model for commercially available capacitors and inductors, to approximate component mass

based on the component's volume (which is typically provided on datasheets). Using this model, Fig. 2.7 shows the comparative specific energy density of commercially available capacitors and inductors. The specific energy density of capacitors is over 10,000x higher than inductors, therefore motivating the use of capacitors in mass critical applications even more than in volume critical applications.

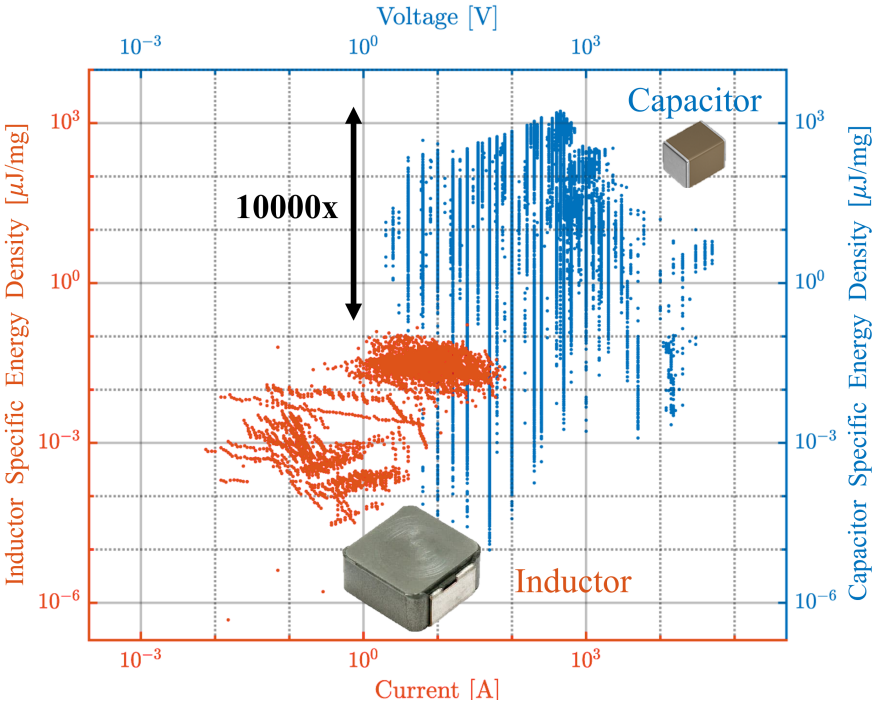

Figure 2.7: Calculated *specific* energy density for a survey of commercially available inductors and capacitors [6]. Note, the most energy-dense capacitor has over 10,000x higher energy density than the most energy dense inductor.

For example, in Chapter 4 the optimization of a converter designed for hybrid electric aircraft is presented. Shown in Fig. 2.8, a 10-level FCML converter, a type of hybrid SC converter shown in Fig. 2.4, results in significantly lower losses and lower mass compared to a conventional switched-inductor boost converter.

There are a number of other specific challenges that exist when designing for aerospace applications. Concerns of reliability, efficiency and resiliency to radiation effects will be discussed throughout the following section and the remainder of this thesis.

2.3 Hybrid Switched-Capacitor Converter Challenges

Hybrid SC converters have gained recent interest due in large part to advancements in devices, both wide-bandgap switches and capacitors. However, there still exist many challenges

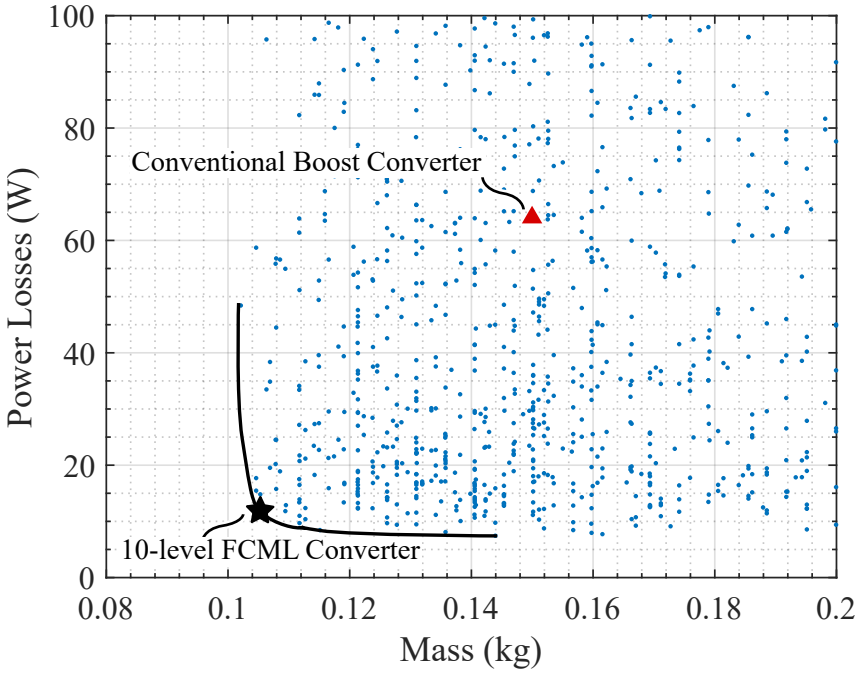

Figure 2.8: Pareto front optimization, where the blue dots represent possible FCML converter designs. The star represents an optimized 10-level FCML converter which minimizes both loss and weight. A conventional boost converter is shown, optimized around the same operating conditions, modeled with 1.2 kV SiC FETs. The design of this FCML converter is described in Chapter 4.

to the implementation of these converter topologies, particularly within aerospace applications. One of the main concerns with hybrid SC converters is the high component count and concerns of reliability [14]. Much of this thesis aims to present high-performance hardware which tackles these challenges, while still achieving high performance. Chapter 5 discusses the concerns of reliability and demonstrates a design which passes low altitude flight qualification, showcasing how careful design and control can be utilized to increase reliability. In addition, the control of high-level count converters is challenging due to the large number of switches, as well as start-up and shutdown operation. As a result, Chapter 4 demonstrates a start-up method while Chapter 6 presents a model which allows designers to consider safe shutdown conditions as part of the initial design. Finally, as more capacitors are utilized in high-performance converters, it is necessary to have more accurate models for the losses of these components under realistic operating conditions, as discussed in Chapter 3.

Chapter 3

Characterization and Modeling of Ceramic Capacitor Losses

3.1 Introduction

Recent work has shown the advantages of using multilayer ceramic capacitors (MLCCs) as the primary energy storage/transfer device in hybrid [16] and resonant switched-capacitor converters [17]–[21]. Reference [22] provides general analytical methods for capturing the passive component volume and power transfer in resonant hybrid switched-capacitor converters, which are helpful to select the most appropriate circuit topologies, but the analysis does not include loss models of the capacitors. Moreover, as shown analytically in [23], and empirically in [24], flying capacitor multi-level converters [10] can achieve significantly higher power density than conventional, two-level designs.

MLCCs are energy-dense and allow for the efficient transfer of energy; however, the performance of these devices is dependent upon a number of operating conditions, making it challenging to accurately capture and model their behavior. To fully capitalize on the potential benefits of MLCCs, it is important to understand and model their energy storage and loss characteristics. Past work [25], [26] has characterized MLCCs under low-frequency (i.e., 50-60 Hz) sinusoidal excitation. Further work in [27], [28] introduced a model for a capacitor's large-signal losses, when operating at sub-kilohertz frequencies. However, little work has been done to characterize and model MLCC losses for high frequency and non-sinusoidal excitation. This work, which extends previous conference papers [29], [30] includes additional high frequency measurements, error analysis and comparisons to low frequency experimental results.

A simple and commonly used MLCC model contains an ideal capacitor, parasitic inductance, and termination and leakage resistance. These two resistances can be effectively combined to equal one equivalent series resistance (ESR) as shown in Fig. 3.1. Furthermore, the losses associated with MLCC operation can then be expressed as shown in Eqn. 3.1.

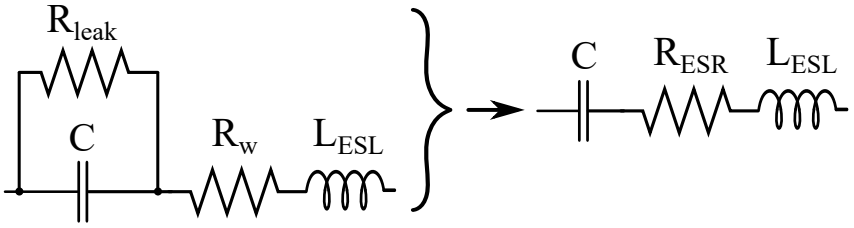

Figure 3.1: Standard capacitor model simplified [31].

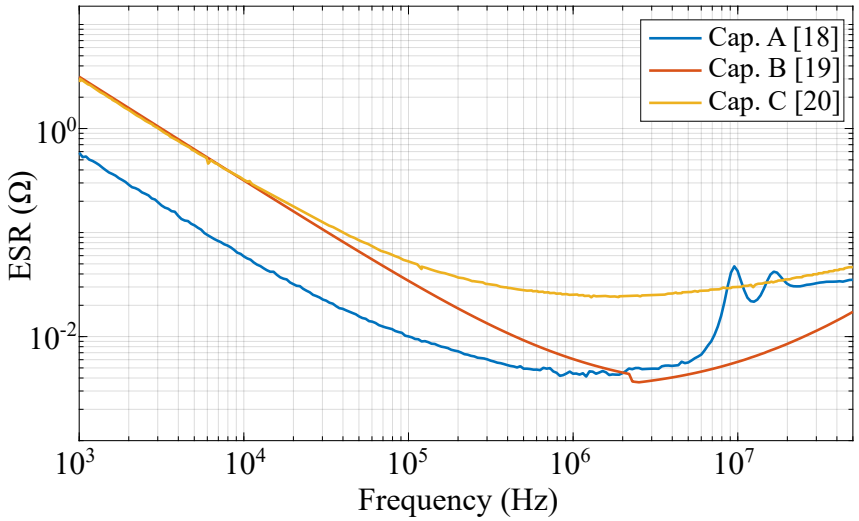

Figure 3.2: Plot of manufacturer-provided ESR of three Class II MLCCs, listed in Table 3.3 over a range of frequencies, at 0 V bias small signal excitation (0.1 V_{rms}) [32] [33] [34].

$$P_{loss} = I_{rms}^2 R_{ESR} \tag{3.1}$$

Typical device data sheets only provide ESR values for small signal sinusoidal excitation at zero or near-zero voltage bias as a function of frequency. Examples of characterizations provided by datasheets are shown in Fig. 3.2. As highlighted through the experimental measurements of this work, small signal loss characterization only captures a small part of the overall losses associated with MLCCs under typical operating conditions. Thus, models based on only small signal characterization can yield highly inaccurate loss estimations. The lack of accurate loss models from the device manufacturers motivate this work, which aims to investigate and characterize how MLCC's parameters change with operating condition. Moreover, it is our hope that the detailed measurement results and analysis will be useful to practicing engineers and researchers that are working on capacitor-based power converters.

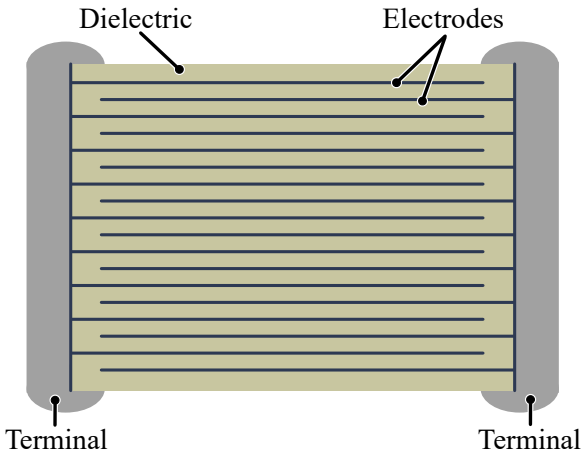

Figure 3.3: Model of MLCC, highlighting the internal structure of interwoven metallic plates and dielectric material resulting in energy-dense capacitors.

The MLCCs achieve high energy density due to the high number of internal layers, as shown in Fig. 3.3. Class I MLCC dielectrics are composed of paraelectric materials which are stable over temperature and voltage bias. The dielectrics of Class II MLCCs are composed of ferroelectric materials which allow for extremely dense energy storage, due to their high permittivity; however, these ferroelectric materials exhibit changes in permittivity due to realignment of electric dipoles within the material. Therefore, while Class I MLCCs have lower energy density than Class II MLCCs, the change in Class II MLCC's permittivity with operating condition results in changes in the capacitance and ESR of the capacitors [35]. The dipole realignment in Class II dielectrics is affected by four main operating conditions: frequency, temperature, dc bias and ac amplitude. Class I devices are stable over temperature and bias. This work focuses on understanding the behavior of commonly used Class II capacitors, while comparing to more stable Class I parameters.

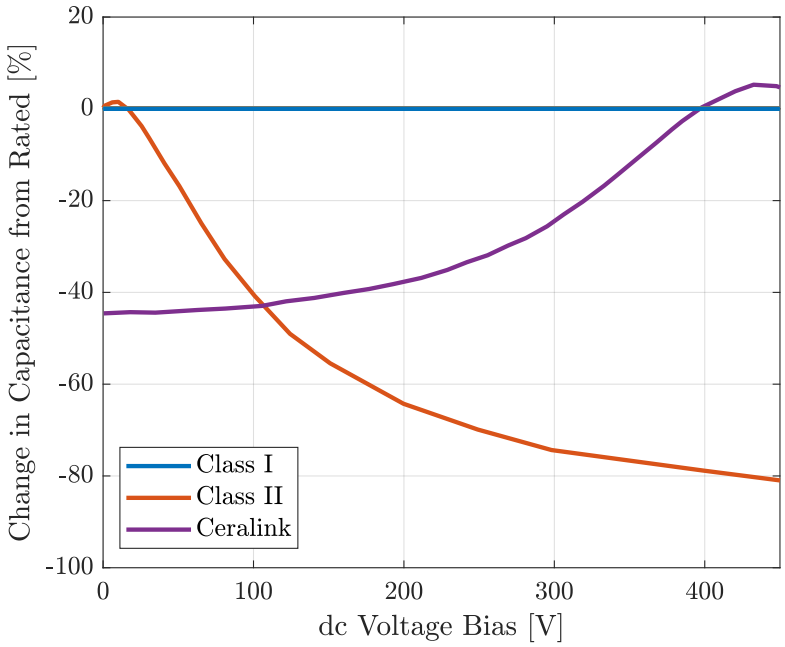

Figure 3.4: Percent change in capacitance over rated dc voltage. From Table 3.3 Cap. E (Class I) has invariant capacitance with dc voltage bias, Cap. A (Class II) de-rates with bias, and Cap. D (Ceralink) has increased capacitance with increased bias.

In addition to Class I and II MLCCs, this work also investigates Ceralink MLCCs [36] which are composed of a PLZT, lead-lanthanum-zirconate-titanate, dielectric. This dielectric is anti-ferroelectric, indicating that as the dc voltage increases the capacitance also increases. This anti-ferroelectric behavior is attractive in hybrid switched-capacitor topologies where high capacitance is often desired under high dc bias. The relative change in capacitance over dc bias voltage is shown in Fig. 3.4.

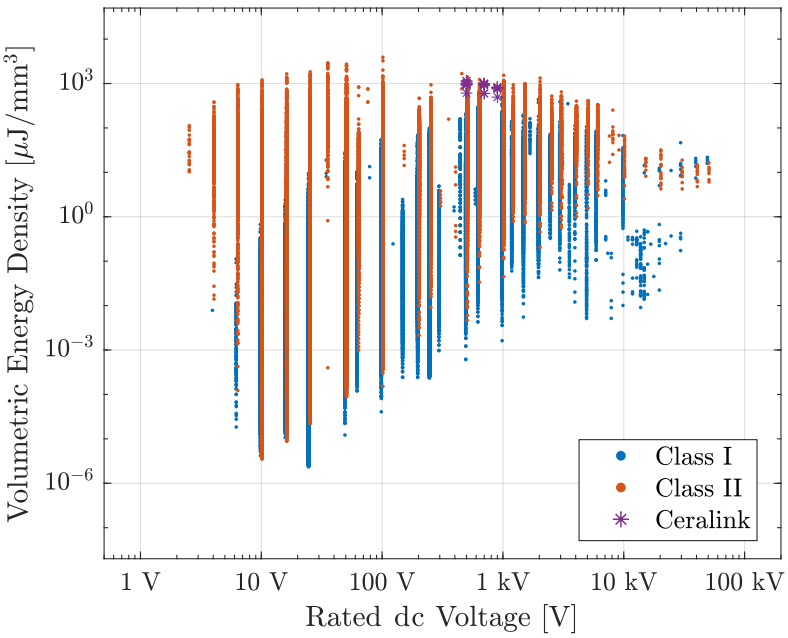

Figure 3.5: Comparison of volumetric energy density of commercially available multilayer ceramic capacitors. Energy density metric includes derating for Class II and Ceralink capacitors.

Shown in Fig. 3.5 is the result of a survey of commercially available Class I, Class II and Ceralink ceramic capacitors [6], which illustrates energy density as a function of blocking voltage for the two technologies. Here, energy density is defined as the maximum energy that can be stored on the capacitor ($1/2\ \mathrm{CV}^2_{rated}$). For this survey, the energy density of Class II MLCCs is calculated using an approximate derating of 60% at rated voltage. As can be seen, at voltages below 1.5 kV, Class II dielectric offers significantly higher energy densities, whereas Class I are more favorable at higher voltages. The Ceralink capacitors have similar volumetric energy densities as Class II MLCCs, however; are only commercially available for limited voltage ratings.

Typical device data sheets only provide ESR values for small-signal sinusoidal excitation at zero or near-zero voltage bias as a function of frequency. However, in many converters these capacitors experience high dc bias voltage and large ripple ac current. One example is the FCML converter [10] as shown in Fig. 3.6-a. In the FCML converter there are $N-2$ flying capacitors which have dc bias voltages equal to $k \cdot V_{out}/(N-1)$, where N is equal to the number of levels and k is the index of the flying capacitor. Example waveforms for an FCML converter operating above resonance with phase-shifted pulse-width modulation (PWM) control is shown in Fig. 3.6-b/c. These waveforms highlight the non-sinusoidal nature of the current and voltage excitations on the capacitors.

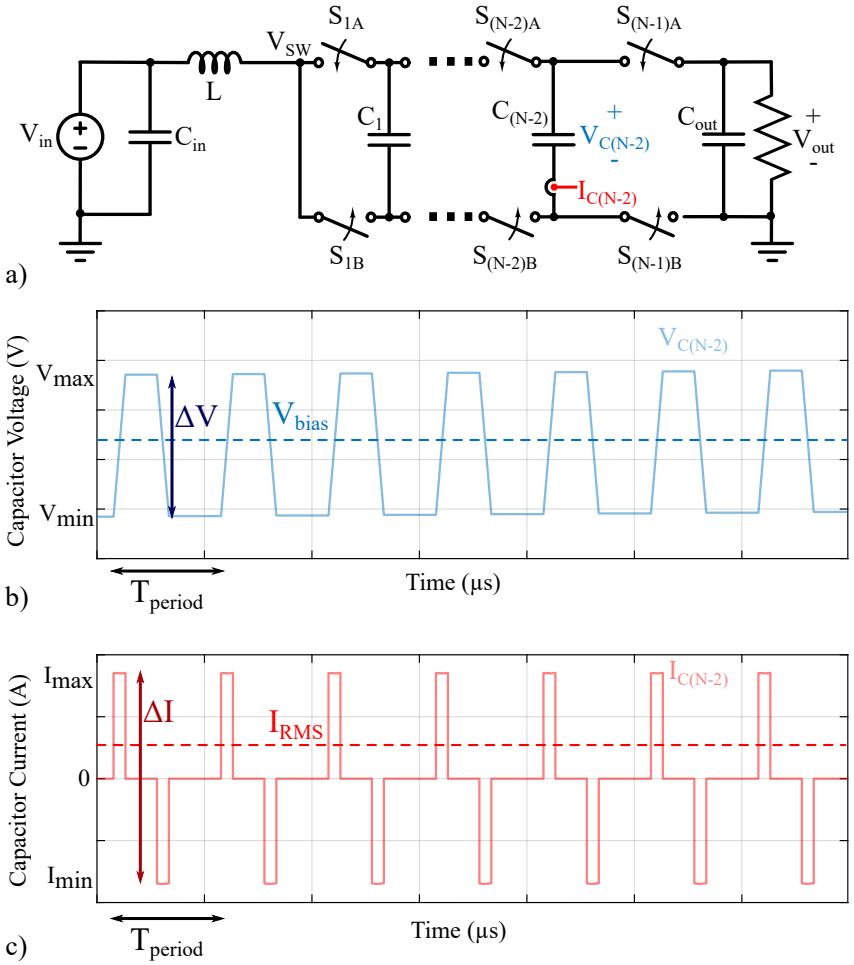

Figure 3.6: Generic N-level FCML boost converter a) schematic, with (b) voltage and (c) current waveforms for a flying capacitor. These waveforms highlight the non-sinusoidal large signal excitations of the MLCC within the circuit.

Table 3.1: Survey of state-of-art FCML converters.

Citation	Type	V_{bias} [V]	ΔV_c [V]	f_{sw} [kHz]
[37]	Datasheet	0	0.28	*all*
[38]	Boost	356	40	50
[39]	Inverter	333	10	30
[40]	Inverter	417	60	120
[41]	Buck	160	50	120

To further illustrate the operation of MLCCs in FCML converters, a survey of state-of-art converters was performed, and the details of the flying capacitors within each converter is shown in Table 3.1. The maximum dc bias voltage and maximum capacitor ripple are approximated based on peak voltage, power and derating characteristics. Moreover, each converter in Table 3.1 utilizes the same flying capacitor [37] due to its high energy density. From this survey, it can be observed that the operating frequencies and capacitor voltage ripple varies in real application, and is in all cases quite different from that of the datasheet ESR measurement conditions.

3.2 Characterization Methodology

The combination of high voltage, current and frequency yields too low of accuracy if traditional electrical loss measurements are employed to attempt to capture capacitor loss. To illustrate these constraints, it is helpful to consider the measurement resolution which can be achieved using a high resolution instrument, such as the WT3000 Yokogawa power analyzer [42]. Considering the conditions for a set of flying capacitors described in the hybrid switched-capacitor converter design in [43], where the MLCC has a voltage bias of 450 V dc and the current excitation of 3 A RMS, the range of measured instantaneous power *transferred* would be approximately one kilowatt. However, the expected measurement of power *loss* for typical values of capacitor ESR would be less than 10 W. Given the accuracy of the power analyzer at frequencies in the hundreds of kHz, an uncertainty on the order of $\pm$10.2 W can be expected. While ac coupled voltage measurements can help reduce the absolute accuracy requirements, electrical measurements remain challenging, owing to the wide frequency range and need for high precision.

Thus, in this work, a calorimetric study is performed to characterize the losses of the MLCCs. Further analysis comparing the accuracy of different measurement techniques can be found in [44]. A custom circuit is designed which applies an excitation representative of flying capacitor operation in hybrid switched-capacitor converters and allows for adjustable dc bias voltage, ac current amplitude and varying frequency. An ideal version of this circuit is shown in Fig. 3.7-a, where a voltage source V_{bias} controls the dc bias voltage and an ideal current source, shown as I_{ideal}, controls the amplitude of the current excitation. The current source is then converted into a square-waveform using an H-bridge which can be controlled to vary the frequency of the excitation. For practical implementation, the circuit shown in Fig. 3.7-b approximates the operation of the ideal circuit closely. The dc bias is adjusted through V_{bias} which is connected to a large capacitance (100x the capacitance of the DUT) allowing a stiff dc bias while still allowing the voltage ripple of the DUT. The ac current amplitude of the DUT excitation is varied by adjusting the current limit of the V_{bridge} supply, which operates in constant current mode and is placed in series with a large inductor, approximating the ideal constant current source. Finally, the frequency of the excitation can be easily adjusted by a micro-controller which can change the frequency of the gate drive signals to the H-bridge. The ability to easily adjust frequency, ac amplitude

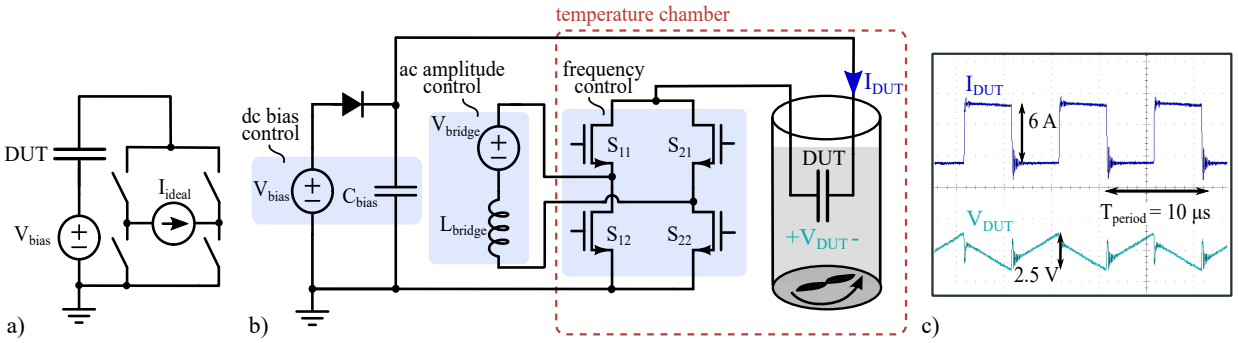

Figure 3.7: a) Ideal circuit which allows for varying dc bias voltage, and varying ac current amplitude with an ideal current source and h-bridge. b) Electrical excitation circuit used to replicate hybrid switched-capacitor operation with adjustable frequency, dc bias and ac amplitude. Portions of the electrical excitation are placed within the temperature chamber to decrease the inductance in the path to the DUT. c) Example capacitor excitations created by the electrical excitation circuit.

and dc bias allows several operating conditions of interest to be studied using the same setup and PCB. The electrical components used in the electrical excitation circuit can be seen in Table 3.2.

Table 3.2: Components used in electrical excitation circuit and calorimetric setup.

Electrical Setup	
Label	Instrument
Switches	GaN Systems GS61008T
Gate Driver/Isolator	SI8275GB-IS1
V_{bias}	Magna-Power dc supply
V_{bridge}	HP 6623A dc supply
L_{bridge}	1 mH Inductor
Microcontroller	TI C2000
Calorimetric Setup	
Temperature Chamber	TPS Tenney TJR-A-WF4
Data Recording	Fluke Hydra Data Bucket
Magnetic Stirrer	INTLLAB MS-500
RTDs	TE Connectivity [45]

In this calorimetric setup, the DUT is placed in an oil bath directly under the PCB. Careful consideration of DUT placement is necessary as to not add parasitic inductance which would change the shape of the excitation waveform. Furthermore, the DUT is attached to

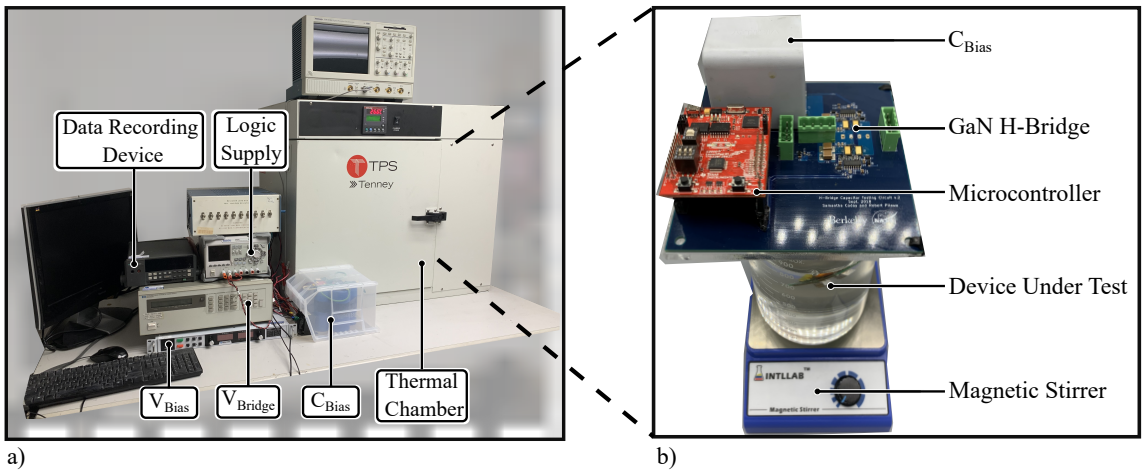

Figure 3.8: a) Equipment setup developed to generate electrical excitation, as well as log temperature data. b) The electrical excitation circuit board and other calorimetric components located within the temperature-controlled chamber.

the PCB using copper strips to decrease the parasitic inductance. The temperature rise of the oil is used to calculate the power dissipation of the DUT [46]. Resistive temperature devices (RTDs) [45] are chosen for this study due to their improved accuracy for temperature measurements over a small temperature range as opposed to thermo-couples. The temperature of the oil and chamber are both measured every five seconds using a Fluke Hydra DAC controlled through custom LabVIEW and MATLAB software. To provide even heat distribution within the oil bath, the beaker is stirred using a magnetic stirring apparatus. A listing of the instrumentation used in the calorimetric setup is provided in Table 3.2, and the setup is shown in Fig. 3.8.

Eqn. 3.2 relates the temperature rise of the oil bath and the power dissipated by the DUT [46].

$$\mathrm{P_{diss}} = \frac{1}{\tau}[k_{oil}\Delta \mathrm{T_{oil}} + \int_0^{\tau} \frac{\mathrm{T}_{oil} - \mathrm{T}_{amb}}{R_{TH}} dt] \tag{3.2}$$

Here τ is the time for which the temperature is observed and T is the temperature measured. The oil bath is characterized by k_{oil} which is the product of the specific heat ($\frac{J}{g \cdot K}$), density ($\frac{g}{cm^3}$) and volume of oil used (mL). The parameter k_{oil} determines how quickly the temperature of the oil rises as convection occurs between the oil and DUT. Parameter R_{TH} ($\frac{K}{W}$) is the thermal impedance between the oil and the ambient environment and can be determined experimentally with a calibration procedure.

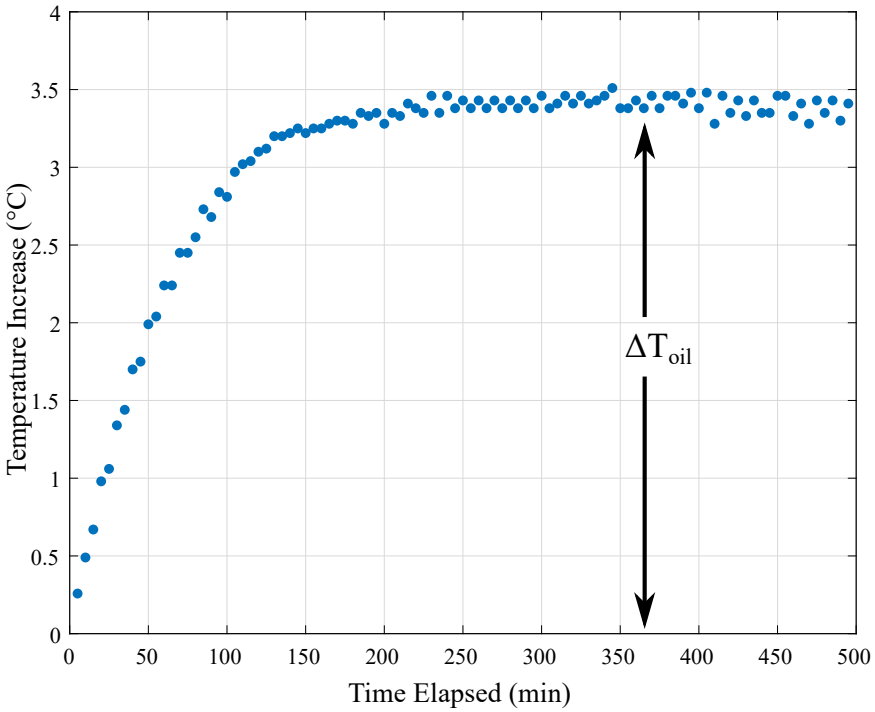

Figure 3.9: Calibration test results, showing temperature measured over eight hours of testing to ensure thermal equilibrium.

Calibration of Setup

The thermal impedance of the setup, R_{TH}, is determined over a series of calibration tests. During calibration, the DUT is replaced with a high-precision, 3.1 mΩ resistor, whose value is chosen to dissipate approximately the same amount of power as expected by the MLCCs under test. Several calibration tests are performed at dc operating conditions to increase the accuracy of the electrically measured power dissipation. The current and voltage of the DUT is measured through Kelvin sensing to accurately determine the power dissipation. The calibration is run in the calorimetric test chamber multiple times, with power levels comparable to those used during capacitor testing. In each calibration test, the temperature of the oil is allowed to reach steady-state, as shown in the example of recorded oil temperatures during a calibration test in Fig. 3.9.

Calorimetric Testing Procedure

For each calorimetric test, the circuit is assembled and placed inside the temperature chamber. Three RTDs are placed inside the temperature chamber and three inside the beaker of oil, after which the temperature chamber is sealed and set to a constant twenty-three degrees

Celsius. This temperature is chosen to match the ambient temperature of the lab and the temperature chamber is used to eliminate variations in ambient temperature which occur over the course of the day due to building heating and cooling schedules. At the beginning of each test the chamber is turned on and allowed to reach thermal equilibrium. Once the inside temperature of the chamber is stable the dc bias and ac excitation are applied to the DUT. The temperature of the thermistor is collected every five seconds, and each calorimetric test is performed for approximately one hour to ensure that sufficient data is collected to extract a high confidence measurement. Additional time is allowed between each test to allow the system to return to the ambient temperature. After the test is complete the temperature data is used to calculate the power dissipated by the DUT, using Eqn. 2. Then the effective ESR is calculated by dividing the power by the squared RMS current. For each measured capacitor, this process repeats for five dc voltage bias points: [0 V, 100 V, 200 V, 300 V, 400 V], and for a span of fundamental switching frequencies. The dc voltage bias points are chosen to span the voltage rating of the lowest rated capacitor and the switching frequencies are chosen to represent typical operation of a hybrid switched-capacitor converter.

Table 3.3: Experimentally evaluated capacitors.

Label	Type	Manufacturer	Voltage	Capacitance	Part Number
A	X6S	TDK	450 V	2.2 μF	C5750X6S2W225K[37]
B	X7R	Knowles	630 V	1.0 μF	2220Y6300105KETWS2 [33]
C	X7R	KEMET	500 V	1.0 μF	C2220C105MCR2L [47]
D	Ceralink	EPCOS	500 V	1.0 μF	B58031U5105M062 [36]
E	C0G	TDK	630 V	0.1 μF	C5750C0G2J104J280KC [37]

3.3 Calorimetric Results

Table 3.3 provides details of the five different MLCCs evaluated in this study. Three Class II MLCCs are chosen due to their high energy density: one with X6S and two with X7R temperature characteristics. A Ceralink (PLZT) MLCC is selected for its high energy density at rated voltage, and for evaluation of the anti-ferroelectric dieletric compared to the ferroelectric dielectric of Class II capacitors. Lastly, a Class I MLCC is selected as the losses are predictably stable over voltage bias, due to their stable paraelectric dielectric. The Class I MLCC thus also serves as a good control capacitor.

It is important to note that the results of this study are not intended to show a direct comparison of performance between capacitors. As can be seen in Table 3.3, the MLCCs tested have varying temperature characteristics, voltage rating and capacitance, and therefore would be suitable for different applications. They are deliberately chosen for this study to capture experimental measurements across a wide range of devices.

Measurement Accuracy

For all data shown in the following sections, error bars indicate the accuracy of each measurement. The error analysis is performed with consideration of the accuracy of RTDs and the calibration method. The effect of temperature on ESR is another accuracy concern, especially as the current amplitude is varied between different tests; therefore increasing the expected temperature rise. Often, MLCC datasheets list the relationship between temperature and ESR [37]. While the ESR is shown to vary widely for temperatures less than zero degrees Celsius, or greater than fifty degrees Celsius, the ESR is relatively stable around twenty-three degrees Celsius which is the ambient temperature of the thermal chamber for all tests. Specifically the ESR variance for Cap. A is only $\pm 2\%$ even with $\pm\ 10°C$. In this work the maximum temperature observed on the DUT is $30°C$, which results in a maximum ESR deviation of 1.5%. Therefore the effect of device temperature on the measurement is not considered in this work.

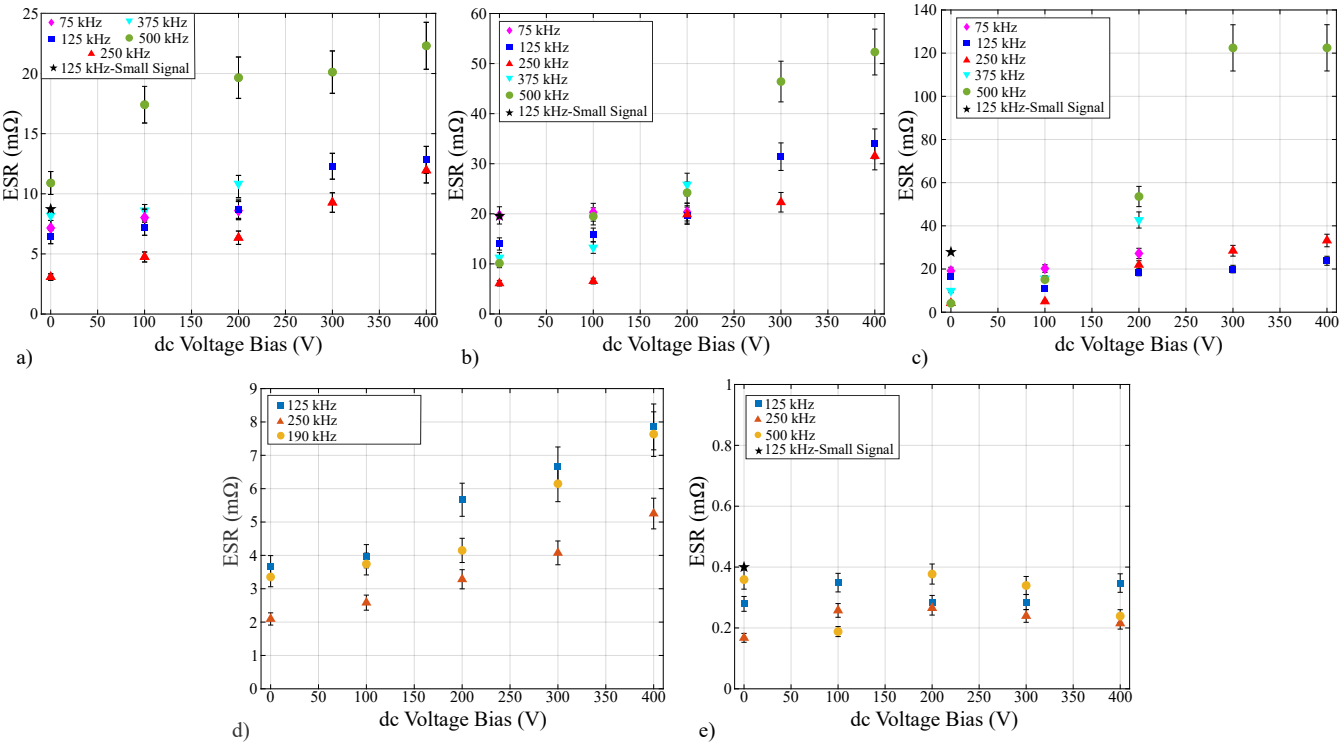

Figure 3.10: The relationship between dc voltage bias and calorimetrically measured ESR for a) Cap. A, b) Cap. B, c) Cap. C, d) Cap. D, and e) Cap. E from Table 3.3. The black star represents the small signal ESR from the data sheet [37]. As expected, compared to Class II dielectric capacitors which exhibit increased ESR with voltage bias, the ESR of this Class I (C0G) capacitor remains relatively invariant to voltage bias.

Effect of dc bias on Class II MLCCs

The impact of dc voltage bias on the MLCC losses is investigated by keeping the current amplitude constant at 6 A peak-to-peak, and then varying the dc voltage of the capacitor. For each capacitor, three to five different frequencies are evaluated at five different voltage biases, to understand the relationship between the frequency and dc voltage effect on losses. Note, for each capacitor the different frequencies tested are chosen to avoid the capacitor's self-resonance frequency. The measured power loss is then used to calculate a corresponding ESR using Eqn. 3.2. The results of the calorimetric testing for the three Class II MLCCs can be seen in Fig. 3.10-a,b,c.

These results show a linear relationship between the dc bias and ESR over a wide range of frequencies. However, between different capacitors and measured frequencies the rate of increase of ESR with dc bias varies. The observed relationship between ESR and frequency is non-linear. Since the excitation is a square-waveform the impact of the subsequent high-order odd harmonics impact the ESR. In particular, as the higher-order harmonics exceed the capacitor's self-resonance frequency the losses increase substantially.

Effect of dc bias on non-Class II MLCCs

Cap. D is evaluated to determine if the observed ESR and bias relationship is similar for PLZT dielectrics. Fig. 3.10-d shows the impact of dc bias on ESR for Cap. D. The relationship is approximately linear, displaying the same trend at each measured frequency. This result aligns well with previously published results for low-frequency, sinusoidal excitation [25]. However, while previous work [25] identified the losses of the PLZT dielectrics to be much greater than Class II MLCCs operating at twice-line frequencies, these results show similar ESR to that of Class II MLCCs with similar voltage ratings. Therefore, this motivates the use of these devices in higher frequency applications.

Moreover, Class I MLCCs are investigated to determine if the similar increase in ESR with dc bias is observed. The measured results for Cap. E from Table 3.3 as seen in Fig. 3.10-e show that the Class I MLCC does not have the same increase in ESR when the dc bias is increased. Due to their stability over operating conditions, the Class I MLCCs can be simply modeled by the zero-bias small-signal ESR from datasheets.

Effect of ac amplitude on Class II MLCCs

Further calorimetric tests are performed to study the effect of ac current amplitude on losses. It is found that as the current amplitude changes the ESR stays relatively constant, as shown in Fig. 3.11. This relationship is confirmed over a variety of dc voltage biases.

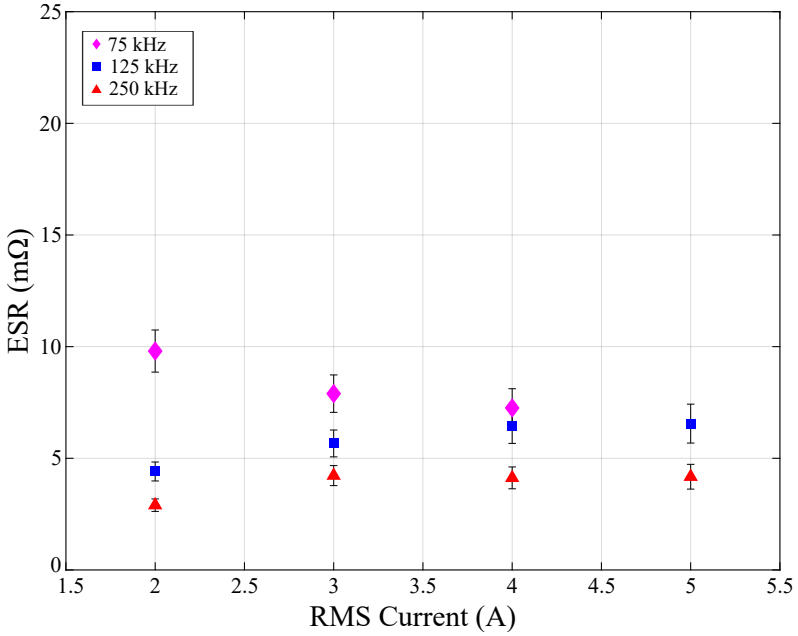

Figure 3.11: The relationship between ac current amplitude and calorimetrically measured ESR with zero volts dc bias for Cap. A from Table 3.3. The y-axis scale is purposefully set to the same scale as Fig. 3.10-a to show that the dc voltage bias has a much larger affect on losses compared to the effect of ac current amplitude.

3.4 Comparison to Low Frequency Electrical Measurements

To further validate the calorimetrically calculated losses and ESR, the results are compared to capacitor losses measured at low frequency using electrical measurements. As discussed in Section II, an electrical evaluation is not employed for the high frequency loss measurements in this work due to the measurement accuracy requirements. However, at a lower frequency the simpler electrical characterizations have sufficient accuracy for comparison and validation.

In [26] a methodology for testing capacitors in buffering applications was introduced. This same setup, shown in Fig. 3.12, is implemented to test the capacitors over a range of sinusoidal frequency excitations, 120 Hz to 500 Hz. The necessary equipment for this setup can be seen in Table 3.4. Using the Yokogawa WT3000 power analyzer, the power dissipated by the DUT is measured and the ESR is computed by dividing by the square of the RMS current. Finally, the dc bias is adjusted by changing V_{dc}.

The results for low frequency measurements for Cap. A in Table 3.3 are summarized in Fig. 3.13. These results verify that even at a low frequency, the ESR generally increases with

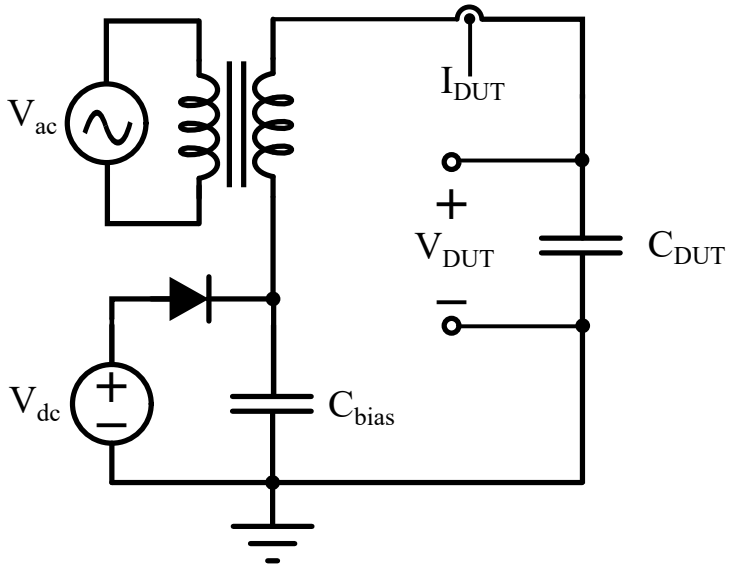

Figure 3.12: Low frequency electrical measurement capacitor testing circuit.

Table 3.4: Devices used in low frequency electrical setup.

Label	Instrument
V_{dc}	Magna-Power Electronics DC Supply
I_{DUT} and V_{DUT}	Yokogawa WT3000 Power Analyzer
V_{ac}	Pacific Smart Source 112-AMX
Transformer	Schneider Electric Cat. No: 151F

applied dc voltage bias. Also, as the frequency is doubled from 250 Hz to 500 Hz, the ESR is approximately halved. This trend matches the small-signal ESR data in Fig. 3.2 where at low frequencies the ESR decreases approximately linearly with frequency. Additionally, at zero-bias the measured ESR at low frequencies is significantly higher than the high frequency calorimetric measurements which matches the expected trends in the small-signal ESR data of Fig. 3.2.

3.5 Capacitor Loss Model from Measured and Datasheet Values

As calorimetric loss measurements are cumbersome and time-consuming, it is highly desirable to obtain simple, yet accurate loss models that can be obtained from datasheet parameters. Thus, to aid practicing engineers in capacitor loss estimation, we present an ESR model

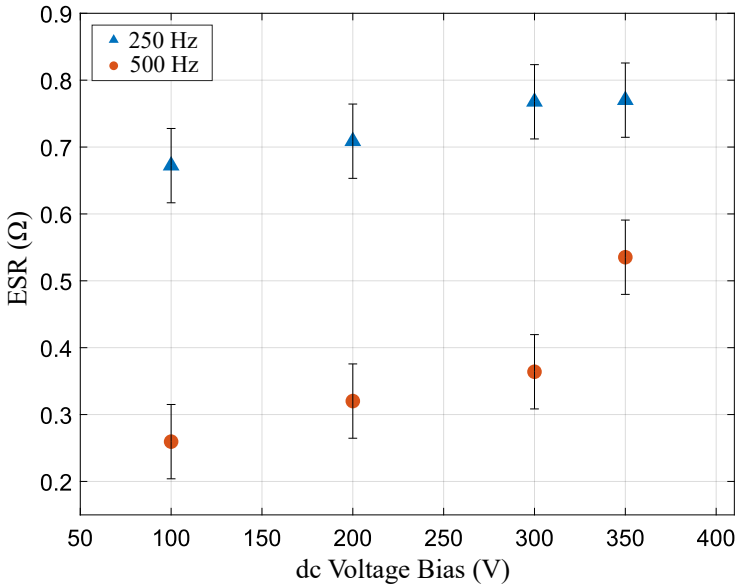

Figure 3.13: Low frequency bias dependent ESR results, for Cap A in Table 3.3, attained through electrical experimental setup.

linearly related to dc bias voltage with increased accuracy over a zero-bias small-signal approximation. The proposed model takes into account the dominant influences on loss—dc voltage bias and frequency. In the tests where capacitor current ac magnitude varies, no appreciable change in ESR is observed.

Due to the non-linear nature of the capacitor losses, and the fact that square-wave excitation (with many harmonics) is employed in this work, the dependence of ESR on frequency yields highly non-linear results. It is the hope of the authors that the preliminary results obtained in this work will stimulate further efforts to develop accurate, yet simple, loss models for ceramic capacitors under realistic large signal conditions.

Constant ESR Approximation

The simplest and most commonly used model for ESR can be found directly from most manufacturer's datasheets. Fig. 3.2 shows the frequency and ESR relationship from three datasheets, for Cap. A, B, & C of this work. Since manufacturer's datasheet provide no information regarding the relationship between dc bias and ESR, a reasonable assumption by a power electronics designer is thus that this ESR remains constant across all operating dc voltage biases.

While simple, this method provides high error when used at high dc voltage operating conditions. For this work, the excitation frequency varied from 75 kHz to 500 kHz range. For this region of interest the small signal ESR provided by the manufacturer is non-linear,

as shown in Fig. 3.2. Moreover, this only showcases the small signal losses for the fundamental frequency, since the excitation of interest is a square waveform, there are higher-order harmonics present which will affect the overall losses.

Linear Model

A simple model can be leveraged from the linear relationship between dc voltage bias and ESR and is empirically described by Eqn. 3.3.

$$R_{ESR}(V) = R_0 + k\frac{V}{V_{max}} \tag{3.3}$$

Here, R_0 is the ESR at zero voltage bias, and V_{max} is the maximum rated dc voltage of the capacitor. The slope of the line, parameter k, can be determined by testing two dc voltage biases. Moreover for simplicity, one point at zero bias can be approximated from a small-signal ESR measurement or a datasheet, therefore only one additional measured data point is necessary to determine the coefficient for the linear model.

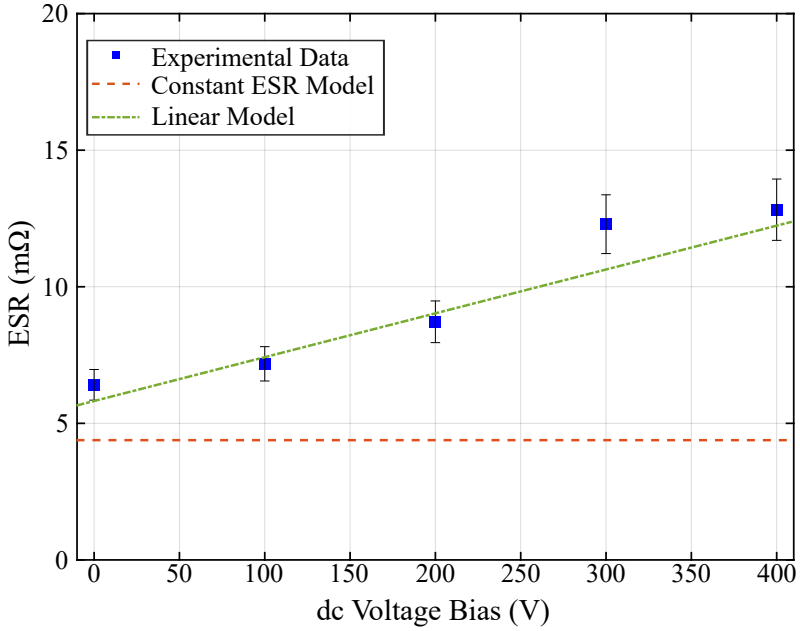

Figure 3.14: The relationship between dc voltage bias and calorimetrically measured ESR, at 125 kHz, for Cap. A from Table 3.3. The proposed linear model is shown. The constant ESR approximation is found from [37].

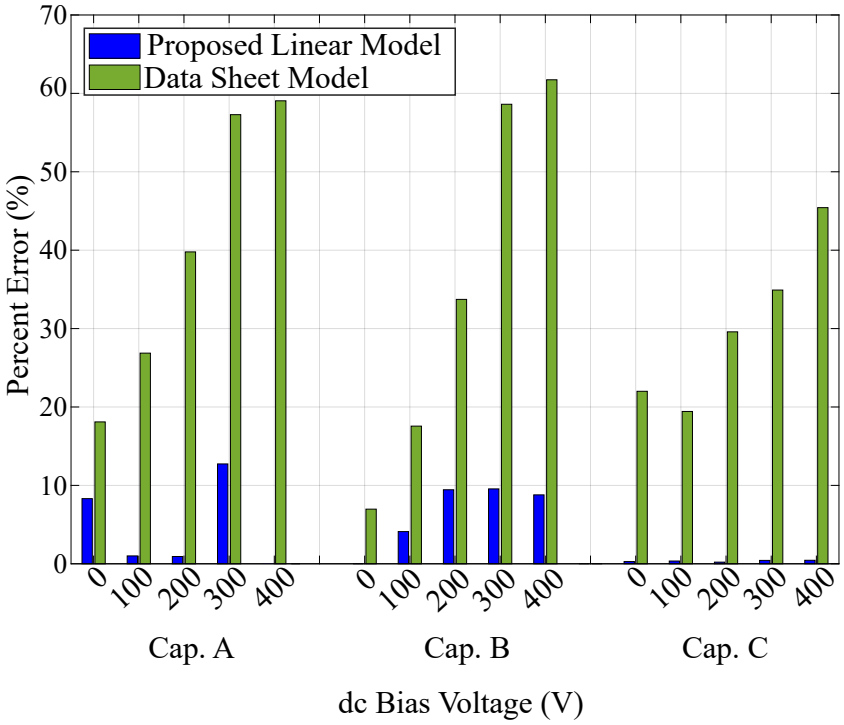

Figure 3.15: The error for the three presented models shown for Cap. A, B and C tested at 125 kHz.

Model Comparison

Fig. 3.14 shows the proposed model for Cap A, at 125 kHz. Fig. 3.15 shows the relationship between the error of each model and the dc voltage bias for the same data as shown in Fig. 3.14. Fig. 3.15 highlights that the constant ESR model underestimates losses at higher voltages by as much as 60% in these cases. The linear model matches the data more closely, but would require designers to collect one additional calorimetrically measured data point in addition to values found on datasheets. The model error for Cap. A, B, & C is shown in Fig. 3.15. Finally, if more data points are measured, a better higher-order fit can be obtained, at the cost of additional experimental measurements and mathematical complexity. Reference [44] provides one such model.

3.6 Conclusion

This work has provided a method for accurately characterizing the losses of MLCCs used in hybrid switched-capacitor power converters. A calorimetric method for accurately determining the ESR over a range of operating conditions has been presented. The results of this

calorimetric study are discussed, with an analysis of the relationship between losses and dc voltage bias, ac current amplitude and frequency. These results can be applied in the future when designing hybrid switched-capacitor power converters to better understand capacitor losses, and eventually can be used to find strategies to mitigate these losses.

Chapter 4

Flying Capacitor Multilevel Converter for Hybrid Electric Aircraft

4.1 Motivation

Hybrid electric, and eventually fully electric, aircraft offer promising advances in decreased emissions, acoustic noise and fuel consumption [3]. To enable electrified aircraft, recent proposals suggest an increase in specific power density of the drivetrain to a target of 25 kW/kg [4]. There are many promising inverters that are approaching this target power density, however most inverters have the highest power density and efficiency with a fixed high dc bus voltage [48]. Moreover, many emerging electric aircraft designs rely on batteries which vary significantly in voltage during flight and with different configurations [49]. Therefore, to allow a wide variety of battery technologies, configurations, and voltages, an intermediate boost regulation stage is proposed, as shown in Fig. 4.1. The bi-directional dc-dc step-up converter also enables low-loss high voltage dc distribution through the aircraft without imposing challenging high-voltage ratings on the battery pack and its enclosure. The proposed architecture also enables incorporation of other energy sources, such as fuel cells, which have different voltages than the battery systems on board [50]. As the boost converter is an additional stage in the system, it is imperative that its specific power density and efficiency is high, therefore enabling the full drivetrain to meet the overall power density targets.

The FCML converter [10] has been shown to have high power density and low losses while exhibiting a very large input or output voltage range in step-up or step-down applications respectively. While the FCML converter has been demonstrated to have high performance, the large number of active and passive devices, as well as the added complexity of start-up and shutdown, have led to concerns about system reliability [39]. This work addresses the concerns of reliability in a ten-level FCML converter through careful design strategies, including innovative low-inductance and high voltage PCB layout, robust control methods and new start-up/shutdown circuitry. Moreover, to demonstrate the resiliency of the suggested design, Chapter 5 demonstrates flight qualification through successful thermal, shock and

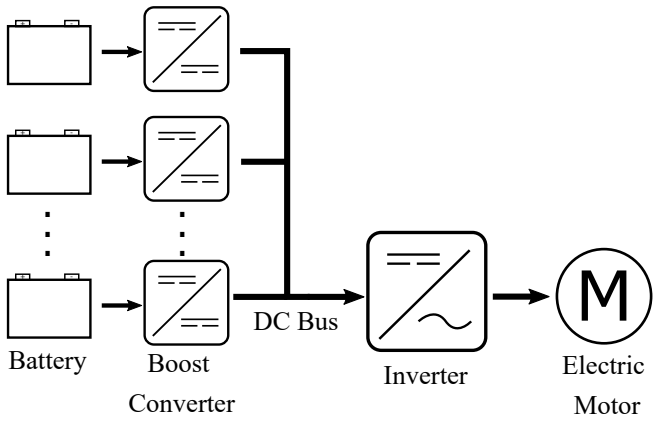

Figure 4.1: Proposed electric aircraft system architecture. This work focuses on the design and implementation of the dc-dc boost converter.

vibration testing that meets the DO-160G standards for low altitude fixed wing aircraft [51].

The contribution's of this work are presented alongside the contributions of prior work, to holistically depict the design aspects and steps necessary to bring a high complexity converter design through to feasible aircraft implementation; a novel application for multilevel topologies. As such, this work is a demonstration that showcases the capability of multilevel designs to meet industry regulatory standards while delivering exceptional performance.

4.2 FCML Converter Design

In this work, the design specifications were chosen to match a small two passenger hybrid electric aircraft, with a battery voltage ranging from 500 V to 750 V with a 750 V dc bus. While the full system requires higher power, this design was optimized for 2.5 kW as an initial prototype to demonstrate flight readiness. The selected power level was also determined by the condition that for flight testing, a resistive load was to be employed, with associated weight and thermal restrictions in the aircraft environment. Moreover, as efficiency and specific power density are used to measure the design's perform. One approach that has been demonstrated in the literature is to compose a system of sub-phases [14], [52] to provide a modular approach that can scale, while potentially facilitating redundancy, phase shedding, and dynamic optimization for a given power level.

The FCML converter is particularly well suited for aerospace applications; the converter offers regulation capability and overall passive volume is greatly reduced compared to a conventional boost converter [22]. This reduction in passive volume is largely due to the increased effective frequency seen by the inductor, which also has the potential to decrease necessary filtering requirements to meet EMI compliance. Moreover, the heat distribution of the FCML converter allows for simple cooling and therefore a robust design [53]. The

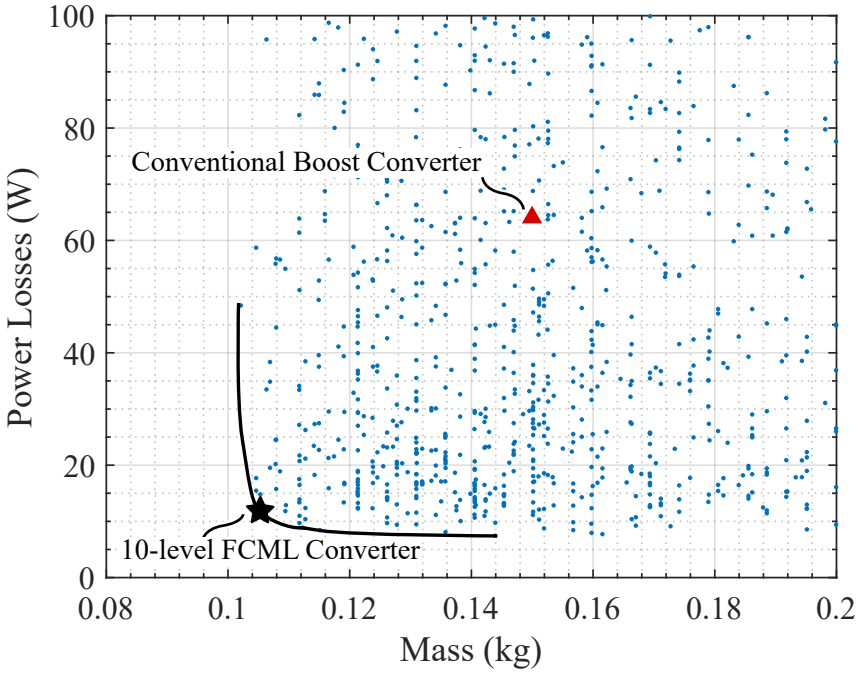

Figure 4.2: Pareto front optimization, utilizing loss model presented in [40]. The star represents the selected design, which minimizes both loss and weight. A conventional boost converter is shown, optimized around the same operating conditions, modeled with 1.2 kV SiC FETs.

following subsection details the design procedure used to optimize the FCML converter for this application.

FCML Level Count Selection

For the FCML boost converter, the steady-state (assuming small capacitor voltage ripple) drain-source voltage (V_{ds}) is given by $\frac{V_{out}}{N-1}$, where N is the number of levels. There are a number of trade-offs to consider when optimizing the level count and component selection of an FCML converter. For example, with higher level counts, lower voltage switches can be used which tend to have better figures-of-merit [12], [14], [54]. However, using many lower voltage switches instead of fewer high voltage switches results in increased system complexity. Moreover, the volt-seconds applied to the inductor (and therefore, approximately its size), decrease as a function of $\frac{1}{(N-1)^2}$, so for higher level counts the weight of the magnetics can be greatly decreased. Since the trade-offs surrounding the level count selection involves a large number of design parameters, a pareto-front optimization was developed which calculates approximate loss and weight based on a set of possible components and operating parameters. This work utilizes the pareto-front optimization introduced in [40] resulting in the design

space. For the plot of Fig. 4.2, the number of levels was varied between 4 and 12, switching frequency between 10 kHz and 500 kHz, with component voltage, current, and loss ratings checked, and only designs meeting the design objectives and all component ratings plotted. In Fig. 4.2, the star represents the selected design: a 10-level FCML, the schematic for which is shown in Fig. 4.3. For reference, a conventional boost converter is also shown in Fig. 4.2. This boost converter was optimized around the same operating specifications, but requires higher voltage switches, 1.2 kV SiC, and a significantly larger inductor to meet the same ripple specifications, highlighting the benefits of multilevel designs.

For the ten-level design proposed in this work, each switch is exposed to a maximum voltage of $V_{out}/9$, with some additional voltage stress due to overshoot and flying capacitor ripple. As detailed in [55], the reliability of GaNFET devices is higher with lower switch stress. As a result, this design utilizes 200 V devices (EPC2034C), which for the nominal output voltage of 750 V yields a switch stress of 83 V, and a correspondingly conservative de-rating of each switch. The devices will remain well under half their rated voltage, even when accounting for switch commutation overshoot and flying capacitor voltage ripple. This conservative de-rating was chosen as reliability reports have shown improved time to failure (TTF) and probability of failure when the GaNFETs operate at lower drain-to-source voltage stress [55].

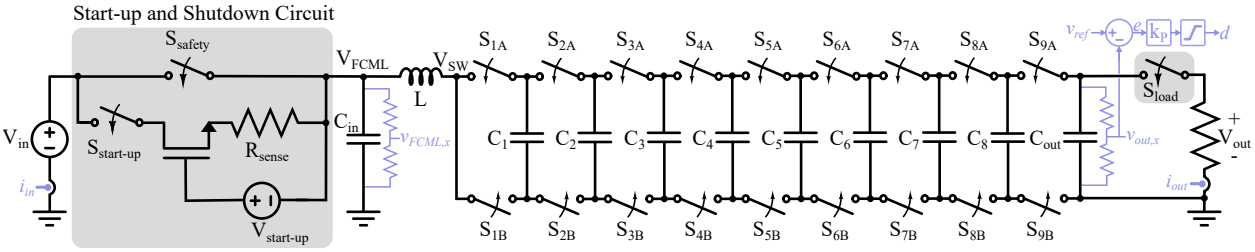

Figure 4.3: Ten-level FCML converter, highlighting the necessary start-up and shutdown auxiliary circuits. The relevant control sensing circuitry and diagram are also shown.

Gate Drive

Owing to the large number of non-ground-referenced power switches, gate drive power delivery is a challenge in the FCML converter. A number of gate drive power delivery techniques are presented and analyzed in [56], and more recent techniques with improved performance are presented in [57]. A limitation of the cascaded bootstrap technique is the accumulating voltage drops of the bootstrap diodes. In this work, diodes with minimal forward voltage drop were chosen to reduce this effect while local linear regulators provide a stable 5 V supply to each gate driver. Nevertheless, at extreme duty ratios the gate drive power supply voltage may fall below the 5 V limit of the devices employed here. To ensure sufficient headroom and reliable operation, the duty cycle range for this work is limited to 0.07-0.93.

Flying Capacitor	Nominal DC Voltage	Capacitor Configuration	Total No. Capacitors	Nominal Capacitance	De-rated Capacitance
C_1	111 V	3 in parallel	3	6.6 μF	3.96 μF
C_2	222 V	3 in parallel	3	6.6 μF	2.64 μF
C_3	333 V	3 in parallel	3	6.6 μF	1.98 μF
C_4	444 V	3 in parallel	3	6.6 μF	1.32 μF
C_5	555 V	2 in series + 5 in parallel	10	5.5 μF	1.65 μF
C_6	666 V	2 in series + 5 in parallel	10	5.5 μF	1.38 μF
C_7	777 V	2 in series + 5 in parallel	10	5.5 μF	1.20 μF
C_8	888 V	2 in series + 5 in parallel	10	5.5 μF	1.10 μF

Table 4.1: Flying capacitor design specifications.

Flying Capacitor Design

To maximize specific power density targets for this high-voltage design, careful capacitor sizing, selection, and implementation are all critical design aspects. In an FCML converter, the average voltage across a flying capacitor is determined by $V_{k,fly} = k * \frac{V_{out}}{(N-1)}$, where k is the number of the corresponding level (numbered as shown in Fig. 4.3 for the boost topology). Class II MLCCs were utilized due to their high volumetric energy density and low losses [27] [30]. Moreover, recent work [6] has shown that these devices also have higher specific energy densities, further validating their use in weight-critical applications. The selected capacitors (C5750X6S2W225K) were shown to have the highest specific energy density of all surveyed MLCCs, motivating their selection in this work. While previously, mass data for capacitors was difficult to acquire, recent work [6] has presented a model for relating mass and volume for different capacitor technologies. Therefore, future optimization strategies can use this model to also select capacitors for minimum converter weight. Future work may instead optimize the design for capacitors selected for increased reliability, such as soft-termination or capacitors with metal frames to reduce mechanical stress [58]. The devices selected for this work are only rated for 450 V, requiring that flying capacitors C_5-C_8 are stacked in series to adhere to component voltage ratings. Additional balancing resistors of 2 MΩ are added to

ensure even voltage division between series stacked capacitors. These additional balancing resistors also add a discharge path in case of a fault during operation. The corresponding schematic for the capacitor and balancing resistor implementation is shown in Fig. 4.5.

Capacitor Balancing

Flying capacitor imbalance occurs when the capacitor voltages deviate from their nominal steady-state dc biases. Capacitor balancing is particularly challenging in high level count FCML converters, where any imbalance may cause both capacitor and switch voltages to exceed design limits. Active balancing techniques [59], [60] offer solutions across a wide range of operating conditions, but require high-bandwidth sensing and control. Component characteristics [61], operating point [62] and level count [63] can all effect capacitor balancing. In fact a theoretical FCML converter with no parasitic elements, i.e. no dampening effects, will not balance at certain conversion ratios. Moreover, recent work has also shown the effect of switch parasitic capacitance on balancing dynamics [64]. For this design, two different GaN devices were tested using the same PCB, with daughter boards to connect the two different footprints. For each switch choice, the switch-node voltage, labeled V_{SW} in Fig. 4.3, was measured at the same operating point. As shown in Fig. 4.4, the device with higher C_{oss}, the EPC2034C GaN FET, has much better balancing dynamics, resulting in overall higher performance and reliability. One should note, however, that the uneven pulse-train of Fig.4.4 (top) does not represent an unstable operating point. Rather, the flying capacitor voltages remain at imbalanced values, and the applied switch-node voltage is periodic, as the converter transitions through the different phases. To maintain even switch voltage stress, and to reduce the ripple current in the inductor, balanced capacitor voltage operation is preferred, and the results shown in Fig. 4.4 provide further experimental validation of the results in [64].

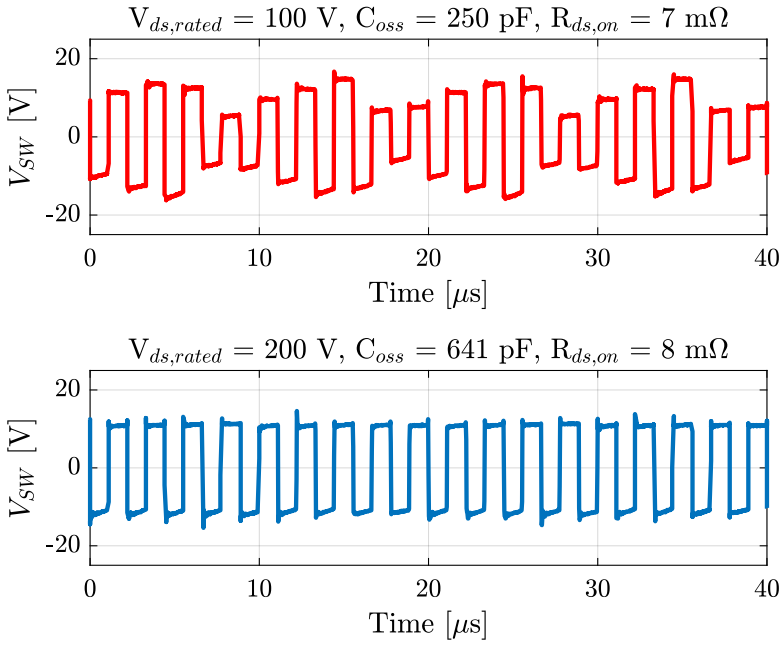

Figure 4.4: Switch-node measurement of 10-level FCML converter, measured with the same board and operating point, but two different GaN switches. Verified by work in [64], the switches with higher C_{oss} results in better flying capacitor voltage natural balancing.

Commutation Loop Design

In considering board layout, it is necessary to minimize commutation loops to decrease overshoot and increase switch transition speeds [65]. In this work, a vertical switching cell design was implemented to allow for a small commutation loop and increased voltage clearance. With the increased number of necessary capacitors, due to the high power and voltage rating, the commutation loop design becomes more challenging. Therefore dedicated commutation loop decoupling capacitors (C_{loop}) are employed, immediately adjacent to the complementary power switches, to reduce the loop area, as shown in Fig. 4.5. These capacitors use small form factor, low-inductance packages, with correspondingly low capacitance value, the value for which can be determined using work done in [66]. The commutation loop is further decreased by implementing a modified version of the electrically thin design, shown in Fig. 4.5-b, as proposed in [67].

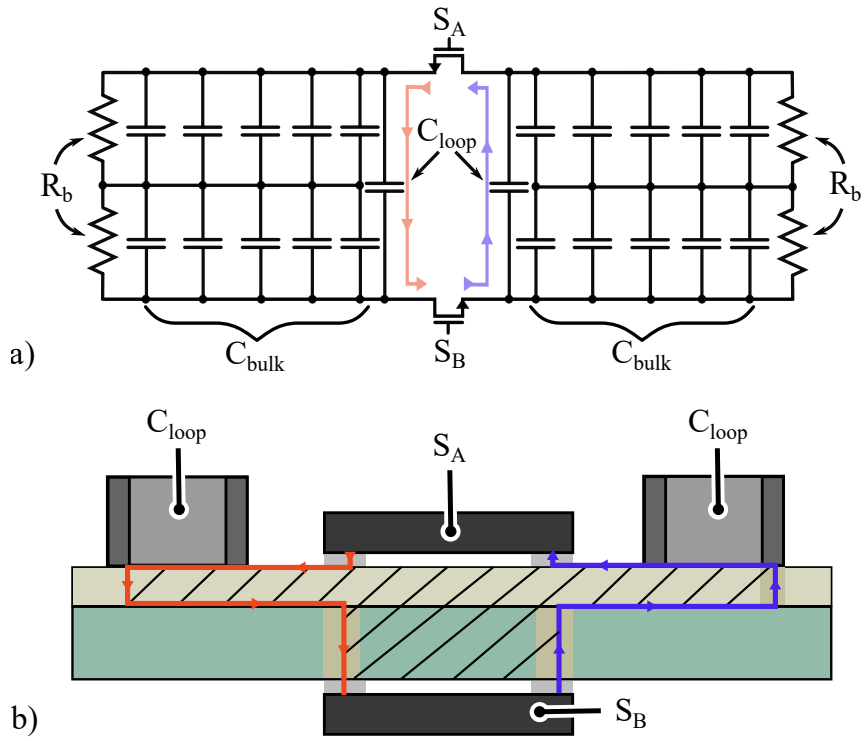

Figure 4.5: a) High voltage switching cell depicting large bulk capacitance and associated biasing resistors in addition to small high-frequency capacitors, C_{loop}, placed close to the switching devices. b) Commutation loop dual sided design using a modified electrically-thin layout with local capacitors to minimize loop inductance and blind vias to shape the current path.

Component	Part Number	Parameters
Switches	EPC 2034C	200 V
$C_{loop,LV}$	TDK C0G	47 nF, 450 V
$C_{loop,HV}$	KEMET C0G	22 nF, 1 kV
C_{bulk}	TDK X6S	2.2 μF, 450 V
Inductor	Coilcraft XAL1510	10 μH
Gate Driver	Si8275	Dual-sided
LDO	LP2985IM5	5 V Output
$S_{start-up}$	G7L-2A-X-L	20 A, 1 kV

Table 4.2: Component list for 10-level FCML boost design.

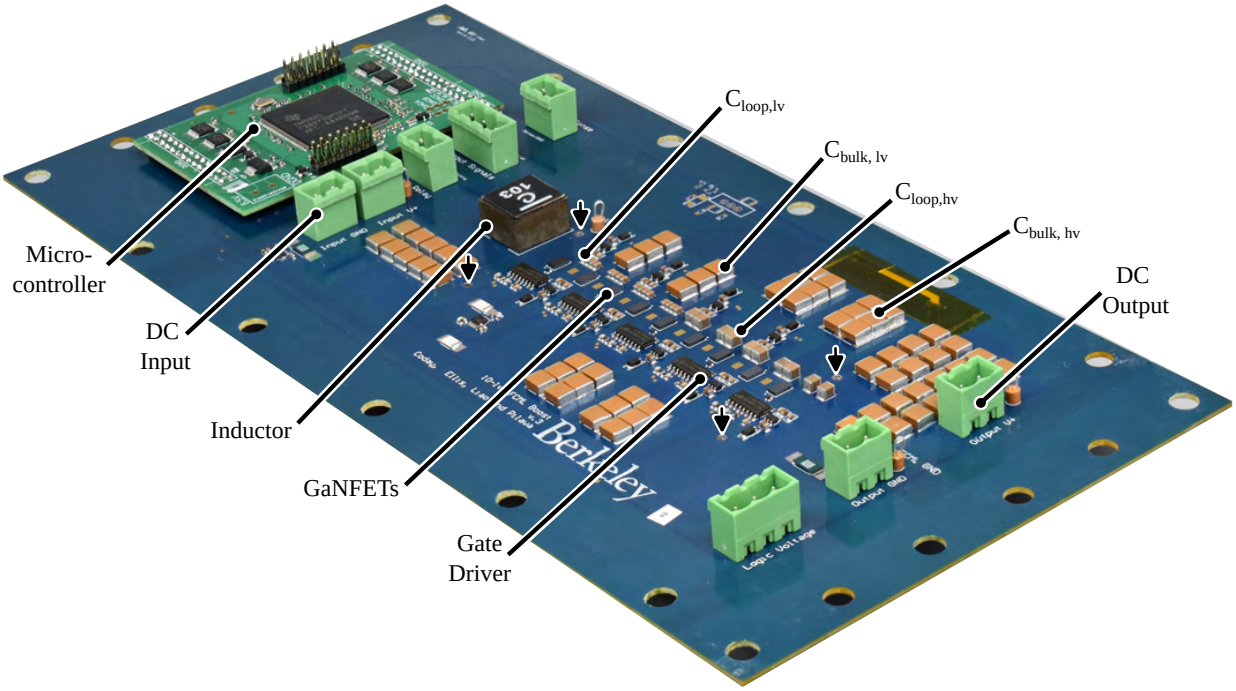

Figure 4.6: Top view of the hardware prototype. The four arrows show the mounting holes placed close to the main power stage to provide further structural support.

4.3 FCML Converter Performance

An annotated photograph of the converter can be seen in Fig. 4.6, with the relevant components labeled, and listed in Table 4.2. The power delivery for the gate drive was implemented using a cascaded bootstrap technique as demonstrated in [68]. The converter efficiency as a function of output power can be seen in Fig. 4.7, where the peak power was measured to be 99.52%, with gate drive losses included. A loss breakdown for converter operation at 1.6 kW is shown in Fig. 4.9. In addition, the weight breakdown of the converter can be seen in Fig. 4.8, which shows that the majority of the weight is due to the capacitors and the printed circuit board (PCB). A summary of the converter performance is shown in Table 4.3. As is evident from the photograph and weight breakdown, further layout/packaging improvement can yield even higher power density, but this initial prototype aimed to balance ease of manufacturing and use with very tight integration.

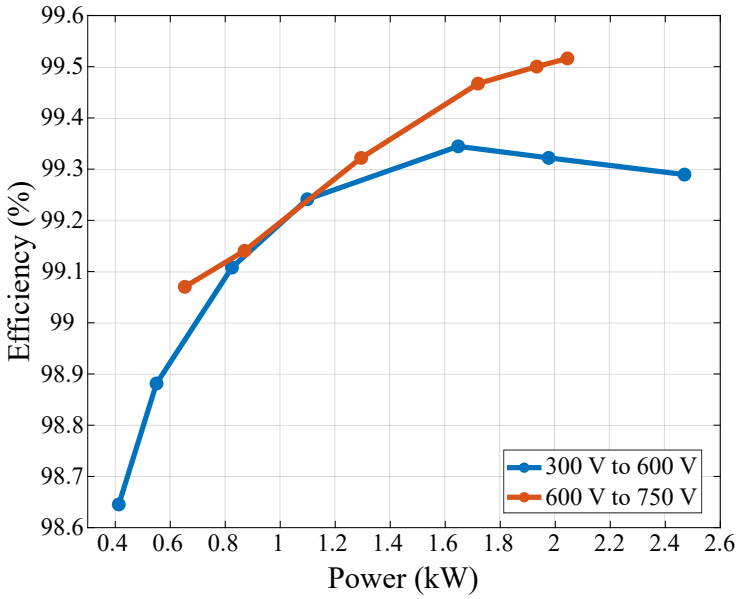

Figure 4.7: Measured efficiency of the FCML converter stage over a range of power levels. Note that these efficiency measurements include gate drive losses.

Description	Value
Input Voltage	100 V - 700 V
Output Voltage	750 V - 1 kV
f_{SW}	50 kHz
Effective frequency	450 kHz
Peak Efficiency	99.52 %
Peak Output Power	2.5 kW
Specific Power Density	28.2 kW/kg
Volumetric Power Density	16.6 W/cm^3 (247 W/in^3)

Table 4.3: FCML converter performance summary.

4.4 Conclusion

This work has presented a 10-level FCML converter capable of achieving efficiencies over 99% through implementation of; a cascaded bootstrap technique for gate drive, optimized device selection and a low commutation loop layout. With a power stage measured specific power density of 28.2 kW/kg, this hardware demonstration is indicative of significant future improvements to the performance of electric drivetrains in next generation hybrid electric aircraft.

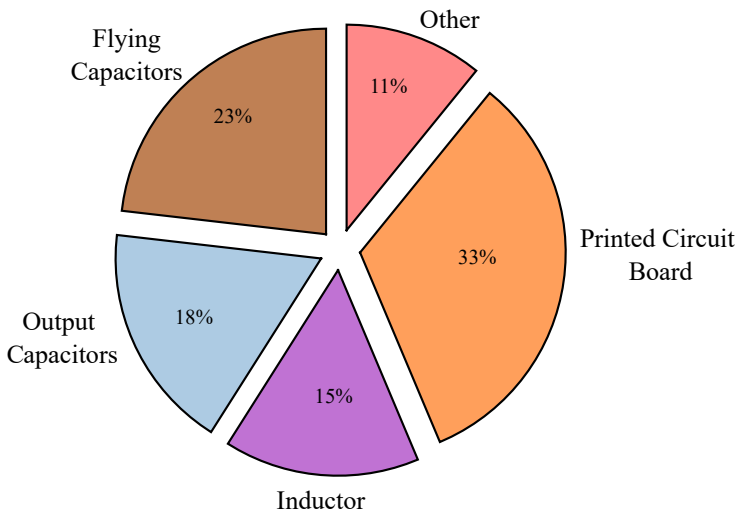

Figure 4.8: Weight breakdown of FCML converter. The majority of the weight is from the PCB and capacitors; both flying capacitance and output capacitance. Note, this weight breakdown is of the FCML converter only, and does not include the enclosure or the auxiliary boards which are independent of core converter design.

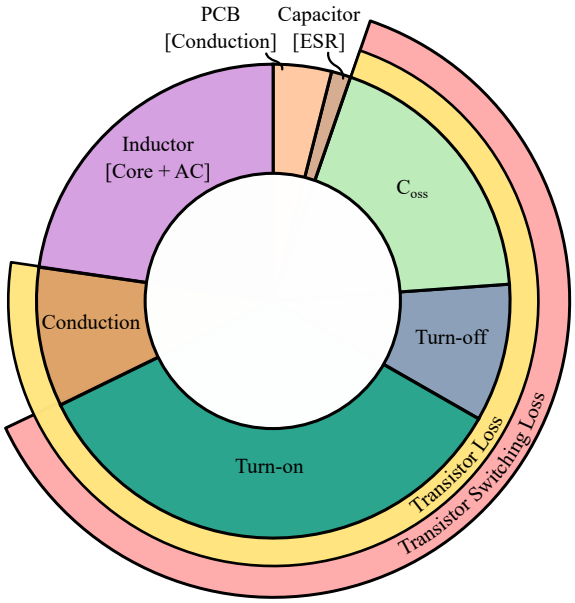

Figure 4.9: Approximate loss breakdown of FCML converter, while operating at 1.6 kW, 500 V input and 750 V output.

Chapter 5

Flight Qualification of a Flying Capacitor Multilevel Converter

5.1 Motivation

The previous chapter introduced the design of a high performance FCML converter, optimized for hybrid electric aircraft. One of the largest concerns of high-level count converters, such as the one presented, is reliability [14]. To motivate the use of these high performance, but also high level count converters in critical applications, this chapter focuses on the control, system design and fault tolerance necessary to increase converter robustness. To prove the resiliency of this system, flight qualification testing through successful thermal, shock and vibration testing that meets the DO-160G standards for low altitude fixed wing aircraft [51] is presented.

5.2 System Design

An annotated photograph of the full system design is shown in Fig. 5.1. In addition to the FCML converter, there are several auxiliary boards which add safety and control to the system. The FCML converter's input and output voltages and currents are sensed as shown in Fig. 5.2. Here the high voltages are sensed using a resistor divider, generating $v_{FCML,x}$ and $v_{out,x}$ which is then fed into the microcontroller. Similarly, the currents are measured using current sense resistors and the associated voltage drop is amplified and then fed into the microcontroller.

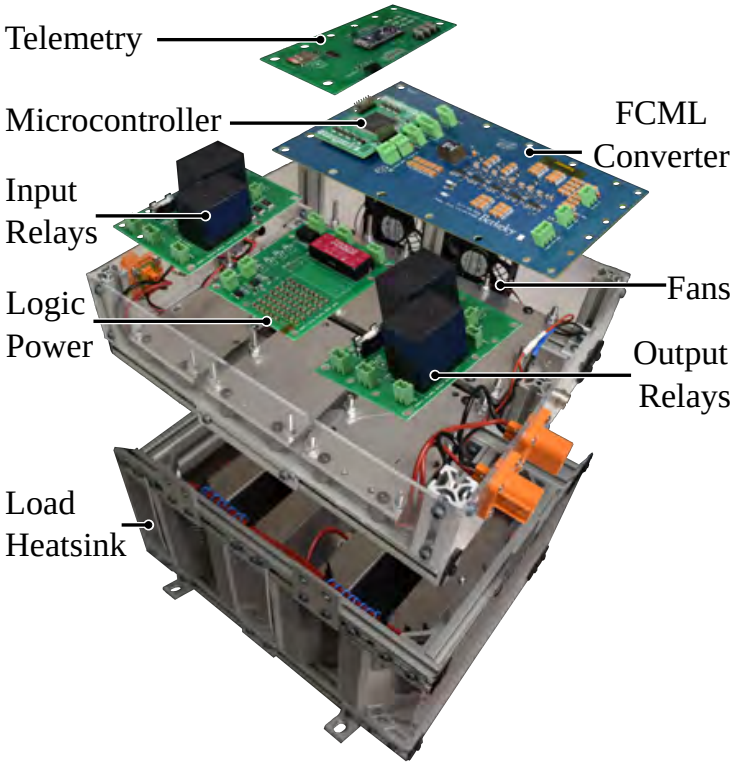

Figure 5.1: Exploded view of system, highlighting key components and printed circuit boards.

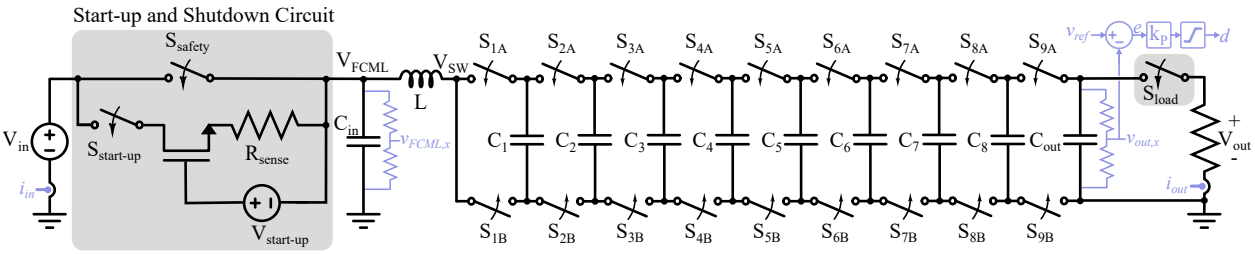

Figure 5.2: Ten-level FCML converter, highlighting the necessary start-up and shutdown auxiliary circuits. The relevant control sensing circuitry and diagram are also shown. This figure first appeared as Fig. 4.3, but is repeated here for readability.

Telemetry Board Design

The telemetry board shown in Fig. 5.1, was designed to communicate via UART with a C2000 microcontroller and additionally supports SPI communication with an on-board micro SD card reader. This allows the telemetry board to set flight status as well as collect and store

sensed data for later use. The telemetry board also collects data from on-board thermistors, which are placed on the inductor, a high-side switch and the output capacitance, enabling thermal verification.

In addition to the telemetry board, three additional auxiliary boards were designed to support operation and integration with the aircraft system. The input relay board contains the input relay (S_{safety}) as well as the necessary start-up auxiliary circuit. The output relay board contains the output relay (S_{load}) and an additional relay which enables a load step (160 W to 1.6 kW) during flight validation. Finally, the logic power board converts the 28 V bus supplied by the aircraft to the housekeeping bus voltages which supply the logic power on the converter, relays and fans.

For the targeted flight demonstration, the system will be connected to the dc bus of the hybrid electric aircraft and for the initial prototype, the output of the system is connected to a resistive load. For the flight qualification testing described below, the entire system (including the load) was verified.

5.3 System Control

Start-up

As described in [41], [69], the FCML converter requires a soft start to avoid capacitor voltage imbalance and over-stressing switches, as the initially discharged capacitors do not provide any blocking voltage. Thus, the rise-time of the input voltage must not be so fast as to overwhelm the self-balancing of the capacitor voltages during operation. It should be noted, however, that most practical converters must employ such limits on the input voltage, typically associated with in-rush current limiters to avoid ringing and overshoot of the input capacitors when they are initially energized. This work addresses start-up with an auxiliary circuit that uses a constant current to ramp the voltage of the input capacitance (Fig. 5.2). During this time, the converter is operating with a fixed duty ratio set to lower than the intended output voltage, for the purpose of providing charge transfer between flying capacitors and natural balancing of their voltages. The voltage ramp of the flying capacitors is shown in Fig. 5.3, where the voltages ramp at the same rate resulting in no over voltage stress on the switches. Once the initial start-up ramp is complete, confirmed with slope detection at the input and output voltages, then the input relay (S_{safety}) is closed. During the initial start-up phase, the load is disconnected to prevent in-rush current. Once the input relay is closed, the load is connected resulting in a current step. While some minimal transient dynamics occur in response to this load step, capacitors are sized sufficiently large such that capacitor voltage balance is maintained within safe regions and the converter is able to continue desired operation.

Finally, once the input and load are connected the closed loop control engages which ramps the output voltage to the desired set point (nominally 750 V in this system). The experimental validation of this start-up technique at high voltage is shown in Fig. 5.4-a.

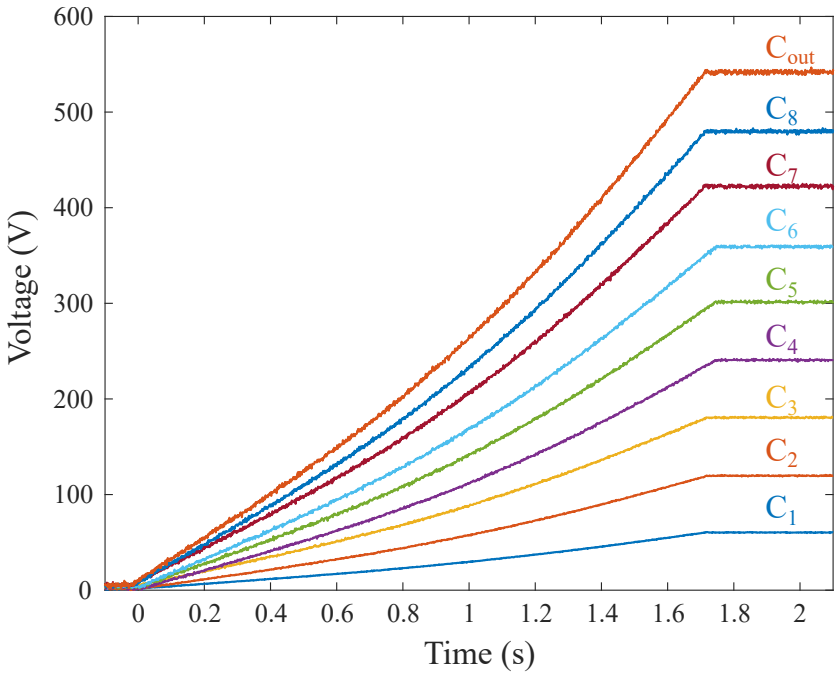

Figure 5.3: Flying capacitor voltages during start-up ramp, $t_{ramp,input}$. Measured at 500 V input.

The switch node voltage, labeled V_{FCML}, ramps with the input voltage and the peak-to-peak amplitude is $\frac{V_{out}}{N-1}$ across all duty ratios. However, when utilizing phase-shifted PWM [24] the average of V_{FCML} changes with the effective duty cycle which is defined as $(N-1)\times$ Mod$(D, \frac{1}{N-1})$. Therefore, in Fig. 5.4-a as the output voltage ramps to the desired set-point, the average of the switch node voltage modulates with the duty cycle. It is also important to note that in the start-up procedure, illustrated in Fig. 5.4-a, there are delays between each step of the start-up process to allow for visual presentation of the various stages. This work focuses on a novel and reliable start-up method, but future work should investigate further methods to speed up this routine depending on system requirements.

Shutdown

Similar to start-up, shutdown of the FCML converter must be carefully designed such that the flying capacitors do not discharge at different rates, causing over voltage stress on the switches. The shutdown process, at 750 V output, can be seen in Fig. 5.4-b. Note that the time-lapse between the initial shutdown, and when the input relay opens is due to the delay internal to the relay. For this implementation of shutdown, there is large capacitance placed on the logic supply for the output relay, which allows the output relay to stay connected during shutdown even when logic power is lost. Keeping the load connected during shutdown

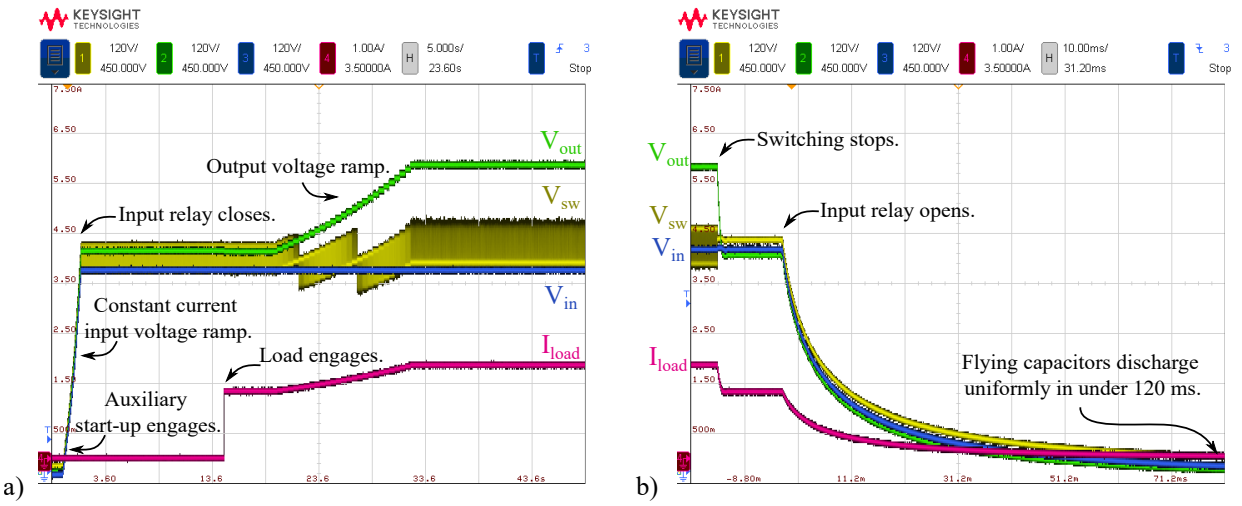

Figure 5.4: a) Experimental waveforms showing FCML converter start-up procedure using auxiliary start-up circuit. Start-up is measured at 500 V input, while regulating to 750 V output and 1.6 kW. b) FCML converter safe shutdown procedure, indicating uniform discharge of flying capacitors. Shutdown is measured at 550 V input, while regulating to 750 V output and 1.6 kW.

results in a fast shutdown (less than 120 ms) and no over-voltage on the switches. Further work investigating shutdown for FCML converters can be found in the following Chapter and in [70].

5.4 Fault Detection

Pre-startup Routine

Before the start-up procedure is initiated, a series of tests are conducted to ensure the system is operating as expected.

Logic Voltage

First, the 28 V bus voltage is sensed using an isolated sensing circuit, as the ground for the 28 V bus and the converter are not connected. This logic voltage bus can vary from 18 V to 30 V during flight. If the voltage is outside of this nominal range, the system will reset.

Communication Validation

To confirm communication with the telemetry board, the micro-controller and telemetry board complete a hand-shake protocol-meaning that both boards must receive and transmit

a key successfully before proceeding.

Short/Open Circuit Detection

An important consideration is the ability to sense a short-circuit load condition, which we accomplish in this work without any additional sensing hardware. While other flight qualified hardware may require similar pre-startup routines for robust operations, here a more unique approach is taken to determine short circuit status. As described below, we rely on an inherent charge redistribution within the FCML converter to infer the output load resistance. Once the previous steps have successfully completed, the FCML's switches (labeled $S_{n,a/b}$ in Fig. 5.2) begin to switch at a constant 0.07 duty ratio and switching frequency of 50 kHz. This duty cycle was chosen as it corresponds to the lowest gain required, assuming that the aircraft's battery is fully charged, and avoids the possibility of over-voltage on the output. During this time, the input/output relays (labeled $S_{start-up}$, S_{safety} and S_{load} in Fig. 5.2) are still open and therefore there is no voltage applied to the input of the converter.

The cascaded bootstrap technique introduced in [68] is used to drive the switches for this converter. This bootstrap method has been shown to significantly reduce the volume required to drive high-side switches in multilevel applications. In this implementation, the bootstrap voltage is 15 V, chosen to be high enough to supply voltage to all the switches, accounting for voltage drops across each bootstrap diode. The 15 V bus is generated with an isolated buck converter supplied from the 28 V bus. Despite there being no input voltage supply connected to the FCML power stage, the 15 V supplied to the bootstrap circuitry injects charge into the FCML's power path via the gate drivers, whose expended gate charge accumulates and results in a static non-zero voltage potential being present at the FCML's output. As a result, for a fixed load, frequency and duty ratio the potential measured at the output of the FCML is deterministic and can be measured to verify the current load condition. For this specific implementation, when the nominal load is connected (400 Ω) the potential seen at the output is 8 V. However, if there is an open circuit condition the output potential is 12 V. Finally, a short circuit condition at the output can be inferred by measuring a lower output voltage: set at a threshold of 4 V in this case. Once these tests have successfully finished, the start-up routine begins. If at any time during the pre-startup routine the tests do not complete as expected the system will set at error flag, resulting in a error detection LED on the telemetry board illuminating, and the system will not continue with the procedure.

Nominal Operation and Fault Detection

After start-up is complete, the output voltage is regulated using a simple proportional controller based on the measured output voltage ($v_{out,x}$) and the desired reference voltage (v_{ref}), as shown in the control diagram in Fig. 5.2. In addition, fault detection is performed every switching period to confirm expected operation. Cycle-by-cycle fault detection, while not

used in this work, has been previously demonstrated for the FCML topology [71] to quickly identify and recover from faults on a short time scale.

Logic Bus Voltage

Similar to pre-startup, during nominal operation the logic voltage bus is sensed to confirm the voltage is between 18 V and 30 V.

Input/Output Voltage and Current Checks

Since the converter is operating with a fixed load, the output voltage and current measurements are used to confirm nominal operation. Moreover, the input voltage which is defined by the battery voltage has an operating range of 500 V to 700 V. If the voltage is too high or low, a fault flag is set.

Transient Detection

In this system, it is not expected that the battery voltage will suddenly change. Instead slow discharge is expected, if a sudden voltage change is detected (the threshold was set to 20 V change within one switching cycle), then a fault flag is set.

Response to Faults

If a fault flag is set during nominal operation, the FCML will enter a safe shutdown routine. First the safety relay (labeled S_{safety} in Fig. 5.2) will open, thereby disconnecting the converter from the high voltage bus. Then the converter will stop switching and discharge all flying capacitors through the load. Once the flying capacitors have discharged (after approximately 200 ms) then the output relay will open (S_{load} in Fig. 5.2).

5.5 Flight Qualification

A key goal of this work was to demonstrate complete flight qualifications of the entire hardware system, so as to enable in-flight testing with our electric aircraft partner. Below, we briefly describe the thermal and mechanical aspects of the tests.

Thermal Testing

An added benefit of the FCML converter is its even distribution of heat. Since all switches conduct the same current for the same duration, and experience the same voltage stress, losses are uniformly distributed, as illustrated in the thermal image shown in Fig. 5.5. This inherent heat-spreading enables simplified cooling approaches: for this demonstration only two small 12 V fans are used to cool the converter. Fig. 5.5 shows the thermal performance

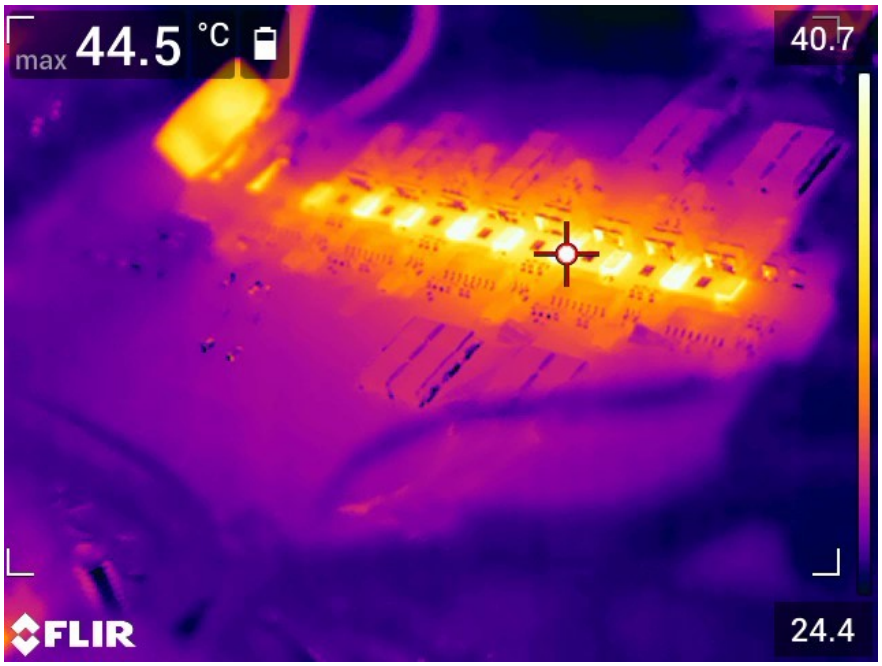

Figure 5.5: Thermal image of FCML converter at 1.6 kW, 500 V input and 750 V output, measured at room temperature, captured with a FLIR T540 thermal camera. The GaNFETs and inductor experience the greatest heat measured at approximately 45 degrees Celsius. Note, in this thermal image the inductor is lifted such that the current can be measured with a current probe.

while operating at full load for the desired flight condition, but while operating at room temperature.

Steady-state elevated temperature thermal testing was performed, with specifications derived from DO-160G [51], Section 4.5.4, Category A1. The converter and auxiliary boards were tested at a full load of 1.6 kW for two hours while placed inside a regulated temperature chamber set to 55 ^{o}C. The thermal test set-up is shown in Fig. 5.6, and the measured temperatures, using the thermistors on the telemetry board, are shown in Fig. 5.7. The maximum temperature on board was 15 ^{o}C above ambient, and well below device limits.

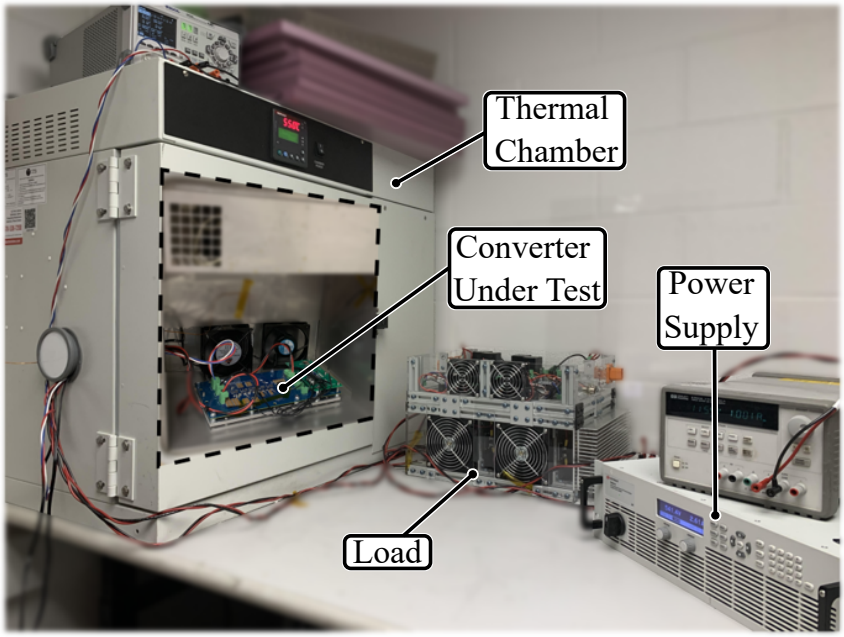

Figure 5.6: Annotated photograph showing thermal testing set-up.

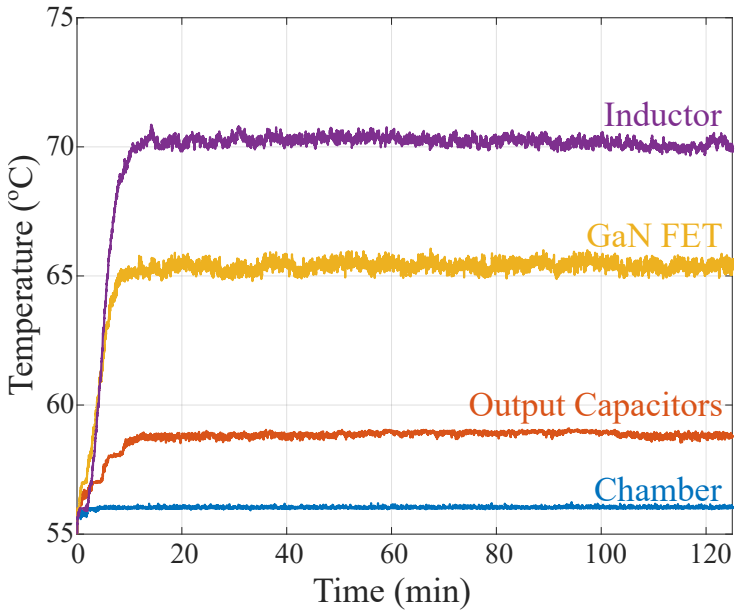

Figure 5.7: Measured temperatures on board the FCML during thermal testing.

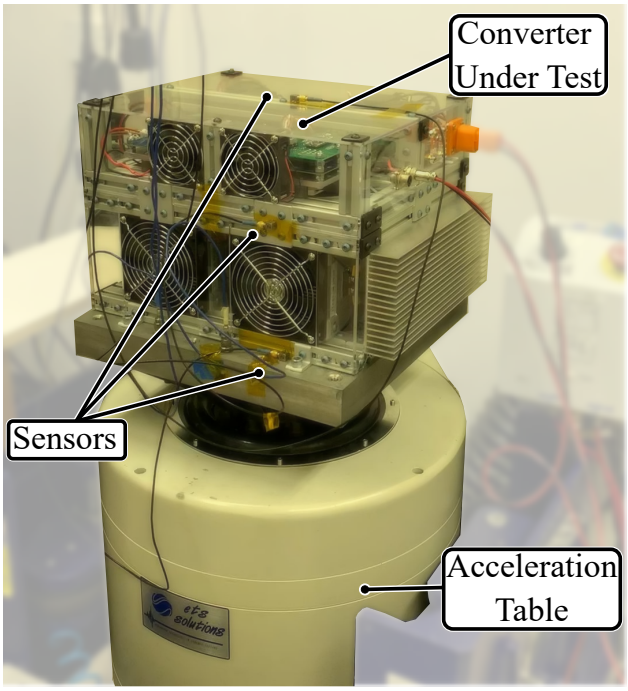

Figure 5.8: Annotated photograph of vibration and shock testing, showing acceleration applied in Z-axis.

Vibration and Shock Testing

Vibration was derived from the DO-160G standard [51], Section 8.0, Aircraft Type 4, Category S, Curve M/Curve L, Zone 1. This test was performed on the entire system, with the set-up shown in Fig. 5.8. For the vibration tests, the converter successfully operated at full output voltage for one-hour, while being accelerated in the X, Y and Z-axis, for a total of three hours of operation during vibration. In addition to the inherently advantageous mechanical properties of the FCML converter (e.g., many small distributed component and a low overall profile), care was taken in the mechanical assembly to avoid mechanical resonance between the converter, load, and enclosure. The required acceleration drive and measured response is shown in Fig. 5.9.

Shock testing was performed, the profile for which was derived from the DO-160G [51] Section 7.0, Category A. For shock verification each axis was tested with an applied 3 second sustained 9 G of acceleration, without mechanical failure.

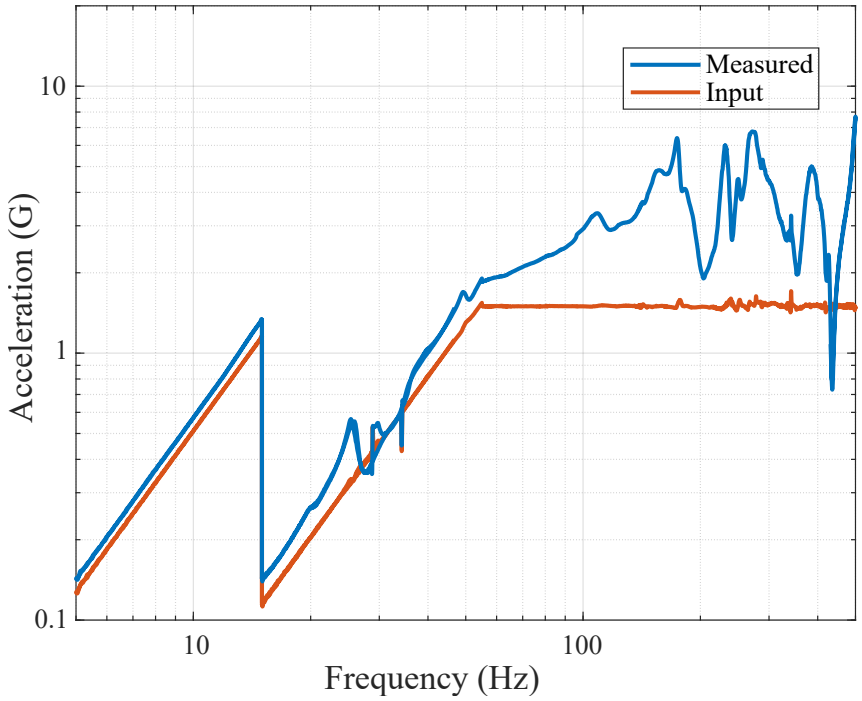

Figure 5.9: Input drive acceleration, used for characterization in X,Y and Z-axis. Measured acceleration from sensor placed on top of system, collected during acceleration in the Z-axis.

5.6 Preliminary Electromagnetic Interference testing

While not the focus of this work, future investigation is required to verify EMI compliance with the DO-160G. For example, recent work [52] has shown techniques for reducing conductive EMI in FCML converters. The successful completion of steady-state thermal, vibration and shock testing represents an important validation of high-level count FCML converters for use in electric aircraft systems and points to the promise of this type of converter for applications that require both ultra-light-weight and robust designs.

5.7 Conclusion

Through careful design, component selection, control and safety features, this work has demonstrated techniques for reliable design of a high-level count multilevel converter. The fault detection protocol and response are presented in detail. The overall system reliability is proven through a series of flight qualification tests.

Chapter 6

Safe Shutdown of Flying Capacitor Multilevel Converters

6.1 Motivation

Flying capacitor multilevel (FCML) converters [10] have been shown to have high efficiency and power density over a wide range of applications [72][24]; from high voltage electric aircraft drivetrains [40], to low voltage data center applications [73] and chip-scale implementations [74], [75]. The FCML converter achieves high power density through the use of flying capacitors, which can be implemented using energy dense capacitors, such as Class II multilayer ceramic capacitors (MLCCs). Moreover, the flying capacitors provide dc voltage blocking, enabling the use of low voltage power transistors with improved figures of merit, fast switching speeds and lower conduction losses [12].

While these flying capacitors enable compact and efficient designs they also present challenges, such as capacitor voltage balancing [76], [77]. If the capacitor voltages are not balanced, the voltage stress on individual switches within the FCML converter may exceed their rating, causing failures. While some control techniques have been proposed which actively balance flying capacitors during steady-state operation [59], [60], ensuring balanced operation at start-up and shutdown is particularly challenging, as all the flying capacitors must ramp up and ramp down with uniform voltages to avoid switch damage. Previous work has presented solutions to the challenge of start-up through additional auxiliary circuits [41] and sophisticated modulation techniques [78], [69]. While start-up has been the primary focus of previous work regarding the practical implementation of FCML converters, little work has been done exploring dynamics of converter shutdown, which is of great importance for practicing engineers who wish to design compact and efficient FCML converters that are also robust.

This work explores the voltage dynamics of the flying capacitors when an FCML circuit is suddenly de-energized, and investigates safe shutdown techniques in practical implementations. As demonstrated in [71], external system faults such as output short circuit transients

can be mitigated through changes to the switch modulation, where the converter switches are controlled to initially counteract the fault, followed by a "ride-through" mode where the converter remains active, but not outputting any power. This work considers the different scenario where the converter is shut down immediately, either due to loss of control/logic power, controller malfunction, or due to power transistor, flying capacitor, or gate drive degradation or failure that necessitates a rapid shutdown. In such scenarios, great care must be taken through design of auxiliary circuitry to ensure that component ratings are not exceeded. Moreover, a computationally efficient dynamic model of the FCML converter during shutdown operation is proposed, and used to demonstrate how device ratings and converter failure can result from sudden loss of control power. Based on the findings of the dynamic model, several safe shutdown techniques are verified and evaluated.

This article extends an earlier conference publication [70] of this work. Here, we present more detailed analysis of shutdown dynamics including the impact of conversion ratio. Moreover, this work presents additional experimental results validating the proposed model and safe shutdown methods. The remainder of this paper is organized as follows: Section II introduces the relevant FCML converter component models. Section III explores the effect of input/output capacitance and conversion ratio on a generic FCML converter shutdown. In Section IV, a model is described which was developed to predict switch stress during converter shutdown. Section V describes an experimental prototype used to validate the model. Section VI proposes three safe shutdown techniques and evaluates the performance of each. Finally, Section VII concludes the paper.

6.2 FCML Circuit Model

A generic N-level FCML boost converter [10], [79], used to model nominal operation, is shown in Fig. 6.1a. While the analysis presented here is for the boost converter, we note that due to the bi-directional nature of the FCML converter, the analysis also applies to a step-down (buck) implementation. In the model of Fig. 6.1a, input and output terminals are connected through switches (S_{input} and S_{output}) that may isolate the converter from the source and load during start-up and/or shutdown. This functionality is often required in practical implementations, where relays or solid-state circuit breakers may be employed.

During nominal FCML operation, switch pairs S_{iA} and S_{iB} operate complimentary to one another, and the flying capacitors are charged to $k \times \frac{V_{out}}{N-1}$, where k is the capacitor index, as shown in Fig. 6.1a as C_k. When capacitor voltages are balanced the voltage across each switch when in the off-state (excluding any flying capacitor voltage ripple) is $\frac{V_{out}}{N-1}$ as imposed by the two adjacent flying capacitors. However, if the capacitors are not balanced, i.e. they are not charged to their nominal voltages, then switch stress will vary and may result in overvoltage and device failure. This work investigates potential failures that stem from capacitor imbalance during the shutdown routine.

In general, converter shutdown can be either planned or unplanned. Here, we investigate the more difficult case - unplanned shutdown - stemming from a loss of control power which

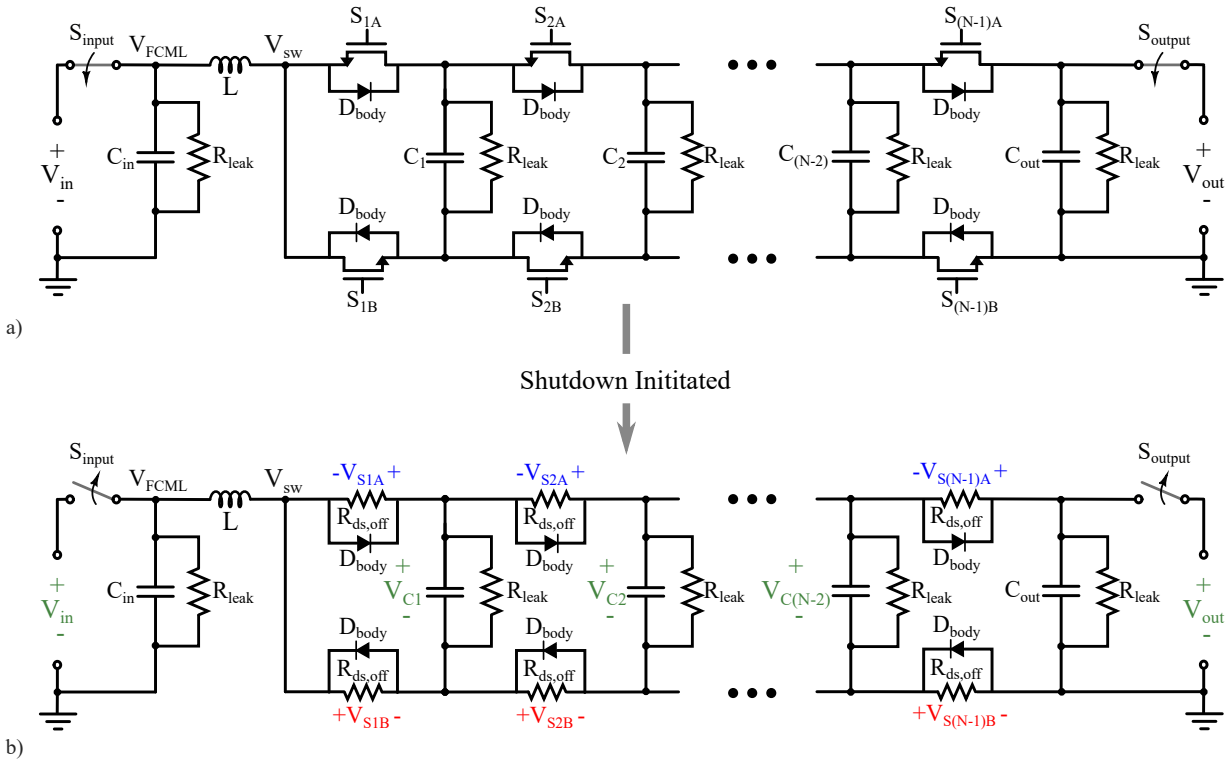

Figure 6.1: a) Circuit model of a generic N-level FCML converter [10], with input and output breakers. b) Circuit model once shutdown is initiated, with relevant parasitic components shown. Capacitor and switch voltages are also labeled.

results in the opening of input and output switches (S_{input} and S_{output}), and the loss of gate-drive power to all FCML switches, $S_{i,A/B}$. Once shutdown has been initiated, the converter can be modeled as shown in Fig. 6.1b. Since all FCML switches are open, they can be represented by their effective off resistance, $R_{ds,off}$ and intrinsic body diodes, D_{body}. Since the time constants associated with shutdown in practical FCML designs are typically very long (on the order of tens of seconds to over a minute), as dictated by leakage paths, the inductor can be modeled as a short. As will be shown in this work, the shutdown behavior of the FCML converter is highly dependent on component non-idealities, such as transistor body diodes and parasitic leakage paths. The following subsections describe the relevant component parasitics.

Switch Model

Body Diode

In Fig. 6.1, the anti-parallel diodes, labeled D_{body}, correspond to body diodes in silicon MOSFET implementations. Although Gallium Nitride (GaN) transistors do not have an intrinsic body diode, their reverse conduction associated with channel inversion is also captured by the diode model. When the diodes are conducting a small forward voltage drop (less than 2 V) may also be modeled. In this work, a diode drop of 1.7 V is modeled, which was chosen to match the GaN transistor used in the experimental validation [80].

$\mathbf{R}_{ds,off}$

Once the switches open, the drain-to-source leakage current can be modeled with an equivalent resistance, $R_{ds,off}$. While this resistance is typically large, it can still be an order of magnitude smaller than the leakage resistance of the flying capacitors and therefore must be included when assessing parasitic discharge paths. In this work, it is assumed that all switches are implemented with the same device and therefore have the same $R_{ds,off}$ value. Furthermore, in this work the $R_{ds,off}$ value is estimated based on the drain-to-source leakage current reported on the manufacturer's datasheet [80].

$\mathbf{C}_{OSS}$

Since each switching device's output capacitance, C_{OSS}, is small compared to to the flying capacitors, it has a negligible impact on shutdown dynamics. Specifically, as the time constants associated with the switch output capacitance is orders of magnitudes smaller than those associated with the flying capacitors, C_{OSS} may be safely neglected and is omitted from subsequent analysis.

Flying Capacitor Model

Capacitor Discharge

Upon entering shutdown, the flying capacitors will begin to discharge through both their internal leakage resistance and the leakage resistance of the switches. In the case where the flying capacitors are Class II MLCCs, the capacitance of the device will increase as the device discharges. An example capacitance de-rating curve for a Class II MLCC can be seen in Fig. 6.2. This creates a non-linear function as the voltage of each flying capacitor decreases at a different rate depending on its operating voltage.

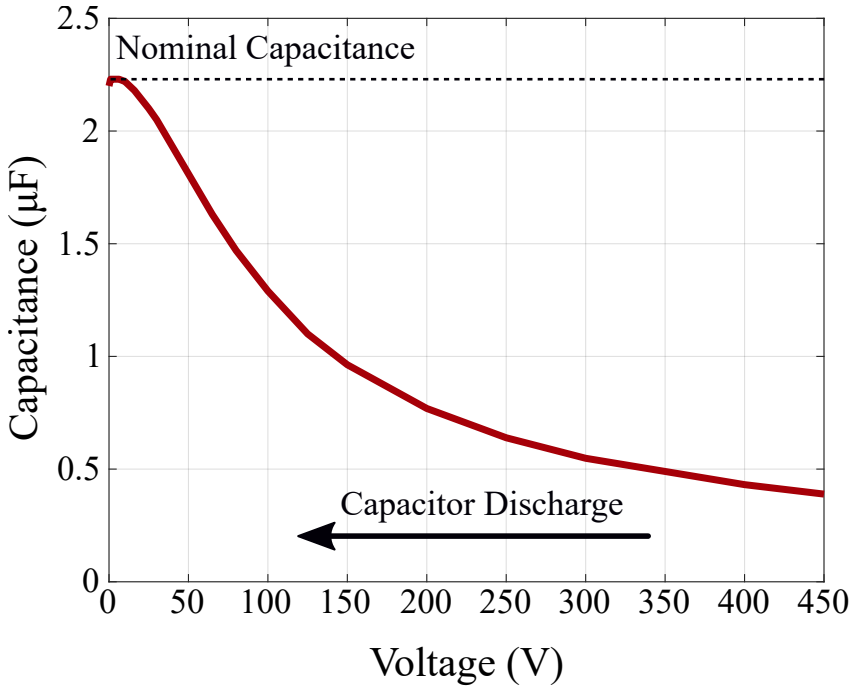

Figure 6.2: Class II MLCC capacitance de-rating curve, as the capacitor discharges the capacitance will increase non-linearly [37].

Leakage Resistance

Further complexity is added due to the leakage resistance which may vary between levels depending on the converter design. For the capacitor described in Fig. 6.2, the leakage resistance is listed as 227 MΩ on the datasheet [37]. However, this leakage resistance is not well documented and may change with operating conditions [29].

Balancing Resistors

In many FCML converter designs the flying capacitors are implemented with stacked MLCCs in series to increase the voltage handling capability [78] [38]. However, this introduces the possibility of unequal voltage sharing between series connected capacitors with variation in leakage resistance. To combat this uncertainty, matched balancing resistors, R_b, may be added as shown in Fig. 6.3. These balancing resistors decrease the effective leakage resistance to be approximately equal to R_b (assuming R_b is significantly smaller than R_{leak}) and thus provide a well defined voltage division between series connected capacitors. The introduction of R_b also acts to increase the discharge rate of the flying capacitors during shutdown. Here we define $R_{fly,i}$ to be the effective leakage resistance of the i^{th} flying capacitor, including the contribution of any balancing resistors.

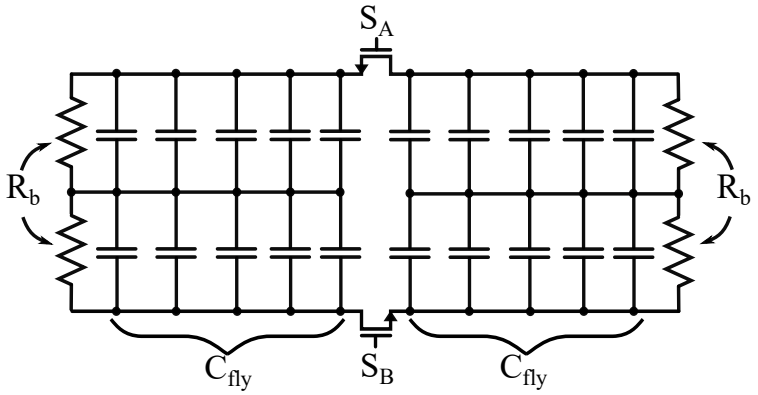

Figure 6.3: Example flying capacitor implementation showing series stacked capacitors and balancing resistors, R_b, which serve to ensure uniform voltage distribution among capacitors.

Input and Output Capacitance

During nominal FCML converter operation the input and output capacitance (labeled C_{in} and C_{out} in Fig. 6.1) has a significant effect on capacitor balancing [61] and converter performance [81]–[83]. Therefore in this work it is assumed that these capacitance values are sized to be at least 10x the flying capacitors, as is common in practical designs. As these capacitors have much larger values than the flying capacitors they will discharge more slowly depending on associated leakage paths, potentially leading to switch over-stress during shutdown.

6.3 General Shutdown Dynamics

Once shutdown is initiated, as shown in Fig. 6.1-b, the flying capacitors will begin to discharge through leakage paths. Additionally, the initial voltages stored on all capacitors, including C_{in} and C_{out}, will shape the discharge trajectory, implying that the converters conversion ratio prior to shutdown must be considered.

Impact of Conversion Ratio

When shutdown commences the voltage across each switch — labeled $V_{Si(A/B)}$ in Fig. 6.1-b — is dictated by the voltage stored on both the input and output capacitors, which initially store V_{in} and V_{out} respectively. Assuming that; all switches have the same leakage resistance $R_{ds,off}$, C_{OSS} is small (Section 6.2), and that all flying capacitors initially hold their nominal dc voltages when shutdown begins (neglect R_{fly}), it follows that the low-side switches will be subjected to an initial voltage stress of

$$V_{Si,B} = \frac{V_{in}}{N-1} \tag{6.1}$$

where i is the index of the low-side switch, and the high-side switches will see

$$V_{Si,A} = \frac{V_{out} - V_{in}}{N-1} \tag{6.2}$$

This results from each switch's $R_{ds,off}$ forming a resistor divider between V_{in} and ground, and V_{out} and V_{in} for low-side and high-side switches respectively.

Considering (6.1) and (6.2), the ratio of input to output voltage will impact the initial condition of the switch voltages which will in turn affect which switches (if any) experience reverse conduction as shutdown progresses.

To better understand the effect of conversion ratio on capacitor discharge, a 10-level FCML converter was simulated in PLECS. In this simulation, the input and output capacitance was fixed at 10x the flying capacitance. For each simulation the initial voltage on C_{in} was swept, while the initial voltage on C_{out} was kept constant. For each swept value, the maximum normalized switch voltage over the entire shutdown time was recorded, with low-side and high-side switches being recorded independently. The normalized value was found by dividing the maximum observed switch voltage by the nominal switch operating voltage, defined as $V_{out}/(N-1)$, and is helpful in showing how much the voltage increases during shutdown compared to nominal operation: in an ideal shutdown scenario the normalized switch stress would not exceed "1" (one).

The plots in Fig. 6.4 show the resulting normalized switch stress as a function of conversion ratio for a number of different conditions: To assess the impact of different leakage paths, the relative values of $R_{ds,off}$ and R_{fly} are varied in relation to both each other and proximal capacitive elements.

Dominant $R_{ds,off}$

In Fig. 6.4a the $R_{ds,off}$ of the switches was set to be 400 kΩ and the flying capacitor leakage resistance was set to be 227 MΩ, therefore indicating that switch leakage will be the dominant discharge path. Assuming that $R_{ds,off}$ is consistent across all switches, a uniform resistor divider string is formed and the capacitors will discharge at a uniform rate, without increasing the voltage stress across the switches. In this simulation, across all conversion ratios the normalized switch stress remains in a safe region, although we note that $R_{ds,off}$ is often poorly characterized and may change across devices and with voltage/temperature.

Dominant R_{fly}

Similarly, in Fig. 6.4b, the switch resistance is increased to 4 GΩ, so that the primary discharge path for the flying capacitors will be either through their balancing resistors or their own intrinsic leakage resistance, defined collectively here as R_{fly}. The rate of discharge is determined by the capacitance value as well as R_{fly} (forming an RC time constant). If the effect of D_{body} is temporarily ignored, capacitor discharge can be described simply by

$$V_C = V_{C,init} e^{\frac{-t}{R_{fly} C_{fly}(V_C)}} \tag{6.3}$$

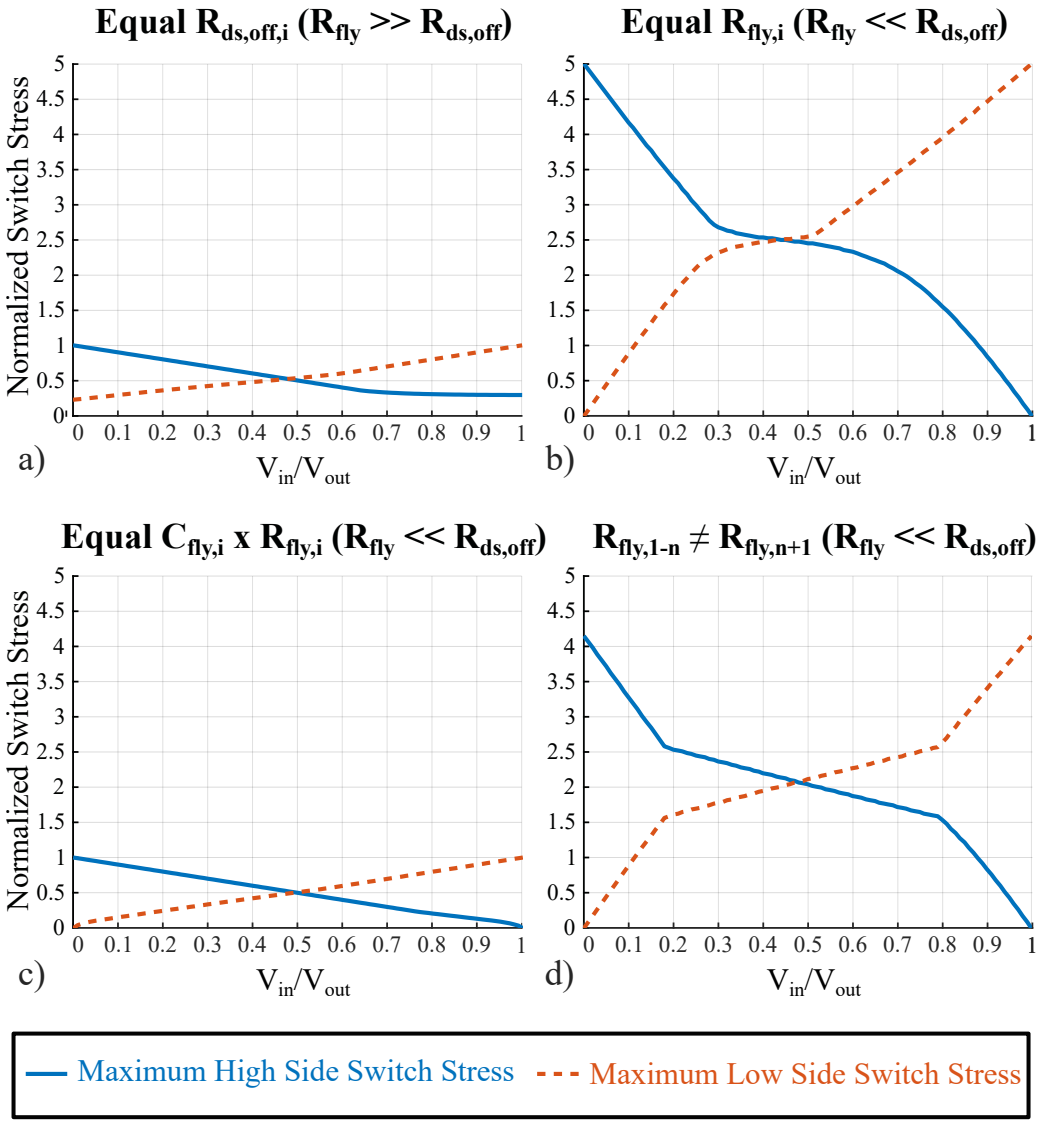

Figure 6.4: Simulated switch stress during shutdown as a function of conversion ratio, normalized about the nominal steady-state blocking voltage. (a) Safe shutdown with $R_{ds,off}$ of each switch equal and with dominant impact on rate of discharge. (b) Increased switch stress observed for R_{fly} induced discharge where $C_{fly} \neq C_{in/out}$ results in mismatched RC time constants. (c) No increased switch stress is observed when RC time constants are well matched. (d) Unequal R_{fly} between cells, where R_b is implemented only for high-voltage cells.

where shutdown commences at $t = 0$, $V_{C,init}$ is the initial flying capacitor voltage, R_{fly} is the effective discharge resistance defined by component leakage or balancing resistors, and C_{fly} may vary significantly with voltage (e.g. Fig. 6.2). In Fig. 6.4b R_{fly} is held equal across all capacitors, despite C_{in} and C_{out} being $10 \times C_{fly}$. As a result, adjacent capacitors experience differing RC time constants and will discharge at different rates thereby imposing increased (or decreased) voltage stress on neighboring switches.

Conversely, if RC time constants and the associated discharge rates of each capacitor is held equal, uniform discharge is again observed, leading to a safe shutdown without increased device stress. In Fig. 6.4c the input and output capacitors are still 10x greater than the flying capacitors, but are modeled with 0.1x the leakage resistance R_{fly}. As a result all the capacitors discharge at an equal rate with all switch voltages remaining at or below their nominal values.

Cautionary Use of Balancing Resistors

As described in Section 6.2, balancing resistors R_b are often used for high-voltage cells that construct flying capacitors using series connected low-voltage devices. This has the potential to significantly alter the effective R_{fly} seen between high-voltage and low-voltage cells, where R_b may not be included for low-voltage cells, absent of any series-connected capacitors. Without care, this may result in strongly mismatched RC discharge rates and in extreme cases lead to device overstress during shutdown. This situation is depicted in Fig. 6.4d where flying capacitors C_{1-i} have $R_{fly} = 227\ M\Omega$, while capacitors $C_{(i+1)-N}$ are simulated with $2\ M\Omega$. Where i is the number of low voltage cells which do not require balancing resistors, and N is the total number of levels. The resultant mismatch in RC time constants yields a voltage stress increase of over $2\times$ across all conversion ratios.

Effect of D_{body}

If the flying capacitors discharge non-uniformly, some switches will see a decreasing voltage stress that progresses at a faster rate than others. Subsequently, upon reaching 0 V, these switches will be subjected to a reverse bias and will begin to conduct through either their reverse body diode or as a result of $V_{GD} > V_{TH}$. Such an occurrence represents a non-linear event in which the circuit dynamics are changed considerably: Once reverse conduction commences, associated flying capacitors form a lumped capacitance and discharge with a new RC time constant defined by the lumped capacitance and leakage resistances. This effect is captured in simulation and causes the non-linearities observed in Fig. 6.4.

Additional effects such as reverse conduction voltage drop and resistance may be considered, but are assumed negligible at the voltage levels of interest.

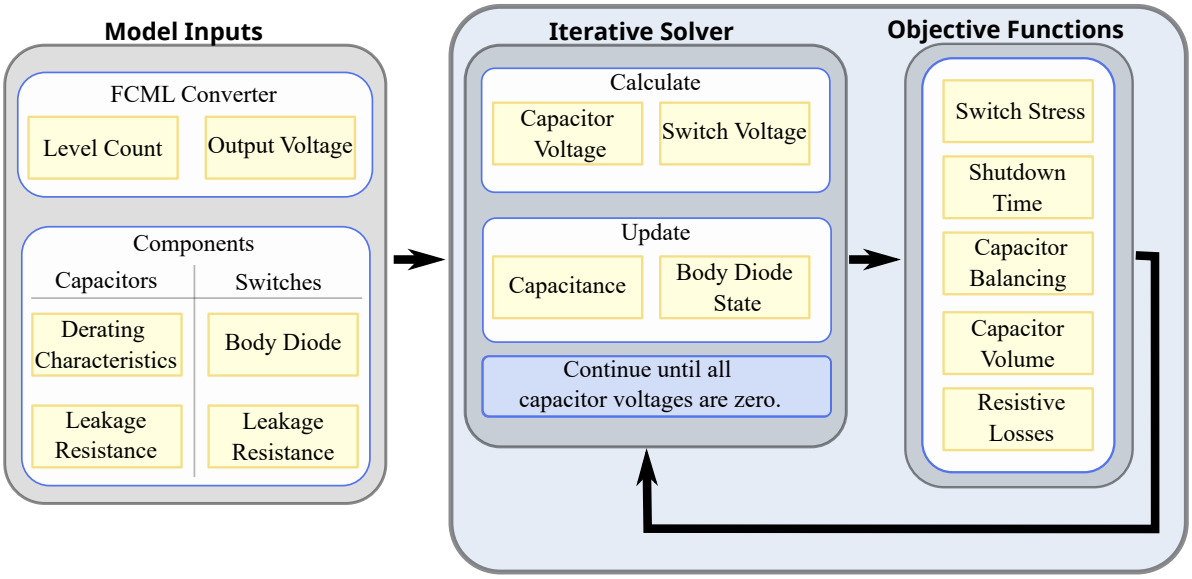

Figure 6.5: Flowchart for iteratively solved MATLAB shutdown model.

Capacitor De-rating

As described above, Class II MLCCs offer high energy density; however, they de-rate with voltage making the shutdown procedure more complicated to model. The PLECS generated results plotted in Fig. 6.4 include capacitor de-rating as shown in Fig. 6.2, although we note that the inclusion of capacitor de-rating does not significantly impact the maximum normalized switch stress.

6.4 Model Description

As noted in the preceding sections, the dynamic behavior of the FCML converter involves both non-linear passive elements, and switching circuit states due to diode turn-on. While circuit simulations (e.g., SPICE or PLECS) can compute the behavior for a specific converter design under narrowly defined operating conditions, it becomes intractable to perform design optimization and investigation across full converter operating ranges using such an approach. To enable computationally efficient investigation and design optimization of the FCML converter at shutdown, an iterative MATLAB model for a wide range of FCML design choices was developed in this work. As described in Fig. 6.5, the model requires the FCML converter design parameters as inputs: the level count, the output voltage, and details of the switch and capacitor choices. Incorporating the effects discussed in Sections 6.2 and 6.3, the model iteratively solves for capacitor discharge over time, updating the non-linear capacitance and diode states using a specified time-step for each cycle. As a result, the switch stress and capacitor voltage limits during shutdown can be included in overall FCML design optimiza-

tion, with shutdown time, balancing effects, volume and losses accounted for. As shown in Fig. 6.4, the worst switch stress occurs when the input voltage equals 0 V or when the input voltage equals the output voltage. In either case the majority of the switch stress will be completely on either the high-side or low-side switches. This work focuses on the case where the input voltage is zero, however the analysis and mitigation techniques provided can be applied to other conversion ratios.

This model also allows designers to investigate alternative fault scenarios. The inputs to the model allow for flexibility, therefore specific faults such as investigating shutdown when a switch which has failed short (i.e. $R_{ds,off} = 0\ \Omega$) is simple within the existing framework. In the following sections this model is used to predict shutdown dynamics and is validated against a constructed hardware prototype.

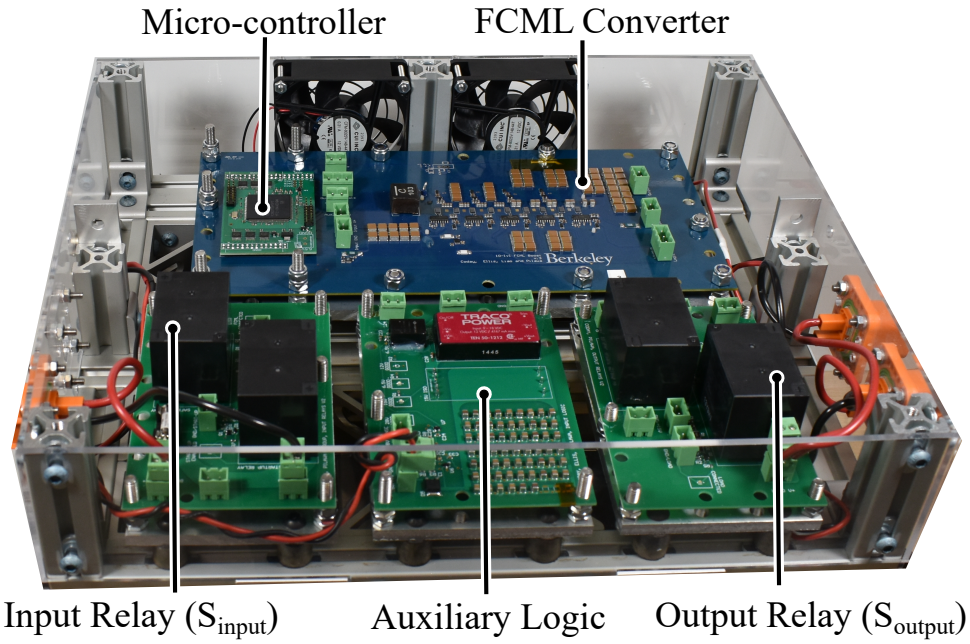

Figure 6.6: Hardware prototype, showing FCML converter, input and output relays.

6.5 Model Validation and Hardware Prototype

Experimental Prototype

For this work, a ten-level FCML converter with an output voltage of 750 V is considered. An annotated photograph of the hardware prototype can be seen in Fig. 6.6, with the input and output relays. The specifications and performance summary of the hardware prototype

is shown in Table 6.1. The nominal voltage and capacitance of each flying capacitor is shown in Table 6.2. The de-rated capacitance is also shown, which is calculated based on the derating curve shown in Fig. 6.2. Furthermore, this converter is designed with 200 V GaNFETs (EPC2034C), therefore it is vital that the switch stress remains below 200 V during shutdown.

Description	Value
Input Voltage	100 V - 700 V
Output Voltage	750 V - 1 kV
f_{SW}	50 kHz
Effective frequency	450 kHz
Peak Efficiency	99.52 %
Peak Output Power	2.5 kW
Specific Power Density	28.2 kW/kg
Volumetric Power Density	16.6 W/cm^3 (247 W/in^3)

Table 6.1: Experimental prototype specifications.

Flying Capacitor	Nominal Voltage	Nominal Capacitance	De-rated Capacitance	Series Capacitors	Parallel Resistance
C_{in}	550 V	33 μF	8.9 μF	Yes	2 MΩ
C_1	83 V	6.6 μF	3.96 μF	No	227 MΩ
C_2	167 V	6.6 μF	2.64 μF	No	227 MΩ
C_3	250 V	6.6 μF	1.98 μF	No	227 MΩ
C_4	333 V	6.6 μF	1.32 μF	No	227 MΩ
C_5	417 V	5.5 μF	1.65 μF	Yes	2 MΩ
C_6	500 V	5.5 μF	1.38 μF	Yes	2 MΩ
C_7	583 V	5.5 μF	1.20 μF	Yes	2 MΩ
C_8	667 V	5.5 μF	1.10 μF	Yes	2 MΩ
C_{out}	750 V	33 μF	6.9 μF	Yes	2 MΩ

Table 6.2: Flying capacitor design specifications.

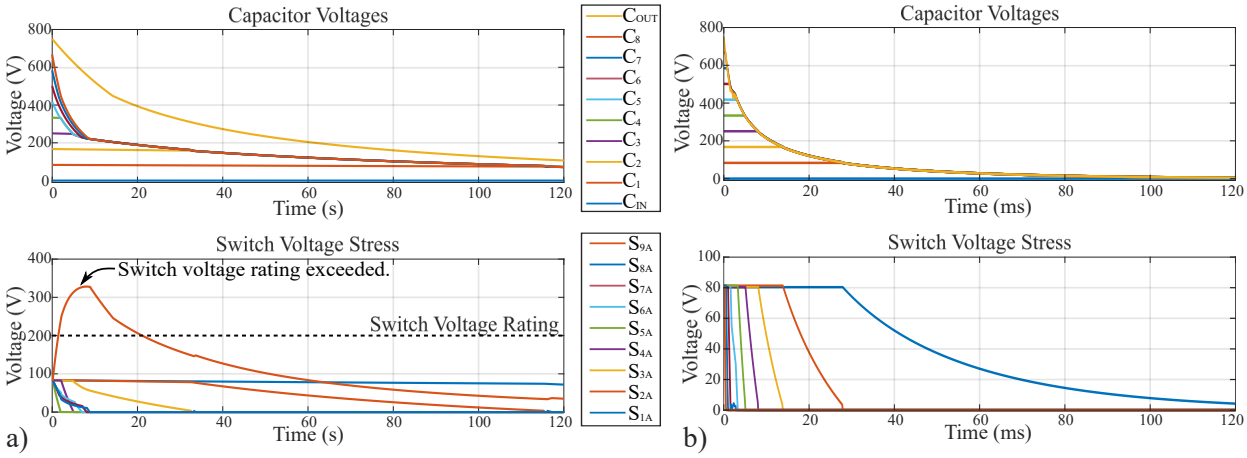

Figure 6.7: a) Modeled shutdown, where no safe shutdown techniques are implemented. The complete shutdown process takes over two minutes and the voltage rating of the switches is exceeded, resulting in an unsafe shutdown condition. b) Modeled shutdown with resistive load. With this method complete shutdown occurs after 120 milliseconds. All switch voltages remain under their rated voltages, therefore resulting in a safe shutdown condition.

Modeled Unsafe Shutdown

Shown in Fig. 6.7a are plots of flying capacitor and switch voltages over time for a shutdown procedure with the model parameters of Table 6.2. Considering the prototype converter with no special consideration for shutdown, the model determines the capacitor discharge and worst case switch stress. During this shutdown the highest high-side switch (S_{9A}) experiences switch stress over 300 V, well above the rated device voltage, which would result in a device failure. The key contributor to the large switch stress is the output capacitor, which decays much slower than the flying capacitors due to its significantly larger capacitance. In addition to the required terminal voltage filtering, a sufficiently large output capacitor (in comparison to the flying capacitors) is also needed to ensure good capacitor voltage balancing during steady-state operation [61]. Thus, simply reducing the output capacitor to avoid this condition is not a feasible solution in a practical implementation. As shown in Fig. 6.8 this shutdown procedure was verified with hardware, to show the increased voltage stress across S_{9A} after shutdown was initiated.

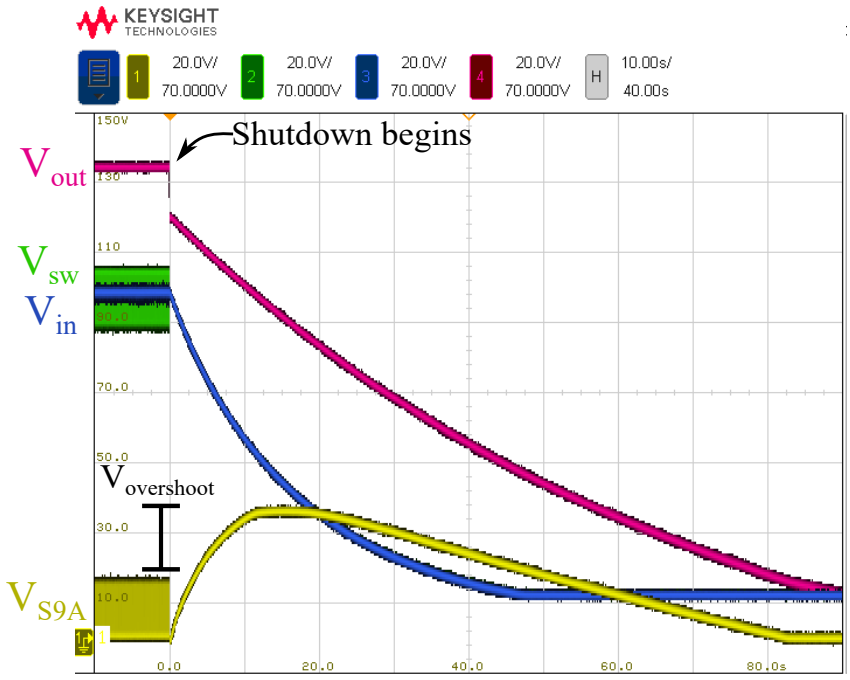

Figure 6.8: Experimentally measured shutdown with no safe shutdown methods. The high side switch V_{S9A} shows increased voltage stress after the shutdown procedure begins.

6.6 Safe Shutdown Techniques

The model was used to test and validate several safe shutdown approaches. These shutdown procedures are designed with the following goals of safe shutdown:

- Low switch stress: The switch stress should not exceed the voltage rating of the device during shutdown procedure. If the drain-to-source voltage of the switch exceeds the device rating, this in an unsafe shutdown condition as it may result is a device failure.
- Short shutdown time: The shutdown time should remain short. If the system does not completely discharge before a subsequent start-up attempt, the capacitors may start-up non-uniformly, resulting in failure.
- Low losses: Any additional circuitry added to the system should not incur significant losses during nominal operation.
- Small footprint: The suggested shutdown circuitry should have a negligible impact on the overall converter volume/weight.

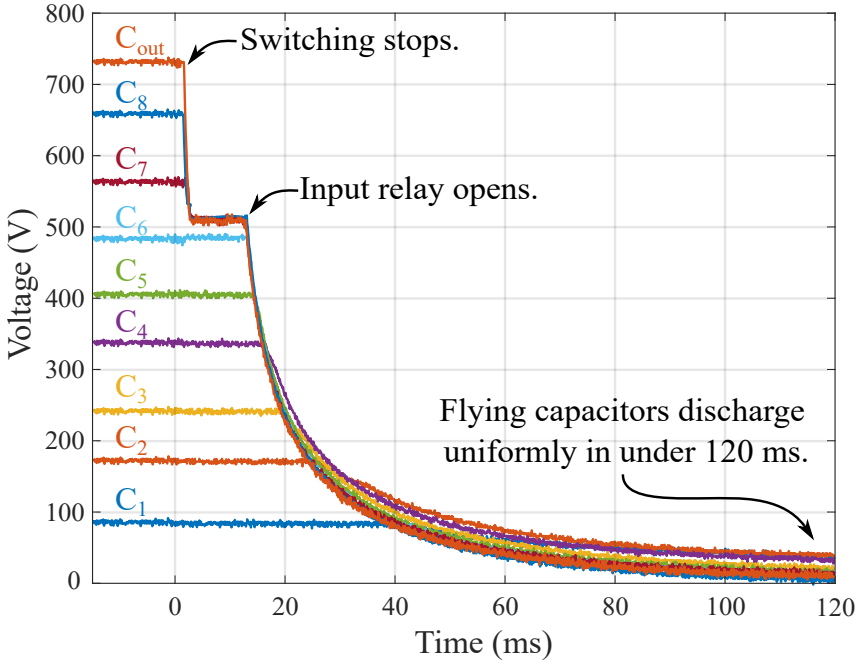

Figure 6.9: Experimentally measured flying capacitor voltages during shutdown, with resistive load connected. Shutdown initiated from 750 V output steady-state operation.

In the following sections, three different shutdown techniques are proposed. For each method the benefits and challenges are outlined, allowing designers to select the best technique for a specific application and constraints.

Normally Connected Resistive Load

The first proposed solution is to connect a resistive load during shutdown. This can be done with a normally-on configured switch in place of S_{output}, as shown in Fig. 6.1a, so that even with loss of logic power the resistive load remains connected to the output capacitance. This method effectively increases the discharge rate of the output capacitance. Fig. 6.7b shows modeled shutdown with the resistive load. With this method there is no over-voltage of the switches and the shutdown process occurs in approximately 120 milliseconds, for the given load of 200 Ω . This shutdown procedure was verified with the experimental prototype at high voltage (750 V) and the flying capacitor voltages were measured. As shown in Fig. 6.9, the experimental results signify safe shutdown through uniform capacitor discharge. Note, the delay shown in Fig. 6.9 between the switching and input relay opening is due to the internal delay in the relay.

While effective, it is not always feasible to keep the load connected during shutdown, which is a limitation of the suggested technique. For safety reasons it is often not desired to continue powering the load during a shutdown. Moreover, this method requires a primar-

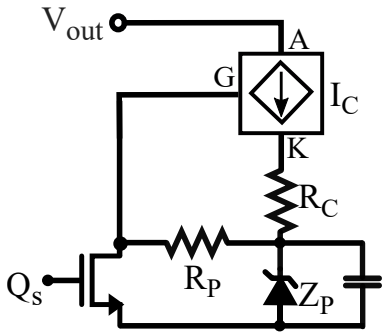

Figure 6.10: Auxiliary shutdown circuit, utilizing a switchable current regulator (I_C).

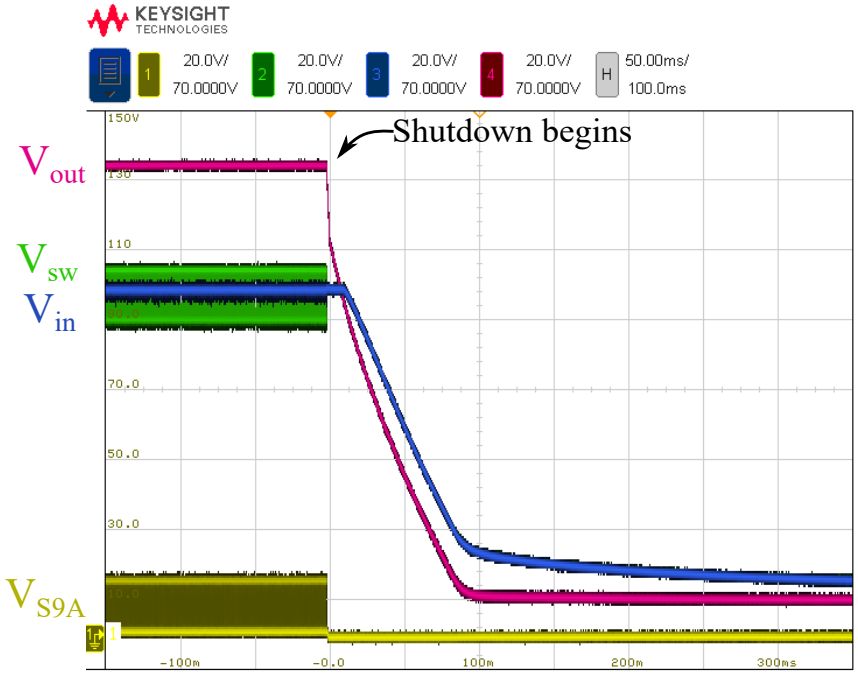

Figure 6.11: Experimentally measured voltages during shutdown, while implementing the auxiliary shutdown circuit shown in Fig. 6.10. With this method no overshoot is observed.

ily resistive load which also is dependent on system architecture. Therefore, the following sections present alternative methods which do not rely on a resistive load.

Auxiliary Shutdown Circuit

Fig. 6.10 shows a proposed auxiliary circuit which implements a switchable current regulator (I_C) [84]. This auxiliary circuit is similar to one proposed in [41] to aid in converter start-up.

A normally high signal from the micro-controller, labeled Q_s keeps the current regulator off during nominal operation. Once shutdown occurs and Q_s transitions to 0 V, the current regulator turns on and provides a discharge path for the output capacitance. The resistor, R_C sets the constant current, designed in this case to 100 mA.

The model was configured to account for this current regulating device, and the results are shown in Fig. 6.12-a. This method results in a shorter shutdown time than the previous method, and ensures no device overvoltage. This auxiliary shutdown circuit was built and tested with the hardware prototype. Fig. 6.11, shows the measured results, indicating no overshoot during shutdown. However, this auxiliary circuit does require added volume. For this prototype the auxiliary circuit was implemented in less than 0.4% of the total converter volume. It should also be noted that this auxiliary circuit does not consume any power during nominal operation and therefore does not decrease the converter efficiency.

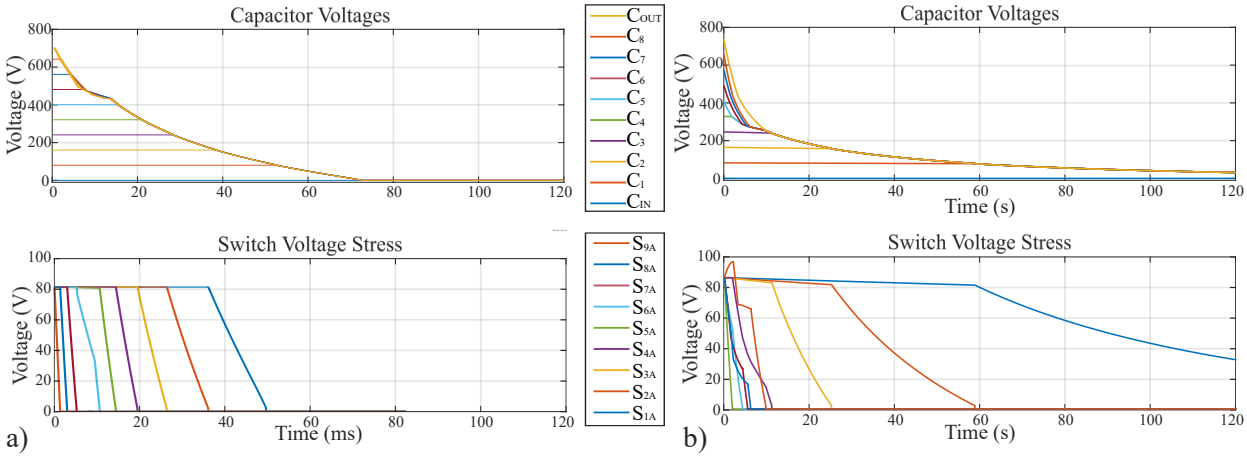

Figure 6.12: a) Modeled shutdown with auxiliary shutdown circuit. b) Modeled shutdown with adjusted balancing resistor value to decrease voltage stress.

Adjustment of balancing resistors

As indicated by the proposed model, the selection of the balancing resistors has a significant impact on the discharge of the capacitors. To increase the discharge rate of the output capacitance the balancing resistor at the output can be decreased. For this example, the effective parallel resistance of the output capacitance was decreased to 1 MΩ. As shown in Fig. 6.12-b, this method results in a small amount of additional voltage stress on the switches, but is still well below their rated voltage. This technique of reducing the output capacitor balancing resistor was confirmed in hardware. As shown in Fig. 6.13 there is a small amount of overshoot observed, but well below the example shown in Fig. 6.8.

This method results in a negligible volume increase as the balancing resistors were already included in the design. However, this resistance does add to the overall converter losses. At

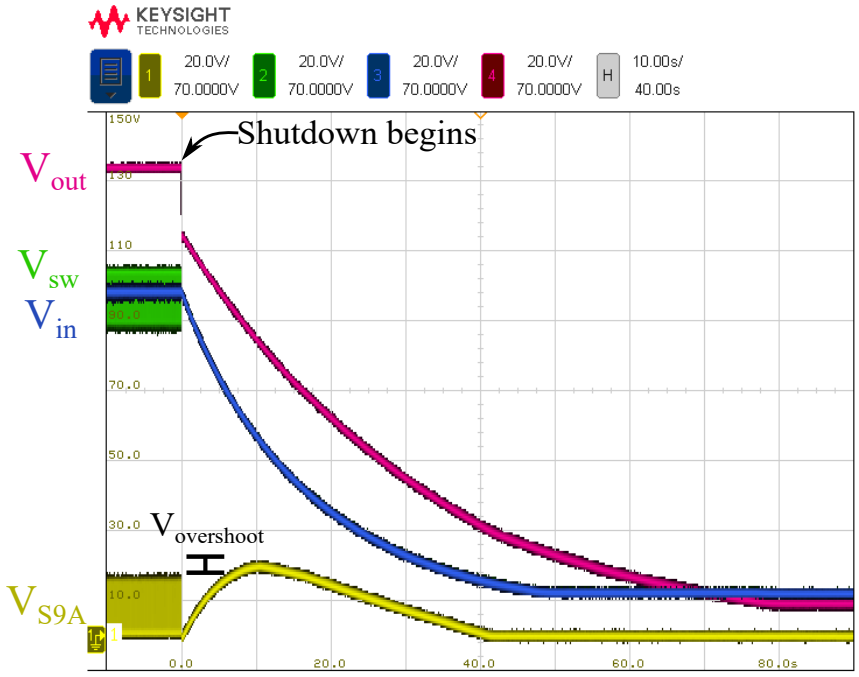

Figure 6.13: Experimentally measured shutdown, with modified output capacitor balancing resistor. There is a small amount of overshoot measured with this method.

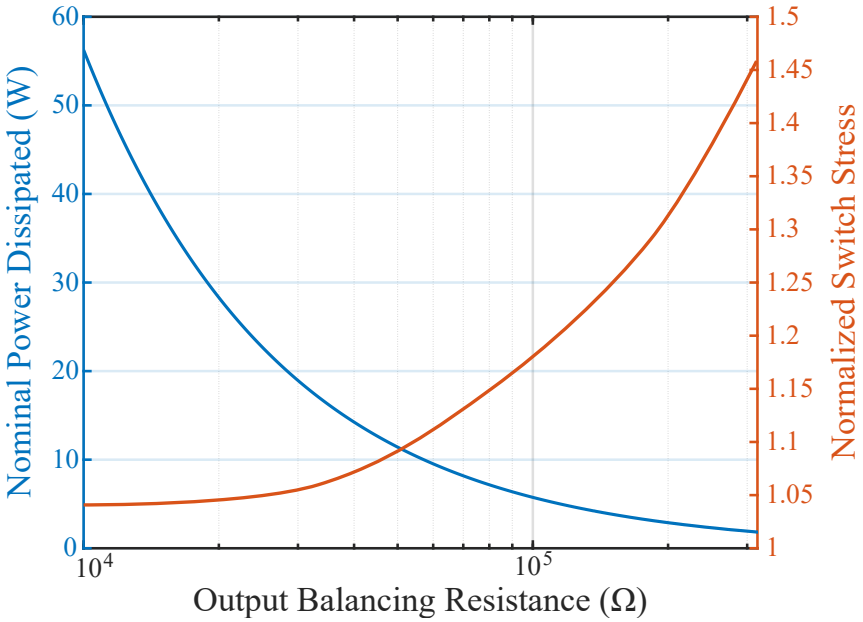

Figure 6.14: Power dissipated in balancing resistors during nominal operation and normalized switch stress as a function of modified output resistance.

750 V output, these balancing resistors will dissipate 1.2 W. These additional losses are considered negligible at high power (2.5 kW for this prototype), but may be deemed significant at light load or idle operation. Fig. 6.14 shows this trade-off between power dissipation and normalized switch stress in a plot where the output balancing resistance is adjusted. The power converter can thus select the appropriate trade-off for a particular design, to meet the overall system objectives. With the chosen balancing resistor values, Fig. 6.13 demonstrates shutdown in approximately 80 seconds. This shutdown duration is significantly longer than shown with methods introduced in the previous sections. Alternatively, the shutdown speed of this method could be shortened with the selection of a smaller balancing resistance. However, as highlighted in Fig. 6.14, selecting a smaller resistance also results in higher nominal power dissipation.

Comparison of Proposed Techniques

It should be noted that although the power converter itself was designed to achieve high power density, in this work startup and shutdown components were not weight or size optimized, but rather focused on demonstrating and exploring the various concepts. A summary of the proposed shutdown methods is shown in Table 6.3, which highlights the added power loss and volume for the various shutdown techniques, as implemented. Note, this comparison is for the specific values tested with the presented experimental prototype and may vary for different converters. For this work a nominally connected resistive load presents a safe, fast and low loss shutdown method. However, this method may not be feasible in some applications, therefore motivating the use of the auxiliary circuit presented in Fig. 6.10. Finally, in a volume-limited application, adjustment of the balancing resistors ensures safe shutdown but with the consequence of additional losses.

Shutdown Method	Switch Stress	Duration	Loss	Added Volume
Resistive Load	$<$ nominal V_{DS}	120 ms	0 W	-
Auxiliary Circuit	$<$ nominal V_{DS}	80 ms	0 W	1 cm^3
Balancing Resistors	10% of nominal V_{DS}	80 s	1.2 W	-

Table 6.3: Comparison of proposed shutdown techniques.

6.7 Conclusion

This work has demonstrated the need for safe shutdown techniques within the FCML converter. A framework for modeling the FCML converter during shutdown was introduced, which includes non-linear component effects. Subsequently, this model may be used to design for safe shutdown dynamics with constrained device stresses. Experimental results verify

safe shutdown with a resistive load. Furthermore, several additional techniques that also result in safe shutdown are modeled and evaluated, providing a framework by which optimal shutdown strategies can be selected for a given design.

Chapter 7

Overview of Converter Requirements in Space Applications

7.1 Radiation Effects in Space

Radiation effects in space make it difficult to design high performance power electronics. The most common types of radiation which affect electronic components are gamma, neutron and heavy ion bombardment [85]. Enhancement mode GaN FETs withstand these types of radiation better than silicon devices. The basic structure of an enhancement mode GaN device is shown in Fig. 7.1.

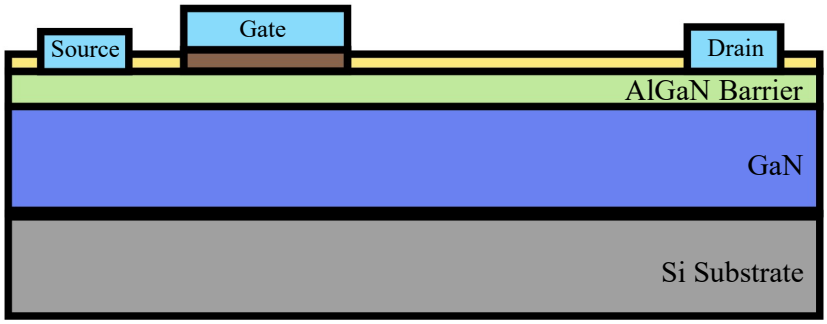

Figure 7.1: Simplified structure of an enhancement mode GaN FET [85], [86].

Typically, gamma radiation results in gate charge that can turn a normally off device into a normally on device. However, in GaN devices the gate is separated and therefore does not accumulate charge. Similarly, neutron radiation results in displacement damage, but GaN has higher displacement threshold energy resulting in less damage. Lastly, heavy ion bombardment results in higher drain-to-source leakage current, which can result in single

event effect (SEE) failures. These SEE failures are more prominent with increased drain-to-source voltage [15]. Therefore, when GaN devices are utilized in high radiation environments the drain-to-source voltage is often derated by 50% to ensure reliable performance.

Recently, Efficient Power Conversion (EPC) has released a product line of radiation hardened GaN FETs [87]. While currently these devices are not available for purchase, they show SEE immunity for linear energy transfer (LET) of 85 MeV/(mg/cm2) with a drain-to-source voltage up to 100% of rated breakdown. This allows designers to use the GaN devices at their full rated voltage instead of derating components. These new devices are plotted against existing GaN devices in Fig. 7.2, showing competitive figures of merit.

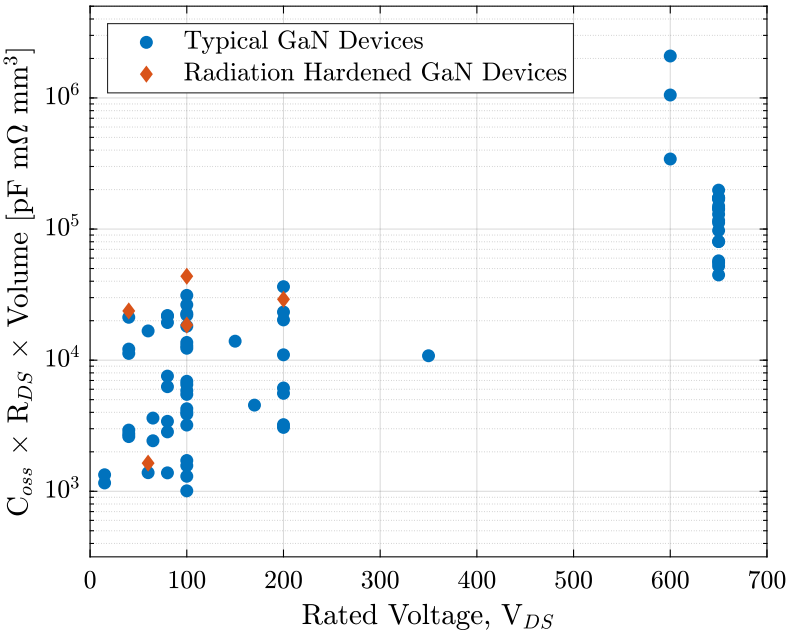

Figure 7.2: Survey of commercially available GaN devices, including EPC 70XX devices which are radiation hardened components [88].

7.2 Motivation for Hybrid Switched-Capacitor Converters

There has been recent preliminary production of GaN FETs which have a blocking voltage greater than 650 V [89]. However, most current technology has a maximum rated voltage of 650 V (as shown in Fig. 7.2), which means with a 50% derating, the maximum drain-to-source voltage designers can utilize in high radiation environments is 325 V. In Chapter 8 and Chapter 9, two examples are presented of converters necessary for future space exploration,

which require input/output voltages exceeding 500 V. By utilizing hybrid SC converters which decrease the necessary switch blocking voltage, higher voltages at the input/output terminals is possible while using lower voltage devices.

Chapter 8

Flying Capacitor Multilevel Converter Designed for Electric Propulsion

8.1 Motivation

Future development of electric propulsion technology is necessary for further space exploration [90]. Many electric propulsion techniques, such as Hall-effect propulsion (HEP), requires high supply voltage to increase the specific thrust [91]. The HEP power is often supplied by solar power systems, which have large variation in voltage as distance from the sun increases and due to the spacecraft's angle to the sun during maneuvering. For maximum system efficiency, and reduced weight and size, it is desirable to connect the wide voltage range photovoltaic arrays to the HEP through a single high step-up power converter [90]. An example of a HEP system powered by photovoltaic arrays is shown in Fig. 8.1.

However, designing power converters which are capable of withstanding hundreds of volts is difficult due to radiation effects such as total ionizing dose (TID) and SEE. Effects from TID and SEE in semiconductor structures increase in severity with higher applied

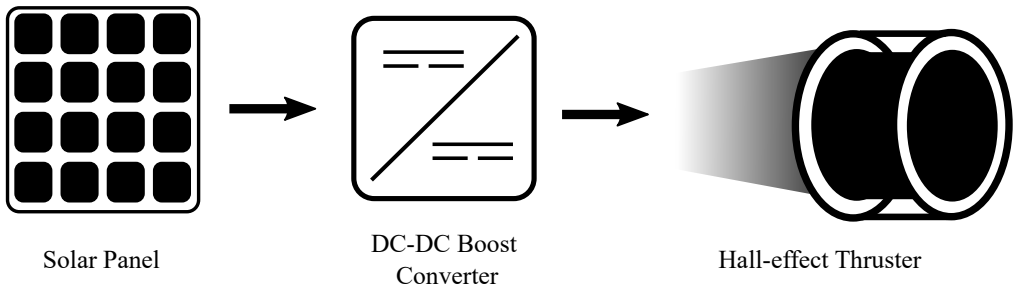

Figure 8.1: System level architecture showing the role of the dc-dc converter presented in this work.

drain-source voltage, limiting device availability for high voltage spacecraft converters [15]. Multilevel topologies allow for higher voltage outputs with lower switch stress, enabling radiation-tolerant, high voltage converters [92]. The FCML converter has shown success in terrestrial applications due to its high efficiency and power density [43],[93]. This work investigates the feasibility of implementing an FCML design for space applications, enabling high efficiency and density of converters for future spacecraft.

In particular, this work addresses the practical challenges of designing a high voltage FCML boost converter for space applications. Experimental results from a hardware design based on space-environment requirements are presented to validate the approach. The remainder of this paper is organized as follows: Section 8.2 provides design details of the gate driver power delivery approach, and the low inductance commutation loop. Following this, Section 8.3 provides experimental validation of the proposed concept through measured results of a high-density hardware prototype. Finally, Section 8.4 concludes the chapter.

8.2 Converter Design

GaN switches have been demonstrated to be extremely tolerant to TID and SEE, especially when compared with commercial Si or SiC FETS [15]. This work utilizes one such switch, the GaN Systems 100 V top-side cooled device as a fundamental building block for a radiation-hardened design, owing to the low $R_{ds,on}$ and a relatively resilient gate [94]. In the FCML boost converter, each switch is exposed to a maximum nominal (i.e. excluding any flying capacitor voltage ripple) drain-source voltage, $V_{ds,max}$, given by $V_{ds,max} = V_{out}/(N-1)$ [79]. With a conservative 2x safety margin, which has been shown to reduce SEEs, ($V_{ds,max}$= 50 V for the 100 V GaN device), a 10-level design can thus support an output voltage of 450 V. A schematic drawing of the proposed 10-level FCML boost converter is shown in Fig. 8.2.

A particular practical challenge of high-level-count FCML converters is the large number of switches that must be controlled, with careful timing. In this work, we employ a fully digital control implementation, utilizing the C2000 microcontroller to generate phase-shifted pulse width modulation (PSPWM) signals. The PSPWM control technique contributes to

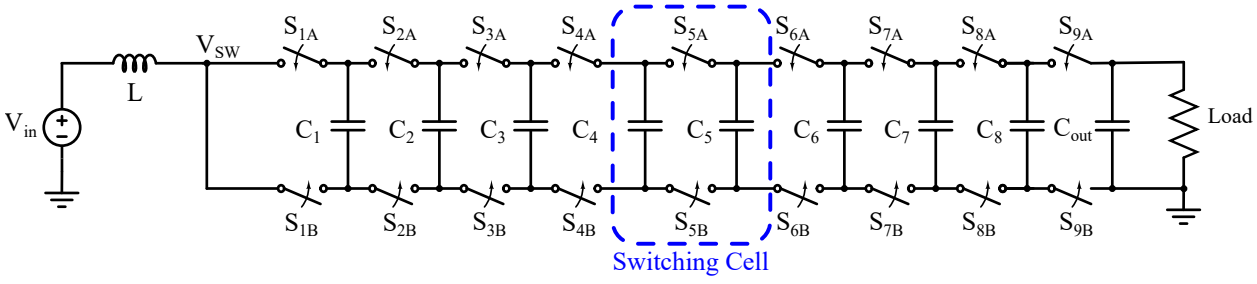

Figure 8.2: Schematic of 10-level flying capacitor multilevel boost converter.

natural capacitor balancing [63], which decreases the complexity of control.

One of the main advantages of the FCML topology is the reduction in the size of the inductor and filtering elements. The inductor is connected to the switch node which has an effective frequency of $(N-1) \times f_{sw}$, where f_{sw} is the switching frequency of each individual switch. Additionally, the magnitude of the switch-node voltage (labeled v_{sw} in Fig. 8.2), is $V_{out}/(N-1)$. This combination of increased effective frequency, and decreased voltage, yields an approximate (N-1) size reduction of the inductor, compared to a conventional boost converter [23], [79]. The decreased inductor size is particularly important for space applications, as the inductor is one of the heaviest components.

Cascaded bootstrap method

The FCML provides an attractive solution for high voltage conversion due to its low voltage stress on each switch. However, the gate drive presents a unique challenge as the converter relies on switches which are not referenced to ground. A common approach for providing power to the gate drive circuitry of multilevel converters is implementing dedicated isolated dc-dc converters for each gate driver [24]. This technique is particularly challenging in space environments, where compact isolated dc-dc integrated circuits rated for this harsh environment and high operating voltage are unavailable. Furthermore, discrete implementations of galvanically isolated power converters are prohibitively area and volume intensive. In this work, we explore the use of a cascaded bootstrap technique, which has been shown [56] to require relatively few discrete component and no dedicated dc-dc converters. Crucially, we exploit the fact that this technique is compatible with radiation environments, utilizing only capacitors, diodes, and low voltage low dropout regulators (LDOs). Fig. 8.3 shows a schematic drawing of the proposed gate drive method designed for the converter of Fig. 8.2. Here, a dual-sided gate driver is implemented for each switch pair, to reduce the total number of components. The supply voltage for each gate driver is generated from the bootstrap circuit, powered by a 15 V auxiliary supply, which is referenced to the bottom switch (S_{9B} as labeled in Fig. 8.2).

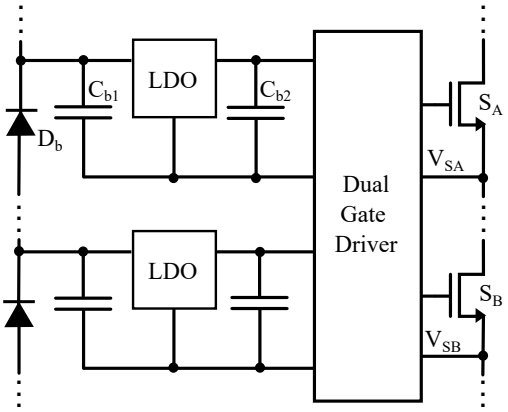

Figure 8.3: Schematic of the cascaded bootstrap circuit, showing one pair of complementary switches.

Commutation loop design

Owing to the large number of switches, and therefore switching transitions, in the the FCML converter, careful attention must be paid to the commutation loop inductance. Excessive commutation loop inductance leads to parasitic voltage ringing across the device drain-source terminals, which in addition to increased switching loss, reduces the device voltage margins and thus also the converter reliability. For the low-voltage GaN devices employed in this work, this is particularly challenging for two reasons: 1) A key benefit of the GaN transistors is their very fast switching speed, which will in turn increase the di/dt in the commutation loop, yielding higher voltage overshoot for a given parasitic inductance. 2) While the FCML converter can employ low-voltage devices, the switching cell itself (comprising two complementary switches and flying capacitors) must be rated to withstand voltages as high as the full output voltage - yielding stringent creepage and clearance requirements. In this work, we utilize a double-sided switching cell design, which exploits the greatly increased dielectric breakdown strength and creepage advantages of the FR-4 material of the printed circuit board (PCB) to allow for a simultaneously low inductance commutation loop, and high voltage rating. For applications requiring less stringent voltage clearances, single-sided commutation loops may also be advantageous, as demonstrated in [95]. Previous work, [65], has shown that an electrically thin design which relies on buried and blind vias to minimize the loop area can achieve both high voltage clearance and small loop inductance. However, buried vias can experience voiding and alignment issues which are detrimental in a vacuum and are difficult to inspect. Therefore, this work investigates a tight and minimized commutation loop which only relies on blind vias. The commutation loop schematic and implementation can be seen in Fig. 8.4.

To further decrease the commutation loop, the necessary flying capacitance for each level is split into a local capacitor, C_{loop}, and a larger capacitor, C_{bulk}. C_{loop} is positioned between switch levels allowing decreased spacing between levels, and is responsible for ensuring low

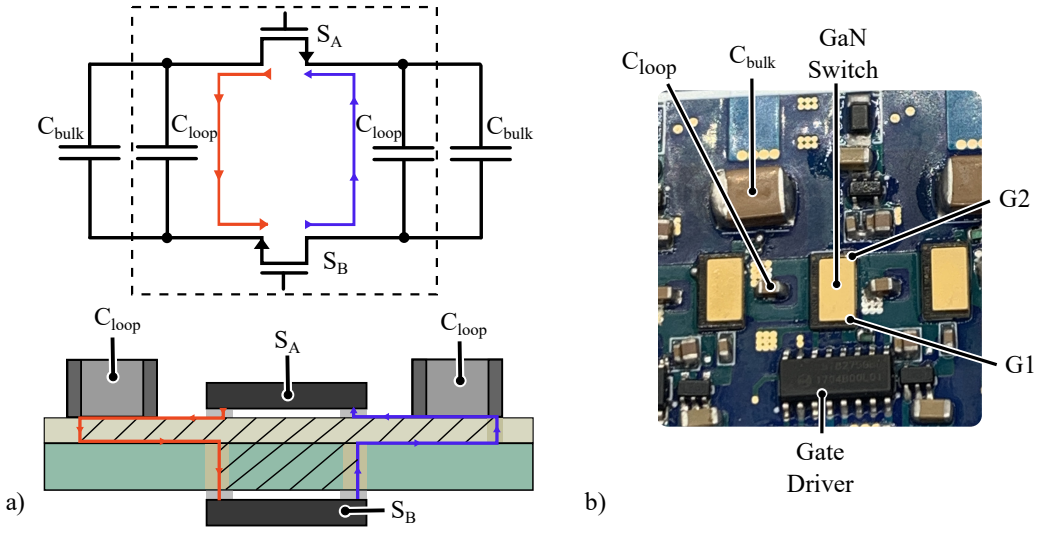

Figure 8.4: a) Commutation loop design using a modified electrically-thin layout with local small capacitors to minimize loop inductance. b) Focused view of commutation loop on top-side of hardware prototype.

commutation loop area, critical for high speed switching transitions. The larger (size and value) C_{bulk} capacitance is placed further away from the GaN switches where the large size does not increase the spacing between switches, but still supplies the necessary additional capacitance to the flying capacitors. During operation, capacitor C_{bulk} provides the bulk charge storage needed to transfer charge during a full switching period.

To experimentally validate the commutation loop performance, the drain-to-source of the GaN switches was measured during a switch transition. Although all commutation loops are identical, switch S_{9B} was chosen for this measurement, as its source voltage is ground referenced, enabling the use of a high bandwidth passive probe. The drain-to-source voltage was measured using a 700 MHz probe (Keysight N2894A) and a 1.5 GHz oscilloscope (Keysight MSOX4024A) to increase measurement accuracy. The switching waveform was captured while the converter was operating with a fixed duty ratio of 0.5, frequency of 80 kHz and input voltage and current of 75 V and 3 A respectively. The resulting waveform is shown in Fig. 8.5, with low overshoot and high ringing frequency (caused by the oscillation of the commutation loop inductance and parasitic drain-source capacitance of the switches).

The commutation loop inductance can be approximated by measuring the frequency of the ringing during the switch transition. As shown in [96], Eqn. 1 can be used to approximate the measured commutation loop inductance.

$$L_{com} = \frac{1}{(2\pi f_L)^2 C_{oss}} \tag{8.1}$$

In Eqn. 8.1, the C_{oss} is determined from the device datasheet. For the measured V_{DS} waveform shown in Fig. 8.5, the computed inductance is approximately 3 nH, enabling

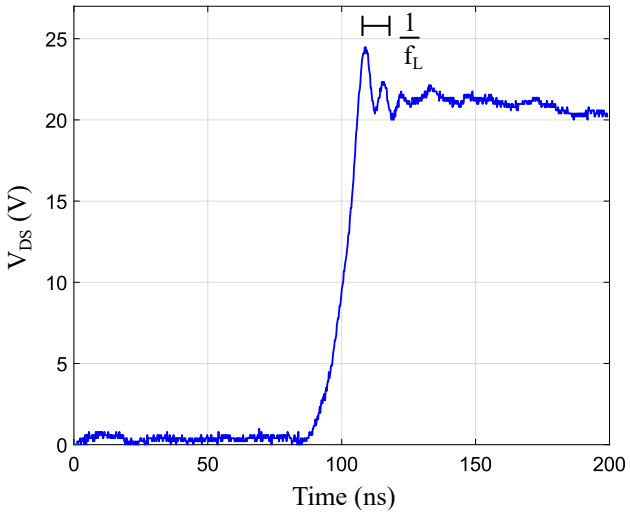

Figure 8.5: Measured V_{ds} of low-side switch during turn-off, the frequency of the ringing is used to approximate the commutation loop inductance.

fast switch transitions and low voltage overshoot. As demonstrated in [96], this technique provides a good match with impedance analyzer measurements of commutation loop inductances.

One advantage of the chosen GaN power transistor is the dual gate design. The device package allows for a gate signal routed on either the top or bottom of the package [97], shown as *G1* and *G2* in Fig. 8.4. To most effectively utilize the board area, the gate drivers for the odd levels (as labeled in Fig. 8.2) were placed below the device and driven by *G1* and the gate drivers for the even levels were placed above the devices and driven by *G2*. This allowed the overall converter box volume to be reduced since the gate driver package has the largest footprint of any component utilized in the design.

8.3 Converter Performance

The key components for this hardware demonstration are listed in Table 8.1.

Component	Part Number	Parameters
Switches	GaN Systems GS61008T	100 V
C_{loop}	TDK C0G	1 nF, 450 V
C_{bulk}	TDK X6S	2.2 μF, 450 V
Inductor	Coilcraft XAL1510	$10\mu H$
Gate Driver	Si8275	Dual-sided
LDO	LP2985IM5	6.1 V Output
C_{boot}	Murata X7R	22 μF, 25 V
D_{boot}	Vishay 2EFH02HM3	2 A, 200 V

Table 8.1: Component list for 10-level FCML boost design.

Description	Value
Input Voltage	20 V - 100 V
Output Voltage	200 V - 500 V
Output Power	1 kW
f_{sw}	80 kHz
Effective frequency	720 kHz
Peak Efficiency	99.1 %
Specific Power Density	24 kW/kg

Table 8.2: Performance summary.

The performance of the proposed design approach was validated with a high density dc-dc converter prototype with the overall performance summary provided in Table 8.2. An annotated photograph of the hardware prototype is shown in Fig. 8.6. As can be seen, care was taken to achieve a compact, low-profile design, as outlined in the white box area. For a device switching frequency of 80 kHz (corresponding to an effective switching frequency of 720 kHz at the switch node), hardware measurements were performed for two different conversion ratios, representing the smallest and largest step-up ratio of the intended application. Experimentally measured efficiencies for output voltages of 200 V and 500 V are provided in Fig. 8.7, which shows excellent efficiency across a wide load range. To achieve good accuracy in the measurements, a high precision power analyzer (Keysight PA2201A) was employed. It should be noted that all efficiency numbers also include the gate drive losses. Finally, the high efficiency was achieved despite relatively poor device utilization, owing to the approximately 2x voltage de-rating for the intended space applications.

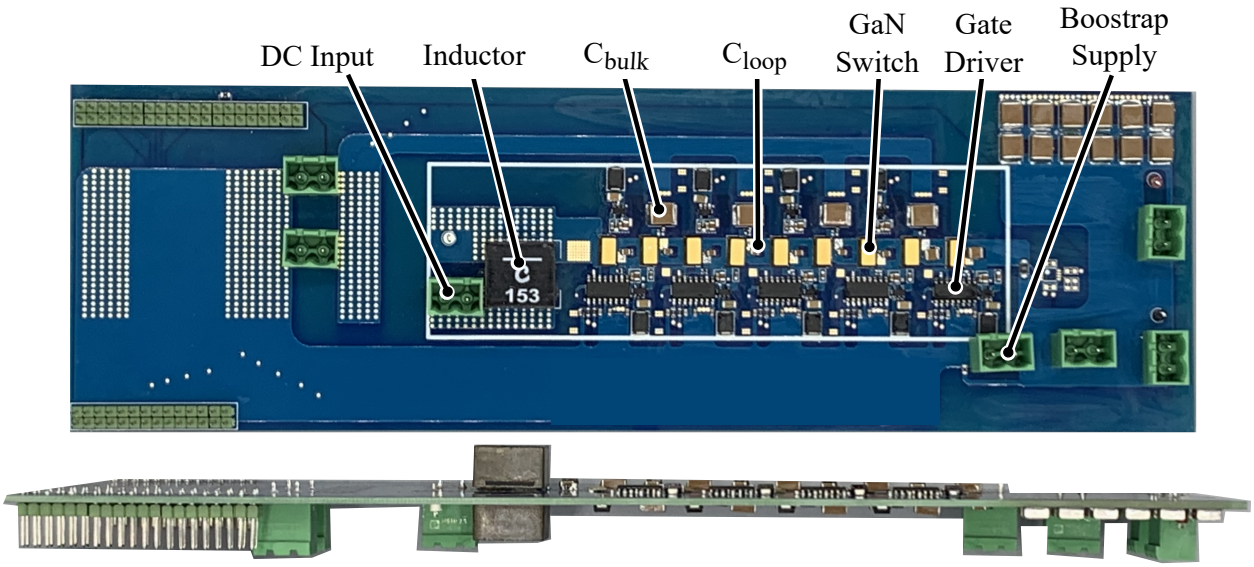

Figure 8.6: Top and side views of the hardware prototype.

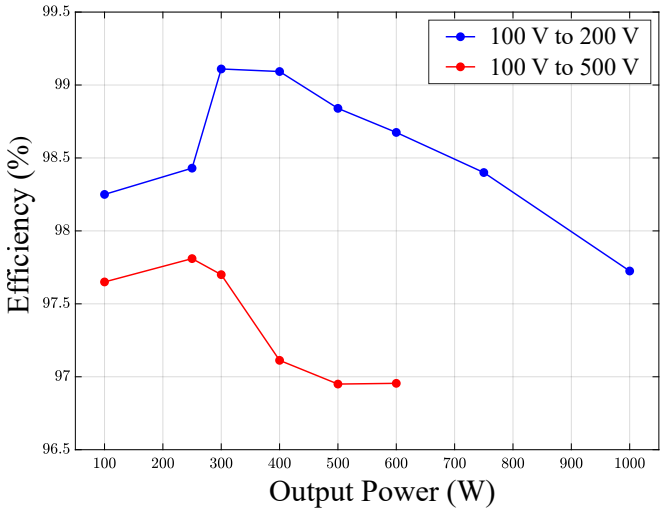

Figure 8.7: Measured efficiency of hardware prototype.

Loss Modeling

The losses at 1 kW were estimated using models proposed in [40] and [30], this breakdown is shown in Fig. 8.8. The dominant losses at this operating point are split between P_L, P_{con} and $P_{t_{on}}$. In this model the inductor losses, P_L, are calculated as a summation of the core loss, the ac losses and dc losses. The conduction losses, P_{con}, are dependent on the

GaN device's $R_{ds,on}$ and the current through the device while it is conducting. The turn-on and turn-off losses, $P_{t_{on}}$ and $P_{t_{off}}$, are dependent on the effective dead-time and the gate resistance.

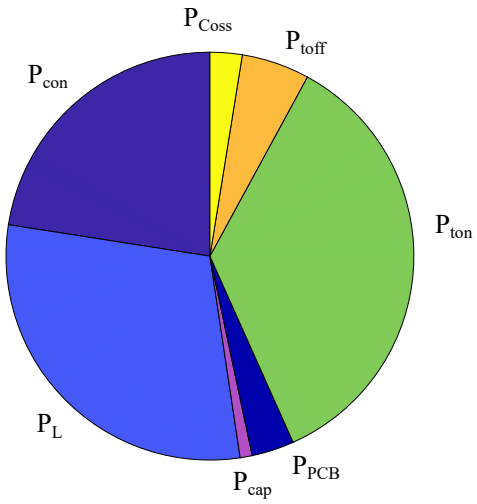

Figure 8.8: Loss breakdown at 1 kW, 100 V to 200 V conversion.

8.4 Conclusion

This work has shown the design methodology for a 10-level FCML. By focusing on a cascaded bootstrap technique, which reduces the component area, the converter weight and volume are minimized. The proposed commutation loop design enables a high voltage clearance, while minimizing the parasitic inductance which allows for increased performance. With these design techniques, a step-up dc-dc converter capable of over 99% efficiency is demonstrated in hardware and analyzed. This converter's demonstrated high efficiency and high power density makes it suitable for space applications.

Chapter 9

Composite Hybrid Switched-Capacitor Converter

9.1 Motivation

Innovations in robot design will allow further exploration of extreme terrain space landscapes, such as vertical lunar pits, lunar permanently shadowed regions, Martian slopes, or Enceladean oceans [98]–[100]. Many of these proposed systems require high-voltage dc tethers to connect the robots to a power source, allowing for efficient power transmission and light-weight cables [101]. As a result, the proposed robotic systems require an on-board dc-dc step-down converter capable of high conversion ratios as well as voltage regulation. However, designing power converters capable of withstanding hundreds of volts is difficult in space applications due to failures caused by radiation, which are more prominent with higher drain-to-source voltages in FET devices. As a result, multilevel topologies have shown promise in extreme radiation environments since they are capable of handling high voltages, while utilizing lower voltage devices [67], [92]. Moreover, GaN FETs have been shown to tolerate both total ionizing dose (TID) and single event effects (SEE) better than commercial Si and SiC devices [15]. Therefore, multilevel GaN-based topologies offer resilient solutions to harsh space environments.

The single-stage Sigma converter, whose structure is shown in Fig. 9.1, has shown very high power density and efficiency due to its use of partial power processing [102], [103]; relying on an isolated high-efficiency fixed-ratio LLC converter to deliver the majority of the power and a small buck-converter for regulation [104]. However, the LLC converter used in the Sigma architecture is not feasible in this application due to the high switch voltage rating required, which is greater than what is available in radiation-tested power devices. Thus, this work investigates the design of an isolated multilevel dc-dc converter for use in the same structure (series input/parallel output) for high-voltage step-down conversion. As shown in [6], the specific energy density of commercially available capacitors exceeds that of inductors by a factor of at least 1000×. Thereby motivating the use of hybrid switched-capacitor

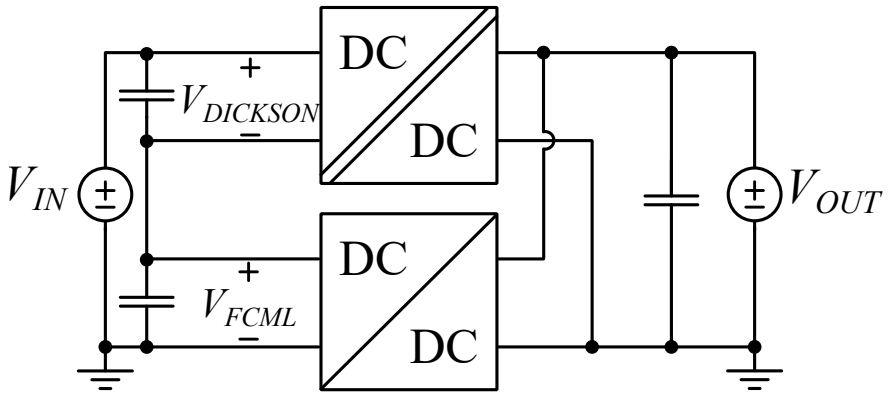

Figure 9.1: Configuration of a high step-down converter which utilizes partial power processing to achieve large conversion ratios and regulation.

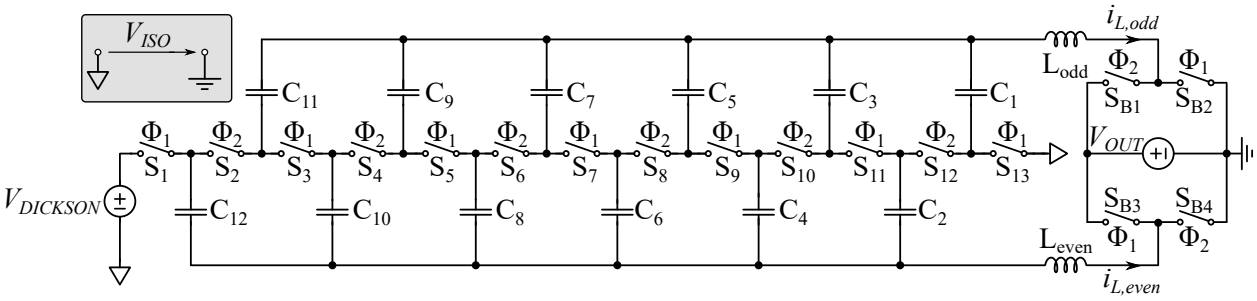

Figure 9.2: Capacitively-isolated Dickson converter, shown in 12:1 step-down configuration. As shown, the isolation voltage V_{ISO}, is defined as the voltage difference between the input and output negative potentials.

converter topologies which rely primarily on capacitors for light-weight energy transfer and storage.

One such topology, the capacitively-isolated Dickson converter [105], is a resonant hybrid switched-capacitor converter which for even conversion ratios can be operated with a 50% duty cycle and achieve complete soft-charging [106] on all flying capacitors. As shown in Fig. 9.2, this topology has a multilevel structure which results in switches experiencing a small fraction of the input voltage, making it ideal for space applications. In addition, the flying capacitors can provide voltage isolation allowing the converter to be used as the isolated dc-dc converter in the system architecture shown in Fig. 9.1.

Moreover, the regulating converter in the Sigma converter is typically implemented as a buck converter, which has high switch voltage stress and large magnetics which result in a large and heavy converter in this application. To reduce system mass, this work investigates the use of a flying capacitor multilevel (FCML) converter [10] to provide regulation. The FCML converter is a hybrid switched-capacitor converter which enables reduced switch stress

Table 9.1: Composite converter operating specifications.

Description	Parameter	Value
Input Voltage	V_{IN}	600-750 V
Output Voltage	V_{OUT}	50 V
Conversion Ratio Range	$N:1$	[12-15]:1
Optimized Power Level	P_{OUT}	350 W

and volt-second requirement on the inductor compared to a conventional buck converter, while still providing a wide regulation range, making it suitable in this composite converter.

The full system specifications can be seen in Table 9.1. As described above, the fixed-ratio Dickson converter is designed to process the majority of the power and is designed for 12:1 conversion ratio, Section 9.2 describes the design, optimization and performance of this converter. Section 9.3 describes the design of the FCML converter which allows for regulation with changing input voltage. Section 9.4 presents results for the full composite system, showcasing the system performance and regulation capabilities. Finally, Section 9.5 concludes the chapter.

9.2 Capacitively-Isolated Dickson Converter Design

The maximum input voltage (V_{IN}) of the system in Fig. 9.1 is 750 V. This voltage is designed to be split between $V_{DICKSON}$ and V_{FCML} as 600 V and 150 V, respectively. This division is determined such that at the lowest possible input voltage (600 V), the FCML converter is processing no power. Therefore, the proposed Dickson converter operates with a 12:1 conversion ratio, and requires an isolation voltage equal to V_{FCML}, or 150 V in this design. This isolation voltage is highlighted in Fig. 9.2 as V_{ISO}, defined as the difference between the input and output negative terminals. A summary of the fixed-ratio Dickson converter operating specifications is shown in Table 9.2.

Converter Operation

A Dickson converter with level count and nominal conversion ratio of N_D, where N_D is even, is operated with two phases and a 50% duty cycle. The switches are controlled to be conducting in either phase one or two, denoted as Φ_1 and Φ_2 in Fig. 9.2. The converter operates as a resonant LC tank converter, where, if all the flying capacitors are equal and defined as C_0, and the inductors are both equal to L_0, then the two phases have the same resonant frequency defined as f_{res}.

$$f_{res} = \frac{1}{2\pi\sqrt{L_0 C_0 (N_D/2)}} \tag{9.1}$$

Table 9.2: Capacitively-isolated Dickson converter operating specifications.

Description	Parameter	Value
Input Voltage	$V_{DICKSON}$	600 V
Output Voltage	V_{OUT}	50 V
Conversion Ratio	$N_D : 1$	12:1
Isolation Voltage	V_{ISO}	150 V
Optimized Power Level	P_{OUT}	250 W
Resonant Frequency	f_{res}	107 kHz

This analysis is only valid for even conversion ratios, as odd conversion ratios are possible but require more complex split-phase timing to achieve complete capacitor soft-charging [107], [108].

Flying Capacitor Selection

Charge flow analysis [81] shows equal charge through all flying capacitors. As a result, for equal capacitance, and using the relationship $Q = CV$, the peak-to-peak ripple across each flying capacitor, Δv_{pp}, is also equal. Using KVL analysis, the dc average voltage for each capacitor can be found to be equal to $V_{C,i}$.

$$V_{C,i} = V_{ISO} + \frac{i \times V_{DICKSON}}{N_D} \tag{9.2}$$

The parameter i is the index of the capacitor as shown in Fig. 9.2. Note, the mid-range voltage of each flying capacitor is dependent on the required isolation voltage and therefore optimal flying capacitance sizing will also depend on the isolation voltage.

Switch Requirements

It can be shown through KVL analysis that the middle switches in the string, $S_{[2-12]}$ as shown in Fig. 9.2, need to block two times the output voltage, V_{OUT}. However, the first and last switch in the string (S_1 and S_{13}) as well as the bridge switches ($S_{B[1-4]}$), only need to block V_{OUT}. Equation 9.3 summarizes the nominal voltage blocking requirement for each switch in this topology.

$$v_{ds,k} = \begin{cases} 2 \cdot V_{OUT} & \text{for } \; k = [1, 12] \\ V_{OUT} & \text{for } \; k = [2...N_D] \\ V_{OUT} & \text{for } \; k = B[1-4] \end{cases} \tag{9.3}$$

The parameter k is the index of the switch as defined in Fig. 9.2. As space applications depend on low voltage stress to decrease failures caused by radiation effects, this low switch stress is beneficial for robust design.

As is typical with tank-based converters [60], the capacitor voltage ripple does not appear across adjacent switches and is imposed on inductors L_{odd} and L_{even} only. Therefore, the switch voltage is independent of selected capacitance and load current. Consequently, the capacitors can be sized for optimal ripple independent of switch voltage stress requirements. The following section discusses an optimization method for selecting the capacitance and inductance values which correspond to the minimal passive component mass.

Design and Optimization

Passive Component Optimization

Understanding the trade-offs between capacitor and inductor sizing in hybrid switched-capacitor converters is vital for minimizing the overall mass of the converter. Previous work in [109] introduced a method for optimally sizing capacitors and inductors for minimized total passive volume in a procedure which can be applied to any resonant hybrid switched-capacitor topology. In this optimization scheme the maximum energy storage requirement for the flying capacitors and inductors is calculated using the peak voltage and current, respectively, for each component. Then the energy density of the passive components is used to estimate passive volume.

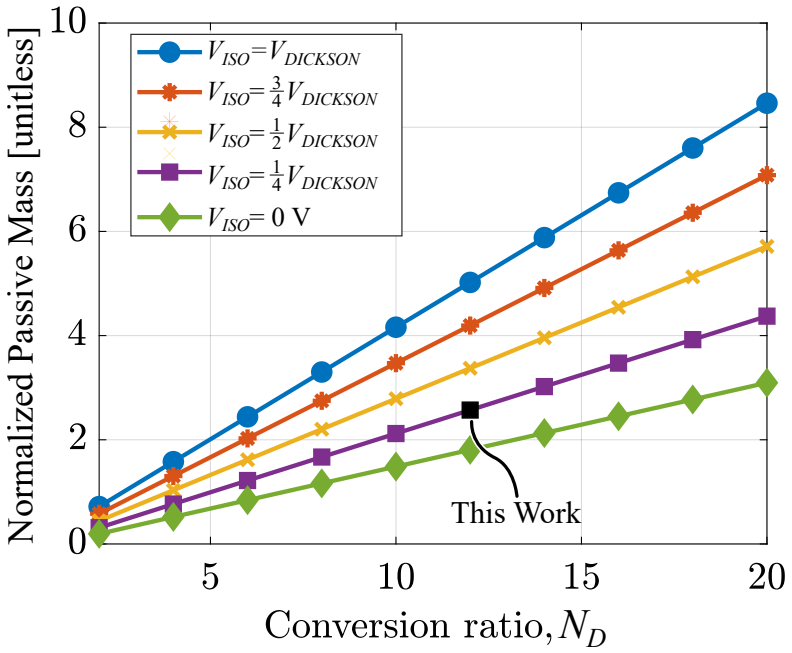

Figure 9.3: Optimized total passive component mass (flying capacitors and inductors) of the capacitively-isolated Dickson converter as a function of fixed-conversion ratio. The total passive mass increases with increased isolation voltage and conversion ratio.

However, this work focuses on space applications where mass is often more critical than volume. Therefore in this work, a modified version of the optimization in [109] is applied, instead optimizing around the total passive component mass. Using the volume to mass transformation proposed in [6], the specific energy density (measured in $\frac{\mu J}{mg}$) of commercially available capacitors (γ_C) and inductors (γ_L) was approximated and used in the modified optimization. The resulting minimum achievable total passive component mass for this topology is shown in Fig. 9.3. Here the total passive component mass is a function of conversion ratio and required isolation voltage, V_{ISO}. This is expected as the maximum voltage on the flying capacitors increases with increasing isolation voltage.

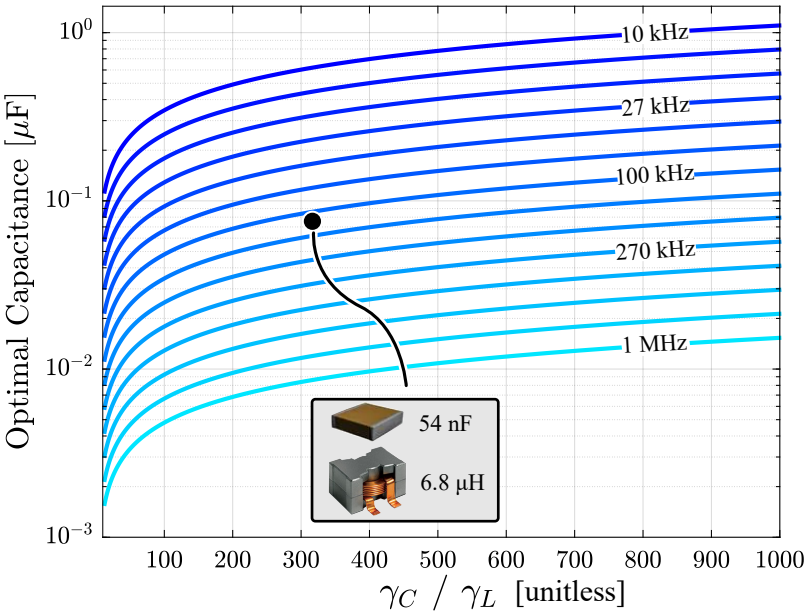

Figure 9.4: The optimal flying capacitance for the capacitively-isolated Dickson converter as a function of switching frequency and relative specific energy density of capacitors (γ_C) and inductors (γ_L). The selected design is shown, based on components with a relative specific energy density (γ_C/γ_L) of 317 and resonant frequency of 107 kHz.

Additionally, the relative energy density is integral to the optimization, as the optimal capacitance will increase and inductance will decrease for an increased γ_C/γ_L ratio. Since this converter is designed to operate at resonance, choosing passive components with stable capacitance and inductance over all operating conditions is preferable, otherwise advanced sensing and control is necessary to maintain resonant operation [110]. As a result, only Class I multilayer ceramic capacitors (MLCCs) and shielded ferrite core inductors were considered in the component optimization. Since Class I MLCCs have significantly lower specific energy density compared to Class II MLCCs and the energy density of commercially available capacitors decreases above 600 V, the relative passive specific energy densities (γ_C/γ_L) is approximated to 100 (compared to approximately 1000 when using Class II MLCCs at lower voltages).

Subsequently, the passive component optimization considers the converter operating parameters and this approximated γ_C/γ_L ratio. Once an optimal flying capacitance and inductance were calculated, real components were selected to closely match the optimal solution, then a new γ_C/γ_L was determined based on these real components. This process was repeated iteratively until values for the ideal optimized components and the real components available matched closely. Figure 9.4 shows how the optimal capacitance varies as a function of γ_C/γ_L and desired resonant frequency. In this design, the resonant frequency was set to

Table 9.3: Components selected for Capacitively-Isolated Dickson converter hardware prototype.

Component	Part Number	Description
C_{1-12}	KEMET C0G	18 nF (x3), 1.7 kV
$L_{even/odd}$	Coilcraft	6.8 μH, 22 A
S_{1-13}	EPC 2050	350 V, 80 mΩ
$S_{B[1-4]}$	GS61008T	100 V, 7 mΩ
Gate Driver	LMG1020	5 V, 7 A / 5 A
Isolator	ADUM5240	Power and Signal

be approximately 100 kHz, based on the selected switches and expected losses. The selected passive design is marked in Fig. 9.4, where the relative specific energy density of the selected components is 317 and the resonant frequency is approximately 107 kHz. The component values and ratings are shown in Table 9.3.

Capacitively-Isolated Dickson Converter Hardware Results

Using the optimization described above, a hardware prototype was designed, shown in the annotated photograph of Fig. 9.5. The designed printed circuit board (PCB) is dual-sided and the inductors are placed on the backside of the board. For the string switches (S_{1-13}), 350 V GaN devices are implemented (as described in Table 9.3), even though each of these switches requires only 100 V blocking (as shown in Eqn. 9.3). Similarly, the bridge switches ($S_{B[1-4]}$) are designed with 100 V rated devices, but only require 50 V blocking. Therefore, for all switches in this design a conservative derating ($\geq$ 50%) is applied which aids in reducing SEE in high radiation environments [15].

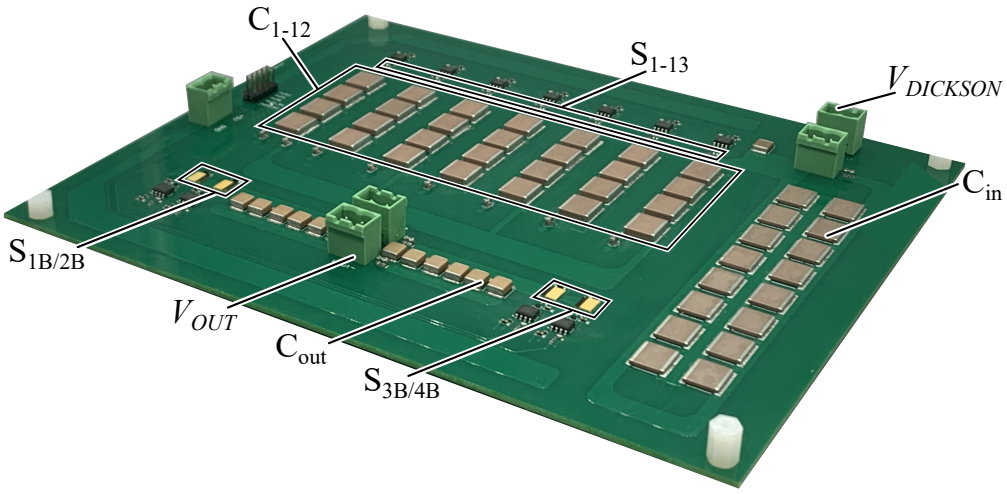

Figure 9.5: Fixed-ratio 12:1 capacitively-isolated Dickson hardware prototype. The inductors are placed on the back of the board below $S_{B[1-4]}$.

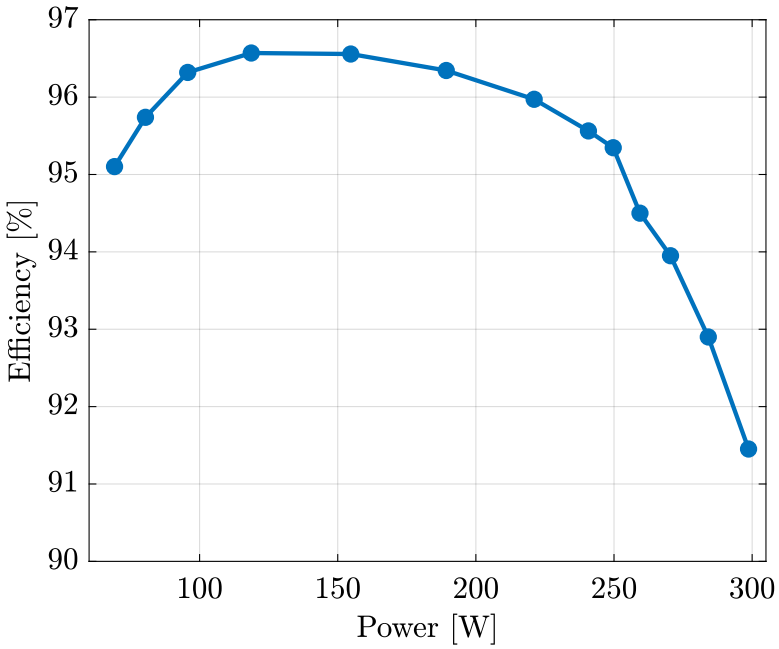

Figure 9.6: Measured efficiency of capacitively-isolated Dickson converter hardware prototype, over a range of output power with a fixed 600 V input ($V_{DICKSON}$).

For an input voltage ($V_{DICKSON}$) of 600 V, the measured efficiency can be seen in Fig. 9.6, where the peak efficiency was measured to be 96.6%. Note, the measured efficiency does

not include gate drive loss as the system's gate drive circuitry was not optimized. Table 9.3 shows the components used for gate drive, including signal and power isolation, but this circuitry is not radiation hardened. Future work is required to design an efficient gate drive system suitable for the space environment.

An approximate loss breakdown for the converter operating at 250 W is shown in Fig. 9.7. Note, the majority of the losses come from the inductors which experience large sinusoidal currents, as depicted in Fig. 9.8. As this system was optimized for minimized mass, future work may investigate methods to increase overall efficiency.

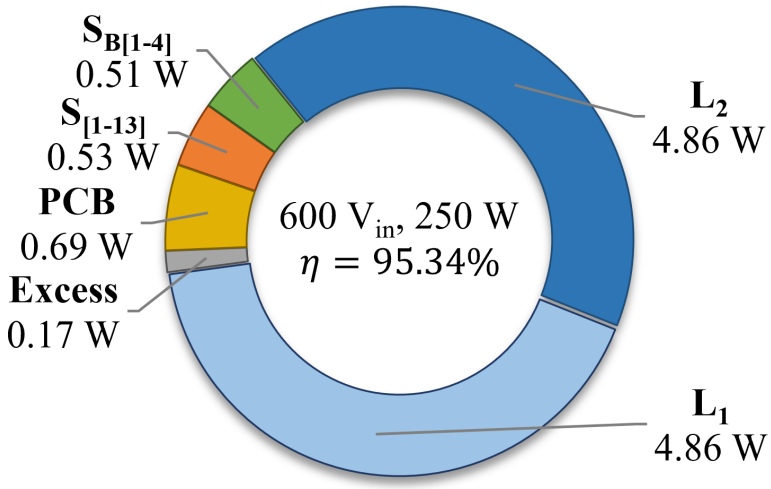

Figure 9.7: Estimated capacitively-isolated Dickson converter loss breakdown for 600 V input, 250 W delivered at 95.34% efficient.

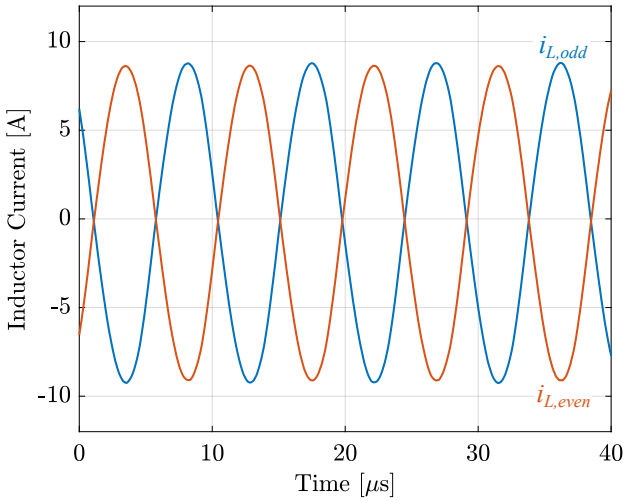

Figure 9.8: Measured inductor currents in the capacitively-isolated Dickson converter, operating at 600 V input and 250 W output power.

Switch Voltage Stress

As described in Section 9.2, the voltage stress on the switches is not dependent on load current nor on capacitor voltage ripple, allowing the use of lower voltage switches. To verify this, the two highest voltage capacitors (labeled C_{11} and C_{12} in Fig. 9.2) and the drain-to-source voltage of the three highest potential switches (labeled S_{1-3} in Fig. 9.2) were measured at two different load conditions, as shown in Fig. 9.9. These measured results verify that as the load increases, the capacitor ripple also increases, however the switch blocking voltage does not increase.

Isolation Testing

The flying capacitor voltages, as can be seen in Fig. 9.10 were measured with differential voltage probes. The even distribution of the mid-range voltages as well as the sinusoidal voltage ripple further confirm both intended resonant operation and complete soft-charging of all flying capacitors. To confirm capacitive isolation capability, the converter was tested with the desired system isolation of 150 V. For this test, the input ground and output ground were disconnected and a power supply was placed between the two terminals to apply the isolation bias. The capacitor voltages were measured before and after isolation bias voltage was applied, as shown in Fig. 9.10. In agreement with Eqn. 9.2, when the isolation voltage is zero, the lowest flying capacitor has a mid-range voltage of 0 V. However, with isolation

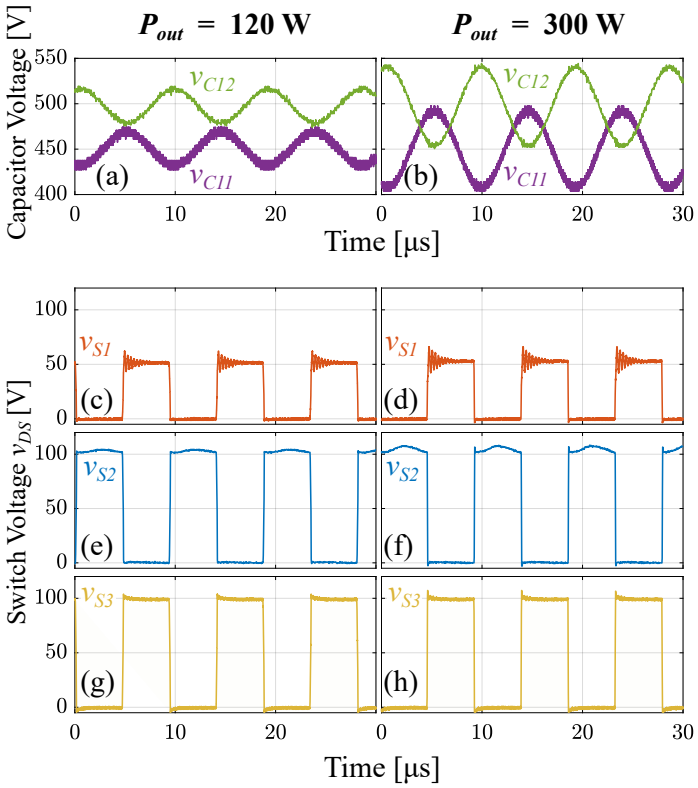

Figure 9.9: Measured operating waveforms of capacitively-isolated Dickson converter (Fig. 9.2) at peak efficiency, 120 W, and heavy load, 300 W. As shown in (a) and (b) as the load increases the capacitor peak-to-peak voltage increases. However, as shown in subfigures (c)-(h) the drain-to-source voltage of the switches does not experience substantial increased ripple, allowing the use of lower voltage devices, independent of load condition.

voltage applied, the lowest capacitor has a mid-range voltage equal to the isolation voltage. Similarly, the voltage of all of the flying capacitors increases by V_{ISO} as shown in Fig. 9.10b.

9.3 Regulating FCML Converter Design

The FCML converter is selected in this work due to its low switch stress and reduced inductor requirements when compared to the conventional buck converter. In the FCML converter each switch blocks a fraction of the input voltage $\frac{V_{FCML}}{N_F-1}$, neglecting capacitor voltage ripple, where N_F is the level count of the FCML converter. This reduced switch voltage stress allows for the use of lower voltage devices which tend to exhibit better figures of merit [12], [14].

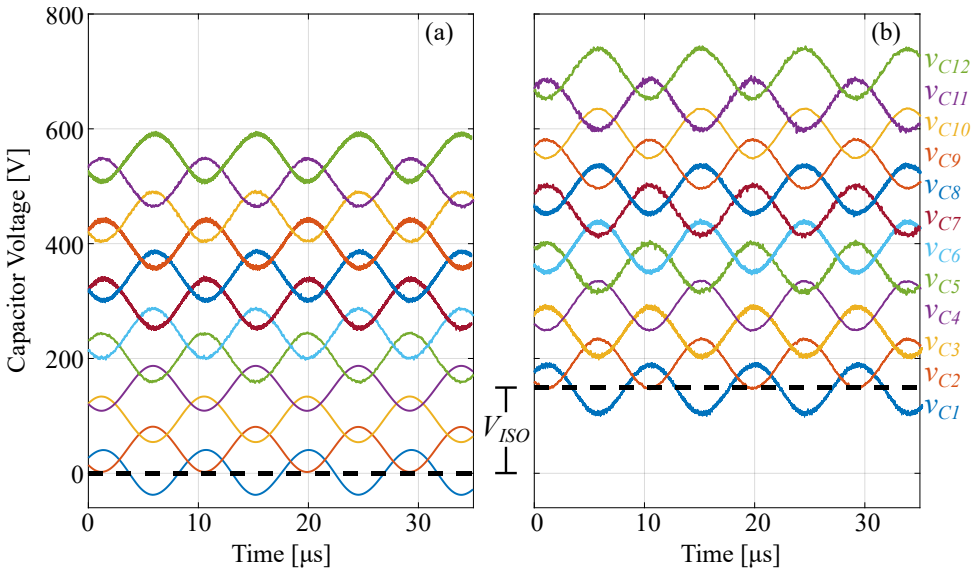

Figure 9.10: Flying capacitor voltages in the capacitively-isolated Dickson converter measured with 600 V input and 250 W output power. a) Measured capacitor voltages with no isolation voltage applied. b) Measured capacitor voltages with 150 V isolation voltage applied.

Table 9.4: Regulating FCML converter operating specifications.

Description	Parameter	Value
Input Voltage	V_{FCML}	50-150 V
Output Voltage	V_{OUT}	50 V
Duty Cycle	D_{FCML}	0.25-1
Optimized Power Level	P_{OUT}	100 W
Switching Frequency	f_{sw}	100 kHz

FCML Converter Operation

This work and following analysis investigates a regulating FCML converter using phase-shifted pulse width modulation (PS-PWM), where each switch operates with a duty cycle (D) and is phase-shifted by $\frac{360^o}{N_F-1}$ [111], [112]. Furthermore, the inductor has an effective switching frequency $f_{sw} \times (N_F - 1)$. Therefore, the inductor has reduced volt-second requirement due to the increased effective switching frequency and decreased voltage across its terminals.

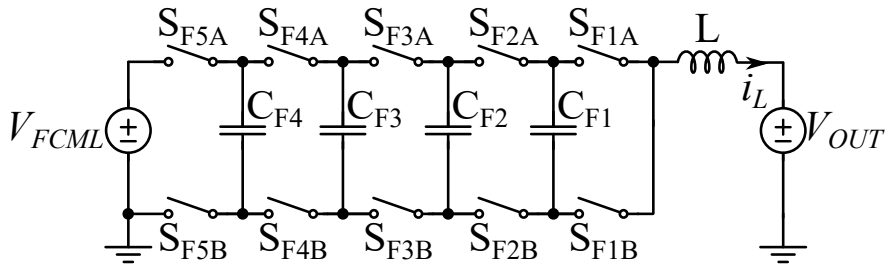

Figure 9.11: Schematic of regulating six-level FCML converter, chosen as the optimal level count to minimize the total passive mass.

Converter Design

For this regulating FCML converter, the operating specifications are shown in Table 9.4. The converter must be able to operate over a wide-range of duty cycles to provide regulation for the full system.

Passive Component Selection

Previous work has determined the level count and passive component selection for a regulating FCML converter using loss models and pareto-front optimizations, typically assuming low-ripple conditions on the passive components [113], [114]. Due to the mass critical application considered in this work, the level-count and passive sizing is instead determined using the peak energy stored in each component to minimize total passive mass, similar to the method described in Section 9.2 for the Dickson converter. In this optimization, it is assumed that the FCML converter is operating significantly above resonance, controlled with PS-PWM and all the flying capacitors are equivalent. Moreover, as the converter is operating well above resonance, and is therefore less sensitive to component variation, Class II MLCCs are used, thereby increasing the ratio between the capacitor and inductor specific energy density (γ_C/γ_L) to 667. This optimization method allows for level count selection which results in minimized passive component mass. For the converter operating specifications shown in Table 9.4, a six-level FCML converter results in a minimized passive component mass. A corresponding schematic drawing of a six-level FCML converter is shown in Fig. 9.11. Figure 9.12 shows the total minimal passive mass for a six-level FCML converter and a typical buck converter (operating in boundary conduction mode as it results in minimized passive mass), showcasing the decreased passive mass of a FCML converter compared to a conventional buck converter.

The peak energy stored in the inductor is dependent on the inductor current ripple, which is defined in [115] and shown in Eqn. 9.4.

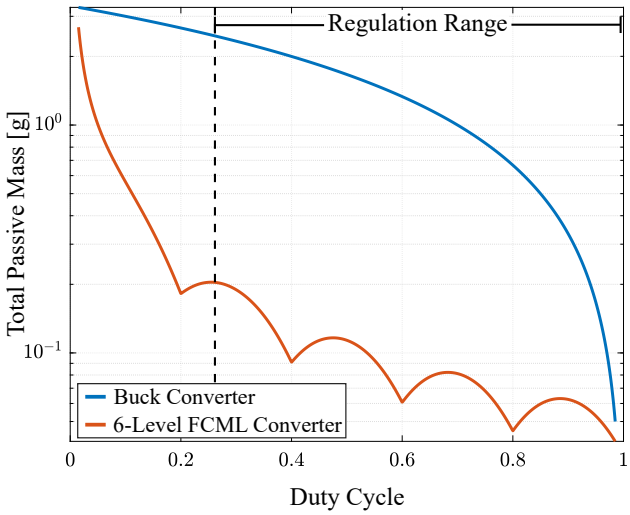

Figure 9.12: Comparison of optimized total passive mass for a six-level FCML converter and a buck converter (operating in boundary conduction mode). Optimization is performed for the operating conditions described in Table 9.4. The range of regulation is annotated, and the worst-case duty cycle of 0.25 is used for the passive component design.

$$\Delta i_{L_{pp}} = \frac{1}{L}\frac{(1-D_{eff})D_{eff}}{f_{SW}(N_F-1)^2}V_{FCML} \tag{9.4}$$

Where the effective duty cycle (D_{eff}), the duty cycle seen by the inductor, is defined as shown in Eqn. 9.5.

$$D_{eff} = D(N_F-1) - floor(D(N_F-1)) \tag{9.5}$$

As D_{eff} approaches zero the inductor current ripple also approaches zero. Therefore, for any given level count there are certain duty ratios which result in minimized energy storage requirements in the inductor and thus reduced total passive mass. This can be seen reflected in Fig. 9.12, where the local minima occur.

As this converter is designed to operate over a wide regulation range, the components are selected to handle the peak energy required during the worst-case duty cycle, which for the six-level FCML converter shown here occurs at $D = 0.25$. The passive mass for the converter at this duty cycle is shown in Fig. 9.13 as a function of flying capacitance. The passive components (Table 9.5) were selected which result in a minimal total passive mass.

Regulating FCML Converter Hardware Results

The six-level FCML converter was designed using the optimal passive components and other circuit components listed in Table 9.5. Figure 9.14 shows an annotated photograph of the FCML converter. The efficiency of the regulating FCML converter hardware prototype is

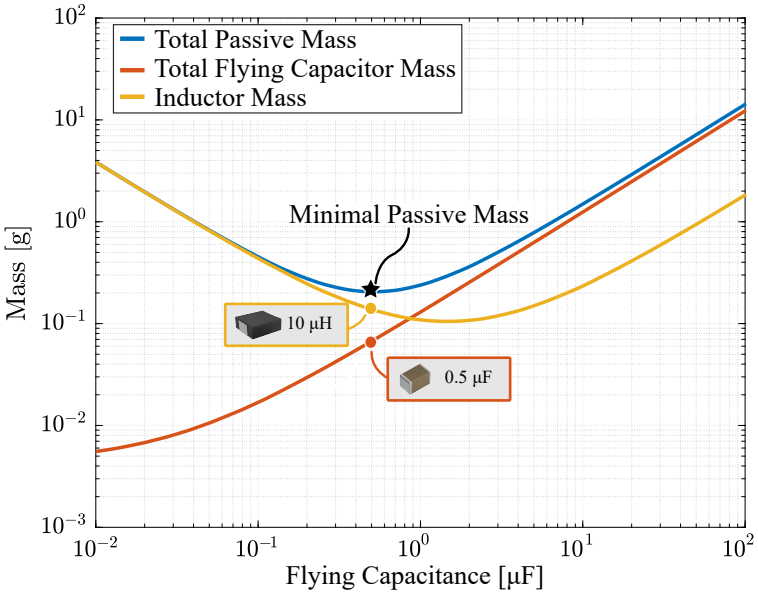

Figure 9.13: Mass of the flying capacitors, inductor and combined total passive mass for a six-level FCML converter swept over flying capacitance values. This analysis is performed under the operating conditions described in Table 9.4 and the worst-case duty cycle shown in Fig. 9.12. The minimal mass is used to select the flying capacitance and inductance used in design.

Table 9.5: Components selected for regulating FCML converter hardware prototype.

Component	Part Number	Description
$C_{F[1-4]}$	TDK CGA	0.1 μF (x5), 350 V
L	Vishay IHLP	10 μH, 2.3 A
$S_{F[1-4]A/B}$	EPC 2218	100 V, 3.2 mΩ
Gate Driver	LMG1020	5 V, 7 A / 5 A
Isolator	ADUM5240	Power and Signal

shown in Fig. 9.15. The peak measured efficiency occurs when the FCML duty ratio is highest (corresponding to the lowest step-down requirement), however the efficiency remains high over the wide range of input voltages (V_{FCML}).

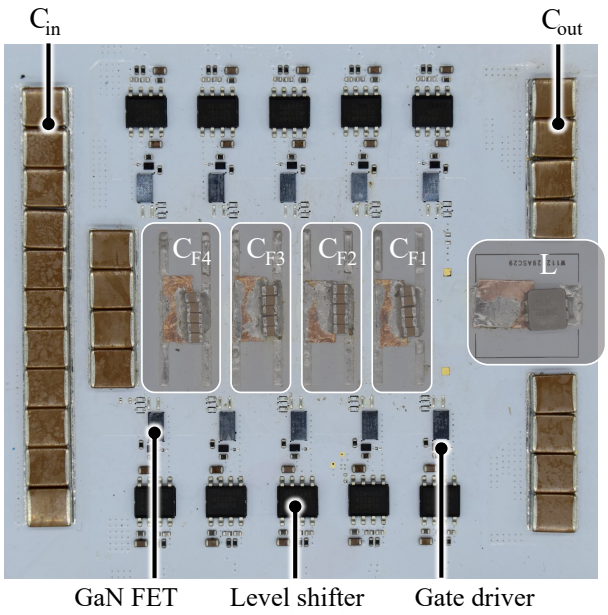

Figure 9.14: Annotated photograph of the FCML converter used to validate the passive volume calculations. Constructed on a white soldermask, the hardware presented in [116] is modified to include the passive component cases depicted in Fig. 9.13.

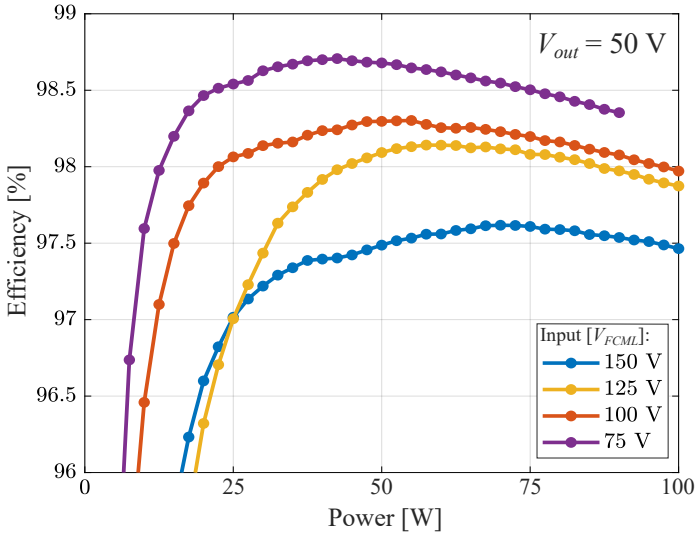

Figure 9.15: Measured efficiency of FCML converter, with a fixed 50 V output and varying input voltages, showcasing the full range of regulation. Note: When the input voltage is 75 V, the output power is limited by the allowable capacitor voltage ripple.

Dickson Converter: 96.42g
Fixed-ratio Stage

FCML Converter: 0.69g
Regulating Stage

Figure 9.16: Photograph of passive components utilized in the hardware prototype. Components are chosen to minimize total passive mass in the Dickson converter and FCML converter. The passive components are shown in the same scale, and highlights the small volume and weight of the FCML converter which is designed to process minimal power.

9.4 Composite Converter Operation

The fixed-ratio Dickson converter and regulating FCML converter are connected with a series-input/parallel-output as shown in Fig. 9.1 to complete the full composite system. A photograph of the passive components of the Dickson converter and the FCML converter is shown in Fig. 9.16. This figure highlights the optimized total passive mass of each subsystem, and the comparative sizes of each converter. The FCML converter passive components are approximately 140 times lighter than the fixed-ratio Dickson converter. This showcases the partial power processing concept as the Dickson converter is designed to operate with three times the power and four times the conversion ratio of the FCML converter.

System Model

The steady-state operation of the composite converter can be modeled as shown in Fig. 9.17. In this model, the Dickson converter is modeled with an ideal conversion ratio, N_D and an output impedance of R_D accounting for non-negligable losses at high output powers. Moreover, the regulating FCML converter can be modeled with a conversion ratio of $\frac{1}{D}$. In this work, the output impedance of the FCML converter is neglected as the converter processes much less power than the Dickson converter and has lower overall losses.

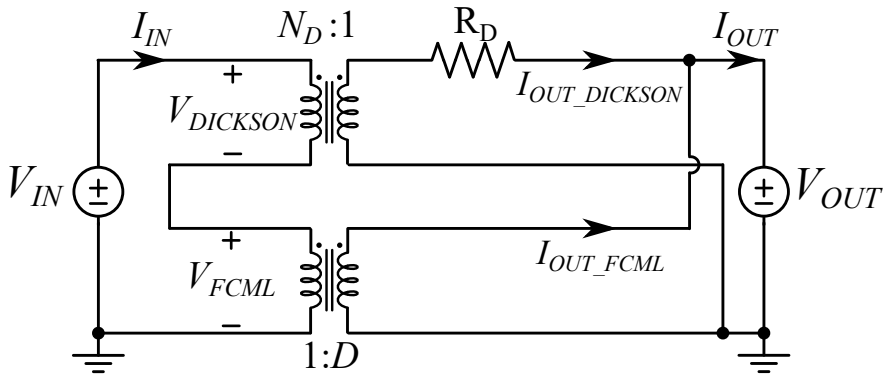

Figure 9.17: Steady-state model of composite converter. The output impedance of the Dickson converter is modeled as R_D.

Using this model, the input voltage can be written as a sum of each converter's input voltage as shown in Eqn. 9.6.

$$V_{IN} = V_{DICKSON} + V_{FCML} \tag{9.6}$$

Then, the input voltage can be expressed as a function of the output voltage using the conversion ratio of each converter, accounting for the output impedance of the Dickson converter as shown in Eqn. 9.7.

$$V_{IN} = N_D(V_{OUT} + I_{IN}N_D R_D) + \frac{1}{D}V_{OUT} \tag{9.7}$$

Finally, the duty ratio can be solved for as a function of operating conditions and the Dickson converter conversion ratio as shown in Eqn. 9.8.

$$\frac{1}{D} = \frac{V_{IN}}{V_{OUT}} - (N_D + \frac{N_D I_{IN}}{\frac{V_{OUT}}{N_D R_D}}) \tag{9.8}$$

Equation 9.8 provides the necessary duty cycle of the FCML converter based on a set of operating conditions.

Measured Dickson Converter Output Impedance

The output impedance of the Dickson converter was measured, over a range of output currents, as shown in Fig. 9.18. As the output current increases the resistance R_D also increases, which is due to non-linear losses in the converter such as the inductor core loss. This output resistance also results in a non-ideal conversion ratio of the Dickson converter, further requiring the regulation provided by the FCML converter in this system.

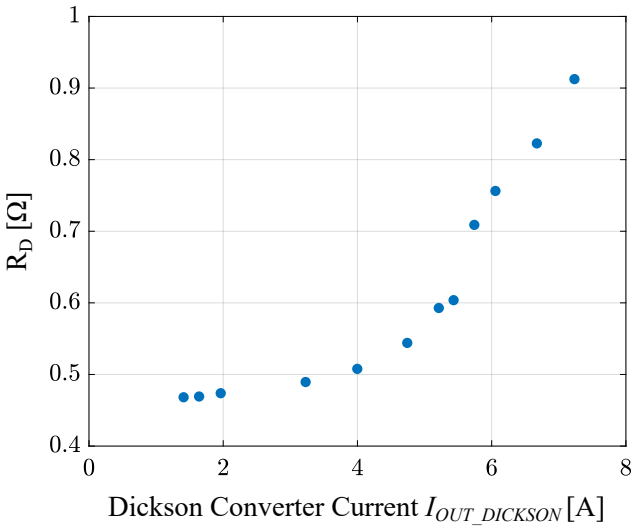

Figure 9.18: The measured output impedance for the Dickson converter over a range of output currents with a fixed 600 V input ($V_{DICKSON}$).

FCML Converter Control

As shown in Eqn. 9.8, the necessary regulation of the FCML converter is dependent on load conditions and input/output voltages. For example, given a 750 V input (V_{IN}) and a desired set point of 50 V at the output (V_{OUT}), the necessary duty cycle is shown as a function of load in Fig. 9.19.

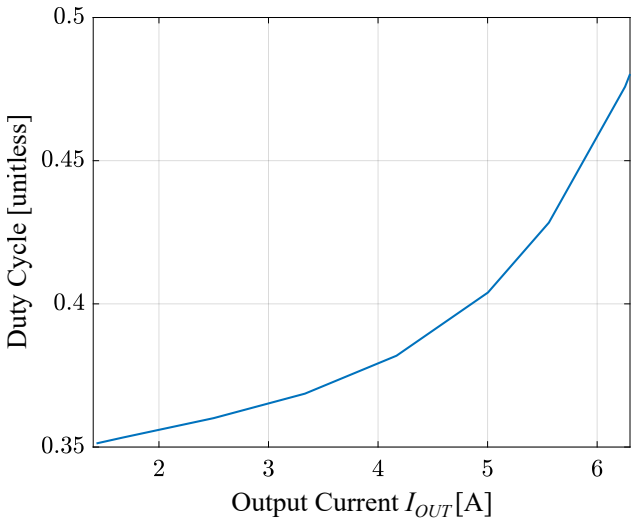

Figure 9.19: The required duty cycle (D) of the FCML converter to maintain a fixed 50 V output voltage (V_{OUT}), given a 750 V input voltage (V_{IN}) over a range of load conditions.

In this work, output regulation is achieved with voltage-mode control sensing the output voltage (V_{OUT}), as it requires less complex circuitry compared to sensing the input/output currents or the high-voltage at the system input. Using a simple PI controller (where $k_p = 1 \times 10^{-4}$ and $k_i = 1 \times 10^{-3}$) implemented on a Texas Instruments F28379D microcontroller, the FCML converter duty cycle is updated at a frequency of 10 kHz, which is approximately 10 times slower than the switching frequency of either discrete converter.

Using this controller, the modeled and experimentally measured Dickson converter ($V_{DICKSON}$) and FCML converter (V_{FCML}) input voltages for a regulated 50 V output voltage (V_{OUT}), given a 750 V input voltage (V_{IN}) over a range of load conditions are shown in Fig. 9.20. This verifies that the controller operation in steady-state matches the model closely.

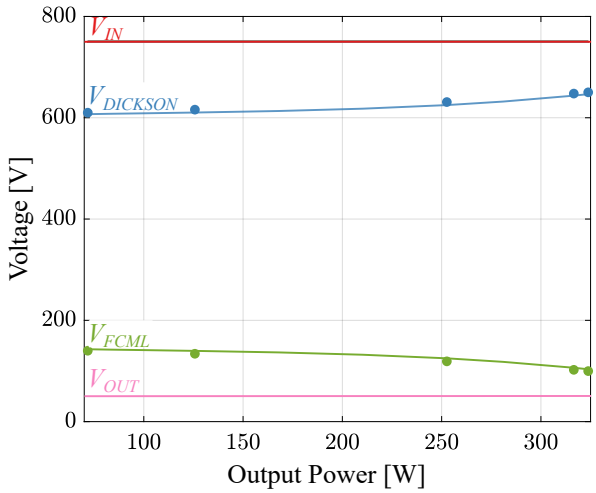

Figure 9.20: The modeled Dickson converter ($V_{DICKSON}$) and FCML converter (V_{FCML}) input voltages for a regulated 50 V output voltage (V_{OUT}), given a 750 V input voltage (V_{IN}) over a range of load conditions. The discrete data points show experimentally collected data, which match closely with the model.

Full System Performance

The efficiency of the full system is shown in Fig. 9.21-a, for a fixed 750 V input (V_{IN}) regulated to a 50 V output (V_{OUT}). The peak system efficiency measured is 96.7% for the nominal 15:1 conversion ratio with regulation enabled. The power delivered by each converter is shown in Fig. 9.21-b. Fig. 9.22-a/b show the input voltage split of the composite structure at 125 W and 325 W, showcasing the regulation capability of the converter under different operating conditions.

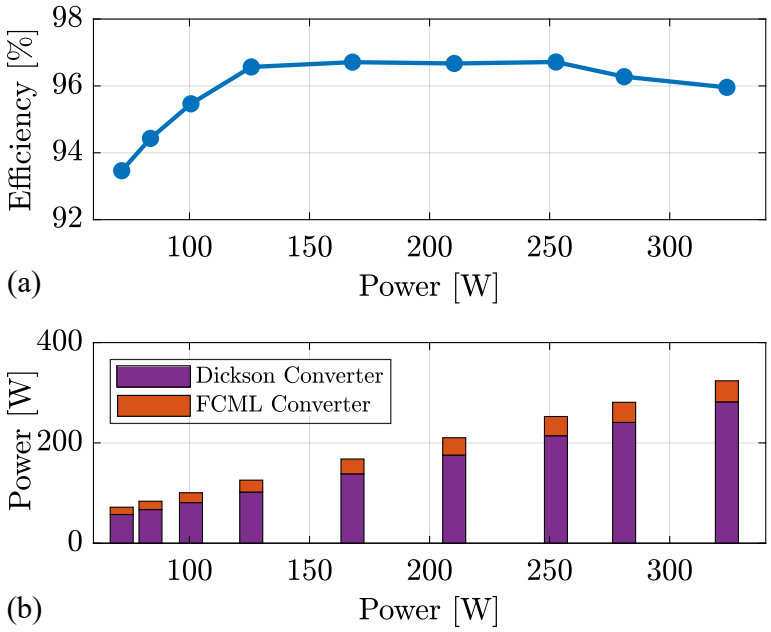

Figure 9.21: (a) Measured efficiency of full composite converter operating at 750 V input (V_{IN}) and regulating to a 50 V output (V_{OUT}). (b) A breakdown of the portion of output power delivered by the Dickson converter and FCML converter.

9.5 Conclusion

This work presents a partial power processing system architecture for achieving high voltage step-down conversion ratios within harsh space environments. A resonant, capacitively-isolated Dickson converter is proposed as the fixed-ratio stage and a FCML converter for the regulating stage. The converters are optimized to minimize the total passive component mass. Finally, a hardware prototype is presented alongside experimental results which verify intended operation of each converter as well as the full composite system. This work demonstrates a method for optimizing the passive component selection hybrid switched-capacitor converters and showcases the use of a partial power processing structure to achieve high step-down conversion with regulation.

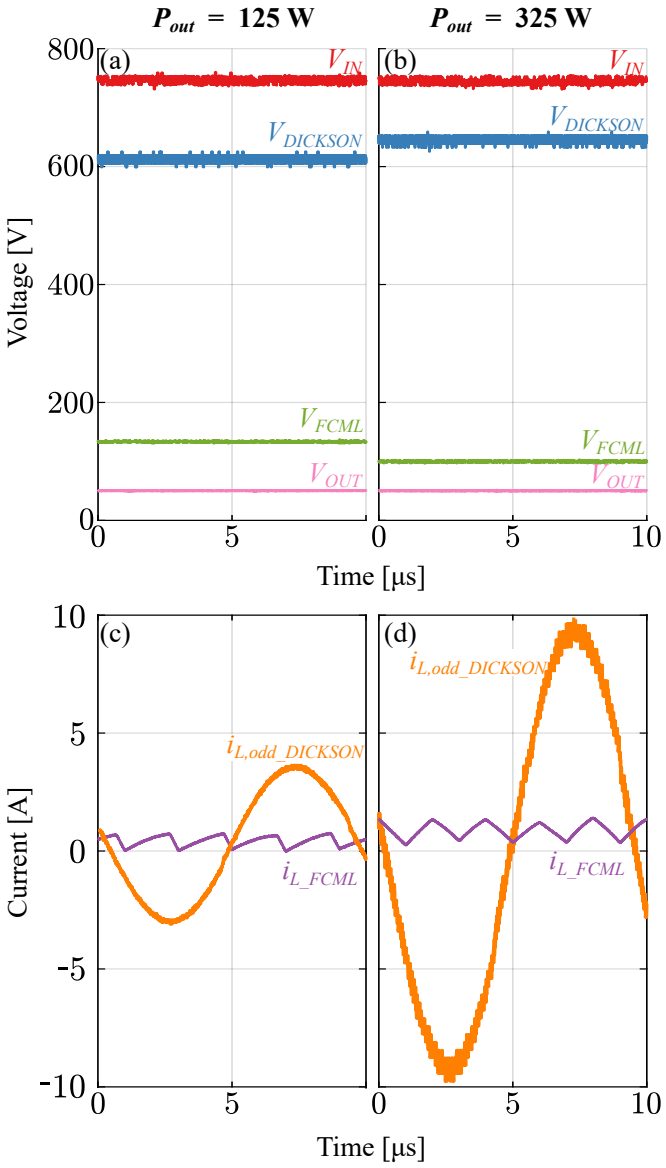

Figure 9.22: Measured operating waveforms of the full composite converter, shown at the peak efficiency, 125 W, and heavy load, 325 W. As shown in (a) and (b) the input (V_{IN}) and output (V_{OUT}) voltages remain constant across load conditions due to the regulation of the FCML converter. However, as the load increases the impedance of the Dickson converter (R_D) increases, as described in Fig. 9.18. Therefore the voltage split between the Dickson converter and FCML converter stages changes with load condition. Subfigures (c) and (d) show the measured inductor currents in the Dickson converter and FCML converter, showing the increased amplitude with increased load.

Chapter 10

Conclusion

10.1 Topology Comparisons

This thesis has focused on two topologies of hybrid SC converters; the capacitively-isolated Dickson converter and FCML converter. There are many different types of hybrid SC topologies, and even some which are newly proposed. To understand the benefits of each topology, it is helpful to have metrics which allow designers to fairly compare topologies, allowing the for the selection of the converter which best suits each application. Here we focus on two metrics; minimized passive mass and switch stress.

The normalized minimal passive mass is found as

$$M^*_{\text{mass}} = \frac{\text{Mass}^*_{\text{tot}}}{\left(\frac{P_{\text{HI}}}{f_{\text{sw},0}\,\gamma_{\text{C}}}\right)} \tag{10.1}$$

where $\text{Mass}^*_{\text{tot}}$ is the total passive component mass when optimized for minimized mass. Parameter P_{HI} is the high-side power (measured in W), $f_{sw,0}$ is the resonant frequency (measured in Hz) and γ_C is the specific energy density of the capacitors (measured in $\frac{\mu J}{mg}$). This minimized component mass includes ripple, allowing for an accurate sizing of components. The process for determining component sizing is discussed in Chapter 9 and in [22]. Finally, by normalizing the passive mass we are able to compare topologies independent of operating condition.

Fig. 10.1 shows the normalized and minimized passive mass for several common hybrid SC converter topologies. All of the topologies shown are operating at-resonance and with a fixed conversion ratio. Some of the topologies, such as the FCML converter, are capable of regulation. However, for fair comparison, the minimized passive component mass for each topology is found assuming fixed-ratio and resonant operation. Moreover, the Dickson (cap-iso) converter shown is the same topology presented in Fig. 9.2. For comparison, the voltage isolation barrier is selected to be the same as that presented in Section 9.2, which is one-fourth the high-side voltage ($V_{ISO} = \frac{1}{4}V_{HI}$). As a result, the capacitively-isolated Dickson converter has the highest passive mass since the capacitors must be sized to block

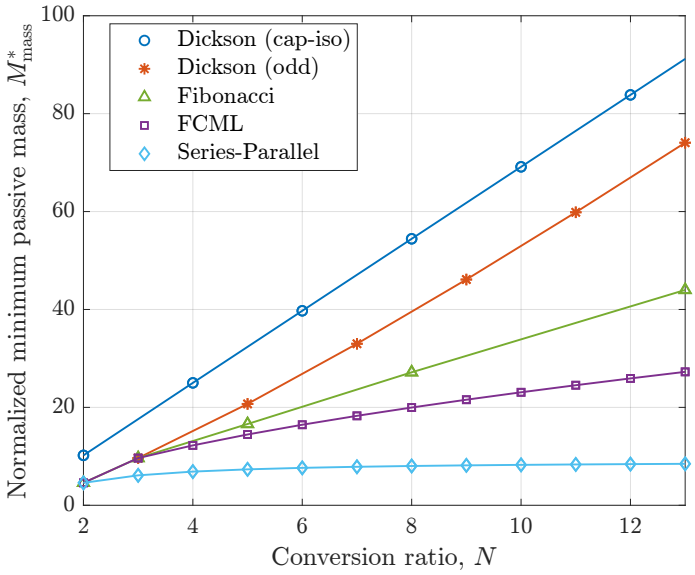

Figure 10.1: Normalized minimum total passive mass versus conversion ratio for a selection of hybrid switched-capacitor converters operating at resonance.

the isolation voltage. If instead, the isolation voltage is set to 0 V (i.e. the input and output grounds are tied together), then the normalized passive mass of the capacitvely-isolated Dickson is equal to that of the conventional hybrid Dickson converter (odd).

In addition to passive mass, the switch stress is also used to understand topology trade-offs. The total VA rating for each converter is found as the sum of the product of the voltage and rms current of each switch, as shown in Eqn. 10.2.

$$\text{VA}_{\text{tot}} = \sum_{i=1}^{N_{\text{S}}} V_{\text{ds,max},i} \cdot I_{\text{rms},i} \tag{10.2}$$

The peak drain-to-source voltage and rms current of the switches is found *including passive component ripple*. The total VA rating is then normalized to the converter's high-side voltage and current as shown in Eqn. 10.3.

$$M^*_{\text{VA}} = \frac{\text{VA}_{\text{tot}}}{V_{\text{HI}} I_{\text{HI}}} \tag{10.3}$$

The normalized switch stress metric is useful for approximating switch losses (i.e. higher M^*_{VA} yields higher losses) and size requirements of the switches (i.e. higher M^*_{VA} can mean larger number of switches or physically larger devices to tolerate increased current/voltage stress).

Figure 10.2 shows the normalized switch stress for common hybrid SC topologies. As in Fig. 10.1, the capacitively-isolated Dickson converter is operating with one-fourth the high

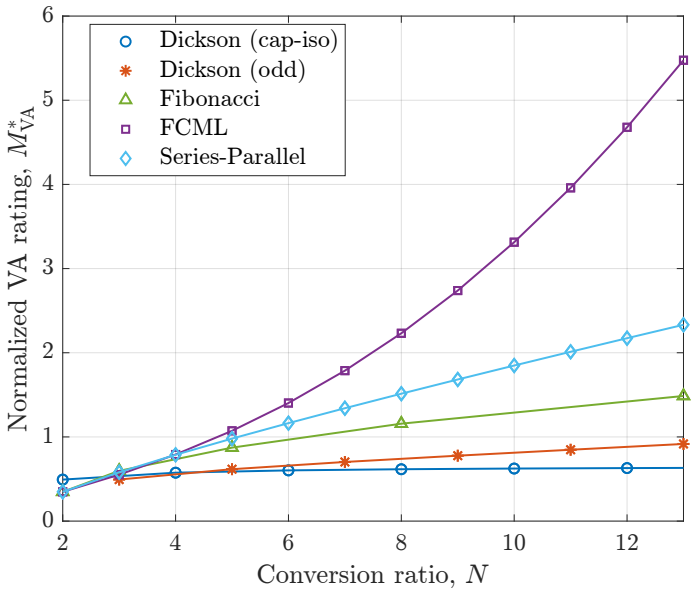

Figure 10.2: Normalized switch stress versus conversion ratio for a selection of hybrid switched-capacitor converters operating at resonance, with optimally sized passive components.

side voltage as the isolation barrier. As discussed in Section 9.2, the tank structure of the capacitively-isolated Dickson converter results in low switch stress even with large passive component ripple, therefore this topology has the lowest normalized VA rating. Conversely, in the FCML converter the switches must be sized to handle the capacitor ripple. As a result, the FCML converter has high normalized VA rating with high conversion ratios. This trade-off may motivate designers to increase the capacitance in the FCML converter which will increase passive component mass, but decrease the normalized VA rating.

As with most design decisions, Fig. 10.1 and Fig. 10.2 indicate the trade-offs that exist with selecting a topology and optimizing for a given application. Moreover, this comparison does not include additional losses such as inductor and capacitor losses which may impact design decisions. Future work is also required to fairly compare these topologies with regulating converters and to conventional inductor-based topologies.

As a response to the growing field of electrification in aerospace, this thesis has showcased several hardware prototypes of hybrid SC converters designed for aerospace applications. Advanced structures, such as the composite architecture shown in Chapter 9, showcase how hybrid SC converters can be used in future extreme environment applications. In addition, the design of these converters, from loss modelling to safe control techniques, has been explained. This work provides a framework for comparing topologies, and design methods which give designers better tools to build reliable and high performance converters.

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