Title
DIGITIZING ELECTRONICS FOR THE EMI MULTI-WIRE PROPORTIONAL CHAMBERS

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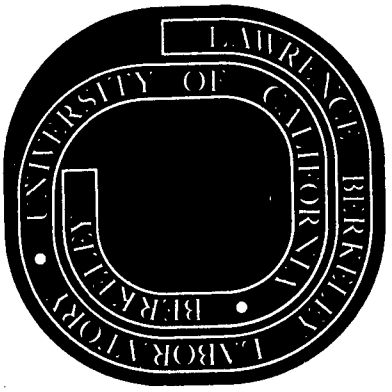

DISCLAIMER

DIGITIZING ELECTRONICS FOR THE EMI MULTI-WIRE PROPORTIONAL CHAMBERS*

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Summary

A complete system of electronics for digitizing pulses from a large array of multi-wire proportional counters is described. The system is based on the method of coupling the chamber pulses onto delay lines developed by Perez-Mendez. All three wire planes of each chamber are digitized, giving positional information for each avalanche in the chamber on three coordinates, x, y and a redundant coordinate.

The system will be used with an array of 30 chambers each one meter square, which will serve as an External Muon Identifier (EMI) for the 15-foot diameter bubble chamber in the neutrino beam line at NAL. Up to 16 events can be digitized in a 60 μs beam spill.

Introduction

A 15-foot diameter bubble chamber is being built for the neutrino beam line at the National Accelerator Center. Under a plan proposed by Stevenson and Peterson,[1] the bubble chamber will be augmented by a layer of Multi-wire Proportional Chambers (MWPC) surrounding a portion of the bubble chamber periphery. The purpose of this layer is to permit identification, external to the bubble chamber, of muons involved in bubble chamber events. The system of MWPCs is therefore referred to as an External Muon Identifier (EMI).

The initial phase of this plan will have 30 square meters of MWPC, consisting of 30 individual chambers each one meter on a side.[2] Each chamber will have 3 coordinate axes digitized--X, Y and U. U is a redundant plane whose coordinate axis is rotated 45° with respect to X. The location of a charged particle passing through a chamber will be digitized to a resolution of ±5 mm on each coordinate axis. During a 60 μs beam spill, an average of 5 events is expected in each chamber.

The MWPC readout is based on the electromagnetic delay lines developed by Perez-Mendez.[3] For this application, delay line digitization has some attractive features compared to other digitizing means, such as the logic channel-per-wire.[4] First, it tends to reduce the cost of electronics, since only seven channels of electronics are necessary to digitize all three coordinates of a chamber. Each channel is reasonably inexpensive, in this case partly because of the relaxed resolution requirements. Amplifier-per-wire logic usually is attached only to one plane of a chamber. In contrast, delay lines can be coupled to all three planes, hence the number of chambers required and the chamber cost is reduced.

*This work was done under the auspices of the U.S. Atomic Energy Commission.

Relationship of Electronics to the Chambers

Figure 1 shows a schematic view of a chamber and its three delay lines, one each for X, Y and U coordinates. The wires of the three planes are extended a sufficient distance to establish a capacitive coupling of each wire onto the delay line. An event (avalanche) on a particular wire results in a voltage pulse being introduced onto the delay line at that point. The pulse then propagates to the ends of the delay line at a velocity of the order of 0.2mm/ns. Seven digitizer channels are used with each MWPC: one on each end of the three delay lines, plus one to record the "prompt" (undelayed) times of the chamber events. Each digitizer channel records the time at which it receives each of up to 16 pulses during a beam burst. Since there are 30 MWPCs, a total of 210 digitizer channels is used. At the end of a beam burst, they deliver all the data they have collected (up to 16x210=3360 words) during the burst.

A suitably designed computer program can analyze the collected data from each chamber to determine the location and time of occurrence of each event within that chamber. The Appendix gives some details of the analysis procedure.

Components of the Digitizer Chain

The pulses at the delay-line outputs generally have amplitudes of a few millivolts and rise-times of the order of 100 ns. The delay lines have characteristic impedances of about 1000 ohms. The preamplifier is mounted physically adjacent to the delay line, and amplifies the signals before they are transmitted from the chambers to the discriminators on 50-ohm coaxial cable. The discriminators develop timing pulses whose leading edges are an accurate measure of the time-of-arrival of the delay line pulse. The timing pulses are delivered to the digitizers. They develop and store binary numbers whose magnitudes are related to the times-of-arrival.

Preamplifiers

The spatial resolution of the digitizing channels depends on how well the times-of-arrival of the pulses can be measured. This in turn is strongly dependent on the signal/noise ratio at the timing discriminator. The relationship is approximately:

$$T_J = \frac{E_n}{S},$$

where T_J = timing error (jitter) introduced by the presence of the noise, seconds;

E_n = noise superimposed on the signal, volts; and

S = the slope of the signal waveform, volts/sec.

Both E_n and T_J are expressed in the same way--e.g., rms, peak or FWHM. For many pulses, S can be expressed as $S=1.25\ E/\tau$, where E is the peak amplitude, and τ is the 10-90% rise-time.

The signal/noise ratio is determined mainly by the characteristics of the input stage of the preamplifier.

Although the spatial requirements for this experiment are relaxed, some experiments require resolution of a fraction of a millimeter. These preamplifiers have therefore been designed for low input noise to accomodate a wide range of applications. An amplifier bandwidth of 3 MHz is sufficient for the signals typical of these delay lines.

A terminated delay line represents a source with impedance Zo/2, where Zo/2 is typically 500 ohms. The resistive noise from a 500 ohm resistor at room temperature in a 3 MHz bandwidth system is 5 μV rms. The equivalent input noise from preamps using low-noise bipolar transistors has been measured to be 8.5 μV, when connected to terminated 1000-ohm delay lines. Since noise voltages add vectorially the noise contribution of the amplifier itself is calculated to be 7 μV.

Low-noise field-effect transistors (FETs) are generally less suitable than bipolar transistors in this application, because of the low impedance of the source. For example, a preamplifier using low noise FETs was found to have a noise performance a factor of two poorer than the one using bipolars.

Some low-cost linear integrated circuits are now available. A few of these have adequate gain-bandwidth product and reasonably low noises. The circuit of a preamplifier using a Fairchild type 733 is shown in Fig. 2. It exhibits an equivalent input noise of 13 μV when connected to a delay line. While this is not as good as the discrete bipolar design, it is adequate for many purposes and results in a smaller printed circuit board size. This is the design used in the EMI project.

Discriminator

Figure 3 shows a functional block diagram of a discriminator channel. Input signals from the preamplifier are differentiated to form a zero-crossing pulse, and then amplified by a factor of 10. The times at which the pulses cross the base-line are detected by the zero-cross detector, which triggers the fast monostable. The final stage then delivers a TTL-compatible output pulse. Seven identical channels are housed in a NIM module.

The zero-crossing detector uses an RCA CA3086 integrated circuit in combination with an 1N3717 tunnel diode (TD) to sense the zero-crossing. Each integrated circuit has one differential pair and three independent transistors. Since all are contained on the same monolithic chip, the transistors maintain their matched characteristics over a wide temperature range. The circuit is therefore considerably stabler than if discrete transistors were used. The only adjustment provided is a tunnel-diode bias control.

A simplified circuit of the zero-cross detector is in Fig. 4a, and the tunnel diode characteristic and load line in Fig. 4b. With no input signal, the current supplied by current source Q3 is adjusted until the TD is operating at point of A of Fig. 4b. Note that point A lies on a load line that passes through point D. A positive-going input to Q_1 diverts current from Q_2, thereby moving the TD operating point toward point B. If the input becomes more positive than the threshold level, the TD switches from B to C. As the input signal returns toward zero, current Q_1 decreases, and the TD operating point moves toward D. If the bias was initially set as described above, the TD switches from D to A just as the input crosses through zero. The switching of the TD from D to A triggers the monostable and generates the output pulse.

The transistor Q_5, between Q_2 and the TD, has the important function of reducing the internal feedback due to the Miller effect. This aids in deriving a precise timing point from a relatively slow-moving input signal, and has been shown to reduce the timing jitter. The timing jitter measured with an input having 100 ns rise-time is less than 1 ns. The time-slewing is within ±2ns for an input amplitude range of 50 to 1500 mv (30:1).

Digitizer Module

The digitizer is a CAMAC module that can digitize the times-of-arrival of up to 16 pulses on each of seven inputs. The time-of-arrival of each pulse is digitized by storing "on-the-fly" the contents of a scaler that is counting externally supplied clock pulses. The digitizer can operate with clock frequencies up to 28 MHz, hence can measure the time-of-arrival to ±36 ns.

The block diagram of Fig. 5 shows the organization of the digitizer. Clock pulses are counted by a 12-bit synchronous scaler. The contents of the scaler are available to each of the seven independent channels. As each signal pulse enters a signal input, it causes the contents of the scaler to be transferred to the corresponding Temporary Store. This transfer may be done only within a certain acceptance interval during each clock period, which, at a clock frequency of 28 MHz, is approximately 20 ns. The input synchronizer insures that this transfer is triggered only at an appropriate phase of the clock period.

The transfer of the data from temporary store to scratchpad memory may take up to 100 ns, since input pulses are not expected to be closer together than that. This permits the use of scratchpads that have longer minimum acceptance times than the temporary store. The scratchpad memories are each composed of three 16x4 bit read/write integrated-circuit memories, with address decoding (IC Type Am31L01). The memories are organized on a last-in-first-out basis. A 4-bit UP/DOWN counter with MAX/MIN carry-out (SN74191) is used as an address scaler for each scratchpad. During digitizing, it is incremented each time a word is stored. If 16 words are stored, the MAX/MIN carry is used to disable the signal input. During readout, the address scaler is decremented, and the MAX/MIN carry signals when all "fresh" words have been read out.

Readout Process. It is generally the case that a random number of pulse inputs are received during the interval that the module is actively digitizing. Thus a random number of words will be stored in each scratchpad memory during this interval. The digitizer

is designed to read out only the words that have been collected since the last previous readout. The module uses the Q-controlled Stop mode* of block transfer to move the data, via the CAMAC Dataway, to the computer or storage device. The Stop mode is especially useful for transfers where the module controls the number of words to be transferred. The digitizer module behaves as though the Read command accesses a single register through which all words are transferred. This register is the only one in the module using F(0), hence subaddresses can be ignored for F(0). A controller can access arrays of digitizers by using the algorithm:

Step 1. Set up Dataway command N(i)·F(0)·A(0) where N(i) is the station containing the first module in the array.

Step 2. Execute a Dataway cycle (module ignores subaddress).

Step 3. Test Q received during this Dataway cycle.

a) If Q=1: Transfer data to storage; increment subaddress (optional); repeat Step 2.

b) If Q=0, this module is finished, so go to the next: Do not transfer data; increment station number, N; reset subaddress to zero (optional); repeat Step 2.

Some CAMAC Branch Drivers** are equipped to execute this algorithm in hardware. The optional subaddress manipulation makes this algorithm compatible with many modules designed for Address Scan mode.

During the transfer of data from a module, the Read Priority Sorter (see Fig. 5) controls the order in which digitizing channels are read out. It first enables the transfer of a single module-identification word (priority 7). During this transfer, the module gives a Q-response of '0' if there are no data words stored in the scratchpads. If there are stored words, the individual channels are read out in order, each channel contributing only the number of data words gathered since the last readout. Since the memory address scalers are decremented during this process, each finally resting at memory address 0, a completely read out module is ready for the next digitizing interval.

Data Identification. Generally, several modules will be read into a single block of computer memory. Since each contributes a variable number of words, some means of identifying the origin of each word must be provided. Fortunately, the scaler is only required to be 12 bits. Therefore, 4 bits are available for identification within the 16-bit word size that is convenient for many computers. One bit is used to uniquely identify the module identification word shown in Fig. 6a. This word, the first word read from each module, carries an 8-bit module identification code. All other words use the format shown in Fig. 6b. Three bits in each data word show the channel number from which it originated. Thus, in the block of memory, the sets of words contributed by individual modules are delimited by words carrying 1's in the most significant bit position. These identify the module contributing the words in the immediately following set. Within this set, identification of the channel originating each word is carried in the word itself.

*See the CAMAC Specification TID-25875[8] (EUR-4100e), Sec. 5.4.3.3. In the Stop mode the module generates a Q=1 response to a Read command [typically F(0)] as long as it has a meaningful data word to transfer on that command. It generates a Q=0 response after all its words have been transferred.

**For example, the EG&G BD-011[5] or the Los Alamos micro-programmed Branch Driver.[6]

Clock Module

The CAMAC clock module provides a common time base for up to 100 digitizers, and helps to synchronize the various phases of the data gathering and readout. Its relationship to the other components is shown in Fig. 7. Its two output signals, Clock and Write Permit are bussed to all the digitizer modules. The state of Write Permit determines whether the digitizers are in the digitizing (writing-into-memory) state. The clock output is a train of 28 MHz pulses derived from a crystal oscillator. These pulses are connected by a scaler in each digitizer which can then measure the times-of-arrival of signal pulses in terms of the number of clock pulses received up to that time.

Arrival of a Start of Beam Spill Sync pulse from the accelerator causes the Write Permit signal to become true, and triggers the start of the clock train. The number of clock pulses in the train issued is preset by CAMAC command or by front panel controls. At the end of the train, Write Permit goes False, and the Clock module raises its 'L' flag to notify the computer of the end of the digitizing period.

Fiducial Module

Each delay line can be fitted with two extra input ports, one near each end of the line. These are used to inject simulated chamber pulses onto the delay line. The simulated pulses can be digitized and the results checked to make sure all components are working properly.

The CAMAC fiducial module generates fiducial triggers under CAMAC control. These are sent to all the chambers to cause the simulated pulses to be generated.

Complete System

A block diagram of a portion of a system is shown in Fig. 7. Figure 8 shows the sequence of major states of the system in processing data from a beam spill. The clock module is enabled, via CAMAC, to accept a Beam Spill Sync pulse. The arrival of the Sync pulse starts the digitizing phase. The computer is notified of the end of this phase by a Look-at-Me from the clock module. The computer then initiates the algorithm described above to transfer the data collected by the digitizers into the computer memory.

Several system testing features are included by which various parts of the system can be checked. For example, with the clock disabled, the scalers in the individual digitizer modules can be loaded with a predetermined number by CAMAC command. Then the scratchpad memories in chosen channels of each digitizer can be caused to store this number. The numbers

so stored can be read out and checked against the predetermined number. Further back in the systems, the discriminators can be triggered to produce output pulses on all channels simultaneously. These are digitized under dynamic conditions--i.e., clock running. All digitizers should have stored the same number to within the usual scaling error of plus or minus one count. If the fiducial module is triggered to generate simulated chamber pulses, then the discriminators are also included in the test.

Acknowledgments

We are happy to have been able to work with a group of Lawrence Berkeley Laboratory-University of Hawaii experimenters while developing this system. This group includes L. Stevenson, V. Peterson, S. Parker, F. Harris, V. Stenger and J. Crosetti.

Appendix

Figure 1 shows that each MWPC chamber will develop a pulse on each of seven channels for every event. Figure 9 illustrates the significance of the pulses. Three time diagrams are shown, one for each delay line. Time increases from top to bottom. The abscissae represent distances along the delay lines. An event that occurs at location X_1, Y_1, U_1 and at time $t=t_{C1}$ is depicted. The line segments at angle α with the horizontal represent the trajectories of the pulses on the delay lines. As a result of this event, pulses arrive at the ends of the delay lines at times t_{A1}, t_{B1}, t_{D1}, t_{E1}, t_{F1}, and t_{G1}. The time t_{A1} is recorded in digitizer channel A, t_{B1} in B, t_{C1} in C., etc. The location of the event can be determined by appropriate mathematical operations on any two of t_{A1}, t_{B1}, and t_{C1} (X coordinate); and any two of t_{C1}, t_{D1}, and t_{F1} (Y coordinate).

For example, X_1 can be calculated by any of the following:

$$X_1 = (t_{A1} - t_{C1})v, \quad (1)$$

$$= L_x - (t_{B1} - t_{C1})v, \text{ or} \quad (2)$$

$$= \frac{L_x}{2} - \frac{t_{B1} - t_{A1}}{2} v, \quad (3)$$

where v = velocity of propagation of pulses in the delay line, and

L_x = physical length of X-plane delay line.

The reconstruction using equation (3) is advantageous for the following reason: a shift in the measured time difference $(t_{B1} - t_{A1})$ of Δt represents a shift in coordinate of the event of $\Delta X=\Delta t/2v$. If (1) or (2) are used, it represents only $\Delta X=\Delta t/v$. Thus a given time resolution in the measuring device results twice as good a spatial resolution if pulses from the two ends of the line are digitized (equation 3), rather than pulses from one end and the prompt pulse (equations 1 and 2).

The pulses t_{F1} and t_{G1} are used to determine the U coordinate. It can be used to resolve ambiguities that arise if two events occur simultaneously in the chamber.

Figure 10 shows a case in which two events occur at time t_{C1}, one at X_1 and one at X_2. Note that channels A and B each receive two pulses, and that the pulses at t_{A1} and t_{B1} (subscripts assigned in time-of-arrival sequence) are not associated with the same event. Given the times-of-arrival t_{C1}, t_{A1}, t_{A2}, t_{B1}, and t_{B2}, a reconstruction of the event in the x-coordinate can be made by noting that $(t_{B2}-t_{C1})+(t_{A1}-t_{C1})=T$ and that $(t_{B1} - t_{C1}) + (t_{A2} - t_{C1})=T$, where $T=\frac{Lx}{v}$ is the total propagation delay of the line. Therefore the coordinates can be found:

$$X_1 = \frac{Lx}{2} - \frac{t_{B2} - t_{A1}}{2}v \text{ and}$$

$$X_2 = \frac{Lx}{2} - \frac{t_{B1} - t_{A2}}{2}v.$$

This timing ambiguity problem can be resolved in the Y and U coordinates in the same way. There still remains a spatial ambiguity if only x and y are used, since X_1, X_2, and Y_1, Y_2 can be combined in four ways to give a point X_i, Y_j. This ambiguity is removed by using the redundant coordinate information.

Figure 11 shows another case. Here two events occur at different times, t_{C1} and t_{C2}, but at a separation that is smaller than the delay line total propagation time. The reconstruction of the events from the data is done in a similar way to that discussed with Fig. 10, except that an additional datum, t_{C2}, must be utilized. The analysis procedure is to search for triplets, t_{Ai}, t_{Bj}, t_{Ck}, such that

$$(t_{Ai} - t_{Ck}) + (t_{Bj} - t_{Ck}) = T. \quad (4)$$

The identified triplets can then be analyzed to determine X_1, etc.

The lines representing pulse trajectories in Figs. 9, 10, and 11 are deliberately made broad in order to represent the finite "size" of pulses on the delay line. These pulses are typically such that, at the delay line output, a minimum separation of the order of 100 ns is necessary to allow individual detection of pulses that occur in pairs. If the vertex of the trajectories for one event lies within the broad trajectory of another event, it may not be possible to resolve them.

References

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Fig. 1. A schematic representation of a MWPC and its three delay lines. The wires of each of the three planes are extended from the chamber so as to capacitively couple to the delay line. The labeling of the signal ports -- A, B, E, etc. -- corresponds to Fig. 9.

Fig. 2. A schematic of the preamplifier design that uses an integrated circuit input stage. The signal-inverting links are shown connected for positive input signals; they are crossed over for negative signals. Because of the relatively high input current of the 733, resistor R1 must be chosen to be equal to the dc source resistance ($Z_o/2$ for line terminated at both ends) plus 200 ohms.

Fig. 3. A block diagram of a discriminator. Seven identical channels are built in a NIM module.

Fig. 4. a) A simplified circuit of the zero-cross detector used in the discriminator. All five transistors are contained in the CA3086 integrated circuit. b) I-V characteristic and load line for the tunnel diode.

Fig. 5. A block diagram of the 7-channel digitizer module.

Fig. 6. Bit formats of words read from the digitizer:
a) The module identification word;
b) A data word.
Bit number 16, the most significant bit, differentiates between identification and data words.

Fig. 7. Block diagram of a complete MWPC readout system using the components described in the report.

Fig. 8. Sequence of major states in the process of digitizing data from a single beam spill.

Fig. 9. A diagram that illustrates the time relationships among pulses arising from an event in the MWPC.

Fig. 10. A time diagram (x-coordinate only) illustrating two events occurring simultaneously in the MWPC at time t_{C1}.

Fig. 11. Illustration of a situation in which two events occur at different times and at different locations.

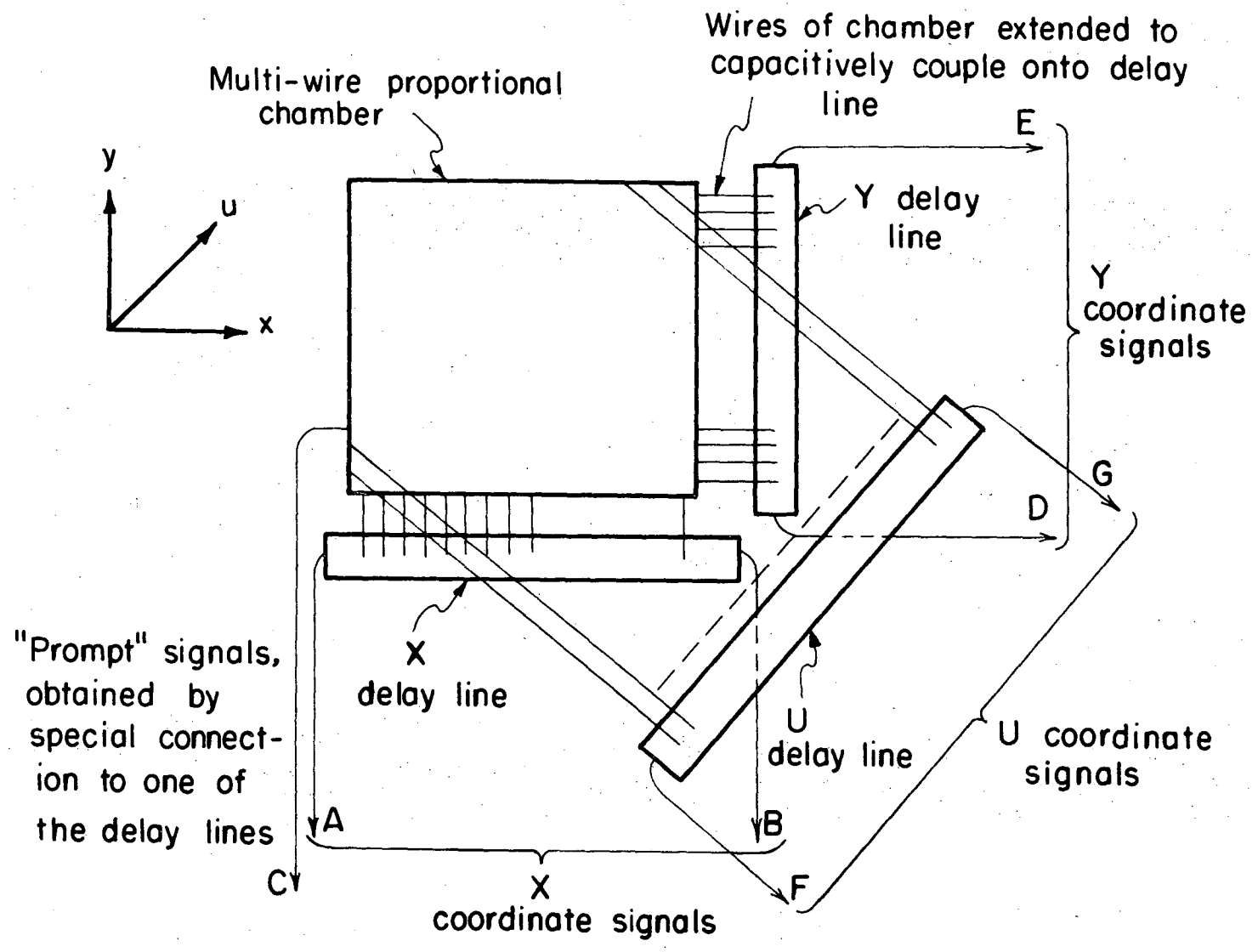
Wires of chamber extended to capacitively couple onto delay line
Multi-wire proportional chamber
y
u
x
E
Y delay line
Y coordinate signals
G
D
"Prompt" signals, obtained by special connection to one of the delay lines
X delay line
U delay line
U coordinate signals
A
B
C
F
X coordinate signals
XBL7211-4416

Fig. 1

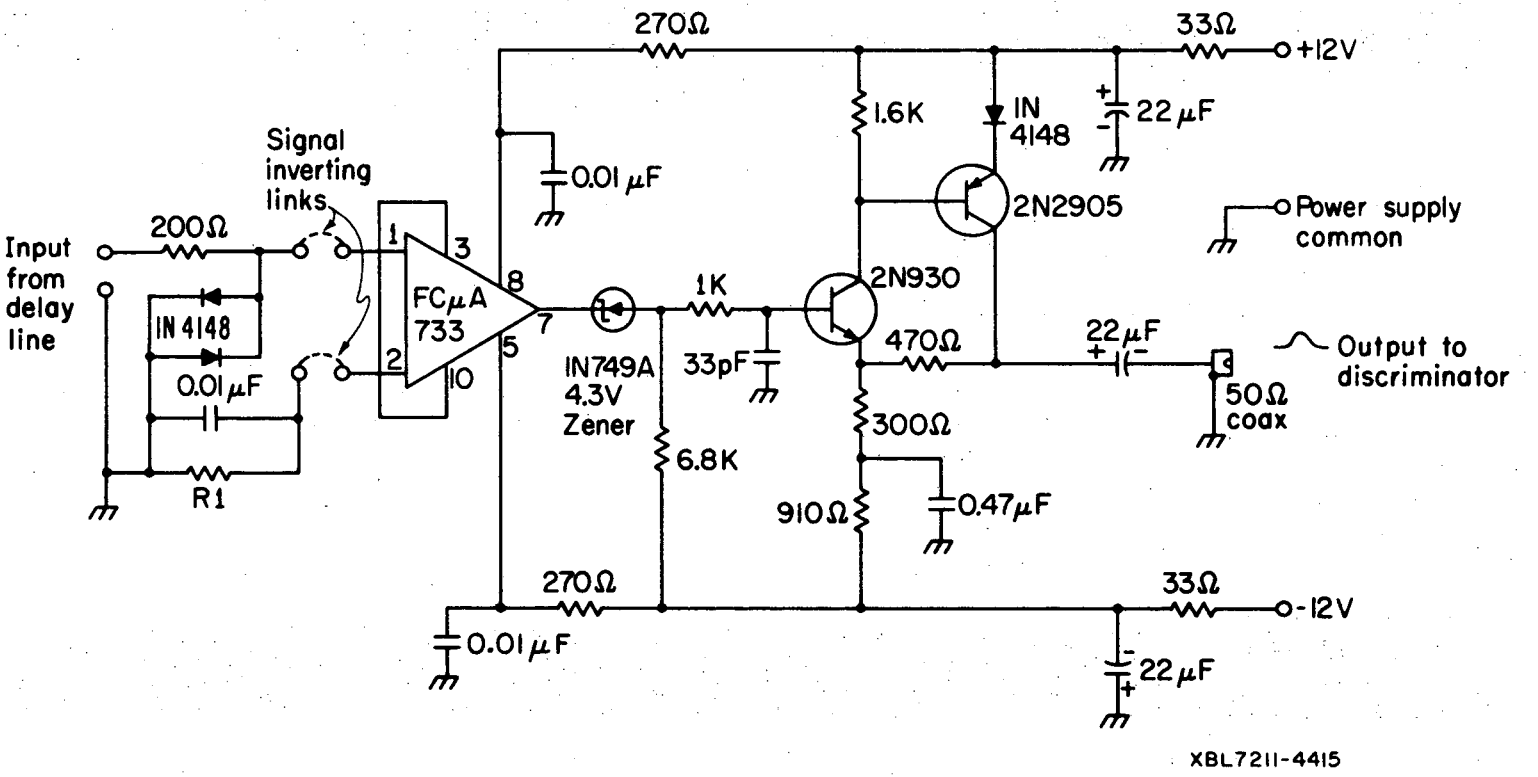
270Ω
33Ω
+12V
1.6K
IN 4148
22 μF
0.01 μF
2N2905
Power supply common
Signal inverting links
200Ω
Input from delay line
IN 4148
0.01 μF
R1
FCμA 733
1
2
3
5
7
8
10
IN749A 4.3V Zener
1K
33pF
2N930
470Ω
22 μF
Output to discriminator
50Ω coax
300Ω
6.8K
910Ω
0.47μF
270Ω
33Ω
-12V
0.01 μF
22 μF
XBL7211-4415

Fig. 2

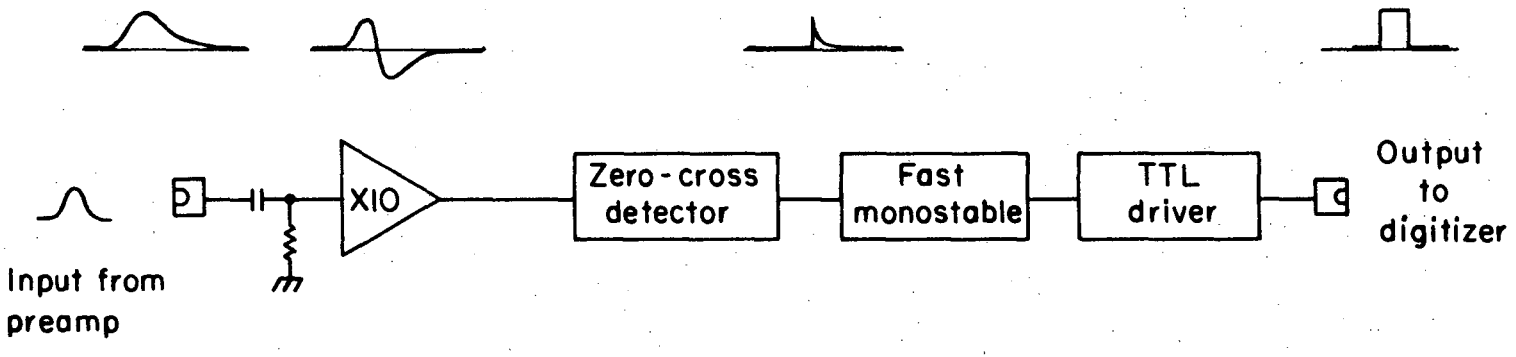
X10
Zero-cross detector
Fast monostable
TTL driver
Input from preamp
Output to digitizer
XBL7211-4414

Fig. 3

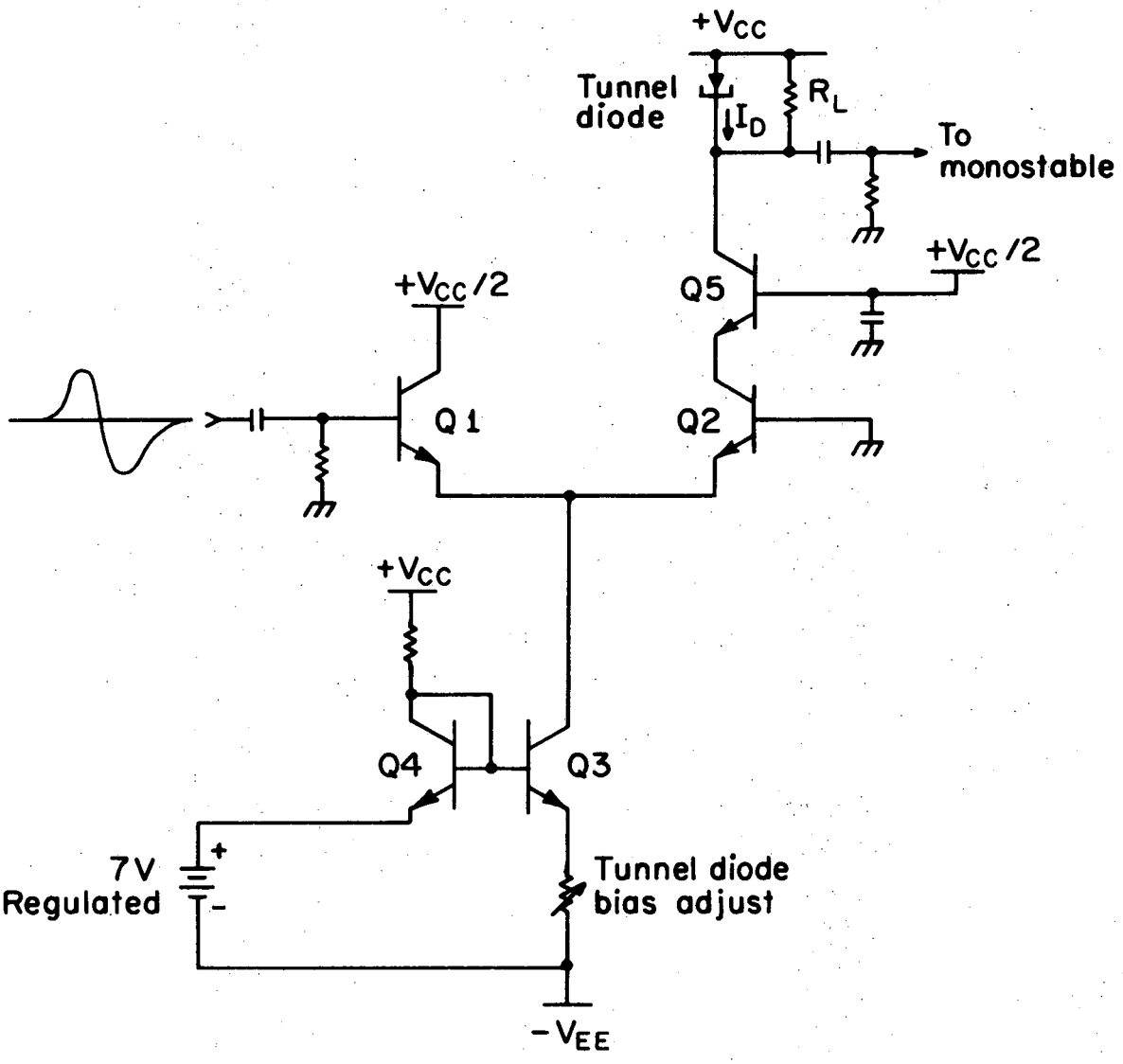
+Vcc
Tunnel diode
ID
RL
To monostable
+Vcc/2
+Vcc/2
Q5
Q1
Q2
+Vcc
Q4
Q3
7V Regulated
+
-
Tunnel diode bias adjust
-VEE
XBL7211-4413

Fig. 4a

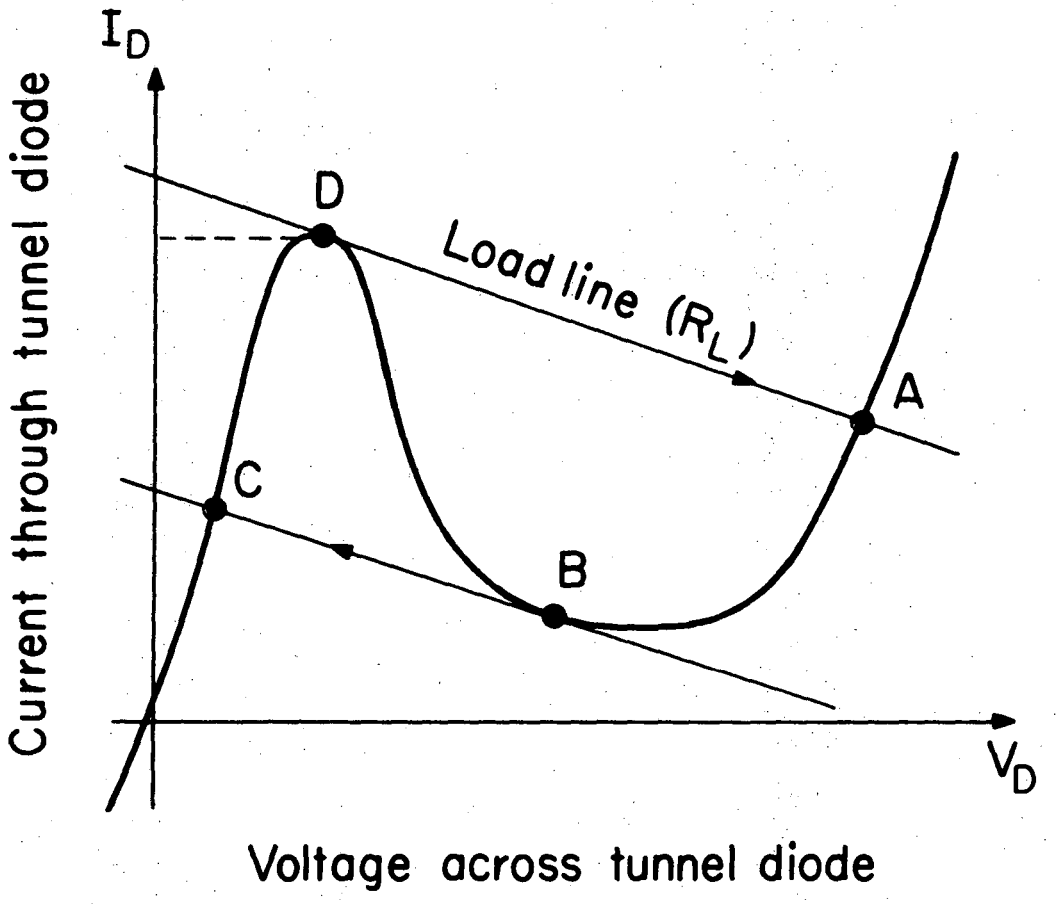

Fig. 4b

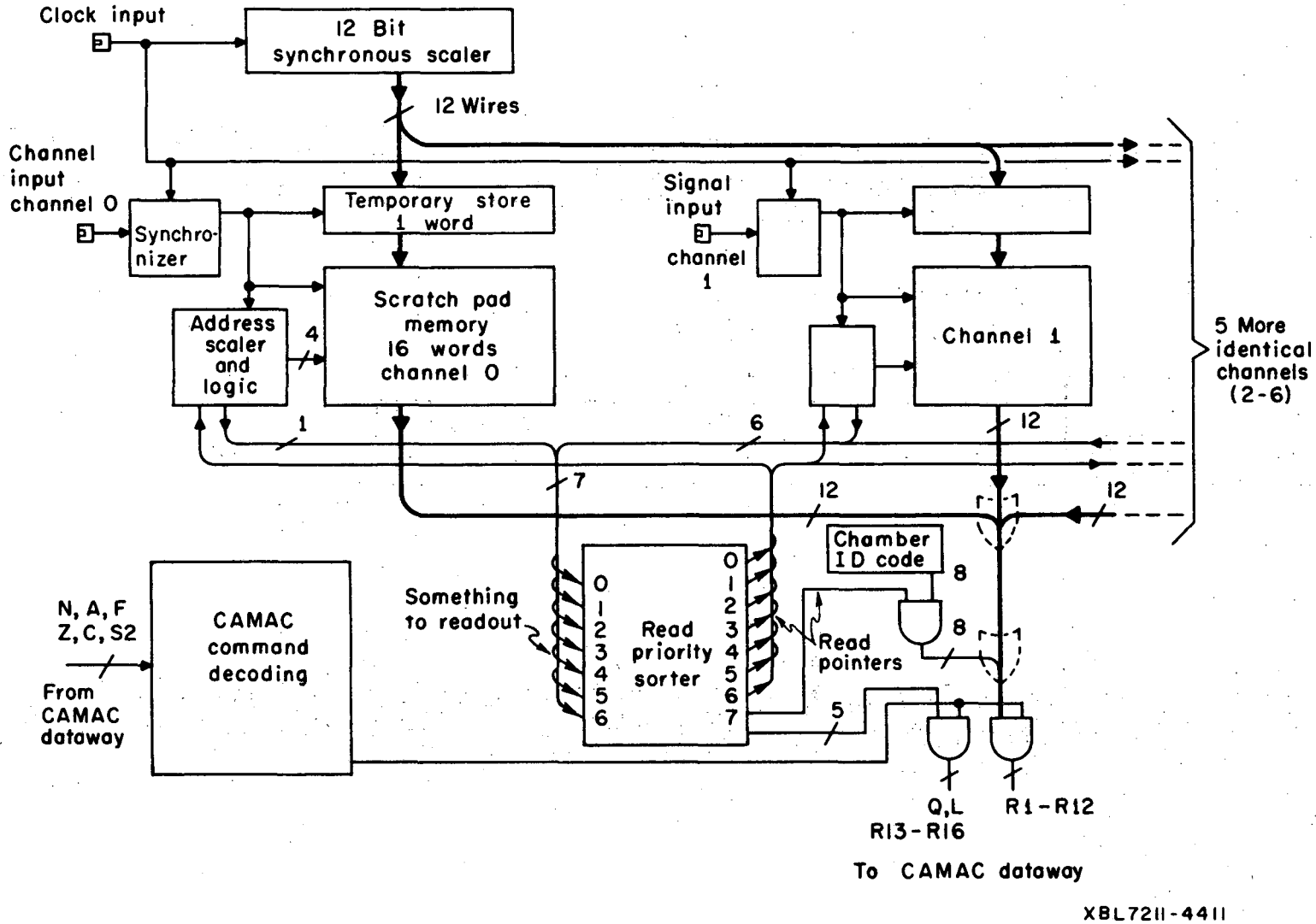
Clock input
12 Bit synchronous scaler
12 Wires
Channel input channel 0
Synchro-nizer
Temporary store 1 word
Signal input channel 1
Address scaler and logic
4
Scratch pad memory 16 words channel 0
Channel 1
5 More identical channels (2-6)
1
6
12
7
12
12
Chamber ID code
8
8
Something to readout
Read priority sorter
Read pointers
N, A, F Z, C, S2
From CAMAC dataway
CAMAC command decoding
5
Q,L R13-R16
R1-R12
To CAMAC dataway
XBL7211-4411

Fig. 5

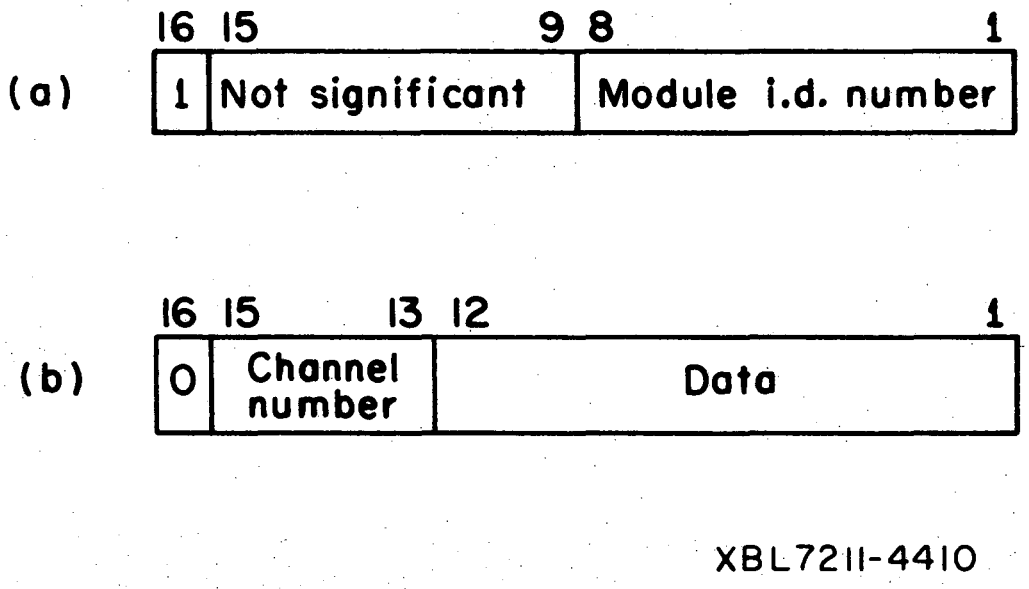
16 15 9 8 1
(a)
1
Not significant
Module i.d. number
16 15 13 12 1
(b)
0
Channel number
Data
XBL7211-4410

Fig. 6

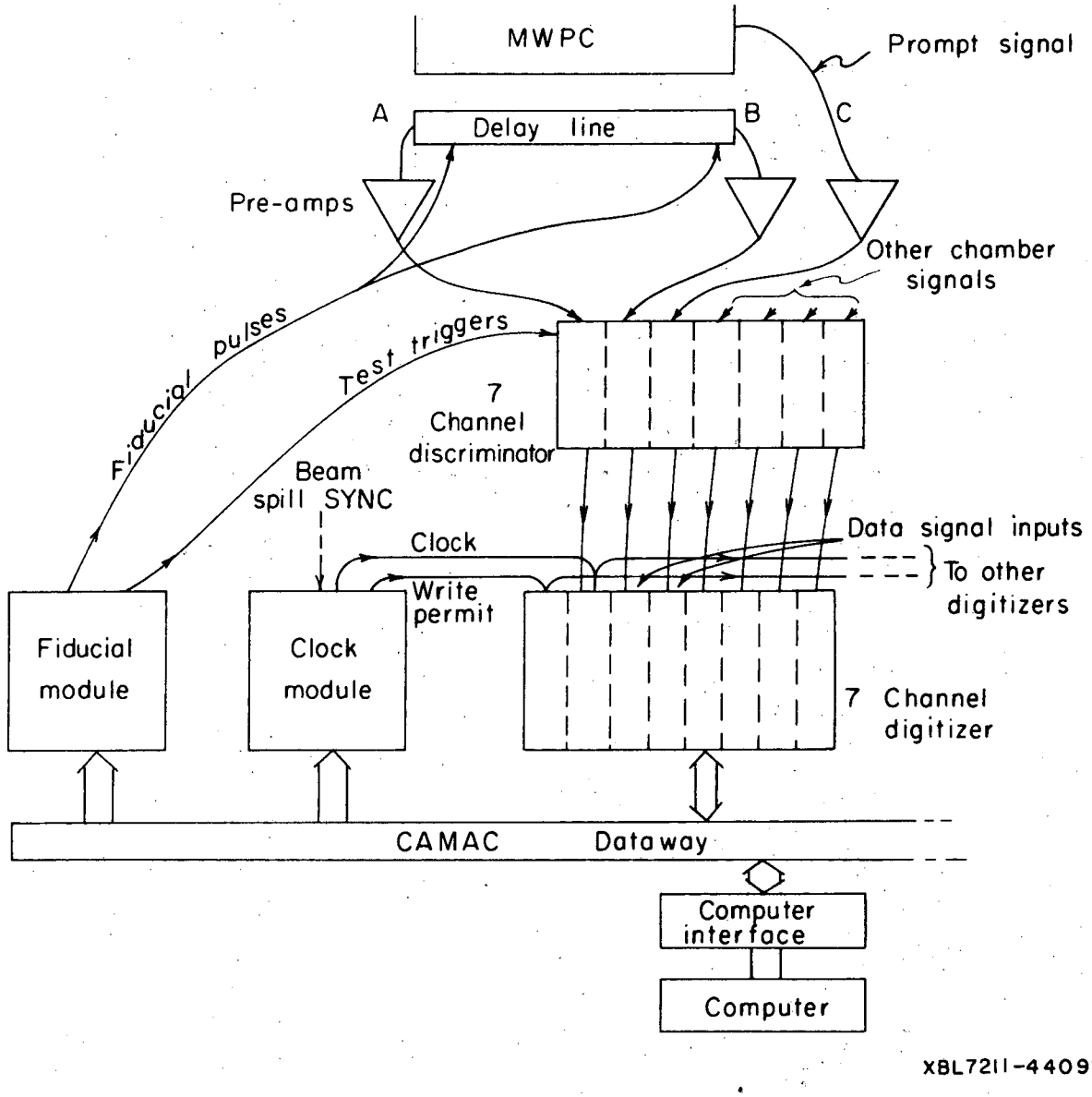
MWPC
Prompt signal
A
Delay line
B
C
Pre-amps
Other chamber signals
Fiducial pulses
Test triggers
7 Channel discriminator
Beam spill SYNC
Clock
Write permit
Data signal inputs
To other digitizers
Fiducial module
Clock module
7 Channel digitizer
CAMAC
Dataway
Computer interface
Computer
XBL7211-4409

Fig. 7

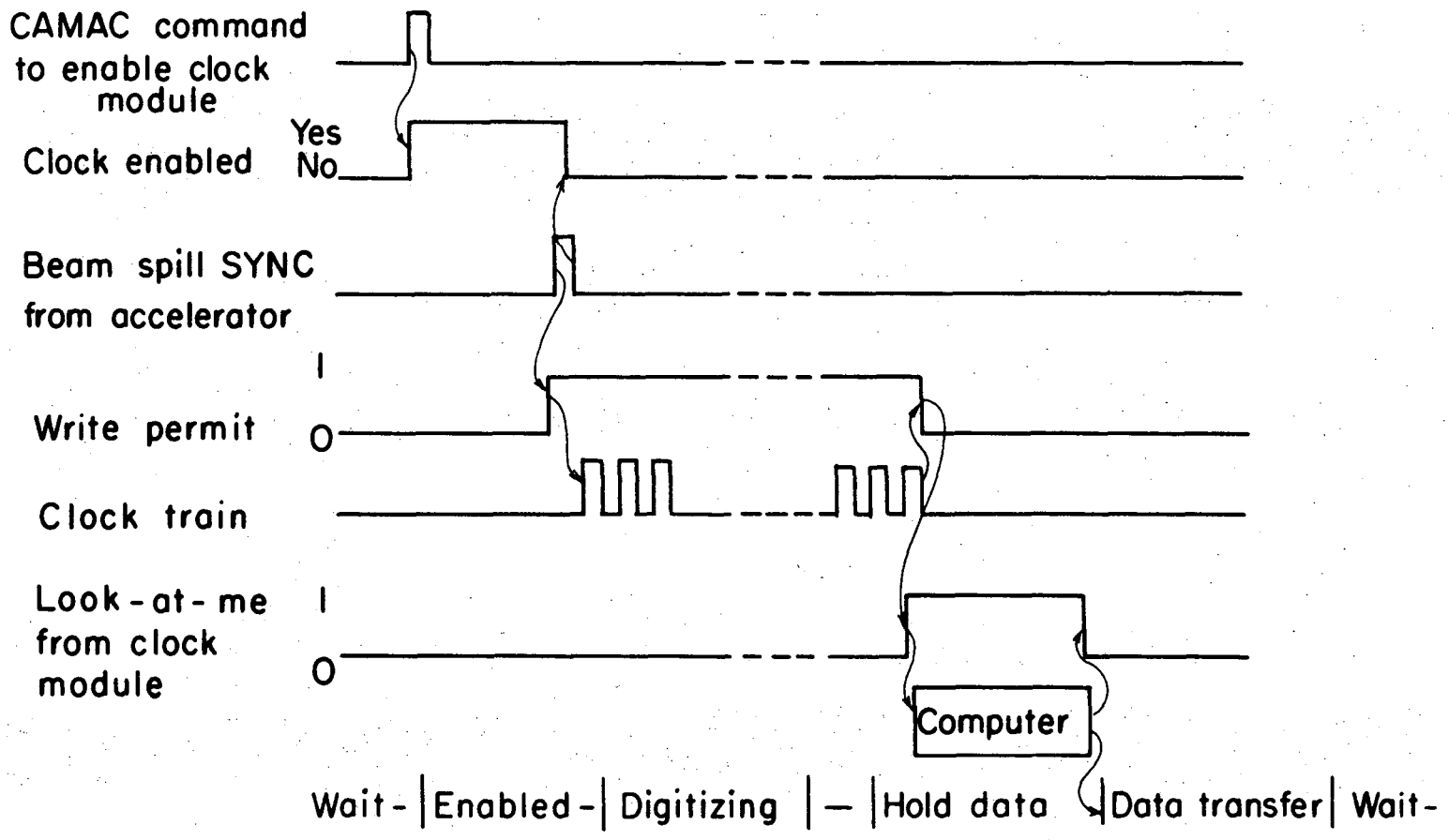
CAMAC command to enable clock module
Clock enabled
Yes
No
Beam spill SYNC from accelerator
Write permit
1
0
Clock train
Look-at-me from clock module
1
0
Computer
Wait-
Enabled-
Digitizing
—
Hold data
Data transfer
Wait-
XBL7211 -4408

Fig. 8

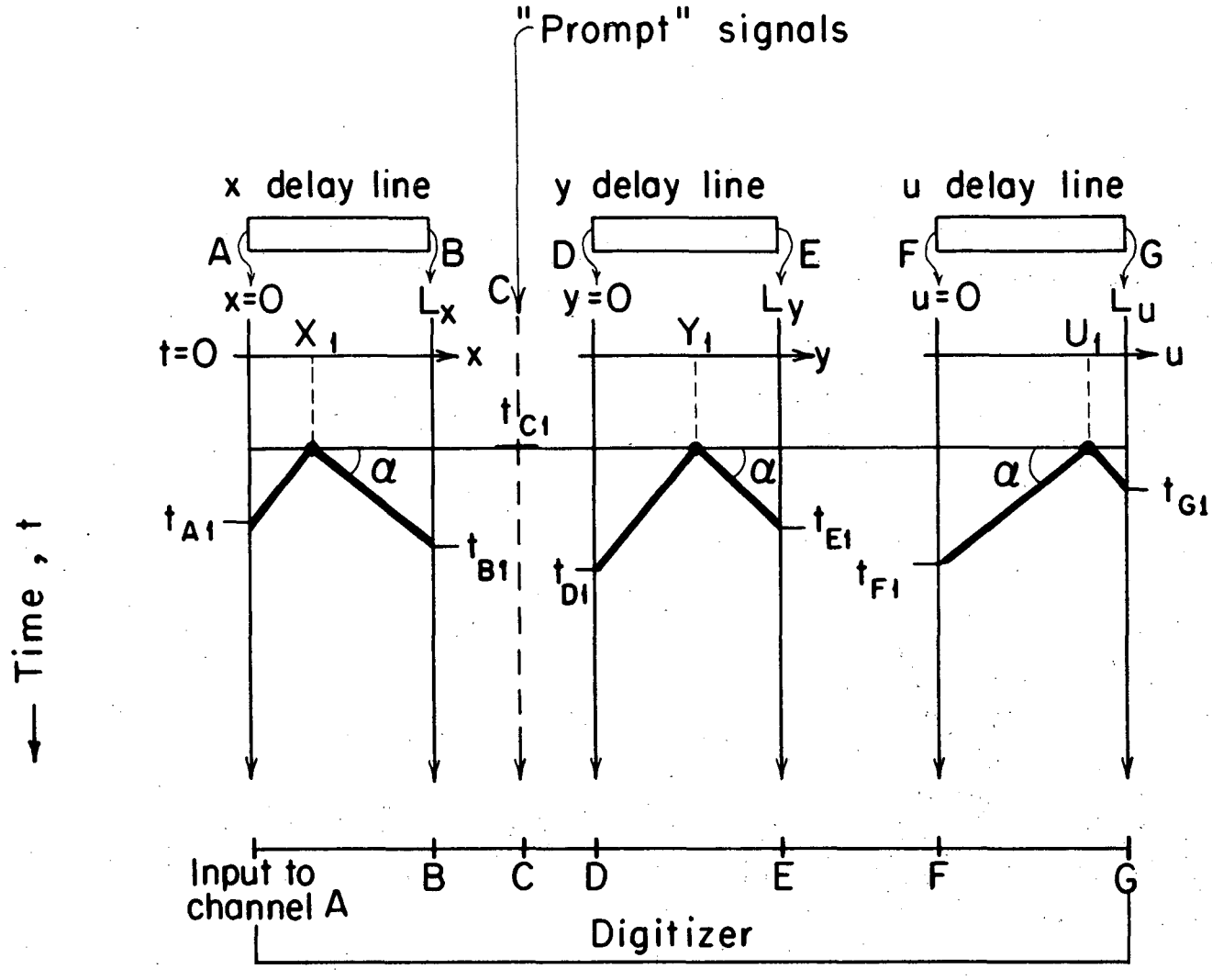

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Fig. 9

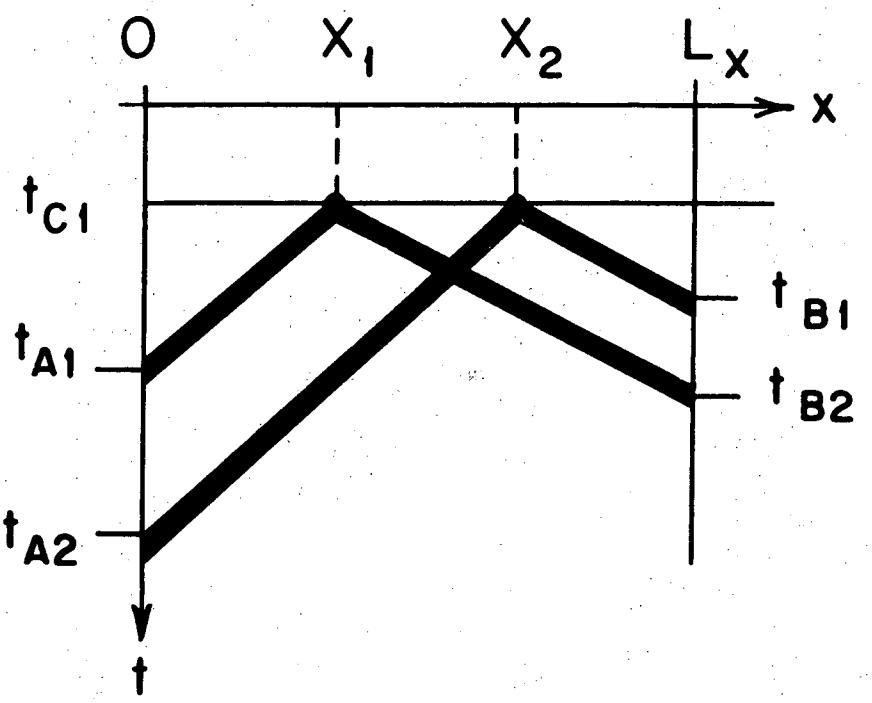

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Fig. 10

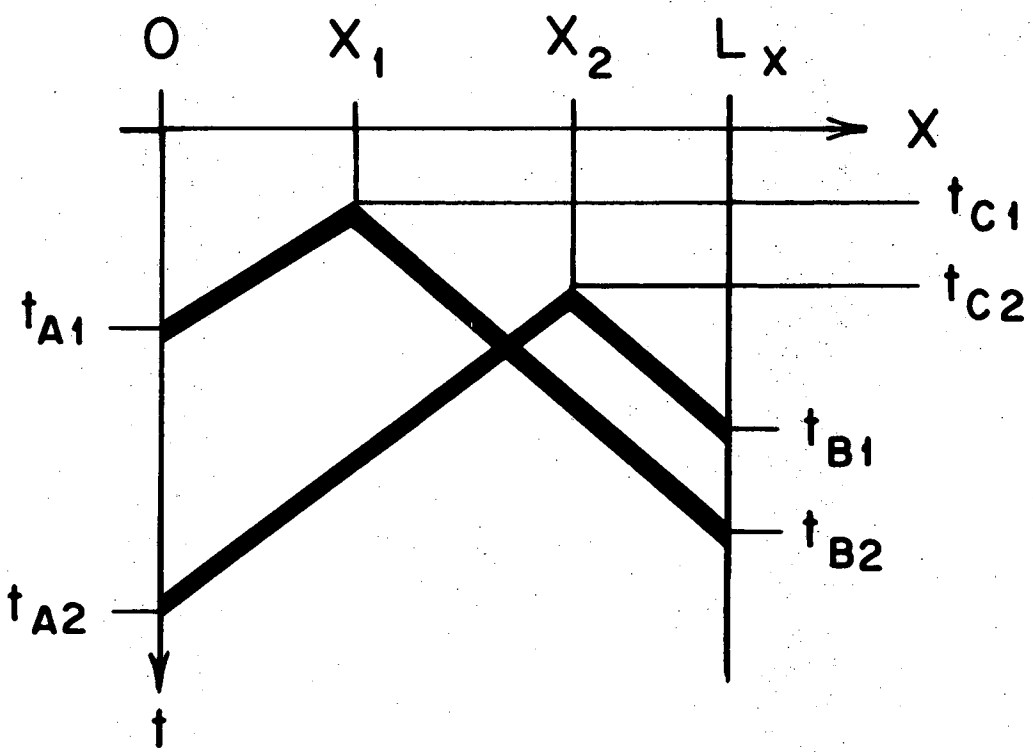

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Fig. 11

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