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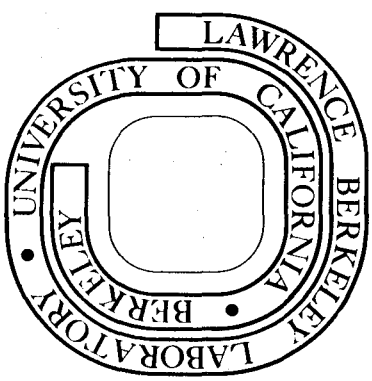

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Part II: High Precision Time Interval Digitizer

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February 25, 1977

Abstract

Position-resolution capabilities of the NASA-Goddard Space Flight Center satellite laser ranging systems are essentially determined by time-resolution capabilities of its optical timing receiver. The optical timing receiver consists of a fast photoelectric device, primarily a standard or microchannel-plate-type photomultiplier or an avalanche photodiode detector, a timing discriminator, a high-precision time interval digitizer, and a signal processing system. The time resolution capabilities of the receiver are determined by the electron time spread of the photoelectric device, the time walk and resolution characteristics of the timing discriminator, and the time interval digitizer. It is thus necessary to evaluate fast photoelectric devices with respect to their time-resolution capabilities, and to design a very low time walk timing discriminator and a high-precision time digitizer which are used in the laser ranging system receiver.

Part II of this report describes the development of a high precision time interval digitizer. The time digitizer is a 10 psec resolution stop watch covering a range of up to 340 msec. The measured time interval is determined as a separation between leading edges of a pair of pulses applied externally to the

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start input and the stop input of the digitizer. Employing an interpolation technique and a 50 MHz high precision master oscillator, the equivalent of a 100 GHz clock frequency standard is achieved. Absolute accuracy and stability of the digitizer are determined by the external 50MHz master oscillator, which serves as a standard time marker. The start and stop pulses are fast 1 nsec rise time signals, according to the Nuclear Instrument Module Standards. Each digitizer input is made level sensitive by means of tunnel diode discriminators. Firing level of the discriminator define start and stop points between which the time interval is digitized.

1. Introduction

Satellite laser ranging method has been used successfully for precise satellite orbit determination, polar motion determination, earth tidal parameters, high precision distance measurement between laser sites, and for calibration of space borne radar altimeters, [1]. More recently, an application of high precision laser ranging system has been proposed for geophysics investigation, particularly with respect to solid earth dynamics measurements and earthquake prediction, using a Laser Geodetic Satellite (LAGEOS), [2], and Space Shuttle, [3]. Since the pulsed laser ranging system determines the range to a target by measuring the time of flight of a short light pulse to the target and back, the system position-resolution capabilities are essentially determined by the time-resolution capabilities of its optical timing receiver. The optical timing receiver consists of a fast photoelectric device, primarily a standard or microchannel-plate photomultiplier or an avalanche photodiode detector, a timing discriminator, a high-precision time interval digitizer, and a signal processing

system. The time resolution capabilities of the receiver are determined by the time spread of the photoelectric device, the time walk and resolution characteristics of the timing discriminator, and the time interval digitizer. Consequently, it is necessary to evaluate available fast photoelectric devices with respect to their time resolution capabilities, and to design a very low time walk timing discriminator and a high-precision time digitizer which will be used in the High Resolution Laser Ranging System Receiver.

The constant fraction discriminator with a time walk of $\pm$ 40 psec or better, over a range of imput pulse amplitudes from 50mV to 5V was designed in the Electronics Research and Development Group of the Lawrence Berkeley Laboratory, [4]. Also, an evaluation of timing characteristics of high gain Amperex 56TVP photomultiplier, used in the receiver subsystem for the NASA satellite laser ranging work at Goddard Space Flight Center, was carried out, [5]. In the near future, a study of the time resolution capabilities of the very fast static crossed-field photomultipliers and optimization of their fast-timing characteristics will be carried out.

As a further step in the development of the high resolution optical timing receiver, it has been necessary to design a high-accuracy time interval digitizer with a time resolution of approximately 10 psec over periods as long as 340 msec.

This report describes the design of a high precision time interval digitizer. The digitizer is basically a very fast digital stop watch, where any individual time event, defined as a time interval between the leading edges of a start/stop pulse pair, is measured digitally with a precision of approximately 10 psec. Absolute accuracy and stability of the digitizer are determined by the externally supplied 50 MHz master oscillator, which serves as a standard time marker. Al-

though a number of systems have been devised for nanosecond time-interval measurements, based on various principles, [6,7], our analysis and design experience have shown that an operating principle based on the stretching of fractions of intervals between the start and stop pulses and the nearest time standard marks is the best method for the very high resolution requirements, [8-11]. These interpolated intervals are digitized along with the coarse interval between the markers. Employing this interpolation technique and a relatively low frequency but high precision master oscillator, the equivalent of a 100 GHz clock reference is achieved. The digitized time intervals are transferred to a PDP-11/40 computer via the CAMAC controller. The maximum dead time of the time digitizer is 50 microseconds, to which the measured time interval and computer processing time should be added.

The design of the time interval digitizer, which is an improved version of instruments described in Ref. 8, 9 and 10, is based on experience acquired over a number of years by the Electronics Research and Development Group spent developing high precision time interval digitizers and very fast timing discriminators for atomic and molecular subnanosecond fluorescence decay time measurements.

2. Operation Principle of the High Precision Time Interval Digitizer

A general block diagram of the high precision time interval digitizer and a photograph of the digitizer front view are shown in Figs. 1 and 3, respectively. Pertinent wave forms at the specified points in the block diagram and the principle of the system operation are shown in the timing diagram in Fig. 2.

Referring to Figs. 1 and 2 simultaneously, the measured time interval, T, which is defined as a separation between leading edges of a pair of pulses applied externally to the start input and the stop input of the digitizer, is split into three portions. T_1 is the portion between the leading edge of a start pulse and the second following time mark of the master oscillator of frequency $f_o=1/T_o$. The interval T_2 is defined similarly concerning the stop pulse. T_{12} is the interval between the two oscilator time marks. Therefore, the measured time interval is:

$$T = T_1 + T_{12} - T_2 \qquad (1)$$

The intervals T_1 and T_2 are stretched in two identical time-to-time converters. The conversion constant k is an integer and selected to be $k=T_o/T_e$, where T_o is the master clock period and T_e the time resolution desired. Since the digitizer readout is selected to be binary, and T_o is equal 2×10^{-8} sec, a value k=2048 leads to a time resolution of $T_e=T_o/k=1/f_o k=9.766\times10^{-12}$ sec. The stretched portions of T_1 and T_2 are synchronized to the master oscillator. The portions are digitized and the resulting pulse bursts are stored in their respective binary scalers. At the same time, the interval T_{12} is converted into a pulse burst counted by the main scaler. Since the weight of each count in the main scaler is kT_e, it is important that no ambiguity exists in digitizing T_{12}.

The contents of the scalers after the conversion is completed are $N_1=kT_1/T_o$, $N_2=kT_2/T_o$, and $N_{12}=T_{12}/T_o$, for time intervals T_1, T_2 and T_{12}, respectively. Since $k_1=k_2=k$,

$$T/T_o=N_1/k+N_{12}-N_2/k. \qquad (2)$$

The time interval T is measured with an error of

$$\Delta T=T\Delta f_o/f_o+T_e(\Delta N_1-\Delta N_2) \qquad (3)$$

Where $\Delta f_o/f_o$ is the stability of the master ocillator, and ΔN_1, and ΔN_2 are interpolation conversion errors. The second part of Eqn. 3 can be minimized if both interpolator converters track each other perfectly. The first part of Eqn. 3 is negligible for short intervals. Consequently, the required master oscillator

stability should be better than 10^{-10}. Furthermore, an additional error is made if the oscillator frequency is modulated by any source. Therefore, a modulation-free master oscillator is imperative to reduce the spread of events measured, or when the total number of events accumulated is not large enough to minimize statistical error.

3. Description of the High Precision Time Interval Digitizer

The Digitizer is a 9.76 psec incremental resolution stop watch covering 10 ranges of up to 340 msec. The measured interval is defined as separation between leading edges of a pair of pulses applied externally to the start input and the stop input of the Digitizer. The start and stop pulses should be fast NIM signals. Typically, rise times are about 1 nsec. Each input is made level sensitive by using a tunnel diode discriminator. The firing level of each discriminator is set to slightly less than half the NIM signal (i.e., at 300 mV into 50-ohm load) and these two levels define start and stop points between which the time interval is being digitized.

The Digitizer is intended to work on-line with a computer or suitable digital storage memory. It has two 35-bit binary registers, which also can be used in manual operation of the Digitizer. Each event is initially stored in the first register and then shifted into the second register. The first register is then free to accept a new event. The two events remain stored indefinitely until either register is cleared.

Each register has its own display. The second register display is an array of 35 light emitting diodes (LED's) presenting the content in straight binary system. The first register, although also binary, has a decimal display to make manual operation easier. The total range of 11 decades is displayed by two 6-digit decimal displays on the front panel of the Decimal Display Module.

The PDP-11/40 computer has been selected for processing data

supplied by the Time Digitizer. In order to make use of easily available hardware and software for the interface between the Digitizer and the computer, the CAMAC system has been selected. Since CAMAC hardware requires a CAMAC crate, the Digitizer also was designed as a CAMAC compatible modular system.

The Time Digitizer comprises 6 modules, each occupying 2 stations in the CAMAC crate (Fig. 3a). They fill up all available stations in a 12-station rack mount CAMAC minicrate. The other half of the crate contains the power supply, which makes the total size of the package equal to that of a standard NIM bin.

A general block diagram of the digitizer system is shown in Fig. 1. The system consists of a start interpolator, a stop interpolator, a clock with calibrator, a logic unit, a buffer register, a decimal display module and a crate controller for the interface to a PDP 11/40 computer. Providing that the Digitizer is initially not disabled internally and not vetoed externally, the leading edge of a start pulse initiates time-to-time conversion of T_1 in the Start Interpolator. This conversion results in generating a start gate pulse that controls the number of clock pulses N_1 which is counted by the Start Scaler of the Logic Unit. Also, the start gate pulse which is synchronous with the master oscillator markers initiates the burst N_{12} of clock pulses counted by the main scaler. Each main scaler count is worth 2048 counts stored by the start or stop scaler.

When the main scaler accumulated the preselected number of counts as set by the front panel switch, a Stop Enable signal is generated that opens the stop gate to the Digitizer's Stop Interpolator. All stop pulses that might have arrived prior to that were ignored. Any valid stop signal pulse entering the enabled stop input initiates time-to-time conversion of T_2 into

the stop gate pulse. The stop gate controls the number of clock pulses N_2 counted by the Stop Scaler. The leading edge of the stop gate also closes the gate to the Main Scaler, terminating the main scaler pulse train N_{12}.

After all of the counting is completed, the content of the Start Scaler and the complement of the content of the Stop Scaler are summed up in the 12-bit adder, performing the $(N_1-N_2)/k$ part of the Eq. 2. The "2^{11}" and "2^{12}" Carry, if any, are then added to N_{12} contained in the Main Scaler. Now the first 11 bits of the Adder, along with the new content of the Main Scaler, represent in straight binary fashion the right hand side of Eq. 2.

Both time interpolators have to be identical in order to expand equally the fractions T_1 and T_2 of the clock period T_o. The expansion ratio k should be made as constant as possible. Here k=2048 has been selected because of the design considerations. Since the same clock frequency $f_o=1/T_o$ is used to digitize the expanded portions of T_1 and T_2, each counted period T_o equals $T_o/k=20\times10^{-9}/2048=9.76\times10^{-12}$ sec.

In other words, each interpolator is an independent 9.76 psec-resolution time stretcher covering the range of about 30 nsec. The interpolators used here need resolution 5 to 10 times better than current commercially available time stretchers. Through careful design, thermal drift and jitter due to noise and imperfect clock-frequency lock-in can be kept low enough to maintain the desired resolution. Also, since in the measured interval appears the difference N_1-N_2 of the start and stop interpolation, errors due to individual thermal drift tend to cancel each other if good tracking of the two interpolators is achieved.

Jitter due to various sources of noise causes the departure from an ideally rectangular channel profile in each interpolator. Major contributors are component noise, power supply ripple, and clock frequency lock-in noise. All of these contribute to the differential nonlinearity of the individual interpolator, causing

a more trapezoidal shape of the channel profile. The combined effect of the two interpolators results in averaging the effects of the supply ripple and clock noise, which is responsible for inherently good linearity of the time digitizer as a whole.

Circuitwise, the Start Interpolator consists of a time-to-time converter (stretcher) that charges a capacitor with a constant current for the duration of the small time interval T_1 from the leading edge of the start pulse to the next clock pulse. From there on the capacitor is being discharged by a constant current 2048 times smaller than charging current. A comparator monitors triangular waveform across the capacitor, generating a square gate pulse 2048 times longer than the original charging interval. That pulse opens a gate, passing a burst of clock pulses whose number is proportional to its length. The start burst pulses are shaped and counted by the start scaler in the logic module, where each event is further digitially processed.

The required stability and accuracy of the stretchers was obtained by the selection and matching of the critical components. Very high bandwidth components are needed for low jitter synchronization of the interpolators with the clock frequency oscillator. Fast level discriminators are used to accept start and stop input pulses in order to precisely define the beginning and the end of each measured interval. The start and the stop inputs are D.C. coupled and any noise superimposed upon the baseline of the start and/or stop signals results in timing error because of the time shift in discriminator firing. Propagation delay of start and stop input signals through the interpolators is made as short as possible in order to minimize time offset error. This shortening of the paths also provides better thermal tracking.

Each interpolator generates a fast NIM Busy output at the front panel. The Busy signal lasts until the conversion process

of the measured time interval is over and data is transferred to the buffer register in the logic module. The inputs are internally inhibited during the busy time of each interpolator. External selection of coincident events is possible by applying an appropriately timed NIM signal at the gate input on the front panel. Coincidence or anticoincidence mode can be selected by a switch.

To obtain maximum time resolution, the start interpolator and/or the stop interpolator must be aligned. This adjustment can be made by a rear panel potentiometers if needed. Alignment procedure is described later in this text.

The stop interpolator is identical to the start interpolator except for the labeling of front and rear panels. Normally, the stop input is disabled. After an accepted start pulse had iniated the conversion, a stop signal can be accepted only after a pre-selected time has elapsed. Nine ranges of stop enable time can be selected by a switch in the logic unit. A final position is provided which makes the stop interpolator independent of the condition of the start interpolator. This is used in measurement of very short time intervals.

When a stop pulse is accepted, the stop interpolator generates a stop gate signal (Fig. 2). The width of this signal is 2,048 times longer than the fraction of the interval T_2 between the stop pulse and the synchronizing clock pulse that follows it. The gate pulse is being digitized by N_2 of the clock pulses which are stored in the stop scaler. The leading edge stops the coarse counting of the main scaler in the logic unit. A NIM stop busy signal is available at the front panel for external timing and monitoring. A gate input connector is provided which permits the external selection of coincident stop pulses. Coincidence or anticoincidence mode can be selected by the front panel switch.

The Logic Unit contains several sections of the digitizer. These include the start, the stop, and the main scaler, the adder,

the buffer register, and the binary display. The start and stop scalers store digitized interpolated intervals T_1 and T_2 and the main scaler digitizes the coarse intervals T_{12}. The simple arithmetic operations indicated in Eq. 2 take place in the adder and the control logic. The result is a 35-bit binary word covering time intervals of up to 340 msec. The least significant bit represents a time increment of 10/1.024=9.76 picoseconds. After the conversion is completed, the data is transferred into the second 35-bit buffer register. The scalers and the logic are cleared for the digitizing an another event. The buffer register can be read out and reset by the computer via CAMAC Dataway. Data stored in the register is being displayed on the front panel 35-bit LED array.

Other lights give the status of the registers. As long as the data is stored in the scaler register its "Ready" light is on. The "Overrun" light blinks for every event where the time interval measured is longer than the selected range of the Digitizer. Ten ranges can be preselected by the front panel switch. Another ten-position switch preselects stop enables time intervals as described before. The buffer register "Ready" light is on when there is data stored there; the "L" light is on when a request for service is sent to the CAMAC dataway and the "N" light goes on each time the buffer register is being addressed by the computer. Also, the registers can be cleared manually by independent front panel push buttons.

The Decimal Display module converts the binary content of the scaler register into a decimal number. The number is displayed on the front planel in two 6-decade rows. The rear panel contains connectors for the cables transferring the data from the Logic Unit. The display is enabled as soon as each event is digitized and lasts until the scaler register is cleared. This display is intended as a stand-alone unit and does not affect the operation of the Digitizer.

The Crate Controller is an ORTEC, Inc. DC011 module for CAMAC interfacing of the Time Digitizer and the PDP 11/40 computer. The Controller should occupy stations #24 and #25 of the CAMAC crate. The front panel connector is tied to the computer via an ORTEC, Inc. BC-11A-10 cable.

3a. Clock Oscillator Description

All timing functions of the Time Digitizer are synchronized by the master clock oscillator located in the Clock Module. The circuitry comprises a crystal oscillator, pulse shaping circuits and buffer amplifiers. The block diagram is shown in Fig. 4.

The crystal oscillator is the temperature compensated Model MOE-10 made by International Crystal Manufacturing Company, Inc. It has an overall accuracy of +0.0005% between -10°C and +60°C.

A front panel mode switch controls the gates G_1 and G_2, selecting either the internal clock oscillator or an external clock supplied via front panel connector. Either signal passes OR gate, OR_1, into buffer amplifiers A_4 and A_5. Amplifier A_4 feeds the main clock timing signal to the logic unit, and A_5 provides a clock source for external use (for instance, to drive the Calibrator or an external frequency monitor).

Amplifiers A_2 and A_3 feed spike shaped clock pulses to start and stop interpolator modules. A differentiator G_3 and D shapes the rectangular oscillator waveform into sharp spikes a few nanoseconds wide. The phase relationship between the clock outputs is important, and it is essential that the connecting cables between the clock module and the other modules are not interchanged.

A_1 is a buffer amplifier for the external clock input and also a logic level translator. A typical input signal of 1 volt peak-to-peak into 50 ohm load is sufficient. Frequency

required is 50 MHz. The input to the Time Digitizer is A.C. coupled to prevent overload damage. At the same time this serves as a filter for low frequency noise.

It is essential for the operation of the Digitizer that the external clock reference be free from any kind of modulation. Since the high resolution of the Digitizer is based on a very accurate phase lock-in, any phase and frequency modulation of the clock will result in a distribution rather than a sharp peak when a constant time interval is being repeatedly measured.

3b. Calibrator Description

A precision pulse generator for calibrating and test purposes is incorporated in the Clock Module. It is completely independent except that it needs an external frequency standard. Essentially, the Calibrator is a digital frequency divider. Regardless of the selected range, the output of the Calibrator retains a constant phase relationship with the input reference clock. The jitter of the calibrating output referred to the clock is estimated to be less than 1 psec for all ranges. The stability of the selected time range is therefore dependent only on the external standard.

Calibrator block diagram and its timing diagram are shown in Figs. 5 and 6, respectively. A reference clock signal passing the level translator T_1 and gate G_1 continually keeps running a 34-bit ripple-through binary scaler. At the same time the signal is applied to the gate G . The outputs of the first two binaries B_1 and B_2 control G_2 along with the logic status of the OR gate, OR_1. For instance, if the shortest range (2^2) is selected by the range switch, OR_1 passes logic "1" to G_2. Whenever the second binary B_2 goes to "1", the trailing edge of the next clock pulse will set B_1 to "1", opening G_2. The following clock pulse passes free through G_2 and the NIM fast logic amplifier A to the output connectors. The trailing edge

of the next clock pulse will set B_1 to "1", opening G_2. The following clock pulse passes free through G_2 and the NIM fast logic amplifier A to the output connectors. The trailing edge of the same pulse sets B_1 and B_2 to "0" as the counting continues. Frequency division by 4 is thus performed.

Ten ranges can be selected by the front panel switch by applying logical "1" to any of the selected OR_1 to OR_{10} inputs. Each higher step includes three more scaler bits, increasing the frequency division by a factor of 8. If the position "2" is selected, for instance, OR_2 keeps G_3 enabled. At the point when 2^5-1 clock pulses have been counted, all the G_2 and G_3 inputs will be logic "1". The next, 2^{5th} clock pulse will be passed through G_2 to the outputs.

The leading edge of the output pulses are delayed with respect to the leading edge of the clock pulses by the amount of propagation delay through T_1, G_1, G_2 and A. This delay is constant regardless of the range selected. Therefore, the stability of the period between two successive output pulses depends only on the quality of the reference clock.

Calibrating of the Time Digitizer is performed by applying the outputs of the Calibrator to the Start and Stop inputs of the Digitizer. When the Digitizer is ready, the stop input is internally inhibited. Therefore, the start pulse that initiates the Digitizer will be rejected at the stop input since they are simultaneous. The next start-stop pair will be accepted by the stop input and rejected by the start input, which has remained busy since the acceptance of the previous pulse.

The exact period between the two events will be thus digitized since both Digitizer inputs are in fact tied in parallel.

If an external clock standard of known accuracy is used to operate the Calibrator, the overall accuracy of the Time Digitizer will be measured. Total error of measuring an interval T is

approximately

$$\Delta T = \left|\Delta T_{st} - \Delta T_{sp}\right| + T\left|\Delta f_o/f_o\right| \qquad (4)$$

ΔT_{st} and ΔT_{sp} are errors of start and stop interpolation and $\Delta f_o/f_o$ is the stability of the reference clock oscillator that runs the Digitizer at the time of measurement.

The two errors can be separated by measuring first the short intervals for which the frequency error is negligible. Then the total error is determined next by measuring long intervals.

Self-testing the clock frequency standard for modulation error is made possible by using Digitizer's Clock Output to run the Calibrator. This makes the start and stop input signals synchronous with the Digitizer's clock system. When using a trombone delay line in a series with the stop input, it should be so adjusted that the centroid of the measured line is symmetrical. If the interpolators are properly aligned, more than 90% of the counted intervals fall into the same 10 ps channel and the rest into the two adjacent channels. By changing the range of the measured interval, the distribution should remain the same. For each range, a different, more distant clock cycle is selected for the stop interpolation. Therefore, if any broadening of the distribution results, it can be attributed only to the phase jitter of the clock frequency standard.

3c. Start Interpolator and Stop Interpolator Description

The start interpolator and stop interpolator modules are identical except for different labeling on the front and rear panels. In all other respects they are made as identical as possible in order to ensure good thermal tracking.

Each interpolator is in fact an analog time-to-time converter. The start interpolator stretches the small time interval between the start input pulse and the second clock pulse following its leading edge by a constant multiplication factor. Similarly, the stop interpolator stretches the time interval between the

stop input pulse and the second following clock pulse by the same factor.

A simplified block diagram and corresponding timing diagram (not in scale) are shown in Figs. 8 and 9. Let's assume that the interpolator has been cleared previously, and the mode switch is set to "Anticoincidence". This condition makes both inputs of OR_{ac} gate in logic zero as long as there is no gate signal present at gate input (this condition maintains at zero one input of G_a and one input of G_c all the time). Therefore, input gate G_i is enabled, and start input pulse will pass it to set the latch L_i. P protects the input circuits against accidental overload. L_i opens G_1 of the clock synchronizer circuit. The first, next clock pulse will pass G_1, and by feedback to OR_1, the output remains in logic "1" state as long as L_i is set. Because of clock delay DL_2, gate G_2 opens about half the clock period later, so that one more clock period later G_2 is latched up by feeding back its output to OR_2.

Some time before this happens, gate G_{ia} has been opened by the delayed output of L_i. This delay is selected to be 3/4 of one clock period. At the time G_{ia} is opened, G_2 is still in logic "0" state, keeping G_{ia} enabled, and the output gate G_s disabled. Therefore, the G_{ia} passes the delayed start signal that initiates charging with constant current the storage capacitor in the Time Stretcher. The comparator circuit in the stretcher feedback loop senses the increase of the voltage across the charging capacitor. Switching to logic "1" state, the comparator opens a feedback loop that maintains constant voltage across the capacitor only when in steady state. At the same time, it enables the output gate G_s. The charging to the stretcher stops when G_2 goes to the state "1". Discharge of the storage capacitor in the stretcher by a constant current set to be exactly k times smaller than the charging current; in this case, k=2048. Therefore, k-times more time is needed to

discharge the capacitor back to the initial level. When this is achieved, the comparator goes back to logic "0", closing G_s and activating again the feedback loop. Due to the feedback, further discharge is stopped and the initial quiescent level maintained. Therefore, the output of the G_s is a logic pulse that starts in synchronization with the clock and is exactly k-times longer than the original time interval. The stretched interval is digitized by counting clock pulses by the Start Scaler in the Logic Module. Each clock pulse thus represents $T_o/k=20\cdot10^{-9}/2048=9.76$ psec.

Until cleared by the Logic Unit, the interpolator remains busy. All subsequent input pulses during the busy time are being rejected. The Busy Output signal can be used for external timing purposes.

Each successive accepted start pulse will produce a start gate pulse of different width since the start pulses come at random with respect to the clock. The same holds for the stop input pulse in the stop interpolator. Since the measured start-stop interval is proportional to the difference of the start and the stop interpolation, good averaging results when the same start-stop intervals are repeatedly measured, leading to inherent excellent linearity of the Digitizer as a whole.

3d. Logic Unit Description

The Logic Unit comprises most of the digital and logic circuit of the Digitizer. The unit operation is controlled by the signals received from the Start and Stop Interpolators, the Clock Oscillator, as well as by the digital informations received by the computer via a CAMAC crate controller. The Logic Unit consists of the scaler input logic and control logic, the scaler register (start scaler, stop scaler, main scaler and adder), buffer register, binary display and CAMAC logic. Figs. 12A, 12B, and 12C show the Logic Unit block diagram. The timing dia-

gram for the Logic Unit is shown in Fig. 13.

3da. Scaler Input Logic and Control Logic Unit

Three signals define the sequence of operations: The main clock pulse from clock module, start gate pulse from start interpolator and stop gate pulse from stop interpolator. The leading edges of start and stop gates are being synchronized by the interpolators, and they appear between two clock pulses so that no ambiguity exists in timing, which is crucial for the operation of the Time Digitizer.

Start gate always precedes a stop gate, since the start interpolator enables, in turn, the stop interpolator. An exception is when Stop Enable Switch is in Position 1. In this position the stop interpolator is enabled at the same time as the start interpolator. If a stop input signal arrives before the start pulse is accepted by the start interpolator, an error in measurements results,because the Digitizer is not wired for measuring negative time intervals. External logic provided by the user should prevent such an event.

Normally, the start gate, arriving first, sets the latch L_1 by passing the normally open gate G_3. Main gate G_m is now open, passing clock pulses toward the main scaler. Also, for the duration of the start gate, G_1 is open passing clock pulses to the start scaler. They pass discriminator-shaper circuit D_{10}. The clock pulses normally do not require additional shaping except for the last one in the series. The width of the start gate pulse is the result of the stretching in the interpolator and, unlike the leading edge, the trailing edge is not synchronized with the clock. G_1 can close any time, chopping off a fraction of the last clock pulse in the series. The toggling of the first binary in the scaler becomes ambiguous as the last clock pulse gets narrower. Most binaries have one toggle threshold for the even state and another one for the odd state. In the-time-to digital conversion this results in different widths for even and odd channels, which can drastically affect the

differential linearity of conversion. In order to avoid this, the discriminator D_{10} reshapes all the clock pulses including the last one, if it was large enough to exceed the threshold. Ambiguity in scaler counting is thus eliminated and a differential linearity plot free of even-odd pattern achieved.

The trailing edge of the start gate pulse closes G_1, stopping the counting in the start scaler. At the same time G_2 is enabled, passing the logic level "1" to G_3 and G_7. G_3 remains disabled until L_1 is cleared, and G_7 is enabled.

A similar sequence takes place when the stop gate pulse is received from the stop interpolator. The difference is that G_m is disabled when L_2 is set by the leading edge of the stop gate pulse. This ends the pulse series to the main scaler. The stop scaler pulse series continues until the trailing edge of the stop gate closes G_4 and, by opening G_5, passes the logic "1" level to G_6 and G_7. G_6 remains disabled until L_2 is reset, and G_7, having logic "1" at both inputs, generates an "end of conversion" signal that propagates through a series of delay circuits. At the same time, this signal is available at the rear panel for oscilloscope triggering.

At this point all the counting is done. The delay circuit D_1 allows for the ripple-trough scalers and adders to settle. A series of delay circuits, D_2, D_3 and D_4, propagate the end-of-conversion signal in three steps. Gates G_8 and G_9 generate two strobe pulses of the width D_2 and D_4, respectively, which are separated by D_3. Strobe pulses are used to check the status of the adder circuits. If the 12^{th} bit of the adder is in the logic state "1", one pulse (worth 20 nsec.) should be added to the content of the main scaler. The next strobe pulse tests the status of "Carry 13" of the adder. If C_{13} is in logic "1" state, a pulse will be generated that adds one count to the second binary (worth 40 nsec.) of the main scaler (Fig. 12b).

After an additional delay D_5, the final decision to accept the event or not is made by the Data Selector Module. The Data Selector Module was designed to sort out events of a certain category through external programming. However, for this version of the Time Digitizer a Data Selector Module has not been requested. Therefore, the gate G_{10} is wired to be permanently enabled, and G_{11} is permanently disabled. The output of G_{10} provides a "Ready" signal that will initiate the transfer of data into the buffer register. The front panel "Scaler Ready" light goes on for the time the "Ready" signal is present. It stays on indefinitely as long as the buffer register is busy. If the transfer occurs immediately, the single shot circuit SS_2 is triggered producing a short blink for every event.

The scaler and interpolators can be cleared and/or inhibited in several ways, as shown in 12a.

1. CAMAC Inhibit. A logic "1" level from CAMAC Dataway passes G_{12}, OR_3, and OR_4, clearing all scalers and latches, and keeps blocked the inputs to the Time Digitizer. If an event is being processed at the moment the inhibit signal is applied, G_{12} is closed until the event has been transferred into the buffer register. After the transfer is accomplished, G_{12} will be enabled and all subsequent events inhibited.

2. $Z.S_2$ from CAMAC. This is a CAMAC "Initialize" command, received by the Digitizer via the CAMAC Dataway. It clears all scalers and latches (except the buffer register), making the Time Digitizer ready for operation.

3. Reset from the Register. A pulse is generated by the buffer reguster after the data transfer into the buffer has been accomplished. A new event can be processed by the Digitizer immediately afterwards.

4. Scaler Clear. The front panel push button clears all scalers and latches. A new event can be processed by the Digitizer immediately after the push button is released.

5. Enable Latch. Each time a clear signal has been generated, the Enable Latch is reset. Its complement output keeps the stop interpolator cleared and disabled. When a new event starts the Digitizer, the latch L_3 will be set only after a present number of counts in the main scaler has been reached, as selected by the Stop Enable Switch. OR_5 will then enable the stop interpolator.

6. Overrun Clear. In case no stop pulse is received after the Digitizer has been started, the main scaler will trigger the single shot SS_1 after a preset number of counts is reached, as selected by the Range Switch. The clear pulse generated by SS_1 will stop further counting, reset all scalers and latches and enable the input of the Digitizer for a new start.

3db. Scaler Register Logic

Most of scaler register logic has been described already in the Control Logic Section. This section consists mainly of a 12-bit 50MHz start scaler and a stop scaler, a 12-bit Adder, a 12-bit Stop Scaler Logic Inverter, a 24-bit 50MHz main scaler and 12-bit output gates. A block diagram and timing diagrams are shown in Figs. 12b and 13.

Pulse trains being counted by the three scalers are generated by the control logic. Bear in mind that each count in the main scaler is worth 20 nsec, and each count in the start or stop scaler is worth 2^{11} times less. In other words, the 12th bit of the start or stop scaler has the same weight as the first bit of the main scaler. Since the counting can be done simultaneously in all three scalers, the final arithmetic operations are performed after all the counting is over.

As it was described earlier, the result of counting should be

$$N = N_{st} + 2^{n-1} N_{mn} - N_{sp} \qquad (5)$$

where N_{st}, N_{mn} and N_{sp} are the reading of the start, main and stop scalers, respectively, and $n = 12$ is the total number of bits in the start and stop scalers. Since $N_{sp} = 2^n - 1 - \overline{N_{sp}}$,

(5) becomes

$$N = (N_{st} + \overline{N_{sp}} + 1) \quad -2^{n} + 2^{n-1}N_{mn} \qquad (6)$$

Since (6) is a simple operation, the part of (6) in the parenthesis can be done first by adding the contents of the start scaler, the complement of the stop scaler, plus 1 in a 12-bit adder circuit.

Next step is to test the status of the 12th bit and carry (C_{13}) output of the adder. The control logic generates two successive strobe pulses. If $S_{12}(2^{11})$ is "1", G_1 passes the strobe pulse, and the first binary of the main scaler is advanced by one count. Similarly, the next strobe pulse tests C_{13} (gate G_2), and if C_{13} output is "1", one count pulse is added to the second binary of the main scaler through OR_2. Differentiator D is placed before OR_2 to produce a pulse for each even count of B_{12}.

When this operation is completed, the Decimal Display Strobe from Control Logic passes the content of the adder through a gate G. The first 11 bits (A_1-A_{11}) will later be strobed into the buffer register along with the 24 main scaler bits. However, all 12 bits and carry C_{13} from the adder are supplied to the decimal display module via the rear panel connector.

3dc. Buffer Register Binary Display and CAMAC Logic

When the conversion of a start-stop time interval is accomplished, the "ready" logic level (waveform v) in Fig. 13 is generated. The digitized event becomes a 35-bit binary word that remains stored in the scalers until the transfer into the buffer register is accomplished.

The register consists of 35 latches into which the whole 35-bit word can be strobed at the same time. The block diagram is shown in Fig. 12_c. Latch L_1 keeps track of the register status. If the register has been cleared before, the latch L_1 will be set by a new ready signal. After a delay (D_1), new data is strobed into the buffer. Delay D_2 and gate G_1 generate a reset signal

by opening G_1 at the end of strobing and closing it after the signal has been propagated through D_2. Reset is sent back to the control logic (Figs. 12A and 13), which further resets the scalers and interpolators as described earlier.

As this is done, G_2 passes the "Read Ready" signal through a buffer amplifier, A_1, to the L ("Look at me") line of the CAMAC Dataway. It has been assumed that this CAMAC station has not been addressed at that moment; i.e., N was logic "0".

As a response to the "L" request, typically a CAMAC read-out cycle into the computer via crate controller would follow. The 35-bit word can be read out in three bytes of 12 bits each. No other than read-out functions are necessary, and therefore, the Function Decoder responds only to F(0) (Read-out the Buffer Register) and F(2) (Read-out and clear the Buffer Register). The CAMAC Subaddress Decoder responds to A(0), A(1), A(2) and A(3). $N \cdot F(0) \cdot A(0)$ reads out the bits B_1-B_{12} into R_1-R_{12}, Read Bus Lines of the Dataway. Similarly, $N \cdot F(0) \cdot A(1)$ reads out the bits B_{13}-B_{24} and $N \cdot F(0) \cdot A(2)$ reads out the bits B_{25}-B_{35} into the same R_1-R_{12} Read Bus Lines. If the function F(2) is selected, the result is the same except for the third step, when $N \cdot F(0) \cdot A(2)$ will result in the read out of the third byte and the reset of the L_1 latch by the clear pulse S_2 at the end of the same CAMAC cycle. (F(0) and A(2) set G_8 into logic "1" state, which enables G_9 through OR_4. S_2 pulse at the end of the CAMAC cycle will then pass G_9 and reset L_1 through OR_1)

In case a new event has been digitized in the meantime, a new "Ready" signal is already waiting at the set input of L_1, and new data at the input of the register. For the duration of the reset pulse the output of L_1 goes to "0" and then immediately back to "1" as the reset pulse disappears. A new read-in cycle starts then as before.

Until cleared, any two successive events can be held in the Digitizer indefinitely. As long as this condition persists, the Digitizer remains busy, and all subsequent start-stop pulses

will be rejected.

In accordance with the CAMAC rules, all valid N·F·A combinations will result in a Q and X response. Also, the register can be cleared upon the receipt of $C.S_2$ instruction via CAMAC. If $Z.S_2$ instruction is received, whole Digitizer is cleared, including the register. For convenience, the front panel "Ready", "L" and "N" lights go on when the register contains data, an L-request sent to the Dataway and/or the module is addressed by receiving an N signal from the Dataway. A front panel LED array displays the content of the register continually.

A front panel push button is provided for manual clear of the buffer register. Each time the push button is released, a new event will be automatically strobed into the register. A manual reset of scalers and interpolators by another push button will not affect the register. In this manner, complete manual operation of the Digitizer is possible. Of course, in that case, only visual display read-out is possible. Bear in mind that the LED array displays the content of the register, and the decimal display shows the content of the scalers, which are two different events. When the register is cleared, the new display shows in binary fashion the same event that was shown before by the decimal display.

3e. Decimal Display Module Description

The Decimal Display Module serves one purpose only - to give the experimenter a quick visual indication of what time intervals are really being measured and stored in the computer. Although the same information is already available on LED array displaying the content of the buffer register, it is hard to quickly interpret a 35-bit binary word in decimal fashion.

Binary-to-decimal conversion of a 35-bit long word takes too much time after each conversion is over, and that means the reduction in rate of events to be digitized. Faster converters

of this size require too much power and circuitry. In the decimal display described here, the decimal conversion takes place in the same time that the actual counting goes on in the logic module of the Time Digitizer.

An additional problem has to be resolved. Due to 50 MHz reference clock frequency used in the Digitizer, the basic coarse time intervals of $1/f_o = T_o = 20$ nsec. are counted by the main scaler. Employing interpolation, this basic interval is digitized in binary fashion by 12-bit words, the least significant bit of which is equal to $T_o/2^{11} = 20 \cdot 10^{-9}/2{,}048 \simeq 9.76.10^{-12}$ sec. The simple conversion of the whole binary number into the decimal system will give a decimal readout, but not in decimal fractions of the second, because the least significant bit equals less than $10 \cdot 10^{-12}$ sec.

When the measured interval is presented in straight binary fashion, the 11^{th} bit has the weight of $10 \cdot 10^{-9}$ sec. Therefore, if a binary word starting from the 11^{th} bit up to the final 35^{th} bit is converted into a decimal number, the whole range is covered by 8 decades, where in the lowest decade the unity is worth 10 nsec. increasing by a factor of 10 for each decade. The readout of the last 8 decades is thus given in decimal fractions of a second.

The first 10 bits of the original binary number amount in real time to slightly less than 10 nsec. In a mathematical sense, they represent any number from 0 up to 1,023 maximum. If a separate 10-bit binary-to-decimal converter is used, the result can be displayed in 4 decades. The only digits that can appear in the highest decade are either zero or one.

In order to get the result in picoseconds, this 4-decade number should be divided by 102.4. No attempt has been made to perform this operation circuitwise. These 4 decades occupy the right hand side of the lower 6-digit display on the front panel of the Decimal Display Module. The two remaining digits on the

left hand side and the six digits of the upper display together make up the 8-decade decimal display in real time, as described before.

To summarize, the display arranged in this manner gives two kinds of reading. First, the time interval is given in decimal fractions of a second over 8 decades. The unity of the lowest of 8 decades is 10 ns. Three more decades (1 nsec., 0.1 nsec., and 0.01 nsec.) are displayed by the last 4 digits. The real time is obtained by dividing the reading of this 4-digit number by 102.4. Since this number cannot exceed 1.023, the maximum real time it represents is 9.99 nsec.

Secondly, all 12 digits displayed still give the exact decimal representation of the 35-bit binary word. The unity in the lowest decade is equal to the least significant bit of the binary number. The lowest four digits can be any number from 0 up to 1,023. When this number if 999 or less, the fourth digit is blank, and the remaining 11 digits display the exact result of binary to decimal conversion. If the last four digits display 1,000 to 1,023, a carry of one should be added to the adjacent, the 5th decade on the left, and the result will still be correct.

The logic diagram and timing diagram of the Decimal Display Module are shown in Figs. 15 and 16, respectively. The 8-decade BCD scaler is cleared before the new conversion starts, along with the scalers in the Logic Module. When the new time interval conversion starts, the same pulse train that is being counted by the main scaler in the Logic Module is also fed into this BCD scaler. Since each pulse in the train is worth 20 nsec., they are fed into the quinary section of the first binary coded decade. Each count, therefore, advances this decade by two because in this decade each increment means 10 nsec. The remaining 7 decades cover the total range of the Digitizer. The highest decade counts tenths of a second and goes up to 3 only, since the maximum range is slightly over 340 msec.

Train pulses are transmitted by a 50-ohm cable from the logic module and, passing logic translator T, they advance the scaler through OR_1. The other inputs to OR_1 are used if additional counts have to be sent to the scaler at the end of the time interval conversion (i.e. if D_{12} and/or C_{13} are logic "1" signal).

The "End of Conversion" signal is received from the logic module when the digitization is over. At the same time, the result of the interpolation is available in a 13-bit binary word (A_1-A_{12}, D_{12} and C_{13}). A_{11}, D_{12} and C_{13} are worth 10 nsec., 20 nsec and 40 nsec, respectively. The "End of Conversion" signal propagates through a series of delay circuits, T_{d1} through T_{d7}. The gates G_1, G_2, G_3 and G_4 will be enabled in sequence for a short period of time. All is strobed into the first binary B_a of the 4th decade, and D_{12} into the second binary, B_b by passing through OR_1. The next two strobe pulses generated by G_3 and G_4 are combined into a double strobe pulse in OR_1 and applied to G_4 to strobe "carry" C_{13}. Since C_{13} is worth 40 nsec., double strobing will advance the B_b binary by two counts.

The first 10 bits (A_1 thru A_{11}) make 3 complete binary coded decades (D_1, D_2 and D_3), plus the first bit of the fourth (A_{31}) at the output of a fast binary-to-BCD converter. Since the highest possible number there is 1,023, the content of the 4th decade is either zero or one.

At the time the "End of Conversion" signal has propagated through delay circuit T_{d8}, all the counting is done and the number ready for the display.

Two 6-decade numeric displays are used. Because of the limited width of the module, the numbers are displayed in two rows. The upper 6 digits display the decades D_6 to D_{11}. Two lower left hand side digits display the decades D_4 and D_5, and the remaining 4 digits display the decades D_1, D_2 and D_3 and the status of A_{31} as was explained earlier.

Each digit of the display is turned on in sequence once the level "1" at the output of T_{d8} has enabled the advancing of the shift register by a free-running 10 kHz clock. The shift register in connection with OR_3 produces repetitive sequences of 7 pulses each. The first 6 pulses will enable the digits of the decimal display one at a time and strobe the proper decade into the 7-segment decoders. The 7th pulse in the sequence resets the latch L_1, which is used for blanking out the unnecessary zeroes on the upper 6-digit display.

In normal operation of the Time Digitizer, the decimal display is practically invisible, because the data transfer into the buffer register and then into the computer takes place very rapidly. In order to see the display, the Digitizer should be operated manually, or its operation may be stopped for a while by holding the clear push button at the buffer register down.

4. Digitizer Alignment Considerations

The Time Digitizer normally does not require any adjustments. However, due to aging or after transportation, the two interpolators in the Digitizer may need realignment in order to ensure the optimum resolution.

It is assumed that the Time Digitizer is operating on line with some kind of a data processor; i.e., computer or multichannel memory. In the example shown in Fig. 18, the Time Digitizer is tied to the Tracor-Northern NS-636 Series Memory Unit, which can process and display 12-bit words in the same way as does a multichannel pulse height analyzer.

A fast rise time pulse generator provides imputs to the Time Digitizer. One output of the 50-ohm splitter is tied directly into the Start Input and the other output via a 50-ohm delay line into the Stop Input. The levels at the inputs should be about 800 mV into 50-ohm terminations. The rate of the start-stop pulse

pairs should be selected around 3000/second to avoid the beat effect with the internal clock frequency of 50 MHz. If a good quality cable is used for delay, very stable start-stop intervals are generated.

Each event processed by the Digitizer will be stored in the Memory Unit. All events having the same address will be added into the same "channel" of the memory. When the desired total number of events has been processed, the content of the memory can be displayed in histograms such as those in Figs. 20 and 21. Each horizontal dot represents a "channel" or a time interval increment of 9.86 psec. Both pictures show only the last 70 channels of the measured time range of 150 nsec because of digital offset. Therefore, only a high resolution "window" at the end of the measured interval is shown regardless of its magnitude. In real time, 70 channels of the window cover 0.68 nsec. The spectra in Fig. 20 show two discrete time intervals generated by changing the length of the delay trombone in series with the stop input.

By analyzing the distribution of the two peaks in Fig. 20, their separation can be resolved to the fraction of one channel. The left peak is centered around channel No. 14,858, and the second one is in the middle between channels 14,888 and 14,889. Therefore, the time difference between the two peaks is 30.5 channels.

Distributions approaching the theoretical limit are obtained when an internal clock is used for the generation of the start and stop inputs of the Digitizer (Fig. 19). The time intervals thus generated by the Calibrator are synchronized to the clock resulting in extremely narrow distributions. The two peaks shown in Fig. 21 for two sets of time intervals have been generated by adjusting the delay trombone. The first peak is placed almost exactly in the middle between channels No. 14,912 and 14,913, and the second one into the channel No. 14,926.

The result shows very close agreement with the theoretical triangular distribution of the Digitizer. The adjacent channels

in the second peak contain only 2% of the total events. Ideally, they should count zero events when the measured interval falls right in the middle of a channel. The 2% of spread is due to the composite noise of the two interpolators as well as the phase noise of the internal clock oscillator. Since the channel width is 9.76 psec, the total time jitter is 2% of that; i.e., less than 0.2 psec.

By calculating the difference of the contents of the two channels in the left peak, it can be concluded that the exact position of this peak is 0.2 psec to the left of the exact middle of the channel. This method is useful for the measurements of very small time delay increments, phase shifts, harmonic oscillator phase purity, etc.

Alignment Procedure

Time intervals generated according to Fig. 18 are not phase correlated to the internal clock frequency of the Digitizer. Each event is defined by

$$N = N_{st} + 2^{n-1}N_{mn} - N_{sp} \qquad (7)$$

where N_{st}, N_{mn} and N_{sp} are the readings of the Start Scaler, Main Scaler and the Stop Scaler, respectively. As long as intervals of the same width are being measured, N will be the same, although N_{st}, N_{mn} and N_{sp} are different for each event. When properly aligned, each interpolator generates a pulse burst for each event that can vary by exactly 2048 counts. Accordingly, N_{st} max $-N_{st}$ min = 2048, and N_{sp} max $-N_{sp}$ min = 2048.

If the Digitizer is run as shown in Fig. 18 for a fixed delay one of the distributions as in Fig. 20 is obtained. If Align Stop position is selected by the rear panel switch of the decimal display module, the counting of the start scaler is inhibited, and therefore $N_{st} = 0$ at all times. N will vary in the same way N_{sp} varies, and the resulting distribution is shown in Fig. 22b. Out of 4096 channels displayed, only 2048 should count, and the

distribution should be flat since all counting channels are equally probable. In the picture shown, the average of the counts per channel is low; so the statistics is relatively poor. The distribution is flat for proper alignment (Fig. 22b). By turning clockwise the stop align pot on the rear panel of the stop interpolator, the distribution changes to the one shown in Fig. 22a. This is because some channels become statistically more probable and they count more. Similarly, some channels count less when the pot is turned counterclockwise (Fig. 22c).

The start interpolator can be aligned in a similar way by selecting the align start position of the alignment switch. It is important that the alignment switch is returned to the neutral position after the alignment procedure is completed.

The best resolution is obtained when the interpolators are properly aligned. However, misalignment of either one or both interpolators merely results in broadening of the distributions in Fig. 20 because of the averaging inherent to the operation principle of the Time Digitizer. The same effect will be observed if the external clock used to operate the Time Digitizer has significant random phase jitter.

To emphasize the need for a pure, phase-modulation free clock when external frequency reference is used, a few test results are shown with several frequency sources that were available at the time in the paragraphs 5b, 5c, 5d and 5e of the Section 5.

5. Digitizer Test Results

5a. Temperature Test

The test was performed in such a way as to approximate the real operating conditions of the Digitizer. The Digitizer was set on a bench with two inches of clearance underneath in a

closed room. The initial temperature in the room was 12°C. The temperature was gradually increased to 36°C during the period of 10 hours. Only natural circulation of air was permitted. The Digitizer was manually operated as described in Section 6 under Manual Testing. The resulting drift is only due to the difference in tracking of the two interpolators and independent of the temperature drift of the internal clock reference. The latter has been measured by the manufacturer of the clock crystal oscillator, and the test results are given in the Specification's Section of this text.

For a time interval T measured by the Digitizer, the expected error due to temperature change is

$$\left|\Delta T\right| = \left|\Delta T_{st} - \Delta T_{sp}\right| + \left|\frac{\Delta f_o}{f_o} \cdot T\right| \qquad (8)$$

where ΔT_{st} and ΔT_{sp} are respective drifts of the start and the stop interpolators and $\Delta f_o/f_o$ is the clock frequency change for a given ambient temperature change. In this measurement, the second part of Eq. 8 is eliminated because both the Calibrator and the Digitizer use the same clock, and the frequency thus becomes an invariant.

The result of the measurement is shown in Fig. 23. The difference in tracking is virtually a linear function of the temperature change. The rate of change is

$$(\Delta T_{st} - \Delta T_{sp})/\Delta t = +4.5 \text{ psec/°C} \qquad (9)$$

Short term drifts at constant ambient temperature are hard to observe because they are a fraction of a channel. The Digitizer was kept running under laboratory temperature conditions for hours without an apparent drift.

No attempt was made so far to try thermal compensation that would bring the slope of the curve in Fig. 23 close to zero. Taking also into account the excellent reproducibility of the measurements, it is believed that such compensation would result

in a tenfold increase of the current thermal stability.

5b. Oscilloquartz S.A. Type 5-5400 Oscillator Test

The oscillator is a very high stability 5 MHz quartz crystal oscillator to be used by NASA for the external clock reference. It has short term stability of better than 10^{-12}/sec and excellent phase noise characteristics. The test setup of Fig. 19 has been used, except for the clock under test being connected to the reference clock input of the calibrator instead. The calibrator is a digital frequency divider. The range was selected so that the calibrator output rate was reduced to below 1 kHz. The Digitizer measures the intervals between the consecutive calibrator output pulses. The results are shown in Fig. 24. The peaks correspond to the three discrete delays preset by the trombone in series with the stop input. The picture shows the expanded end portion of the measured interval of more than 3 msec. The first peak falls into the channel 327, 697, 874, and the next two are a fraction of a nanosecond apart. Since in this experiment the external source is checked against the internal clock, the result is composite distribution of both clocks over periods of 3 msec.

5c. NASA 50 MHz Frequency Multiplier Test

A 10X frequency multiplier is needed to drive the Time Digitizer by the 5 MHz frequency standard. The operation of the Time Digitizer is based on the expansion of the 50 MHz clock period and, therefore, even a trace of subharmonics can cause broadening of measured distributions or, in some cases, result in separate peaks. Fig. 25 shows the frequency spectrum of the 10X multiplier provided by NASA. The most dominant is the 40 MHz subharmonic. The other two subharmonics of 30 MHz and 45 MHz are below 60 db, and their effect is small.

The output of the multiplier was fed into the reference clock input of the Calibrator, and the measurement done according to the Fig. 19. The result shows double peaks (Fig. 26a), indi-

cating that the synthesized 50 MHz source has two dominant periods different from each other by about 30 psec. A 50 MHz narrow band filter was used next in order to reduce the harmonics to below the 60 dB level. The result shows only one peak (Fig. 26b) having FWHM reduced by a half of that in Fig. 26a.

5d. Model 1062 General Radio Synthesizer Test

The synthesizer was set to 30 MHz and tested in the same manner as the crystal clock in the test 5a. The result is shown in Fig. 27. A much broader distribution (7 channels FWHM) is due to comparatively large inherent phase noise of this kind of instrument.

5e. 30 MHz Frequency Tripler Test

An existing 30 MHz frequency tripler was tested in the same manner. The 10 MHz reference source was the synthesizer used also in the test 5c. The frequency spectrum shows two subharmonics of 10 MHz and 20 MHz (Fig. 28). The time interval of 540 microseconds shows a distribution spread out into three discrete peaks (Fig. 29).

6. Operation Instructions

The Time Digitizer should be checked for mechanical damage after any shipment. Make sure that all modules are in proper place and the thumbscrews fastened. Check that the rear panel cables are properly interconnected and their connectors tightened. Should any cable become disconnected, make sure that it be returned to the right place.

All cables are of the same length except for MNCK where the coiled cable should be used. The Time Digitizer may malfunction if a short cable is used by mistake.

Check that the 25-pin rear panel connectors on the Logic Unit and the Decimal Display have the connecting cable in place and

properly tightened.

Disconnect all input and output connectors on the front panel of the Time Digitizer, including the cable to the Crate Controller. Plug the Time Digitizer to 117V AC, 60 Hz main voltage. Turn the power on and measure voltages at the test points on the front panel. At the time of the last check, the readings were:

+ 24V.....,+ 23.87V
+ 6V.....+ 5.973V
- 6V.....- 5.996V
- 24V.....- 24.30V

For details read the PCS/2 CAMAC Power Supply Instruction Manual provided by the manufacturer of the Minicrate.

After the power has been turned on, any binary or decimal number can be displayed. Each should be resettable by depressing Scaler Register Clear or Buffer Register Clear push button, respectively.

Manual Testing of the Time Digitizer

Set the front panel controls and make the connections as follows:

Calibrator Range: Position 9
Clock Switch: External
Start Interpolator Switch: Anticoincidence
Stop Interpolator Switch: Anticoincidence
Logic Unit Range Switch: Position 10
Logic Unit Stop Enable Switch: Position 2

In addition, tie a 1-foot long cable between Clock Output and Reference Clock Input of the calibrator and two identical 4-foot long cables between the start output of the calibrator and the start input of the start interpolator and between the stop output of the calibrator and the stop input of the stop interpolator. Depress Buffer Register Clear push button several times.

Two successive events generated by the calibrator should be shown on the displays. The difference between them should not be greater than 0.01 on the decimal display (corresponding to the least significant bit on the decimal display). The upper 6 digits of the display should read 167 772, and the lower digits should read 1910.00. Since the two cables can not be expected to be identical, a small difference in their respective propagation delays will make the last 4 digits greater or smaller than 10.00.

Throw the switch on the start interpolator into the coincidence position. Depress the Buffer Register Clear push button once. The buffer will be cleared and the number shown on the decimal display transferred anddisplayed by LED's in binary fashion. Check that the transferred number is the same. The decimal display will go blank since the start input is disabled. By deparessing the Clear push button twice, the buffer memory is cleared and both displays remain blank.

Put the switch back into Anticoincidence position. Two events will be processed,stored and displayed. Each time the Buffer Register Clear push button is depressed, the buffer is cleared, the event stored in the scaler register is transferred into the buffer, and a new event accepted and stored in the scaler register again.

Turn off the power, and connect the Crate Controller to the computer. Turn the power on again and run the test program to ensure that the Time Digitizer and the computer communicate in the right way.

7. Summary of Digitizer Specification

Internal clock frequency (f_o)	50.000 000 MHz
Internal clock frequency stability (-10°C to +60°C)	± 0.0005%
Reference clock frequency	50.000 000 MHz
Reference clock input (50 ohm terminated)	± 1V (peak)
Clock output (50 ohm terminated)	- 0.7V min
Calibrator ranges (1 to 10):	$2^2, 2^5, 2^8, 2^{11}, 2^{14}, 2^{17}, 2^{20}, 2^{23}, 2^{26}$, OFF.
Start input (50 ohm terminated)	- 0.7V min
Stop input (50 ohm terminated)	- 0.7V min
Gate input (50 ohm terminated)	- 0.7V min
Busy output (50 ohm terminated NIM complement)	- 0.7V min
Decimal display (displays scaler register)	11 + 1 digits
Binary display (displays buffer register)	35 bits
Incremental Resolution (binary)	1×2^{-36}
Incremental Resolution (decimal)	1×10^{-11}
Calibration (least significant bit)	10/1.024 = 9.76 psec./channel
Calibration (T = time interval measured, f_o = exact clock frequency in MHz, N = digital readout)	$T = \frac{1}{2f_o} \cdot \frac{N}{1.024}$
Time interval ranges (Pos. 1 to 10):	0.6,1.3,2.6,5.3,10.0, 21,42,83,170,340(msec)
Stop enable ranges (Pos. 1 to 10):	Enabled 0.3,0.6,1.3,2.6, 5.2,10,20,41,83(μsec.)
Thermal drift	4.5 ps/°C
Deadtime (T = measured interval)	$T + 60 \cdot 10^{-6}$ [sec.]max.
Power Input	117V, 0.8A
Dimensions	L = 19", W = 17", H = 8 3/4"
Weight	50 pounds

CAMAC functions

N . [F(0)+F(2)].A(0)	Read out B1 to B12
N . [F(0)+F(2)].A(1)	Read out B13 to B24
N . [F(0)+F(2)].A(2)	Read out B25 to B36
N . F(2) . A(3)	Clear Buffer Register
C . S2	Clear Buffer Register
Z . S2	Clear Digitizer
I	Inhibit Digitzer
L	Data ready for readout
Q,X	Response for valid address
Manual Scaler Register Clear	Front Panel
Manual Buffer Register Clear	Front Panel
Front Panel Lights:	Scaler register ready
	Scaler register overrun
	Buffer register ready
	CAMAC L
	CAMAC N

8. Conclusions

The results of the tests performed sofar on the Time Digitizer have indicated that a new generation of digitizer can be designed with greatly improved resolution. Indeed the resolution may be increased to about 0.1 psec. This will require thermal stability improvements, the use of the same interpolator for both the start and stop inputs for elimination of certain tracking difficulties. Also the conversion deadtime can be reduced by employing tandem interpolation technique.

The present state of art of other components of the optical receiver such as photodectors and pulse positioning discriminators are not adequate yet to justify development of such a digitizer.

However, it can be used now for more accurate ranging at shorter distances where much larger return signals are expected and less sensitive but faster photo detectors can be used.

Another completely new application of this kind of digitizer is fast measurement of phase differences and phase difference structures of various high frequency repetitive waveforms down into femtosecond range. Also, phase noise distributions of high quality harmonic and other frequency sources can be measured.

9. Acknowledgments

This work was performed as a part of the program of the Electronics Research and Development Group of the Lawrence Berkeley Laboratory, University of California, Berkeley, and was supported by the National Aeronautics and Space Administration-Goddard Space Flight Center, Greenbelt, Maryland, under Contract NDPR No. S-55772A, and the Energy Research and Development Administration under Contract No. W-7405 ENG-48.

10. References

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11. Figure Captions

Fig. 1 System block diagram of high precision time interval digitizer.

Fig. 2 General timing diagram of high precision time interval digitizer.

Fig. 3a Front view of high precision time interval digitizer.

Fig. 3b Rear view of high precision time interval digitizer.

Fig. 4 Clock oscillator block diagram.

Fig. 5 Calibrator logic block diagram.

Fig. 6 Calibrator timing diagram.

Fig. 7 Front view of clock oscillator and calibrator module.

Fig. 8 Block diagram of start interpolator and stop interpolator logic.

Fig. 9 Timing diagram of start interpolator and stop interpolator.

Fig. 10 Front view of start interpolator.

Fig. 11 Front view of stop interpolator.

Fig. 12a Block diagram of scaler input logic and control logic in the logic module.

Fig. 12b Block diagram of scaler register in the logic module.

Fig. 12c Block diagram of buffer register binary display and CAMAC logic in the logic module.

Fig. 13 Timing diagram of logic functions in the logic module.

Fig. 14 Front view of logic module.

Fig. 15 Block diagram of decimal display logic.

Fig. 16 Timing diagram of decimal display logic.

Fig. 17 Front view of decimal display module.

Fig. 18 Setup for generation and measurement of very constant pulse intervals.

Fig. 19 Setup for using internal calibrator of the Time Digitizer for extremely small phase difference measurements.

Fig. 20 Measurement of two time intervals generated by a passive delay line and a trombone and using external pulse generator as shown in Fig. 18.

Fig. 21 Measurement of two time intervals generated by a passive delay line and a trombone and using internal calibrator for pulse generator as shown in Fig. 19.

Fig. 22a Stop Align Pot: +1/4 turn.

Fig. 22b Typical distribution of events over 2048 channels of the stop interpolator when properly aligned. The spread is due to low statistics. Figs. 22a and 22c show two cases of slight misalignment.

Fig. 22c Stop Align Pot: -1/4 turn.

Fig. 23 Time interval error of the digitizer due to difference in thermal tracking of the interpolators. The temperature was gradually increased during the period of 10 hours. Frequency change of the reference clock oscillator is negligible because of short intervals measured.

Fig. 24 Phase noise distribution of the Oscilloquartz SA Type B-5400 5 MHz time standard, fed into the reference clock input of the calibrator in the setup as in Fig. 19. Each peak is generated by a small change of the trombone length.

Fig. 25 Frequency Spectrum of the NASA 10X multiplier.

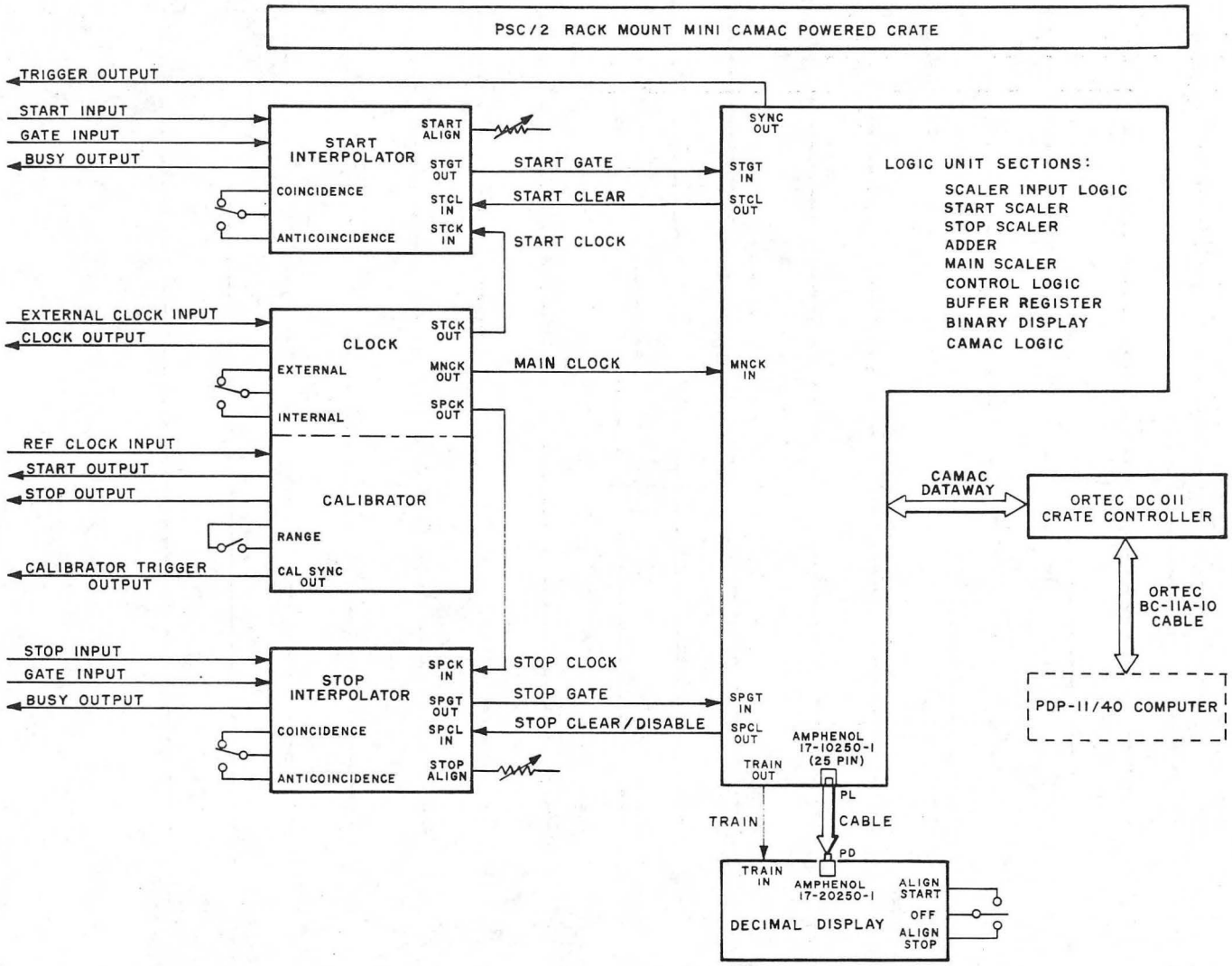
Fig. 26a Phase distribution of the NASA 5-to-50 MHz frequency multiplier. The double peak shows two dominant phases 30 ps apart due to a strong 40 MHz sub-harmonic.

Fig. 26b Phase noise distribution of the NASA 5-to-50 MHz frequency multiplier after filtering.

Fig. 27 Phase noise distribution of the Mod. 1062 General Radio Synthesizer at 30 MHz, fed into the reference clock input of the calibrator in the setup as in Fig. 19.

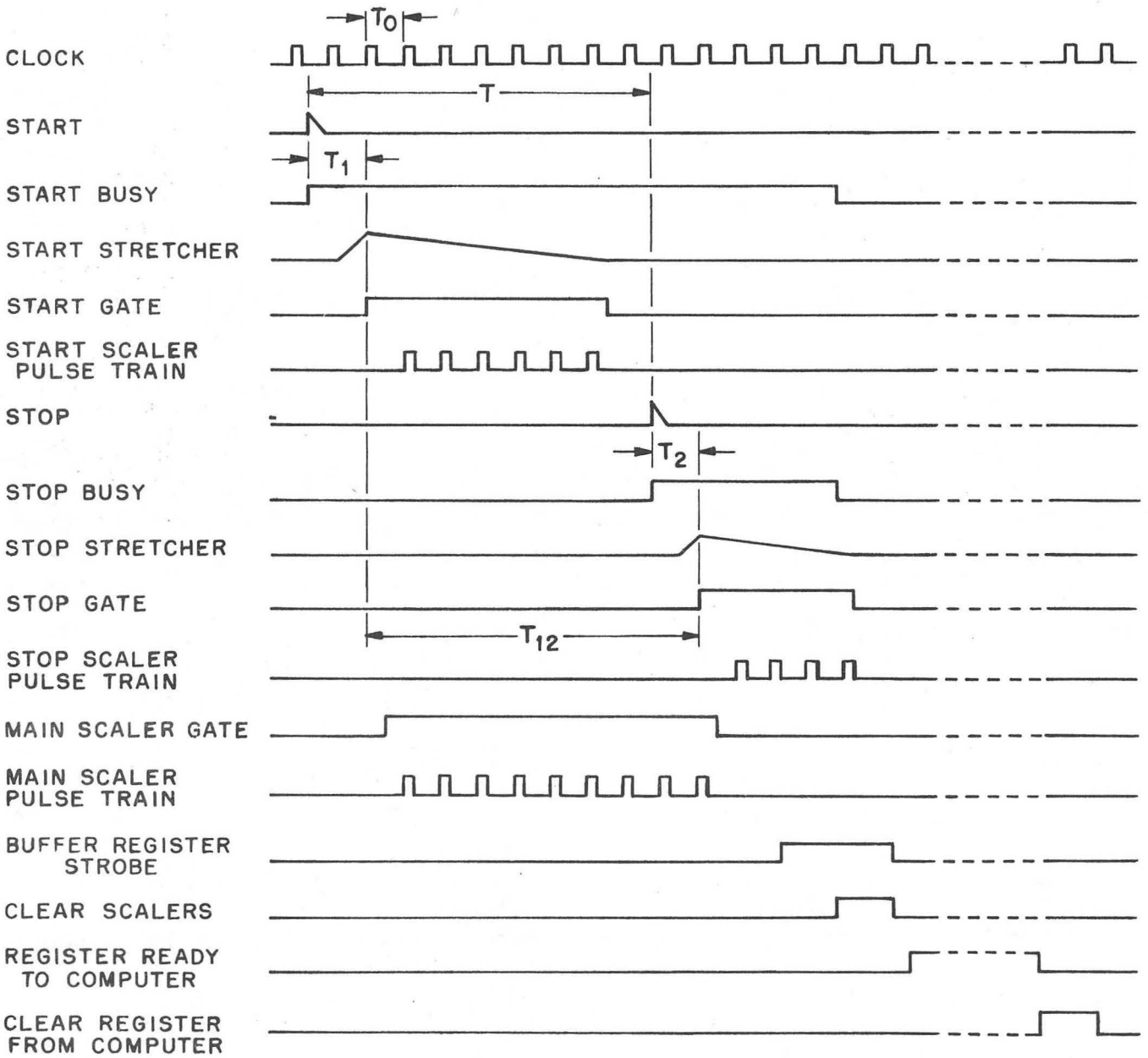
Fig. 28 Frequency Spectrum of 3X multiplier.

Fig. 29 Phase distribution of the 10-to-30 MHz frequency tripler from Fig. 28 shows 3 discrete peaks due to strong 10 MHz and 20 MHz subharmonics.



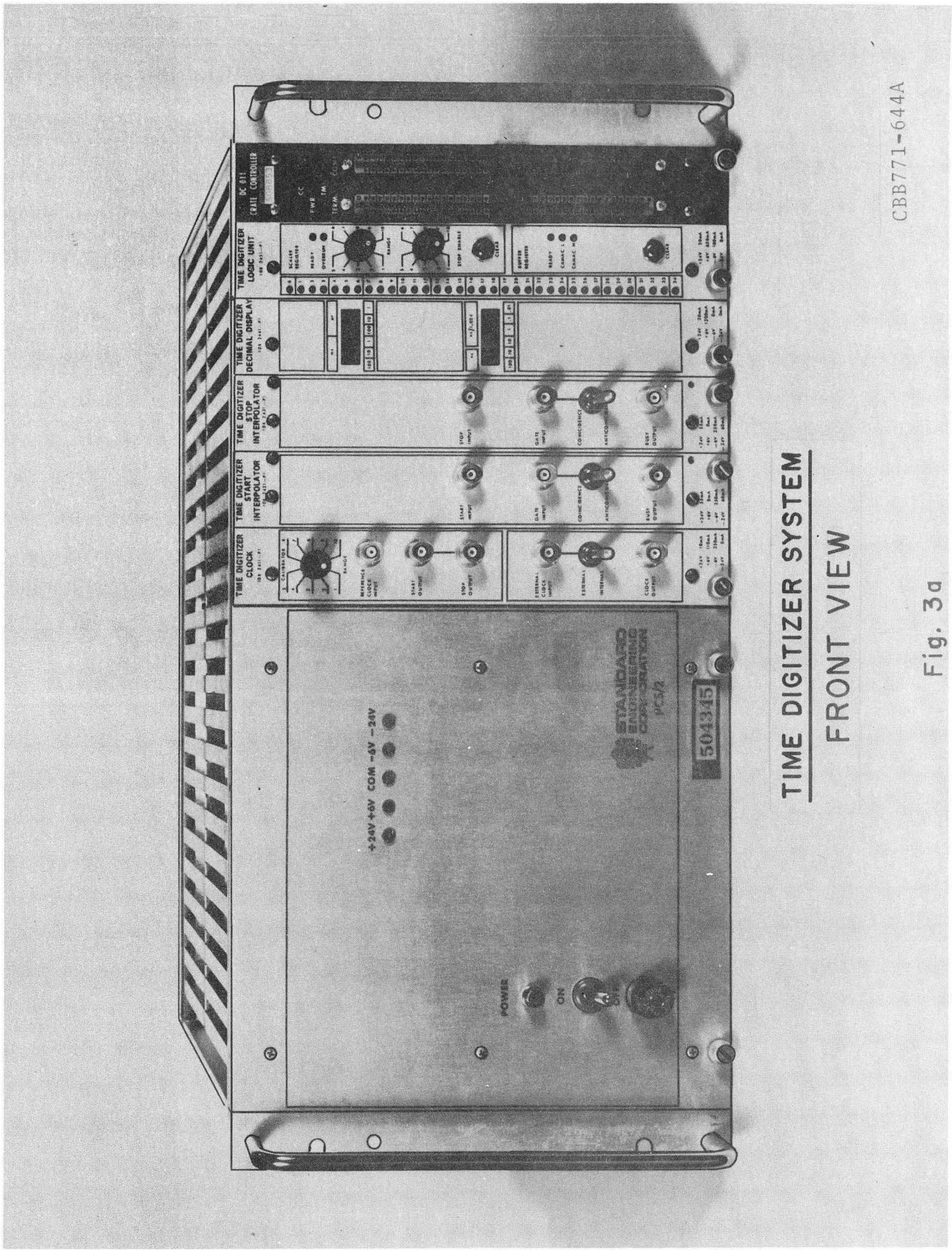
XBL 773-7890

Fig. 1



XBL 773-7891

Fig. 2



TIME DIGITIZER SYSTEM

FRONT VIEW

CBB771-644A

Fig. 3a

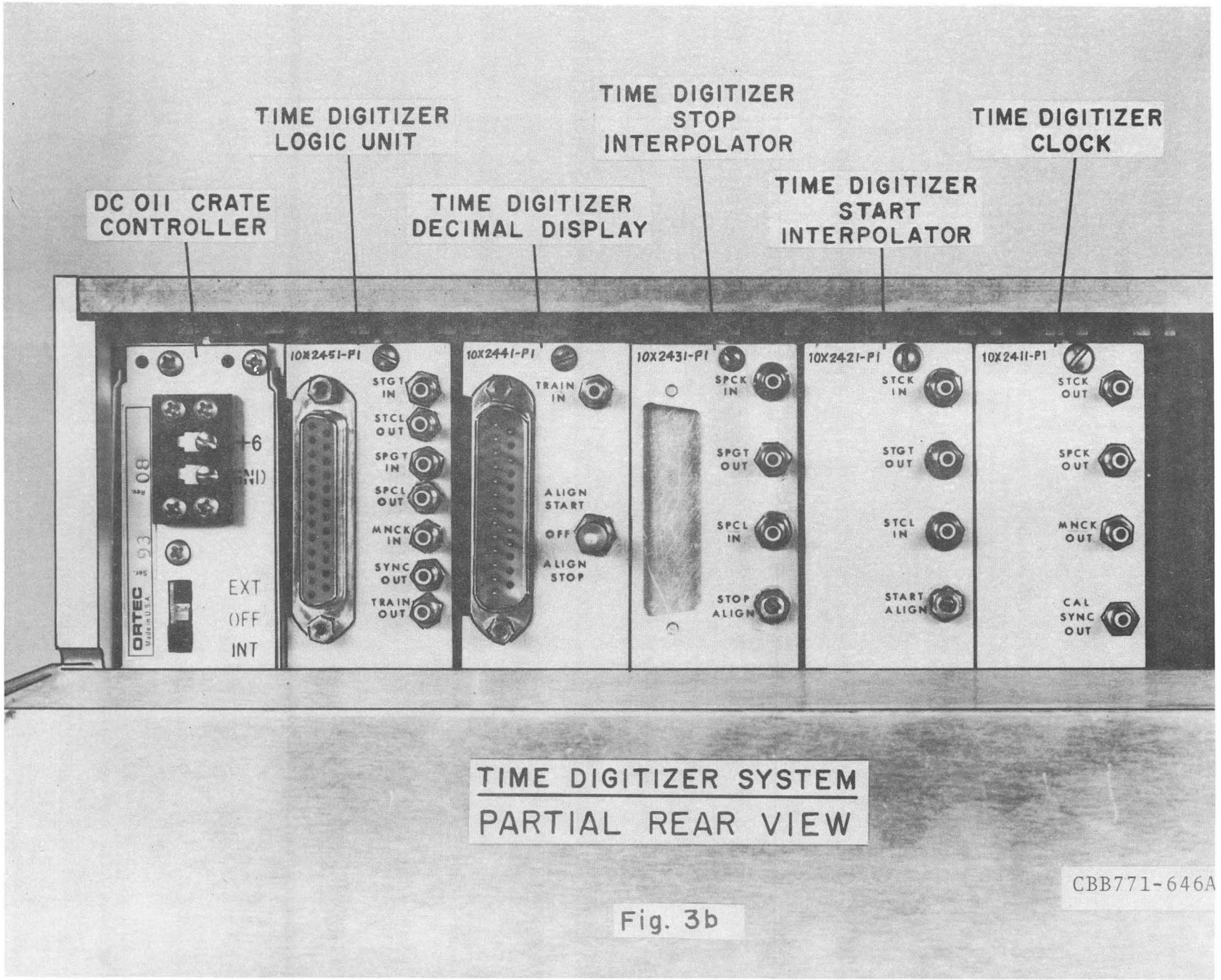
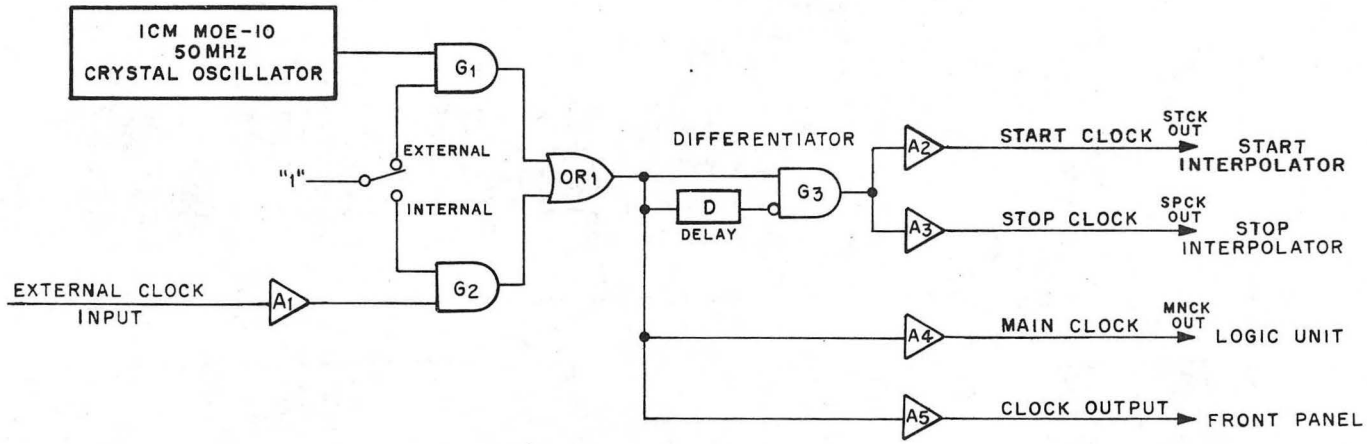
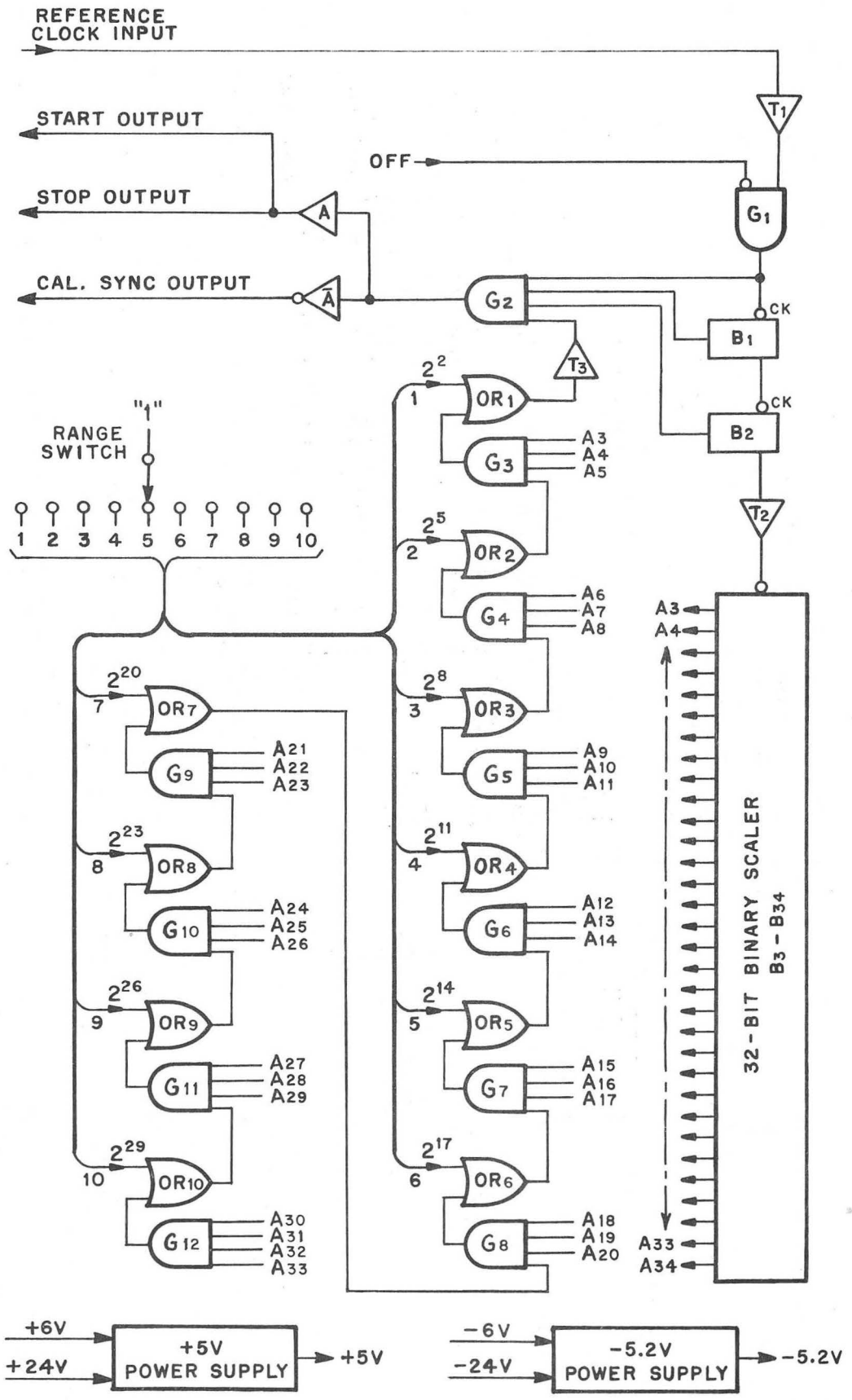

TIME DIGITIZER LOGIC UNIT
TIME DIGITIZER STOP INTERPOLATOR
TIME DIGITIZER CLOCK
DC 011 CRATE CONTROLLER
TIME DIGITIZER DECIMAL DISPLAY
TIME DIGITIZER START INTERPOLATOR
10X2451-P1
STGT IN
STCL OUT
SPGT IN
SPCL OUT
MNCK IN
SYNC OUT
TRAIN OUT
10X2441-P1
TRAIN IN
ALIGN START
OFF
ALIGN STOP
10X2431-P1
SPCK IN
SPGT OUT
SPCL IN
STOP ALIGN
10X2421-P1
STCK IN
STGT OUT
STCL IN
START ALIGN
10X2411-P1
STCK OUT
SPCK OUT
MNCK OUT
CAL SYNC OUT
ORTEC
EXT
OFF
INT
TIME DIGITIZER SYSTEM
PARTIAL REAR VIEW
CBB771-646A

Fig. 3b



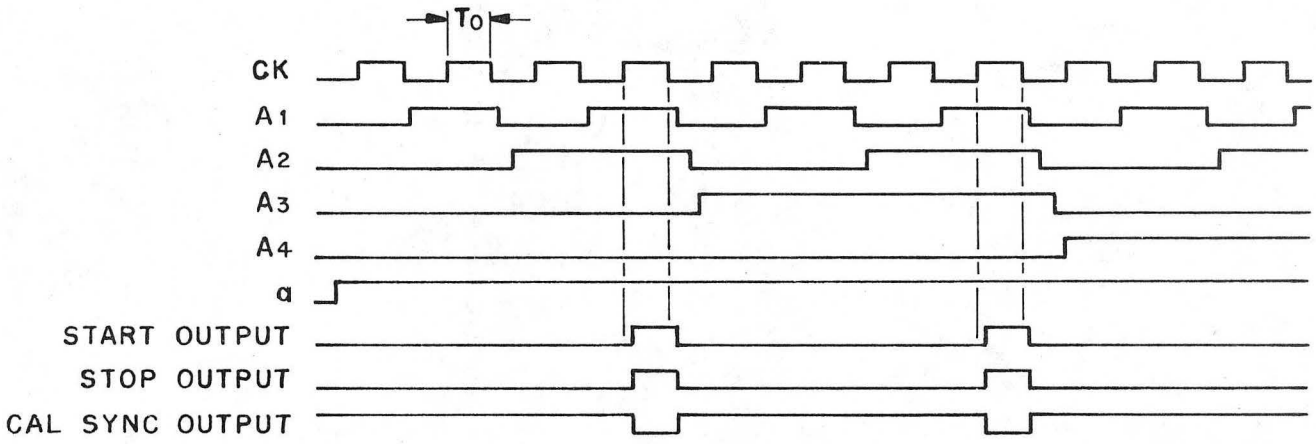
XBL 773-7894

Fig. 4



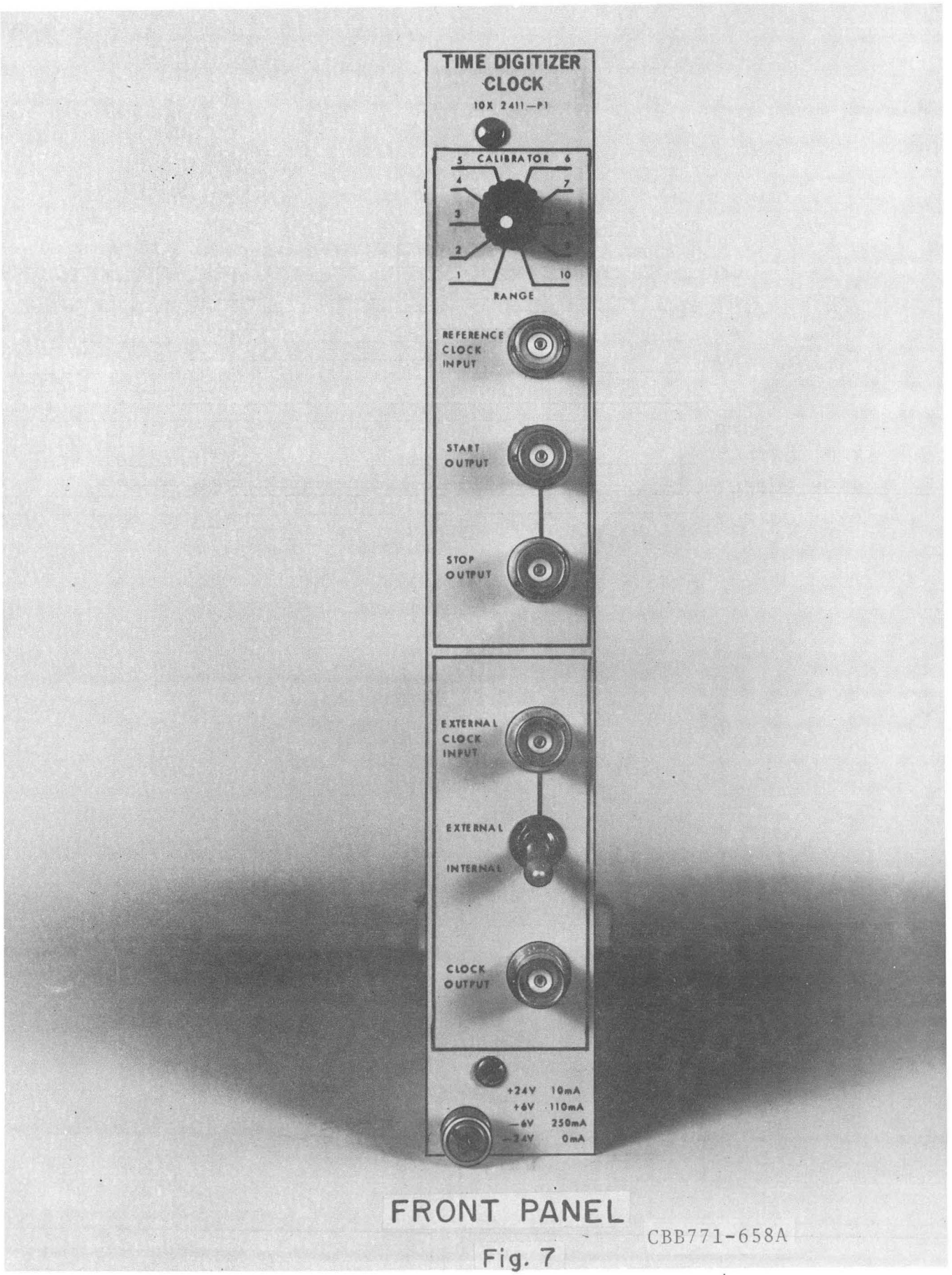
XBL 773-7895

Fig. 5



XBL 773-7896

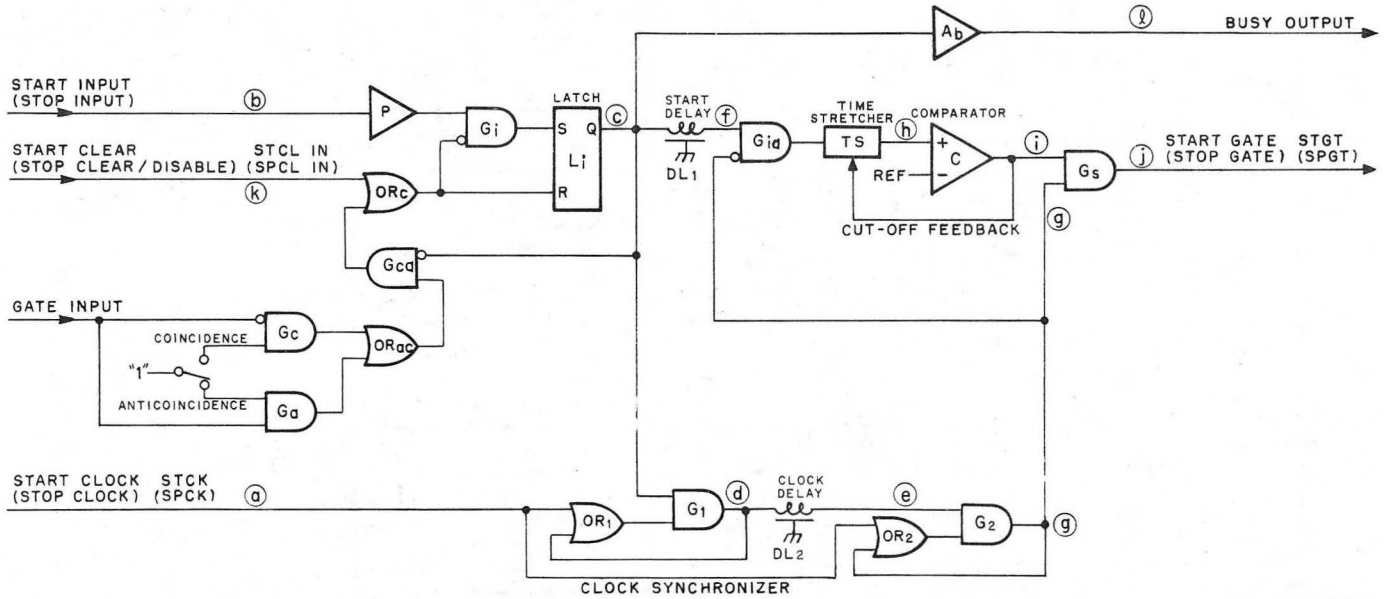
Fig. 6



FRONT PANEL

CBB771-658A

Fig. 7



XBL 773-7898

Fig. 8

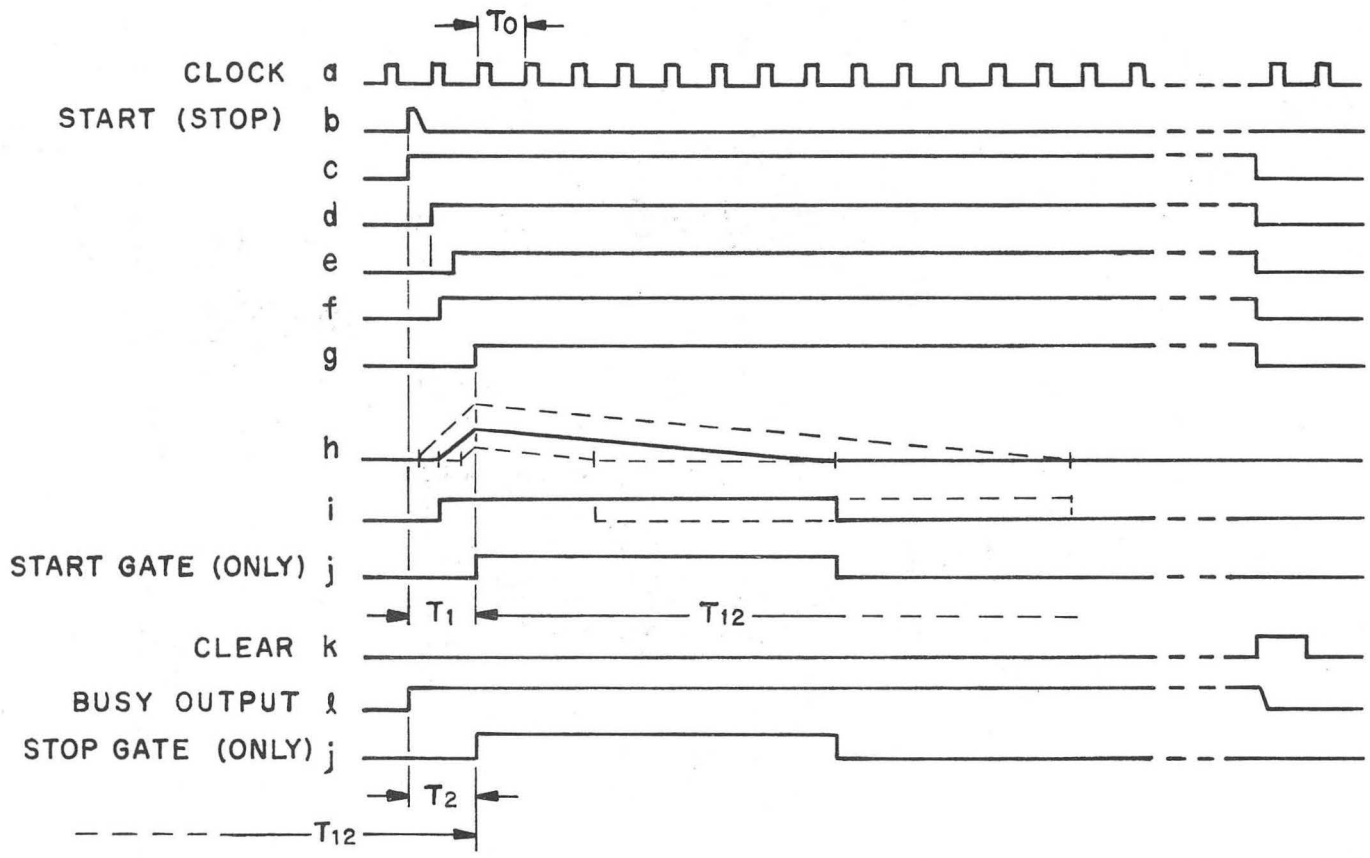
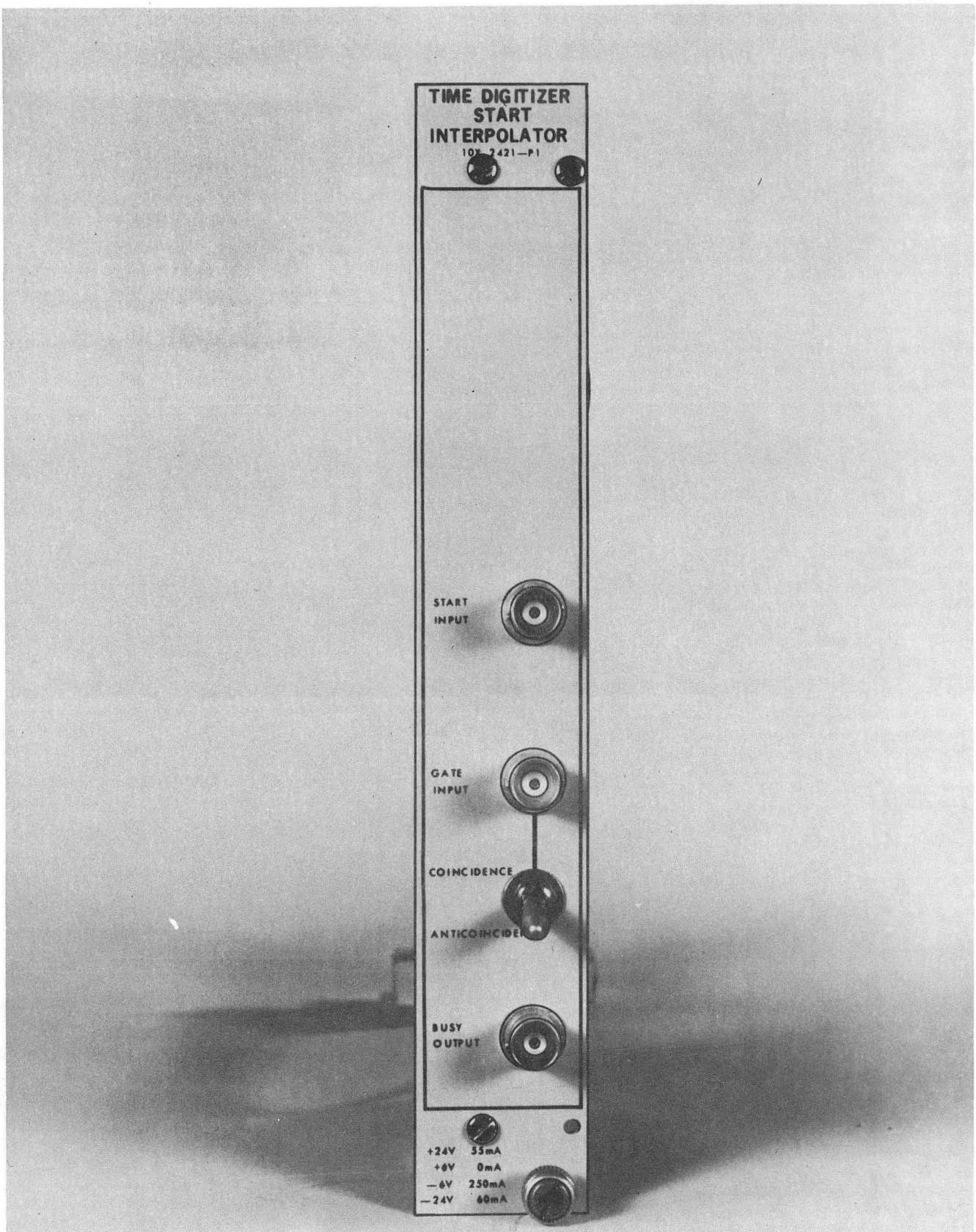

T0
CLOCK a
START (STOP) b
c
d
e
f
g
h
i
START GATE (ONLY) j
T1
T12
CLEAR k
BUSY OUTPUT ℓ
STOP GATE (ONLY) j
T2
T12
XBL 773-7899

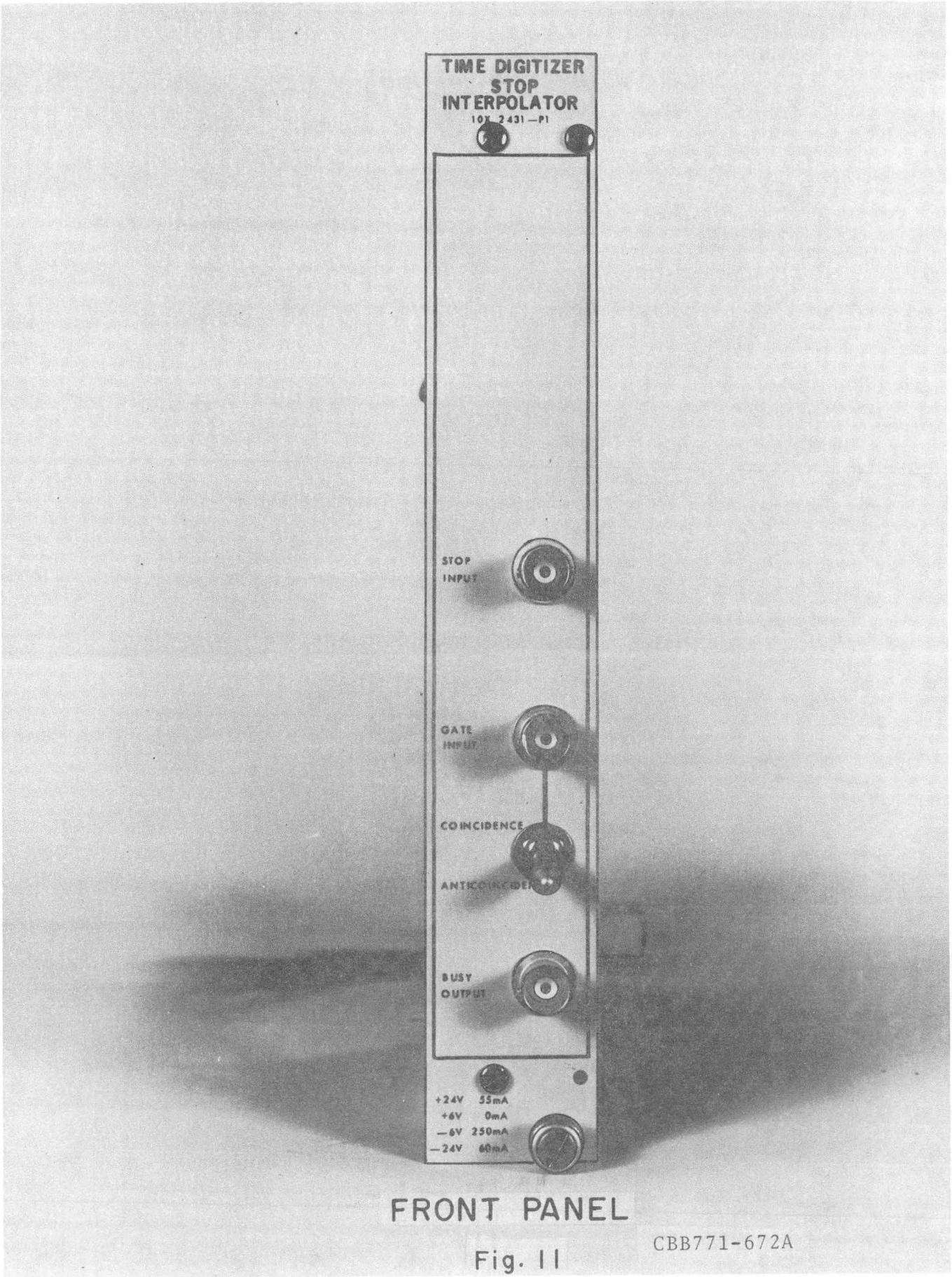
Fig. 9



FRONT PANEL

CBB771-670A

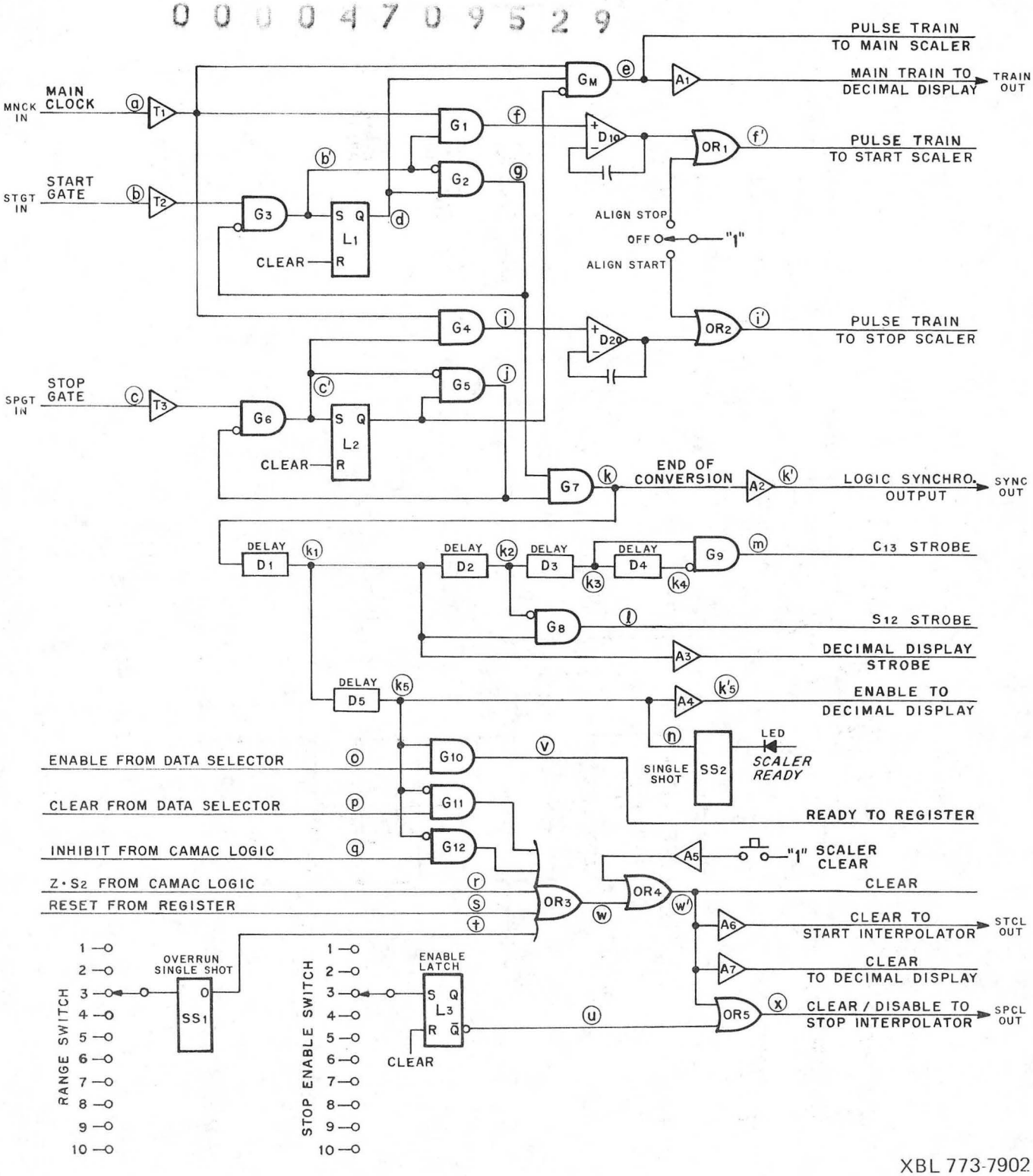
Fig. 10



FRONT PANEL

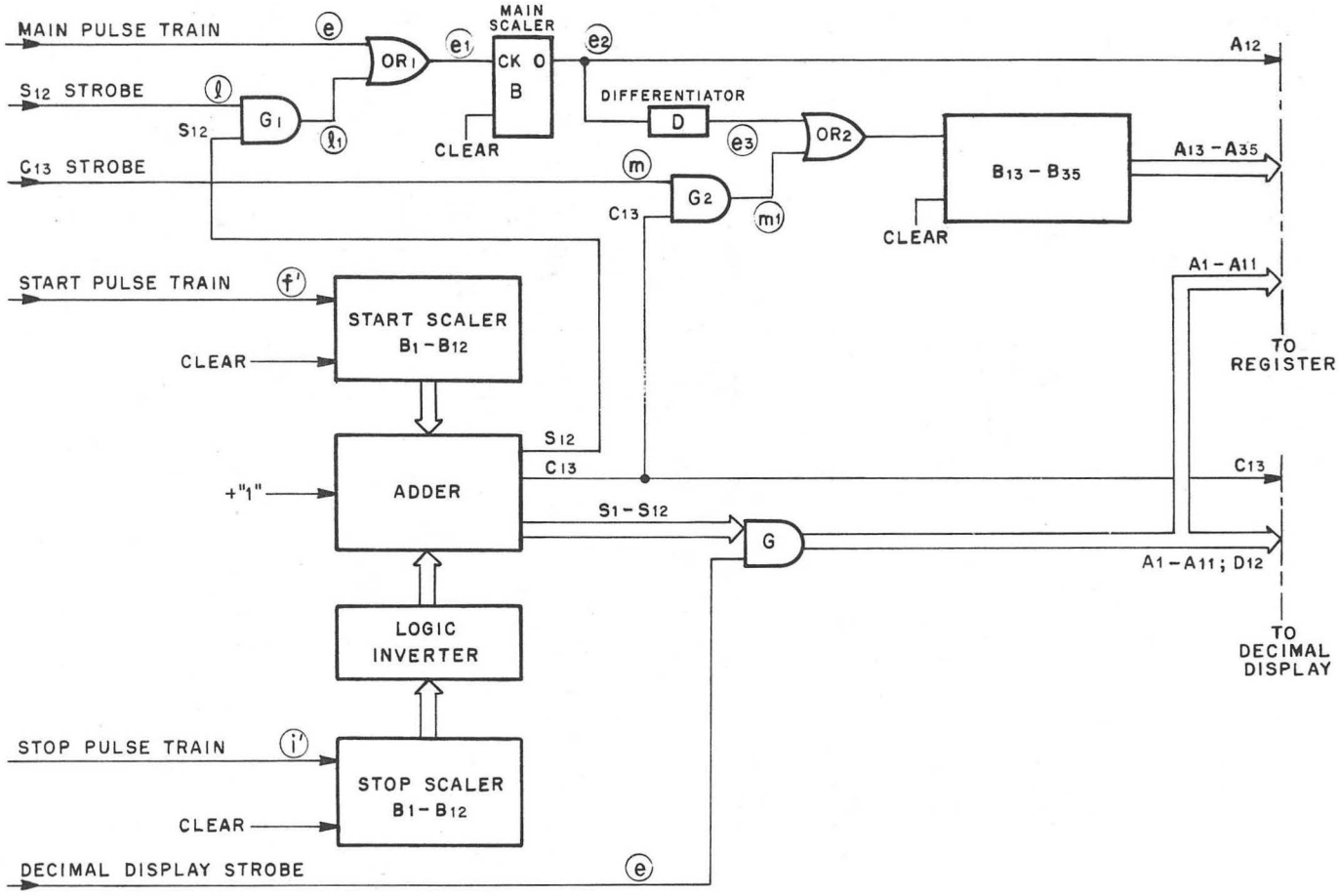
CBB771-672A

Fig. 11



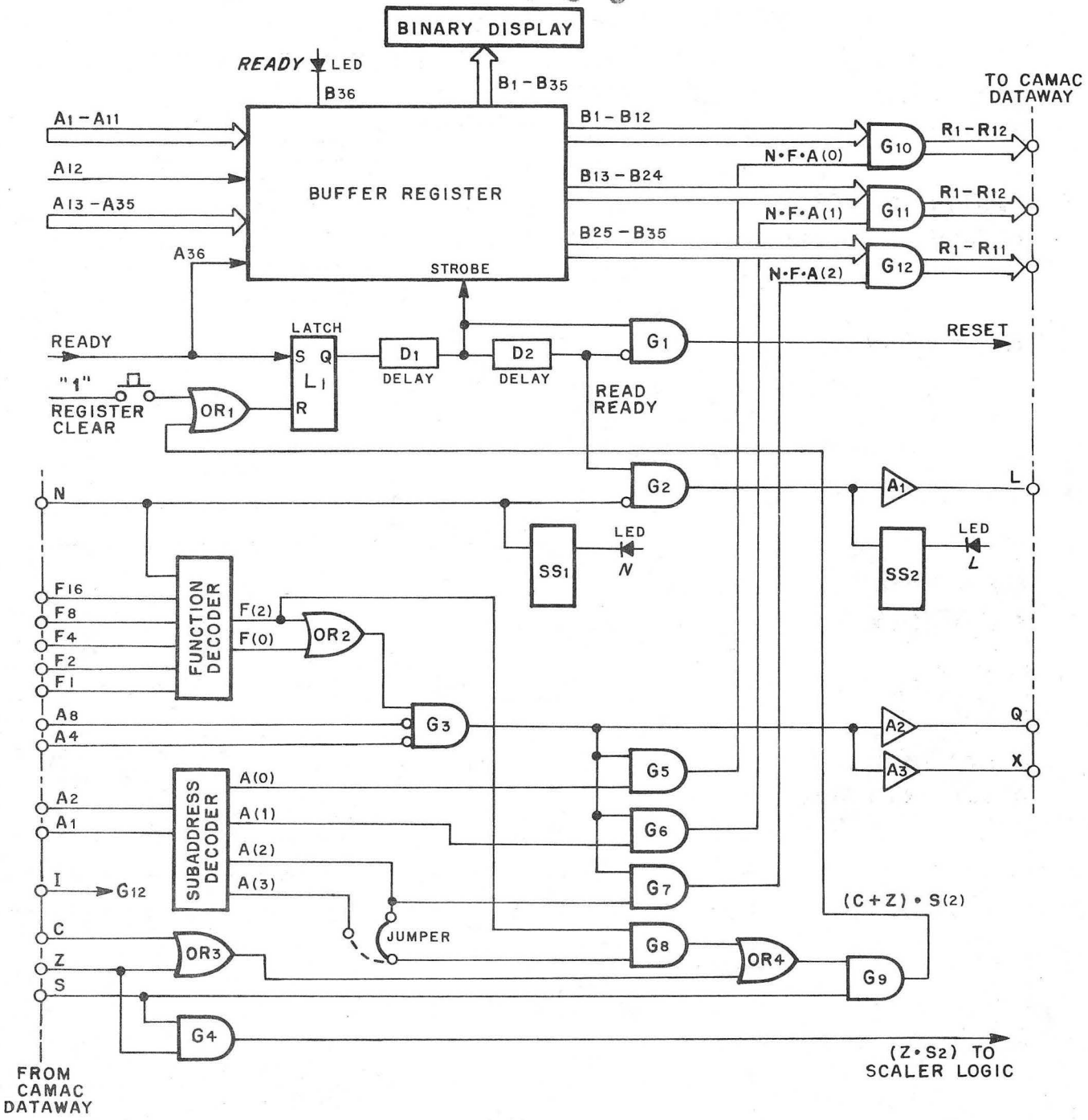
XBL 773-7902

Fig. 12a



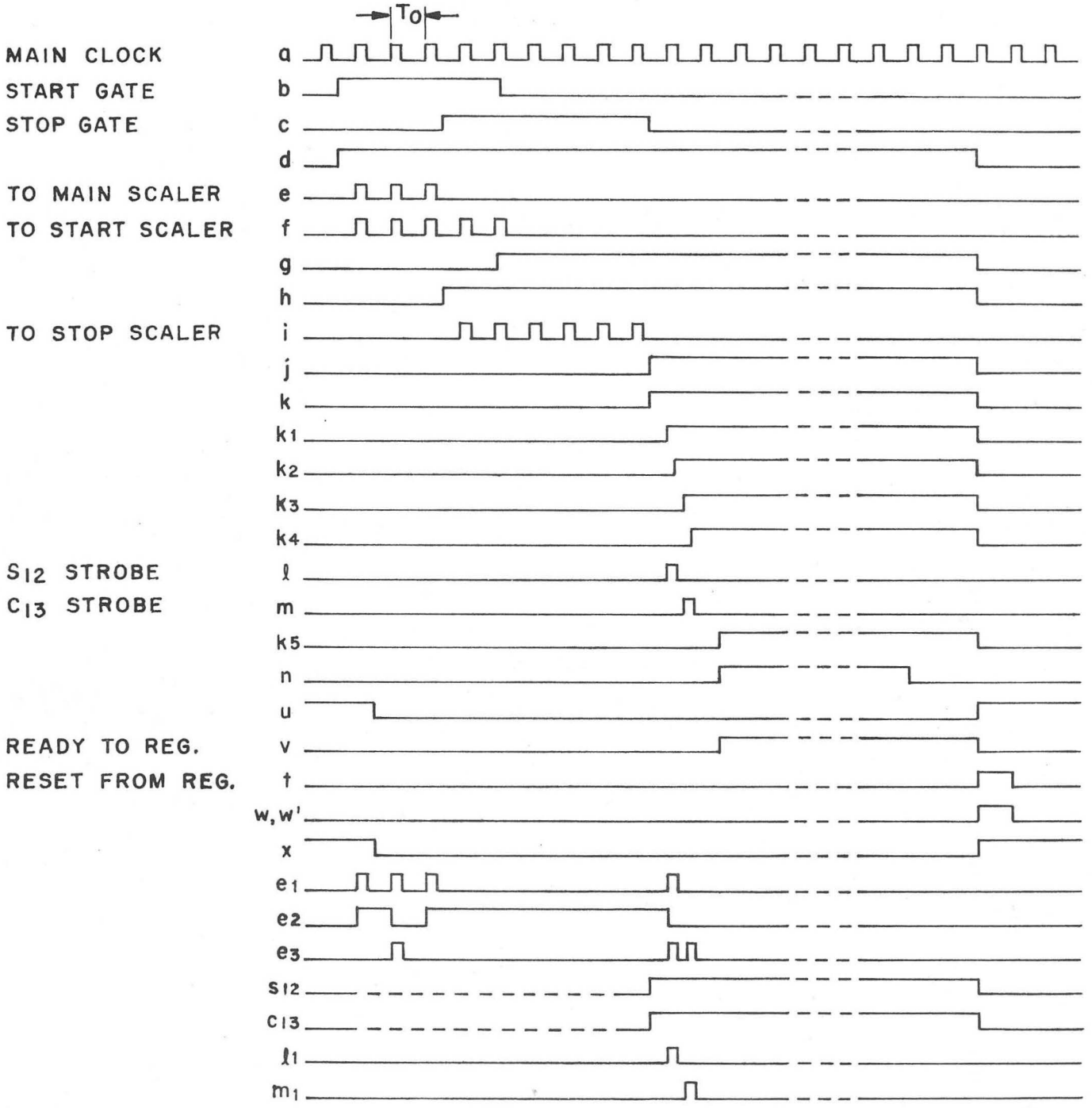
XBL 773-7903

Fig. 12b



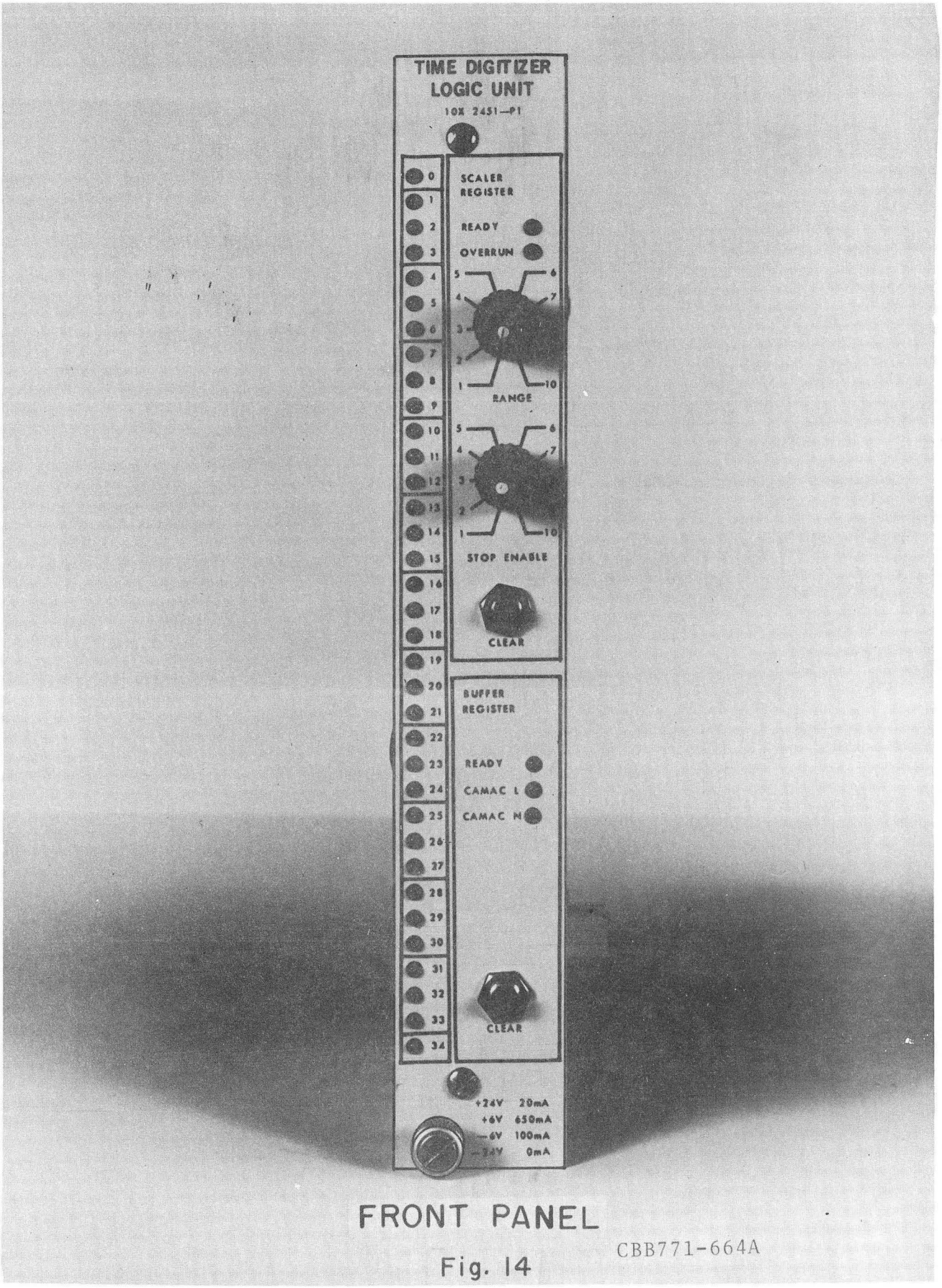
XBL 773-7904

Fig. 12c



XBL 773-7905

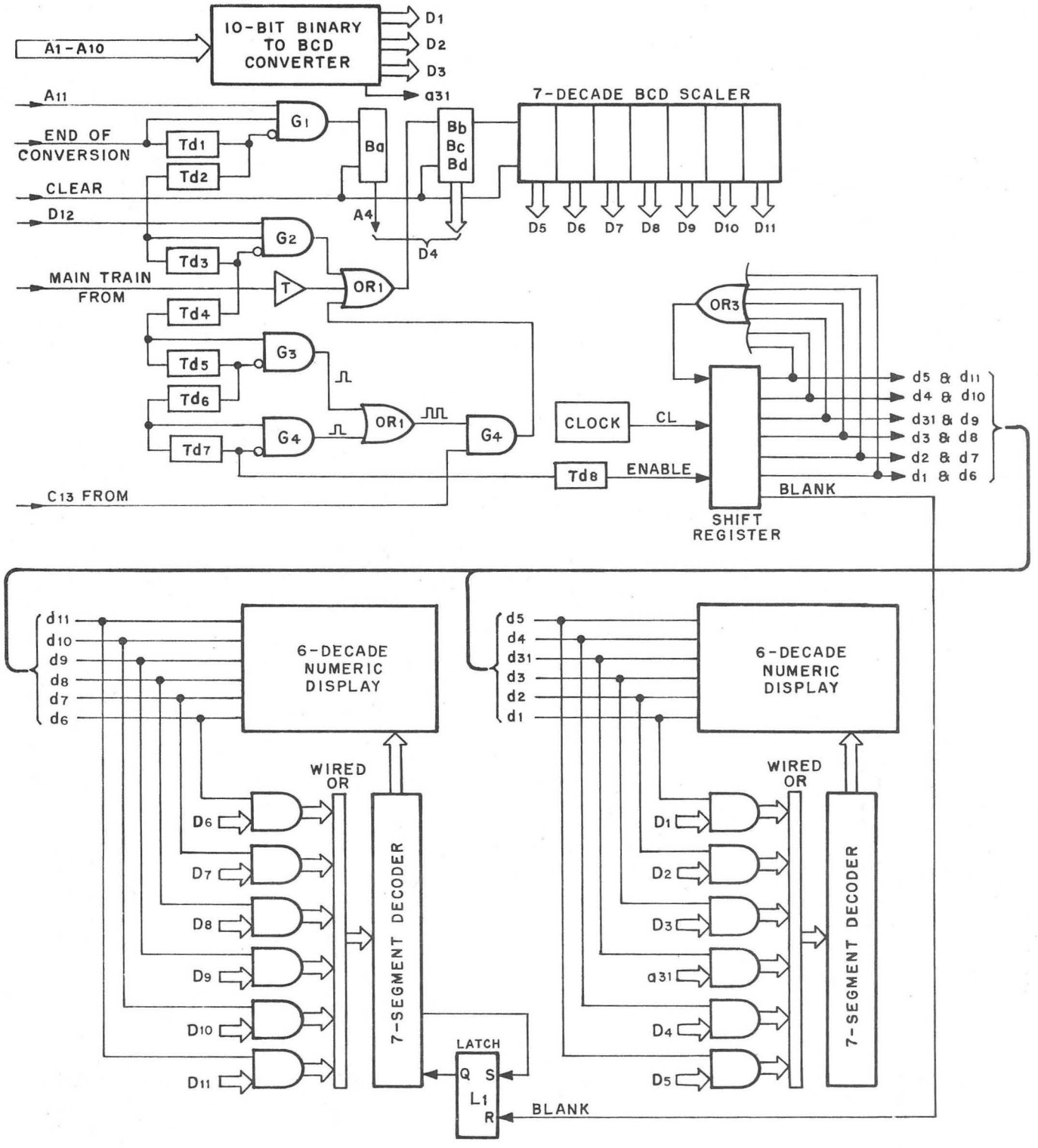
Fig. 13



FRONT PANEL

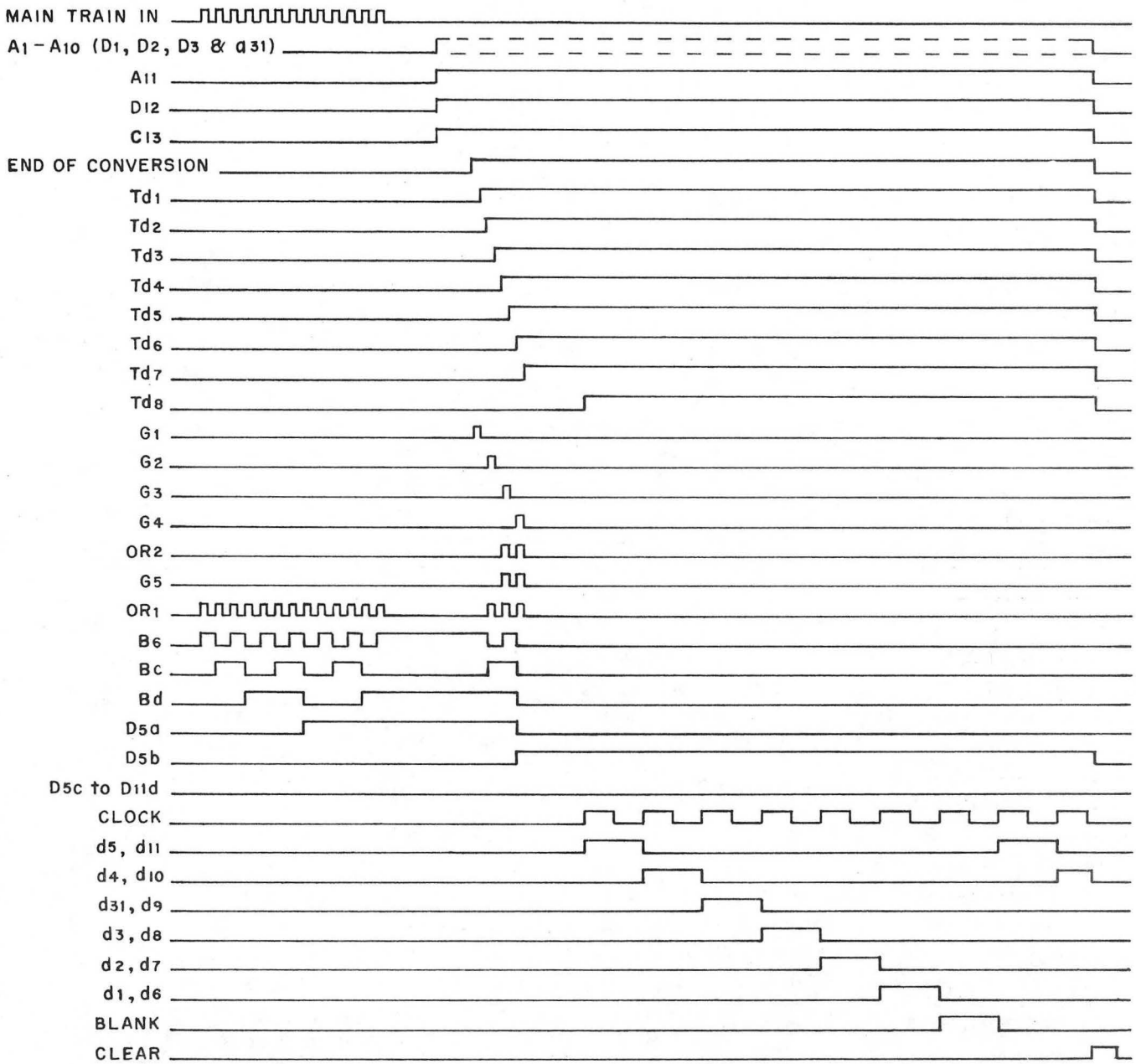
CBB771-664A

Fig. 14



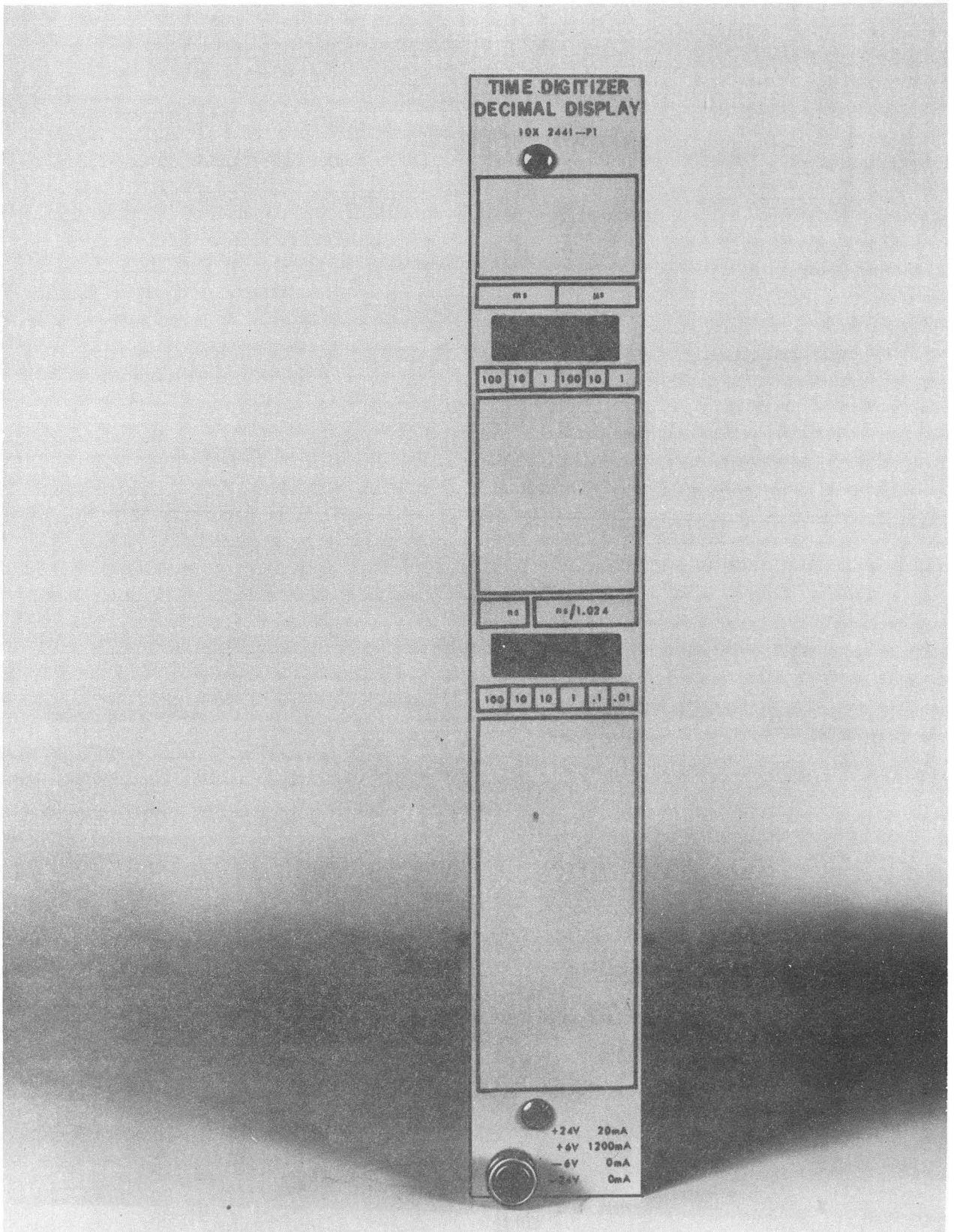
XBL 773-7907

Fig. 15



XBL 773-7908

Fig. 16



FRONT PANEL

CBB771-652A

Fig. 17

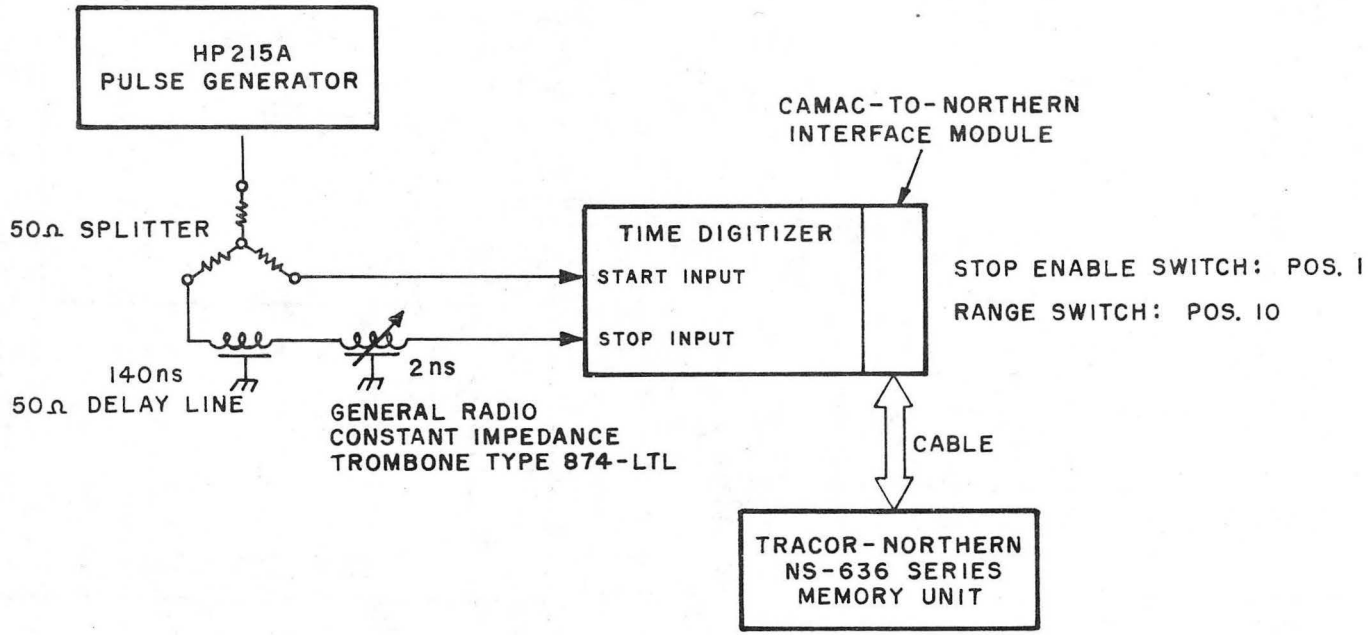
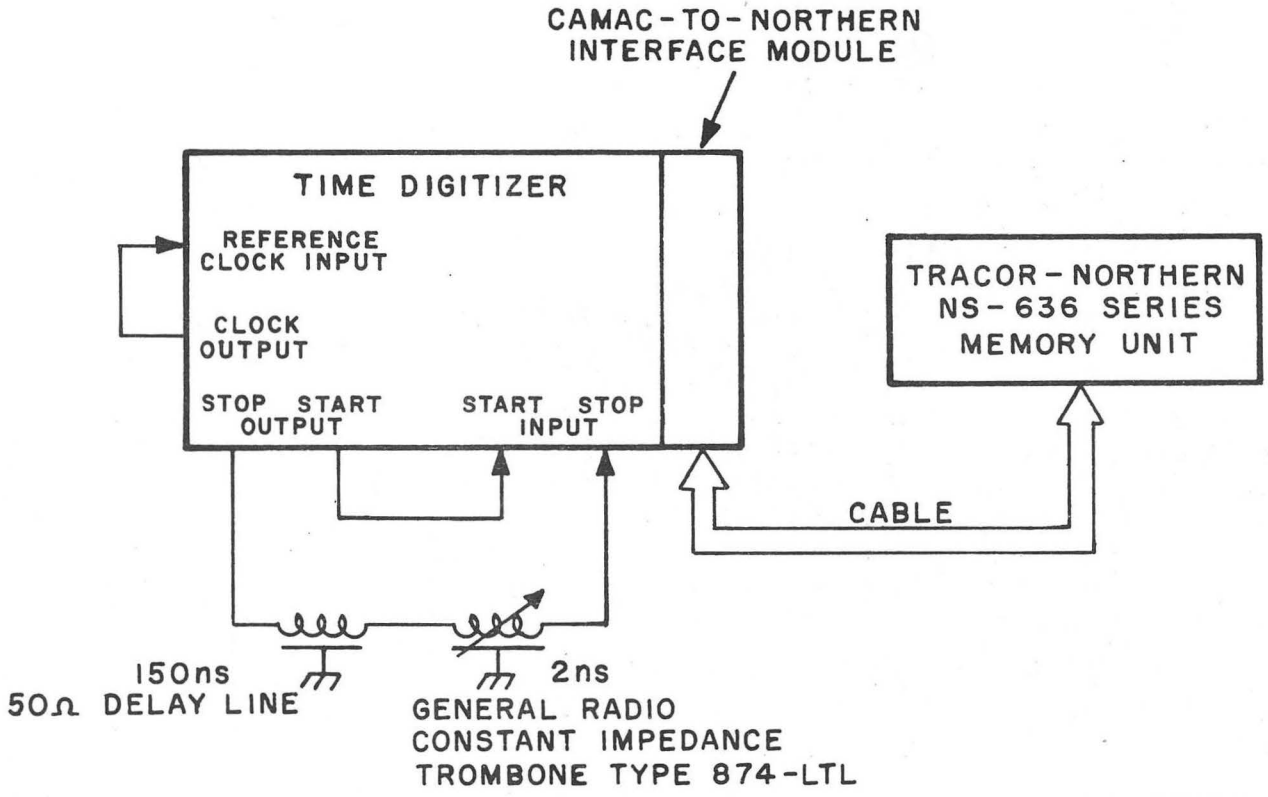


Fig. 18



XBL 773-7911

Fig. 19

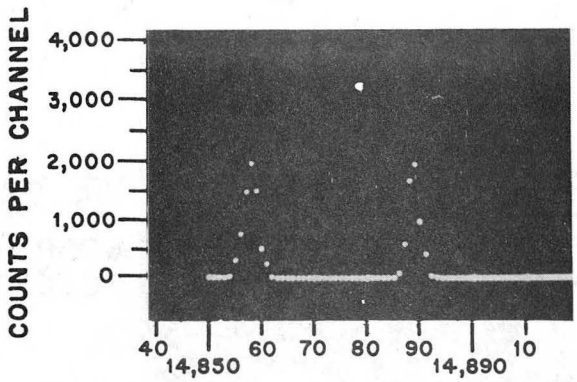


Fig. 20

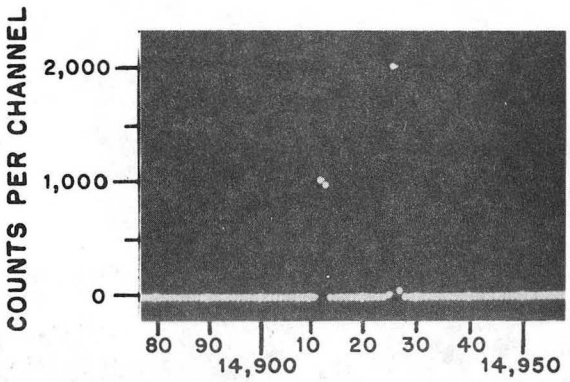


Fig. 21

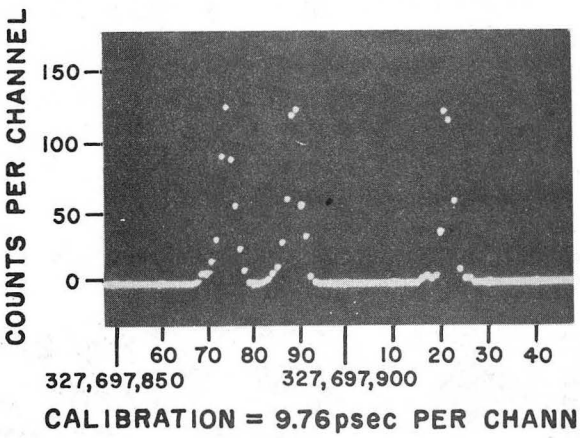


Fig. 24

XBB 773-2292

STOP INTERPOLATOR ALIGNMENT
PULSE REPETITION RATE: 3000pps

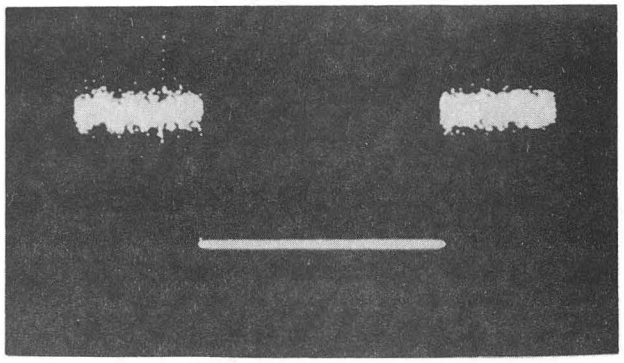


Fig. 22a

STOP ALIGNMENT
POTENTIOMETER: +1/4 TURN

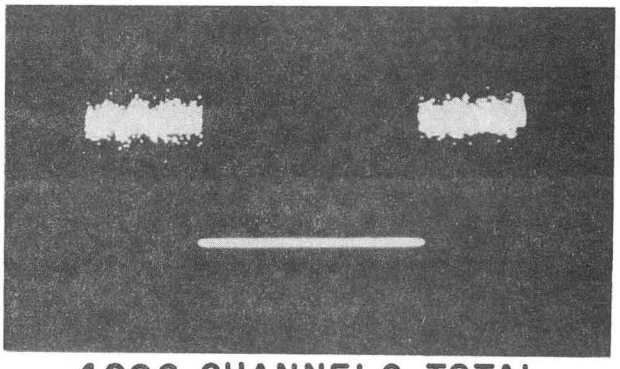


Fig. 22b

STOP ALIGNMENT
POTENTIOMETER: PROPER
ALIGNMENT

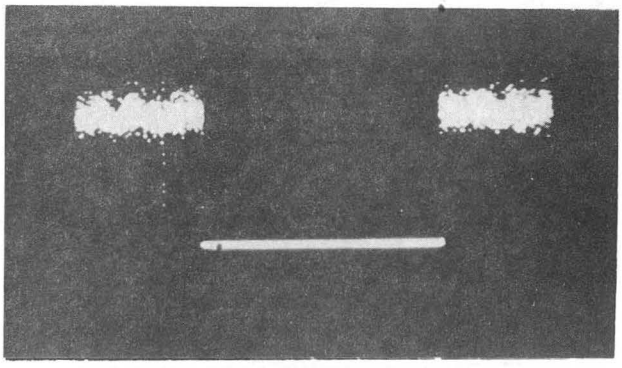
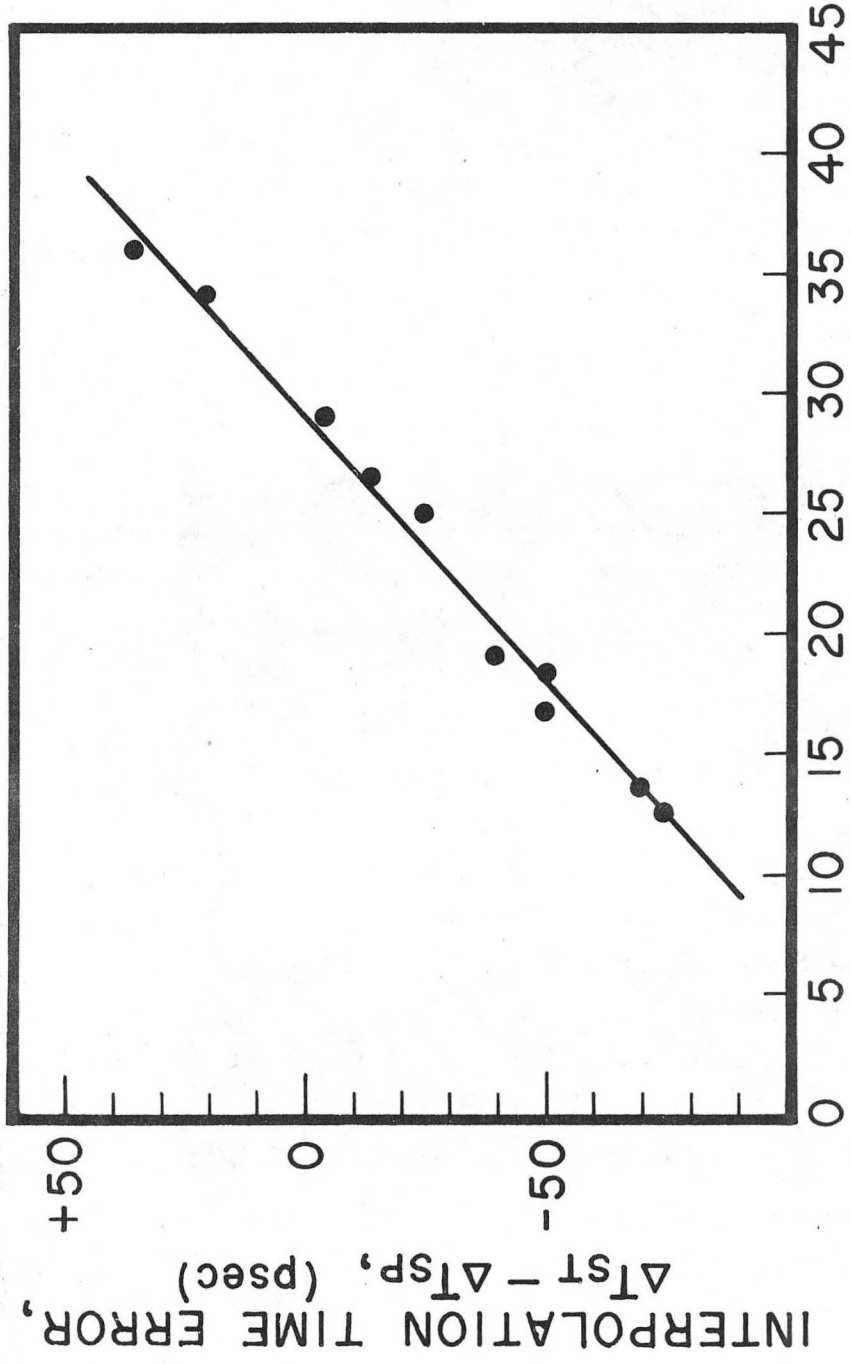


Fig. 22c

STOP ALIGNMENT
POTENTIOMETER: −1/4 TURN

XBB 773-2291



XBL 773-7915

Fig. 23

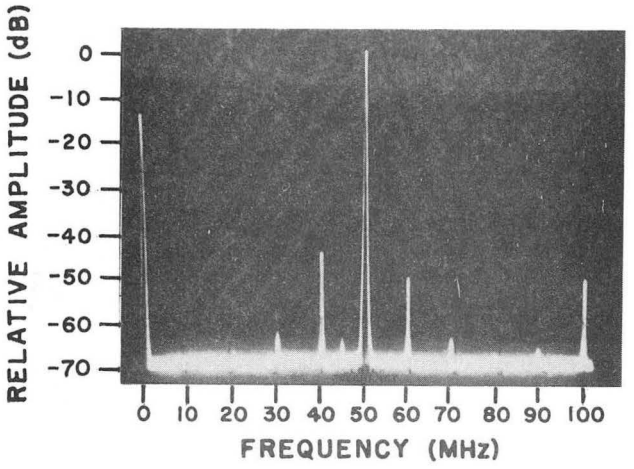


Fig. 25

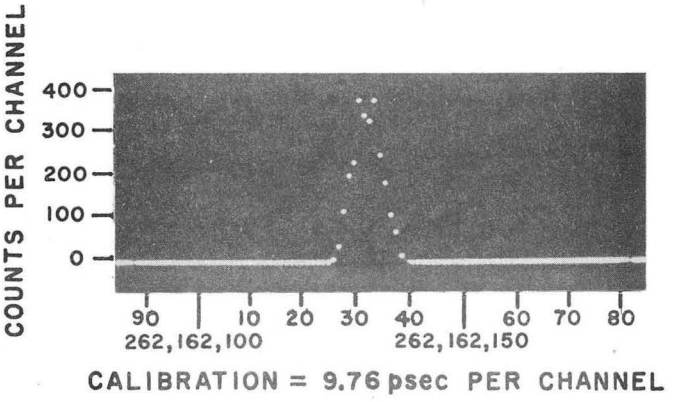


Fig. 26a

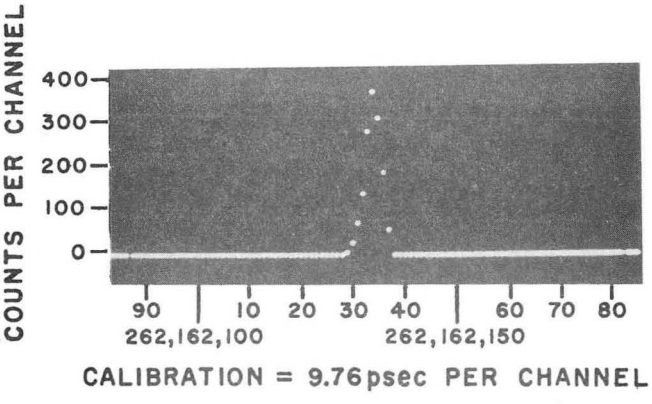


Fig. 26b

XBB 773-2289

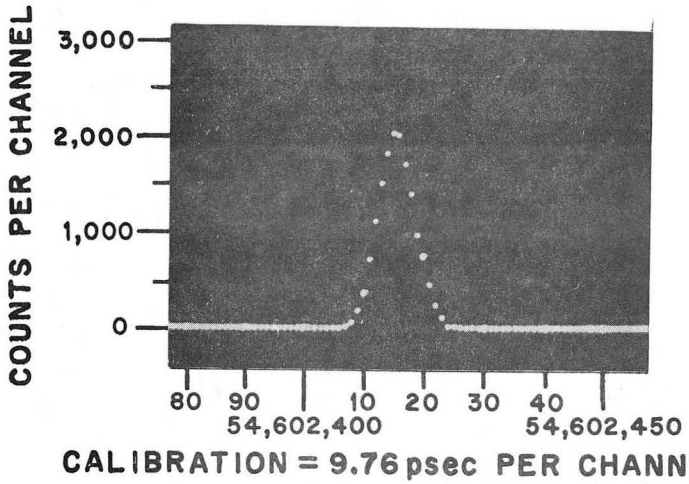


Fig. 27

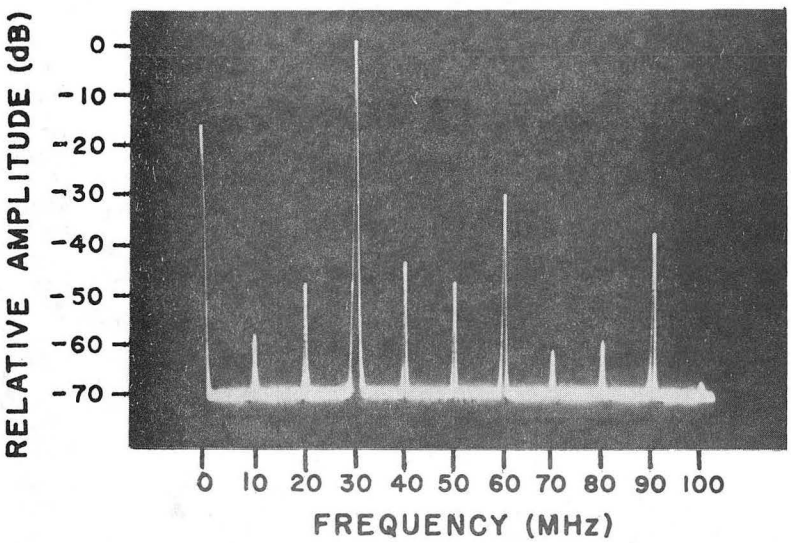


Fig. 28

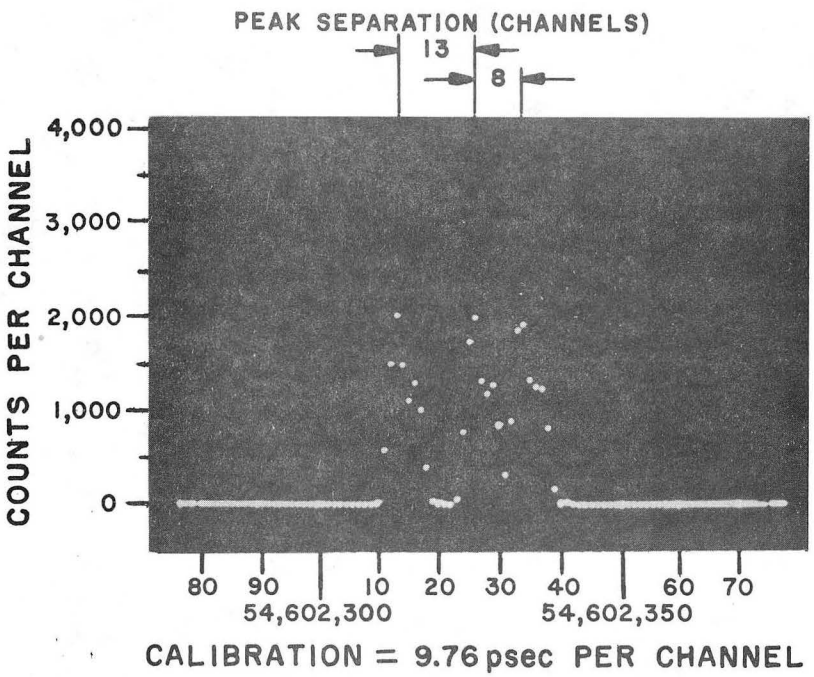


Fig. 29

XBB 773-2290

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