Acquisition and Processing of Multiparametric Information from a Pixel Matrix

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***Abstract*--This paper addresses the design of a system intended to readout multiparametric information from a matrix of pixels.**

The system presented here acquires the charge associated with the signal and provides a timing information from each pixel. Although it lends itself to a broad range of time-correlated imaging situations involving any kind of pixel matrices, the design constraints assumed here are particularly tailored to the application with pixels that sense the output charge distribution from a Micro Channel Plate (MCP).

The combination of a microchannel plate and a pixel matrix is an extremely versatile detector and the readout system must be able to fully exploit the intrinsically high position resolution and time accuracy featured by the MCP.

The behavior of the readout system described in this paper is based upon advanced concepts to meet the above application requirements and is believed to provide a significant functional improvement over the conventional pixel systems.

I. INTRODUCTION

THE introduction of pixel detectors in tracking applications has set the demand for high density readout electronics consisting of one cell per pixel with the task of identifying the address of the pixels where signals above a preset threshold are recorded. The same readout electronics associated with a histogramming memory to build-up the distribution of counts recorded by each pixel in a fixed time interval is employed in imaging applications. In either case, only the presence of a signal is recorded by the readout system [1], [2], [3], [4]. There are, however, situations, where signal-related parameters are to be extracted and a readout that is able to acquire and process multiparametric information is required.

For example, if the value of the charge associated with the signal is available, it is possible to increase the position resolution well beyond the geometric size of the pixel by using an interpolation approach.

Signal timing is important in several time-resolved or time-correlated position sensing and imaging applications. Examples of situations requiring both position and time information are provided by Time-of-Flight mass spectroscopy and by the analysis of reactions initiated by photo ionization (molecular dissociation), where the photo ionization produced by laser light results in fragmentation. Multi hit time-resolved detection may be required in this case [5], [6].

One more example of a situation demanding accurate timing is the principle of three dimensional imaging based upon time-domain reflectometry associated with a pixel matrix.

The idea of multiparametric acquisition from pixel matrices can be extended to more complex cases including other signal features, for instance, shape-related parameters.

The present paper discusses the design of a multiparametric system to be associated with a pixel matrix.

As already pointed out, the system, though not restricted to this application, is conceived to meet the requirements set by the detector shown in Fig. 1, consisting of an MCP read out by a matrix of electrodes deposited on an insulating substrate. The detector of Fig. 1 is extremely versatile. By a suitable choice of the photocathode material or of the input converter, it may be employed to detect photons on a very broad range of wavelengths, from infrared to low energy X-rays as well as particles of different nature, such as neutrons and electrons. The intrinsic position resolution of an MCP is substantially better than that of a semiconductor pixel detector. This is due to two reasons. The diameter of an MCP pixel, the pore, is typically 10 μm and will be reduced to about 0.5 μm in the new MCP generation. Secondly, in a semiconductor detector the lateral spread of the charge cloud is determined by the delta-electrons, while in an MCP it is limited by the MCP pore size. The only way of retaining this feature by a pixel readout of the type shown in Fig. 1 is by making use of position interpolation. A spatial resolution substantially better than the geometric size of the sensing electrodes in Fig. 1 can be reasonably expected from this approach. A remarkable improvement over the existing imaging techniques may be expected in such an important field like mammography.

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In the actual pixel design, the pixel size is 100 μm x 100 μm. The simulation shows that a position resolution of 10 μm, that is, ten times smaller than the pixel size, is obtainable by interpolation provided that the charge be spread over more than three pixels in each direction (X and Y). The improvement in space resolution introduced by an increase in the number of pixels on which the interpolation is carried out (e.g. five in each direction) is not such to justify the increased complexity in the centroid finding logic. However, in the unidimensional case (strip detector), where the centroid algorithm is simpler, the interpolation is done on five elements. One more important feature of the MCP is its timing accuracy, which makes the detector of Fig. 1 particularly suitable for time-resolved and time-correlated applications.

The design concepts presented in this paper have been developed to support a broad spectrum of applications using highly segmented detectors, mainly pixel matrices and, as a particular case, microstrip structures. The next section is devoted to the discussion of these concepts.

II. SYSTEM DESIGN CONCEPTS

The fundamental part of any readout system to be associated with a highly segmented detector is the elementary cell in the case of a pixel readout or the individual channel in the case of a microstrip readout. The former case sets obviously more stringent area limitations, for the pixel size in the matrix fixes the limit to the silicon area available for the elementary cell. The goal assumed in the actual design was a cell complying with the pixel area limitations, whose layout, in the case of a microstrip readout, would be modified to benefit from the more relaxed constraints in the area available.

The application considered of highest importance and originality is the acquisition and processing of charge and time information associated with the signals delivered by the pixels in a detector of the type of Fig. 1.

The following features were considered as targets to be achieved with the elementary cell.

- Must be able to operate at high rates, between 10^6 and 10^7 s^{-1}.
- Its input- equivalent noise charge (ENC) must be in the 500 e region at a detector capacitance of 2 pF.
- Must provide timing accuracy in the subnanosecond region on a broad range of input charge values.
- Must be able to resolve in real time clusters of events, implying a deadtime less than about 100 ns.
- Must be based upon a radiation hard implementation.

The block diagram of the elementary cell is shown in Fig. 2. It consists of a linear amplifying and shaping channel whose output is split along two lines. One is a high accuracy timing channel based upon a constant fraction approach which provides the event timing and also the sequencing signals. The other one is the amplitude storage line, basically a peak sensing analog memory whose operation is controlled by the timing circuitry.

The whole acquisition and processing system will be realized by providing an elementary cell of the type described in Fig. 2 for each pixel to be processed and by adding the circuits that implement the additional functions like centroid finding. The centroid will be determined by applying the suitable algorithm to the values of the charge stored in the analog memories associated with the pixels that belong to a given submatrix, for instance the nine-unit region in Fig. 1.

The complete multiparametric readout system will be built-up by arranging the described elementary cells in a monolithic matrix to match the pixel mosaic. The transmission of the acquired and processed information to the outside world will be based upon a column readout architecture [7].

The basic cell of Fig. 2 may also provide the basis for the development of a microstrip readout system based upon the same concepts illustrated for the case of the pixel matrix. However, in association with a microstrip detector the centroid finding architecture becomes much simpler and can be based on the circuitry whose schematic diagram is shown in Fig. 3 for the case of a three strip position interpolation.

The elementary cells are schematically represented by the triangular blocks in Fig. 3. The Q line out of each cell transmits the charge information as it appears on the storage capacitor C_h in Fig. 2 to the position interpolator. The T lines carry the timing signals from each elementary cell. The position interpolator is enabled by the coincidence of the T signals from the three central strips and vetoed by a T signal which may appear on either of the strips above and below the three on which the centroid is evaluated. The circuit function can be easily extended to situations involving larger number of strips.

The elementary cell was designed in two versions that differ for the geometry of the input active device in the preamplifier and for its standing current. One version is intended for pixel applications for detector capacitances up to 200 fF, the other is tailored for larger pads and short strips up to a detector capacitance of 2 pF.

Emphasis in the design was put on achieving extremely low noise performances at shaping times of a few tens of nanoseconds, to enable the cell to operate at very high hit rates.

As a first example of a system based on the elementary cell of Fig. 2, the realization of a microstrip readout utilizing the logic cluster selection of Fig. 3 is presently underway in a CMOS 0.5 micron process. The next step will be the pixel readout system to be associated with the microchannel plate.

III. THE ELEMENTARY CELL

This section provides a description of the design concepts that have been adopted in the design of the main blocks in the elementary cell.

A. Concepts underlying the design of the preamplifier

In the most advanced CMOS processes with the gate oxide thickness of 10 nm or less, the choice of a P-channel as a

preamplifier input device, driven by the need of reducing the 1/f-noise is no longer mandatory. N-channel MOSFETs parts of a thin oxide process have the advantage of a larger transconductance-to-standing current ratio g_m/I_d over the P-channel MOSFET, yet featuring an acceptably small 1/f – noise. An N-channel MOSFET was chosen as the input active device in the charge-sensitive loop in Fig. 2. In the version intended for larger capacitances, up to 2 pF, the input MOSFET has a gate width W=300 μm and a length L=1 μm. At the design standing current of 200 μA it features a transconductance g_m of 3.3 mS. In the version for smaller detector capacitances, below 200 fF, the input device has a gate width W=30 μm and a length L=1 μm. At a standing current of 20μA it features a transconductance of 0.33 mS, both being the g_m values provided from simulations. The feedback capacitor is 0.14 pF in both configurations.

B. Concepts adopted in the design of the shaper

For the shaper which follows the preamplifier in Fig. 2, a design approach which is to be considered original in a monolithic CMOS implementation has been adopted. The idea was to transfer onto a monolithic chip the design of a triangular or trapezoidal shaper which in a discrete design would rely upon delay lines.

For this purpose a delay unit was required. It has been realized on the basis of a feedback, unity gain buffer. The Laplace-domain operator $(1-e^{-sT})$, where s is the complex variable, has been obtained as shown in the block diagram of Fig. 4a), where D is a difference amplifier.

The actual realization is shown in Fig. 4 b), where the buffer is made of the long-tailed pair Q1,Q2, the source follower Q3 and associated current sources. The difference amplifier D, made of transistors Q4 through Q14 is an open-loop structure. Nonetheless, its linearity is good thanks to the distorsion-compensation technique applied to both signal paths (Q7 Q6 Q4 Q5 Q14) and (Q8 Q9 Q10 Q11 Q12 Q13).

The delay-based shaping concept sketched in Figs. 4a) and b) was proven to be adequate. Within a given CMOS process, indeed, the delay obtained from the feedback unity-gain buffer is to be considered stable and reproducible to the extent required by the actual application.

C. The architecture of the elementary cell

The complete architecture of the elementary cell is shown in Fig. 5. The signal at the output of the first shaper unit, the one implementing the $(1-e^{-sT})$ operator, splits along two lines. The upper one completes the shaping by introducing a second delay-line operator $(1-e^{-2sT})$ to multiply the first one. The resulting bipolar signal goes to an integrator which produces at its output a trapezoidal signal. B is a unity gain buffer, Z is the zero-crossing trigger and A the preset (arming) circuit.

The lower signal path includes the constant-fraction trigger which provides the hit timing and the control of the charge storage circuit. The presence of a flat-top in the trapezoidal shaper and the timing accuracy of the constant fraction trigger guarantee that the ballistic errors and the amplitude loss in the storage operation be kept very small. The signal provided by the constant fraction trigger and the trapezoidal integrator output are shown in Fig. 6 a) and b).

D. The timing circuit

The timing circuit is a constant fraction discriminator. Its implementation benefits from the delay-based approach adopted for the shaper. As shown in Fig. 5, which describes the entire analog cell, its core is the multistage difference amplifier D1. This subtracts the signal at the output of the first shaper section, attenuated by the capacitive divider C, C(1-f)/f, which defines the constant fraction f, from a signal taken from a node inside the second section of the shaper. The amplified difference signal, by virtue of the large amplification, features a very steep slope at the crossover point, whose time of occurrence is detected by a zero-crossing discriminator to provide the time definition of the hit.

Particular design care had to be taken to prevent the high gain difference amplifier D1 in Fig. 5 from undergoing a heavy overload in presence of a large input signal.

IV. CIRCUIT BEHAVIOR

In the version that will be fabricated in 0.5 micron process, the circuit of Fig. 5 is intended for operation with values of the input charge ranging between $2x10^4$ and $5x10^5$ electrons.

The simulations have provided information about the circuit behavior, adding more support to the choice made of designing the shaper on the basis of the delay principle.

The analog signal obtained from the shaper in response to a delta-impulse current from the detector, shown in Fig. 6b), approaches closely the trapezoidal waveform it aimed at. It has a well pronounced rounded top, which makes the sampling operation very accurate. It has a shape, with almost symmetric leading and trailing portions and features a regular, monotonic recovery to the baseline. These characteristics, associated with its short basewidth, about 45 ns according to Fig. 6b), make the circuit suitable for operation at very high hit rates.

The signal shape of Fig.6 b) is the same regardless of whether the charge-sensitive loop employs the larger or the smaller input transistor. This is due to the choice of the geometry and of the value of the standing currents which, as pointed out in sect II A, provides in either case a value of the transconductance which is proportional to the largest value of the detector capacitance foreseen for each configuration. This results in a preamplifier risetime which has a little dependence on the detector capacitance the cell is operating with, thus affecting the final shaped signal only to a negligible extent.

The logic signal of Fig. 6 a) is the gating command provided by the timing circuitry. Comparison of the time

relationship of Figs. 6 a) and b) shows that the storage of the analog amplitude is achieved with a high degree of timing accuracy, in correspondence of the center of the rounded top of the analog signal.

The simulated noise behavior for the two versions of the cell was investigated with reference to the delta-response of Fig. 6 b).

The cell employing the charge sensitive loop with the larger input transistor, W/L=300/1 operating at a 200 μA standing current, features an equivalent noise charge ENC of 550 e rms at a 2pF detector capacitance.

The noise-induced time-resolution variance σ in the triggering instant of the timing circuit is plotted in Fig. 7 as a function of the charge injected at the input by a delta-impulse.

The plot of Fig.7 shows that the noise-induced dispersion of the triggering remains almost constant for input charge exceeding $2x10^4$ electrons. This indirectly proves that the slope at the crossover point of the signal presented at the zero crossing discriminator is independent of the injected charge value.

This independence results in a limited time walk which is less than 1ns over the entire range of input charge values, from $2x10^4$ to $5x10^5$ electrons.

The cell employing the charge sensitive loop with the smaller input transistor, W/L=30/1 operating at a 20 μA standing current, features an equivalent noise charge ENC of 240 e rms at a 0.2 pF detector capacitance.

The noise-induced time-resolution variance σ in the triggering instant of the timing circuit is plotted in Fig. 8 as a function of the charge injected at the input by a delta-impulse. Comparison between the curves of Figs. 7 and 8 shows that the values of the noise-induced dispersion in either version of the elementary cell are approximately proportional to the relevant ENC, which confirms that the values of the slope at the crossover point are independent of the geometrical features and standing current of the input device in the charge-sensitive loop. This is one more benefit of having designed the two versions with the criterion of having the same risetime in the charge-sensitive loop.

The value of ENC has a good degree of uniformity across the the chip. This is related to the large size of the input transistor in the preamplifier, which results in a little dispersion in the transconductance, the parameter which governs the dominant noise source, the channel thermal noise. The channel-to-channel ENC dispersion has been evaluated to be less that 5%, a value which has been confirmed experimentally by previous implementations of similar chips.

The offset contribution to the comparator threshold dispersion across the chip was estimated to be about 2.5 mV rms. This value is determined to a large extent by the gate area 24μmx0.5μm of the balanced amplifier at the comparator input. A larger area would have resulted in a smaller threshold dispersion, which however would have impaired the triggering speed of the comparator.

The static power dissipation in the cell designed for larger capacitances, whose input device operates at a higher current is 3mW. As the only difference between the two cells is in the input device, the static power dissipation in the cell designed for small capacitances is slightly less, as determined by the difference in the input transistor current (20 μA against 200 μA). Considering the low noise and accurate timing performance of the cell, the above power levels are fully satisfactory. A substantial power reduction can be achieved by relaxing the constraint of a low noise charge measurement at the shaping times over 50 ns.

V. CONCLUSION

A monolithic readout system for highly segmented radiation detectors is being developed, based upon the advanced concepts of the elementary cell described above. The system stores the value of the charge associated with the detector signal to allow position evaluation by charge interpolation and performs an accurate determination of the time of occurrence of the signals.

The low noise, high counting rate and timing accuracy are attributed to the original approach adopted in the shapers that follow the charge-sensitive loop. This approach consists in transferring onto a silicon chip the concept of a trapezoidal shaper which in a discrete circuit realization would rely upon delay lines.

VI. REFERENCES

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VII. DISCLAIMER

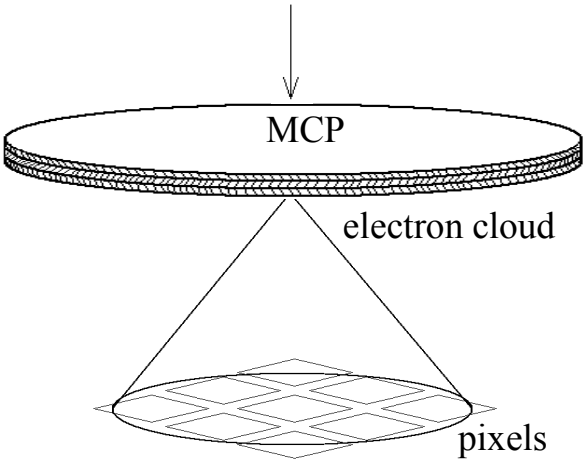

Fig. 1. Micro Channel Plate read out by a pixel matrix.

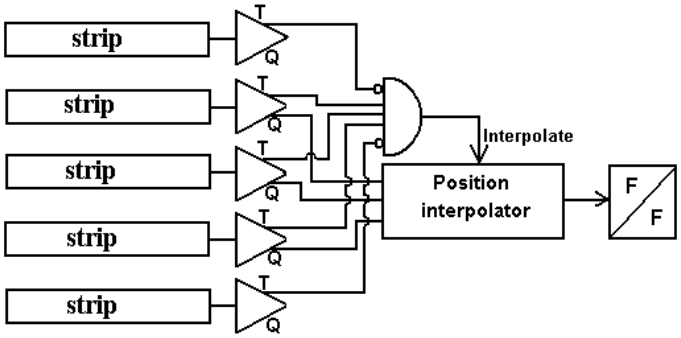

Fig. 3. Centroid finding logic for a microstrip readout
F/F is a flip-flop. The triangles are the elementary cells.

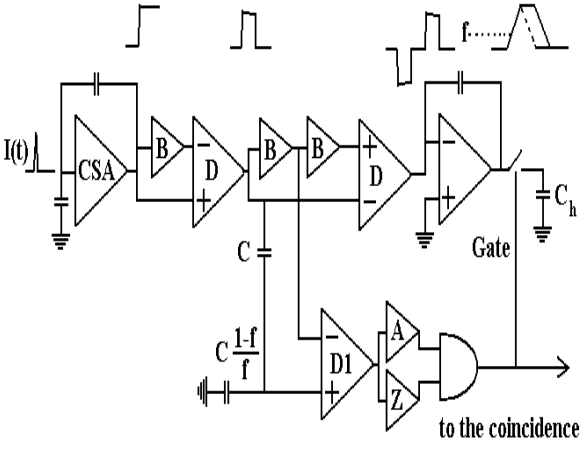

Fig. 5 Architecture of the analog channel.
CSA is the charge-sensitive preamplifier, C_h the storage capacitor, B is a unity-gain buffer, D,D1 are difference amplifiers, A is the arming circuit, Z is the zero-crossing discriminator and f is the constant fraction.

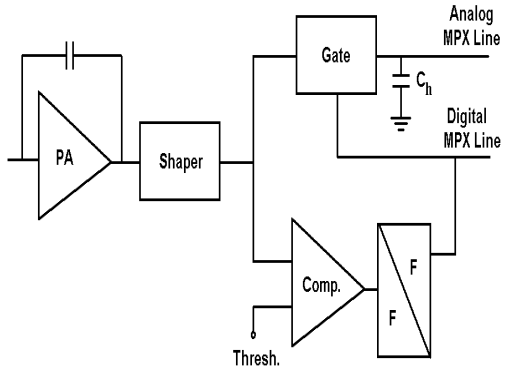

Fig. 2. Conceptual diagram of the elementary pixel cell.
PA is the preamplifier, F/F is a flip-flop and C_h the storage capacitor.

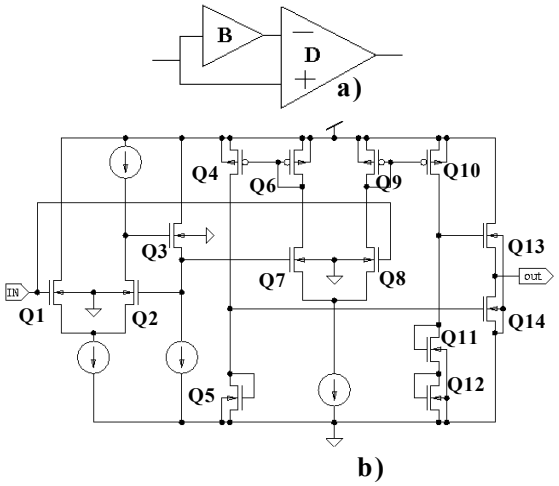

Fig. 4 – On-chip realization of the $(1-e^{-sT})$ operator.
a) block diagram b) detailed circuit
B is a unity gain buffer and D is a difference amplifier.

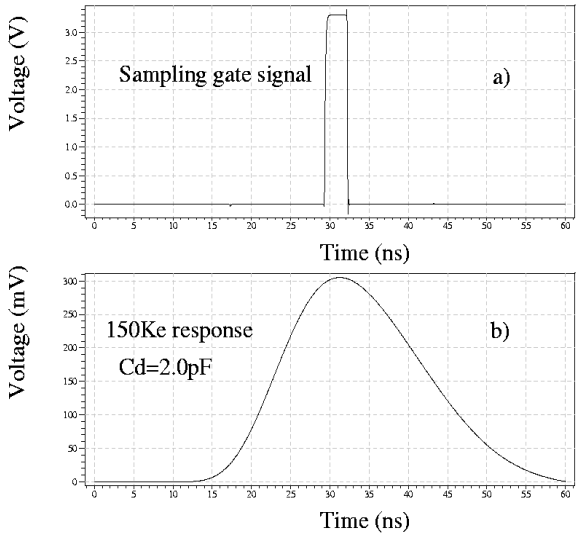

Fig. 6 Waveforms relevant to the elementary cell according to the simulations. a) gating signal provided by the timing circuit b) trapezoidal signal at the shaper output.

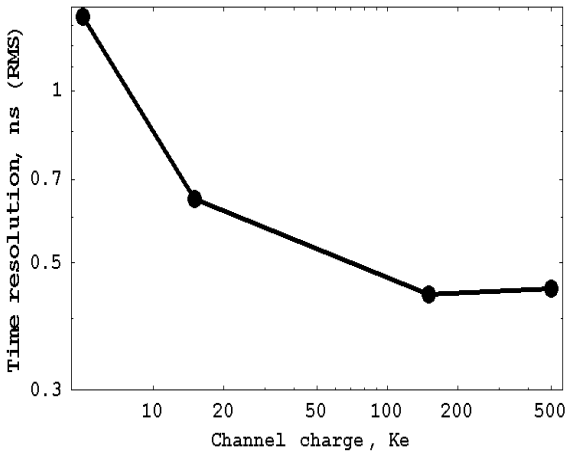

Fig. 7. Noise-induced dispersion on the triggering instant of the timing circuit as a function of the charge injected at the input of the preamplifier by a delta-impulse. The plot refers to the channel for detector capacitances up to 2 pF.

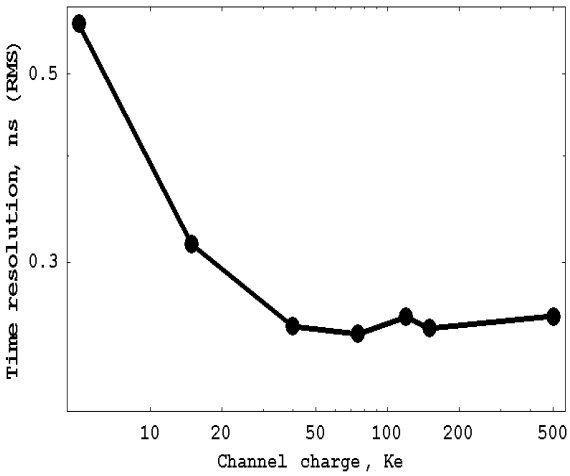

Fig. 8. Noise-induced dispersion on the triggering instant of the timing circuit as a function of the charge injected at the input of the preamplifier by a delta-impulse. The plot refers to the channel for detector capacitances up to 0.2 pF.