UNIVERSITY OF CALIFORNIA
RIVERSIDE

Lithographic Patterning for the Seeded CVD Growth of Novel 1D and 2D Materials

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Materials Science and Engineering

by

Michelle Wurch

September 2021

Dissertation Committee:
Dr. Ludwig Bartels, Chairperson
Dr. Jianlin Liu
Dr. Chun Hung Lui

The Dissertation of Michelle Wurch is approved:

Committee Chairperson

University of California, Riverside

Acknowledgment

I would first like to express my sincerest gratitude for my advisor Ludwig Bartels. He provided many opportunities for learning which promoted my educational and personal growth. Under his supervision and guidance, I was able to contribute to a wide variety of research endeavors. I would also like to thank Dr. Valentine Vullev who supervised my research as an undergraduate student in the bioengineering department. I'm extremely grateful to have had such an incredible variety of research experiences which ultimately steered me onto my current path in life. In order to achieve the most out of research in a lab, mentors are of upmost importance because their daily guidance allows for smooth integration into such environments. As such, I give my most heartfelt gratitude to my mentors John Mann, Jillian Larsen and Edwin Preciado. They each guided me through unique research paths and taught me the foundational skills I spent my graduate years building upon. Throughout my graduate years I met a variety of other students whom I'd like to thank as well, in no particular order: Koichi Yamaguchi, Thomas Empante, Daniel Coyle, Kortney Almeida, I-Hsi Lu, Velveth Klee, Jing Jin, Mike Valentin, Adam Berges, Sarah Bobek, Ariana Nguyen, Joe Martinez and David Barroso. I would like to thank Dr. Hubert Krenner for my time spent working in his lab during my Nano-Initiative Munich summer fellowship program in 2017 as well as his two students, Sebastian Hammer and Lisa

Janker, who treated me with upmost hospitality and made my stay in Germany a cherished memory.

Finally, I would like to thank my family: my parents, my brother Andrew Wurch, my aunt Tatyana Virkh, my uncle Misha Virkh and my cousin Yelena Virkh. They supported me through many difficult moments and helped to celebrate the happy occasions.

ABSTRACT OF THE DISSERTATION

Lithographic Patterning for the Seeded CVD Growth
of Novel 1D and 2D Materials

by

Michelle Wurch

Doctor of Philosophy, Materials Science and Engineering
University of California, Riverside, September 2021
Dr. Ludwig Bartels, Chairperson

Lithographic device fabrication is a crucial part in the characterization of novel 1-and-2-dimensional (1D/2D) materials for electronic applications. In this thesis, I will present patterns and devices tailored, respectively, to the seeded chemical vapor deposition (CVD) growth and characterization of MoWSeS alloys, tantalum triselenide ($TaSe_3$) nanowires, and zirconium tritelluride ($ZrTe_3$) nanoribbons. Patterning of silicon dioxide (300 nm) on silicon wafer pieces allows for predetermined channel width and height of subsequent devices on the deposited transition metal dichalcogenide (TMD) 2D films. Patterning of 8 nm thick nickel metal films, allows for predetermined and predesignated $TaSe_3$ nanowire growth on SiO_2/Si substrates as a pathway for future on-chip interconnects by direct CVD growth. These nickel “waypoints” also serve as probe contact pads for facile and quick electrical characterization with minimal processing steps.

Table of Contents

List of Figures

Chapter 1: Foreword

1.1 Background

The advancement of technology has been a crucial aspect of our progress as a society. As such, it is with no surprise that we have keenly documented and followed the advancement in an attempt to predict a roadmap for leading research into the uncharted territories of smaller and smaller transistors on integrated circuits. As Moore's law states: the number of transistors on any given microchip will double every two years. There is much speculation and debate that our progress has slowed sufficiently that Moore's law is no longer valid in our current year. Much research has been done in an effort to find new materials that will support ongoing miniaturization of microelectronic devices: These include two-dimensional transitional metal dichalcogenides (2D TMDs), as well as new material for replacements of traditional copper metal serving as on-chip and chip-to-chip interconnects. An example of the latterare one-dimensional transition metal trichalcogenides (1D TMTs).

Many standard, as well as, unique approaches have been explored in the study of these materials properties. Ideally, we study these materials at their smallest/thinnest size so as to most closely resemble the conditions for their future application in microchips. The most common method of obtaining thin

samples of 2D TMDs and 1D TMTs is to exfoliate them from a bulk crystal sample. However, exfoliation arguably selects for the worst material in the bulk, as the exfoliation tears away first, what was least attached to the bulk, presumably due to the presence of defects.

In Dr. Bartels' research group, we took a different approach: direct synthesis via chemical vapor deposition (CVD) where appropriate reagents are vaporized in a closed system and allowed to nucleate and propagate on a substrate surface, forming single crystalline material of varying scales in size.

Both exfoliation and CVD growth are challenged in controlling the location and orientation of the materials.This thesis aims to explores how lithographical patterning of wafer substrates can encode and guide CVD material growth.

1.2 Two-Dimensional (2D) Materials (MoS_2)

Molybdenum disulfide (MoS_2) is a two-dimensional (2D) transition metal dichalcogenide (TMD) material that can be prepared in a stable form down to the single-layer limit. As this material is thinned down from bulk to the monolayer, it transitions into a direct bandgap semiconductor with a gap of ~1.8 eV [1, 2]. Single-layer MoS_2 transistors have been fabricated and studied with electrical transport measurements. These studies report the transistors as having mobilities on the order of 1 $cm^2\ V^{-1}\ s^{-1}$ and beyond [3-6]. Most MoS_2 materials, whether bulk or at the monolayer limit, exhibit *n*-doped behavior [3-9]. MoS_2

shows extremely promising results as a future candidate for electronic transistors, phototransistors and – due to spin-orbit coupling in the d-orbitals – valleytronics devices[8][10-14].

Although mechanical exfoliation [15] of MoS_2 monolayers is the most common method to prepare single-layer islands/films in the lab, MoS_2 can also be synthesized by chemical vapor deposition (CVD); many studies have confirmed its ability to grow on Cu [16], Au [17-20], SiO_2 [17, 21], and various other surfaces [6, 17, 22]. MoS_2 growth via CVD is a very simple process. I started work in this field by contributing to one of the first publications that achieved single layer growth of TMDs.

Monolayer TMD films, such as MoS_2 and WS_2, show promise in continuing Moore's law towards smaller transistors; this is due to their well-defined semiconducting behavior and relatively stable nature in atmosphere.[23-25] At the single-layer limit, TMDs show high on-off switching ratios and other interesting electronic and optical properties [26-30].

The CVD growth of MoS_2 is conceptually simple, yet there are challenges in detail. One of the key factors to success is the cleaning and treatment of the growth substrate. In my studies I use 300 nm SiO_2 on Si wafers that are diced into ~1cm × 1.5cm pieces. They are thoroughly cleaned using an acetone/IPA rinse and then soaked in a Piranha solution for 20 minutes. These substrates are then rinsed multiple times with deionized water, dried with nitrogen gas, and

directly loaded into the tube furnace in the center of the hot zone as shown in Fig 1.1. Before the furnace is r heated, the precursor reagents (molybdenum oxide and sulfur) are placed such that the growth substrate sits on the oxide boat and the sulfur boat is placed just outside the tube furnace enclosure. The boats are made of a ceramic material called alumina, which is aluminum oxide. Purging the tube with nitrogen gas is a crucial step for creating our desired environment and the furnace is heated to 150℃ and held for 1 hour to promote dehydration. The last step is to ramp the furnace temperature to 650℃ and hold it for 5 minutes. Subsequently the furnace turned off and allowed to cool to room temperature.

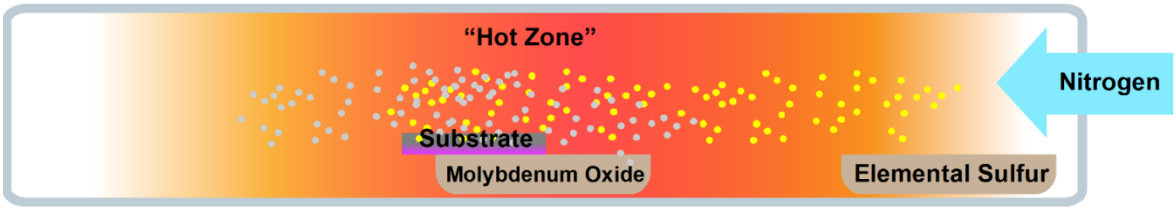


Figure 1.1: Schematic of CVD growth of MoS_2 including the sealed heated quartz tube with an inlet and outlet for nitrogen gas, the two precursor reagents (elemental sulfur and molybdenum oxide), and the growth substrate (300nm SiO_2 on Si).

1.3 One-Dimensional (1D) Materials ($TaSe_3$/$ZrTe_3$)

Recently, there has been wide-spread interest in new materials which resemble the 2D materials in that their bulk crystal structure contains van der Waals gaps. However, for these new materials, the gaps are tubular in nature creating one-dimensional (1D) stacks of bound atoms separated from each

neighboring stack. $TaSe_3$ has a monoclinic unit cell and consists of stacks of Ta atoms, each of which are bonded to three selenium atoms above and below along the b axis. Initial transport measurements on metallic 1D vdW tantalum triselenide ($TaSe_3$) and zirconium tritelluride ($ZrTe_3$) show good conductivity and high breakdown current which reveals these 1D materials as viable replacements for copper in on-chip and chip-to-chip connections. The chemical vapor deposition (CVD) growth of $TaSe_3$ and $ZrTe_3$ allows for the synthesis of nanowire material of just a few nanometers of cross-sectional area. These are the ideal sizing for most realistic industry standard processing conditions for testing purposes. Although the nanowire bundles are small, they retain their bulk conductivity, unlike for traditional metals such as copper which are severely affected by electromigration and thus have drastic drops in bulk conductivity when they are thinned down[33-35]. Low-frequency noise measurements of $TaSe_3$, as thin as 10 nm across, shows electromigration resistance of more than twice copper and has an extremely large breakdown current of more than $1 \times 10_8$ A/cm^2 [36]. As such, we can see why these 1D materials are suitable areas of study as potential interconnect material suitable for the scaling down of transistors and in line with Moore's law[37-40].

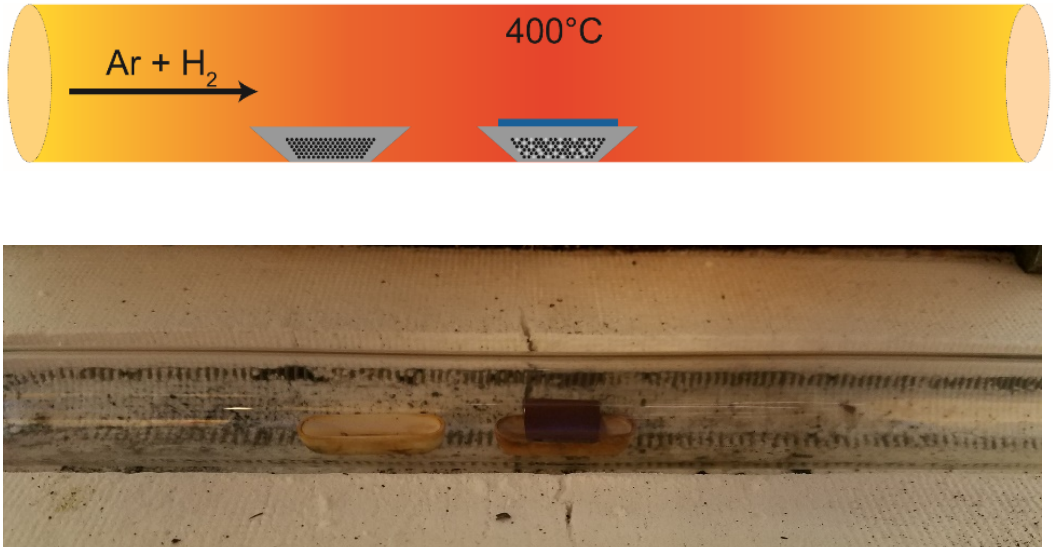


Figure 1.2: (Top) Schematic drawing of CVD growth process for TaSe3 nanowires including sealed heated quartz tube with gas inlets and outlets for argon and hydrogen. Precursor reagents of selenium powder and tantalum pentachloride contained in alumina boats with growth substrate in the center. (Bottom) Actual image of boats and substrate placements inside tube furnace.

The preparation of the 1D TMT material, $TaSe_3$, begins on a commercial 300 nm SiO_2/Si substrate using process parameters (ambient pressure, ≤ 400°C process temperature, ≤ 5 min process duration) that are amenable to conventional back-end-of-the-line (BEOL) process limits. The CVD growth (Fig. 1.2) method involves placing the growth substrate over an alumina boat containing selenium and tantalum pentachloride precursor reagents. This boat is then placed in the center of the hot zone. A boat with extra selenium precursor is placed downwind and acts to replace selenium vaporization off the growth substrate. Argon and hydrogen gas purge the quartz tube and the furnace is

heated to 400 C. It is held at that temperature for 2 minutes and then cooled to room temperature.

1.4 Lithographic Encoding of Growth Locations

This thesis explores strategies how lithographically patterned wafer substrates as potential “roadways” guiding 2D and 1D material growth, thus offering control over material placement/location and orientation. We have studied numerous ways of inducing preferential nucleation of 2D material growth. Several such methods include 1) creating artificial defects by purposefully scribing marks into the growth substrate, 2) creating defects in SiO_2 surface by patterning the wafer followed by etching and 3) creating patterns on the wafer via photolithography or electron-beam lithography and depositing certain metals meant to act as precursor reagents and nucleation spots. Figure 1.3a,b shows the same array of circular patterns which have either been raised or etched down, thus creating artificial defect edges along the wafer surface which act as nucleation spots. We have also used this mask to deposit a thin layer or molybdenum metal which also acted as seeding/nucleation spots. We have indeed seen that thin-film TMDs can coalesce during CVD growth and form a large-scale film. An important question to ask for 1D material is if they have any “interconnect” potential. Can they “coalesce” or branch and, if not, then can two wires which touch actually conduct current through their junction? Fig 1.3c shows that 1D TMT materials such as TaSe3 do have capability of growing in branched

directions and as such, there is strong indication of the materials ability to seed growth along a pre-defined wafer pattern.

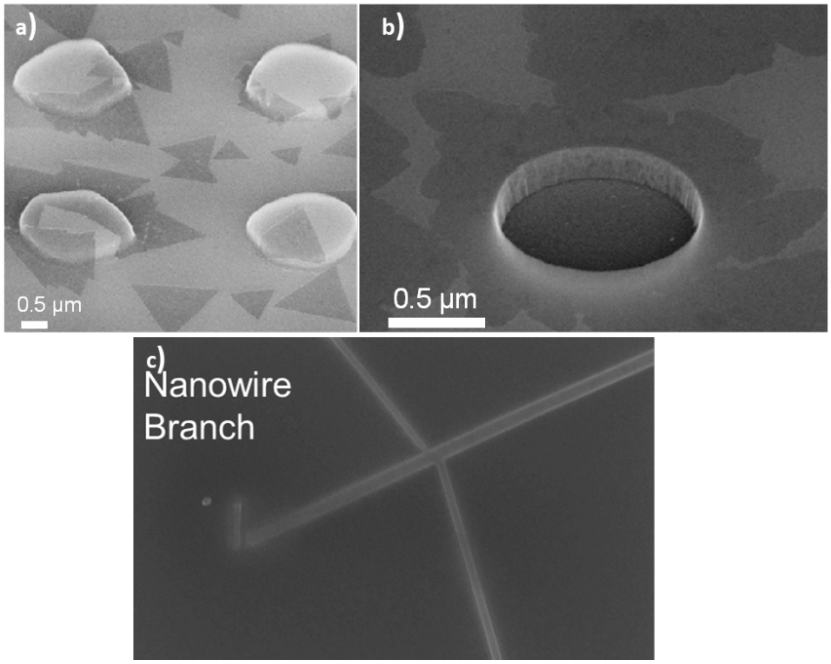


Figure 1.3: SEM imaging of prepatterned substrates with SiO_2 circles raised 250nm from the surface (a) and with the circles etched down 250nm (b). 2D TMDs preferentially nucleate on these features. (c) 1D TMT can grow in a branched manner, indicating the potential for wire-routing applications, if strategy is found to guide the growth location and direction on the substrate.

Chapter 2: Cleanroom Processes

2.1 Device Lithography

The two most common methods for patterning silicon wafers are Ultraviolet (UV) -photolithography and electron beam lithography (EBL). Generally, for these methods, one spins a thin layer of a polymer-based photo- or electron-beam resist onto a wafer substrate and then expose certain patterns/areas to the UV-light or an electron beam. This exposure induces a chemical reaction that causes renders the resist either more (positive resist) or less (negative resist) soluble in a solvent called the developer.

UV-photolithography is the most commonly used method for exposing large wafer areas for pattern transfer from a mask or reticle. A UV-photolithography mask is traditionally made of a square quartz substrate with a chromium film into which a pattern is etched. Where the chromium film is etched away, UV light passes through the mask and exposes the resist; where the film is present, UV-light is reflected away and the resist is not exposed. Wafer preparation for UV-photolithography starts by a several-step cleaning process using various solvents including acetone, isopropyl alcohol (IPA) and methanol.

The wafer is then dried with nitrogen gas and baked on a hotplate to ensure complete removal of any water or remaining solvent residues. Next, to prepare the wafer for the photoresist, a surfactant such as HMDS (hexamethyldisilazane, [(CH3)3Si]2NH), is usually spun onto the wafer. This renders the surface of the wafer more hydrophobic and allows for rapid and uniform wetting by the photoresist. The cleaning, dehydration bake and HMDS application are the three most crucial steps for successfully preparing a wafer and avoiding delamination of photoresist from the wafer in subsequent processing steps. Delamination results in profound pattern errors later in the process flow. Once the wafer is prepared, the photoresist may be applied via spin-coating. Either a positive or negative photoresist may be used at this time. In a positive resist the UV exposed areas will degrade and become slightly acidic, facilitating their removal in the slightly basic developer environment later. When negative resist is used, the UV light causes polymer cross-linking resist in the exposed areas and patterns, which strengthens the resist against dissolution and allows for the remaining unexposed areas to be dissolved in the developer solvent.

Once the photoresist has been applied properly, the wafer is placed into an exposure instrument, such as the Karl Suss mask aligner in UCR's cleanroom, where the mask is placed in between the wafer and the UV light source. After the exposure to the UV light, the wafer is immersed in the developer solution for a certain period of time allowing the pattern to be revealed. After development, the wafer substrate is frequently baked on a hotplate which

serves both to smoothen out any rough edges in the pattern and to again dehydrate the exposed surface of the wafer, preparing it for the next steps it might undergo. The patterned wafer may now go through a wet or dry-plasma etching process such as reactive ion etching (RIE), inductively coupled plasma etching (ICP-RIE) or have material deposited via plasma enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), sputtering deposition or electron beam evaporation. Once the etching or material deposition is complete, the photoresist is stripped or “lifted off” by soaking and spraying the wafer with acetone and/or special photoresist stripping solvents. As such, UV photolithography is a great method for rapid large-scale (industrial) pattern definition and transfer onto wafers. However, its critical limitation is the minimum aspect ratio available for pattern size. In the instrument in UCR’s cleanroom, this is roughly 1 – 2 micrometers. For smaller pattern designs, we must use another lithographic method called electron beam lithography.

Electron beam lithography is more commonly used for smaller and unique pattern designs for research and testing purposes. These are patterns and designs that must change often to fit each unique sample need and fulfil specific testing requirements. I use EBL mostly for creating various potential CVD growth seeding patterns as well as designing and fabricating electrical devices on the resulting 2D film and 1D/Quasi 1D nanowires and nanoribbons. EBL is operated under very high vacuum environments because a beam of electrons is generated at a tip and guided through a large column with many electromagnets to guide

the directionality of the beam. The beam is scanned following a pattern design created in computer-aided design (CAD) software. The most critical parameter for EBL is the dosage as it changes frequently depending on the gun current and pattern design aspect ratio (i.e. how large or small the exposed area shall be and how close or far the exposed area is from other exposed areas). More commonly, we can describe this as the proximity effect which is due to the exposed dose distribution as normally the developed area will be slightly larger than the area scanned by the beam, because of the primary electron scattering.[41] As such, it is imperative to take correction counter-measures such as using different dosages for different sections in the pattern, for example, larger exposed areas using less dose and smaller exposed areas using higher dose, but smaller exposed areas near other exposed areas using less than the former.[42] This is because areas near and or adjacent to previously exposed areas will receive an overall “higher than intended” dose of the electrons because of aforementioned scattering. Always we must keep the design and exposure area in mind when performing EBL on various samples. This includes the striations in the spun-coat resist caused by nonuniform samples, such as samples that have undergone CVD growth process and thus may contain varying amounts of post-growth debris and precursor adhesion in different areas on the substrate. This causes an uneven spinning of the resist such that we must note which areas may have slightly thinner and slightly thicker layering of the resist so

that we can adjust the electron dose accordingly (i.e. thinner areas requiring less dose than thicker areas).

The most commonly used electron beam resist is polymethylmethacrylate (PMMA) and this is a positive resist. PMMA usually comes in acetone solvent, but I use PMMA dissolved in chlorobenzene to offer less sensitivity towards our very thin as well as oxygen sensitive 2D and 1D CVD grown materials. Once the PMMA is spin-coated onto our samples, the first step is to EBL write an alignment matrix. This is to give us a way of localizing the area of interest so that we can find our ribbon or nanowire of choice under the electron beam and give the offset coordinates to guide the beam for writing. The alignment matrix is a numbered grid of varying size which gives us a localized plane to mark and hit our target sample area within error of less than 50 um. The cross hairs in the matrix are spaced 50 um apart and this allows us to centralize the beam at specific crosshairs and as it acts as the zero/zero point, the CAD drawing marks x-y distances from the central crosshair to write the designed pattern in local areas of interest. Once the matrix has been written and the sample has been developed, I map out the area with optical imaging and create a collage of the images in the CAD software, overlaying it onto the original CAD drawn matrix. The better the optical images overlay with the original drawn matrix, the more precise the device positioning will be in the next steps. Designing the device drawing is unique to each sample because the CVD grown wires come in different sizes and sometimes interconnect at varying angles which requires the

adjustment of device design in terms of channel width and channel height. The zirconium tritelluride ($ZrTe_3$) ribbons also come in very different sizes and shape. The ribbons sometimes have tapered (pointed) ends and sometimes grow as standard trapezoids.

Device design is crucial for our electrical characterizations. While the design is imperative, we recognize that the dimensions shift slightly due the previously discussed proximity effect and PMMA thickness differences. Therefore, once the devices are completely measured for the electrical properties, the PMMA cap is removed via acetone and then final device dimensions are acquired via scanning electron microscopy (SEM) and atomic force microscopy (AFM). SEM can give us lateral width dimensions of the metallized contacts and the spacing between them. AFM gives us very accurate device height dimensions. These dimensions allow us to perform cross-sectional area and volume parameters from which we can calculate resistivity and conductivity.

The next step in the EBL process is to align in the FIB/SEM system the developed crosshairs shown in the detector. The detector can see the conductivity change in the PMMA material versus the underlying “opened” SiO_2 material surface. From the labels in the matrix, we can locate our previously designated “zero-zero” center point from which the CAD drawn device is overlayed. This alignment step is also very critical because of the 1D nanowires

and nanoribbons provide a very small landing area. The room for error is approximately 50 – 100 nanometers therefore the alignment step must include even stage rotation to ensure the axis between the two crosshairs 50 um apart is as centered as possible. The smaller features such as the material contacts and "vias" leading away are written in a smaller 20 um aperture. The "pads" which are the probe contacts for our electrical measurements are then written in the larger 120 um aperture (this is because they are a much larger feature with less critical parameters and thus, using a 120-um aperture allows us to drastically cut down on write time). I perform another alignment step when switching the aperture because the aperture centers are not perfectly aligned so there is a beam shift required. Once all device alignment and writing is complete, we can develop in MIBK and IPA. Then a very quick check in the optical microscope to ensure proper alignment and development is performed before the sample is carefully taped to a metal disk which is placed into a metal e-beam evaporator. We choose to use yttrium metal as an adhesion layer because for the previous 2D materials, such as molybdenum disulfide, we found that it lowered the Schottky barrier and gave us better electrical measurement results. Since then, I have tested this with $TaSe_3$ wires and saw that yttrium, as opposed to titanium or scandium, also gave us better electrical results. Usually, we evaporate only about 5 nanometers of the yttrium for adhesion, and then depending on the predicted material thickness, we evaporate a ranging thickness of gold going anywhere from 70 nm to 350 nm. The thinner ranges are usually used for the

tantalum trisellenide wires, whereas the thicker ranges are usually used for the zirconium tritelluride ribbons. The metal is lifted off in an acetone wash. The samples soak in acetone for about 10 minutes sometimes less and gently rinsed off with acetone spray bottle followed by IPA and finally dried with nitrogen gas. To preserve the material properties (since they are incredibly thin and sensitive to atmosphere, they are then capped with another layer of PMMA. Some might use hexa-boron nitride as a capping layer; however, we have found PMMA to be a suitable and versatile capping layer because it covers the entire substrate rather than just a small sample area that can be covered by a single hBN flake. Also, to reach the pad probe area, we just rewrite the pad design in the EBL system and develop which opens the pads.

2.2 Substrate Patterning for Seeded CVD Growth

There are two main routes for patterning a substrate with the purposes of seeding 2D or 1D material growth: using UV optical photolithography or EBL. This, again, goes back to the aspect ratio and size limitations and or repeatability of patterning on wafer surfaces and I have used both which we will discuss further. Because 2D materials such as MoS_2 and WS_2 tend to grow out as films or islands of films, they can have a much larger aspect ratio “bracket” or “window” for the seeding patterns. For example, MoS_2 usually grows in a

triangular crystallite island with a span width of anywhere between 5 um – 20 um. As such, we can have a pattern consisting of circles with 1.5 – 2 um diameter which are spaced 7 – 10 um apart to seed the growth. The first experiment with seeding was first theorized when noticing that the 2D material preferentially grew around defects in the substrate surface (such as accidental scratch marks on the SiO_2 top layer). From this we decided to attempt creating artificial “defects” from patterning the substrate and then using the reactive ion etcher to etch away the exposed areas in the photoresist. Using optical lithography, samples with the circle pattern (as described earlier) where created both with positive resist, where the exposed circled were then etched down, and negative resist, where the circles were protected, and the remaining area of the sample was etched away (leaving raised miniature pillars). In both cases, MoS_2 preferentially “nucleated” at the center of the circles and grew outwards as seen in Fig 2.1. This was a repeatable behavior for the other 2D CVD grown materials, such as WS_2, as well. Another patterned design for seeding involves creating striped samples where the width between each stripe if 5 um – 7 um. The sample was then placed inside an atomic layer deposition tool where a thin hafnia oxide was deposited and the photoresist was subsequently stripped away, leaving alternating stripes of the native SiO_2 and ALD grown HfO_2. These substrates were used to CVD grow WSe_2 which preferentially grew thickly on the HfO_2 stripes and connected to the neighboring HfO_2 stripe (leaving a thin monolayer of material on the SiO_2 area). An electrical device was fabricated on the sample to measure the thick

contacts and mobility across the channel. This showed us that substrate encoded channel length and location by oxide deposition and patterning can be determined pre-CVD growth of TMDs and is a reliable method to create bulk-like contacts which allow for higher mobility and more ohmic contact behavior because of the reduced Schottky-barrier at a metal-3D TMD interface instead of at a metal-2D interface.

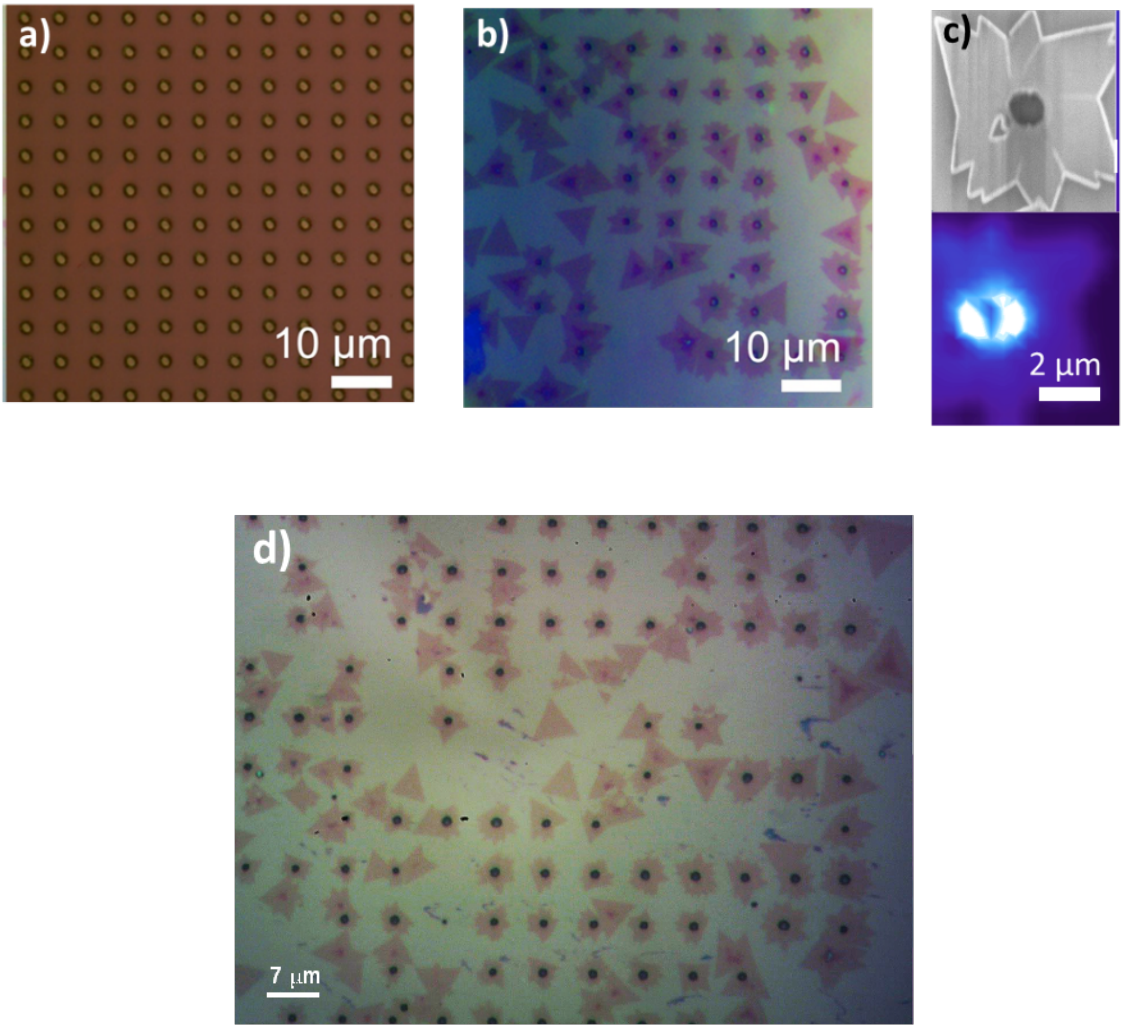


Figure 2.1: a) An optical image of a patterned and etched SiO_2 on Si wafer piece. Post CVD growth of MoS_2 islands over the etched patterned areas confirms seeding practice in b) and d). SEM and PL mapping of MoS_2 island over an etched area shows higher PL response indicative of strain over the etched hole.

As these were promising results for 2D TMD materials, we wanted to see if seeding patterning methods could be designed for 1D nanowire material as well. During initial testing, simply recreating the standard dot pattern (1.5 um diameter, 7 um pitch) did not work as intended shown in Fig 2.2.

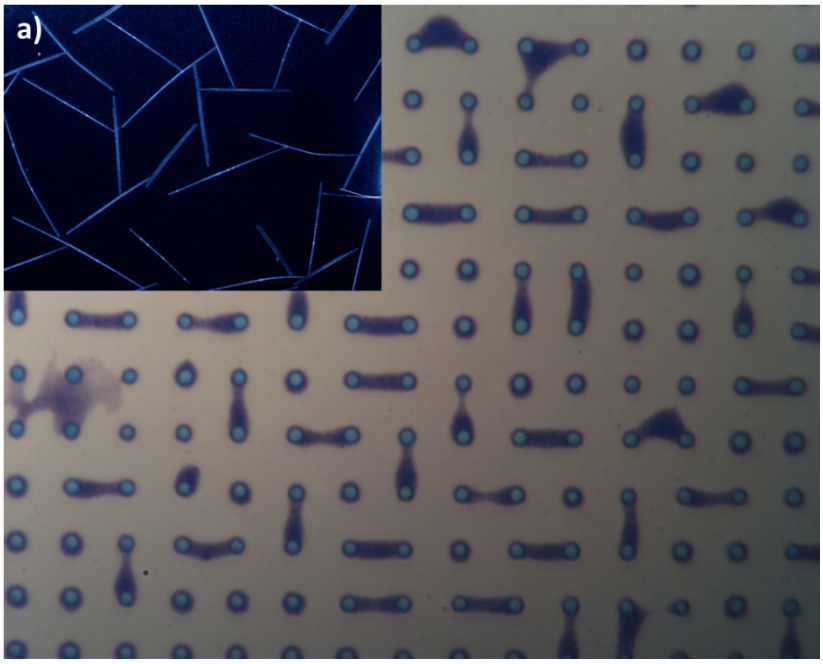


Figure 2.2 Optical image of patterned SiO_2 on Si wafer where the blue dots are 25 nm thick nickel metal dots and the film between appears as pre-growth of nanowires: The inset shows a colorized SEM image of $TaSe_3$ nanowire growth exhibiting preferential connectivity of the rods for future interconnect applications.

This was then understood as an issue of differing aspect ratios of the CVD grown material. Because 2D materials growth spans outwards as films, they can nucleate at patterned defects and continually grow outwards. Since the 1D nanowire materials have a much smaller aspect ratio (growing on average about 2 um long and 20 - 100 nm wide), we needed to use the EBL to write smaller patterns. The prototype pattern I finally concluded with was a series of 100 nm by 100 nm squares spaced 1 um apart to form hexagonal outlines (Fig 2.3a). We needed a pattern that has clearly defined “paths” in a repetitive but not crowded way. What I mean by crowded is, in example, the array of dots that form an

overall square. When the seeded growths occur there, we cannot determine with extreme certainty that the seeding actually promotes the growth in a specific path, or if during the growth process, a cluster just happened to grow in this area. This is because the dots are neighboring each other in an extremely repetitive manner and in close proximity to each other. However, having the waypoints form just a hexagonal outline allows us to determine if these points promote the directionality of nanowire growth rather than just having the growths there by being randomly scattered/clustered. This worked very well as shown in Fig. 2.3b,c and attempts proved sufficient to progress towards making devices on the interconnected nickel waypoints to collect electrical transport measurements across the nanowires and their junctions. Future applications include replacing copper on-chip interconnections with these much smaller nanowires that retain their resistivity across different cross-sectional areas.

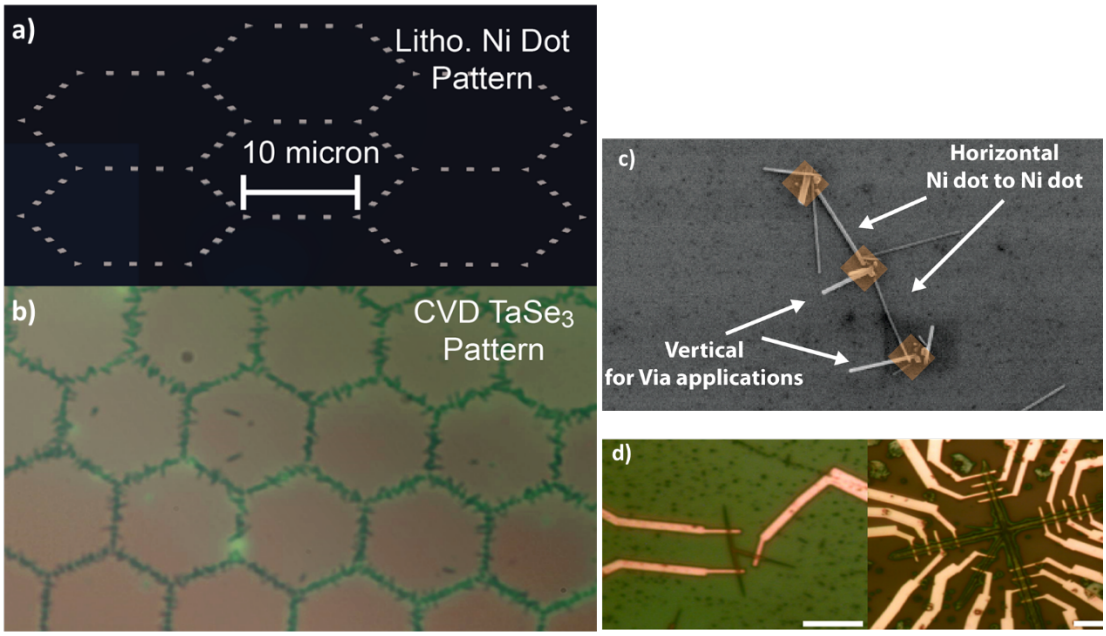


Figure 2.3: Figure a) shows the CAD drawing (not to scale) of prototype seeding pattern for nanowires and 1D material growth. The design consists of 100 nm x 100 nm squares arranged in a hexagonal outline pattern. Post-CVD growth of $TaSe_3$ shows great seeding affinity for the nickel square waypoints in the optical image in b). c) Closer SEM inspection of growth results shows nickel-to-nickel connection of $TaSe_3$ rods horizontally with some rods facing outwards from the sample (vertical). d) Two prototype devices on interconnected $TaSe_3$ wires for preliminary electrical transport measurements.

2.3 Electron-Beam Metal Evaporation

Electron beam evaporation, usually referred to simply as e-beam evaporation, is a deposition technique used for applying a uniform metallic layer onto your samples. The chamber consists of a rotary wafer holder at the top, target material in a crucible underneath, and an electron source below that. The chamber is loaded with a wafer facing downwards towards the deposition material targets. Once the chamber has been pumped down to below 4 x 10^{-6}

torr, the high voltage for the electron gun can be turned on. The gun emits electrons which are guided by an electromagnetic field towards the material target. When the electrons strike the target, they allow the target atoms to be removed from the target surface and approach the wafer surface. As the wafer holder rotates inside the chamber, the target material is thinly and uniformly coated over the entire wafer. A quartz crystal monitor inside the chamber allows us to control the deposition thickness and once optimal thickness is achieved, the shutter over the target is closed and the gun turned off. The chamber is vented with nitrogen gas and the wafer is ready for remaining processing techniques (such as lift off).

2.4 Plasma Enhanced Chemical Vapor Deposition

Plasma enhanced chemical vapor deposition (PECVD) is a deposition technique where the process gasses are ionized into plasma to enhance their chemical reactivities as they form a thin film from the vapor state into solid state on a sample surface. Some of the most common process gasses used include: SF_6, NH_3, SiH_4, N_2O, N_2, and a mixture of CF_4 and O_2. PECVD is most commonly used to deposit thin films of SiO_2, SiO_xN_y, SiN_x and amorphous silicon. I have also used the PECVD for rough SiO_2 etching using a high flow of SF_6 at high radio frequency (RF) power. Predictably, this causes a very high surface roughness.

2.5 Dry (Plasma) Etching

Reactive ion etching (RIE) is the most commonly used dry etching technique in cleanroom processing. The RIE tool is a chamber where, under low pressure conditions, chemically reactive gasses are made into plasma that interacts with wafer surfaces to remove specified material. The gasses enter the chamber through inlets at the top of the chamber and pass through an oscillating radio frequency electromagnetic field which removes electrons from the molecules, thereby ionizing them into plasma state. This plasma pool then travels downwards to interact with the wafer surface where it either chemically reacts with the surface to remove material or even knocks off surface material through transferring its kinetic energy (also called sputtering). Common gasses used in RIE are sulfur hexafluoride, carbon tetrafluoride, oxygen, chlorine, and trifluoromethane.

Altering critical etch parameters such as process gas, gas flow rate, chamber pressures and radio frequency (RF) power can influence etch results such as sidewall profile and surface roughness. In the inset of Fig. 2.4, we can see the top-down optical view of a 300 nm SiO_2 on silicon wafer piece which has been patterned using UV-photolithography. The white appearing circles are about 1 um in diameter and spaces 2.5 um apart and represent the areas covered with photoresist, whereas the blue background is the SiO_2 top layer. The first RIE etch process used CF_4 to target the SiO_2 layer and a second etch

chemistry using SF_6 was used for the deep etching creating an isotropic sidewall profile. The SEM image in Fig. 2.4 shows the resulting topography of these structures as seen from a 45-degree tilt angle.

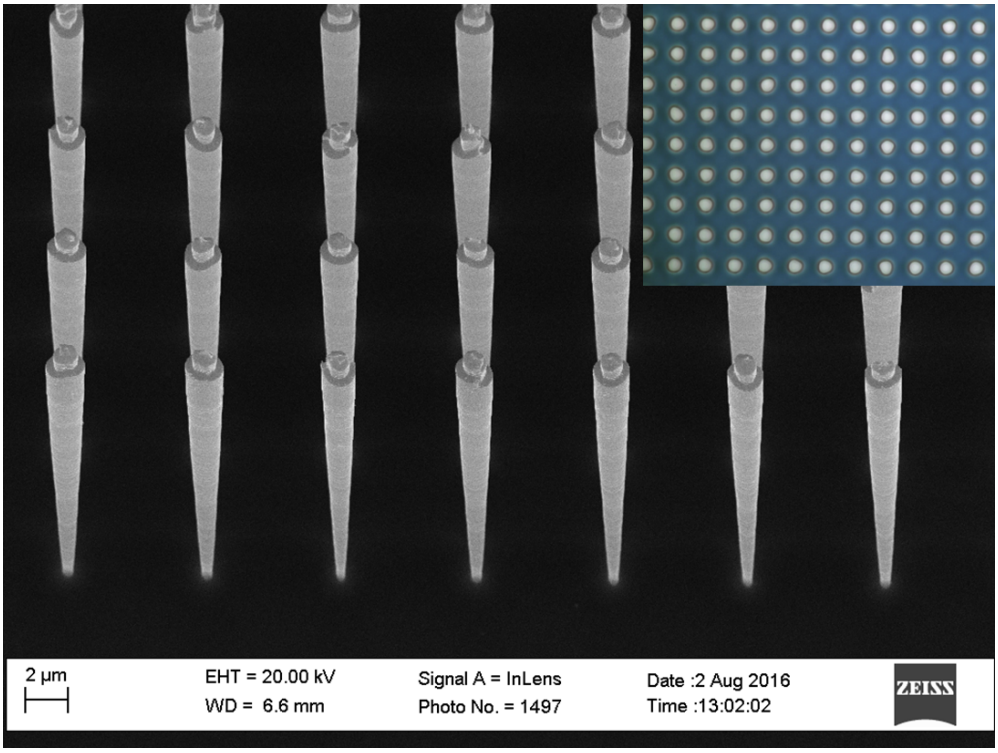


Figure 2.4: The inset in this figure optical image of a patterned SiO_2 on Si wafer piece where the white circles are the areas covered in photoresist and the blue behind is the 300 nm layer of SiO_2. The main figure is an SEM image where the stage was tilted at a 45-degree angle away from the gun and shows post-deep RIE processing.

Chapter 3: Material and Device Characterization

3.1 Raman and Photoluminescence (PL) Spectroscopy

Raman spectroscopy is instrumental in helping us identify which material has been produced during the CVD growth process and photoluminescence (PL) can confirm layer amount in the case of 2D materials because of their intrinsic nature of having a bandgap at the monolayer and not in bulk. Excitation of material from a laser can lead to inelastically scattered photons such as lower Stokes or higher anti-Stokes photons. In MoS2, the E^1_{2g} mode measures the in-plane vibrations from the Mo and S atoms while the A_{1g} mode measures the out-of-plane S vibrations, as depicted in Fig 3.1. Monolayer molybdenum disulfide must have Raman A_{1g} and E^1_{2g} peaks of less than $20cm^{-1}$ difference, usually found at $380cm^{-1}$ and $400cm^{-1}$, as can be seen in Fig 3.2b. Larger peak difference is indicative of a multilayered material.

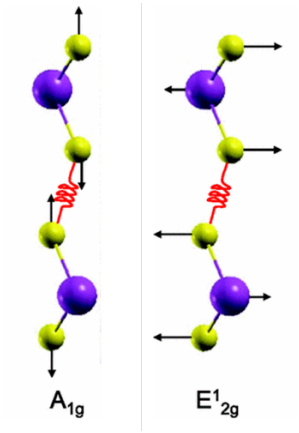


Figure 3.1: Drawing indicating the vibrational directional Raman modes in MoS_2. The E^1_{2g} mode measures the in-plane vibrations from the Mo and S atoms while the A_{1g} mode measures the out-of-plane S vibrations

Photoluminescence spectroscopy can also be used as an indicator of thickness of the material of TMD by measuring optical bandgaps. Bulk MoS_2 has an indirect transition of the bandgap at the K-point but as it is thinned down to the monolayer limit, a shift occurs where the bandgap at the K-point becomes direct allowing for strong photoemission. Monolayer MoS_2 has a PL peak between 1.80 and 1.85eV and the intensity is usually very high, unlike multilayered MoS_2 which would have intensity counts below 100. We can see the well-defined and very intense photoluminescence response of MoS_2 in Fig 3.2c.

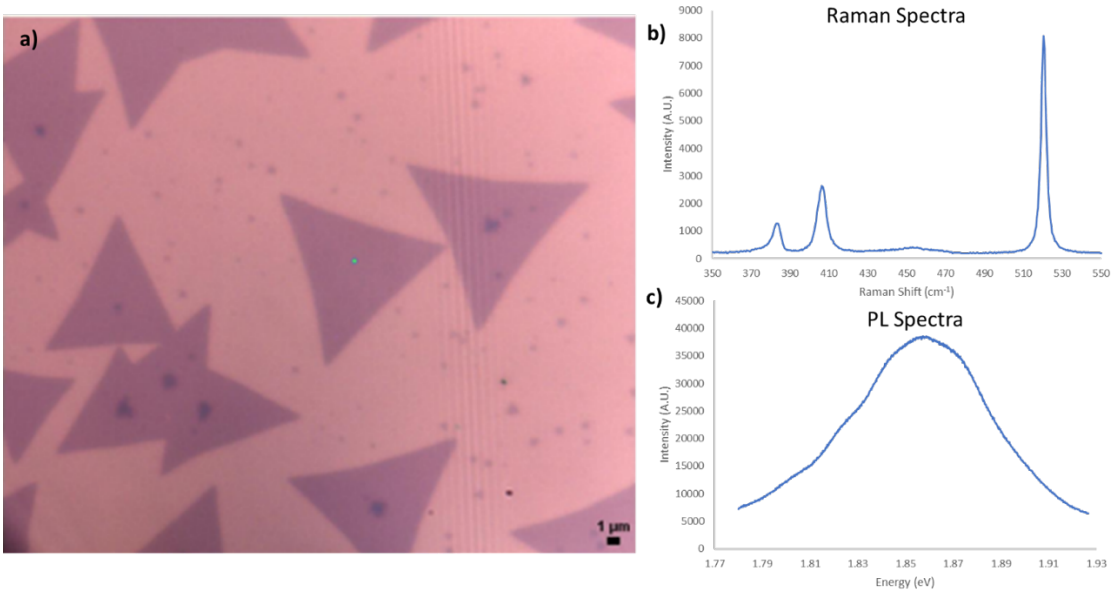


Figure 3.2: The optical image of a single monolayer MoS_2 triangular island shown in a) and its respective Raman and photoluminescence peaks in b) and c).

3.2 Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) is an imaging technique where a tungsten filament (in our SEM instrument at UCR) is used to source an electron beam that interacts with a sample surface in ultra-high vacuum conditions. Two main types of electrons are collected by the detector which updates an image on the computer screen. The two types are backscattered electrons (BSEs) and secondary electrons (SEs). The secondary electrons offer the most topographical information regarding sample surface and is most used to describe sample dimensions. Backscattered electrons can offer some information regarding atomic number and phase differences in the materials being investigated. As

such, we use the secondary electrons for measuring the space between electrodes (sample length) and width of sample. If the sample is thick enough (usually $ZrTe_3$), the stage can be tilted at a 60-degree angle and sample height/thickness can be calculated from those measurements. If the sample is thinner than 120 nm, we employ the use of another topographical mapping technique such as atomic force microscopy. As seen in Fig. 3.3, when viewing the optical image of the material (a), it's difficult to distinguish material structure and I thought it was a single nanowire. However, once using SEM for imaging, it becomes clear in Fig 3.3b-d that the crystal structure of this particular $TaSe_3$ sample was quite complex.

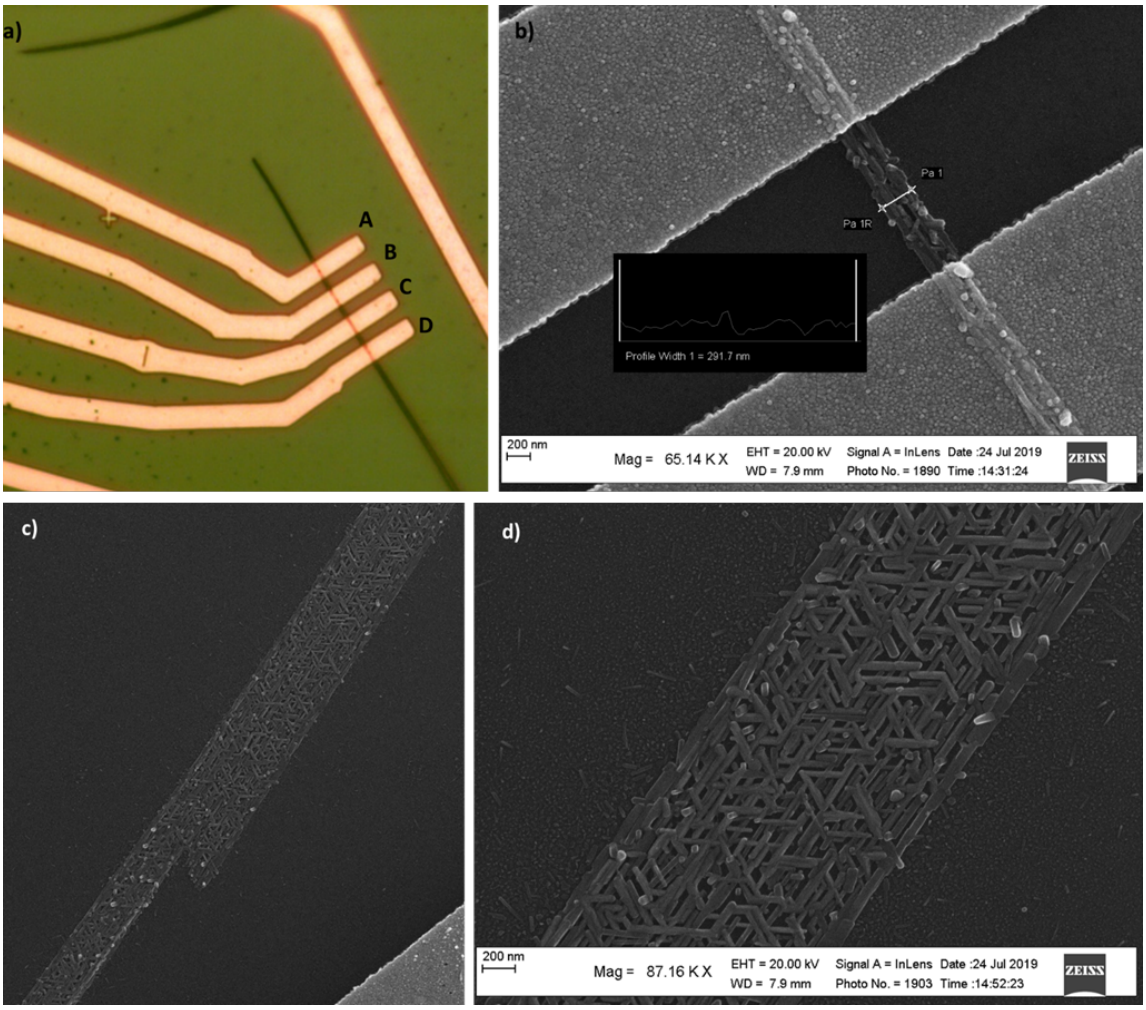


Figure 3.3: a) Optical image of a fabricated device on a thick $TaSe_3$ wire. SEM imaging from b-d) showing higher magnification of material structure. This shows that $TaSe_3$ material can grow interconnected and further electrical transport measurements confirms good conductivity.

3.3 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a technique where a tip is made to raster across a sample surface while performing a “tapping” motion. In some

methods, you can choose to have the tip physically tap the surface while in other methods, you may choose the tip to not actually physically tap the surface but hover above which is often referred to as the “air tap” method. This method is useful if you are concerned about damaging the sample you are imaging.

3.4 Ellipsometry

Ellipsometry is a characterization technique that can be used to measure the properties of dielectric materials such as film thickness/depth and composition. This is done by the ellipsometer which measures the change in the polarization of the light when it is reflected off from the sample surface. We use ellipsometry to measure the thickness and elemental composition of silicon dioxide and silicon nitride films deposited by PECVD.

3.5 Electrical Transport Measurements

The sample is now ready for our current voltage characterization measurements. The first step is to attach a gating wire. This helps us to verify later that the oxide layer remains intact and undamaged (no leaking of current through the oxide into the silicon material underneath). To attach the gating wire, we use a diamond scribe on a corner of the sample to scratch a small area towards the silicon material, then glue a thin insulated copper wire using silver

epoxy or silver adhesive paint. The sample is placed into our nitrogen enclosed glove box where the probe station is contained.

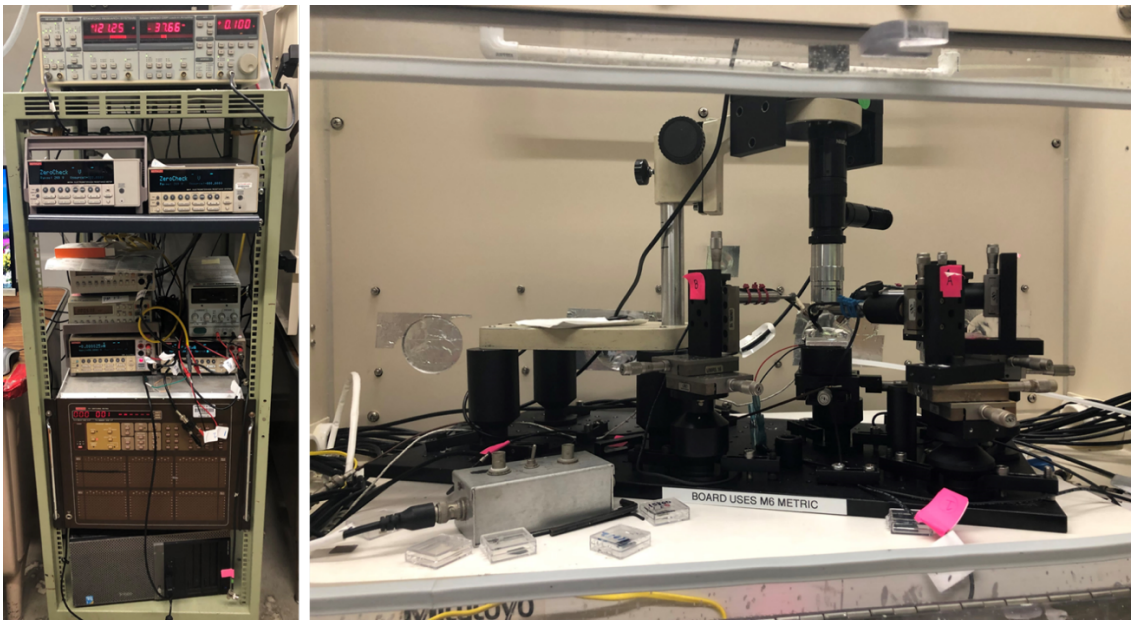


Figure 3.4: Image of electrical measurement set-up with nitrogen glove box containing contact probes (right) and all measurement tools including lock-in amplifier, Phillips's multimeters, electrometers, Keithley 2400 source meters, and switch matrix (left).

Here, the gating wire epoxy/paint cures for about 30 minutes. Once the gating wire is securely attached, we connect it to our switch matrix. The sample is placed onto a stage with vacuum to hold it securely in place. Then the camera above guides the landing of the probes which are also connected to the switch matrix. Probe landing is also guided by a lock-in amplifier which uses the sine wave input from the gating wire to give signal when the probe is just above and just touching the metal pads. Voltage is then slowly ramped to promote the electrodes contacting the material to "open up" or break through the small oxide

layer that inevitably forms during the material processing and device fabrication steps. Then we carefully proceed with ramping the voltage between channels and recording the current data we receive. This is done using Keithley 2400 source meters and electrometers to record the voltage seen by all other probes currently landed on the other electrodes.

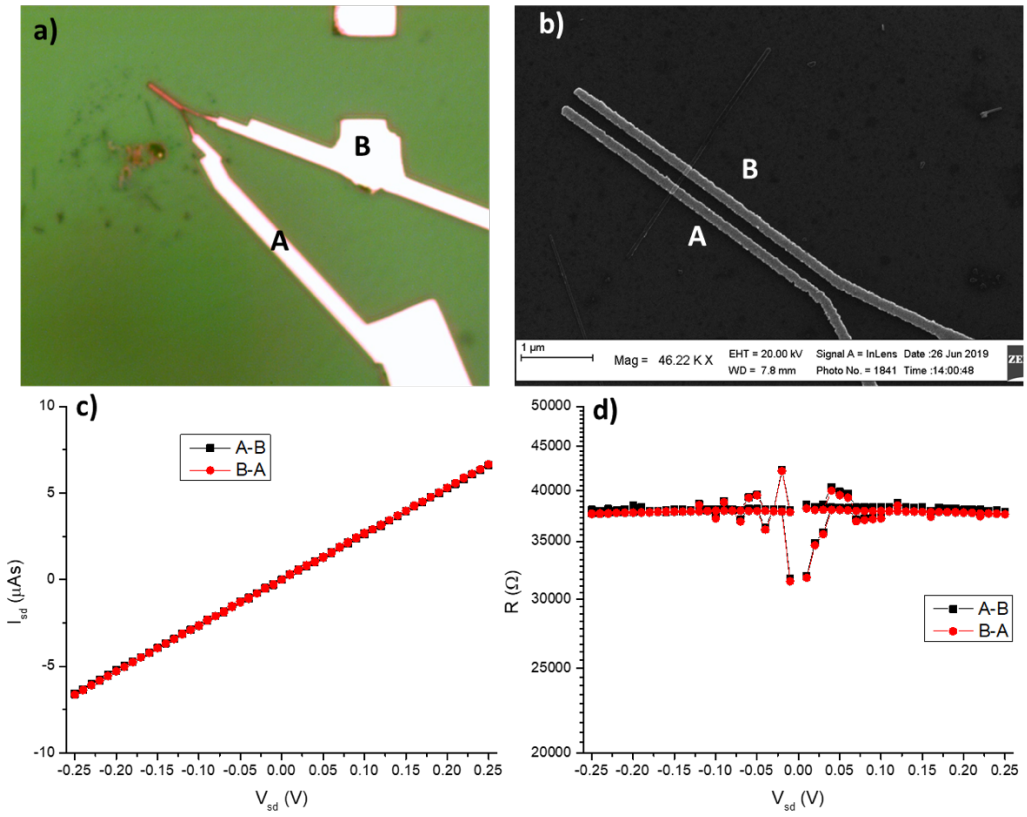
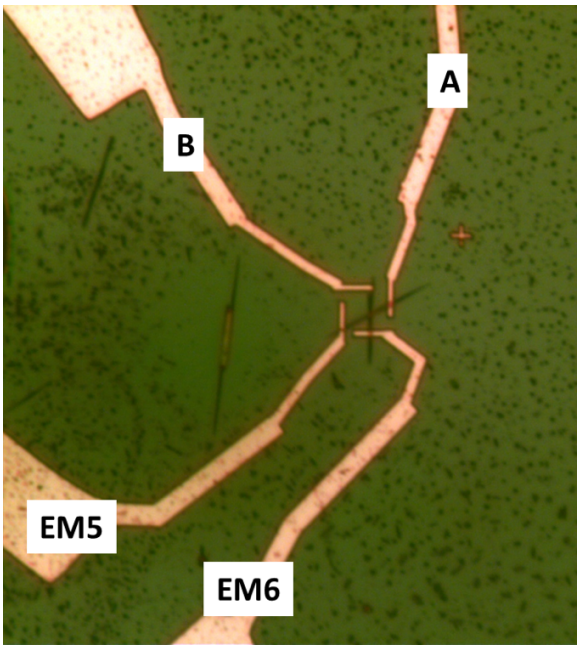
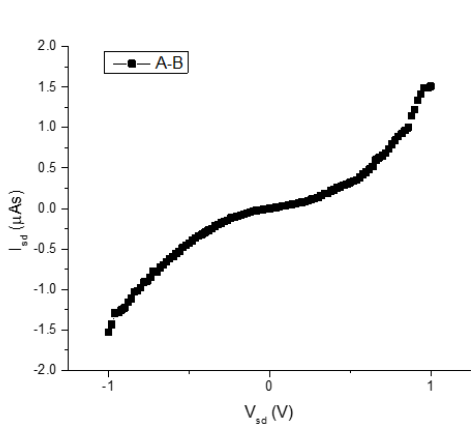
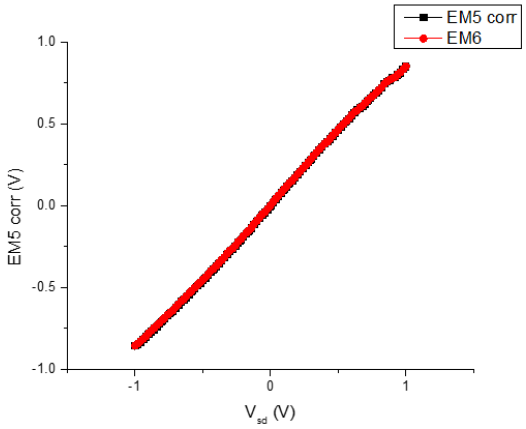


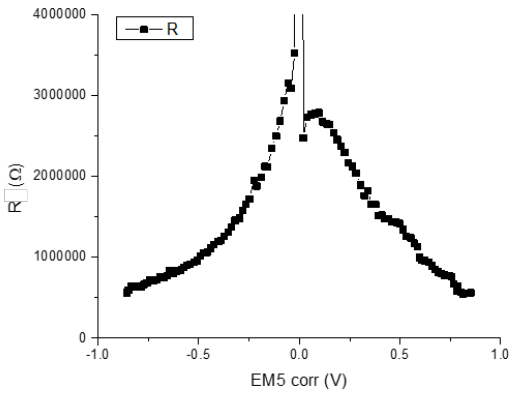
Figure 3.5: The optical and SEM images of a device on a $TaSe_3$ nanowire are shown in a) and b). In b) we can measure the width of the wire to be 40 nm and the length between the two contacts to be 160 nm. This device had 10 nm of cobalt and 70 nm of gold with the intent for future spin hall measurement applications. Figures c) and d) provide electrical response measurements where although the current-voltage curve (forwards and backwards) is extremely linear and reproducible, the resistivity is extremely high.

In addition to standard electrical transport measurements of a single nanowire growth, testing of interconnectivity between wire-to-wire was performed. As seen in this Fig. 3.5c-d, we have shown that transport from one wire to another is possible however the junction points of some of these interconnected devices created a resistance barrier which could be overcome by slowly ramping voltage to greater values. This can be due to similar reasons of oxide formation because of the processing steps during device fabrication and due to oxygen buildup in the PMMA which might interact with the 1D materials it is meant to cap as a barrier from atmosphere.


A
B
EM5
EM6


A-B
I_{sd} (μAs)
V_{sd} (V)


EM5 corr
EM6
EM5 corr (V)
V_{sd} (V)


R
R (Ω)
EM5 corr (V)

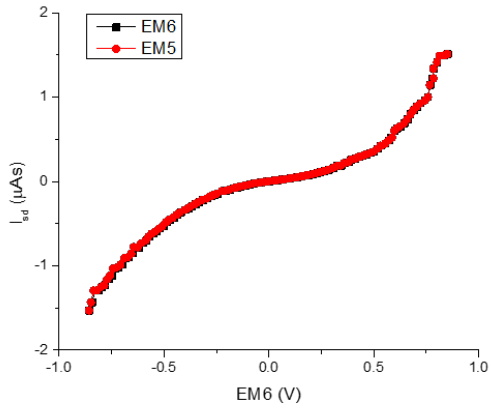

EM6
EM5
I_{sd} (μAs)
EM6 (V)

Figure 3.6: The top is an optical image of a completed interconnected $TaSe_3$ device. Two nanowires have grown together, and the device contacts the ends of each wire using 5 nm of yttrium for adhesion and 70 nm of gold. Shown below are the electrical transport measurements specifically for device setup of voltage applied from contact A to B with the two electrometers reading voltage on the opposite ends.

The interconnected device shows a non-metallic current-voltage response (Fig. 3.6) which could be in part due to the junction between the two wires or, more likely some contamination during the CVD growth process. We have more recently seen some indications of iron contamination in the $TaSe_3$ nanowires by using energy dispersive x-ray analysis (EDX/EDS). This iron contamination might come from the stainless-steel clamps used to seal the quartz tube during CVD growth or from the spatulas used for measuring and mixing precursors pre-growth. Regardless, more testing of interconnected 1D nanowires must be performed before we can make final conclusions.

Chapter 4: Facile Growth of Monolayer MoS_2 Film Areas on SiO_2

The following is taken from an article published in The European Physical Journal B[43] in collaboration between myself, and other students: John Mann, Dezheng Sun, Quan Ma, Jen-Ru Chen, Edwin Preciado, Taisuke Ohta, Bogdan Diaconescu, Koichi Yamaguchi, Tai Tran, KatieMarie Magnone, of Ludwig Bartels, Tony F. Heinz, Gary L. Kellogg, and Roland Kawakami. It has been edited in a form appropriate for the dissertation.

Abstract

Areas of Single-layer MoS_2 film can be prepared in a tube furnace without the need for temperature control. The films were characterized by means of Raman spectroscopy, photoluminescence, low energy electron diffraction and microscopy, and x-ray photoelectron spectroscopy and mapping. Transport measurements show *n*-doped material with a mobility of 0.26 $cm^2 V^{-1} s^{-1}$.

Introduction

Molybdenum disulfide, MoS_2, has attracted widespread attention as a material that can be prepared in a stable form down to the single-layer limit. As

a monolayer, the material becomes a direct-gap semiconductor with a gap of 1.8 eV [1, 2]. Single-layer MoS_2 transistors have been reported with mobilities on the order of 1 $cm^2 V^{-1} s^{-1}$ and beyond [3-6], as well as on-off ratios up to 10^8 at room temperature. Bulk MoS_2 and most mono- or few layer MoS_2 materials examined to date exhibit *n*-doped behavior [3-9], but *p*-doped behavior has also been reported [17]; the use of gating with an ionic liquid has permitted access to ambipolar operation [44]. Phototransistors made of single-layer MoS_2 show reasonable switching behavior (~50 ms) and stable performance [8]. More recently, MoS_2 has also been shown as a candidate for valleytronics devices, and dynamic valley polarization has been achieved by excitation with circularly-polarized light [10-14].

Apart from mechanical exfoliation [15], MoS_2 monolayers can be fabricated by chemical vapor deposition (CVD) based growth on Cu [16], Au [17-20], SiO_2 [17, 21], and various other insulators [6, 17, 22]. In addition to MoS_2 film areas, several other forms of MoS_x have been reported, including MoS nanowires [45, 46] and Mo_2S_3 films [47, 48]. Here we show that the preparation of MoS_2 can be achieved in a very facile manner. Prior MoS_2 growth started from thin Mo layers [17] prepared by physical vapor deposition (PVD) or dip-coating of a substrate in a Mo-containing solution [6] followed by sulfurization. Another promising approach involves the simultaneous deposition of molybdenum (typically from a MoO_3 source) and elemental sulfur [21]. In this manuscript, we follow the latter method and show that the fabrication of continuous films

hundreds of microns across can be achieved with minimal control of the growth conditions.

Our films are found to be uniform in their spectroscopic properties and feature large areas that are of monolayer thickness. In this manuscript we provide photoluminescence (PL), Raman spectroscopy, low energy electron diffraction (LEED) and microscopy (LEEM), x-ray photoelectron spectroscopy (XPS), Atomic Force Microscopy (AFM) imaging and transport measurements to validate the quality of our films.

Results and Discussion

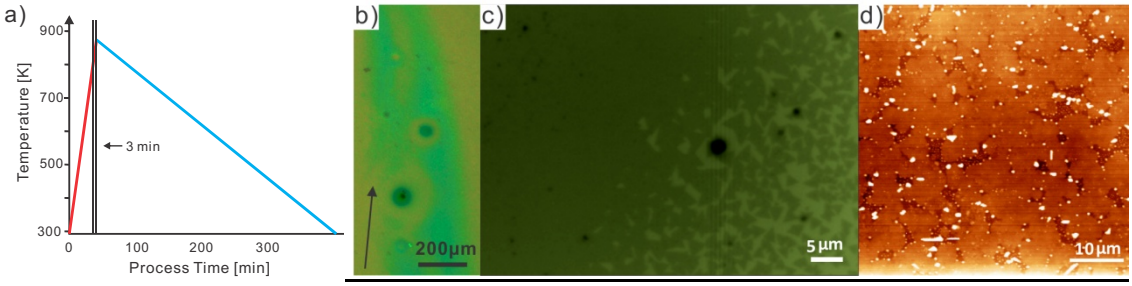


Figure 4.1: a) Approximate temperature transient during MoS_2 growth. The furnace is powered until 3 minutes after the sulfur is molten and subsequently switched off. b) Optical microscope image taken with neutral color balance filter of the MoS_2 film (light green) on the substrate. The N_2 flow direction is indicated by an arrow. The circle feature is an area of multilayer MoS_2. c) At its edge, the MoS_2 film (dark area) transitions into an array of individual MoS_2 islands of mostly triangular form. d) AFM imaging shows the continuous film to have a small number of irregularly shaped pits, however no domain boundaries were found/resolved.

Our growth process for MoS_2 monolayers is based on the solid-source scheme of Lee *et al*. [21]. We use two alumina crucibles (Aldrich Z561738, 70 mm × 14 mm × 10 mm) containing MoO_3 (Aldrich 99.5%) and sulfur (Alfa 99.5%) powders as our Mo and S sources, respectively. These sources are placed in a quartz process tube (2" diameter), which is inserted in a furnace (Mellen TT12), only the center zone of which is powered. A rapid flow of nitrogen gas (99.999%) is used to purge the tube (5.0 SCFH), with subsequent film growth occurring at a reduced nitrogen flow rate (0.5 SCFH). The MoO_3–containing crucible is placed at the center of the heated zone with the substrate resting directly on the crucible across its middle, and the sulfur-containing crucible is placed upstream, outside the zone of the tube furnace that was heated. Our substrate is a 3×3 cm piece of a boron-doped Si(110) wafer covered by a 300-nm thick layer of oxide (SUMCO). The substrate is cleaned immediately prior to growth by a piranha etch solution, formed as a mixture of 3 parts sulfuric acid and 1 part hydrogen peroxide (30%). We also applied an O_2 plasma etch to some substrates, and found similar results to those for the unprocessed substrates. The MoO_3 crucible is located at the center of the heated section of the process tube. We optimized the position of the sulfur crucible so that during heat-up the sulfur melts and forms a flat, uniform liquid surface at the time that the center section of the process tubes (where the MoO_3 crucible is located) reaches ~880K (as measured by a type-K thermocouple at the outer surface of the process tube). We find that the duration that the substrate is exposed to vapor from the liquid sulfur is crucial in

determining the structures that we grow. We achieved the growth described in this manuscript by waiting and continuing to power the center section of the furnace for 3 minutes after the sulfur melts. Subsequently, all power to the furnace is switched off and it is left to cool undisturbed, while continuing the N_2 flow. Thus, no temperature control of the furnace is required. Fig. 4.1a shows the temperature transient.

After deposition, the substrates display elongated areas hundreds of microns long and ≈100 microns across (fig. 4.1b) that are continuously covered by a MoS_2 film. The long axes of these areas are aligned with the nitrogen flow during growth. In the following, we show spectroscopic evidence that identifies these areas as single layer MoS_2. At their edges, these areas are surrounded by isolated islands, mostly triangular in shape (fig. 4.1c), which exhibit spectroscopic and topographic characteristics identical to the film (*vide infra*). In contrast, other regions of the substrate are covered by triangular multilayer MoS_2 islands or show no deposited material at all. We also find thicker MoS_2 films predominantly surrounding areas with substrate point defects, such as the dark circles in Fig. 4.1b,c.

AFM shows that the film is interrupted by a small number of isolated irregular pits. No dislocation lines or 2D grain boundaries are resolved by AFM.

LEED on the film shows a hexagonal pattern commensurate with the lattice vectors of MoS_2. The orientation of the LEED pattern varies across the

film. Dark-field LEEM imaging [49] was used to collect electrons from the (01) LEED spot at different rotational angles. Fig. 4.2a,b) shows two such images obtained for ~10° rotation (our azimuthal acceptance angle was about ± 5° each time). Areas of the film appear at different brightness depending on whether one of their MoS_2's (01) LEED spots is angularly aligned with the diffraction aperture position. This provides direct evidence of the domain crystallinity, orientation, and size. Most domains are 3-5 microns across.

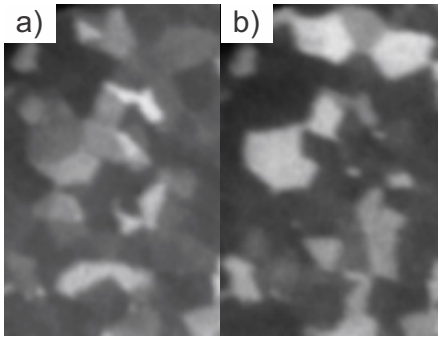


Figure 4.2: a,b) spatial distribution of intensity from the MoS_2 (01) diffraction spot at two angular orientations ~10° apart. MoS_2 monolayer domains appear at different brightness depending on their angular alignment with our LEED acceptance angle. Image size: 18×28 microns^2.

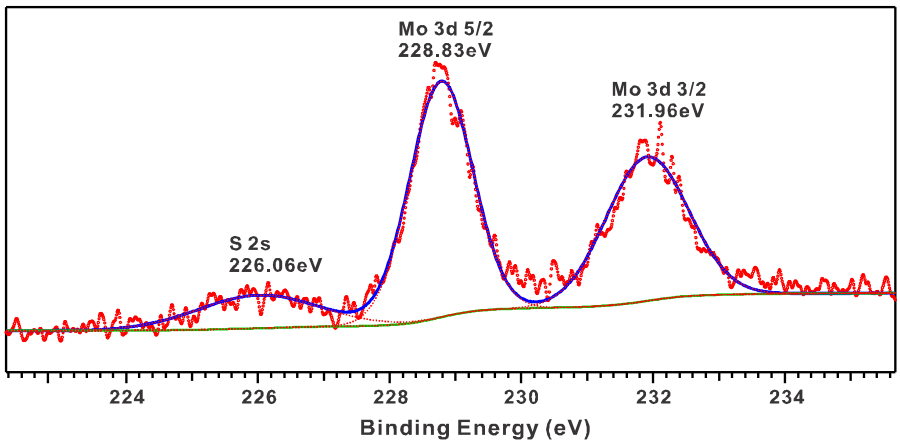


Figure 4.3 1 XPS of the Mo 3d and S 2s peaks from the MoS2 films on a SiO2/Si substrate.

Figure 4.3: XPS of the Mo 3d and S 2s peaks from the MoS_2 films on a SiO_2/Si substrate.

Selected area XPS measurements of the film using a Mg K-α source and a VG Scienta R3000 analyzer (Fig. 4.3) show the sulfur 2s and molybdenum 3d 5/2 and 3/2 peaks at 226.1, 228.8, and 232.0 eV, respectively. These core-level binding energies suggest the charge states of S^{2-} and Mo^{4+}. Referencing the spectrum to the silicon peaks of the substrate, we find peak positions in good agreement to those previously reported for bulk MoS_2 [50]. Although some areas of the sample exhibited peaks/shoulders corresponding to a higher oxidation state of molybdenum (Mo^{6+}, indicative of MoO_3) as shown in [17], these features were absent in the region of the continuous film area and the monolayer islands. These measurements confirm that the films we produce are comprised of pure MoS_2.

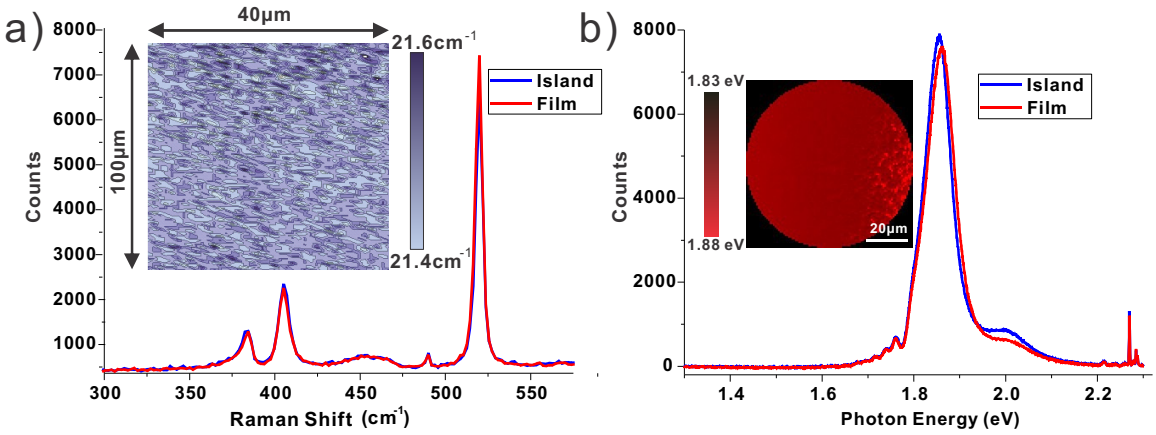


Figure 4.4: a) Raman spectra of the continuous MoS_2 film and region with island structures. Two characteristic peaks are located at Raman shifts of 384.3 and 405.2 cm^{-1}, corresponding respectively to the MoS_2 E^1_{2g} and A_{1g} vibrational modes. The inset shows mapping of the frequency difference between the E^1_{2g} and A_{1g} modes, which is determined by the layer thickness. The variation of ≤ 0.2 cm^{-1} is indicative of the high uniformity of the film. b) PL spectra of the MoS_2 film for both continuous film and nearby individual island structures exhibit the same single peak at 1.87 eV. The inset shows mapping data from a continuous film (left) to an area covered partly by islands (right).

For Raman spectroscopy (Fig. 4.4a), we used a 532-nm cw laser with a power of 0.1 mW in a spot size of ≈1 micron. The spectrum shows the E_{2g} and A_{1g} peaks of MoS_2 at 384 and 405 cm^{-1} and the silicon substrate peak at 520 cm^{-1}. The separation of the E_{2g} and A_{1g} peaks can be used to identify the MoS_2 film thickness. We find a value of 21.5 cm^{-1}, which is in good agreement with prior measurements on CVD-grown MoS_2 [6, 17, 21, 51] and lies between the values observed for monolayers and bilayers of exfoliated MoS_2 [52]. The Raman peak position and separation is uniform across our film areas. Mapping the sample in a 1 micron grid, we observe variations ≤0.3 cm^{-1} over an area >100 microns across

(inset in Fig. 4.4a); the islands at the edge of the film area show a Raman signal identical to the center of the film.

PL measurements (Fig. 4.4b) were performed with the same laser excitation source and conditions as for Raman spectroscopy. We find a single emission peak at a photon energy of 1.87 eV. This peak corresponds to the direct-gap transition of monolayer MoS_2 [1, 2]. The photoluminescence yield was about twice as high as what we find for MoS_2 monolayers exfoliated on SiO_2. The continuous film and the area consisting of individual islands show the same photoluminescence characteristics.

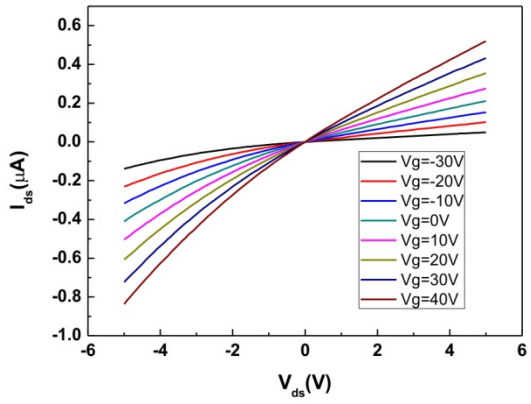


Figure 4.5: Current-Voltage (I-V) measurements in a 4-probe setup across a 2 micron gap at the edge of our monolayer MoS_2 film as a function of gate voltage, (V_g). The conductivity increases with positive gate voltages, indicating *n*-type material.

We measured the I-V characteristics (Fig. 4.5) in a 4-point probe setup across a two-micron gap as a function of a gate voltage applied to the silicon

substrate. The results reveal an *n*-doped material, as is typically found for both exfoliated and deposited MoS_2 films [3-8, 53]. We speculate that this behavior is caused by sulfur vacancies in the film and that further optimization of the growth process can reduce their number. Application of gate voltages up to -100 V (for a nominal oxide thickness of 300 nm) was insufficient to render the device ambipolar. We measured a room-temperature mobility of 0.26 $cm^2 V^{-1} s^{-1}$, comparable to results of many previous measurements of similar MoS_2 samples [3-6].

Summary

In summary, we have shown the possibility of growing large-area MoS_2 films using a simple solid-source deposition scheme, without the need for temperature control. The resultant films show monolayer behavior and excellent uniformity in their photoluminescence and Raman signals. Future research will address the chemical and catalytic properties of these films.

Chapter 5: High-Vacuum Particulate-Free Deposition of Wafer-Scale Mono-, Bi- and Trilayer Molybdenum Disulfide with Superior Transport Properties

The following is taken from an article published in ACS Applied Materials & Interfaces[54] in collaboration between myself and other students: Kortney Almeida, Adane Geremew, Koichi Yamaguchi, Thomas A. Empante, Michael D. Valentin, Michael Gomez, Adam J. Berges, Gordon Stecklein, Sergey Rumyantsev, and Joseph Martinez of Ludwig Bartels and Alexander Balandin. It has been rewritten in a form appropriate for the dissertation.

Abstract

Wafer-scale MoS_2 growth at arbitrary integer layer number is demonstrated by a technique based on the decomposition of carbon disulfide on a hot molybdenum filament, which yields volatile MoS_x precursors that precipitate onto a heated wafer substrate. Colorimetric control of the growth process allows precise targeting of any integer layer number. The method is inherently free of particulate contamination, uses inexpensive reactants without the pyrophoricity common to metal-organic precursors and does not rely on particular gas-flow profiles. Raman and photoluminescence mapping, as well as imaging by electron

microscopy, confirm the layer homogeneity and crystalline quality of the resultant material. Electrical characterization revealed microampere output current, outstanding device-to-device consistency, and exceptionally low noise level unparalleled even by exfoliated material, while other transport properties are obscured by high-resistance contacts typical to MoS_2 devices.

Introduction

Mono- and few layer transition metal dichalcogenide (TMD) films, particularly MoS_2 and WSe_2, are promising candidate materials in the continuing miniaturization of semiconductor devices. They combine robust well-defined semiconducting behavior with appreciable processing stability.[23-25] Indeed, it has been shown that at the monolayer limit they offer unparalleled on-off ratio,[26] sub-thermionic tunnel field effect transistor (FET) performance,[55] and unique electronic and optical properties.[27-30] The wide band gap of few-layer MoS_2 makes it promising for high-temperature applications.[56] It has also been demonstrated that MoS_2 is a versatile sensor material.[57, 58] While semiconductor devices conventionally utilize the substrate semiconducting material as the transistor channel, introduction of vertical cell access transistors called for by the ITRS roadmap in 2019 requires the deposition of high-quality channel material after initial patterning steps. Here, two dimensional (2D) van der

Waals (vdW) materials offer the advantage of very shallow channels at reduced surface scattering. Previous methods to produce wafer-scale monolayer TMD films have included tube-furnace chemical vapor deposition (CVD),[43, 59-64] liquid-phase exfoliation,[65-67] and metal-organic CVD or atomic layer deposition.[68-75] These techniques utilize chloride, sulfide, or oxide-based transition metal precursor powders or high-vapor-pressure carbonyls/metal-organic compounds. An ideal deposition method produces high quality homogenous films at arbitrary integer layer number and wafer scale coverage without the use of any powder or pyrophoric precursor to avoid particulate contamination and processing hazards. Here we show the growth of wafer-scale continuous MoS_2 films by a process that fulfills all of these requirements and yields a material superior in current noise characteristics to exfoliated and CVD films.

Our process departs significantly from prior work by the use of a set of metallic molybdenum filament wires (Alfa Aesar) as the molybdenum source. Fig. 5.1a shows a schematic of our growth setup. The method utilizes the difference in volatility between molybdenum metal (melting point: 2623 °C) and MoS_2 (melting point: 1,185 °C) as well as other MoS_x species; this ensures that exclusively MoS_x species are released from the filaments. Consequently, the material deposited onto the substrate is already of the correct elemental composition and sufficient surface-mobile to arrange itself into large grains and, ultimately, a continuous film. A background of carbon disulfide gas at a pressure

of 6×10^{-4} Torr (compared to a base pressure of the reactor of 1×10^{-7} Torr) is used as a sulfur source for formation of MoS_x species on the filaments and to assure stoichiometry in the resultant film. At a process time of up to 60 min depending on layer number, a continuous and homogeneous single-layer film of MoS_2 is deposited at wafer scale (Fig. 1b).

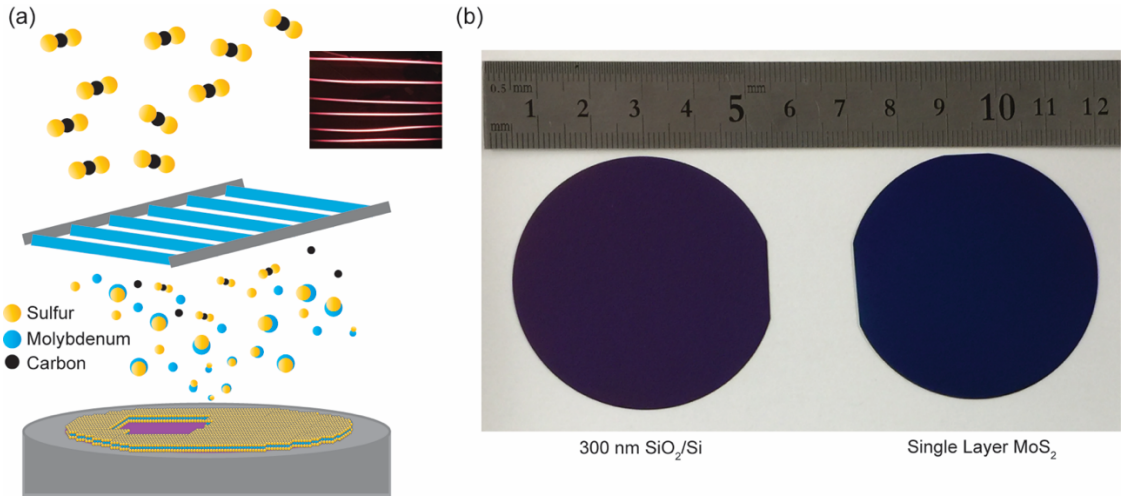


Figure 5.1: (a) Schematic of the high vacuum growth process utilizing a set of directly-heated molybdenum filaments and carbon disulfide as chalcogen source. Volatile MoS_x precursors are formed at the filament and precipitate onto the heated substrate coalescing into a continuous and crystalline film. Inset: photograph of heated filaments; (b) photograph of substrates before and after single-layer MoS_2 growth.

A number of prior studies[76-78] have addressed the CVD growth of MoS_2 single layers and found a sequence of nucleation and in-plane aggregation. Fig. 5.3a illustrates how we control the film growth: light from the hot molybdenum filaments (inset in Fig. 5.1a) is reflected from the wafer substrate during growth. As CS_2 molecules decompose at the molybdenum filaments, MoS_x precursors evolve, evaporate from the rods, and deposit onto the substrate where they

obtain stoichiometric sulfur contents from the environmental CS_2 and form into extended islands - or evaporate again, given the high platen temperature of 650 °C. In a balance between incoming MoS_x species and evaporation of material, the film ripens into larger and larger crystalline islands. The growth rate is highest when a sizable number of large grains have formed that are stable from evaporation and offer edge sites for growth; it is lowest whenever a layer is complete.

In this work we employ concomitant measurement of the hue of the specular-reflected Mo-filament light from the substrate for process control. This approach is novel for process control, but the dependence of the substrate color on single- and few-layer films has been well understood. Blake and Hill described the contrast and color-dependence of graphene on different thickness SiO_2 layers on Si using a multiple internal reflection method [79]. This description has since been expanded, for instance by Zhang et al., [80] to reveal wavelength/color dependent amplification in MoS_2 imaging and spectroscopy.

Results and Discussion

Fig. 5.3 shows the hue value of the light from the molybdenum filament reflected on the substrate as the film is growing layer-by-layer. The hue value is obtained by pointing a video camera from above and through the gaps of the

glowing molybdenum rods at the sample during growth. Translation of the camera's red-green-blue (RGB) encoded signal into the common hue-saturation-brightness (HSB) format yields the hue value which cycles through the color circle from 0 to 255. The inset in Fig. 5.3a shows the camera view on the filament in the bottom and its reflection from the substrate in the top. Numeric color temperature correction based on the albedo of the filament (bottom) has the power of removing dependence of the hue signal of the reflection (top) from the filament temperature but is not commonly required for growth.

The main graph of Fig. 5.3 shows the evolution of the hue value during growth. Initially the growth is slow due to the absence of growth nuclei and rapid re-evaporation of the material into vacuum. As the growth proceeds, more stable island perimeter becomes available and it speeds up, just to get slower again, when the first layer is about to complete and the available island perimeter to attach to becomes smaller. This is visible as the first inflection on the hue curve. A growth stopped at this point shows single layer Raman signal, as shown in the inset on the right.

If the growth process is continued at unchanged filament temperature, substrate temperature and CS_2 gas concentration, then a second layer nucleates, increases in size, speeds up in growth, and the growth decelerates again once it nears completion. Stopping the growth at this point, a bilayer film is

produced with the corresponding Raman signal (inset). If the film growth is continued, the trilayer color (inset) is reached and ultimately a thick film emerges.

In order to achieve the highest quality films, the actual growth process proceeds not at constant filament brightness as used in the experiment of Fig. 5.3. Rather as each layer nears completion, the filament temperature is reduced gradually to slow down growth and allow optimal ripening/arrangement of the inter-island/domain boundaries as well as evaporation of any adlayer islands that may have formed during the growth process. Fig. 5.2 shows a scanning transmission electron microscopy image that corroborates attachment between adjacent grain boundaries, which is important for film utility. If another layer is desired, the filament temperature is increased again to speed up film growth and reduced again toward the completion of the next layer.

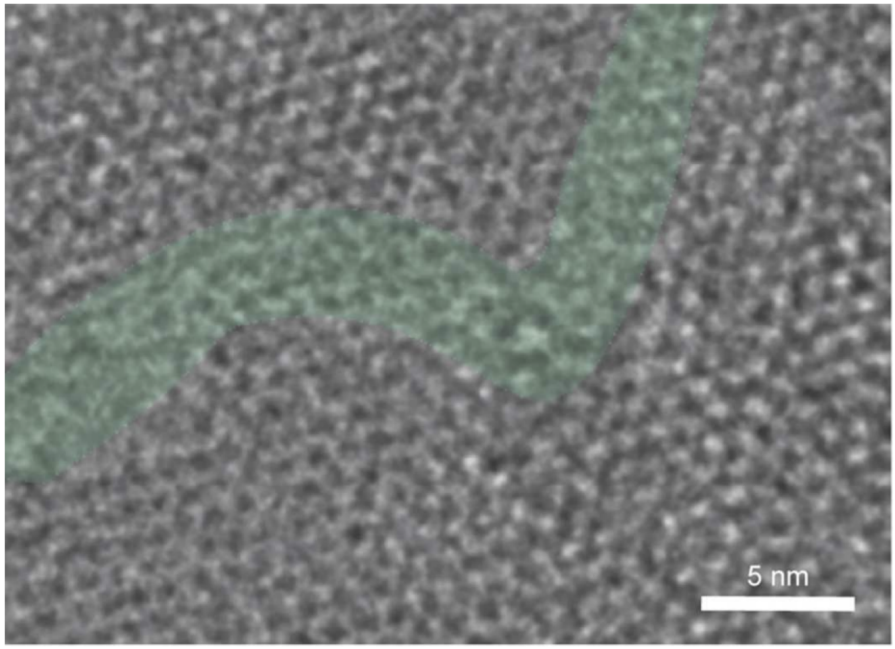


Figure 5.2: STEM image of the MoS2; the green outlines the dislocation in the lattice. Continuous film growth across the dislocation line is visible.

The Raman spectra in the inset of Fig. 5.3 show the E^1_{2g} in-plane and A_{1g} out-of-plane peaks for different layer thicknesses. The peak separations are 19 (1L), 22 (2L), 23 (3L), and 25 (bulk) cm^{-1}. The separations match well the literature values for mono-, bi-, trilayer and bulk MoS_2 respectively.[27, 28]

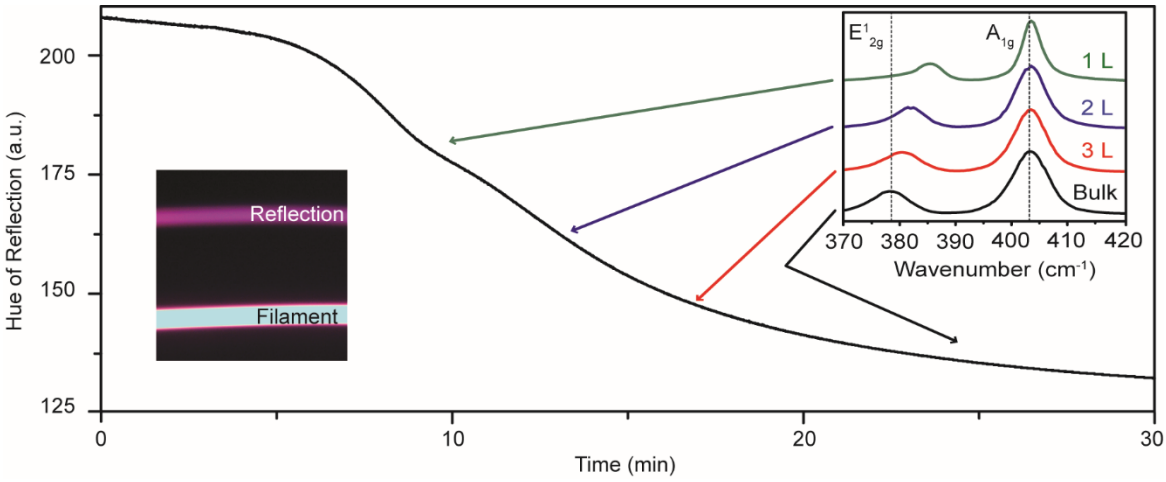


Figure 5.3: Hue (0-255) of the Mo-rod reflection (top in left inset) during film deposition. The hue-curve reveals the completion of layers, for which Raman spectra are shown in the right inset.

Mapping of the Raman E^1_{2g} and A_{1g} peak separation confirms the homogeneity of the material. Fig. 5.4a-c show millimeter-scale maps of the peak separation; at each layer thickness the variation is well below one wavenumber. The isolated white and black dots are caused by dust deposited onto the sample during Raman mapping in ambient unfiltered air and are not a consequence of the growth process. In order to ascertain the homogeneity of the film over a large range, we took Raman spectra at 840 micron separation across a wafer refocusing the beam at each location. Fig. 5.4d shows the results and affirm the large range homogeneity of the wafer beyond the millimeter-scale map areas of Fig. 5.4a-c.

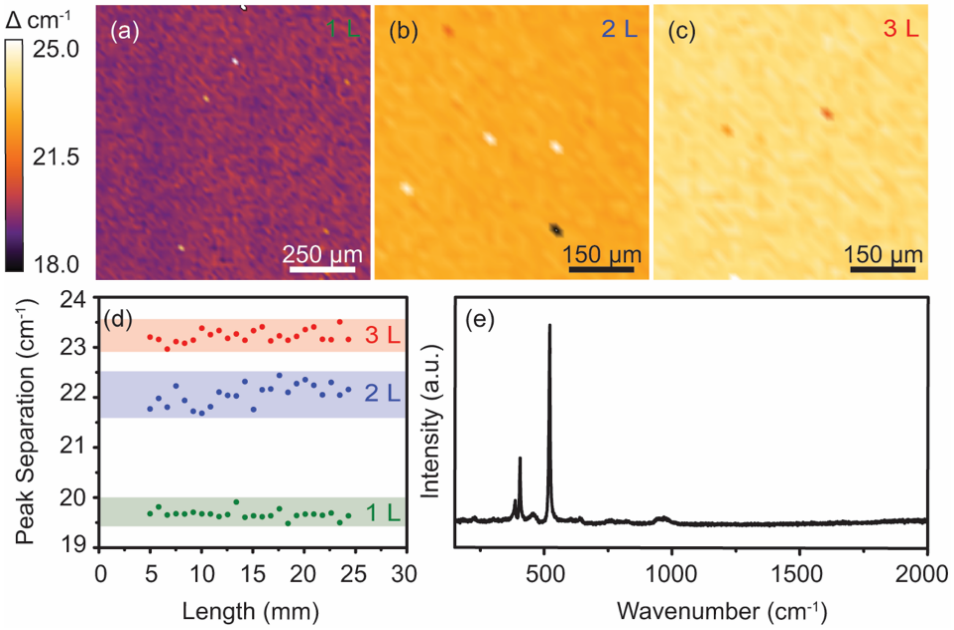


Figure 5.4: (a-c) Spatial mapping of the separation of the in-plane (E^1_{2g}) and out-of-plane (A_{1g}) modes of single-, bi-, and trilayer films, respectively. The values of 19.5, 22, and 23 cm^{-1} are tell-tale of the respective film thickness. (d) Trace of the Raman peak separation in steps of 840 μm across one inch of a wafer substrate. (e) Extended range of the Raman spectrum for single layer MoS_2 film.

Despite the use of carbon disulfide as a precursor, we find no Raman signature of a carbon film (Fig. 5.4e). The presence of strong photoluminescence (as strong as on exfoliated samples) is a further indicator of the absence of a carbon film. XPS measurements of the substrate before and after transfer of an MoS_2 film show no significant difference of carbon trace contamination.

The photoluminescence (PL) is an indicator of the film quality and sensitive to adsorbed contaminants, strain and other extrinsic effects. A typical PL spectrum of the film is shown in Fig. 5.5a. The A exciton is found at 1.89-1.90 eV, slightly blue shifted compared to conventional CVD and exfoliated

material.[81] We attribute this to strain induced by the higher thermal expansion coefficient of the SiO_2 substrate as compared to the MoS_2 film leading to compressive strain during cool down from growth temperatures, as is to be expected for a continuous film. Compressive strain of MoS_2 is typically associated with a blue-shift of the PL signature, as observed here.[82] This finding ascertains the mechanical continuity of our film at the wafer scale. The full width at half maximum of the PL peak is consistently at an excellent value of ~0.077 eV. The PL brightness of the films rivals the best exfoliated and CVD samples we have produced. The B exciton is barely visible at 2.06 eV further confirming the material quality. Mapping of the PL peak position across the sample shows variations on the single-digit millielectronvolt scale only (Fig. 5.5b).

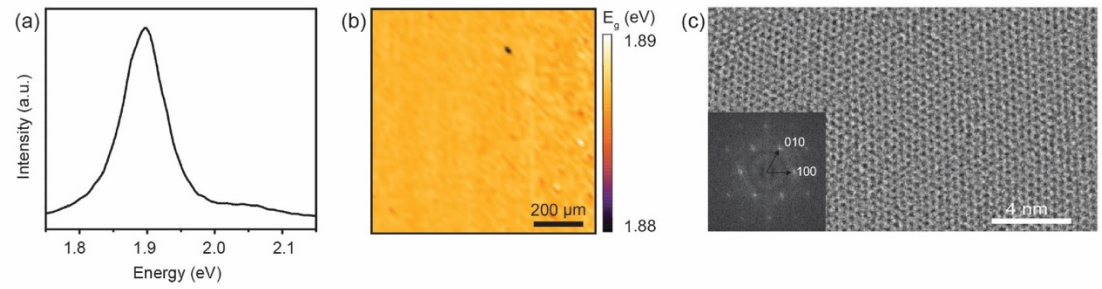


Figure 5.5: (a) Photoluminescence spectrum of a single-layer MoS_2 film. (b) Mapping of the A-exciton position across 1x1 millimeter of sample area reveals variations well below 10 meV (full color scale). (c) STEM image of the crystalline structure of the film. The inset shows the Fourier transformation and two indexed peaks.

Scanning electron microscope images of the MoS_2 single layer film are featureless at any length scale (Fig. 5.6). The AFM root mean square surface

roughness is at 0.2 Å slightly better than that of the bare SiO_2 substrate before the growth. Transfer of the film onto a grid for scanning transmission electron microscopy reveals a highly ordered array of MoS_2 unit cells at the expected periodicity (3.31 Å) of the 2H phase (Fig. 5.5c). Extended areas of single-crystalline domains are surrounded by a band of a number of very small (~10 nm) domains, validating the growth mode described above. Fig. 5.2 shows that adjacent extended domains are chemically connected through the small domain band surrounding them, as is important for transport applications.

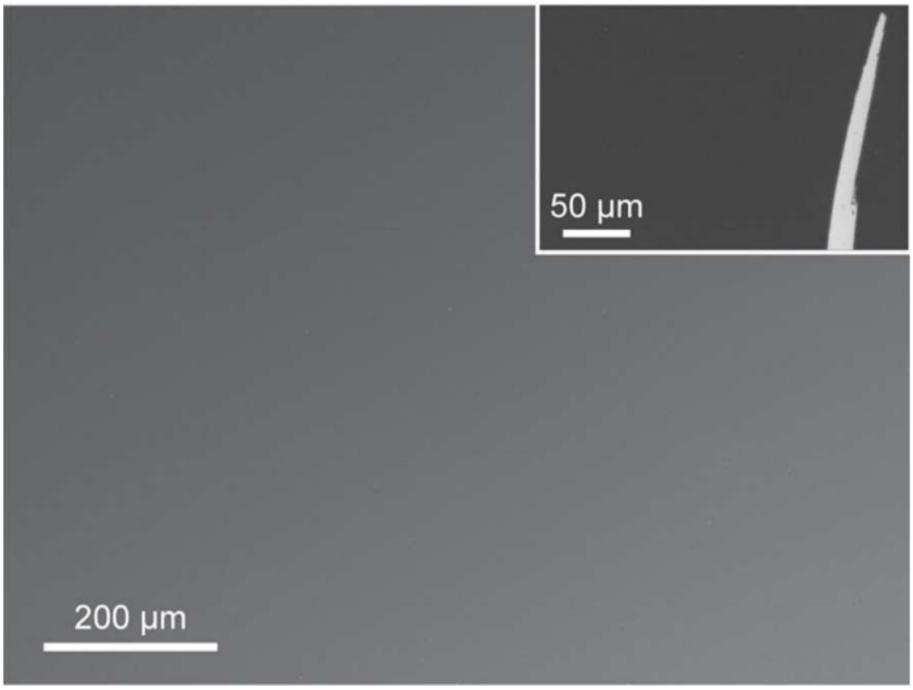


Figure 5.6: SEM image of the monolayer film. Images are entirely featureless given the continuous coverage of the film. Inset of a scratch showing the contrast between the SiO_2 and the MoS_2 monolayer.

Appealing transport properties of the film are crucial for the technological application of the method. Electron beam lithography was used to fabricate 50 field-effect transistor (FETs) test structures using the oxide of the growth substrate as the gate dielectric (bottom-gated without transfer). It is important to highlight that our growth process is sufficiently benign to the substrate that oxide pinholes resulting in gate leakage are absent. We use a device geometry that includes channel length/width of 0.25/20 microns (see insets in Fig. 5.7a for the optical image of the device). The electrodes were fabricated from a stack of 5 nm of yttrium for adhesion and 50 nm of gold. At source-drain voltage V_{sd} below 0.5 V, the output current voltage characteristics (source-drain current I_{sd} as a

function of the source-drain voltage V_{sd}) were linear and symmetric indicating near-Ohmic properties of the drain and source contacts. Fig. 5.7a shows the measured output characteristics at high drain voltage up to 4 V. This biasing condition corresponds to the 160 kV/cm electric field in the channel and power density dissipated by the channel of the order of 10^9 W/cm^3. The reliable operation of mass-fabricated devices at these extreme conditions indicates the high quality of the material. It is known that the temperature dependence of the current voltage characteristics in this type of MoS_2 transistors is governed by two competing mechanisms: decrease of the threshold voltage and decrease of the mobility with the temperature increase.[56] The superlinearity of the characteristics in Fig. 5.5a can be naturally explained by the Joule heating causing a decrease of the threshold voltage and a small degradation of the mobility.

Fig. 5.7b shows the measured current as a function of applied gate voltage at fixed source-drain biases. The characteristics in Fig. 5.7b do not show any trend of saturation at high gate voltage and are quite typical for bottom-gated MoS_2 devices in the absence of engineered contacts, such as edge contacts or the use of graphene as a contact material. The low apparent mobility in these devices on the order of 1 can directly be attributed to the common challenge of contacts to MoS_2 devices rather than indicating a property of the film; we expect that integration of top-/dual-gating and engineered contacts would show the full potential of this material.[83-90]

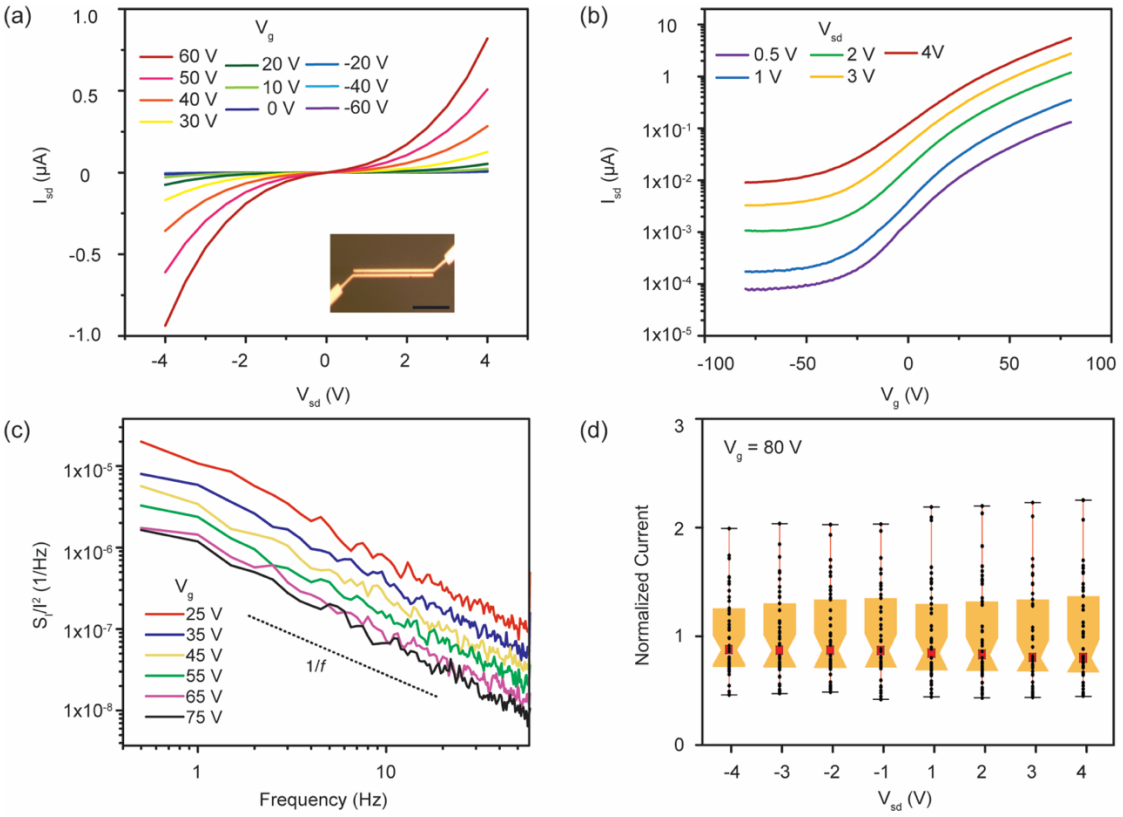


Figure 5.7: (a) IV characteristics of the single layer MoS_2 film at different gate voltages. Inset of an optical image of the device structure. The scale bar is 10 μm. (b) Source-drain current as a function of gate voltage for a single layer MoS_2 device. (c) Noise power as a function of frequency. (d) Box and whisker plots of the variation of I_{sd} at fixed V_g and for a set of V_{sd}, normalized to the average I_{sd} at the respective V_{sd}. Data is collected from 47 devices evenly spread across >1 cm^2 of substrate area.

The level of the low frequency noise is an important metric of the material quality and suitability for electronic applications.[91] It is particularly important for two-dimensional materials where conduction electrons in the device channel are ultimately exposed to various defects in the gate dielectric and top surface.[92] The level of the low frequency noise can be used to assess the concentration of defects and material tolerance to electromigration. In practical applications, the

low frequency noise defines the phase noise in communication systems and sets the limits for sensor sensitivity and selectivity. The low-frequency noise was measured in the frequency range from 1 Hz to 50 Hz at room temperature. The devices were biased in a common source mode. Details of our noise measurement procedures have been reported by some of us elsewhere.[93-95] Fig. 5.7c shows the normalized noise spectral density S_I/I_{ds}^2 as a function of frequency for a representative MoS_2 device. The noise is of clear 1/*f* type (*f* is a frequency). The absence of the generation – recombination bulges indicates that there are no high concentrations of any specific defect, which would dominate the low frequency noise response. The noise spectral density reveals scaling with the applied gate bias, i.e. carrier concentration in the channel, expected for semiconductor devices.[96] The 1/*f* noise level in field effect transistors is often characterized by the noise amplitude normalized to the channel area.[97] The minimum noise level measured in studied devices was of the order $2x10^{-7}$ $Hz^{-1}\mu m^2$. This is smaller than that reported in earlier publications for MoS_2 transistors implemented with the exfoliated or CVD material.[94, 98] The latter provides an additional confirmation of the material quality from the device applications' point of view.

In order to demonstrate the homogeneity of the film, we fabricated a set 50 devices evenly spaced across more than 1 cm^2 of substrate area. Of the 50 devices fabricated, one had a failure of the electron beam during writing, and two were lithographically nonviable. Fig. 5.7d shows a box and whisker plot of the

variation of I_{sd} at different V_{sd} across all remaining 47 devices. We find a maximum variation by a factor of 2 and an interquartile range of 0.8-1.3 with 1 normalized to the average current at any V_{sd}.

Summary

In conclusion, the scalable growth of continuous single- and few-layer MoS_2 is demonstrated using a high vacuum deposition process. Optical and electrical characterization validate high quality and homogeneity of the material as well as superior noise performance. We highlight that these results are achieved using an amorphous SiO_2 substrate and without any powder or metal-organic precursors. Using the color of light reflected from the substrate, process control at the single-layer limit is achieved.

Chapter 6: Epitaxial Molybdenum Disulfide / Gallium Nitride Junctions: Low-Knee-Voltage Schottky-Diode Behavior at Optimized Interfaces

The following is taken from an article published in ACS Applied Materials & Interfaces[99] in collaboration between myself, and other students: Hae In Yang, Daniel J. Coyle, Prachi R. Yadav, Michael D. Valentin and Kortney Almeida of Ludwig Bartels and Mahesh R. Neupane of ARL. It has been rewritten in a form appropriate for the dissertation.

Abstract

Low turn-on (knee) voltage (~0.3 V) Schottky-diode behavior of a four-layer (4L) MoS_2 / GaN junction is achieved by optimizing the i*n-situ* interface preparation of the GaN substrate prior to MoS_2 overlayer growth in a vacuum system using metallic molybdenum and hydrogen sulfide gas as precursors. The process leads to a clean nitrogen-terminated GaN surface that bonds well to the MoS_2 film revealing a 2x2 reconstruction at the interface observed in low-energy electron diffraction (LEED). Atomic force microscopy and X-ray photoelectron spectroscopy provide clear images of the GaN terraces through the MoS_2 overlayer confirming close adhesion and absence of oxygen and other

contaminants. Density functional theory calculations predict the formation of the 2x2 superstructure at a clean interface. Transport measurements show diode behavior at an on/off ratio of ~10^5 for ± 1V with a forward direction for positive voltage applied to the MoS_2 layer. Combining transport and photoelectrons spectroscopy measurements with theory, we deduce a Fermi-level position in the MoS_2 gap consistent with interface charge transfer from the MoS_2 to the substrate. The high performance of the MoS_2/Gan diode highlights the technological potential of devices based on GaN/MoS_2 interfaces.

Introduction

Molybdenum Disulfide (MoS_2) and related layered metal dichalcogenides have experienced extreme interest for electronic applications since the seminal discovery of their semiconducting characteristics down to the single layer in the Heinz[27] and Wang[28] groups a decade ago. Prototypical MoS_2 transistor, memory, memristor, etc. devices have been fabricated, yet a large technological impact is still outstanding. During the same period, gallium nitride (GaN) – initially introduced into semiconductor technology as a wide-bandgap material able to provide blue light emitting diodes[100]– has found a great number of additional applications in high-frequency electronics[101] and for power conversion.[102, 103] Serendipitously, these two materials are almost perfectly lattice matched at

a mismatch of only ~0.8%,[104] while offering complementary properties in many respect including: MoS_2 is a layered (2D) material facile to grow by chemical vapor deposition (CVD) on a great number of substrates[43, 59, 61, 64] while GaN's lattice is non-layered so that CVD growth requires well-matched substrates for appreciable material properties;[105, 106] the bandgap of MoS_2 between 1.26 eV (bulk) to 1.9 eV (single-layer)[27, 28] is only about half that of GaN (3.4 eV).[107] Heterostructures of these materials offer large untapped technological opportunities; their realization and utility rely on understanding of the material interface both for MoS_2 grown on GaN and, ultimately, the reverse. Several recent publications explored them.[108-115] Here we offer detailed insight into the optimization of the former interface using a broad range of surface science and ex-situ techniques.

Beyond exfoliation or transfer,[108, 111] a number of prior studies addressed the growth of MoS_2 on GaN. Work at the Army Research Lab in collaboration with the Robinson group showed growth of MoS_2 single- and multi-layer islands as well as films aligned with the GaN substrate. [116, 117] The absence of photoluminescence from these MoS_2 islands was noted. Extension to thicker layers by means of "metal-organic CVD (MOCVD)"[118, 119] using carbonyl precursors in a flow reactor led to well-layered MoS_2 material separated by several disordered substrate/interfacial layers from the GaN substrate. Several properties of the interface were investigated including a knee voltage of >1eV under diode operation.[120] The Chen group investigated the growth of

MoS_2 GaN composites for photocatalytic water splitting and found that a nitridation step greatly improves the electronic performance of the interface.[121] Liu et al. and Desai et al. grew MoS_2 onto patterned GaN substrates using tube-furnace CVD from powder sources.[109, 112] Lee et al. employed a horizontal hot-wall furnace.[110]

In this study, we start with commercial thin *n*-type GaN layers (NTT-AT, 300 nm *n*-GaN [$2.5x10^{17}$ cm^{-3} Si-doping], 700 nm *n*-GaN [~$1x10^{18}$ cm^{-3} Si-doping], ~3900 nm *i*-GaN/buffer layer [C-doped], 1000 um p-Si [Resistivity ≤ 0.03 Ω·cm]), explore their optimal surface cleaning, and then grow single-layer (1L) as well as thicker (4L) MoS_2 films on them, analyzing the interface by Low Energy Electron Diffraction (LEED) and X-ray Photoelectron Spectroscopy (XPS), as well as Raman spectroscopy, optical and atomic force microscopy (AFM) before presenting electrical transport measurements. Density Functional Theory Modeling (DFT) using the Vienna Ab-Initio Simulation Package (VASP)[122, 123] provides a foundation to our structural determination of the interface and corroborates MoS_2-GaN charge transfer. We identify sputtering with Ne-ions to remove 2nd period contaminants (oxygen, etc.) from the GaN surface as crucial for a high-quality interface. For high-throughput screening of a broad range of sputter fluences, we developed a gradient sputtering technique that offers parallel preparation and investigation of a broad interval of process parameters.

The presence of van der Waals (vdW) gaps above and below each MoS_2 layer reduces its interaction with the substrate and facilitates its layered crystalline growth, but it also reduces the propensity of such growth for epitaxy. CVD MoS_2 growth proceeds substrate-aligned (epitaxial) only on a small number of substrates beyond GaN (e.g., sapphire[64]). In this study we use an ultra-high-vacuum compatible CVD growth technique described previously:[124] our system is capable of seamlessly i) clean a GaN substrate by sputtering, ii) then apply a high-temperature ammonia treatment to replace nitrogen lost during the sputtering process and generate a well-defined surface termination, and iii) finally grow a MoS_2 film of controlled and uniform layer number - all without breaking vacuum. Fig. 6.1 shows a schematic representation of the system (the supplementary section S1 shows a photo). So as to test a broad range of sputter fluences all in one run and without any variation in other growth conditions, a precision-controlled shutter is guided over the sample to generate a dose gradient. Measurement of the target current validates sputter fluence and beam alignment on the target (see supporting information section).

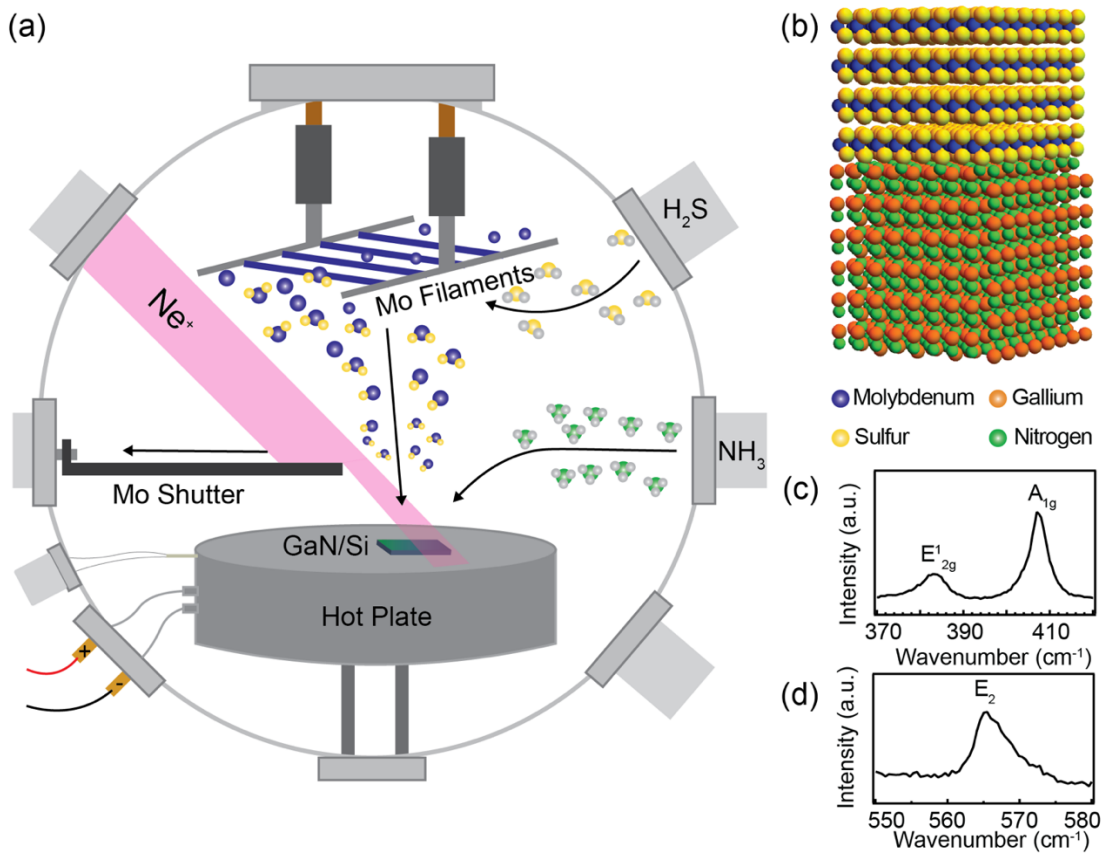


Figure 6.1: (a) Schematic representation of the growth reactor with different process steps indicated. (b) Atomic representation of stacked multilayer MoS_2/GaN structure. (c) Raman spectra of the MoS_2 E^1_{2g} and A_{1g},modes and (d) the E_2 mode of the GaN substrate.

MoS_2 deposition proceeds by exposing hot metallic molybdenum filaments (pyrometrically determined to be ~1,700 ºC hot) to H_2S gas, resulting in the decomposition of the latter on the filament surface and generating MoS_x precursors with a vapor pressure far higher than refractory molybdenum. These precursors evaporate from the filaments, precipitate on the substrate that is held at 650 ºC by a hot plate, and form a continuous MoS_2 layer. Colorimetric analysis of the reflection of the filaments from the sample allows us to monitor the layer

thickness during growth and to end the deposition process precisely at the desired integer layer number.[124] XPS and LEED analysis was performed after transfer of the sample to a vacuum system equipped with a Spectra RS3000 analyzer, an OCI LEED system modified for computer control of gun and sample position, as well as ancillary instrumentation such as a sputter gun and evaporation sources.

Results and Discussion

The resultant MoS_2 film exhibits a Raman spectrum (Fig. 6.1c) as expected from the literature and is otherwise free of optical contrast. The GaN substrate retains its characteristic Raman mode during overlayer growth (Fig. 6.1d). No photoluminescence of the MoS_2 is observed on the GaN substrate. Prior to MoS_2 growth, the as-received *n*-type GaN substrates were cleaned using a subsequent rinses in acetone, isopropanol, and de-ionized water. before being dipped into a piranha solution (30 ml H_2SO_4, 10 mL H_2O_2) for 5 min. The method described here leads to the lowest peaks for oxygen and carbon, and the best defined GaN valence band edge.

To validate epitaxial growth and the quality of the GaN-MoS_2 interface, we performed low energy electron diffraction (LEED) on a single-layer of MoS_2 on GaN. LEED has a very high surface sensitivity[125] rendering work on a

monolayer (rather than a multilayer) of MoS_2 necessary to gain structural information on MoS_2/GaN interface. Fig. 6.2 shows four LEED images across the sputter gradient of the GaN substrate from lower to higher sputter dosage; the sputter doses are indicated in each panel. At a low dose of 5 mC/cm^2, a sharp hexagonal diffraction pattern is visible (Fig. 6.2a), which we attribute to the substrate periodicity (which is in good match to that of MoS_2, especially given the known flexibility of the material).[126] Increase of the sputter dose to values between 15 and 35 mC/cm^2 results in a doubling of the periodicity (Fig. 6.3b,c) generating a 2×2 pattern. Further sputter exposure results in broadening of the initial hexagonal spots and the 2×2 spots disappear. We interpret this as the substrate surface becoming disordered leading to less than epitaxial growth atop of it (Fig. 6.2d).

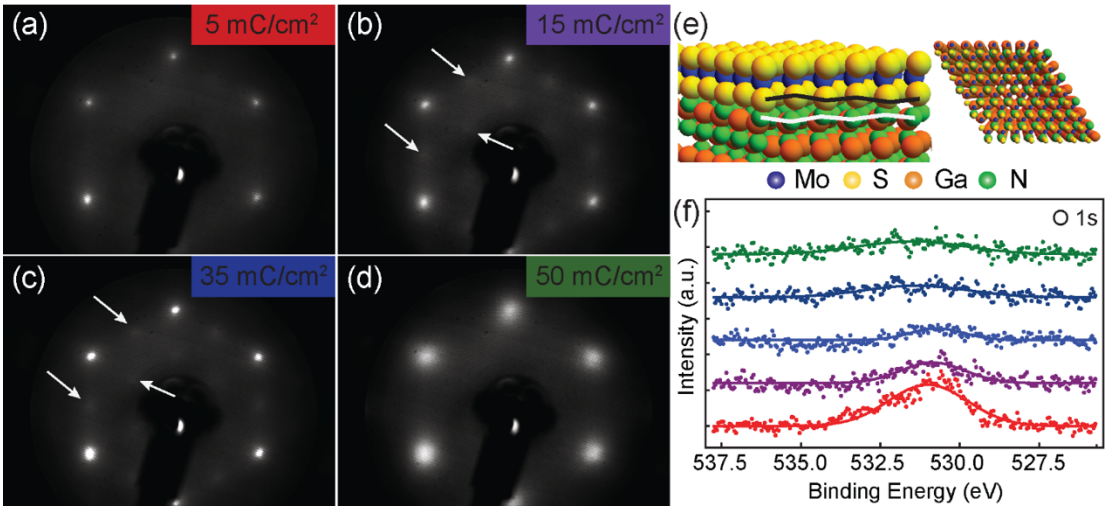


Figure 6.2: LEED patterns obtained at 100eV beam energy on (a) 5 mC/cm^2, (b) 15 mC/cm^2, (c) 25 mC/cm^2, and (d) 40 mC/cm^2 sputtered portions of a 1L MoS_2/GaN sample. A 2x2 superstructure is observed for intermediate sputter doses; the associate LEED spots are annotated by arrows; (e) DFT model of an N-terminated GaN/MoS_2 interface exhibiting a buckling of the top nitrogen layer (highlighted by the wavy line) with a 2x2 periodicity; f) photoelectron spectroscopy of the oxygen 1s core level as a function of the sputter dose (same color code as labels in a-d).

There are several DFT simulation of the MoS_2/GaN interface available in the literature;[114, 121, 127, 128] generally, it is found that the surface energy of the Ga-terminated surface is higher than that of the N-terminated surface,[127] and that MoS_2 correspondingly exhibits a higher adsorption energy on the former. For each termination, the optimal adsorption geometry places the MoS_2 sulfur atoms on top of the substrate top-layer atoms (Fig. 6.2e). Our nitridation step directly prior to MoS_2 growth ensures that a nitrogen-terminated surface is present in our experiments. Using a 6-layer stack of GaN and both 1L and 4L MoS_2 (Fig. 6.1b) in a 2x2 lateral supercell (for a total of 144 atoms), we minimized the total energy for both the N- and Ga-terminated surface testing a

variety of adsorption sites, namely Ga-top, N-top and intermediate sites, and obtained results consistent with the literature.[117, 129] We noticed that energy minimization on the favorable configuration on the N-terminated surface (Fig. 6.2b) is unique among the superstructures in that it naturally results in a 2x2 superstructures with alternating top-layer substrate nitrogen atoms being depressed and lifted resulting in a similar buckling of the first-layer sulfur layer of the MoS_2 overlayer. To ascertain the validity of this finding, we optimized the supercell until all forces were below 2 meV/Å both for the N-terminated surface, where the 2x2 superstructure is found, and the Ga-terminated one, where it remains absent. Notably, the vertical separation between the top nitrogen layer and the bottom sulfur layer is found to be only ~2.4 Å, smaller than the previously reported separation on Ga-terminated GaN on MoS_2 system[129]. We conclude that the S states (s, p_y and p_z) strongly hybridized with the N states (p_x, p_y and p_z).

We interpret the buckling found in DFT as the origin of the 2x2 superstructure spots in the LEED patterns at intermediate sputter dose. The presence of the 2x2 superstructure attests to a clean and well-ordered termination of the GaN substrate; were the substrate contaminated or rough, then a comparatively long-range order at the heart of the 2x2 reconstruction could not form and no 2x2 spots were observable in LEED.

XPS can serve as an alternative way to ascertain the cleanliness of the substrate. Our XPS measurements use a hemispherical analyzer read out by a 2D multichannel plate detector. One of the detector axes corresponds to energy dispersion in the hemisphere; the other to the spatial position on the substrate along the sputter gradient. Thus, slicing of the 2D dataset along the energy direction at different locations provides us with spectra and their variation with sputter fluence. We performed such measurements across the sputter gradient for all relevant elements (Mo, S, Ga, N; impurities: C, O; Valence Band (VB) edge) both for 1L and 4L MoS_2 films. Fig. 6.2f shows how the oxygen contamination of the surface decreases with sputter dose up to ~25 mC/cm^2, when it is not identifiable anymore. The supporting information shows the entire dataset for 1L MoS_2 including the other elements. For Ga,N,S, and Mo, we find sharpening of the peaks towards intermediate sputter fluence, with broader peaks at lower dose (presumably due to insufficient removal of contamination) and higher dose (presumably due to surface damage). We will discuss the XPS results more in the context of explaining the transport measurements.

Atomic Force Microscopy (AFM) was used to characterize the surfaces after film growth. Fig. 6.3 shows three AFM images taken at locations of low, intermediate and high sputter dose on a 1L MoS_2 on GaN sample. There is a marked distinction between areas of different sputter dose: at a low dose of 3 mC/cm^2, no clear image of the GaN terrace structure could be obtained (Fig. 6.3a), presumably due to less than perfectly conformal substrate coverage

caused by remaining substrate contamination. Imaging at a location with 25 mC/cm^2 sputter dose, the substrate terraces are clearly defined under the MoS_2 overlayer attesting to good adhesion and conformal coverage. At an area with a local sputter dose of 48 mC/cm^2 we observe very small clusters on the surface that disrupt clear imaging and, presumably, uniform MoS_2 overlayer growth. We tentatively attribute the clusters to gallium sulfide or similar compounds formed during post-sputtering sulfurization of a nitrogen deficient surface in the course of MoS_2 growth. We note that neon was chosen as sputter gas to assure good mass match with 2^{nd} period contaminants (such as oxygen and carbon, but also the GaN nitrogen), yet is unlikely to remove gallium atoms from the substrate.

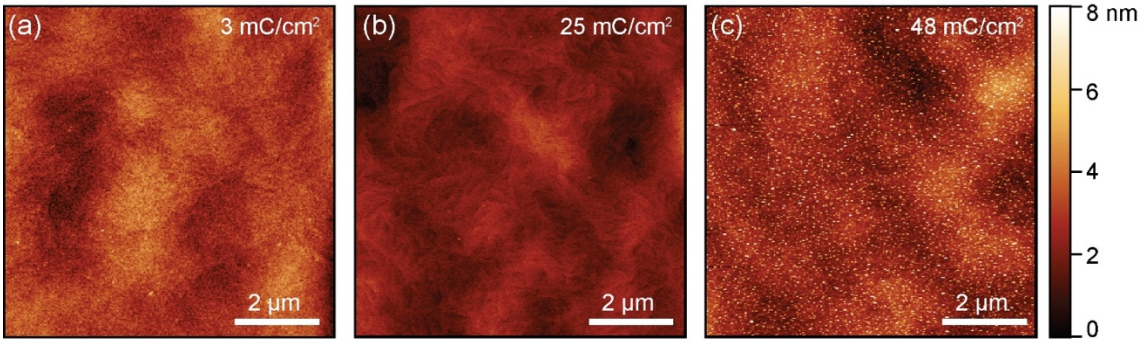


Figure 6.3: AFM images at different locations in a sputter gradient on a 1L MoS_2/GaN sample. (a) 3mC/cm^2; (b) 25 mC/cm^2; (c) 48 mC/cm^2. Conformal adhesion of the MoS_2 revealing a clear image of the underlying GaN terrace structure is only found at intermediate dose.

In order to test the ramification of the different interface preparations on the electrical properties, in particular the transconductance, of the MoS_2-GaN interface, we patterned devices on the substrate as shown in Fig. 6.4a. Each

device consists of a row of 120 by 120 micron Ti/Au pads placed on GaN and MoS_2/GaN. Fabrication proceeded in multiple steps of electron beam lithography: in the first lithographic steps, the MoS_2 contact areas are defined (i) and a 5nm titanium/50nm gold stack is deposited (ii). After lift-off and deposition of a new resist layer, the GaN contact is defined and the MoS_2 material is removed via sputtering with argon at 3keV (iii). Argon is chosen instead of neon for optimal mass match with sulfur, molybdenum and gallium, so as to prepare a clean and reactive GaN surface to support contact adhesion and reduce contact resistance. Without breaking the vacuum (base pressure 1×10^{-8} torr), a 5nm Ti and 50 nm Al stack is deposited as described by Greco et al.[130] (iv). Note that no annealing occurred so as to preserve the MoS_2 layer. After Al deposition, the sample is transferred through air to a gold evaporator and a capping layer of 50nm is applied. After liftoff, the third lithographic step begins by defining the area between the contacts (v). Subsequently, the MoS_2 is removed here as well by Ar sputtering (vi). The supporting information shows a picture of a series of such devices across the sputter gradient.

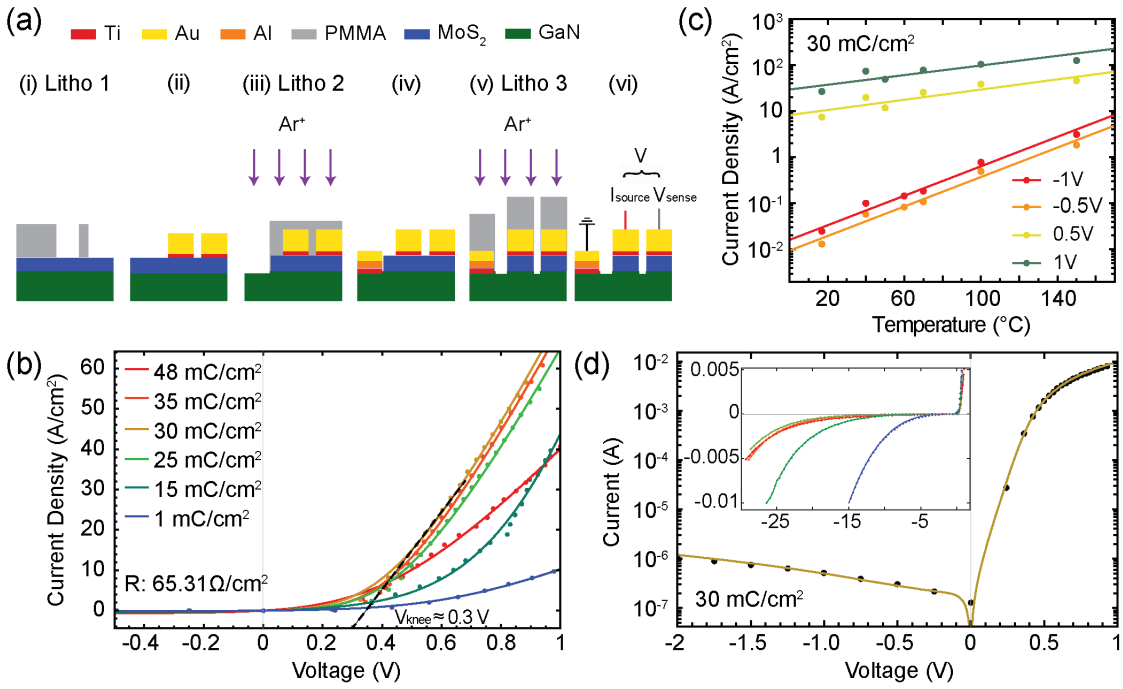


Figure 6.4: a) schematic representation of 4L MoS_2/GaN device fabrication; b) Current density vs. voltage for devices fabricated at locations with different sputter dose. A low knee voltage of 0.3 V is observed; c) temperature dependence of the current density at different bias voltages; d) a logarithmic plot of the I-V data for the optimal sputter dose can be fitted by an analytic function and reveals an on-off ration of ~10^5. The inset shows that reverse-voltage breakdown occurs at lower voltage for less sputtered interfaces.

The transport characteristics of the MoS_2/GaN diodes are shown in Fig. 6.4b with the voltage source from a Keithley 2400 source meter applied to the MoS_2 and ground to GaN. All measurements proceeded under voltage control in a three-terminal setup. To sense the voltage prior to the diode junction, we use a Keithley 6517a electrometer. The voltage *V* on the x-axis of Fig. 6.5 is the difference between the voltage applied to the MoS_2 and the observed electrometer voltage at the sense contact, thus approximating the voltage drop

across the MoS_2/GaN stack while excluding contact resistance at the metal/GaN interface and most of the lateral voltage drop in the GaN layer. The supporting information shows the electrical properties of our GaN contacts and affirm that the features of Fig. 6.4 do not stem from the latter. In particular, the exclusion of the metal/GaN interface in our measurement is motivated by an earlier study by Regan and et al.[129] where it was demonstrated that the transport characteristics across a metal/1L-MoS_2/GaN stack is dominated by the metal/GaN interface for both the *n*- and *p*-doped GaN.

We find a marked diode behavior of the MoS_2/GaN stack, whose details depend on the sputter dose of the interface. The forward direction of the diode is found, similar to previous studies,[108, 112, 120] for a positive voltage applied to the MoS_2, i.e. for electron transfer from the GaN to the MoS_2 layer. The turn-on or knee voltage (V_{knee}) of the diode is ~0.3V, much lower than for Si-based diodes (0.6-0.8V) and rather resembling a Schottky diode (0.2-03V). It is also much lower than the value reported in Ref. [120], presumably owing to the interface preparation. The diode has a high current density of ~100 A/cm^2 at 1V. The current at -1V bias is ~5 orders of magnitude smaller than that at +1V, i.e., the diode has an on-off ratio of ~10^5.

We find best diode behavior at sputter doses of ~30 mC/cm^2; doses in excess of 40 mC/cm^2 lead to lower forward current while sputter doses below 20 mC/cm^2 have a similar effect and also push the knee voltage (V_{knee}) towards

larger values. Low sputter doses also lead to reverse breakdown at lower voltage (inset of Fig. 6.4d).

We attribute the high dose behavior to a rougher MoS_2/GaN interface. As can be seen from Fig. 6.3c, at high sputter dose AFM observes the formation of small clusters on the substrate, presumably reducing the area of perfect interface between the substrate and MoS_2 overlayer. This reduces the active area of the diode and, thus, its forward current. We attribute the deterioration of the properties at low sputter dose to the presence of oxygen in the interfacial layer changing both its electronic character and preventing optimal adhesion/epitaxy. Exfoliation of MoS_2 onto GaN has been shown to lead to diodes with a knee voltage of 1-2V and an on-off ratio at ±5V of ~ 10^3, almost two orders of magnitude smaller than those sputtered at ~30 mC/cm^2.[108] Other growth studies either found results[112] similar to exfoliation MoS_2 junctions or high transconductance but no pronounced blocking behavior,[110, 111] which may be interpreted as breakthrough at very low reverse bias, similar to the trend we observe for low sputter doses.

Fig. 6.4d includes a fit of the measured current (I) data using the Schottky model of a diode: $I = I_S(\exp[V/(nV_T)]-1)$ with I_S the scale current, n the ideality factor, and V_T the thermal voltage taken as $V_T = kT/q$ =25.85 mV, with k the Boltzmann constant, T the absolute temperature, and q the absolute of the electron charge. We expanded the Schottky model by two terms, replacing V by

*V-I*R* to account for a series resistance *R* of the junction[131] and an additive *V*/*Vp***Ip**(1-exp[*V*/*Vp*]) term[132] to account for a tunneling current *Ip* at reverse voltage *Vp* through the thin diode layer:

$$I = I_S\left(e^{V-I\times R}/_{n\times V_T}\right) + {}^{V}/_{V_P}\, I_P\left(1 - e^{V}/_{V_P}\right) \qquad (1)$$

Fitting the experimental data reveals a series resistance of ~50 Ohm, an ideality factor of 1.8, a scale current of 20 nA, and the tunneling behavior described by 2 μA at 2.4 V for I_P and V_P, respectively. These are excellent values for our prototypical device geometry.

Temperature-dependent data on the transconductance were obtained both for forward and reverse bias (Fig. 6.4c). We observe a marked distinction of the thermal behavior at forward and reverse bias, as expected for a diode as thin as the one fabricated here. The supporting information section provides an Arrhenius-type fit of the current density $J = A \exp(E_b/kT)$ with A as a prefactor term and E_b as an energy barrier. At reverse bias, we find E_b to be ~380 meV, in line with the knee voltage. At 0.5V/1.0V forward bias, we find values of ~140 meV/110 meV.

Note that *n*-type behavior is expected both for the GaN substrate (through doping) and the MoS_2 layer, as is typically for CVD MoS_2 material. Thus, a pronounced diode behavior is not necessarily expected. To understand its origin, it is helpful to take another look at XPS data: Fig. 6.5a compares the valence

band (VB) region of bare GaN after nitridation (bottom) and following 4L MoS_2 deposition (top). On bare GaN, we find the VB edge at ~3.1 eV suggesting *n*-type GaN material consistent with the commercial supplier specification. In addition, we observe some density of states near the Fermi edge (arrow in Fig. 6.5a), which we attribute to unsaturated dangling nitrogen bonds at the nitrogen terminated surface. The supporting information section shows the element-projected density of state (pDOS) for a 4L MoS_2/GaN interface (6 layers of GaN). Nitrogen-originating density of states is found right below the Fermi level in the semiconductor gap.

The MoS_2 VB edge is found at ~0.4 eV below E_F, closer to the Fermi energy than for material grown on $SiO_{2[133]}$ and indicating a material that appears like a *p*-type semiconductor (4L MoS_2 has a bandgap of 1.26 eV, so for the VB edge at 0.4 eV below EF, the Fermi energy is below mid-gap). We attribute this observation to charge transfer at the interface.

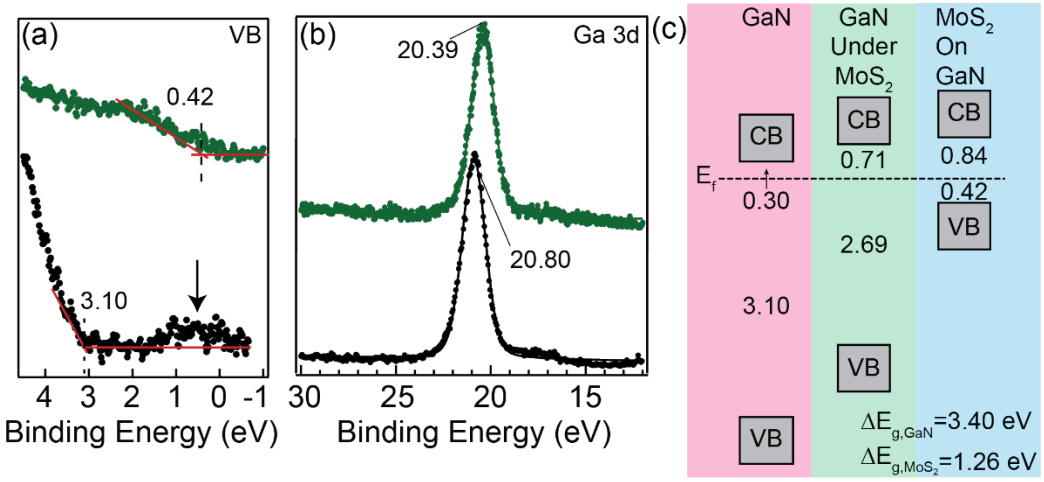


Figure 6.5: a) Valence band (VB) edge XPS spectra of nitridated GaN prior to (bottom) and after (top) 4L MoS_2 growth. The respective band edges are indicated. Additional, density of state from the nitrogen termination is observed near the Fermi energy (E_f) on bare GaN (arrow); b) GaN 3d state before (bottom) and after (top) MoS_2 overlayer growth. The upshift shows surface band bending associated with charge transfer to the GaN; c) energy diagram of the VB and conduction band (CB) position of GaN prior to 4L MoS_2 deposition (left), after 4L MoS_2 deposition (middle), and of the MoS_2 layer (right) based on known band gaps indicated.

To understand the interface charge transfer, we address the Ga 3d peak. Prior to MoS_2 deposition, we find the Ga 3d state at ~20.8 eV binding energy, well in line with typical values for GaN. After MoS_2 deposition, we observe an upshift by ~0.4 eV to ~20.4 eV. This indicates surface band bending by 0.4 eV in the course of MoS_2 deposition, i.e. charge transfer from the MoS_2 to the GaN. As MoS_2 is typically natively *n*-type, we interpret this finding as the *n*-type carriers of the 4L MoS_2 CB dropping into the GaN CB, thereby shifting the energy of the GaN surface and the Ga 3d state up, i.e. upward surface band bending. In this process the MoS_2 loses its *n*-type character shifting the Fermi level below midgap.

Fig. 6.5c shows the VB and CB edge positions as obtained from the XPS measurements and calculated based on literature bandgap values, respectively. Assuming that the GaN VB edge upshifts in sync with the GaN 3d state, the MoS_2 CB edge comes to lie 0.1-0.2 eV above the GaN CB edge, corroborating the notion of *n*-type carriers dropping from MoS_2 into GaN. We note that this mechanism also explains the absence of photoluminescence for MoS_2 on GaN: excitons rapidly split by transfer of the excited carrier into the GaN CB.[134]

As a consequence of this band alignment, the MoS_2/GaN diode resembles much more a Schottky diode of an *n*-type material than a *pn*-juction; all transport takes place in the CB. The knee voltage of 0.3eV is in reasonable agreement with the MoS_2-GaN CB offset of 0.1-0.2 eV to enable electron transport from the GaN CB to the MoS_2 CB and on into a metal contact. It also agrees well with the barrier for reverse current found from the temperature-dependent measurements on the diode.

Finally, we seek to corroborate this finding by analyzing the charge and potential distribution in our computational supercell. Fig. 6.1b shows its thickness; each supercell layer contains 2x2 GaN or MoS_2 unit cells and there are 4 MoS_2 and 6 GaN layers in our calculation. We caution that our DFT simulation does not represent overall band alignment faithfully, likely because of absence in the model of (i) explicit *n*-doping of the GaN substrate, (ii) native *n*-doping of the MoS_2 layer, and (iii) termination of the bottom Ga-layer of the GaN

slab. However, we can still evaluate the charge transfer directly at the GaN/MoS_2 interface. This will lead to a built-in electrical field and potential that can affect the transfer characteristics of the 2D/3D heterostructures.

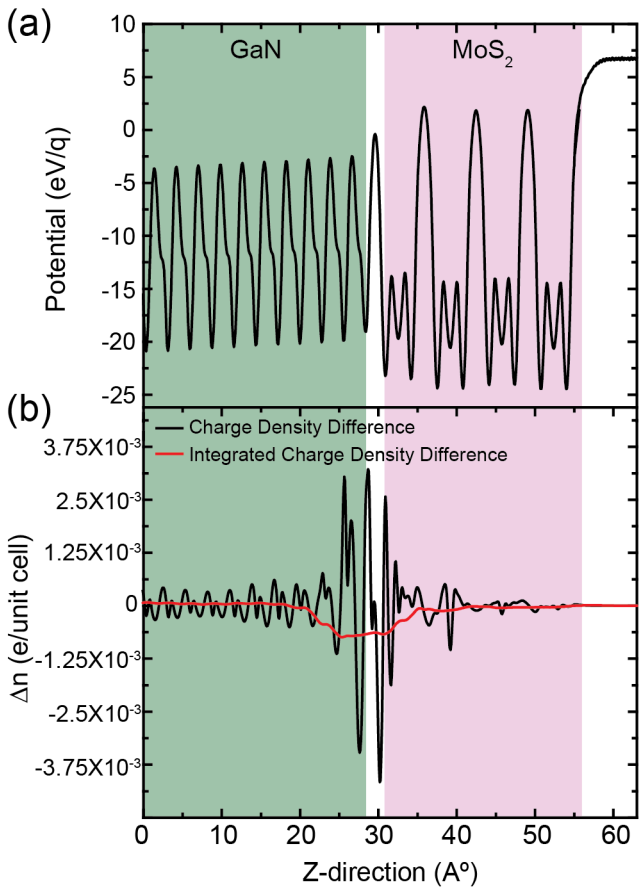


Figure 6.6: a) Planar potential variation at the GaN/MoS_2 interface: upward band bending is observed for GaN toward the interface; b) Interface charge transfer: the charge density difference (black) of the combined MoS_2/GaN system as compared to the separated system and its integral from the right (red). Visible is charge transfer from the MoS_2 layer and particularly the interface region to the GaN bulk.

Figure 6.6 illustrates electrostatic potential and charge difference profiles along z-direction, i.e. normal to the heterostructure. As can be seen in Fig 6.6a,

the interfacial built-in potential throughout the vdW interface, mainly due to the charge reconfiguration at the hybridized S and N states, leads to an upward slope in the GaN region towards the interface, ie. a surface band bending consistent with the experimental finding. In addition, the local electrostatic potential around the sulfur atoms at the interface in the heterostructure is reduced by 4 eV, as compared to the isolated 4L-MoS_2 system, leading to a lower barrier for electron migration across the interface. The charge redistribution is visualized in Figure 6.6b as the difference between charge density of the isolated layer slabs and the combined ones. Significant deviation (black line) from the isolated slabs in the vicinity of the interface attests to the chemical interaction here manifest in the 2x2 superstructure. The integrated charge density difference (red line, using a 10Å-width rolling average) shows charge density loss throughout the MoS_2 film amplified directly at the interface, and charge gain by the GaN substrate except directly at the interface, where direct chemical interactions between the nitrogen and sulfur layer are observed. This net charge transfer was also predicted from the XPS data.

In order to quantify and validate the MoS_2/GaN charge transfer, we performed a Bader charge analysis[135] across the interface. The S atoms at the interface loose on average 0.025 electron charges each, consistent with the charge profile picture. Most of the transferred electrons are acquired by the surface N-atoms yet N-atoms in neighboring layers also acquire a small fraction

of electrons, which is also evident from the non-zero charge profile feature in the GaN region, away from the surface in Fig. 6.6b.

Summary

In conclusion, we find that careful optimization of the interface allows fabrication of high quality GaN/MoS_2 diodes with a low knee voltage and high on-off ration. Because of the device geometry employed here, no meaningful high-frequency measurements are feasible, however, all results suggest that good high-frequency response is expected. Future research seeks to extend this work to GaN/MoS_2/GaN *npn*-heterojunction bipolar transistors. In this context, it is an important outcome of the current work, that MoS_2 loses its native *n*-type character simply by the interface interaction at the N-terminated GaN substrate and that no further treatment of the MoS_2 (e.g., such as niobium doping[136]) may be necessary to attain such a goal. Our findings highlight the importance of atomistic control of the interface, even for 2D vdW materials, which are generally assumed to be more robust to interface contamination than classic epitaxial systems such as GaAs/GaAlAs.

Chapter 7: Low Resistivity and High Breakdown Current Density of 10-nm Diameter van der Waals $TaSe_3$ Nanowires by Chemical Vapor Deposition

The following is taken from an article published in Nanoletters[36] in collaboration between myself, and other students: Thomas A. Empante, Aimee Martinez, Yanbing Zhu, Adane K. Geremew, Koichi Yamaguchi, Miguel Isarraraz and Sergey Rumyantsev of Ludwig Bartels, Alexander Balandin, and Evan Reed. It has been rewritten in a form appropriate for the dissertation.

Abstract

Micron-scale single-crystal nanowires of metallic $TaSe_3$, a material that forms -Ta-Se_3-Ta-Se_3- stacks separated from one another by a tubular van der Waals (vdW) gap, have been synthesized using chemical vapor deposition (CVD) on a SiO_2/Si substrate, in a process compatible with semiconductor industry requirements. Their electrical resistivity was found unaffected by downscaling from the bulk to as little as 7 nm in nanowire width and height, in striking contrast to the resistivity of copper for the same dimensions. While the

bulk resistivity of $TaSe_3$ is substantially higher than that of bulk copper, at the nanometer scale the $TaSe_3$ wires become competitive to similar-sized copper ones. Moreover, we find that the vdW $TaSe_3$ nanowires sustain current densities in excess of 10^8 A/cm^2 and feature an electromigration energy barrier twice that of copper. The results highlight the promise of quasi-one-dimensional transition metal trichalcogenides for electronic interconnect applications and the potential of van der Waals materials for downscaled electronics.

Introduction

The preparation, characterization, and application of two-dimensional (2D) materials such as graphene[137-140], transition metal dichalcogenides (TMDs)[25, 27, 28, 141-143], and MXenes[144-147] have attracted broad attention over the past years. This is partly due to the unique properties such materials exhibit when thinned to a single layer, yet it is also due to the astounding chemical stability and well-defined optical and electronic properties that these materials retain, even when only a single layer thin. Arguably, the latter is their most outstanding feature; it is caused by the presence of a planar van der Waals (vdW) gap in the crystallographic structure that affords some independence between the layers even in the bulk. When thinned to a single layer, the vdW gap prevents dangling bonds on the basal plane reducing

scattering in transport and chemical reactivity to the environment. Recently, some of us have discovered almost 500 known compounds that resemble these 2D materials in as much as that their bulk contains vdW gaps, but these gaps are tubular in nature creating one-dimensional (1D) stacks of bound atoms separated from the neighboring stack similar to how a graphene or MoS_2 sheet is separated from the one above and below. Initial transport measurements on metallic 1D vdW tantalum triselenide ($TaSe_3$)[95, 148, 149] and zirconium tritelluride ($ZrTe_3$)[150] by some of us revealed good conductivity and exceptionally high breakdown current on mesoscopic exfoliated wire bundles, however no systematic study of the dependence of the wire conductivity on its width/height has been conducted so far. Here we show that chemical vapor deposition (CVD) allows the fabrication of wire bundles as small as a few nanometers across (i.e. consisting of a hundred atom stacks or less in parallel), scaled to the demand of the semiconductor industry for upcoming processing nodes. Most importantly, we find that such nanoscale bundles retain the bulk conductivity, much different to conventional metals, which at the 10 nm cross section scale are strongly affected by surface and grain-boundary scattering.[33-35] Additionally, we find that $TaSe_3$ exhibits a barrier to electromigration more than twice that of copper and can sustain current densities in excess of 10^8 A/cm^2. The favorable scaling of the conductivity with wire cross section renders these materials to be of great interest as next generation interconnect material as copper reaches its scaling limits in 2023 according to the ITRS roadmap.[37-40]

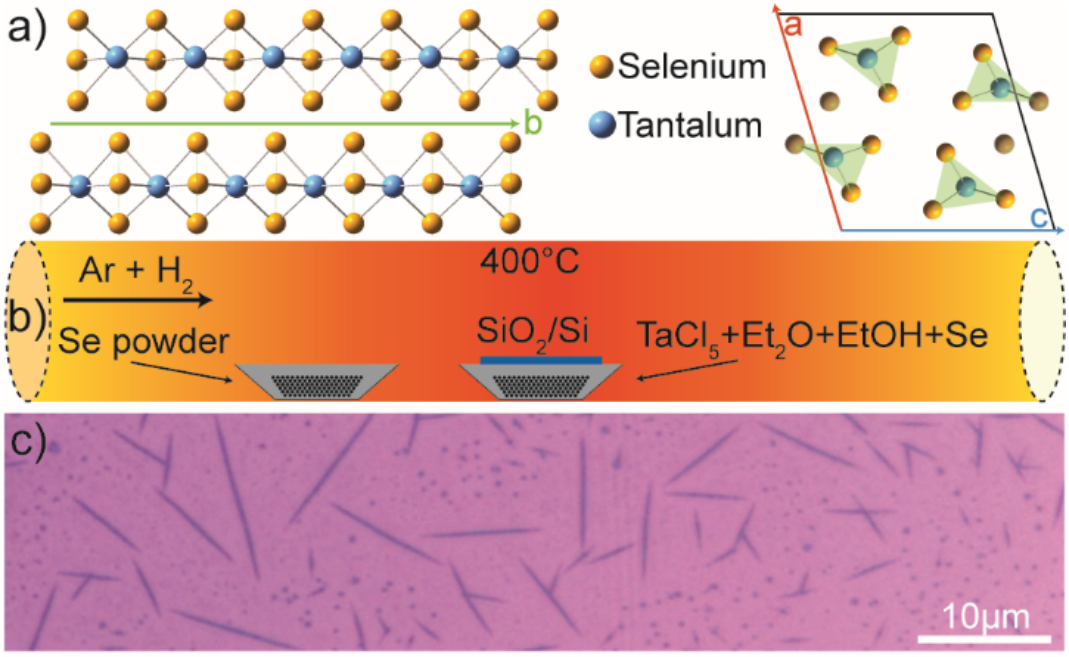


Figure. 7.1 a) Crystallographic structure of $TaSe_3$ consisting of four nanowire Ta-Se_3 stacks per unit cell along the b axis. The greyed atoms inside the unit cell correspond to those shown outside of it in order to highlight the selenium triangles between each tantalum plane; b) schematic representation of the chemical vapor deposition process inside a tube furnace; c) optical image of a population of $TaSe_3$ nanowires.

This manuscript focuses on the preparation and characterization of a specific transition metal trichalcogenide (TMT), $TaSe_3$, on a commercial 300 nm SiO_2/Si substrate using process parameters (ambient pressure, ≤ 400°C process temperature, ≤ 5 min process duration) that are amenable to conventional back-end-of-the-line (BEOL) process limits. Despite the large interest in TMDs, TMTs have been largely left unstudied at the nanoscale; they have varying structures from 2D thin films to 1D wires and properties ranging from insulating to

metallic.[149, 151-153] $TaSe_3$ has a monoclinic unit cell and consists of stacks of Ta atoms, each of which are bonded to three selenium atoms above and below along the b axis (Fig. 7.1a). Neighboring -Ta-Se_3-Ta-Se_3- stacks are separated from one another by a tubular vdW gap exposing chalcogen atoms only, similar to the gap between the Se-Mo-Se layers in 2D $MoSe_2$. $TaSe_3$ has been known for a long time and bulk samples have been prepared using chemical vapor transport (CVT), a process that requires long process times and is not amenable to current semiconductor processing paradigms; exfoliation of such samples yielded the results reported by some of us earlier.[95, 148, 149]

Interconnect performance is crucial for low-power high-clock-frequency computing: the transition from aluminum to copper interconnects starting some 20 years ago was driven by both the better conductivity of copper and the better manageability of electromigration in copper, the key failure mechanism for interconnects.[154, 155] However, as the cross section of an interconnect becomes shorter than the electron mean free path (~40 nm in copper),[33-35] its resistivity increases dramatically due to scattering at the material surface and at internal grain boundaries. A 1D material without surface dangling bonds or internal grain boundaries would, in theory, lack these drawbacks and be a prime candidate.

The best aspect ratio of interconnect cross sections has been studied intensely optimizing interconnect topology while reducing capacitive cross coupling.

Modern processors use aspect ratios between 1.2 and 1.5 on the first four (0-3) metal layers.[156] We show a CVD method that natively generates nanoscale wires with a width to height aspect ratio of ~1, close to the optimal one.

Results and Discussion

The 1D vdW $TaSe_3$ nanowire bundles are synthesized in a chemical vapor deposition (CVD) process using $TaCl_5$ and Se powder as reactants (both 99.99%, Sigma Aldrich). Concurrent volatilization of both reactants under growth conditions is tantamount to sufficient chemical potential of each reactant on the surface during nanowire formation and elongation to the desired length. Thus, in order to match the vapor pressure of the tantalum precursor to that of selenium and the optimal growth temperature of $TaSe_3$, we first add diethyl ether to $TaCl_5$ in an inert nitrogen atmosphere to form the well-known metal chloride adduct $TaCl_5[OEt_2]$.[157] The adduct is dissolved in ethanol, leading possibly to (partial) ligand exchange; a small amount of gas evolution is observed when adding the ethanol. The supporting materials section provide more details on these adducts. Elemental selenium powder suspended in selenium-saturated ethanol is added, and the reactants are well mixed and dried in an alumina crucible. The supporting material section show micrographs that confirm the absence of nanowire formation at this stage. A 300 nm SiO_2/Si wafer substrate is placed across the alumina crucible, which is centered in a quartz process tube. A

second crucible with elemental selenium is placed upstream so as to maintain selenium pressure during the entire growth process (Fig. 7.1b). The process tube is placed in a tube furnace; a mixture of argon and hydrogen is used as ambient-pressure process gases. The furnace is heated to 400°C as fast as possible (~ 15 minutes), held for a few minutes (see below), and then rapidly cooled to ambient temperatures resulting in populations of $TaSe_3$ nanowires as shown in Fig. 7.1 c).

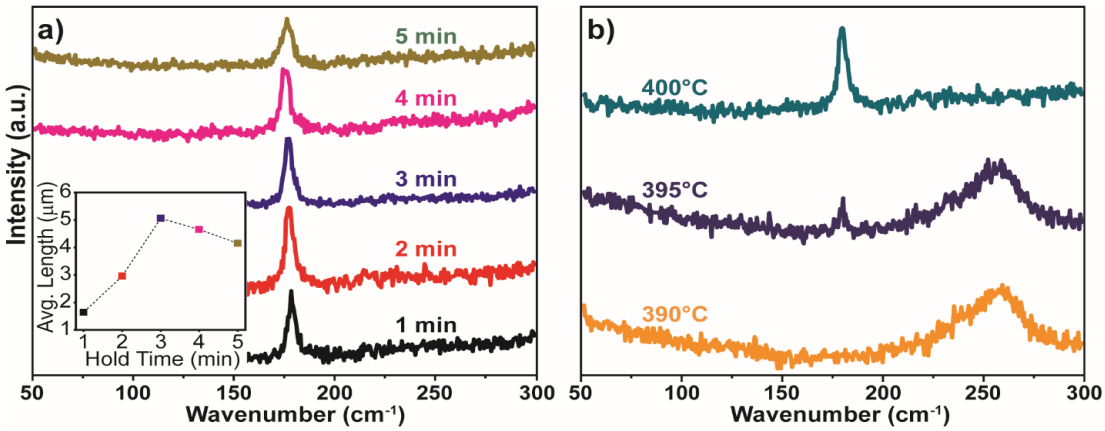


Figure 7.2: a) Raman spectra of $TaSe_3$ nanowire bundles held for different duration at the growth temperature of 400°C. A hold time beyond 3 minutes causes the Raman spectrum to broaden. The inset shows the resulting length distribution peaking at 3 min hold time; b) Nanowire Raman spectra as a function of growth temperature. Starting at 400 °C the desired peak at ~180 cm^{-1} is dominant.

Raman spectroscopy (Horiba Labram HR800, 532 nm wavelength laser, linear polarization, 0.8 mW of laser power on sample) was used to characterize the nanowire bundles grown at hold times varying from 1 to 5 minutes (Fig. 7.2a) at 400°C. The feature at ~180 cm^{-1} is typically referred to as B2 or B2/Ag in the

literature. In addition, if we align the plane of polarization of the Raman excitation perpendicular to the nanowires, we find a second, weaker mode at ~ 215 cm^{-1}. This peak in the literature referred to as another A1g mode. Computational modeling of the phonon spectrum and the associate atom displacement suggest that the dominant mode in Fig. 7.2a is associated with axial wagging of the selenium trimer with regards to the Ta atom and the peak at ~ 215 cm^{-1} with the symmetric and asymmetric stretch motion of the Se atoms in the trimer. The supporting information provide angle-dependent Raman spectra and graphic representations of the modes. The supporting while nanorods were formed in each instance, up to ~3 minutes hold produced the nanowires with the sharpest Raman signature at ~180 cm^{-1}; longer hold is associated with a broadening of the Raman mode by a higher energy shoulder. The supporting material shows a table of the fit parameters of the spectra. Determining the average length of a large set of nanowires generated at each hold time using optical microscopy, we find a maximum wire length at ~3 min hold time (inset in Fig. 7.2a). The supporting material shows histograms. This finding suggests that during the hold time the nanowires do not only form and elongate, but also can decompose, presumably from selenium loss. We studied the Raman spectra of the nanowires as a function of the peak process temperature (Fig. 7.2b) and find that 400°C is the minimum temperature at which nanowires with the desired Raman signature form. The nanowires with the broad spectral feature at ~260 cm^{-1} formed at process temperatures below 400°C exhibit transport properties far inferior to

those nanowires described in the remainder of this manuscript; their precise composition is unknown to us.

In order to be of technological relevance, the $TaSe_3$ 1D vdW nanowires need to be prepared on the scale of a few nanometers in cross section yet significant in length. To this end we evaluated the length to width to height ratios in a population of nanowires. Fig. 7.3a and b show atomic force and scanning electron microscopy (AFM and SEM, respectively) images of the same population of growth seeds and short wires. We obtain the nanowire height from atomic force microscopy yet we use SEM to establish the nanowire width because of the finite size of any AFM tip and associated convolution of tip radius and nanowire width. Fig. 7.3c shows the width-to-height aspect ratio of the nanowires plotted as a function of the nanowire length. Nanowires shorter in length than ~120 nm exhibit ratios between 0.75 and 2.5 which we attribute to the seeding of the growth (gray area). Longer nanowires have an aspect ratio very close to unity: as the axial growth sets in, the nanowires appear to minimize surface area by maintaining a width to height ratio near unity (black markers). Fig. 7.3c includes also a significant number of long nanowires that form the basis of the transport measurements in the next section of this manuscript. The inset shows the dependence of width to height for the black markers of the main panel. The slope is 1.06.

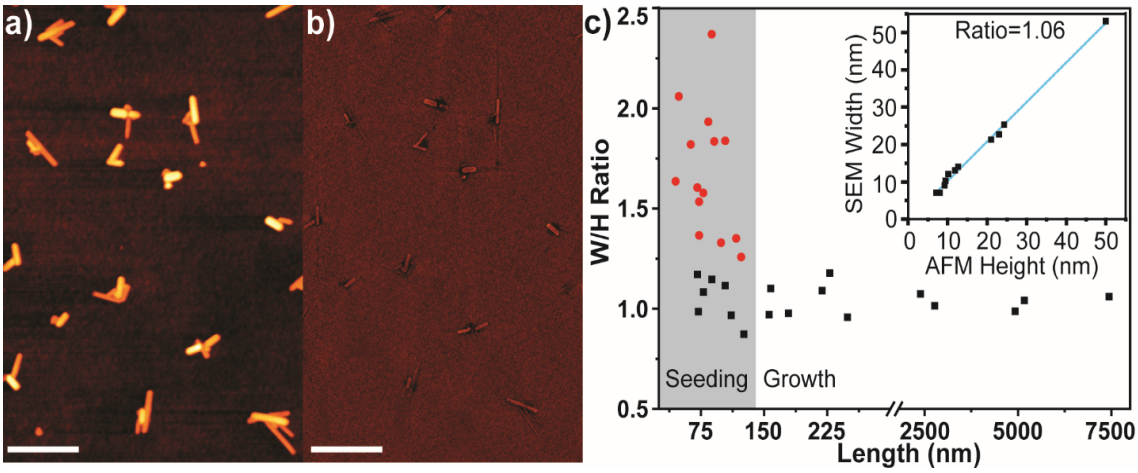


Figure 7.3: a,b) Atomic force microscopy (AFM) and scanning electron microscopy (SEM) images, respectively, of the same population of $TaSe_3$ 1D vdW nanowire bundles (scalebar is 500 nm); c) The width to height ratio of the 1D vdW $TaSe_3$ nanowires at seeding (grey area) and as uniaxial growth continues: longer wires have a width-to-height aspect ratio of practical unity. The inset plots SEM width vs. the AFM height of the wires indicated by black markers in the main panel.

For measurement of the electrical transport properties of the $TaSe_3$ nanowires we employed electron beam lithography (EBL) to fabricate contacts consisting of 5 nm of yttrium for adhesion and 50nm of gold for conduction and stability. Previous studies of $TaSe_3$ nanowires[95, 148, 149] used encapsulation in *h*-BN to avoid surface decomposition by oxygen and moisture from the air. Striving to utilize only scalable methods in our work, we took a different approach: immediately following removal from the process tube, we cap the substrate containing the 1D vdW $TaSe_3$ nanowires with spin-coated polymethyl methacrylate (C5 PMMA) resist under a nitrogen-atmosphere. Subsequently, we characterize the nanowires by Raman spectroscopy through the PMMA film and then use the same resist film to fabricate electrical contacts. Care is taken to

minimize the time between development and metal deposition so as to reduce air exposure of the sample. Immediately following metal liftoff, we again spin coat the sample with a layer of PMMA in a nitrogen glovebox. Subsequently, a second EBL process is performed to remove resist from the surface of the probe pads only. Electrical characterization proceeds in a nitrogen atmosphere.

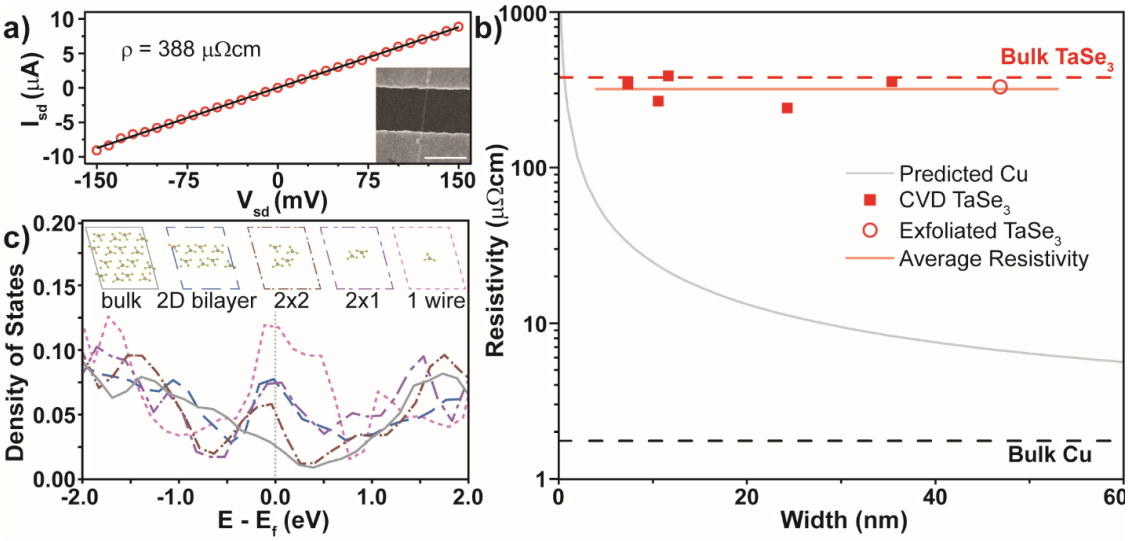


Figure 7.4: a) Source-Drain Current vs. Voltage (I_{sd} vs. V_{sd}) for a 11.6 nm $TaSe_3$ nanowire; a linear dependence is observed in this two-probe measurement that corresponds to the current density shown on the y-axis and the resistivity highlighted. The inset shows an SEM image of a 1D vdW $TaSe_3$ nanowire bridging two electrodes (scalebar is 500 nm); b) resistivity of $TaSe_3$ nanowire bundles with width-to-height aspect ratios near unity (1.0-1.1) as a function of bundle width. For reference, we include bulk values for copper and $TaSe_3$ as dashed lines, as well as a prediction for the scaling of the copper resistivity with wire width based on Ref. [35] The smallest exfoliated nanowire of our prior studies is indicated as open dot. [95, 148, 149] c) Calculated density of states (DOS) near the Fermi level (E_F) for bulk $TaSe_3$, a 2D bilayer of wires, a 2×2 wire bundle, a 2×1 wire bundle and a single wire. The confined wire geometries have higher DOS at E_F than the bulk material suggesting that quantum confinement does not adversely affect charge transport in $TaSe_3$.

Fig. 7.4a shows a typical current-voltage (I-V) diagram measured on a $TaSe_3$ nanowire with width and height of ~11.6 nm each. We use electrodes separated by 500 nm (inset). A linear I-V dependence is observed, from which a resistivity ρ of 388 μΩcm is obtained. The secondary y-axis of Fig. 7.4a shows the corresponding current density *J*.

We tested a large number of nanowires, each time followed by AFM and SEM characterization of their respective width and height. Fig. 7.4b shows the resistivity of wires with width ≤ 50 nm and cross section aspect ratios near unity (1.0-1.1). In a few cases we found wires that exhibited significant non-linear response for small voltage, which we ascribe to contact resistance. These were omitted from Fig. 7.4b. The figure reveals that the specific resistance of 1D vdW $TasSe_3$ nanowires is independent of the cross section of the wire bundle down to 7 nm in width and height. This presents a marked contrast to the behavior of copper at the nanoscale for which Fig. 7.4b includes a reference line based on the work of Steinhogel et al. *[35]* assuming surface *p* and grain boundary *R* scattering amplitudes of 0.5 and 0.6, respectively. At a few nanometer wire width, the resistivity of $TaSe_3$ becomes competitive to that of copper, assuming that a pinhole-free deposition of copper wires is possible at that width scale, which is not immediately apparent.[158]

If scattering does not limit the scaling of the conductivity of $TaSe_3$ nanowires, we explore whether quantum confinement perpendicular to the

nanowire direction may do so. To this end, we assume that the conductivity of a metallic material in first order scales with its density of state (DOS) near the Fermi level (E_F) and calculate the DOS of various nanowire bundle configurations. We employ density functional theory as implemented in the Vienna Ab initio Simulation Package (VASP)[159] using the projector augmented wave method[160, 161] and treating the electron exchange-correlation interaction by the generalized gradient approximation (GGA) functional of Perdew, Burke, and Ernzerhof (PBE).[162] All calculations use periodic boundary conditions and the Brillouin zone was sampled by a 2×7×2 Monkhorst−Pack k-point grid.[163]

Fig. 7.4c compares the density of states (DOS) of an infinite bulk of $TaSe_3$ (solid line) to an infinite 2D bilayer of wires, bundles of 2×2 and 2×1 wires, as well as a single wire. In each case we find considerable DOS near the Fermi level (E_F) and no band gap. Indeed, as the wire bundle is thinned to a bilayer and a finite number of wire stacks, the DOS near E_F increases. This finding suggests that – at least for some wire bundle geometries – a higher native conductivity is possible than for the bulk case. We recognize, however, that this analysis omits fundamental stability limitations (such as the Mermin-Wagner-theorem[164]) yet we note that additional research is necessary to fathom their impact as shown for graphene.[165] The smallest wire bundle for which we obtained transport measurements had a width and height of ~ 7nm (Fig. 7.4b) and thus as few as ~10x10 wires in parallel; it is almost an order of magnitude larger than the computationally readily tractable ones of Fig. 7.4c.

Finally, we turn to the stability of the 1D vdW nanowires with regards to degradation under transport. Measurements of the low-frequency noise are commonly used to assess the quality and reliability of conventional[166-170] and novel 2D materials [92, 95, 150] for device applications. Changes in the noise spectra can serve as a convenient indicator of the onset of electromigration and other material degradation mechanisms. In the context of interconnect research, the low-frequency noise can provide a fast estimate of the device's mean time to failure. The low-frequency noise measurements were performed using an experimental setup consisting of a "quiet" battery, a potentiometer biasing circuit, a low noise amplifier, and a spectrum analyzer; additional details have been reported elsewhere.[97, 171]

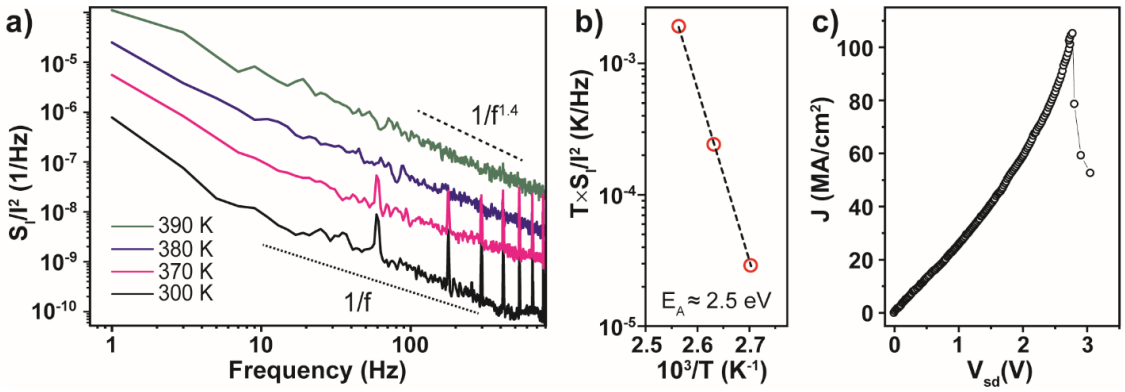


Figure 7.5: a) Normalized current noise spectral density of a ~10×10 nm^2 (width × height) CVD 1D vdW $TaSe_3$ nanowire bundle at different temperatures T using a source-drain voltage V_{sd} of 0.1 V. b) Arrhenius plot of $T \times S_I/I^2$ vs. 1000/T for a frequency f of 11 Hz. The extracted activation energy E_A is 2.57 eV. c) Current density J response of a ~7×7 nm^2 nanowire as the voltage is slowly increased. Failure occurs at a current density in excess of 10^8 A/cm^2.

Figure 7.5a shows the normalized current noise spectral density S_I/I^2 as a function of frequency f for a $TaSe_3$ nanowire with a cross-section of ~ 10×10 nm^2. The noise level S_I/I^2 of ~10^{-8} Hz^{-1} at f=10 Hz and T=300K in the downscaled CVD $TaSe_3$ nanowires is appreciably low. Although it is higher than measured in conventional metals[172, 173] and also for larger cross section exfoliated $TaSe_3$ nanowires,[95, 173] the latter is expected because the noise originating from a volume of independent fluctuators scales inversely proportional to the size of the volume.[166] Indeed, one can write for the noise spectral density[166-168] $S_I/I^2=\alpha_H/Nf$, where α_H is the coefficient of proportionality referred to as the Hooge parameter, and $N=n\times V$, where n is the concentration of the charge carriers and V is the volume of the sample. The noise levels of 10^{-9} Hz^{-1} – 10^{-5} Hz^{-1} are found in conventional transistors and other electronic devices.[168]

Fig. 7.5a reveals increase in the noise level with increasing temperature. The informative frequency range from 10 Hz to ~400 Hz exhibits a deviation from pure 1/f noise; approximately $1/f^{1.4}$ provides the best fit at elevated temperatures. This trend is consistent with observations on thicker exfoliated $TaSe_3$ nanowires.[95] In metals the deviation from 1/f-type behavior is commonly attributed to the onset of electromigration. We construct an Arrhenius plot of $T\times S_I/I^2$ vs. 1000/T (Fig. 7.5b) to extract the activation energy (E_A) for the noise inducing process in CVD 1D vdW $TaSe_3$ nanowires. The resultant value of ~2.5 eV is larger than that for exfoliated $TaSe_3$ nanowires[95] and more than twice that for electromigration in copper (0.76-1.10 eV) and aluminum (0.67- 1.14 eV)

using similar measurements.[169, 170, 173, 174] This finding suggests very good resistance of CVD $TaSe_3$ 1D vdW nanowire to electromigration.

The electromigration resilience of the CVD 1D vdW $TaSe_3$ nanowires is confirmed by successively increasing the voltage applied to a 7×7 nm^2 wire bundle (about 100 parallel Ta-Se_3 stacks in total). Fig. 7.5c shows that the wire bundle was able to sustain in excess of 10^8 A/cm^2 before electrical breakdown. This current density is an order of magnitude higher than that found for thicker, exfoliated $TaSe_3$, and also slightly better than our previous findings for $ZrTe_3$.[150] We note that acquiring the dataset of Fig. 7.5c took almost an hour of slowly increasing the bias, so that self-heating may have contributed to reduced overall current carrying capacity and increased susceptibility to electromigration. Embedding the nanowire with a better thermal sink than the underlying SiO_2 substrate and the surrounding PMMA resist may result in even higher sustained current densities.

Summary

In conclusion, we find that chemical vapor deposition allows the growth of $TaSe_3$ nanowires on a SiO_2 substrate that are competitive in resistivity to conventional metals scaled to sub-10-nanometer wire diameters, while offering significantly enhanced electromigration resilience and breakdown current. The growth proceeds at back-end-of-the-line compatible temperatures (~ 400°C) and

because it takes just a few minutes, it has a comparatively low thermal budget impact. Future work will adapt prior findings on the spatially-selective growth of TMD materials[175-178] so as to generate the $TaSe_3$ nanowires not randomly dispersed on the sample but at desired locations only.

Chapter 8: Rapid Chemical Vapor Deposition of Metallic $ZrTe_3$ Nanoribbons on a SiO_2 Wafer Substrate

The following is taken from an article being written[179] in collaboration between myself, and other students: Jing Jin, Saba Seyedmahmoudbaraghani, Daniel J. Coyle and Thomas Empante of Ludwig Bartels, Alexander Balandin, and Fariborz Kargar.

Abstract

Chemical Vapor Deposition (CVD) growth of quasi-1-dimensional zirconium tritelluride ($ZrTe_3$) at temperatures below 600℃ and process times under an hour results in material on a SiO_2/Si wafer substrate that offers electrical conductivity comparable to the bulk. This study combines tailored CVD processing using a tube-in-a-tube technique with characterization by optical microscopy, Raman spectroscopy and scanning electron microscopy (SEM). Transmission electron microscopy (TEM) validates the composition and offers atomic contrast. Electrical transport measurements employ an yttrium-gold stack to achieve good adhesion and low contact resistance. A positive temperature coefficient is observed, as expected for metallic material.

Introduction

The continued progress of miniaturization of microelectronic devices provides materials and fabrication challenges pertaining not only to the active semiconducting region of the transistors, but also to the electrical leads, interconnects, wiring them up. Finer and finer wires have higher and higher surface to volume ratio resulting in greater resistance originating from surface and grain-boundary scattering of electrons. Copper has been the material of choice for the past two decades for interconnects in high-end semiconductor devices. Because of its very long mean free path for electrons, 40 nm,[33, 34] it is very susceptible to electron surface scattering and exhibits substantially higher resistance at current sub-20nm interconnect cross section. In contrast, the resistivity of materials that do not rely on long mean free path for excellent conductivity, such as cobalt and ruthenium, are less affected by surface scattering; recent work at Intel and elsewhere transitioned away from interconnects made from copper for that reason.[156, 180] Alternate contact materials such as cobalt[181] and ruthenium[182-184] trade inferior bulk conductivity against reduce surface scattering. They offer also new process challenges: for instance, because of their refractory nature, annealing to mitigate the effect of grain boundaries is more difficult. Metallic 1-dimensional (1D) or quasi-1D materials may attain an important role in future nanoscale devices because their van der Waals (vdW) gap between adjacent wires in a bundle

natively shields electrical transport along their main axis from surface scattering, thus, avoiding the problem inherent to elemental metals and their alloys. Indeed, in a past study[36] we have shown that $TaSe_3$ wire conductivity is not affected by surface scattering down to the minimal wire cross section we could produce (7nm). However,1D materials will only be of technological utility if they a) have a sufficiently low native resistivity and b) can be deposited on an oxide surface using chemical vapor deposition (CVD) or related techniques at both low enough temperatures and short enough process times.

1D and quasi-1D vdW materials have long been studied for the charge density waves they support.[185-190] Recently, increased interest has been attracted by them and a multitude of $MX_{3...5}$ (M: transition metal such as Ta,[36] Zr,[187, 191-197] Nb[186, 198]; X chalcogen: S, Se, Te) have been synthesized for electronic,[36, 149, 150, 199, 200] magnetic,[191, 194, 195] superconducting[186, 189, 193, 196, 197, 201, 202] and optical[187, 192] characterization. In this study, we build on our prior work on $TaSe_3$ CVD[36] and develop a tailored technique to provide access to $ZrTe_3$ on SiO_2 substrates – simple transference of the growth technique developed for $TaSe_3$ does not lead to $ZrTe_3$ growth. Bulk $ZrTe_3$ has a better conductivity[200] than $TaSe_3$; this was also found in a number of studies on exfoliated microscopic flakes.[95, 149, 150] While selenium and tellurium share many chemical properties as both chalcogens and metalloids, their ease of activation is quite different, with tellurium typically requiring higher temperatures or more time. Conventionally,

$ZrTe_3$ crystals have been grown using chemical vapor transport (CVT) techniques, in which zirconium and tellurium precursors are allowed to react over days or weeks in the presence of a transport agent (e.g., iodine) to form large crystallites of the desired material. Derived from that approach, Yu et al.[191] showed in an impressive study a CVD technique, which provided high-quality samples by requiring in excess of 600℃ process temperature and hold times on the order of an hour. Here we focused on reducing hold time and temperature so as to better comply to thermal budget requirements; in particular, we show how $ZrTe_3$ crystallites can be grown *in situ* on SiO_2 at process temperature well below 600 °C and process times well below 1 hour. The resultant nano- and micron-scale material is highly-crystalline and feature metallic conductivity (e.g., positive temperature coefficient of resistivity, bulk-like high conductivity).

A key challenge in the development of CVD growth methods of 1D nanomaterials is the identification and characterization of the product material. This is particularly the case when working with tellurium, because elemental tellurium also forms 1D structures.[203-206] To guide future practitioners, we also characterized the tellurium nanowire biproducts that form when the process conditions are slightly off. Raman modes overlapping with $ZrTe_3$ provide challenges here that are best resolved by rotating the polarization axis of the incoming laser relative to the wire axis. This study offers a combination of tailored CVD process conditions and thorough characterization of the resultant material

including polarization-dependent Raman spectroscopy and temperature-dependent transport measurements.

Results and Discussion

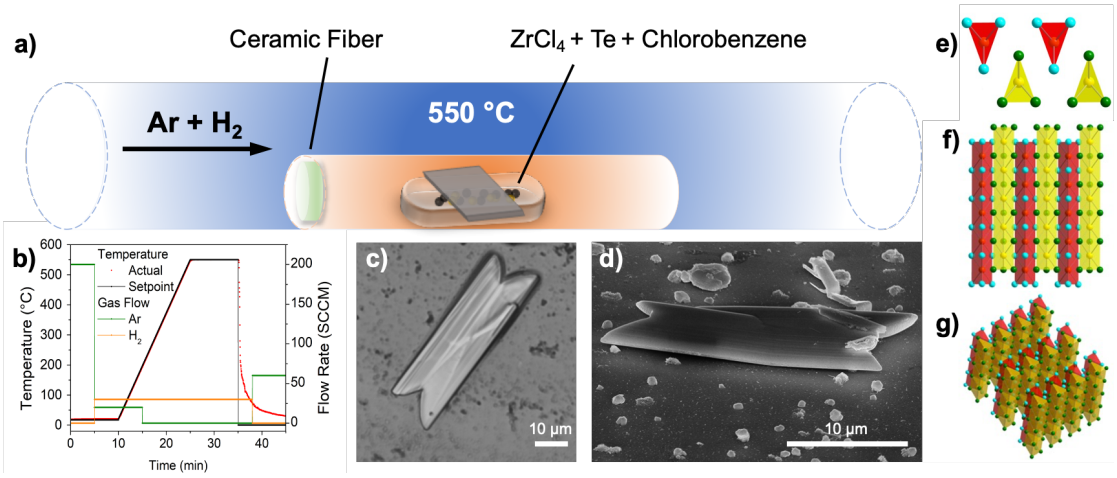


Fig. 8.1: (a) schematic representation of the CVD growth setup consisting of a process tube housing a test tube stoppered by a bale of porous ceramic fiber. Inside the test tube growth precursors are placed inside an alumina boat and the growth substrate on top. (b) temperature and gas profile during the growth. The hold time is 10 min. (c) optical image of a ZrTe3 crystallite grown on SiO_2/Si. SEM image of a $ZrTe_3$ crystallite obtained at 60 degree tilt of the gun. (e-g) crystallographic structure of $ZrTe_3$ plotted from different angles.

Fig. 8.1a provides a schematic representation of the growth setup using a clamshell-type tube furnace with a 2” process tube. We use elemental tellurium powder (99.8%, Sigma-Aldrich) and zirconium tetrachloride (99.9%, Sigma-Aldrich) as tellurium and zircon precursors, respectively. To increase the chemical potential of tellurium at the CVD growth location, we place a 0.5 inch test tube (with closed end) inside the 2 inch process tube. The open end of the

test tube (facing upstream) is constricted with ceramic fiber wool. Inside the test tube, we place a 1ml alumina boat (Coors) filled with a mixture of both precursors homogenized by stirring in chlorobenzene prior to growth. The wafer substrate is placed directly atop the boat.

Fig. 8.1 b shows the temperature and process gas transients as applied here. Argon is used for purging and the CVD proceeds in a hydrogen atmosphere. Hydrogen serves two purposes: providing a reducing atmosphere to prevent oxidation of the species and, importantly, much improved thermal conductivity compared to argon or nitrogen resulting in more rapid thermal transients at the sample location. These are also visible from the good compliance of the temperature trace to the setpoint temperature.

Following growth, so as to shield the samples from oxygen in air, we covered them immediately in a ~500 nm thick layer of PMMA (polymethyl methacrylate) resist (MicroChem); care was taken to reduce the oxygen dissolved in the PMMA by keeping it consistently in a nitrogen-filled glove box. All spectroscopic studies and optical imaging were performed through that PMMA layer; this layer was also used for subsequent lithographic processing.

Fig. 8.1c shows an optical image of a representative $ZrTe_3$ crystallite several tens of microns long. These crystallites exhibit a metallic sheen and are very reflective in optical images. ZrTe3 crystallites typically appear as two trapezoids attached at their shorter sides.

Scanning electron microscopy (SEM) provides higher resolution imagery of the $ZrTe_3$ crystallites grown on the oxide substrate. Fig. 8.1d show a tilted (60^o) view of one of the larger $ZrTe_3$ crystallites. Practically all of them grow in this double trapezoid shape, which we tentatively attribute to a dislocation at the center of the crystallite. Yu et al. observed similar shapes.[191] As a result, only one side of the islands lies flush on the substrate, whereas the other is lifted up. Depending on the hold duration during growth, we observe these crystallites to grow tens of micrometers in the long axis; shorter crystallites are obtained at shorter growth duration.

The crystallographic structure of monoclinic $ZrTe_3$ is depicted in Figs. 8.1e-g. Two of the $ZrTe_3$ formula units compose a unit cell of the crystal. The vertical rods in panel f are the direction of high conductivity; these colored rods represent the quasi-1D wires of this material. They assemble in sheets, which in turn stack to make up the bulk. The geometric data underlying this plot was obtained from the Materials Project database.[207]

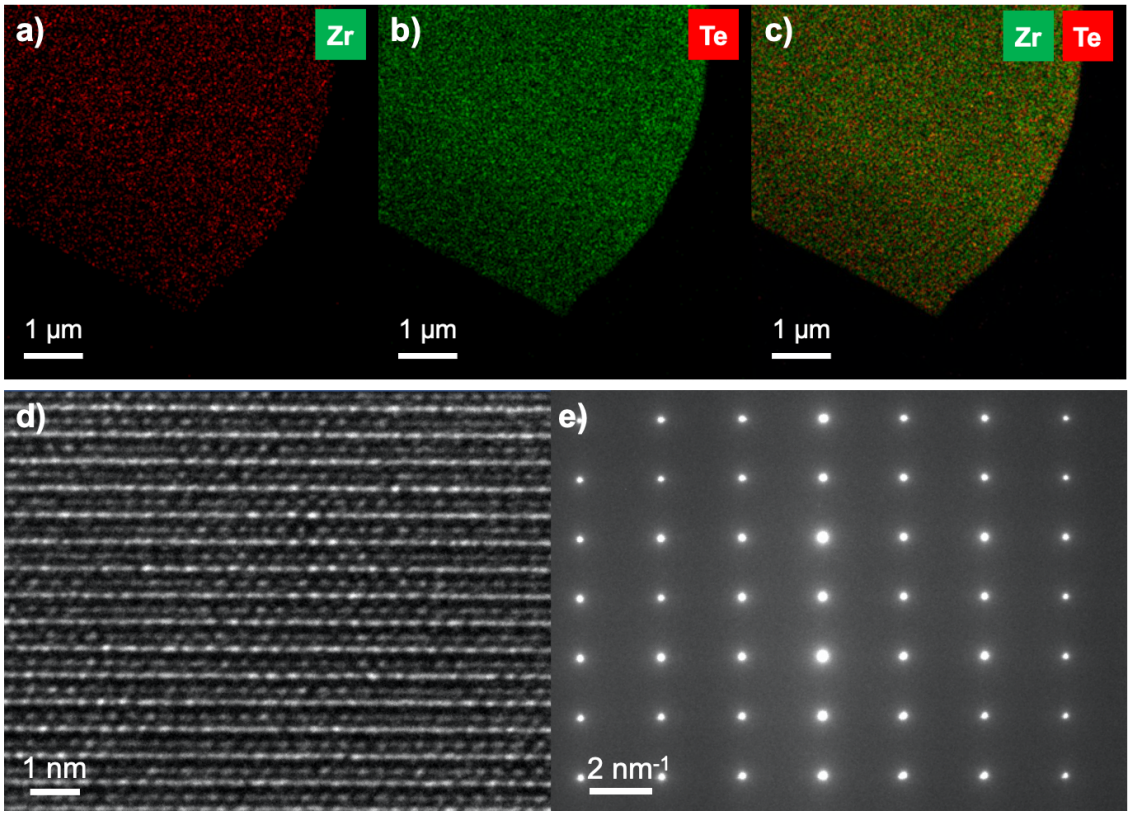


Figure 8.2: a-c) EDX images of a $ZrTe_3$ nanocrystallite confirming the composition of the material; d) HAADF image of the atomic structures of the $ZrTe_3$ crystallites; e) local diffraction confirming the arrangement of the material in the monoclinic structure shown in Fig. 8.1e-g.

Figure 8.2 shows transmission electron microscopy (TEM) data obtained on a $ZrTe_3$ crystallite after transferring it onto a lacey carbon coated 300 mesh copper TEM grid by first scraping the crystallites with a tungsten needle off the substrate and then catching the resultant particles from distilled water. Panels a-c) show elemental maps obtained by energy dispersive X-ray spectroscopy (EDX) that confirm the crystallites to consist of zirconium and tellurium.

Quantitative evaluation of the emitted x-rays is consistent with the 1:3 composition of the material.

High angle annular dark field (HAADF) imaging reveals the atomic setup of the $ZrTe_3$ nanowires (Fig. 8.2d); the atomic rows visible in the figure are aligned with the long axis of the crystallites. Electron diffraction (Fig. 8.2e) in these areas results in a pattern consistent with the monoclinic structure of $ZrTe_3$.

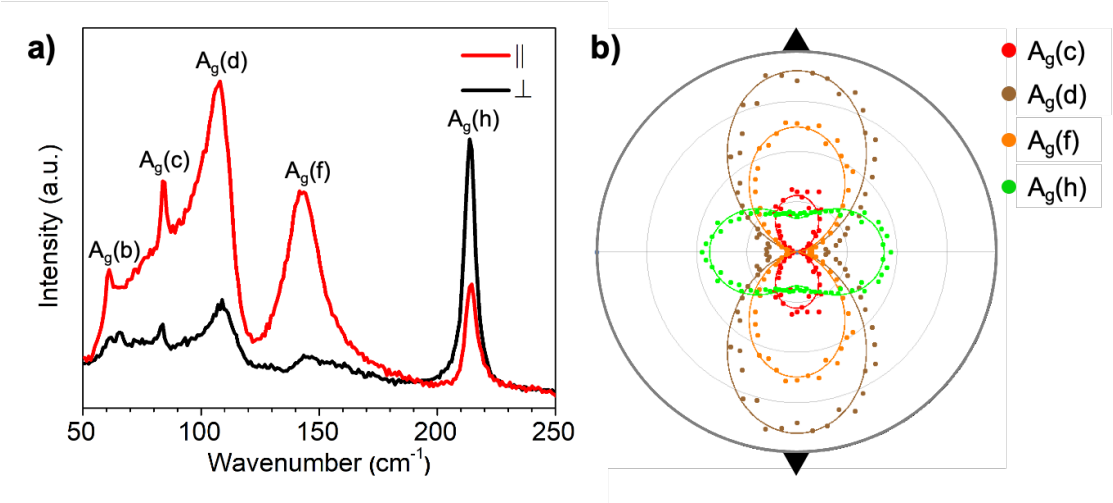


Figure 8.3 a) Raman spectra with the excitation laser aligned parallel (red) and perpendicular (black) to the ZrTe3 nanowire long axis. The mode assignment is based on Ref: [187] b) polar plot of the angular intensity variation of the Raman peaks of panel a) and associate fit curve. The nanowire direction is indicated by the marks on top and bottom of the plot.

Further characterization of the material involved Raman spectroscopy using a Horiba Labram HR800 instrument with 0.8mW of 532 nm wavelength laser light applied to the sample. We readily noticed great variation of the spectra depending on the orientation of the plane of polarization with respect to the crystallographic axis of the islands. Fig. 8.3a shows two spectra with the polarization of the excitation laser parallel and perpendicular to the long axis of the 1D wire. The A_g(c), A_g(d), A_g(f), and A_g(h) modes are found at 84 cm^{-1}, 113 cm^{-1}, 138 cm^{-1}, 214 cm^{-1}, respectively. The labeling of the modes in Fig 8.3a follows the work by Hu et al.[187] Panel 3b shows a polar plot of the strongest modes of the Raman spectrum. The angular dependence of the A_g(c), A_g(d), and A_g(f) modes is well represented by a $\sin^2$ fit. The Ag(h) mode was fitted by a superposition of two orthogonal $\sin^2$ dependences. The numerical fit suggests a ~1cm^{-1} shift between two modes making up this peak.. Hu et al.[187] also observed the presence of the 215 cm^{-1} in both polarization directions and attributed it to defects.

To ascertain the electrical transport properties of the CVD material grown in-situ on SiO_2, we fabricated 4 terminal devices on their side (we deposited 5 terminals, in case one of them would have a fabrication problem). Only the contacts applied to one side of each crystallite offer electrical connectivity, those on the opposite side are not connected to the leads because that side of the crystallite is lifted up (Fig. 8.1d).

Device fabrication employs the PMMA layer that was initially deposited as an oxidation barrier for the first lithographic step. Electron beam lithography was used to define pads, leads and contacts to the crystallites. Within minutes after development, we deposited an adhesion layer of 10 nm of yttrium followed by 300 nm of gold at pressures better than 1×10^{-6} torr. Rapid deposition of this contact layer is crucial to avoid excessive contact resistance. Subsequently, the sample was sealed again in a PMMA layer. In a second lithographic step, the PMMA was removed from the contact pads. Electrical characterization proceeded in a probe station under nitrogen atmosphere.

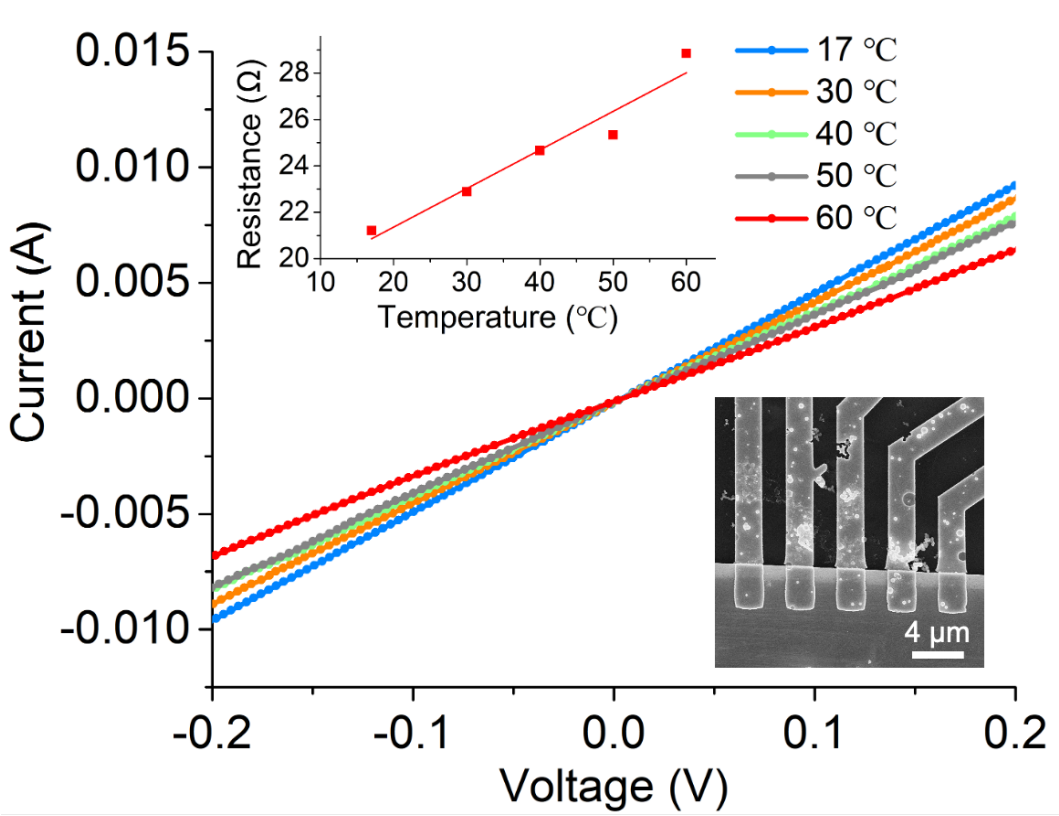


Figure 8.4: Electrical transport of a $ZrTe_3$ crystallite. A linear I-V relationship at 21 Ω is observed at room temperature (17℃). The bottom inset shows an SEM image of the device with a channel length of 1.9μm, width of 2.9μm and depth of 0.7μm. The top inset shows how the nanowire resistance increases with temperature, as expected for a metal.

Four-point measurements employed a Keithlyer 2400 sourcemeter operated in voltage control to apply a current between the two inner of the four electrodes in a row. To each of the outside electrodes, a Keithley 6517 electrometer is connected. Plotting the current versus the voltage difference between the electrometers generates the I-V plot of Fig 8.4 and eliminates contact (and lead) resistance from the $ZrTe_3$ nanowire resistance. A linear

relationship indicative of a metallic material is observed; the resistance at room temperature (17℃) is 21 Ohm.

Comparing the electrometer voltages to the sourcemeter voltage, we find a combined lead and contact resistance of typically ~10 Ohm. This comparatively low value is a result of optimizing the yttrium adhesion layer deposition. Attributing the entire resistance to contact resistances, an upper limit of the contact resistance of 1×10^{-6} Ω×cm^2 is found.

If we assume that the entire bulk of the material between the electrodes contributes equally to the conduction, then a resistivity ρ^o at 17℃ of $\frac{21\Omega\times0.7\mu m\times2.9\mu m}{1.9\mu m} = 2.3m\Omega\times cm$ results for a film thickness of 0.7 micron, an electrode width of 2.9 microns and an electrode separation of 1.9 microns. The actual resistivity is expected to be lower because only a thin sheet and not the entire volume of the material contributes to the transport in reality. A simulation in COMSOL assuming isotropic resistivity and contact both at the side wall and the top of the crystallites suggests a value 1.7 mΩ×cm. As such, the conductivity approaches the bulk one within an order of magnitude.[200] The remaining deviation is attributed to our assumption of isotropic resistivity and scattering on the nanowire surface.

Fitting temperature-dependent transport measurements to a linear model of the resistivity ρ(T+ΔT) = ρ^o (1 + c ×ΔT) reveals a positive temperature (*T*)

coefficient *c* of 0.0056 1/K. To our knowledge, this is the first time that a positive temperature coefficient was directly measured on a 1D vdW nanomaterial other than carbon nanotubes.

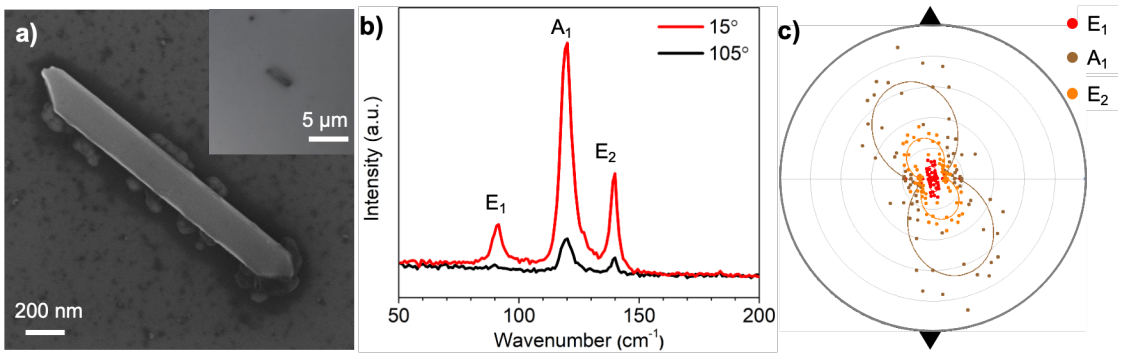


Figure 8.5: a) SEM image of a tellurium nanowire; the inset shows an optical image. b) Raman spectrum on the tellurium nanowire and c) polar plot of the peak intensity. The highest intensity is found at ~15º angle between the long axis of the nanowire and the plane of polarization of the excitation laser. The modes are labeled according to Ref: [206]

Preparing $ZrTe_3$ nanocrystallites on SiO_2, we frequently observe nanowires that look quite similar but do not offer appreciable conductivity. We identified them as elemental tellurium nanowires.[203-206] To guide anyone seeking to reproduce our work, we provide their characterization in Fig. 8.5 as they are easily mistaken for $ZrTe_3$ nanowires both because of their geometry and overlapping Raman modes. Fig. 8.5a shows the SEM (and as inset the optical) image of such a Te crystallite. The Te-nanowires typically have a (single) trapezoid shape and not a double trapezoid shape as the $ZrTe_3$.

The Raman modes of this material partially overlap with that of $ZrTe_3$; the most reliable identification involves measuring the angular dependence of Raman modes, where the maximum of the Raman response is found to be not aligned with but at an angle of 15^o to the tellurium nanowire direction.

Summary

In conclusion, we find that ZrTe3 nanocrystallites can be grown by CVD in a rapid process on SiO2/Si using inexpensive zirconium-(IV)-chloride and tellurium as reactants. The process yields material of high crystallinity and sufficient size for electronic processes; its electrical conductivity is comparable to the bulk. This effort brings the realization of 1D vdW material as interconnects in electronic devices one step closer.

References

1. Zhao, L.Y., et al., *Visualizing Individual Nitrogen Dopants in Monolayer Graphene.* Science, 2011. **333**(6045): p. 999-1003.
2. Ohta, T., *Photochemical and Photoelectrochemical Hydrogen-Production from Water.* International Journal of Hydrogen Energy, 1988. **13**(6): p. 333-339.
3. Qi, H.J., et al., *Nickel and manganese co-modified K/MoS_2 catalyst: high performance for higher alcohols synthesis from CO hydrogenation.* Catalysis Communications, 2003. **4**(7): p. 339-342.
4. Chen, P., et al., *Single-nanoparticle catalysis at single-turnover resolution.* Chemical Physics Letters, 2009. **470**(4-6): p. 151-157.
5. Chen, P., et al., *Single-molecule fluorescence imaging of nanocatalytic processes.* Chemical Society Reviews, 2010. **39**(12): p. 4560-4570.
6. Mills, G.A., *Summary of the Higher Alcohols Synthesis Workshop*. 1992: B. R. Service Corporation.
7. Li, H., et al., *Fabrication of Single- and Multilayer MoS2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature.* Small, 2012. **8**(1): p. 63-67.
8. Yin, Z., et al., *Single-Layer MoS_2 Phototransistors.* Acs Nano, 2011. **6**(1): p. 74-80.
9. Ayari, A., et al., *Realization and electrical characterization of ultrathin crystals of layered transition-metal dichalcogenides.* JOURNAL OF APPLIED PHYSICS, 2007. **101**(1): p. 014507-5.
10. Smith, K.J. and R.B. Anderson, *A Chain Growth Scheme for the Higher Alcohols Synthesis.* Journal of Catalysis, 1984. **85**(2): p. 428-436.
11. Xu, R., et al., *Influence of promoter on catalytic properties of Cu-Mn-Fe/ZrO_2 catalysts for alcohols synthesis.* Reaction Kinetics and Catalysis Letters, 2004. **81**(1): p. 91-98.
12. Zhao, N., et al., *Cu/Mn/ZrO_2 catalyst for alcohol synthesis by Fischer-Tropsch modified elements.* Reaction Kinetics and Catalysis Letters, 2002. **75**(2): p. 297-304.
13. Chu, W., et al., *Conversion of Syngas to C1-C6 Alcohol Mixtures on Promoted Cula2zr2o7 Catalysts.* Applied Catalysis a-General, 1995. **121**(1): p. 95-111.
14. Cao, T., et al., *MoS2 as an ideal material for valleytronics: valley-selective circular dichroism and valley Hall effect.* Arxiv:1112.4013, 2012.
15. Muramatsu, A., T. Tatsumi, and H.O. Tominaga, *Active Species of Molybdenum for Alcohol Synthesis from Co-H2.* Journal of Physical Chemistry, 1992. **96**(3): p. 1334-1340.
16. Esterling, K.M., M.A. Neblo, and D.M.J. Lazer, *Estimating Treatment Effects in the Presence of Selection on Unobservables: The Generalized Endogenous Treatment Model.* Political Analysis, 2011. **19**: p. 205-226.

17. Li, X.G., et al., *Higher alcohols from synthesis gas using carbon-supported doped molybdenum-based catalysts.* Industrial & Engineering Chemistry Research, 1998. **37**(10): p. 3853-3863.

18. Nielsen, L.P., et al., *Combined TPS, XPS, EXAFS, and NO-TPD study of the sulfiding of Mo/Al_2O_3* Catalysis Letters, 2001. **73**(2-4): p. 85-90.

19. Helveg, S., et al., *Atomic-scale structure of single-layer MoS_2 nanoclusters.* Physical Review Letters, 2000. **84**(5): p. 951-954.

20. Shen, H., W.L. Xu, and P. Chen, *Single-molecule nanoscale electrocatalysis.* Physical Chemistry Chemical Physics, 2010. **12**(25): p. 6555-6563.

21. Maxwell, I.E., *Driving forces for innovation in applied catalysis.* 11th International Congress on Catalysis - 40th Anniversary, 1996. **101**: p. 1-9.

22. Lehn, J.M., J.P. Sauvage, and R. Ziessel, *Photochemical Water Splitting Continuous Generation of Hydrogen and Oxygen by Irradiation of Aqueous Suspensions of Metal Loaded Strontium-Titanate.* Nouveau Journal De Chimie-New Journal of Chemistry, 1980. **4**(11): p. 623-627.

23. Butler, S.Z., et al., *Progress, challenges, and opportunities in two-dimensional materials beyond graphene.* ACS Nano, 2013. **7**(4): p. 2898-926.

24. Choi, W., et al., *Recent development of two-dimensional transition metal dichalcogenides and their applications.* Materials Today, 2017. **20**(3): p. 116-130.

25. Bhimanapati, G.R., et al., *Recent Advances in Two-Dimensional Materials beyond Graphene.* Acs Nano, 2015. **9**(12): p. 11509-11539.

26. Ozcelik, V.O., et al., *Band alignment of two-dimensional semiconductors for designing heterostructures with momentum space matching.* Physical Review B, 2016. **94**(3): p. 035125.

27. Mak, K.F., et al., *Atomically thin MoS_2: a new direct-gap semiconductor.* Physical Review Letters, 2010. **105**(13): p. 136805.

28. Splendiani, A., et al., *Emerging photoluminescence in monolayer MoS_2* Nano Letters, 2010. **10**(4): p. 1271-1275.

29. Mak, K.F., et al., *Control of valley polarization in monolayer MoS_2 by optical helicity.* Nature Nanotechnology, 2012. **7**(8): p. 494-498.

30. Cao, T., et al., *Valley-selective circular dichroism of monolayer molybdenum disulphide.* Nature Communications, 2012. **3**: p. 887.

31. White, R.M. and F.W. Voltmer, *Direct Piezoelectric Coupling to Surface Elastic Waves.* Applied Physics Letters, 1965. **7**(12): p. 314-&.

32. Reindl, L.M., et al., *SAW-Based Radio Sensor Systems.* Ieee Sensors Journal, 2001. **1**(1): p. 69-78.

33. Gall, D., *Electron mean free path in elemental metals.* Journal of Applied Physics, 2016. **119**(8): p. 085101.

34. Steinhogl, W., et al., *Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller.* Journal of Applied Physics, 2005. **97**(2): p. 023706

35. Steinhogl, W., et al., *Size-dependent resistivity of metallic wires in the mesoscopic range.* Physical Review B, 2002. **66**(7).

36. Empante, T.A., et al., *Low Resistivity and High Breakdown Current Density of 10 nm Diameter van der Waals $TaSe_3$ Nanowires by Chemical Vapor Deposition.* Nano Letters, 2019. **19**(7): p. 4355-4361.

37. Li, B.Z., et al., *Reliability challenges for copper interconnects.* Microelectronics Reliability, 2004. **44**(3): p. 365-380.

38. Lloyd, J.R. and J.J. Clement, *Electromigration damage due to copper depletion in Al/Cu alloy conductors.* Applied Physics Letters, 1996. **69**(17): p. 2486-2488.

39. Hu, C.K., et al., *Copper Interconnection Integration and Reliability.* Thin Solid Films, 1995. **262**(1-2): p. 84-92.

40. Kapur, P., et al., *Technology and reliability constrained future copper interconnects - Part II: Performance implications.* Ieee Transactions on Electron Devices, 2002. **49**(4): p. 598-604.

41. Chang, T.H.P., *Proximity Effect in Electron-Beam Lithography.* Journal of Vacuum Science & Technology, 1975. **12**(6): p. 1271-1275.

42. Owen, G., *Methods for Proximity Effect Correction in Electron Lithography.* Journal of Vacuum Science & Technology B, 1990. **8**(6): p. 1889-1892.

43. Mann, J., et al., *Facile growth of sub-millimeter scale monolayer MoS_2 films on SiO_2/Si.* European Physical Journal B, 2013. **86**: p. 226.

44. Zhang, Y., et al., *Ambipolar MoS2 Thin Flake Transistors.* NANO LETTERS, 2012. **12**(3): p. 1136-1140.

45. Maeda, K., et al., *GaN : ZnO solid solution as a photocatalyst for visible-light-driven overall water splitting.* Journal of the American Chemical Society, 2005. **127**(23): p. 8286-8287.

46. Vilfan, I., *Mo6S6 nanowires: structural, mechanical and electronic properties.* The European Physical Journal B - Condensed Matter and Complex Systems, 2006. **51**(2): p. 277-284.

47. Sun, D., et al., *An MoS_x Structure with High Affinity for Adsorbate Interaction.* Angewandte Chemie, 2012. **124**(41): p. 10430-10434.

48. Zhou, X.C., et al., *Size-Dependent Catalytic Activity and Dynamics of Gold Nanoparticles at the Single-Molecule Level.* Journal of the American Chemical Society, 2010. **132**(1): p. 138-146.

49. Robinson, J.T., et al., *Electronic Hybridization of Large-Area Stacked Graphene Films.* Acs Nano, 2013. **7**(1): p. 637–644.

50. Fujishima, A. and K. Honda, *Electrochemical Photolysis of Water at a Semiconductor Electrode.* Nature, 1972. **238**(5358): p. 37-+.

51. Li, X.G., et al., *Alcohol synthesis over pre-reduced activated carbon-supported molybdenum-based catalysts.* Molecules, 2003. **8**(1): p. 13-30.

52. Ochoa, M.A., et al., *Interpreting single turnover catalysis measurements with constrained mean dwell times.* Journal of Chemical Physics, 2011. **135**(17).

53. Sato, S. and J.M. White, *Photo-Decomposition of Water over P-TiO_2 Catalysts.* Chemical Physics Letters, 1980. **72**(1): p. 83-86.

54. Almeida, K., et al., *High-Vacuum Particulate-Free Deposition of Wafer-Scale Mono-, Bi-, and Trilayer Molybdenum Disulfide with Superior Transport Properties.* ACS Appl Mater Interfaces, 2018. **10**(39): p. 33457-33463.

55. Sarkar, D., et al., *A subthermionic tunnel field-effect transistor with an atomically thin channel.* Nature, 2015. **526**(7571): p. 91-95.

56. Jiang, C., et al., *High-temperature performance of MoS_2 thin-film transistors: Direct current and pulse current-voltage characteristics.* Journal of Applied Physics, 2015. **117**(6): p. 64301.

57. Samnakay, R., et al., *Selective chemical vapor sensing with few-layer MoS2 thin-film transistors: Comparison with graphene devices.* Applied Physics Letters, 2015. **106**(2): p. 23115.

58. Liu, G., et al., *Selective Gas Sensing With h-BN Capped MoS2 Heterostructure Thin-Film Transistors.* Ieee Electron Device Letters, 2015. **36**(11): p. 1202-1204.

59. Lee, Y.-H., et al., *Synthesis of Large-Area MoS_2 Atomic Layers with Chemical Vapor Deposition.* ADVANCED MATERIALS, 2012. **24**: p. 2320-2325.

60. Najmaei, S., et al., *Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers.* Nature Materials, 2013. **12**(8): p. 754-759.

61. Ling, X., et al., *Role of the seeding promoter in MoS_2 growth by chemical vapor deposition.* Nano Lett, 2014. **14**(2): p. 464-72.

62. Shaw, J.C., et al., *Chemical vapor deposition growth of monolayer MoSe2 nanosheets.* Nano Research, 2014. **7**(4): p. 511-517.

63. Tongay, S., et al., *Tuning Interlayer Coupling in Large-Area Heterostructures with CVD-Grown MoS2 and WS2 Monolayers.* Nano Letters, 2014. **14**(6): p. 3185-3190.

64. Dumcenco, D., et al., *Large-Area Epitaxial Monolayer MoS_2.* Acs Nano, 2015. **9**(4): p. 4611-4620.

65. Velusamy, D.B., et al., *Flexible transition metal dichalcogenide nanosheets for band-selective photodetection.* Nature Communications, 2015. **6**: p. 8063

66. Kappera, R., et al., *Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors.* Nature Materials, 2014. **13**: p. 1128–1134.

67. Kang, J., et al., *Thickness sorting of two-dimensional transition metal dichalcogenides via copolymer-assisted density gradient ultracentrifugation.* Nature Communications, 2014. **5**.

68. Kang, K., et al., *High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity.* NATURE, 2015. **520**(7549): p. 656-660.

69. Shinde, S.M., et al., *Surface-Functionalization-Mediated Direct Transfer of Molybdenum Disulfide for Large-Area Flexible Devices.* Advanced Functional Materials 2018: p. 1706231

70. Kalanyan, B., et al., *Rapid Wafer-Scale Growth of Polycrystalline 2H-MoS2 by Pulsed Metal-Organic Chemical Vapor Deposition.* Chemistry of Materials, 2017. **29**(15): p. 6279-6288.

71. Ho, T.A., et al., *Edge-On MoS2 Thin Films by Atomic Layer Deposition for Understanding the Interplay between the Active Area and Hydrogen Evolution Reaction.* Chemistry of Materials, 2017. **29**(17): p. 7604-7614.

72. Tan, L.K., et al., *Atomic layer deposition of a MoS_2 film.* Nanoscale, 2014. **6**(22): p. 14002-14002.

73. Mattinen, M., et al., *Atomic Layer Deposition of Crystalline MoS2 Thin Films: New Molybdenum Precursor for Low-Temperature Film Growth.* Advanced Materials Interfaces, 2017. **4**(18): p. 1700123.

74. Pyeon, J.J., et al., *Wafer-scale growth of MoS2 thin films by atomic layer deposition.* Nanoscale, 2016. **8**(20): p. 10792-10798.

75. Jang, Y., et al., *Wafer-scale, conformal and direct growth of MoS2 thin films by atomic layer deposition.* Applied Surface Science, 2016. **365**: p. 160-165.

76. Zhou, D., et al., *Unveiling the Growth Mechanism of MoS_2 with Chemical Vapor Deposition: From Two-Dimensional Planar Nucleation to Self-Seeding Nucleation.* Crystal Growth & Design, 2018. **18**(2): p. 1012-1019.

77. Zhu, D.C., et al., *Capture the growth kinetics of CVD growth of twodimensional MoS_2.* Npj 2d Materials and Applications, 2017. **1**: p. 1-8.

78. Ji, Q.Q., et al., *Chemical vapour deposition of group-VIB metal dichalcogenide monolayers: engineered substrates from amorphous to single crystalline.* Chemical Society Reviews, 2015. **44**(9): p. 2587-2602.

79. Blake, P., et al., *Making graphene visible.* Applied Physics Letters, 2007. **91**(6).

80. Zhang, H., et al., *Interference effect on optical signals of monolayer MoS2.* Applied Physics Letters, 2015. **107**(10).

81. Plechinger, G., et al., *A direct comparison of CVD-grown and exfoliated MoS_2 using optical spectroscopy.* Semiconductor Science and Technology, 2014. **29**(6): p. 064008.

82. Johari, P. and V.B. Shenoy, *Tunable Dielectric Properties of Transition Metal Dichalcogenides.* Acs Nano, 2011. **5**(7): p. 5903-5908.

83. Singh, A.K., C. Hwang, and J. Eom, *Low-Voltage and High-Performance Multilayer MoS2 Field-Effect Transistors with Graphene Electrodes.* Acs Applied Materials & Interfaces, 2016. **8**(50): p. 34699-34705.

84. Zhao, M.V., et al., *Large-scale chemical assembly of atomically thin transistors and circuits.* Nature Nanotechnology, 2016. **11**(11): p. 954-959.

85. Baik, S.S., S. Im, and H.J. Choi, *Work Function Tuning in Two-Dimensional MoS2 Field-Effect-Transistors with Graphene and Titanium Source-Drain Contacts.* Scientific Reports, 2017. **7**.

86. Andleeb, S., et al., *MoS2 field-effect transistor with graphene contacts.* Journal of Materials Chemistry, 2017. **C 5**(32): p. 8308-8314.

87. Radisavljevic, B., et al., *Single-layer MoS_2 transistors.* Nature Nanotechnology, 2011. **6**(3): p. 147-150.

88. Radisavljevic, B. and A. Kis, *Measurement of mobility in dual-gated MoS_2 transistors.* Nature Nanotechnology, 2013. **8**(3): p. 147-148.

89. Fuhrer, M.S. and J. Hone, *Measurement of mobility in dual-gated MoS_2 transistors.* Nature Nanotechnology, 2013. **8**(3): p. 146-147.

90. Liu, H. and P.D.D. Ye, *MoS_2 Dual-Gate MOSFET With Atomic-Layer-Deposited Al_2O_3 as Top-Gate Dielectric.* Ieee Electron Device Letters, 2012. **33**(4): p. 546-548.

91. Balandin, A.A., *Noise and fluctuations control in electronic devices*. 2002, Stevenson Ranch, Calif.: American Scientific Publishers. xxi, 390 p.

92. Balandin, A.A., *Low-frequency 1/f noise in graphene devices.* Nature Nanotechnology, 2013. **8**(8): p. 549-555.

93. Renteria, J., et al., *Low-frequency 1/f noise in MoS_2 transistors: Relative contributions of the channel and contacts.* Applied Physics Letters, 2014. **104**(15): p. 153104.

94. Rumyantsev, S.L., et al., *1/ f Noise Characteristics of MoS_2 Thin-Film Transistors: Comparison of Single and Multilayer Structures.* Ieee Electron Device Letters, 2015. **36**(5): p. 517-519.

95. Liu, G.X., et al., *Low-Frequency Electronic Noise in Quasi-1D $TaSe_3$ van der Waals Nanowires.* Nano Letters, 2017. **17**(1): p. 377-383.

96. Dmitriev, A.P., M.E. Levinshtein, and S.L. Rumyantsev, *On the Hooge relation in semiconductors and metals.* Journal of Applied Physics, 2009. **106**(2): p. 024514

97. Rumyantsev, S., et al., *Electrical and noise characteristics of graphene field-effect transistors: ambient effects, noise sources and physical mechanisms.* Journal of Physics-Condensed Matter, 2010. **22**(39): p. 395302.

98. Wang, J.W., et al., *Controlled Low-Frequency Electrical Noise of Monolayer MoS2 with Ohmic Contact and Tunable Carrier Concentration.* Advanced Electronic Materials, 2018. **4**(1): p. 1700340.

99. Yang, H.I., et al., *Epitaxial Molybdenum Disulfide/Gallium Nitride Junctions: Low-Knee-Voltage Schottky-Diode Behavior at Optimized Interfaces.* Acs Applied Materials & Interfaces, 2021. **13**(29): p. 35105-35112.

100. Nakamura, S., T. Mukai, and M. Senoh, *High-Power GaN P-N Junction Blue-Light-Emitting Diodes.* Japanese Journal of Applied Physics, 1991. **30**(Part 2, No. 12A): p. L1998-L2001.

101. Fay, P., D. Jena, and P. Maki, *High-Frequency GaN Electronic Devices*. 2020, New York: Springer.

102. Chowdhury, S., et al., *Current status and scope of gallium nitride-based vertical transistors for high-power electronics application.* Semiconductor Science and Technology, 2013. **28**(7): p. 074014.

103. Scott, M.J., et al., *Merits of gallium nitride based power conversion.* Semiconductor Science and Technology, 2013. **28**(7): p. 074013.

104. Gupta, P., et al., *Layered transition metal dichalcogenides: promising near-lattice-matched substrates for GaN growth.* Sci Rep, 2016. **6**: p. 23708.

105. Ponce, F.A., et al., *Microstructure of GaN epitaxy on SiC using AlN buffer layers.* Applied Physics Letters, 1995. **67**(3): p. 410-412.

106. Nakamura, S., *GaN Growth Using GaN Buffer Layer.* Japanese Journal of Applied Physics, 1991. **30**(Part 2, No. 10A): p. L1705-L1707.

107. Pearton, S.J., C.R. Abernathy, and F. Ren, *Gallium Nitride Processing for Electronics, Sensors and Spintronics*. 2006: Springer-Verlag London.

108. Moun, M. and R. Singh, *Exploring conduction mechanism and photoresponse in P-GaN/n-MoS2 heterojunction diode.* Journal of Applied Physics, 2020. **127**(13): p. 135702

109. Liu, C.Y., et al., *Hybrid Integration of n-MoS2/p-GaN Diodes by Quasi-van der Waals Epitaxy.* Acs Applied Electronic Materials, 2020. **2**(2): p. 419-425.

110. Lee, J., et al., *Growth and characterization of MoS2/n-GaN and MoS2/p-GaN vertical heterostructure with wafer scale homogeneity.* Solid-State Electronics, 2020. **165**: p. 107751.

111. Krishnamoorthy, S., et al., *High current density 2D/3D MoS_2/GaN Esaki tunnel diodes.* Applied Physics Letters, 2016. **109**(18).

112. Desai, P., et al., *Synthesis of MoS_2 Layers on GaN Using Ammonium Tetrathiomolybdate for Heterojunction Device Applications.* Crystal Research and Technology, 2021(56): p. 2000198.

113. Song, Y.M., et al., *Exploration of Monolayer MoS2 Template-Induced Growth of GaN Thin Films via Plasma-Enhanced Atomic Layer Deposition.* Crystal Growth & Design, 2021. **21**(3): p. 1778-1785.

114. Wang, J., et al., *Thickness-Dependent Phase Stability and Electronic Properties of GaN Nanosheets and MoS_2/GaN van der Waals Heterostructures.* Journal of Physical Chemistry C, 2019. **123**(6): p. 3861-3867.

115. Jain, S.K., et al., *2D/3D Hybrid of MoS2/GaN for a High-Performance Broadband Photodetector.* ACS Applied Electronic Materials, 2021. **3**(5): p. 2407-2414.

116. Ruzmetov, D., et al., *Vertical 2D/3D Semiconductor Heterostructures Based on Epitaxial Molybdenum Disulfide and Gallium Nitride.* ACS Nano, 2016. **10**(3): p. 3580-3588.

117. Ruzmetov, D., et al., *Van der Waals interfaces in epitaxial vertical metal/2D/3D semiconductor heterojunctions of monolayer MoS_2 and GaN.* 2d Materials, 2018. **5**(4): p. 045016.

118. Leonhardt, A., et al., *Improving MOCVD MoS2 Electrical Performance: Impact of Minimized Water and Air Exposure Conditions.* Ieee Electron Device Letters, 2017. **38**(11): p. 1606-1609.

119. Islam, Z., et al., *Quality enhancement of low temperature metal organic chemical vapor deposited MoS2: an experimental and computational investigation.* Nanotechnology, 2019. **30**(39): p. 31234158.

120. Zhang, K.H., et al., *Large scale 2D/3D hybrids based on gallium nitride and transition metal dichalcogenides.* Nanoscale, 2018. **10**(1): p. 336-341.

121. Zhang, Z.F., et al., *Interface Engineering of Monolayer MoS_2/GaN Hybrid Heterostructure: Modified Band Alignment for Photocatalytic Water Splitting Application by Nitridation Treatment.* Acs Applied Materials & Interfaces, 2018. **10**(20): p. 17419-17426.

122. Kresse, G. and J. Hafner, *Abinitio Molecular-Dynamics for Liquid-Metals.* Physical Review B, 1993. **47**(1): p. 558-561.

123. Kresse, G. and J. Furthmuller, *Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set.* PHYSICAL REVIEW B, 1996. **54**(16): p. 11169-11186.

124. Almeida, K., et al., *High-Vacuum Particulate-Free Deposition of Wafer-Scale Mono-, Bi-, and Trilayer Molybdenum Disulfide with Superior Transport Properties.* ACS Applied Materials & Interfaces, 2018. **10**(39): p. 33457-33463.

125. Somorjai, G.A., *Introduction to surface chemistry and catalysis.* 1994, New York: Wiley. xxiv, 667 p.

126. Roldan, R., et al., *Strain engineering in semiconducting two-dimensional crystals.* Journal of Physics-Condensed Matter, 2015. **27**(31): p. 313201.

127. Sung, D., K.A. Min, and S. Hong, *Investigation of atomic and electronic properties of 2D-MoS_2/3D-GaN mixed-dimensional heterostructures.* Nanotechnology, 2019. **30**(40): p. 404002.

128. Wan, Y., et al., *Epitaxial Single-Layer MoS_2 on GaN with Enhanced Valley Helicity.* Advanced Materials, 2018. **30**(5): p. 1703888.

129. O'Regan, T.P., et al., *Structural and electrical analysis of epitaxial 2D/3D vertical heterojunctions of monolayer MoS2 on GaN.* Applied Physics Letters, 2017. **111**(5): p. 051602.

130. Greco, G., F. Iucolano, and F. Roccaforte, *Ohmic contacts to Gallium Nitride materials.* Applied Surface Science, 2016. **383**: p. 324-345.

131. Durmus, H. and U. Atav, *Extraction of voltage-dependent series resistance from I-V characteristics of Schottky diodes.* Applied Physics Letters, 2011. **99**(9): p. 093505

132. Kriplani, N.M., et al., *Modelling of an Esaki Tunnel Diode in a Circuit Simulator.* Active and Passive Electronic Components, 2011. **2011**: p. 830182

133. Merida, C.S., et al., *Gold Dispersion and Activation on the Basal Plane of Single-Layer MoS_2.* Journal of Physical Chemistry C, 2018. **122**(1): p. 267-273.

134. Tahersima, M.H., et al., *Testbeds for Transition Metal Dichalcogenide Photonics: Efficacy of Light Emission Enhancement in Monomer vs Dimer Nanoscale Antennae.* Acs Photonics, 2017. **4**(7): p. 1713-1721.

135. Tang, W., E. Sanville, and G. Henkelman, *A grid-based Bader analysis algorithm without lattice bias.* Journal of Physics-Condensed Matter, 2009. **21**(8): p. 084204.

136. Laskar, M.R., et al., *p-type doping of MoS_2 thin films using Nb.* APPLIED PHYSICS LETTERS, 2014. **104**(9): p. 092104.

137. Novoselov, K.S., et al., *Electric field effect in atomically thin carbon films.* Science, 2004. **306**(5696): p. 666-669.

138. Castro Neto, A.H., et al., *The electronic properties of graphene.* Reviews of Modern Physics, 2009. **81**(1): p. 109.

139. Lee, C., et al., *Measurement of the elastic properties and intrinsic strength of monolayer graphene.* Science, 2008. **321**(5887): p. 385-388.

140. Zhang, Y.B., et al., *Experimental observation of the quantum Hall effect and Berry's phase in graphene.* Nature, 2005. **438**(7065): p. 201-204.

141. Chhowalla, M., et al., *The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets.* Nat Chem, 2013. **5**(4): p. 263-75.

142. Bernardi, M., M. Palummo, and J.C. Grossman, *Extraordinary Sunlight Absorption and One Nanometer Thick Photovoltaics Using Two-Dimensional Monolayer Materials.* Nano Letters, 2013. **13**(8): p. 3664-3670.

143. Empante, T.A., et al., *Chemical Vapor Deposition Growth of Few-Layer $MoTe_2$ in the 2H, 1T', and 1T Phases: Tunable Properties of $MoTe_2$ Films.* ACS Nano, 2017. **11**: p. 900.

144. Lukatskaya, M.R., et al., *Cation Intercalation and High Volumetric Capacitance of Two-Dimensional Titanium Carbide.* Science, 2013. **341**(6153): p. 1502-1505.

145. Naguib, M., et al., *Two-Dimensional Transition Metal Carbides.* Acs Nano, 2012. **6**(2): p. 1322-1331.

146. Naguib, M., et al., *25th Anniversary Article: MXenes: A New Family of Two-Dimensional Materials.* Advanced Materials, 2014. **26**(7): p. 992-1005.

147. Khazaei, M., et al., *Novel Electronic and Magnetic Properties of Two-Dimensional Transition Metal Carbides and Nitrides.* Advanced Functional Materials, 2013. **23**(17): p. 2185-2192.

148. Geremew, A., et al., *Unique features of the generation–recombination noise in quasi-one-dimensional van der Waals nanoribbons.* Nanoscale, 2018. **10.1039/C8NR06984K**.

149. Stolyarov, M.A., et al., *Breakdown current density in h-BN-capped quasi-1D $TaSe_3$ metallic nanowires: prospects of interconnect applications.* Nanoscale, 2016. **8**(34): p. 15774-15782.

150. Geremew, A., et al., *Current Carrying Capacity of Quasi-1D $ZrTe_3$ Van Der Waals Nanoribbons.* Ieee Electron Device Letters, 2018. **39**(5): p. 735-738.

151. Bjerkelund, E. and A. Kjekshus, *On the Properties of TaS_3, $TaSe_3$ and $TaTe_4$.* Zeitschrift Fur Anorganische Und Allgemeine Chemie, 1964. **328**(5-6): p. 235-242.

152. Canadell, E., et al., *Comparison of the Electronic-Structures of Layered Transition-Metal Trichalcogenides $TaSe_3$, TaS_3, and $NbSe_3$.* Inorganic Chemistry, 1990. **29**(7): p. 1401-1407.

153. Ariya, S.M., A.I. Zaslavskii, and I.I. Matveeva, *Khimiya Soedinenii Peremennogo Sostava .4. Sistema Tantal-Selen.* Zhurnal Obshchei Khimii, 1956. **26**(9): p. 2373-2375.

154. Heidenreich, J., et al., *Copper dual damascene wiring for sub-0.25 mu m CMOS technology.* Proceedings of the Ieee 1998 International Interconnect Technology Conference, 1998: p. 151-153.

155. Bohr, M., et al., *A high performance 0.25 mu m logic technology optimized for 1.8V operation.* Iedm - International Electron Devices Meeting, Technical Digest 1996, 1996: p. 847-850.

156. Fischer, K., et al., *Low-k Interconnect Stack with multi-layer Air Gap and Tri-Metal-Insulator-Metal Capacitors for 14nm High Volume Manufacturing.* 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM), 2015: p. 5-7.

157. Marchetti, F. and G. Pampaloni, *Interaction of niobium and tantalum pentahalides with O-donors: coordination chemistry and activation reactions.* Chemical Communications, 2012. **48**(5): p. 635-653.

158. Wang, T.C., et al., *Copper voids improvement for the copper dual damascene interconnection process.* Journal of Physics and Chemistry of Solids, 2008. **69**(2-3): p. 566-571.

159. Kresse, G. and J. Furthmüller, *Efficiency of ab-initio total energy calculations for metals and semiconductors using a plane-wave basis set.* Comput. Mat. Sci., 1996. **6**: p. 15.

160. Blochl, P.E., *Projector Augmented-Wave Method.* PHYSICAL REVIEW B, 1994. **50**(24): p. 17953-17979.

161. Kresse, G. and D. Joubert, *From ultrasoft pseudopotentials to the projector augmented-wave method.* PHYSICAL REVIEW B, 1999. **59**(3): p. 1758-1775.

162. Perdew, J.P., K. Burke, and M. Ernzerhof, *Generalized gradient approximation made simple.* Physical Review Letters, 1996. **77**(18): p. 3865-3868.

163. Monkhorst, H.J. and J.D. Pack, *Special Points for Brillouin-Zone Integrations.* Physical Review B, 1976. **13**(12): p. 5188-5192.

164. Mermin, N.D. and H. Wagner, *Absence of Ferromagnetism or Antiferromagnetism in One- or 2-Dimensional Isotropic Heisenberg Models.* Physical Review Letters, 1966. **17**(22): p. 1133-&.

165. O'Hare, A., F.V. Kusmartsev, and K.I. Kugel, *A Stable "Flat" Form of Two-Dimensional Crystals: Could Graphene, Silicene, Germanene Be Minigap Semiconductors?* Nano Letters, 2012. **12**(2): p. 1045-1052.

166. Dutta, P. and P.M. Horn, *Low-Frequency Fluctuations in Solids - 1-F Noise.* Reviews of Modern Physics, 1981. **53**(3): p. 497-516.

167. Vandamme, L.K.J., *Noise as a Diagnostic-Tool for Quality and Reliability of Electronic Devices.* Ieee Transactions on Electron Devices, 1994. **41**(11): p. 2176-2187.

168. Balandin, A.A., *Noise and Fluctuations Control in Electronic Devices*. 2003, World Scientific Publishing Co.

169. Beyne, S., et al., *1/f noise measurements for faster evaluation of electromigration in advanced microelectronics interconnections.* Journal of Applied Physics, 2016. **119**(18): p. 184302.

170. Bagnoli, P.E., et al., *Electromigration in Al based stripes: Low frequency noise measurements and MTF tests.* Microelectronics and Reliability, 1996. **36**(7-8): p. 1045-1050.

171. Liu, G.X., et al., *Low-Frequency Current Fluctuations and Sliding of the Charge Density Waves in Two-Dimensional Materials.* Nano Letters, 2018. **18**(6): p. 3630-3636.

172. Dutta, P., P. Dimon, and P.M. Horn, *Energy Scales for Noise Processes in Metals.* Physical Review Letters, 1979. **43**(9): p. 646-649.

173. Koch, R.H., J.R. Lloyd, and J. Cronin, *1/F Noise and Grain-Boundary Diffusion in Aluminum and Aluminum-Alloys.* Physical Review Letters, 1985. **55**(22): p. 2487-2490.

174. Chen, T.M. and A.M. Yassine, *Electrical Noise and Vlsi Interconnect Reliability.* Ieee Transactions on Electron Devices, 1994. **41**(11): p. 2165-2172.

175. Liao, I., et al., *Hybrid Single-Layer/Bulk Tungsten Diselenide Transistors by Lithographic Encoding of Material Thickness in Chemical Vapor Deposition.* 2D Materials, 2018. **6**: p. 015017.

176. Sun, D.Z., et al., *Chemical vapor deposition growth of a periodic array of single-layer MoS_2 islands via lithographic patterning of an SiO_2/Si substrate.* 2d Materials, 2015. **2**(4): p. 045014.

177. Gong, C.H., et al., *2D Nanomaterial Arrays for Electronics and Optoelectronics.* Advanced Functional Materials, 2018. **28**(16): p. 1706559.

178. Young, J.R., et al., *Uniform large-area growth of nanotemplated high-quality monolayer MoS2.* Applied Physics Letters, 2017. **110**(26): p. 263103

179. Jin, J., et al., *Rapid Chemical Vapor Deposition of Metallic ZrTe3 Nanoribbons on a SiO2 Wafer Substrate.* 2021: p. Submitted.

180. Beyne, S., et al., *The first Observation of p-type Electromigration Failure in full Ruthenium Interconnects.* 2018 IEEE International Reliability Physics Symposium (IRPS), 2018: p. 6D-7.

181. Mont, F.W., et al., *Cobalt Interconnect on Same Copper Barrier Process Integration at the 7nm node.* 2017 IEEE International Interconnect Technology Conference, 2017.

182. Zhang, X.Y., et al., *Ruthenium Interconnect Resistivity and Reliability at 48 nm pitch.* 2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference 2016: p. 31-33.

183. Wen, L.G., et al., *Ruthenium Metallization for Advanced Interconnects.* 2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference 2016: p. 34-36.

184. Dutta, S., et al., *Finite Size Effects in Highly Scaled Ruthenium Interconnects.* IEEE Electron Device Letters, 2018. **39**(2): p. 268-271.

185. Liu, G., et al., *Total-Ionizing-Dose Effects on Threshold Switching in 1T-TaS_2 Charge Density Wave Devices.* IEEE Electron Device Letters, 2017. **38**(12): p. 1724-1727.

186. Yang, X.J., et al., *Pressure induced superconductivity bordering a charge-density-wave state in NbTe4 with strong spin-orbit coupling.* Scientific Reports, 2018. **8**: p. 6298.

187. Hu, Y.W., et al., *Charge density waves and phonon-electron coupling in $ZrTe_3$.* Physical Review B, 2015. **91**(14): p. 144502.

188. Perucchi, A., L. Degiorgi, and H. Berger, *Infrared signature of the charge-density-wave gap in $ZrTe_3$.* European Physical Journal B, 2005. **48**(4): p. 489-493.

189. Gleason, S.L., et al., *Structural contributions to the pressure-tuned charge-density-wave to superconductor transition in $ZrTe_3$: Raman scattering studies.* Physical Review B, 2015. **91**(15): p. 155124.

190. Monceau, P., *Electronic crystals: an experimental overview.* Advances in Physics, 2012. **61**(4): p. 325-581.

191. Yu, X., et al., *Fast and controlled growth of two-dimensional layered $ZrTe_3$ nanoribbons by chemical vapor deposition.* Crystengcomm, 2019. **21**(37): p. 5586-5594.

192. Pant, A., et al., *Strong dichroic emission in the pseudo one dimensional material ZrS_3.* Nanoscale, 2016. **8**(36): p. 16259-16265.

193. Nakajima, H., K. Nomura, and T. Sambongi, *Anisotropic Superconducting Transition in $ZrTe_3$.* Physica B & C, 1986. **143**(1-3): p. 240-242.

194. Liang, T., et al., *Anomalous Hall effect in $ZrTe_5$.* Nature Physics, 2018. **14**(5): p. 451-455.

195. Tang, F.D., et al., *Three-dimensional quantum Hall effect and metal-insulator transition in $ZrTe_5$.* Nature, 2019. **569**(7757): p. 537-541.

196. Zhu, X.Y., et al., *Disorder-induced bulk superconductivity in $ZrTe_3$ single crystals via growth control.* Physical Review B, 2013. **87**(2): p. 86–91.

197. Yadav, C.S. and P.L. Paulose, *Superconductivity at 5.2 K in $ZrTe_3$ polycrystals and the effect of Cu and Ag intercalation.* Journal of Physics-Condensed Matter, 2012. **24**(23): p. 235702

198. Itkis, M.E., F.Y. Nad, and F. Levy, *Energy-Band Structure of the Quasi-One-Dimensional Conductor NbS_3.* Synthetic Metals, 1991. **43**(3): p. 3969-3972.

199. Roucau, C., et al., *Electron-Diffraction and Resistivity Measurements on the One-Dimensional Orthorhombic and Monoclinic Structures of TaS_3 - Comparison with $NbSe_3$.* Physica Status Solidi a-Applied Research, 1980. **62**(2): p. 483-493.

200. Hooda, M.K., T.S. Tripathi, and C.S. Yadav, *Semiconducting nature and thermal transport studies of $ZrTe_3$.* Journal of Alloys and Compounds, 2019. **785**: p. 603-609.

201. Sambongi, T., et al., *Superconductivity in One-Dimensional $TaSe_3$.* Journal of the Physical Society of Japan, 1977. **42**(4): p. 1421-1422.

202. Tsuchiya, S., et al., *Effects of pressure and magnetic field on superconductivity in $ZrTe_3$: local pair-induced superconductivity.* New Journal of Physics, 2017. **19**: p. 063004.

203. Pokhrel, D., et al., *Aspect ratio controlled synthesis of tellurium nanowires for photovoltaic applications.* Materials Advances, 2020. **1**(8): p. 2721-2728.

204. Mohanty, P., J. Park, and B. Kim, *Large scale synthesis of highly pure single crystalline tellurium nanowires by thermal evaporation method.* Journal of Nanoscience and Nanotechnology, 2006. **6**(11): p. 3380-3383.

205. Wang, Q., et al., *Fabrication and growth mechanism of selenium and tellurium nanobelts through a vacuum vapor deposition route.* Journal of Physical Chemistry C, 2007. **111**(35): p. 12926-12932.

206. Qin, J.K., et al., *Raman response and transport properties of tellurium atomic chains encapsulated in nanotubes.* Nature Electronics, 2020. **3**(3): p. 141-147.

207. Jain, A., et al., *Commentary: The Materials Project: A materials genome approach to accelerating materials innovation.* Apl Materials, 2013. **1**(1): p. 011002.