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FAST READOUT OF CCD IMAGES

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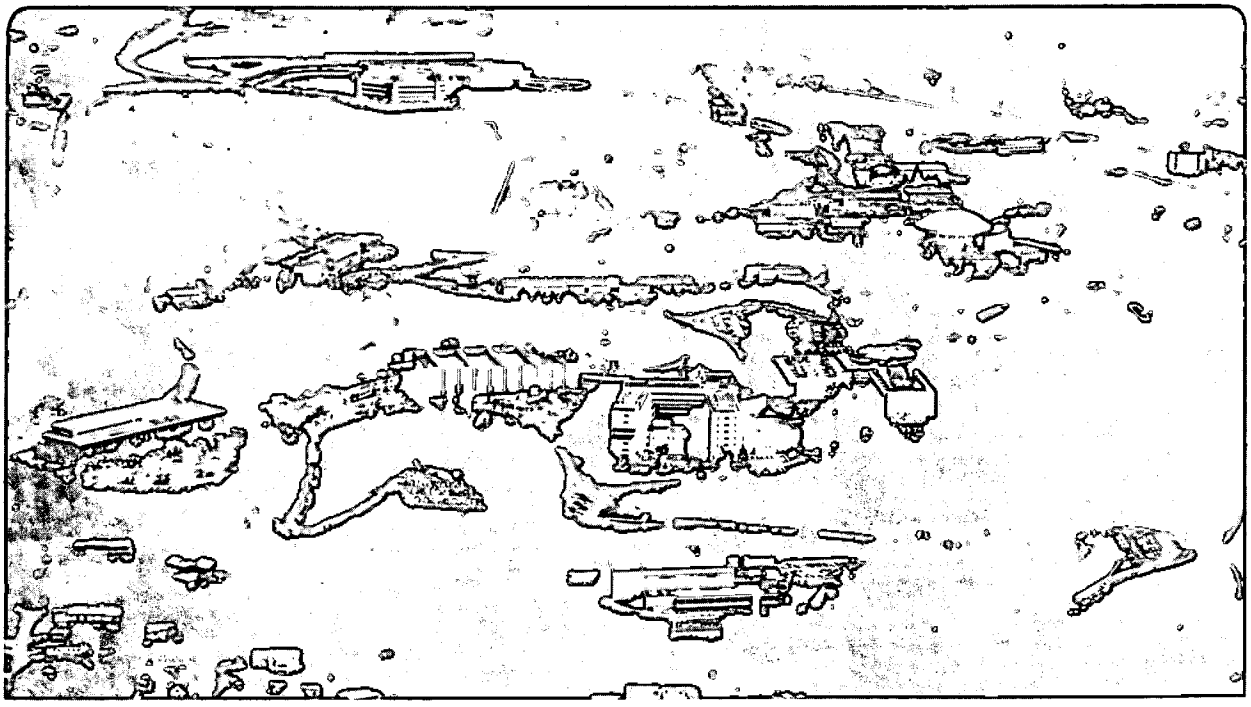

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FAST READOUT OF CCD IMAGES

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ABSTRACT

A new fast serial readout system for CCD imaging devices is described. Clock frequency of up to 65 MHz and 1 μs line transfer time make possible frame rates of approximately 500/s. A baseline stabilized video amplifier and fast peak stretcher also make possible high resolution frame readout with excellent dynamic range. It uses a fast dump readout sequence which clears the analog registers prior to the image charge transfer from the photoelements. The charge of any preset pixel can be individually extracted, its peak stretched, and the noise distribution measured by a multichannel pulse-height analyzer. Photographs of test pattern readouts at high clock frequencies are shown and the effect of clock and frame readout rates and temperature on noise distribution have been measured.

INTRODUCTION

State-of-the-art charge-coupled devices (CCD) for solid state area image sensing offer, at the rated readout clock frequencies, a signal dynamic range in excess of 1000:1 with virtually no geometric distortion. The dark noise level can be made very low by cooling the device, making possible imaging at very low light levels. Typically, the photoelements are arrayed in a rectangular matrix, frequently with an aspect ratio close to that of a standard video frame.

Each CCD photoelement integrates the charge generated by the photons during the time between successive frame readouts. The transfer of the charge from all the photoelements into analog charge transport registers takes place simultaneously at the beginning of each frame. The signals from the frame are then read out serially line by line first into a horizontal shift register by a sequence of vertical transport clocks, and then through a charge sensitive amplifier by a series of horizontal clock pulses. The amplifier video output can be made compatible with the standard television format by choosing an appropriate charge transport clock frequency. A relatively low clock frequency is sufficient for readout rates not exceeding 30 frames/second.

CCD imaging devices can be used in many applications where high resolution and dynamic range, low noise and virtually no spatial distortion are required. In general, however, they have not been able to reach high frame readout rates, due to the limited bandwidth of their video amplifier and difficulty of driving charge transport clocks at high frequencies. The present work aims to improve this situation.

A fast readout system applied to the Fairchild Corp. CCD 222 image sensor is described. Although the device is rated for a maximum clock frequency of 20 MHz, the results show an excellent linearity and dynamic range at the frequencies exceeding 50 MHz. At high light levels the charge integration time can be short which allows such rates, keeping the noise level low even at room temperature. High resolution imaging at high frame rates of up to 500/sec is thus possible.

Critical for the operation of the readout are clock drivers capable of charging large CCD stray capacitances at high frequencies, and a high-frequency video output processing amplifier. The digital circuits of the system allow operation at any clock frequency up to 65 MHz (supplied by an external source) without the need for adjustment. This makes the system easily adaptable to many applications.

GENERAL DESCRIPTION

The basic blocks of the system are shown in Fig. 1 and a general layout of the CCD 222 image sensor in Fig. 2. The sensor has 488 lines of 380 discrete photoelements each. The size of each element is 18 x 12 μm. Each photoelement has an access to one of the 380 vertical transport registers. The register is divided into 244 compartments, each one alternately serving a pair of even and odd adjacent photoelements.

The charge integrated in the photoelements is transferred into the registers by the combination of three clock pulses. When the photogate pulse ϕP is low for the duration the vertical transport pulse $\phi V1$, the charge from all odd photoelements is transferred into the registers (Fig. 3A, top line). Similarly, when ϕP is low during the pulse $\phi V2$, all the charge from even photoelements is transferred. The charge in the registers is shifted by one step upwards each time all three clock pulses occur simultaneously. The charge in the top compartment of the vertical registers is transferred into the corresponding compartment of a horizontal transport register (Fig. 2) after each vertical shift.

A pair of horizontal clock pulses $\phi H1$ and $\phi H2$ shift the charges of a whole line down the register in 380 steps, past the sensing electrode of a floating gate amplifier, into a sink diode. Each vertical transfer step, followed by 380 horizontal steps, thus makes one line of the video frame. The frame is composed of two fields, one by reading out even and the other odd photoelements (note, this is similar to interlaced beam scanning of conventional TV).

Both fields can be combined into a single frame by transferring the even and odd fields at the same time into the vertical registers (Fig. 3B). If ϕP is low during both $\phi V1$ and $\phi V2$ clock pulses, the charge of the two adjacent even and odd photoelement pairs are added in the same segment of the vertical register. The vertical resolution of the image is reduced in half, and the frame readout rate doubled.

This system allows for one more readout mode, especially suitable in imaging with pulsed light sources. Although the surfaces of all CCD registers are made opaque, some light penetrates the barriers, creating undesired charges that will get superimposed upon the image. In the "fast dump" mode of the readout system, the continuous readout of frames can be interrupted at any time upon the receipt of a command (Fig. 3C). One fast dump cycle is generated for each such command, which consists of a sequence of vertical transfer pulses only. All the charge in the vertical

registers will be quickly cleared since no time is spent for horizontal transfer. The following regular readout cycle will thus start by the transfer of the image into the vertical registers free of any residual charge.

The great increase of the frame transport rates is due to the design of new clock drivers. The vertical transport cycle can be reduced to 1 µs from the typical 7 µs. The drivers have to charge the 15000 pF and 12000 pF resp. of stray capacitances of the photogate and vertical clock ports up to 10 volts. The first two lines of a frame are shown in Fig. 5A. The horizontal clocks have to charge a stray capacitance of 200 pF to 10V. Only a few milliwatts of stand-by power is required by the driver clocks. The dissipation increases with the readout frequency. The low dissipation and small size of the drivers reduces cooling problems of the sensor, allowing a very compact package. Two pairs of horizontal clock pulses at the beginning of a line are shown in Fig. 5B.

DIGITAL AND LOGIC CIRCUITS

The digital circuits provide proper timing for the clocks and control the operation of the video amplifier. All the timing is referred to the reference clock oscillator. Either a fixed frequency internal oscillator or an external variable frequency reference can be used. The required frequency has to be twice the desired line frequency of the horizontal clock. The simplified diagram in Fig. 4 shows the basic blocks that generate the proper sequence of pulses for each of several modes of video frame readout.

In the continuous readout mode, the frequency divider B1 is enabled, feeding two preset counters. The horizontal counter HC defines the number of pixels of each line and the width counter WC the pause between the lines. The vertical transfer clock pulses are generated during the pause. The pause width can be optimized for a given clock frequency and for an individual CCD chip to minimize the vertical transfer time. The horizontal counter is normally preset to 380 steps, sufficient to shift all of the regular line charges. The line can be lengthened by presetting to more than 380 steps for a study of the register transfer efficiency and the video amplifier response.

The WC and HC counting is controlled by the binary B2, which toggles once for each line. The transition of B2 advances the preset vertical counter VC, which counts the number of vertical lines of the frame. Again, by presetting VC to more than 244 steps, the efficiency of the vertical CCD register transfer and the video amplifier can be inspected. Since the signal should be discharged after the readout of the last 244th line, any residual charge in the following line is a measure of the register transfer efficiency.

Four adjustable timers T1-T4 are fired in series at the beginning of each line. They define the widths and separation of the vertical transfer pulses ϕP, ϕV1 and ϕV2. The gates G1-G3 and the binary B5 ensure that the timing of these pulses conform to the selected mode of operation, as shown in Fig. 3. The clocks for the two line drivers controlling the CCD horizontal register are selected by the gates G4 to G6. An additional clock output is provided by the latch L2 and gate G7 for the strobing an external video digitizer. Also, a frame trigger output signal is generated by the latches and gate L3, L4 and G4 at the beginning of each new frame.

The fast dump cycle, described earlier, can be initiated at any time by an external pulse, or manually. The leading edge of this command stops the frame in progress by generating a clear signal that resets all the latches and stops the frequency divider. The trailing edge of the command sets the latch L1, which in turn restarts the clock. The binary L2 is reset, and, for the duration of the dump cycle, keeps the horizontal counter HC preset to one, meaning that each horizontal line is shortened from its original 380 clock pulses to one pulse. The first frame after the start pulse has only vertical transfer pulses and no horizonal pulses. Also, the transfer of the charge from the photoelements into the vertical register is inhibited.

The binary L2 is again set at the beginning of the new frame, allowing the horizontal counter to be preset to 380 counts per line. The regular frame sequence is resumed again.

The circuits, consisting mostly of low power Shottky TTL chips, work up to a horizontal clock frequency of 70 MHz. An external sinusoidal reference of twice the line frequency and about 2V RMS is required.

VIDEO SIGNAL PROCESSING

The charge clocked past the CCD floating gate is sensed by an on-chip gated amplifier (Fig. 2). The gate bias ϕBE is synchronous with the horizontal clock pulses ϕH1, and the charge reset between the lines to the external bias level by the clock pulses ϕR. The reset pulse ϕR is synchronous with the vertical transfer pulse ϕV1. At low horizontal clock frequencies the amplifier sample-and-hold circuit is strobed during the positive portion of the bias clock signal, upon which the video signal is superimposed. The response of the circuit is too slow for the clock frequencies exceeding 15 MHz. The CCD sample-and-hold gate is therefore biased open at all times, making the video amplifier "transparent" for all the charge sensed by the floating gate. Two pixels of a line at 10 MHz from the amplifier output are shown in Fig. 6. Sharp feed-through transients from the fast square bias clock are seen superimposed upon them.

A fast dc coupled video amplifier was designed. No coupling time constant adjustment is therefore necessary for reading out frames of different durations. The video amplifier consists of a level shifting preamplifier and a main amplifier (Fig. 1). Also, an optional baseline stabilizer is incorporated. Once during each line of the frame, at the time the floating gate is being discharged to the reference bias, the video ouput level is strobed in a fast track-and-hold circuit. The level is compared with the reference bias voltage, correcting the video amplifier baseline if it has shifted.

At higher clock frequencies the video output becomes a series of sharp pulses with the amplitude proportional to the light intensity (Fig. 8). Most of the commercial "frame grabbers" do not have the bandwidth that would allow the digitizing of such waveforms within an acceptable error margin. A fast peak stretcher was built that senses the amplitude of each pixel in the video signal and retains this level until discharged shortly before the arrival of the next one (Fig. 9A). The video signal stays flat long enough to match the frame grabber's required acquisition time, minimizing the analog-to-digital conversion error.

An additional feature of this system is the single pixel selector circuit (not shown in Fig. 4). This circuit generates a strobe pulse once during the course of each frame, at the time the preset pixel in the

preset line is reached. This strobe can be used to control the fast peak stretcher. All pixels in the frame will then be suppressed except for the selected one (Fig. 9B). The long triangular pulse thus generated can be digitized by a multichannel pulse-height analyzer. Dynamic range and noise distribution of the video signal can be measured with a high resolution and accuracy in this manner.

TEST RESULTS

Preliminary tests of the new CCD image readout system on the Fairchild Corp. CCD 222 488 x 380-element area image sensor are shown. A slide with an accurate test pattern (Fig. 7) was focused on the sensor surface. The slide was rotated until the rows of test bars were perpendicular to the horizontal lines of the frame. One line, which runs across the middle row of test bars, was selected and displayed at three selected pixel clock frequencies of 20, 50 and 70 MHz respectively (Fig. 8). The left column of photographs shows the top portion of the video waveform in the range between the "dark" and "saturation" levels. The dark levels were obtained by exposing the photographs for the second time with the CCD light off. The peaks of the waveform show three rows of the test pattern bars.

The central portion of the line is further expanded in the right column of Fig. 8. Three first groups of four bars each are clearly resolved. The other groups are blurred since the width of the bars became smaller than the width of the individual CCD pixel (12 μm). The bottom photograph, although taken at the frequency of 70 MHz, well beyond the expected operation range of the system circuitry, still shows two sets of bars resolved.

At low clock frequencies the CCD 222 amplifier has time to settle, as the Fig. 6, taken at 10 MHz, shows. Assuming the exponential response of the amplifier to the step change of charge, caused by the floating gate bias clock change, the pixel amplitude would decrease as

$$v=(v_0+v_s)\exp(-nT/\alpha)$$

where v_0 is the video amplitude at the dark level including the reset clock feed-through, v_s is the increase of the signal when the pixel is illuminated, α is the discharge time constant and T the period of horizontal clock. The unwanted contribution of the signal v_s of an arbitrary pixel to the signal of the nth following pixel will be $v_s\exp(-nT/\alpha)$. For a clock frequency of 50 MHz (T=20 ns) and α=10 ns (found experimentally), the fraction of v_s superimposed upon the amplitude of the three following pixels would amount to 13.5, 1.83 and 0.24 per cent resp. Appropriate corrections should be made when data is analyzed in high resolution image digitizing, particularly at high frequencies.

Linearity of response of CCD 222 to light intensity at high clock frequencies was also measured. The amplitude of a selected pixel was digitized (Fig. 9B) by a multichannel pulse-height analyzer in a manner described earlier. An incandescent light source was used. The pixel amplitude above the dark level as a function of the light source voltage at a 32 MHz clock frequency is shown in Fig. 10 (Curve E). The change of slope at the high intensity end indicates the beginning of the CCD saturation region.

A set of calibrated neutral density filters was used for the attenuation of light, and corresponding reduction in amplitude digitized. Measurements taken at four different initial light intensities, shown in Fig. 10 (Curves A to E, upper scale), demonstrate an excellent linearity of the CCD amplitude response to light intensity, covering a range of three decades. The top measured point in the Curve A is off due to the beginning of the saturation region, as indicated by the Curve E.

The pulse-height analyzer also provides distributions of pixel amplitudes as a function of light intensity, pixel clock frequencies, frame readout rates (i.e. dark current integration time) and temperature. Figure 11, taken at 26°C, 40 MHz and frame rate of 3.6 ms, shows three distributions at different light intensities and one in the dark. The distributions result from the superposition of dark noise, video amplifier and stretcher noise, and to some extent the contribution of the 60 cycle ground currents due to the dc coupling of all components of the measuring system. The distributions broaden as the frame readout rate is decreased, due to the increase of integration time of the dark current noise. The frame readout at high rates thus offers a possibility of the high resolution imaging at room temperatures, provided that the image intensity is high enough for the given integration times.

CONCLUSIONS

The measurements on the CCD 222 area image sensor show the new fast frame readout system described here extends the useful range of the device to well over a 50 MHz clock range, permitting readouts of 500 frames per second. Normally they are rated at 20 MHz maximum. The excellent linearity and dynamic range are not much impaired at the high rates, making high resolution imaging at high frame rate possible even at room temperature due to shortened dark noise integration time. The measurements, performed so far, indicate a possibility of operating the device at even higher readout frequencies.

ACKNOWLEDGEMENTS

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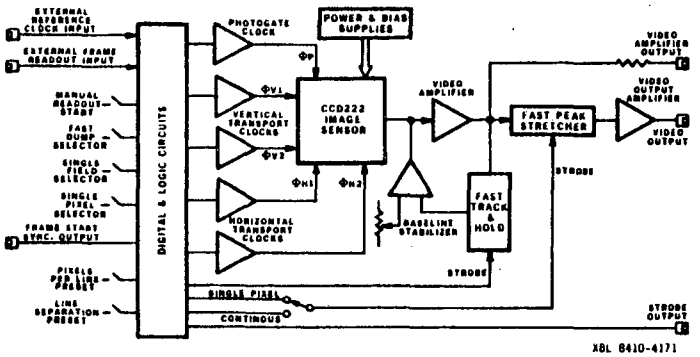

Fig. 1. Block diagram of fast CCD image readout system.

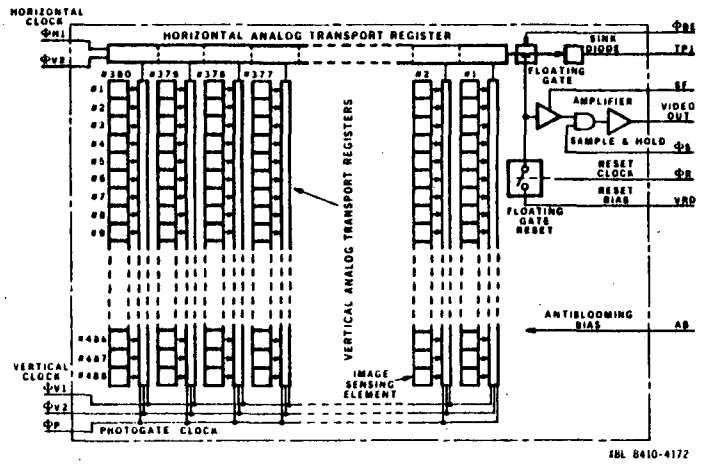

Fig. 2. Basic components of Fairchild Corp. CCD 222 488 x 380-element area image sensor.

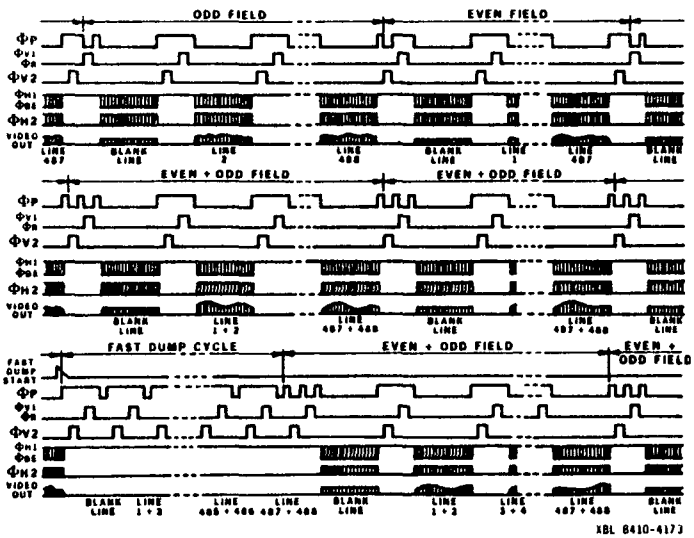

Fig. 3. Sequences of CCD 222 charge transport clocks for the three modes of readout.

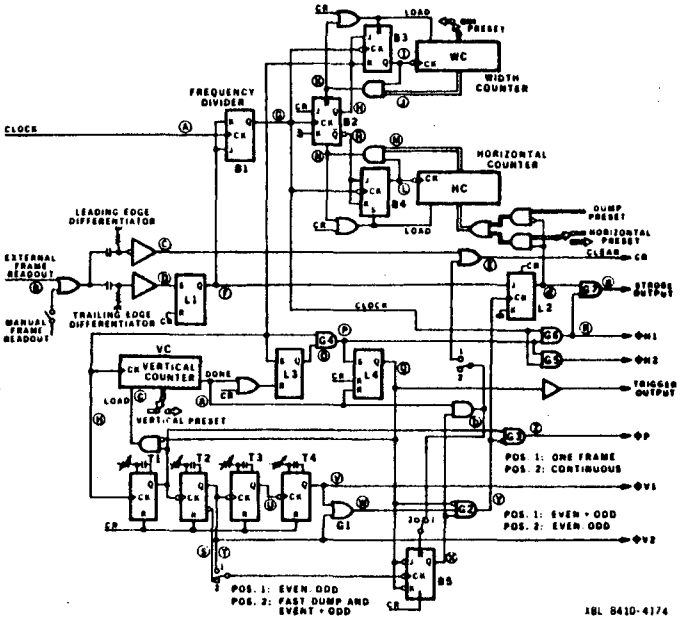

Fig. 4. Digital and logic circuit block diagram of the fast CCD readout.

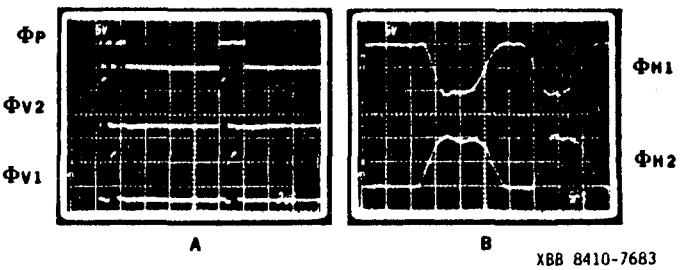

Fig. 5. A. Sequence of vertical charge transport clocks at the beginning of a frame (even and odd fields combined). B. Horizontal transfer clock pulses at the beginning of a line at 50 HMz.

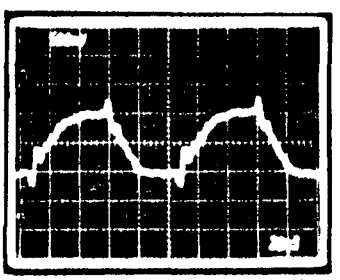

Fig. 6. Two pixels of the video output of CCD 222 image sensor at 10 MHz clock frequency .

Fig. 7. Slide with a pattern for testing CCD image sensor.

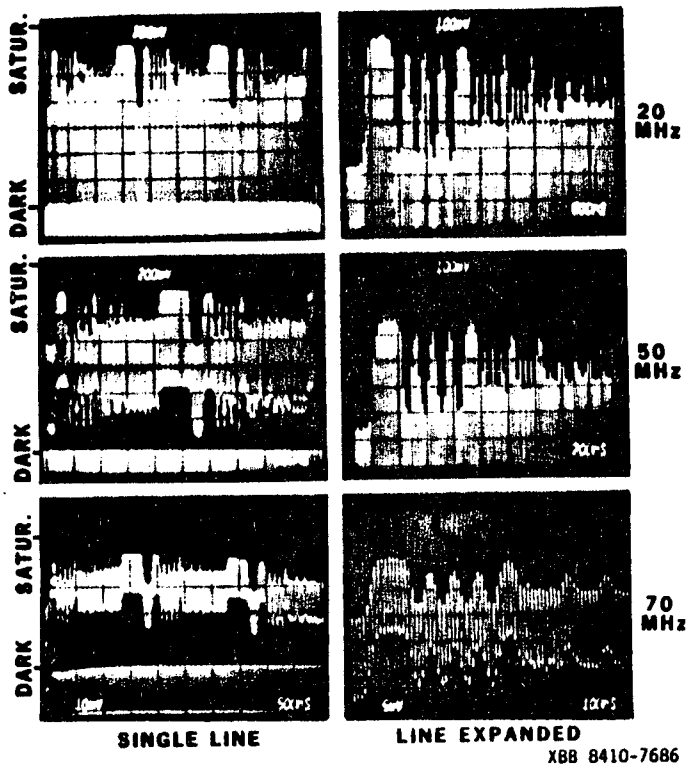

Fig. 8. One line of a video frame at 20, 50 and 70 MHz pixel frequency with the pattern (Fig. 7) focused on CCD 222. Expanded line (right column) shows three sets of four bars each of the test pattern. Remaining sets are blurred as the bars grow smaller than CCD pixels. At 70 MHz, only two groups of bars are resolved.

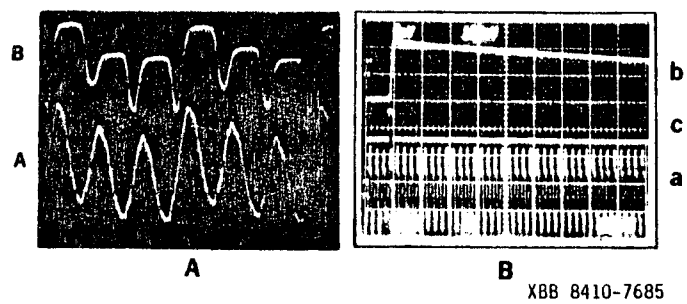

Fig. 9. A. Fraction of video line at 40 MHz. Bottom: video amplifier output. Top: video peak stretcher output. B. Fraction of a line at 40 MHz. Bottom: video amplifier output. Middle: single pixel strobe. Top: single pixel amplitude at the output of video peak stretcher.

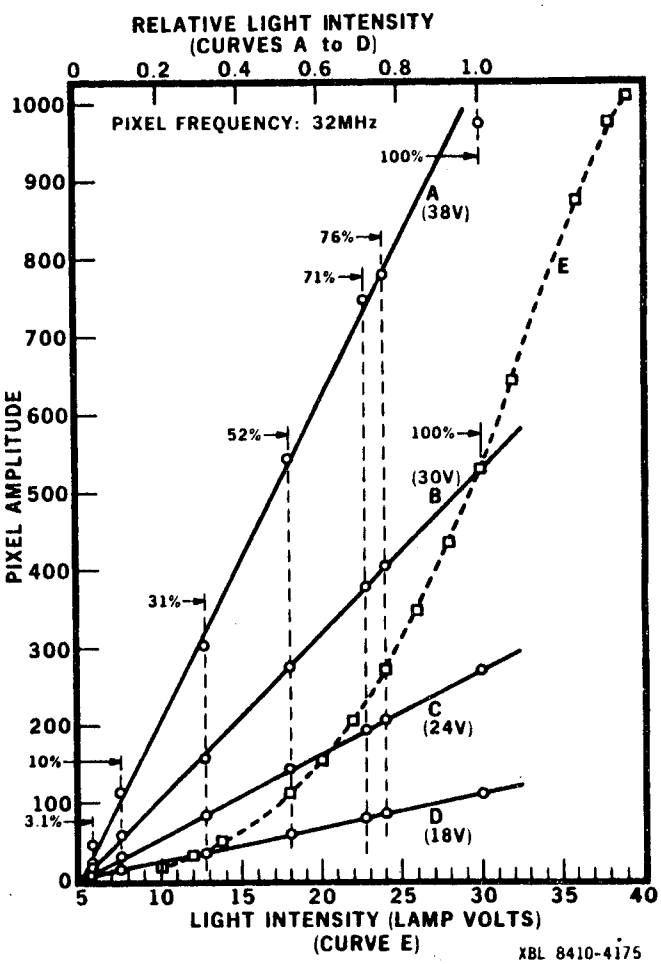

Fig. 10. Single pixel amplitude vs. light source voltage calibration at 32 MHz clock frequency (curve E, bottom scale). Linearity test with calibrated filters of pixel amplitude vs. attenuation at four points in the range between saturation and dark levels (curves A to D, top scale).

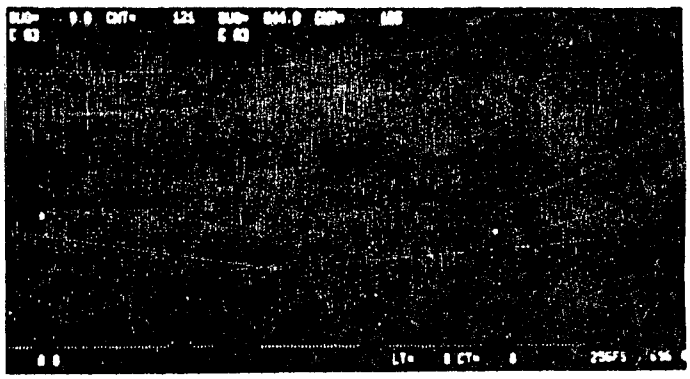

Fig.11. Single pixel amplitude distributions at 26°C, 40 MHz clock and 3.6 ms frame rate at three light intensities. First distribution on left is at dark level.

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