PETRIC - A Positron Emission Tomography Readout Integrated Circuit

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***Abstract*-- We present architecture, critical design issues and performance measurements of PETRIC, a 64-channel mixed signal front-end integrated circuit (IC) for reading out a photodiode (PD) array coupled with LSO scintillator crystals for a medical imaging application (PET). Each channel consists of a low noise charge sensitive pre-amplifier (CSA), a RC-CR pulse shaper and a winner-take-all (WTA) multiplexer that selects the channel with the largest input signal. Triggered by an external timing signal, a switch opens and a capacitor stores the peak voltage of the winner channel. The shaper rise and fall times are adjustable by means of external current inputs over a continuous range of 0.7 μs to 9 μs. Power consumption is 5.4 mW per channel, measured Equivalent Noise Charge (ENC) at 1 μs peaking time, zero leakage current is 33 rms electrons plus 7.3 rms electrons per pF of input capacitance. Design is fabricated in 0.5 μm 3.3V CMOS technology.**

I. Introduction

We are designing a Positron Emission Tomography (PET) detector module to identify 511 keV photons generated by positron annihilation with good spatial and temporal resolution. The detector module consists of a 8 x 8 cerium-doped lutetium oxyorthosilicate (Lu_2SiO_5[Ce] or LSO) scintillator crystal array coupled on one side to a 8 x 8 photodiode (PD) array of 3 mm^2 pixels, on the other to a single channel Photomultiplier Tube (PMT). Whenever a gamma ray interacts in the scintillator array, a timing and an energy signal are generated by the PMT, and an energy signal is generated in the PD array. The PMT provides an accurate timing pulse and initial energy discrimination for the 64 crystals in the module while the PD array identifies the crystal of interaction. The sum of the charges collected at the PMT end and at the PD end, PD+PMT, provides a total energy signal while the depth estimator ratio PD/(PD+PMT) determines the Depth Of Interaction (DOI) in the crystal. Fig. 1 shows the detector module.

The large number of electrons generated by the LSO crystal during gamma interaction (3000 to 5000) makes the noise due to statistical fluctuation in photon emission in the PMT negligible. The electronic noise at the PD end is important, given the constraints of the detector capacitance (~3pF), leakage current (300 pA) and data rate (peaking time ~1μs) and thus must be minimized [1]. The identification of the crystal of interaction has to occur in a short time compared to the expected period between different input events (10 μs/detector module).

PETRIC provides a unique mixed-signal solution to readout the signal from PD array through the novel on-chip integration of an array of highly sensitive amplifier channels with a Winner-Take-All multiplexer.

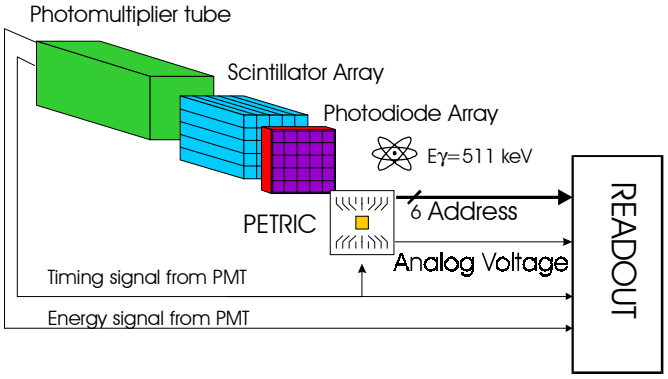

Fig. 1. Elements of the PET Camera Detector Module. The IC sits on a printed circuit board used to fan-in the PD array. The IC continuously amplifies the energy signals from the PD array and produces at its output an analog pulse whose peak amplitude is proportional to the charge collected in the channel with the largest input signal (winner channel) and the 6-bit digital address of the winner channel. The timing signal from the PMT can be used to Track-and-Hold the output analog pulse.

II. Integrated Circuit Requirements and Implementation

The use of CMOS amplifiers for PET front-end electronics was evaluated in [2]. Our IC has to simultaneously acquire input signals and perform analog and digital readout; it can be set in the desired configuration (gain, channel masking) before acquisition and readout begin. Input signals come from a 64 pixel photodiode array DC coupled to the IC; each

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photodiode has a shunt capacitance C_d of ~3 pF and a dark leakage current I_{dark} in the range of 100 to 600 pA. The IC continuously outputs the amplified pulse signal corresponding to the element of the array with the highest signal and its digital address. The peaking time and the gain must be adjustable to comply with different signal/data-rate systems. An externally generated Track-and-Hold signal stores the pulse peak voltage on an on-chip capacitor. Electronic noise should dominate; therefore it must be minimized. To achieve a reasonable Signal-to-Noise ratio the total input referred noise should be less than 200 electrons rms. Noise contributions from the electronic readout and from the leakage current of the detector have been studied extensively in the field of electronics for high-energy physic experiments [3]. Power consumption should be minimized since the module that hosts the IC does not provide cooling. We have selected a 0.5 μm 3.3 V CMOS technology with silicide block and linear capacitor options based on current availability. We have fabricated and tested a 16-channel amplifier prototype and a 16-channel WTA prototype; these prototype designs, with minimal modification, were merged and expanded to realize the 64 channel IC. Noise coefficients for 1/f noise extracted from prototype measurement showed that the 1/f noise contribution to the Equivalent Noise Charge (ENC) is relevant at our target shaping time and input leakage current.

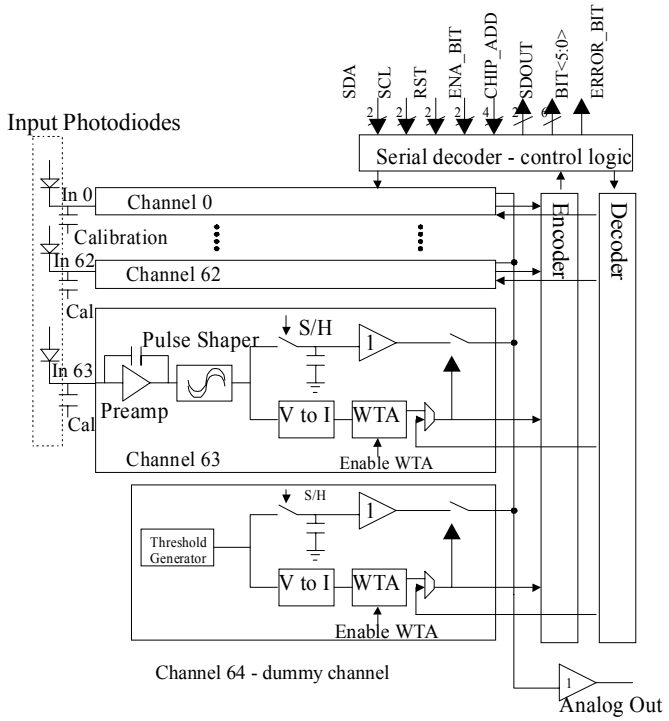

Fig. 2. PETRIC Architecture. Each channel consists of a pulse amplifier (CSA and RC-CR filter) and a WTA cell. When a WTA cell recognizes its amplifier channel as producing the largest output voltage a hit bit is generated. This bit is encoded to produce the address of the winner channel.

The chip architecture is shown in Fig. 2. Input charge signals are pre-amplified and filtered to optimize signal to noise ratio. The Winner-Take-All (WTA) circuit, DC coupled to the amplifier outputs, continuously selects the channel with the largest input and connects it to an output buffer.

A dummy channel, without an amplifier, presents a DC only voltage to the WTA and acts like a threshold that the other channels need to exceed in order to be identified as the winner. The dummy channel should be selected when no input signal comes from the PD array and prevents the WTA from switching due to electronic noise. The choice of the threshold voltage comes from consideration of several factors: the random electronic noise at the output of the amplifier channel, the noise coupling from the switching circuit to the sensitive amplifiers, the DC output dispersion of the amplifiers and the DC input dispersion of the WTA. The threshold should be large enough to prevent switching due to noise, while it should be small enough to allow identification of small signals.

Triggered by an off-chip signal, a Track-and-Hold capacitor can store the analog peak voltage. The control logic sets the preamplifiers' gains, masks individual channels form the WTA and connects a calibration circuit for testing. For minimum cross talk between the digital and the sensitive analog sections it is possible to gate the digital signal from the WTA to the encoder: in this way the encoder can be activated after the peak voltage has been stored in the holding capacitor.

III. Circuit Design and Layout

A. Amplifier Channel

The amplifier channel consists of a low-noise charge sensitive amplifier (CSA) followed by a RC-CR shaper and AC amplifier.

1) Charge Sensitive Preamplifier

The single-ended CSA consists of a common source cascode stage with regulated cascodes to boost DC gain, followed by a source follower stage. A simplified schematic is shown in Fig. 3. The input device M_{inp} is a PMOS with gate capacitance C_{inp}; the size of M_{inp} has been chosen as a compromise between 1/f noise minimization ($C_{inp} = C_d$) and thermal noise minimization ($C_{inp} = 1/3\ C_d$) [4]. The bias current of M_{inp}, given by $I_{inp} = I1+I2$, sets M_{inp} in the region of operation at the onset of strong inversion to obtain a reasonable g_m/I_{inp} ratio while achieving a high transconductance $g_m \sim 8$mS [5]. The main noise contribution to the noise of the CSA comes from M_{inp}, although the noise contribution from the current sources I1 and I2 are not negligible due to the low power supply and the limited voltage available to degenerate them [6]. The feedback capacitance C_f is placed between the input node IN and the gate of the source follower stage to avoid introduction on the closed loop of the complex poles of the follower stage and to isolate the feedback capacitor from the following stage. Switching between different feedback capacitors allows different gains to be achieved. The low-level input signal requires a small feedback capacitance to achieve a reasonable gain at the preamplifier output. With a choice of $C_f = 14$ fF for the maximum gain setting in the preamplifier, the feedback factor f, given by

$$f = \frac{C_f}{C_d + C_{inp} + C_{parasitic}} \qquad (1)$$

is f = 2.3x 10^{-3}. This small feedback factor provides high gain and relaxes the design constraints for closed loop stability, at the expense of a slower response of the preamplifier. Charge restoring is provided by minimum length PMOS reset transistor M_f (W/L = 2.4/0.6 μm) that is biased to operate in the saturation region. M_f adds negligible parasitic capacitance to the feedback capacitance, although its minimum size could result in a spread of its output resistance due to mismatch and thus channel-to-channel reset time variations. Achieved Drain to Source resistance R_{ds} is 14 to 3 GΩ in the 100 to 500 pA range; at zero leakage current the maximum achievable R_{ds} is limited by the MOS source and drain diode leakage current to 70 GΩ. The DC biasing of M_f is provided by a replica bias like in [7]. Due to the direction of the leakage current M_f operates at constant gate-to-source voltage; a large spread in the leakage current dictates adjustment of the bias on a channel-by-channel basis. This is accomplished by an on-chip DAC.

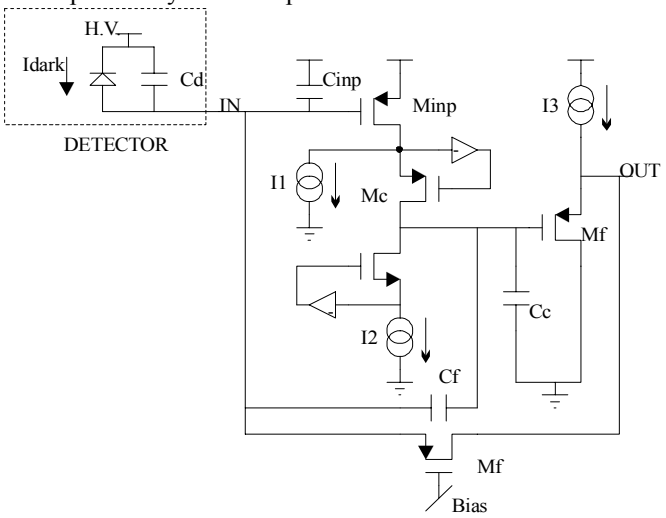

Fig. 3. Simplified schematic of the CSA. The telescopic cascode design still fits in 3V power supply but will require folding for lower voltage operation.

2) Pulse Shaper

The pulse shaper is a two stage Gm-C filter and it is a single-ended, first order version of the design presented in [8]. A simplified schematic is shown in Fig. 4. The two identical Operational Transconductance Amplifiers (OTAs) OTA1 and OTA2 that determine the time constants are based on the design presented in [9]; they use transistors operated in the triode region to degenerate their input differential pairs. The OTAs' tail current can be externally adjusted to modify their transconductance and achieve the desired shaping time. The filter is followed by an AC amplifier that provides no shaping, due to the long time constant introduced by OTA3 and its feedback capacitance; this block eases the requirements of large signal linearity of the preceding blocks at the expense of power consumption.

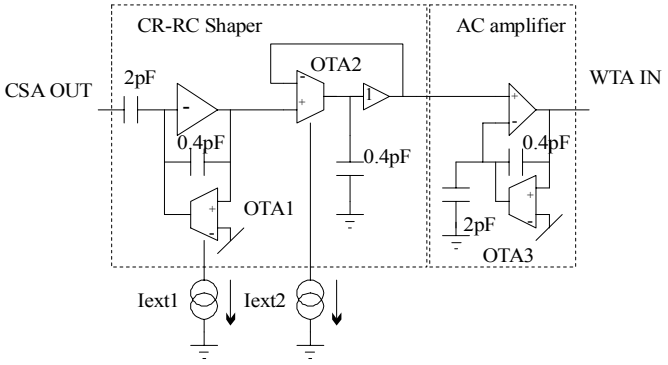

Fig. 4. Simplified schematic of the pulse shaper. Two external currents Iext1 and Iext2 are used to tune the transconductances of the OTAs and thus to change the pulse shaping time.

B. Winner-Take-All

The Winner-Take-All (WTA) circuit is DC coupled to the previous amplifier stage and is based on the design presented in [10]; it consists of a Voltage-to-Current (VtoI) converter followed by a high gain non-linear differential circuit. A simplified schematic is shown in Fig. 5. The VtoI circuit consists of a resistor followed by a common gate stage. The WTA cells in each channel share a common tail current Icom that is taken by the channel with the largest input, like in a large-signal driven differential pair. The channel with the highest input voltage has Iout = Icom while all the others Iout is ~ 0; a current comparator compares the output current of each channel to a fixed current and generates the logic signal that identifies the winning channel. Due to its high gain, the main source of error of the WTA is due to mismatch of the transistors and resistors in the VtoI. The selection circuit is designed to have a first-order response and a GBW product of 8 MHz.

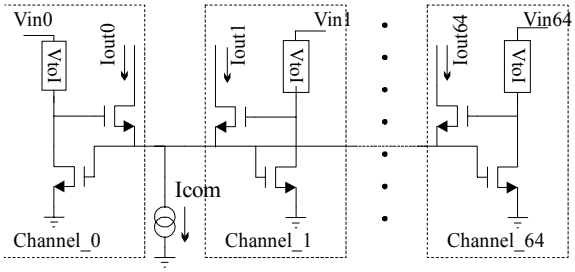

Fig. 5. Simplified schematic of the WTA. Based on a two-transistor per cell design this circuit is compact and dissipates very little power. Icom is set equal to 15 μA by an external reference.

A DC level shifter sets the DC output voltage of the dummy channel ~40 mV above the other channels.

When a switch is toggled by an external signal, the Track and Hold capacitor stores the analog voltage from the preceding stage; charge injection and clock feedthrough are minimized by a compensation scheme [11].

C. Control Logic

The digital control section has been synthesized from a state-machine diagram using standard cells. The logic uses static, fully synchronous CMOS registers. Decoding a digital

protocol based on the Xicor I2C, this logic circuit controls the gain and reset time constant of the preamplifiers, masks out unwanted channels from the WTA, connects different channels to the calibration capacitance, and produces an error bit when multiple channels are selected. The IC can be set to operate in two different modes: in WTA (default) mode the WTA selects the channel with the highest output signal. In MUX (test) mode the WTA is disabled and a channel selected by the user is connected to the analog output.

D. Layout

Fig. 6 shows a microphotograph of the realized circuit. To minimize coupling to the sensitive amplifier from the switching circuitry, separate quiet power supply lines and pads have been utilized for the input transistors' supply, the input transistors' well and the amplifier channel; the WTA, the encoder and the digital section share the same supplies. Non-power carrying substrate contact lines are employed; furthermore to take advantage of the low resistive substrate and to reduce substrate noise coupling the chip back has been gold plated [12]. The layout is pad-limited: the bond pad size and spacing have been dictated by minimum line pitch and bonding constraints on the fan-in printed circuit board that will host the IC. The die area is 4.5 mm x 4.8 mm. The capacitors in the preamplifiers are realized as Metal 1 to Metal 2 plates while all the other capacitors are implemented using the linear capacitor option, i.e. polysilicon-thin_oxide-p+diffusion. Test pads have been provided at the output of the CSAs, shapers, and AC amplifiers and to monitor the status of the internal digital logic.

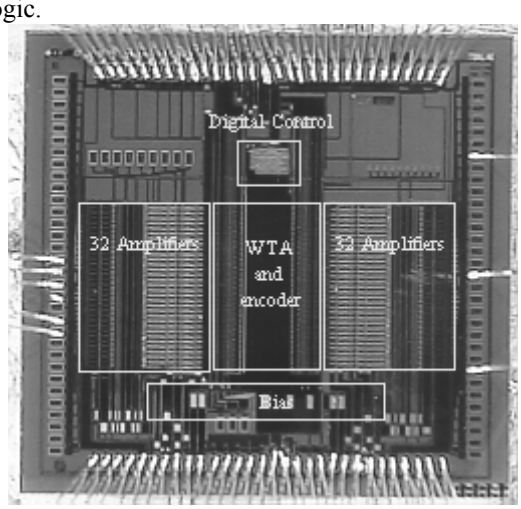

Fig. 6. Microphotograph of the realized IC. The 64 channels are split in two columns and they share a common bias; the WTA cells sit in the center, the digital control logic is on top.

IV. Performance Measurements

A. Amplifier Channel

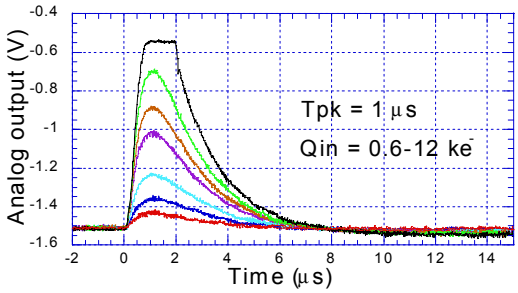

Fig. 7. Voltage output response of a single amplifier channel to different input charges.

1) Gain

We measured the gain of the amplifier's channel using external injection capacitors. Fig. 7 shows the waveforms present at the analog output when different charges are injected into one amplifier. At maximum gain setting (120mV/ 1000e$^-$), 1μs peaking time (achieved with equal RC and CR time constants in the shaper), detector capacitance C_d = 3.7 pF, the gain is linear within 1% in the range of 750 to 4000 electrons input charge. For higher input charges (5ke$^-$ to 9ke$^-$) the non-linearity of the pulse shaper degrades the performance and finally the output stage enters into saturation for input charges bigger than 9ke$^-$.

Using the internal calibration circuit we have measured 3% relative rms gain dispersion between channels on the same IC.

2) Pulse Shaping

Adjusting the external currents shaping times are achievable in the range of 0.7 to 9 µs as shown in Fig. 8.

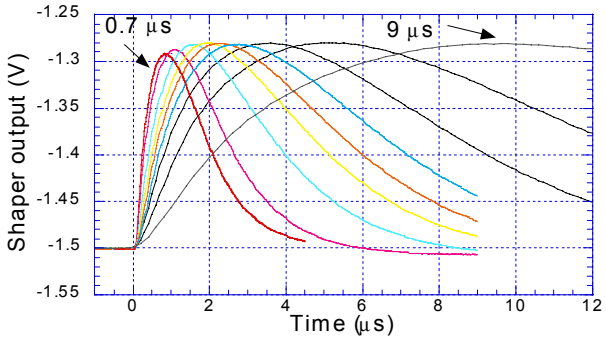

Fig. 8. Voltage output response of a single channel to an 1800 electrons input charge for different values of the external current sources of the shaper stage.

3) DC Output Offset Voltage

The DC dispersion at the output of the amplifier channel is determined by the input random offset of the feedback transconductor of the AC amplifier. Measurements show a value for the DC offset variation of 8 mV rms.

4) Electronic Noise

Noise measurements were performed on a test board, since a detector module was not yet available at the time of publication of this paper. The characterization of the chip noise performances was carried out on both unbonded

channels (no external load) and on channels that were bonded to outside loading capacitors. Input ENC was measured on each channel as the standard deviation of the output peak voltage distribution, assumed to be gaussian. In Fig. 9 the results of the measurements are plotted as a function of the input external capacitance at a filter peaking time setting of 1µs. Even if these data do not take into account any leakage detector current, the results confirm noise performances well below the required 200 electrons specification for a foreseen 3pF load. Noise performances were also measured as a function of the filter peaking time setting, as plotted in Fig. 10, to extrapolate the 1/f noise floor limit, for three different input capacitances. The data in this plot report a dominance of white noise contribution until 10µs peaking time and confirm an ENC scaling with capacitance equal to 7.2 electrons per pF. As a crosscheck, input referred noise spectral density was extracted from measurements and compared to the expected one. In a linear system the input referred noise charge can be expressed as

$$ENC^2 = S_W \frac{A_1}{\tau} C_{TOT}^2 + A_2 C_{TOT}^2 S_{1/f} + A_3 \tau S_{//} \quad (2)$$

where S_W is the input noise spectral density, A_1 is the white series noise coefficient, A_2 is the 1/f series noise coefficient, A_3 is the parallel noise coefficient, Ctot is the total input capacitance and τ is the filter peaking time [13]. At 1µs peaking time, the filter bandwidth is large enough to assume that the white noise contribution to the total input noise is dominant, in absence of parallel noise. The relation between ENC and input capacitance is linear and the input white noise spectrum can be inferred from the measurements.

$$S_w = \frac{\tau}{A_1}\left[\frac{\partial ENC}{\partial C_D}\right]^2 \quad (3)$$

With a measured A_1 value close to 1, the preamplifier input white noise spectral density is 1.3 nV/√Hz in agreement with the simulation results. Data in Fig. 10 confirm the result, with and extracted 1.4 nV/√z against an input device simulated noise of 1.2 nV/√Hz.

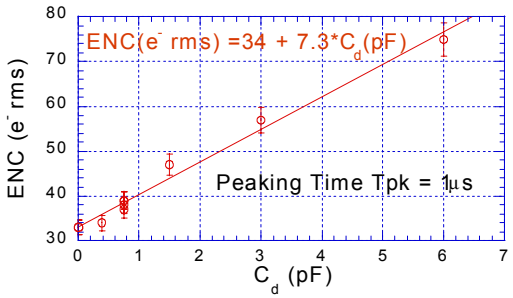

Fig. 9. ENC vs. peaking time for different detector capacitances.

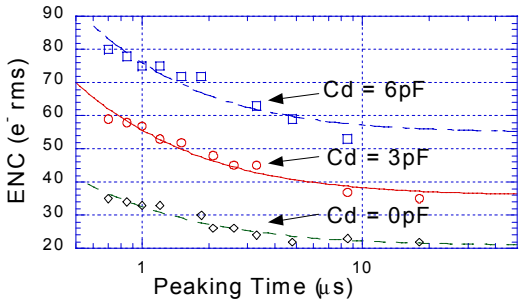

Fig. 10. ENC vs. detector capacitance Cd at 1 µs peaking time. Data are fitted neglecting the parallel noise contribution.

B. Amplifiers and Winner-Take-All

1) Channel Selection

The WTA selects the input channel with the highest dc voltage in less than 150 ns, connects it to the analog buffer amplifier, and outputs the digital address bits of the winning channel. In Fig. 11 two recognizable RC-CR shaped pulse are shown at the analog output of the IC. The time that the WTA takes to identify the winner channel is the sum of the switching times of the WTA cell, the current comparator and the decoder.

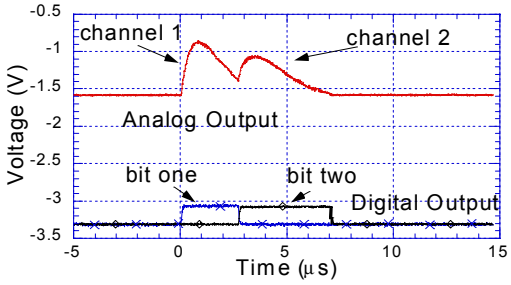

Fig. 11. Two different input signal charges are injected in two different channels. The first signal Q 1 is injected at time zero while the second signal Q2 (Q1 > Q2) is injected after ~ 2.5 μs. The analog output tracks the pulse generated by Q1 until the pulse generated by Q2 becomes higher in voltage. The digital output bits toggle accordingly.

2) Input DC Threshold Dispersion

Connecting two channels at the time to the WTA, one channel with no input signal and the dummy threshold channel, we have varied the threshold channel voltage until the other channel would be identified as the winner. We have measured 20 mV rms DC dispersion at the input of the WTA. This value is the sum of the output dispersion of the amplifier channel and of the input dispersion of the WTA channel. Since the measured DC output dispersion of the amplifiers is 8 mV rms it is the WTA circuit input dispersion that dominates. When no input signal is present at the amplifier inputs, the dummy channel is always selected as the winner by the WTA.

3) Track-and-Hold

The output analog voltage of the amplifier channel is stored in a 400fF holding capacitor when the hold signal is received by the IC. Track-and-Hold operation is shown in Fig. 12. The measured voltage error in the holding capacitor due to clock

feedthrough and charge injection is less than 4 mV; the error is signal dependent and could be minimized increasing the holding capacitor size from its current value, at the expense of loading the previous stage.

The performances of the IC are summarized in Table I.

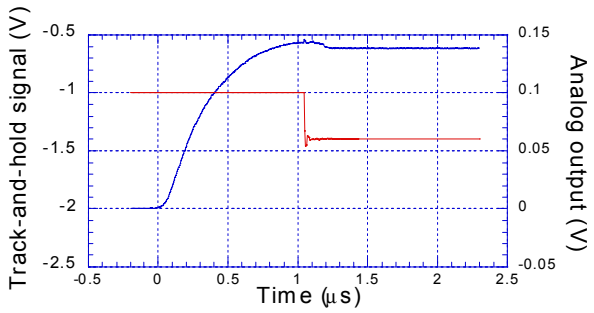

Fig. 12. The analog voltage is stored in the holding capacitor when the Track-and-Hold signal toggles.

TABLE I
SUMMARY OF THE IC'S PERFORMANCES

Technology	CMOS 0.5 µm 3.3 V
Die Area	4.5 mm x 4.8 mm
Leakage Current	30 – 600 pA
Detector Capacitance	3 pF
Number of Channels	64
Max Gain	120mV/1000e$^-$
Min Gain	40 mV/1000e$^-$
Shaping	0.7 to 9 µs unipolar
Noise at 1µs Tpk	34 + 7.2*Cd(pF) e$^-$rms
Power	5.4 mW/Channel

V. CONCLUSIONS

Compactness, high performances and flexibility make PETRIC a unique and ideal solution for PET camera modules front-end readout. Due to the flexibility of its architecture and of the analog front end, the IC is well suited for any application employing low capacitance PD detectors in moderate to high data rate environments and it is currently considered for single photon cameras readout [14].

Future directions of this work include on-chip integration of a peak detection circuit and band-gap voltage reference, a self-adjusting reset scheme in the preamplifier and a characterization of the Electro Static Discharge (ESD) protection structures for production development.

VI. ACKNOWLEDGMENT

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