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Two-dimensional semiconductor and heterostructure for novel electronics and optoelectronics



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# Two-dimensional semiconductor and heterostructure for novel electronics and optoelectronics

A dissertation submitted in partial satisfaction of the

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Material Science and Engineering

by

Jian Guo

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ABSTRACT OF THE DISSERTATION

Two-dimensional semiconductor and heterostructure for novel electronics and optoelectronics

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Doctor of Philosophy in Material Science and Engineering

University of California, Los Angeles, 2019

Professor Yu Huang, Chair

The success of carbon nanotubes and graphene drives people to continuously search for novel low dimensional materials. Among the various discovered two-dimensional (2D) materials, 2D semiconductors (2DSCs) has been most extensively studied due to their unique electronic, optoelectronic, and mechanical properties. In terms of fundamental semiconducting performance, the ultra-thin body of 2DSCs enable strong electrostatic gate control, which is favored for high output current and ultra-low leakage current for field effect transistors. Meanwhile, the atomic thin film of 2DSCs is free of dangling bonds due to its layered structure, which contributes to low interfacial density of state and sharp turn on of density of states at the band edges. Those electronic properties are specially desired for short channel field effect transistor and tunneling transistor. Besides, the layer dependent band structure offers tremendous options for opto-excitation detection and heterostructures. However, the research of 2DSCs is limited on transition metal dichalcogenides (TMDCs) such as $MoS_2$ and $WSe_2$. Experimental studies of 2DSCs on

other group compounds has little been reported. Besides, detailed studies of charge transport in 2DSCs transistor in both lateral and vertical direction requires further understanding; studies on metal/semiconductor contact and interface engineering in 2DSCs heterostructure potentially enable fascinating electronic functions.

In this thesis, I will present my effort on uncovering a new group of 2DSCs, charge transport in 2DSCs transistor and their heterostructure with either other 2DSCs or metals. I will include the work from two of my first author publication. I will first present my research studies on characterizing a new group of 2DSCs from IV-V group compound, 2D GeAs for the first time. By examining the semiconducting properties of few-layer GeAs transistors, we achieve high ON-OFF ratio of $10^5$ and maximum hole field-effect mobility of 99 $cm^2$ $V^{-1}s^{-1}$at room temperature. Due to highly anisotropic crystal structure, highly angle dependent optical and electronic transport is also observed. To reveal the intrinsic carrier transport, we carried out systematic studies on Schottky barrier and contact resistance. The intrinsic mobility proves charge impurity scattering limited transport of GeAs transistor. At last, we demonstrate mid-infrared photodetector by utilizing the band gap of GeAs crystal. Then I will show our investigation of charge transport in multilayer $MoS_2$ transistor with optimized van der Waals contact. For the first time we demonstrate a vertical built-in potential in 2DSCs that induces negative transconductance (NTC) behavior. By varying measurement temperature, body thickness and terminal numbers, we reveal that the NTC originates from the vertical barrier due to distinct doping type and carrier distribution. We further demonstrate a frequency doublers and phase shift keying circuits based on single transistor by utilizing the NTC phenomena. Furthermore, I will present a study on tunneling transistor based on 2DSC SnSe/GeAs heterostructure. By stacking two flexible n-type and p-type semiconductor, we acquire a hetero-pn junction. The cryo-temperature study of the

heterostructure proves a type III band alignment and Esaki type diode, which indicates intrinsic tunneling current at low bias. The subthreshold swing and gate coupling efficiency has also been discussed. For the final part, we will discuss about a novel approach to enable memristive switching behavior on metal and 2DSCs interface. With alignment transfer technique, we can integrate active metal with fragile 2DSC without introducing any destruction on 2DSC. Due to gentle interdiffusion of active metal and native oxide on 2DSC surface, a resistive switching layer forms and enable switching with ON/OFF ratio up to three orders. Resistive random-access memory and synaptic modulation has been realized with our metal/oxide/2DSC memristor. Moreover, we examine the working principle of our memristor and propose the formation and dissolution of metal oxide as the working mechanism. These findings and engineer could provide exciting opportunities for 2DSCs for novel electronics and optoelectronics.

The dissertation of Jian Guo is approved.

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## Biography

Jian Guo received his B.S. and master's degree in electrical engineering and Computer Science from Peking University, Beijing, China in 2011 and 2014. He joined Dr. Yu Huang's group in 2014 and conducted the research of two-dimensional semiconductor for novel electronic and optoelectronics. He was awarded UCLA graduate division Fellowship from 2014 to 2015. He has 2 first-author and 6 co-author papers published in peer-review journals. His research interests include electrical and optoelectrical properties of two-dimensional semiconductor.

## INTRODUCTION

Following the discovery of graphene, emerging studies of diverse electronic and physical properties has demonstrated enormous success of two-dimensional (2D) materials. In contrast to their bulk parent materials, atomic thin body gives 2D materials perculiar and exciting properties. For graphene, single layer structure brings excellent electronic[1, 2, 3], mechanical[4], and thermal[5] properties. However, its zero-band gap[6] limits the application as signal switching device for logic circuits. The desire for sizable band gap materials with atomic thin thickness drives people to continuously search for novel two-dimensional semiconductors (2DSCs). Among the explored 2DSCs, the metal dichalcogenides (TMDCs) is the most well-known group for their excellent stability, electronic performance, and strong spin-orbit interaction[7]. TMDCs possess layered $MX_2$ structure, in which the hexagonal lattice of cation (Mo, W) is sandwiched by two hexagonal lattices of anions (S, Se, Te)[8] (figure 1-1a). For the electronic properties, interestingly, 2DSCs present highly tunable band structure as a function of body thickness. Taking the well-studied $MoS_2$ for example, the bulk $MoS_2$ crystal has indirect bandgap of 1.29 eV while its monolayer counterpart has a direct bandgap of 1.9 eV[9] (figure 1-1b). High carrier mobility has been reported among the TMDCs, for example, monolayer $MoS_2$ shows 200 $cm^2V^{-1}s^{-1}$ with $HfO_2$ capping[10], while the monolayer $WSe_2$ based FET shows hole mobility up to ~250 $cm^2V^{-1}s^{-1}$ with subthreshold swing of ~60 mV/dec[11]. Due to the layered structure of 2DSCs, they retain no dangling bond on surface[12], resulting in low interfacial density of state and sharp turn on of density of states[13] (DOS) at the band edge, which is particularly desired for tunneling transistors. 2DSCs for field effect transistor possess inherent and superior immunity to short channel effects[14] because of their atomic thin body and suppressed depletion extension. Due to the same reason, ultra-thin body <1 nm, 2DSCs shows smaller gate screening length and strong electrostatic gate control. Another benefit from layered structure is the great flexibility for 2DSCs synthesis, dielectric deposition,

heterostructure preparation, and substrate integration without considering the traditional limitation of lattice mismatch and material incompatibilities. By the virtue of above excellent properties, 2DSCs have been well studied and utilized for field effect transistor[15], logic circuits[16], light-emitting diode[17], photodetector[18], and memories[19].

Despite tremendous efforts past years, the electrical performance of 2DSCs based electronics is still not ready for real application. There are four aspects where challenge and opportunity coexist by considering four geometric positions of a typical electronic device: intrinsic semiconducting properties of channel materials, charge transport in channel material of an electronic device, interface engineer between 2DSCs layers and interface engineer between 2DSCs layers and metal electrodes. For the first aspect, TMDCs has demonstrated excellent semiconducting properties, however, their carrier mobility is still around the order ~100 $cm^2V^{-1}s^{-1}$, merely compared to silicon device. Especially rare p-type semiconductor shows excellent electrical performance, which hinders the completion of complementary MOSFET. Thus, continuous discovering of novel 2DSCs is of great interest. Recently, the group IV and V monolayers, group IV-V and IV-VI compounds has been theoretically demonstrated. However, the experimental studies regarding novel 2DSCs and their applications of transistor has not yet been widely reported. Thus, the experimental exploring of this group of 2DSCs is appealing considering expanding of 2DSCs family. For the second aspect of challenge and opportunity of 2DSCs devices, all recent studies only focus on lateral transport since the unoptimized metal/semiconductor junction barrier notably cover up the vertical transport characteristics in the layered materials. Thus, to fully understand the charge transport in layered 2DSCs, metal and 2DSCs contact needs to be optimized and vertical transport characteristics could be ready for exploring. The well understanding of vertical transport in layered semiconductor can bring opportunity for novel functioning device. For the third aspect, which is the interface engineer

between 2DSCs layers, opportunity has been proved by studying the heterostructure with stacked two distinct type of 2DSCs with van de Waals atomic sharp interface. P-N heterojunction has demonstrated superior light detection, emitting performance, and unique interlayer interaction. Because of abundant options of band alignment of P-N heterojunction, careful selection could enable type III band offset, which is desired for tunneling transistor. However, little work has been done by utilizing 2DSCs heterostructure for tunneling transistor, which leaves us a fantastic opportunity. For the fourth aspect, which is the engineer of 2DSCs and metal interface, special integration technique enables memristive switching between the 2DSCs and metal interface. By manipulating the native layered structure of 2DSCs and vertical transports, we could explore novel memristive device with low working voltage enabling random access memory and neuromorphic computing.

In this thesis, my work will focus on the discussed four aspects of challenges and opportunities of 2DSCs based electronic device by characterizing a new group of 2DSCs, studying the vertical charge transport in 2DSCs transistor, designing 2D heterostructures for tunneling transistor and examining 2DSCs/metal interface for memristor. I will first present the characterization of semiconducting GeAs, a new type of 2DSCs from IV-V group compound. By fabricating few-layer GeAs transistors and carrying out DC measurement, we achieve ON-OFF ratio of $10^5$ and hole field-effect mobility of 99 $cm^2\ V^{-1}s^{-1}$at room temperature. Utilizing the anisotropic crystal structure, we examine the angle dependent optical and electronic transport and achieve anisotropic ratio of mobility up to 4.2. To reveal the intrinsic carrier transport, systematic studies on Schottky barrier and contact resistance has been carried out by studying the temperature dependent DC characteristics and multiterminal devices. The intrinsic mobility after subtracting the contact resistance indicates charge impurity scattering limited transport of GeAs transistor especially at cryo-temperature. By utilizing the small bandgap of GeAs semiconductor, we

demonstrate mid-infrared photodetector and communication. Then I will show our investigation of vertical charge transport in multilayer $MoS_2$ transistor with optimized van der Waals contact. For the first time we demonstrate a vertical built-in potential in 2DSCs that induces negative transconductance (NTC) behavior. By studying the multiterminal device, we locate the NTC position at metal/$MoS_2$ and vertical $MoS_2$ region. With further examination of the measurement temperature, body thickness dependent DC behavior, we reveal that the NTC originates from the vertical barrier due to distinct doping type and carrier distribution. We further demonstrate a frequency doublers and phase shift keying circuits based on single transistor by utilizing the NTC phenomena. Furthermore, I will present a study on tunneling transistor based on semiconducting SnSe/GeAs heterostructure. By stacking n-type SnSe and p-type GeAs flakes, we achieve a P-N heterojunction with clean, van de Waals and atomic sharp contact. The cryo-temperature electrical study of the heterostructure shows a true negative differential resistance at low forward bias, which proves Esaki type diode and intrinsic tunneling current at low bias. The subthreshold swing around 121 mV/dec and gate coupling efficiency of 10% has also been discussed. For the final part, we will present a novel approach enabling memristive switching behavior on metal and 2DSCs interface. With alignment transfer technique, we can integrate active metal on top of fragile 2DSC without introducing destruction or disorder on 2DSC. Due to gentle interdiffusion of active metal and natively grown oxide on 2DSC surface, a resistive switching layer forms and enable switching with ON/OFF ratio up to three orders. Resistive random-access memory and synaptic modulation has been realized with our active metal/oxide/2DSC memristor. Moreover, we examine the working principle of the memristor and uncover the working mechanism which involves the formation and dissolution of metal oxide. Our findings and engineer of novel 2DSCs for field effect transistor, tunneling transistor and memory could provide exciting opportunities for novel electronics and optoelectronics.

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**Figures and Legends**

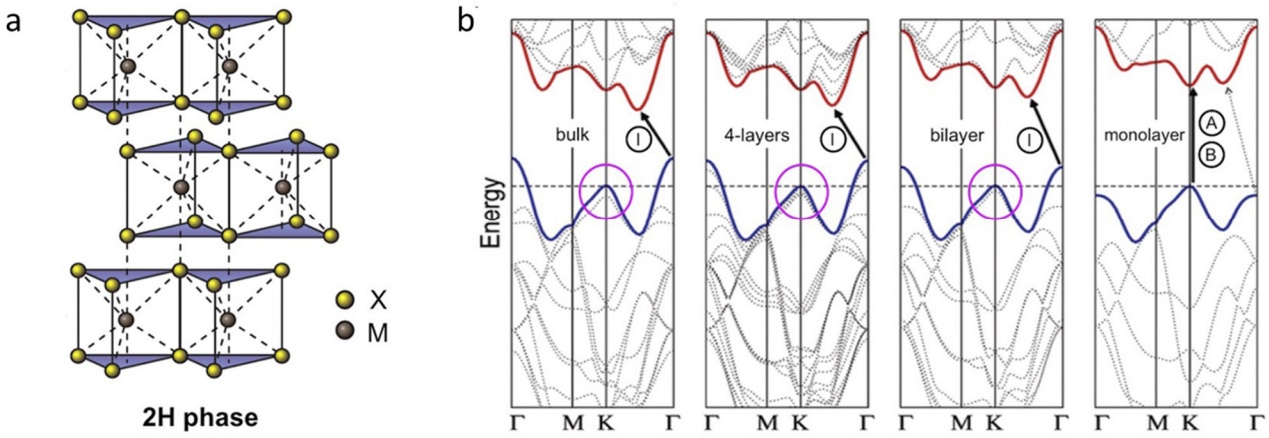


**Figure 1-1. Illustration of TMDCs crystal structure and layer number dependent band structure. a**, Schematic of the most common TMDC phases and crystal structure[20]. **b**, Changes in the electronic band structure of $MoS_2$ as a function of layer number[21]. Figures adapted from: **a**, © 2012 Nature Publishing Group. **b**, © 2010 American Chemical Society.

## Chapter I: Few-Layer GeAs Field-Effect Transistors and Infrared Photodetectors

### A. Introduction to two-dimensional semiconductor-based transistor

With the discovery and rapid rise of graphene, 2D layered materials (2DLMs) were rapidly enriched by rediscovering atomic thin properties of well-studied layered bulk crystals, [1] such as black phosphorus [2,3] and as $MoS_2$. [4] Among many 2DLMs, 2DSCs are highly attractive for their highly tunable bandgap, [5,6] atomic thin body, [7] and superior immunity to short channel effects. [8–10] For example, with a body thickness $t_{body} < 1$ nm, layered $MoS_2$ shows smaller gate screening length($\lambda = t_{body}^{0.5}$) [11] and larger bandgap (1.9 vs 1.1 eV) [12] compared to silicon, both of which will suppress short channel effects and reduce power dissipation. [13] Layered black phosphorus exhibits high carrier mobility $\mu > 1000$ $cm^2 V^{-1}s^{-1}$ [14] at room temperature, in contrast to the poor electrical performance of silicon ($\mu < 500$ $cm^2V^{-1}s^{-1}$) [15] when shrinking down to 5 nm body thickness. Importantly, the dangling-bond-free surface [16] and weak van der Waals (vdW) interaction [17] in 2DSC ensures excellent electronic properties and great flexibility in terms of 2DSC growth, [18] dielectric deposition, and substrate integration without the traditional constraints of lattice mismatch [19] and other material incompatibilities. These promising properties have intrigued continuous searching for novel 2DSCs. Recent theoretical studies [20,21] have revealed another large family of 2DSCs with tunable bandgap, which includes IV–V group compound germanium and silicon monopnictides (e.g., GeAs and SiAs). Although early studies have inspected their lattice structure, [21] bandgap, [20] Hall mobility, [22] and thermoelectric performance [23] in bulk crystals, there are no reports of electrical properties based on few-layer flakes. Here, we report, for the first time, the semiconducting electronic properties of 2D GeAs. With a back-gate geometry, few-layer GeAs transistors show high ON-OFF ratio of $10^5$ and maximum hole field-effect mobility of 99 $cm^2 V^{-1}s^{-1}$ at room temperature, comparable with that of transition metal dichalcogenides (TMD) materials. We also observe highly angle dependent optical and electronic properties in GeAs flakes. To reveal the intrinsic electronic properties of multilayer GeAs, metal and semiconductor contact was systematically studied by examining the Schottky barrier height and temperature dependent contact resistance ($R$). The extracted intrinsic mobility implies charged impurity

scattering limited transport of GeAs at low temperature. Taking advantage of the narrow band gap of multilayer GeAs, we demonstrate GeAs-based mid-infrared photodetector with considerable responsivity and fast response time. Our study here not only demonstrates a new promising 2DSC, but also expands the 2D family to group IV–V compounds that are more closely related to traditional group IV (e.g., Si, Ge) and group III–V semiconductors (e.g., GaAs).

## B. Crystal structure and optical characterization of few layer GeAs crystal

Crystal structures of GeAs bulk crystals have been well studied theoretically. Briefly, GeAs bulk crystalizes in layered GaTe structure type in the space group *C*2/*m* (No. 12). [24] As illustrated in Figure 2-1a, within each layer, Ge atoms (green) bond with one Ge atom and three As atoms (red), forming distorted As2@Ge6 octahedra. Each GeAs layer is terminated by As atoms and interacts with others by weak van der Waals forces. Interestingly, two types of Ge-Ge bonds are clearly distinguishable in the crystal structure: one type is parallel and the other one is perpendicular to the layer plane, which demonstrates anisotropic nature of GeAs crystal structure. To experimentally identify the layered structure of GeAs crystal, atomic thin GeAs film was peeled onto a $SiO_2$ substrate by micromechanical exfoliation and was then examined by optical microscope and atomic force microscope (AFM). The optical image in Figure 1b shows several ultrathin GeAs stripes successfully obtained on $SiO_2$ substrate, which present distinct optical contrast. Further study of corresponding height profile in AFM image (Figure 2-1c) identifies single, double, triple and four layers of GeAs flakes, which are marked by numbers 1–4 in both optical and AFM image. The height profile also gives a typical layer spacing of GeAs flakes around 0.65 nm, which is like those of TMDs. High resolution transmission electron microscopy (HRTEM) is then utilized to examine GeAs atomic structure. Through a proper zone axis (toward plane (25, 0, -11)), slightly distorted hexagonal structures (bright white dots) are observed (Figure 2-1d), which are projections of the vertically aligned As atoms and Ge atoms.

Raman spectroscopy is widely exploited as a fingerprint for identifying materials and powerful tool for determining crystal symmetries. A typical Raman spectrum of a multilayer

GeAs flake shows multiple peaks due to highly asymmetric structure (Figure 2-1e). Two of the most intense peaks (167 and 220 $cm^{-1}$) correspond to atomic vibrations perpendicular to the *b*-axis. [25] Angular-resolved polarized Raman spectrum is then measured. The polar plot of Raman peak at 268 $cm^{-1}$ shows anisotropic variation period of 180˚, while the peak at 272 $cm^{-1}$ reach the maximum intensities by 90 ˚ spacing (Figure 2-1f). To match the anisotropic Raman spectrum and crystal orientation, we examine the corresponding HRTEM image (Figure 2-5a, b), which suggests that the maximum intensity of peak at 272 $cm^{-1}$ corresponds to incident excitation polarizing parallel to [010] direction. Thus, the crystal orientation of GeAs flake can be readily determined via angular-resolved Raman spectroscopy. To confirm the small band gap of multiplayer GeAs, we measure its Fourier- transform infrared spectra (FT-IR) (Figure 2-5c). A sharp drop of transmission is observed starting from 1.8 um (black curve), which confirms its absorption of mid-infrared light due to small band gap. The corresponding Tauc plot of multilayer GeAs flake is also plotted (blue line) considering an indirect transition. Optical bandgap of 0.62 eV is then estimated by extrapolation (red dashed line) of the linear region to the abscissa, the value of which is close to theoretical result.[23] Other optical characterization of GeAs has not been completed due to the unstable nature of few layer GeAs flake in the air and its indirect band gap for all thickness.

### C. Performance of GeAs field effect transistor at room temperature

We have next carried out systematic investigation of the electronic properties of GeAs flakes. Theoretical work has reported that bulk GeAs has a calculated indirect bandgap of 0.57 eV [23] that can expand to indirect bandgap of 1.66 eV [26] when shrinking down to monolayer thickness. To characterize the electrical properties of GeAs, we fabricated back-gated field- effect transistors using multilayer GeAs flake as the channel. Because of the metastable nature of GeAs under ambient conditions, single-layer GeAs transistor on $SiO_2$ shows poor electronic performance. Therefore, we focus our investigation on few-layer GeAs transistors. GeAs flakes with various thicknesses were exfoliated from the bulk crystal and then transferred onto a p++ silicon substrate with 300 nm thermally grown silicon oxide. After patterning contact via e-beam lithog- raphy

technique, metallization was performed by evaporating 20 nm/50 nm Ni/Au on GeAs flakes. Schematics of a finished GeAs transistor is illustrated in Figure 2-2a. Left panel of Figure 2-2b shows a SEM image of finished GeAs transistor for transfer length method (TLM) test and right panel shows an optical image of finished GeAs transistors for angle-resolved transport measurement, which are discussed in detail below.

The transfer and output characteristics of typical few-layer (5–10 nm) GeAs transistors are first measured at room tem- perature under vacuum of $10^{-5}$ Torr. By sweeping gate voltage from 60 to -60 V, GeAs transistors are turned ON at threshold voltages of ~-10 V (Figure 2-2c), indicating p-type electrical trans- port. Note that the ON–OFF ratio of few-layer GeAs transistors current exceeds 105 at room temperature at bias of 1 V, which is enough for typical logical electronics. With detailed investigation, we found that the ON–OFF ratio drops when body thick- ness becomes thicker. Specifically, multilayer GeAs transistor cannot be completely turned OFF when thickness is over 21 nm (32 layers) (Figure 2-6a). Such thick- ness-dependent transfer characteristics is commonly observed in multilayer 2DSCs transistors, in which the gate electric field depletes channel region only within Debye length, so the channel region beyond Debye length remains conductive maintains high OFF current.[27] For the output characteristics (Figure 2-2d), linear curves are observed for most negative gate voltage, which demonstrate satisfactory Ohmic contact at room temperature. Details of the metal-GeAs contacts are discussed below.

We have next extracted the field-effect mobility via linear region of transfer curve $I_D$–$V_G$ using equation$\mu = \frac{1}{C_{OX}}\frac{L}{W}\frac{dG}{dV_G}$, where $L$, $W$ is channel length and width, $C_{ox}$=11.6 nFcm$^{-2}$ is 300 nm $SiO_2$ dielectric capacitance, $G$ is channel conductance, and $V$G is gate voltage. For total 25 transistors, we plot the extracted mobility as a function of thickness (Figure 2-2e). For thickness below 6 nm, mobilities are rather low (<10 cm$^2$ V$^{-1}$s$^{-1}$) due to unstable nature of GeAs flakes in air. Considerably higher mobility values (~50–100 cm$^2$ V$^{-1}$s$^{-1}$) are observed in the 6–10 nm regime due to reduced impact on the surface degradation. It is also noted that mobility decreases again in thicker flakes (~15–50 cm$^2$ V$^{-1}$s$^{-1}$ for 10–40 nm flakes), which may be attributed to electrostatic screening effect in the thick flakes, making it less sensitive to gate field and thus leading to apparently lower field-effect mobility. Similar effect was also observed in thickness

dependent mobility studies in $MoS_2$. [28–30] It is also noted that mobility data points are scattered for a given thickness, which may be partly attributed to the highly anisotropic transport in GeAs crystals. Overall, the highest mobility reaches 99 $cm^2 V^{-1}s^{-1}$, while the average mobility is around 40 $cm^2 V^{-1}s^{-1}$. We would note the extrinsic mobility of GeAs transistor is comparable with that of typical TMDCs, e.g., $MoS_2$ transistors [4,31] without contact optimization or dielectric engineering.

Considering highly anisotropic nature of GeAs crystal structure and Raman spectrum, we investigated the angle-resolved transport in GeAs crystal utilizing the device geometry shown in right panel of Figure 2-2b. The polar plot of angle dependent field-effect mobility is plotted in Figure 2-2f with resolution of 15˚, which shows obvious anisotropic characteristics with period of 180 ˚, coincident with periodicity of Raman spectrum. The anisotropic ratio, i.e., ratio of maximum and minimum mobility is as high as 4.8, which is comparable with black phosphorus [32] and promising for the realization of novel polarization dependent electronic and optoelectronic devices. To match the maximum mobility with crystal orientation, we plot the angle resolved Raman intensity of peak at 272 $cm^{-1}$ and hole mobility in one polar plot (Figure 2-5d). The orientation of polar plot also corresponds to optical image of the device in Figure 2-2b right panel. Specifically, each data point of Raman intensity in Figure 2-5d corresponds to incident excitation on Figure 2-2b right panel with polarization along the data point and origin point. While each data point of mobility corresponds to electrical current flowing perpendicular to the direction along data point and origin point. Since maximum value of Raman intensity and mobility in polar plot is overlapping approximately, so we infer that maximum mobility is reached when intralayer current flows perpendicular to *b* direction of GeAs crystal.

**D. Exploring intrinsic charge transport of GeAs FET**

To unveil the intrinsic electronic properties of GeAs, metal and semiconductor contact, which generally dominates the electronic transport in 2DSC transistors, needs to be systematically studied and carefully excluded during analysis. Temperature dependent transport measurement gives detailed insight to electronic properties of channel material as well as contact

properties. Hence, we carry out temperature dependent electrical measurement of GeAs transistors using physical property measurement system (PPMS, Quantum Design Inc.). As shown in Figure 2-3a, upon a temperature reduction for a typical few-layer GeAs transistor, the transfer curves show a transition from p-type unipolar transport to ambipolar transport. Meantime, for a typical thick GeAs transistor, transfer curves show enlarged ON–OFF ratios as well as a transition from unipolar to ambipolar transport (Figure 2-6b). Theoretically, at low temperatures, ionization of dopants and intrinsic excitation of carriers could be suppressed. Thus, for GeAs transistors at low temperature, channel becomes more neutrally doped due to incomplete ionization of dopants and presents ambipolar transport. Meanwhile, gate tunability could be enhanced due to less populated carriers and leads to higher ON–OFF ratio. Our observation and theory are consistent with previous reports of other narrow bandgap semiconductors such as germanium.[33]

The output characteristics of typical few-layer GeAs transistors at various temperature are next studied. The $I_D$–$V_{DS}$ curves (Figure 2-3b) at gate voltage of -60 V show noticeable nonlinearity below 50 K, which is especially obvious for short channel devices. The nonlinearity normally implies barrier limited transport, which becomes prominent at lower temperatures due to insufficient thermal energy for thermal emission. To prove our inference, we extracted effective barrier height from temperature dependent source drain current in short channel device using thermionic emission model $I_{sat}= AA^*T^2\exp[-q\Phi/(k_BT)]$, where $A$ is the Schottky junction area, $A^*=4\pi qm^*k_b^2h^{-3}$ is the Richardson constant, $q$ is the elementary charge, $k_B$ is the Boltzmann constant, $T$ is temperature, $m$ is the effective mass, and $h$ is the Plank constant.[34] Richardson plot of $\ln(I/T^2)$ versus $1000/T$ (Figure 2-3c) shows negative and varied slope at different gate voltage. Effective barrier heights as function of gate voltage are then extracted (Figure 2-3d) from fitting data in Figure 2-3c. All barrier heights show positive values, ranging from 10 to 21 meV for gate voltage from -60 to 60 V. Hence, the noticeable Schottky barrier height could be the reason for inducing nonlinearity at low temperature, especially for short channel devices.

To precisely assess the intrinsic carrier mobility of GeAs transistor, we measured the temperature dependent $R$C by TLM using device structure in left panel of Figure 2-2b, Then the intrinsic mobilities are extracted from $R$C deducted transfer characteristics. Since the $R$C is highly

dependent on GeAs thick- ness, source–drain bias, and gate voltage, we choose GeAs transistor with few-layer thickness and a high ON–OFF ratio. Then total resistance is measured under fixed 0.1 V and 60 V on drain-source and gate-source terminal, respectively. The total resistance ($R$T) and extracted $R$C using TLM both continuously increase at low temperatures (Figure 2-3e), which, at first glance, indicates possible barrier limited transport as discussed above. However, after examining $R$T of various channel length, we found that $R$T of longer transistor (green dots in Figure 2-3e) is significantly higher than $R$C at all temperature region. It means that $R$C is only a minor portion of $R$T for longer channel transistor even at low temperatures. To confirm our inference, we examined the output curves of two channel length transistors at $T$=50 K (Figure 2-6c). The longer transistor (red curve) exhibits near-linear output characteristics while the shorter transistor (black curve) shows obvious nonlinearity. Thus, the potential barrier from contact is not completely limiting electrical transport in relatively long few-layer GeAs transistors. To assess the intrinsic transport at low temperature, we then deducted the contact resistance from transfer characteristics (transistor corresponding to red dots in Figure 2−3e) and obtained the intrinsic mobility without $R$C (Figure 2-3f). Obviously, the mobility excluding $R$C is considerably higher than mobility including $R$C in a wide temperature region. Thus, in this temperature region the $R$C limits the transport in shorter channel transistors. At low temperature, intrinsic mobility continuously drops due to strong charged impurity scattering, which is a common limiting factor of carrier mobility at low temperatures. Similar charged impurity scattering limited transport was also reported in other defect-rich materials including 2D and traditional semiconductors.[35–37]

**E. GeAs photodetector for mid-infrared communication**

Narrow bandgap semiconductors can enable photoresponse to mid-infrared radiation and hence are widely utilized for optical communication. Multilayer GeAs crystal has bandgap of 0.57 eV (corresponding to 2175 nm wavelength) with photon absorption range covering the mid-infrared region. We have therefore examined photoresponse of few-layer GeAs transistor under

the excitation of 1.6 μm wavelength continuous laser source. Considering the excitation wavelength is at the top end of the linear region of Tauc plot (Figure 2-5c), absorption at 1.6 μm should not be from Urbach tail[38] of a defective semiconductor. When switching the excitation with 3.5 nW power, the output current at $V_D$=2 V and $V_G$=60 V was measured. The current versus time (Figure 2-4a) exhibits a relatively short rise and fall time of 2.5 and 3.2 ms, respectively. The photoresponse is limited by the bandwidth of the current meter used to measure the photocurrent. Because of the relatively low photocurrent, a high sensitivity (20 $nAV^{-1}$) for current meter is required, which results in small bandwidth (400 Hz) with a millisecond response time. By varying the laser power, GeAs transistor shows considerable photoresponsivity ranging from 1.13 to 6.42 A $W^{-1}$ at $V_D$=2 V (Figure 2-4b). The fast photoswitching behavior and considerable photoresponsivity of multilayer GeAs transistor at mid-infrared region enables novel 2D optoelectronics for optical communication.

## F. Summary

To conclude, we examine the crystal structure and electrical properties of few-layer GeAs. The few-layer GeAs transistors show p-type transport with ON–OFF ratio of $10^5$ and highly anisotropic field-effect mobility with maximum of 99 $cm^2\ V^{-1}s^{-1}$ at room temperature. We found charged impurity scattering limits the intrinsic transport of GeAs at low temperature. Fast and intense photoresponse to mid-infrared radiation is demonstrated in multilayer GeAs transistors.

## G. Experimental Section

Bulk GeAs was synthesized from elements via solid-state synthetic methods with a 5% excess of As added, then later sublimed off using a temperature gradient.[23] The as-grown crystal cleaved into shiny, reflective, mirror-like surfaces, which were then micromechanically exfoliated

to obtain the GeAs flakes. The HRTEM images were captured using Titan scanning transmission electron microscopy operating at 300 kV after wet transferring GeAs flakes on TEM grids. The height profile of GeAs flakes was obtained by using atomic force microscope system (Dimension Icon). Raman spectrum studies of GeAs flakes were conducted using a confocal micro-Raman system (Horiba LABHR) excited by 633 nm laser and angle dependent Raman spectrum was obtained by precisely rotating sample orientation. FT-IR spectra were obtained with a Perkin-Elmer Spectrum instrument equipped with a universal attenuated total reflectance accessory. After preparing GeAs flakes on SiO2/Si substrate, two-probe contacts were patterned using electron beam lithography and followed by electron beam evaporation of Ni/Au and lift-off process. Electrical measurements at room temperature were carried out in probe-station (Lakeshore, TTP4) coupled with a precise source/measurement unit (Agilent B2902A). Temperature dependent transport was studied in PPMS (Quantum Design Inc.) under 10 Torr vacuum also coupled with Agilent B2902A. Time resolved photoresponse was studied by measuring output current while chopping (7 Hz) 1.6 μm continuous mode laser beam (Santec TSL-210V) with SR570 Low-Noise Current Preamplifier with sensitivity of 20 nA $V^{-1}$.

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## I. Figures & Legends

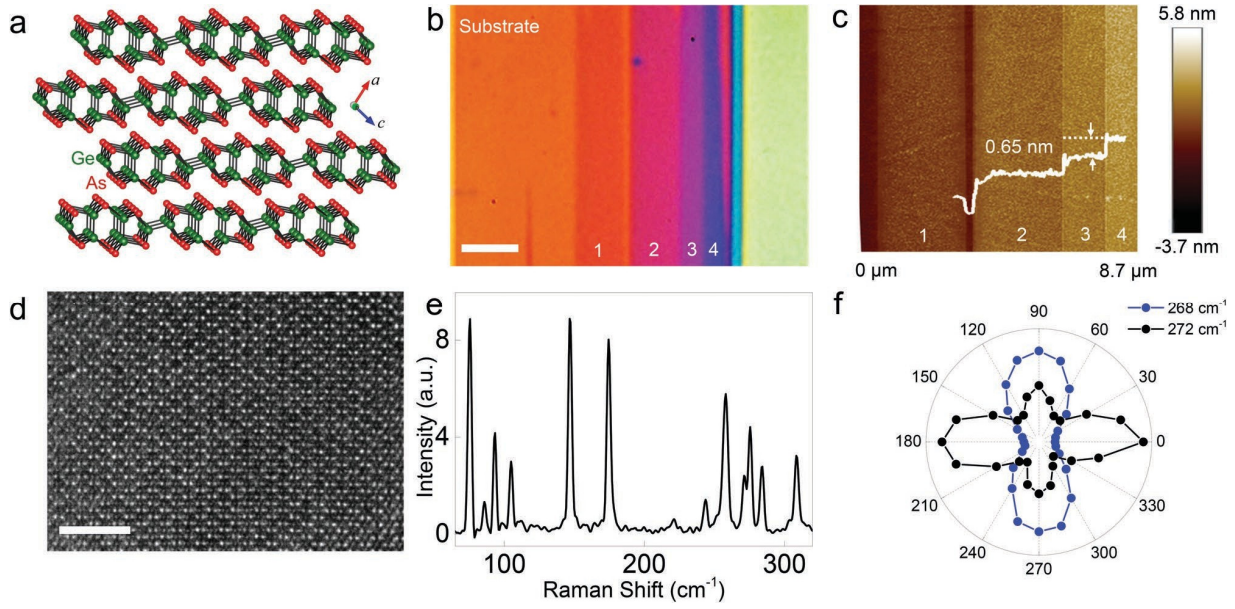


**Figure 2-1. Crystal structure, schematics and material characterization.** a, Schematics of GeAs crystal structure. b, Optical image of ultrathin GeAs flakes on $SiO_2$ substrate. Numbers from 1 to 4 mark the number of layers for each flake. The scale bar is 5 μm. c, AFM image of corresponding GeAs flakes (in b), which demonstrates atomic thin flakes with the number of layers from 1 to 4 as indicated. d, High resolution TEM image of GeAs atomic layers. Scale bar is 3 nm. e, Raman spectrum of multilayer GeAs flake using 633 nm polarized laser excitation. f, Polar plot of angle-resolved Raman spectrum at peak 268 and 272 $cm^{-1}$, which demonstrates highly anisotropic characteristic.

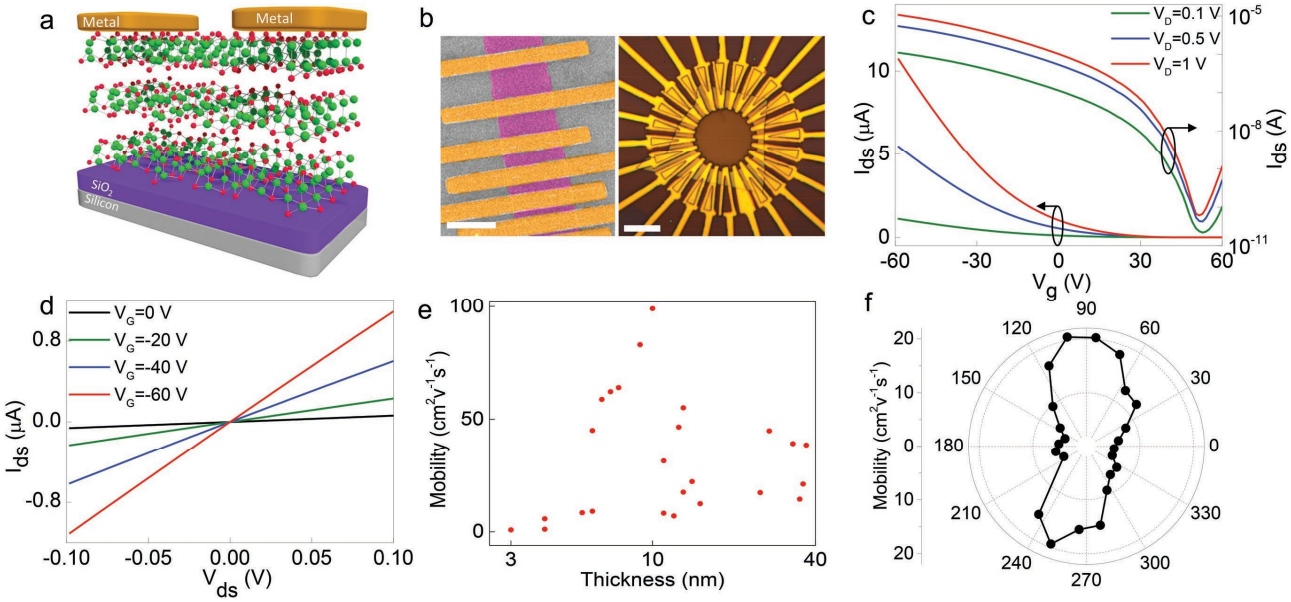


**Figure 2-2. Electrical transport of GeAs field-effect transistors at room temperature.** a, Schematics of device structure of few-layer GeAs transistor with back-gate configuration. b, The left panel is SEM image of transistor on one GeAs flake but with various channel length for TLM test. Scale bar is 3 μm. The right panel is optical image of transistors on one GeAs flake but with electrodes spaced 15˚ apart for angle dependent transport measurement. The scale bar is 10 μm. c, Transfer characteristics of a typical few-layer GeAs transistor at source–drain bias of 100 mV, 500 mV, and 1 V with linear axis on the left and logarithmic axis on the right. d, Output characteristics of few-layer GeAs transistor in (c) at various gate voltage. e, Hole mobility of GeAs flakes as a function of thickness. The highest field-effect mobility reaches 99 $cm^2\ V^{-1}s^{-1}$ and average value is around 40 $cm^2\ V^{-1}s^{-1}$. f, Polar plot of anisotropic field-effect mobility. Anisotropic ratio reaches 4.8.

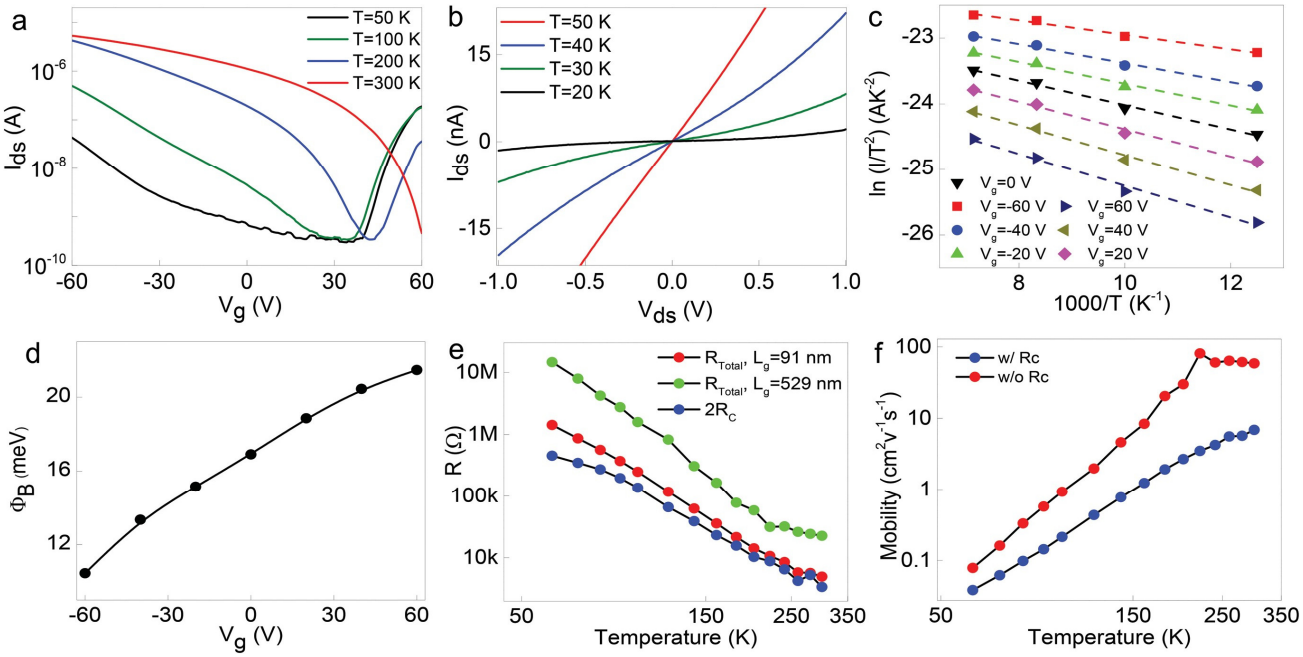


**Figure 2-3. Temperature dependent transport of GeAs transistors.** a, Transfer characteristics of few-layer GeAs transistor under various temperature. The bias voltage $V_{DS}$ is 1 V. Ambipolar behavior is observed below 200 K. b, Output characteristics of few-layer GeAs transistor under various temperature. *I–V* curve shows observable nonlinearity below 50 K. c, Richardson plot of ln(I/$T^2$) versus 1000/T for Ni/Au and GeAs contact under various gate voltage. d, Schottky barrier height versus gate voltage extracted from fitting curves in (c). e, Temperature dependent transistor resistance (red and green dots) and contact resistance (blue curve) of few-layer GeAs transistor. The red and green dots correspond to transistors of 91 and 529 nm channel length, respectively. The *R*C is extracted by transfer line method under bias and gate voltage of 0.1 and 60 V. f, Temperature dependent field- effect mobility with (extrinsic mobility) and without (intrinsic mobility) RC.

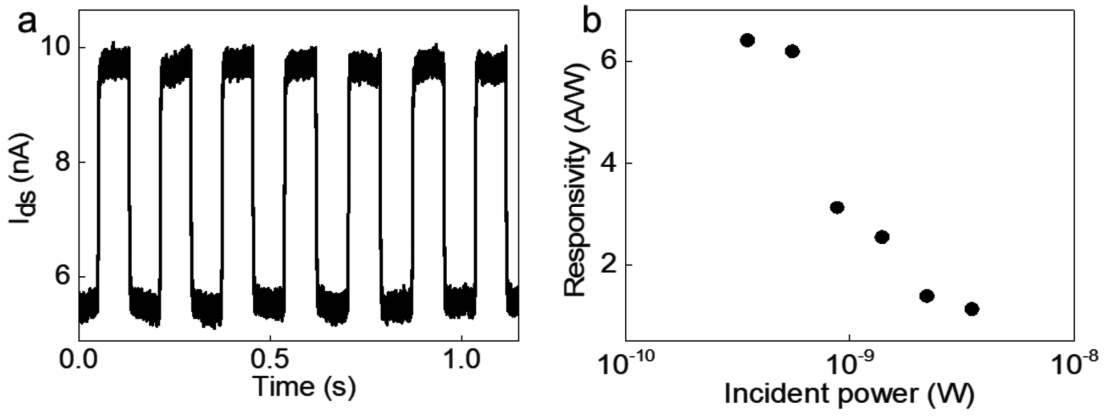


**Figure 2-4. Photoresponse of GeAs transistor to infrared 1.6 μm laser for optical communication.** a, Photoswitching behavior of GeAs transistor recorded at *V*d = 2 V and incident power of 3.5 nW. Rise and fall time of 2.5 and 3.2 ms are determined, respectively. b, Photoresponsivity as a function of incident power at drain bias of 2 V.

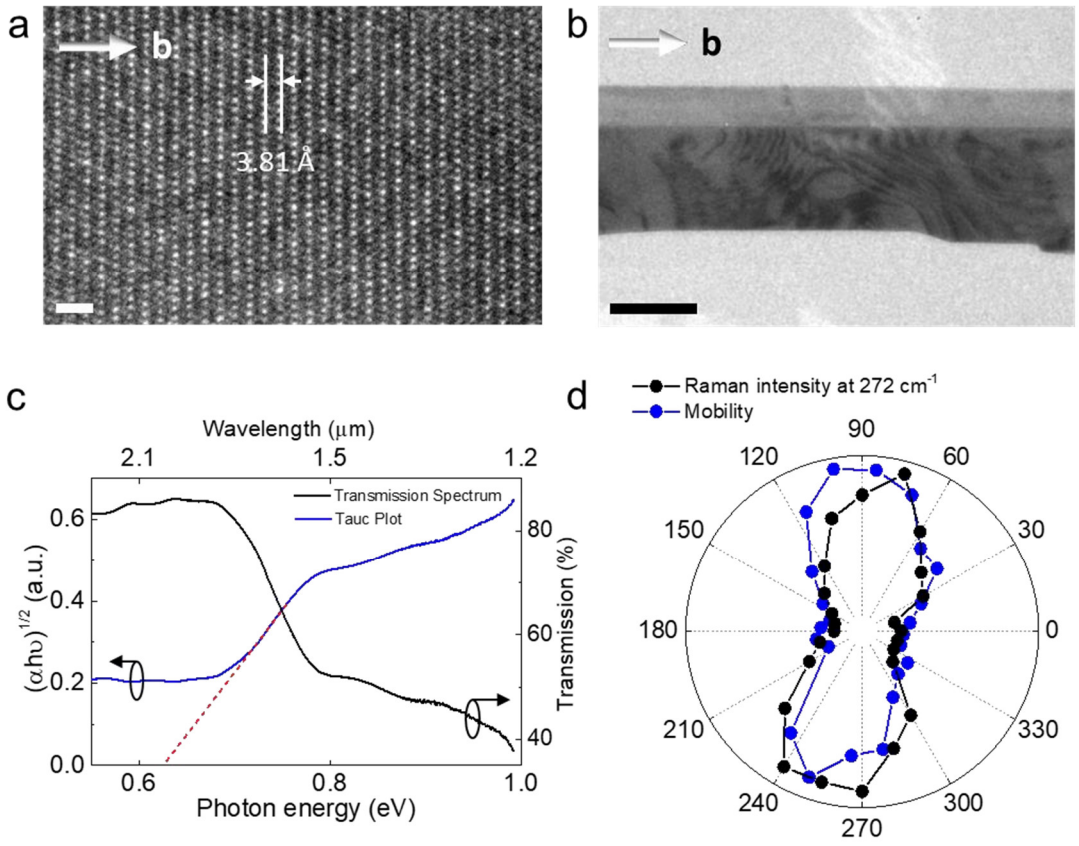


**Figure 2-5. TEM image, transmission spectrum and anisotropic behavior of multilayer GeAs. a**, TEM image of multilayer GeAs flake along zone axis [100]. The d-spacing of 3.81 Å confirms (010) planes, then b direction is determined (white arrow), which is perpendicular to (010) planes. The scale bar is 1 nm. **b**, Low magnification TEM image of multiple GeAs flake corresponding to a, which shows that b direction is along one of sample edge. The scale bar is 5 μm. **c**, Transmission spectrum and corresponding Tauc plot of multilayer GeAs flake. Optical bandgap of 0.62 eV is estimated by extrapolation of the linear region to the abscissa in Tauc plot. **d**, Polar plot of Raman intensity at 272 $cm^{-1}$ and field effect mobility with orientation corresponding to optical image in figure 2-2b right panel.

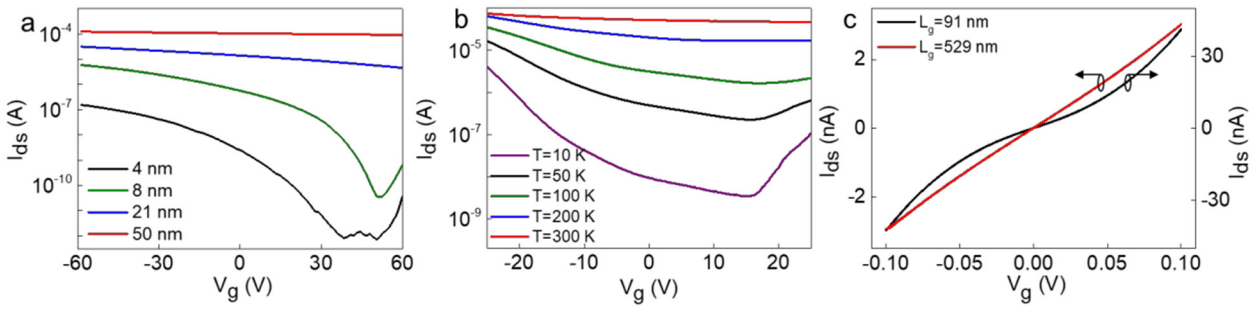


**Figure 2-6. Transfer curve of multilayer GeAs transistor at various temperature. a**, Transfer characteristics of GeAs transistors with flake thickness from 4 nm to 50 nm at Vd=1 V and room temperature. **b**, Transfer characteristics of multilayer GeAs at various temperature. **c**, Output curves of two GeAs transistors on same GeAs flake but with gate length of 529 nm and 91 nm at Vg=-60 V and T=50 K. The longer channel shows linear output characteristics while the output curve of shorter channel shows obvious nonlinearity.

## Chapter II: Vertical Charge Transport and Negative Transconductance in Multilayer Molybdenum Disulfides

### A. Introduction to charge transport in two-dimensional thin film transistor

Two-dimensional semiconductors (2DSC) are of considerable interest for their unique combination of excellent electrical, optical, and mechanical properties[1-6]. The 2DSCs typically exhibit a thickness-dependent electronic band structure, reasonably high carrier mobility[7-10] along with many other unique attributes such as coupled spin-valley physics and the valley Hall effect,[11] leading to various applications including transistors, memories, logic circuits, light-emitting diode and photodetectors.[12-21] However, the studies in 2DSCs to date have been primarily focused on lateral intralayer charge transport properties, whereas the investigation of vertical interlayer transport inside 2DSCs is limited by the unoptimized contact, where a finite Schottky barrier dominates the carrier transport due to Fermi level pinning at the metal-2DSC interface.[1,5,22] To address this challenge, graphene has been explored as a unique van der Waals contact with tunable work function to enable barrier-free contact to mono- or few layer $MoS_2$,[8,23-25] which has allowed to unveil unique intrinsic properties in 2DSCs such as ultrahigh mobility,[23] distinctive Shubnikov-de Haas (SdH) oscillations, and trend toward quantum Hall effect.8 Herein we report a systematic investigation of charge transport behavior in multilayer 2DSC transistors with optimized van der Waals contact and for the first time demonstrate a vertical built-in potential inside 2DSC (such as $MoS_2$, $WSe_2$) can dictate the vertical charge transport to result in a negative transconductance (NTC) behavior, representing a new mechanism for NTC operation besides previous theories based on quantum mechanical tunneling[26–31] and mobility degradation.[32–35] A systematical investigation of the measurement temperature, body thickness, and screening length reveals that the unique NTC behavior originates from a vertical potential barrier formed in the 2DSC from near-substrate region to bulk region due to different doping mechanisms and inhomogeneous

carrier distributions, which is distinct from conventional semiconductor with homogeneous doping defined by bulk dopants. With this NTC behavior, we further show that a single transistor can be used to create frequency doublers and phase shift keying circuits. Our study sheds light on the fundamental interlayer charge transport in 2DSC transistors and may open new opportunities for future electronic circuit design.

### B. Fabrication of $MoS_2$ transistor with optimized contact

Figure 3-1a schematically illustrates our device structure. To fabricate the device, multilayer $MoS_2$ flakes with various thicknesses are first mechanically exfoliated onto a heavily doped silicon substrate with 300 nm silicon oxide. Next, monolayer graphene grown by chemical vapor deposition (CVD) method[36] is prepatterned into 2 × 30 $\mu m^2$ stripe arrays (on a sacrifice wafer) using photolithography and oxygen plasma, and then transferred on top of $MoS_2$ flakes with standard wet transfer technique. Figure 3-1b shows the atomic force microscopy (AFM) images of a typical $MoS_2$ flake with graphene stripes transferred on top. It is noted the use of prepatterned graphene here is essential to avoid plasma etching process directly on $MoS_2$, which would otherwise cause considerable damage and greatly degrade the electrical performance of the $MoS_2$ flake.[37] Finally, a thin layer of Ni/ Au (20 nm/50 nm) was defined and deposited on top of graphene using e-beam lithography and e-beam evaporation (Figure 3-1c).

### C. Electrical transport of multilayer $MoS_2$ transistor at varying temperature

Electrical transport studies were carried out using in a physical property measurement system (PPMS, Quantum Design Inc.) at 10 Torr. Figure 3-2 shows the $I_{ds}-V_{gs}$ transfer characteristics at

various temperatures for a multilayer $MoS_2$ device with a thickness of 41 nm. At room temperature, the device displays a typical n-type transistor behavior (Figure 3-2a, black curve), which is in agreement with previous reports.[38] Interestingly, the $I_{ds}$ shows an apparent saturation at large gate voltage at low temperature (e.g., at 100 K, green line in Figure 3-2a). With further reducing the temperature below 100 K, n-type behavior cannot be retained in the high gate voltage regime and the $I_{ds}$ decreases with increasing gate voltage (Figure 3-2b), demonstrating a unique NTC and antibipolar behavior. Figure 3-2c shows the three-dimensional (3D) (semilog) plot of $I_{ds}$ versus $V_{gs}$ at various temperatures, where an evolution from unipolar (n-type) transport ($T > 100$ K) to antibipolar transport ($T < 100$ K) is clearly observed with reducing temperature.

We would like to note this novel NTC behavior is not only observed in devices using our unique graphene/metal hybrid contact, it can also be observed in conventional metal contacted multilayer $MoS_2$ system (e.g., Ti-$MoS_2$, Ni-$MoS_2$). However, their NTC signal is rather weak and can be easily overlooked due to the large contact Schottky barrier that dominates the carrier transport behavior, especially at low temperature regime. In contrast, the use of metal/graphene hybrid van der Waals contact with graphene buffer layer could greatly reduce the Fermi level pinning effect and the contact barrier[1,37,39] and enhance the $I_{ds}$ signal by over 3 orders of magnitude (at 10 K temperature), thus enabling an optimized contact to better reveal the NTC transport that cannot be explored in devices with larger contact barrier.

**D. Probing origin of antibipolar behavior in multilayer $MoS_2$ transistor**

To probe the fundamental origin of such unique transport behavior, we have first utilized multiterminal measurement to separate the resistance of channel region ($R_{channel}$) and contact region

($R_{contact}$). With increasing gate voltage, the total resistance ($R_{total}$) of $MoS_2$ transistor decreases markedly first ($V_g$ < 10 V) and then increases ($V_g$ > 10 V) (Figure 3-3a), while the channel resistance (red curve) is 1 order of magnitude smaller and always decreases with increasing gate voltage, consistent with the expected n-type behavior. The contact resistance ($R_{contact}$) shows a similar trend to $R_{total}$ and contributes >90% of $R_{total}$ at large gate voltage (blue curve). Together, we can attribute the NTC and antibipolar behavior to the contact effect within multilayer devices, excluding the possible contribution from the channel area (e.g., channel mobility degradation or thermal effects[32]). We would note that within multilayer devices the contact resistance not only includes the resistance at metal-stack−$MoS_2$ interface but also the resistance of interlayer vertical transport from top to bottom $MoS_2$ layers, which will be further discussed in detail below.

To further probe the origin of NTC at low temperature, we investigated the thickness-dependent transport properties of the $MoS_2$ transistors at 10 K. For the thin few-layer device (four layer), a typical n-type behavior is observed without NTC at large gate bias (black curve in Figure 3-3b), which is in agreement with previous low-temperature measurement results of thin $MoS_2$ transistor.[28] With increasing the thickness to 31 layers, an apparent decrease of $I_{ds}$ and NTC behavior starts to emerge in large gate voltage regime (red curve in Figure 3-3b), resulting in an antibipolar characteristic. Further increasing the thickness could make this antibipolar behavior more evident. To quantitatively evaluate the NTC behavior here, we extracted the peak-to-valley ratio (PVR) for devices with various $MoS_2$ thickness, where the PVR is defined by the ratio of maximum peak current ($I_{peak}$) versus the valley current at largest gate voltage ($I_{valley}$ at $V_g$ = 60 V,). It is evident that the PVR remains 1 for the thickness below 24 layers, indicating the unipolar n-type behavior in thin $MoS_2$ devices (Figure 3-3c); with further increasing the thickness of $MoS_2$, the PVR rises over 1 and with a maximum value of 47 observed in a 71-layer $MoS_2$ device. It should also be noted that although the channel width of $MoS_2$ transistors could have an effect on

the exact value of Ipeak and Ivalley but would not significantly impact the PVR. The variations of the PVR observed in our devices with a given thickness (Figure 3-3c) could be attributed to the differences in $MoS_2$ flake quality or contact resistance.

The observation of NTC and multiterminal measurement presented in Figure 3-3a clearly indicate that there are two competing transport mechanisms within multilayer $MoS_2$ system: a thickness irrelevant lateral n-type transport in the channel area, and a thickness dependent interlayer vertical transport in the contact region due to interlayer screening.[40,41] The critical screening length λ of multilayer $MoS_2$ is determined to be 27.8 nm (~42 layer) by conducting capacitance−voltage ($C-V$) measurement of a typical metal-oxide-semiconductor (MOS) capacitor made from multilayer $MoS_2$ (Figure 3-3d).[42] With the screening length determined, we can plot the band diagram in Figure 3-4a,b. For monolayer or few layer $MoS_2$ with the thickness smaller than the screening length ($t < \lambda$), the carrier concentration and Fermi level inside the entire $MoS_2$ body can be well controlled by gate, demonstrating a monotonically increased $I_{ds}$ with gate voltage and a typical unipolar n-type behavior (Figure 3-4a). In contrast, in thicker multilayer $MoS_2$ ($t > \lambda$), the carrier transport will be separated into two regions in the vertical directions of $MoS_2$, where the region near the bottom substrate (red color, Figure 3-4b) will screen the applied electrical field, leaving the top bulk region (blue color, Figure 3-4b) intrinsic regardless of gate voltage. We would note top regime inside bulk $MoS_2$ is intrinsically lightly p-doped, as reported in bulk molybdenite crystal,[43,44] and confirmed from our hall measurement. In addition, the lightly p-doping in bulk region of $MoS_2$ transistor is also consistent with previous literatures,[45,46] where the transfer curve from n-type to p-type is observed by increasing $MoS_2$ thickness. The lightly p-type doping in top bulk regime is opposite to the bottom substrate region, which is normally n-doped due to the presence of positively charges in the oxide substrate[47,48] and the resulting surface sulfur vacancy.[49,50] The p-type doping in bulk region and the doping mechanisms of $MoS_2$ is further

discussed. Thus, a vertical potential barrier is naturally formed inside the $MoS_2$ due to the inhomogeneous carrier distribution in $MoS_2$ from the bottom near-substrate region and top bulk region due to different doping mechanism, which is distinct from conventional semiconductors with homogeneous doping profile defined by ion implantation or bulk impurities. Within our theory, this vertical potential barrier is responsible for the observed unique NTC behavior (Figure 3-2) and can be confirmed from three different aspects, as discussed in detail below.

First, the barrier height can be modulated by gate voltage. With increasing gate voltage, the Fermi level of bottom $MoS_2$ will be shifted up forming larger potential barrier in band diagram (Figure 3-4b) and reducing the carrier transport from bottom to top regime, thus mimicking a p-type behavior. This vertical interlayer p-type transport in series with planar n-type transport inside channel area is responsible for the observed unique antibipolar behavior. To further confirm this theory, we measure the $I_{ds}$−$V_{ds}$ output characteristic of a multilayer device at 10 K at which temperature the NTC behavior can be clearly observed. As shown in Figure 3-4c, the shape of the $I_{ds}$−$V_{ds}$ curve changes dramatically with gate voltage. At small gate voltage ($V_g < V_{peak}$), linear $I_{ds}$−$V_{ds}$ curve is observed (Figure 3-4c, green line), suggesting the negligible potential barrier within vertical direction, as well as the optimized contact by using graphene/ metal stack. By increasing gate voltage beyond $V_{peak}$ (e.g., $V_g$ =30 V), the $I_{ds}$−$V_{ds}$ curve begins to display sublinear behavior (Figure 3-4c, red curve), a clear indication of the increased potential barrier with increasing gate voltage. Further increasing the gate voltage to 60 V leads to even larger barrier and more obvious nonlinearity in the output curve (Figure 3-4c, blue curve). We have further extracted the effective barrier height using drift-diffusion model[51] from Arrhenius plot (Figure 3-4d). Importantly, the extracted barrier height increases with increasing gate voltage ($V_g > 0$), confirming our theory of the gate controlled vertical diffusion barrier.

Second, due to potential barrier-dominated carrier transport the NTC and antibipolar effect is

also greatly influenced by the applied bias voltage $V_{ds}$. To demonstrate this, we plot the conductance of this multilayer device with various bias voltages from 10 to 200 mV at 10 K (Figure 3-4e). With increasing bias voltage, we clearly observe the transition from antibipolar to unipolar n-type behavior, which can be explained by the drain- induced barrier lowing effect and superimposed tunneling contribution. This can also be observed from the $I_{ds}-V_{ds}$ output curve (Figure 3-4c), where the nonlinear $I_{ds}$ under high gate voltage (red curve) eventually intersects and passes linear $I_{ds}$ at zero gate voltage (green curve) with increasing bias voltage.

Finally, because of the barrier nature of the vertical charge transport the antibipolar behavior is also temperature dependent. At room temperature, the carriers have enough thermal energy to overcome this potential barrier and the vertical potential barrier has negligible resistance on the overall current (Figure 3-2a, black line). However, with decreasing temperature this interlayer barrier effect becomes more and more pronounced, gradually reducing the $I_{ds}$ and finally becoming a competing mechanism with intralayer lateral transport, resulting in the NTC and antibipolar behavior at low temperature. This mechanism fits well with the phenomena observed in Figure 3-2. Besides $MoS_2$, our model of inhomogeneous doping barrier could extend to other 2DSCs such as $WSe_2$, where the NTC behavior is also observed with PVR $\sim$ 1.2.

To further confirm our proposed working mechanisms based on vertical p−n junction, we have also excluded the possible contribution to NTC behavior by gate induced vertical n−n+ junction. Although a potential barrier and space charge region also forms at n−n+ junction, the electrons are always the majority carriers and the overall current is dominated by drift current that is insensitive to the potential barrier. In this case, when the gate potential electrostatically n-dopes the bottom region of $MoS_2$ transistor, the increased electron concentration with the increasingly positive gate voltage should lead to a continued increase of the electron drift current and the thus the overall current, which is at odd with our experiment result ($I_{ds}$ decrease with $V_g$). The impact of gate

induced n−n+ junction is further quantitatively analyzed.

**E. Demonstrating analog circuit application utilizing antibipolar behavior**

With the unique NTC behavior, the sign of the trans- conductance could be changed from positive to negative, which can open up unique opportunities in analog circuit applications. For example, by connecting with a pull-down resistor, our device works as a frequency doubler. As shown in Figure 3-5a, a sinusoidal alternating current (ac) signal (±10 V) carried by direct current (dc) offset voltage is applied as the input signal, where the source electrode is connected with a 100 KΩ resistor. The transfer characteristic of $MoS_2$ devices is shown in Figure 3-5a with a peak current at gate voltage 20 V ($V_{peak}$ = 20 V). When the offset voltage is biased at $V_{offset} < V_{peak}$, the transconductance is positive and the output voltage ($V_{out}$) increases with the input ac signal. The case is opposite when $V_{offset} > V_{peak}$, where the output signal decreases with increasing input signal. In this way, local maxima and minima output signal can be achieved whenever the input signal crosses $V_{peak}$ in either direction, resulting in perfect frequency doubling when $V_{offset}$ is set equal to $V_{peak}$ (Figure 3-5b, green). If $V_{offset}$ is moved away from $V_{peak}$, the frequency doubling is incomplete, leading to partial frequency doubling and further signal tunability (red, blue curves in Figure 3-5b).

Furthermore, by using same circuit shown in Figure 3-5a, the multilayer $MoS_2$ transistor could be used to realize more complex analog signal processing circuits such as phase shift keying (PSK) circuits. The major function of PSK circuit is to modulate the ac signal in phase for digital 0 signal and out of phase for digital 1 transmission. To achieve this function using our device, the input signal ($V_p$ = 5 V) is a sinusoidal wave superimposed on a modulating square wave signal. Importantly, the output sine wave is in same phase with the input wave when the square wave is

low ($V_g$ = 10 V, 0 state) (Figure 3-5c, upper panel), and undergoes a 180° phase shifting when the square wave is high ($V_g$ = 30 V, 1 state). Further changing amplitude of the input square wave, binary frequency shift keying (BFSK) can be demonstrated (Figure 3-5c, lower panel). BFSK circuit achieves frequency doubling of ac signal only when the square wave is at high (1 state) and is a special case of frequency modulation with applications in microwave radio and satellite transmission systems. The unique advantage of the multilayer $MoS_2$ based circuit here is the simplicity of circuit design. In contrast, it requires at least seven transistors to achieves such circuit function in conventional integrated circuits, although recently reported novel structure could simplify the circuit utilizing a two different material p−n heterostructure.[52,53] In contrast, our multilayer $MoS_2$ device is based on one transistor with two competing mechanisms of interlayer and intralayer transport in multilayer 2DSCs, thus can greatly simplifying the circuit design. We note that frequency doubler and BPSK circuit demonstrated here are achieved at low temperature (10K) and may offer exciting potential in the space technology and satellite communication where low temperature is not a limitation.

**F. Summary**

In conclusion, we have observed a vertical built-in potential inside 2DSC for the first time, resulting in unique NTC behavior with an entirely new NTC mechanism. By further varying measurement temperature and body thickness, we found the vertical potential barrier is created due to the different doping mechanisms and inhomogeneous carrier distribution inside 2DSC from the substrate−2DSC interface region to bulk region, which is in contrast to conventional semiconductor with homogeneous doping defined by bulk dopants. This NTC and antibipolar behavior enables the creation of frequency doublers and phase shift keying circuits with only one transistor, greatly simplifying the circuit design compared to conventional technology.

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## H. Figures and Legends

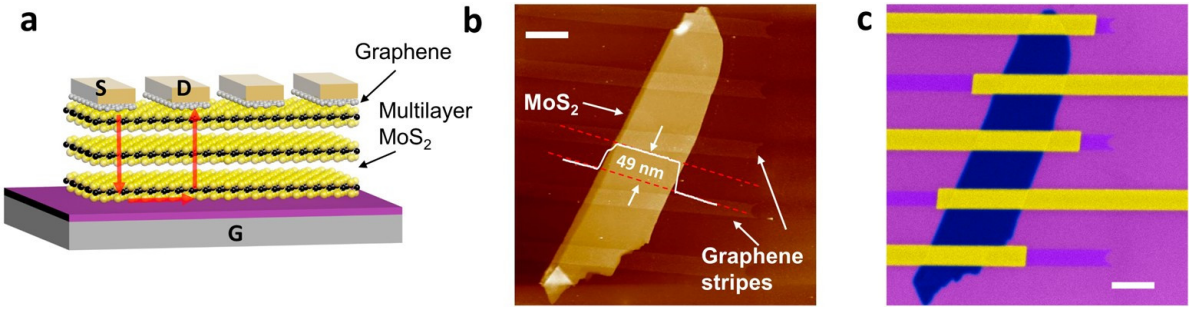


**Figure 3-1. Schematics and structure characterization of multilayer $MoS_2$ transistors using metal/graphene hybrid contact**. (a) Schematics of multilayer $MoS_2$ transistors. Three $MoS_2$ layers are used here to demonstrate its multilayer nature. Red arrows indicate the charge transport is governed by both interlayer vertical transport and intralayer planar transport. (b) AFM image of a typical multilayer $MoS_2$ flake with graphene buffer stripes transferred on top. The height of this flake is ~49 nm. (c) False-color SEM image of the final device after metal electrodes deposition. Scale bar in panels b and c is 5 μm.

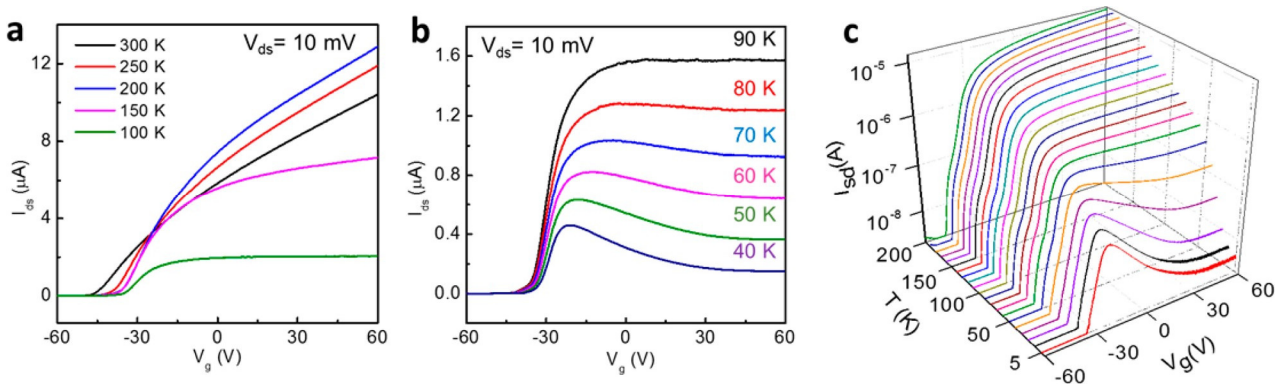


**Figure 3-2. $I_{ds}$−Vgs transfer characteristic of a typical multilayer $MoS_2$ (41 nm thickness) at various temperature.** (a) The transfer curve of this device at various temperature from 300 to 100 K with a step of 50 K. Typical n-type characteristic can be observed in this temperature regime. (b) The transfer curve of same device (in a) at various temperature from 90 to 40 K with a step of 10 K. At this temperature regime, antibipolar behavior and negative transconductance is observed. (c) The 3D semi-log plot of the $I_{ds}$ as a function of gate voltage and temperature, clearly demonstrating the evolution from unipolar (n-type) behavior to antibipolar behavior. Bias voltage is 10 mV in panels a−c.

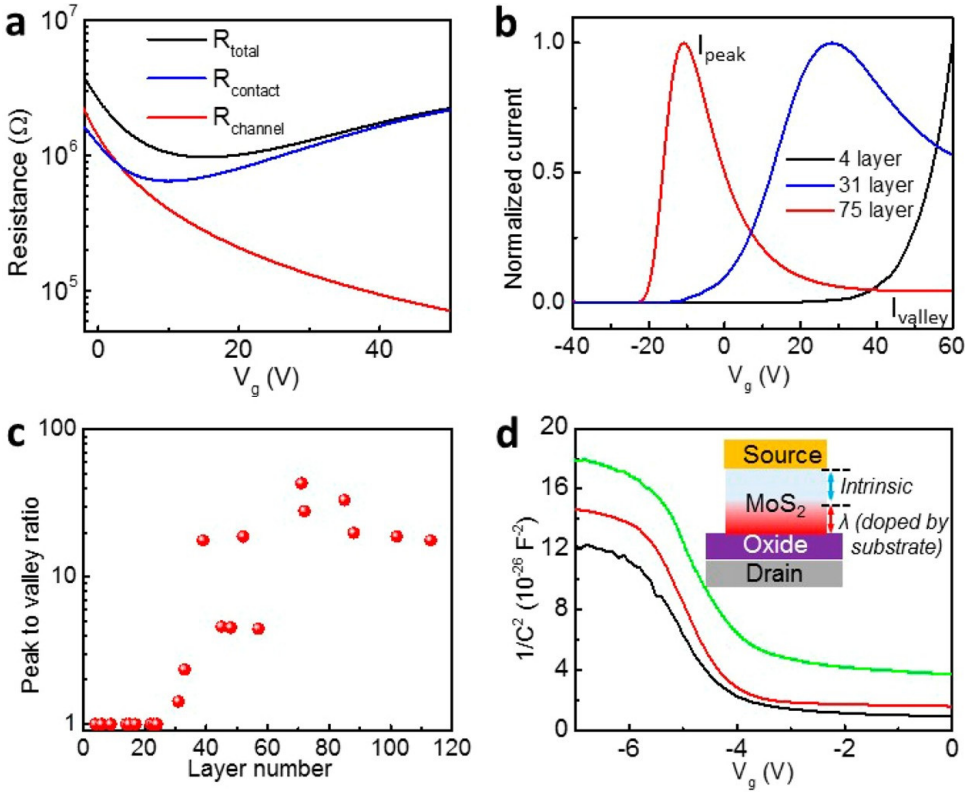

**Figure 3-3. Four terminal measurement and thickness dependent measurement of multilayer $MoS_2$ transistor.** (a) Rtotal, Rcontact, Rchannel of a typical multilayer $MoS_2$ device, measured using four terminal methods at 10 K measurement temperature. Rchannel (red curve) is 1 order of magnitude smaller than Rtotal and remains almost constant with increasing gate voltage. Rcontact (blue curve) increases parallel with the Rtotal at large gate voltage (Vg > 0), indicating the Rcontact dominates the negative transconductance behavior. (b) Normalized $I_{ds}$–Vgs transfer curve with varies $MoS_2$ thickness with 4-layer device (black curve) demonstrating typical n-type behavior and 31-layer device (blue curve) demonstrating antibipolar behavior. Further increasing the thickness could make this antibipolar behavior more obvious. (c) Peak (Imax) to valley (Vg=60 V) ratio with various $MoS_2$ thickness. (d) The measured 1/C2 with various gate voltage for a typical $MoS_2$ MOS capacitor at 10 kHz (green), 100 kHz (red), 500 kHz (black) frequency. The inset shows the device schematics, where gate-induced electrons are most populated within the Debye length (red area).

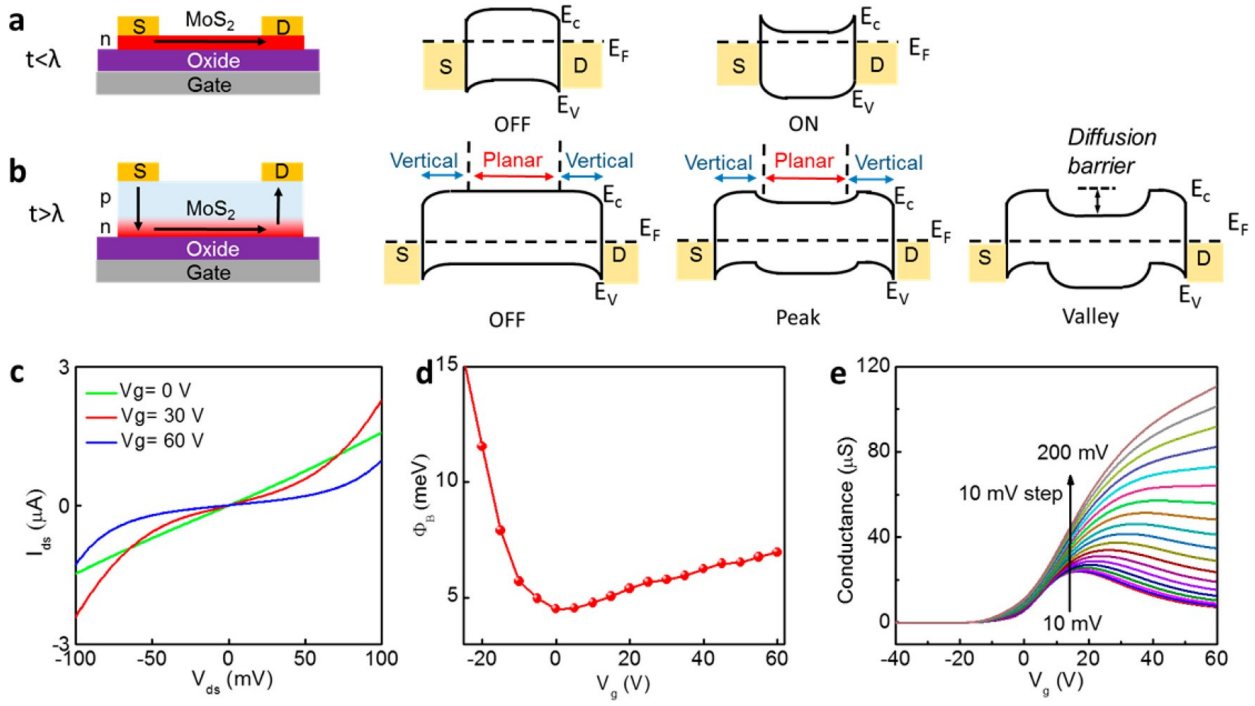


**Figure 3-4. Mechanism of antibipolar transport and negative transconductance.** (a) Band diagram of thinner (t < λ) $MoS_2$ transistors (top) under OFF and ON state. (b) Band diagram of

thicker ($t > \lambda$) $MoS_2$ transistors (bottom) under OFF, peak, and valley state. (c) $I_{ds}$–$V_{ds}$ output curve of a typical multilayer $MoS_2$ device at 10 K temperature, demonstrating linear output curve under small gate voltage (0 V) and nonlinear output curve under large gate voltage. (d) Extracted barrier height with various gate voltage. At large gate voltage, barrier height increases with gate voltage, demonstrating a p-type barrier behavior. The measurement bias voltage is 10 mV. (e) Conductance of the device under various bias voltage from 10 mV to 200 mV with 10 mV step.

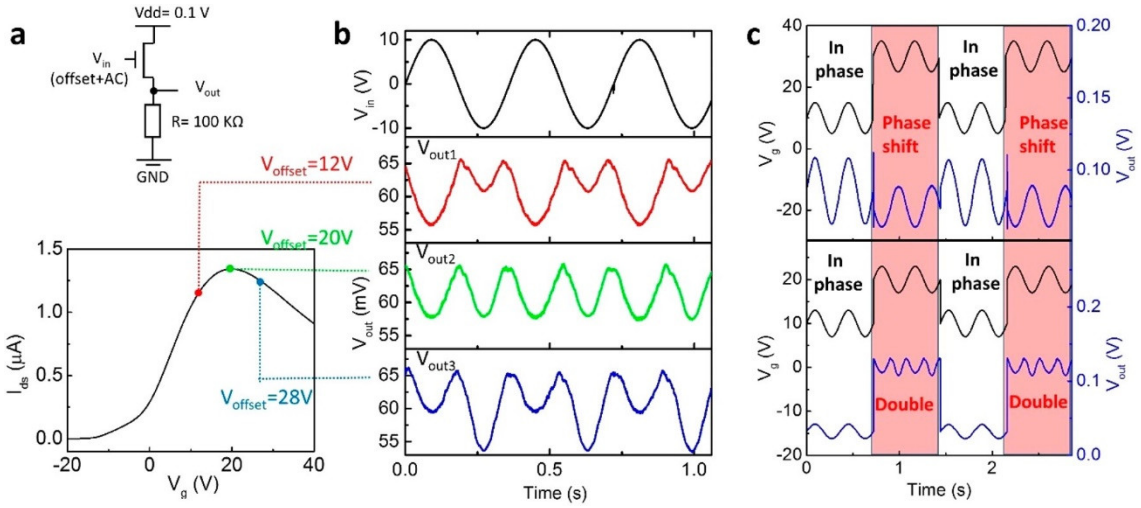


**Figure 3-5. Frequency doubling and phase shift keying circuit based on single $MoS_2$ transistor**. (a) Circuit diagram using multilayer $MoS_2$ transistor for frequency doubling and phase shifting. The circuit uses a single multilayer $MoS_2$ transistor in series with a resistor (100 KΩ). Bias voltage (*V*dd) is 100 mV and the measurement temperature is 10 K. The bottom graph is the corresponding transfer characteristic of this multilayer $MoS_2$ transistor, demonstrating NTC behavior. The offset voltage is a dc voltage, and the signal is an ac sinusoidally voltage. (b) Input ac signal (black) and three output signal for the three different values of the offset voltage indicated in panel a. (c) Binary phase shift keying (BPSK) operation using a square dc offset plus sinusoidal input. In the upper panel, the square carry voltage is 10 (low) to 30 V (high), and the output wave demonstrate a phase shift compared to the input sine wave for each half of the square wave modulation. In the lower panel, the square carry voltage is 10 (low) to 20 V (high), and the frequency of the output signal (blue) is doubled for every alternate modulation of the square wave.

## Chapter III: Tunneling transistor based on two-dimensional SnSe/GeAs heterostructure

### A. Introduction of two-dimensional semiconductor based tunneling transistor

Transistor, an electronic device for amplifying or switching electronic signal, was invented in 1947[1], and after only several decades, it evolved to ultra-large-scale integrated circuit and revolute the whole field of electronics. Among varies transistors such as junction transistor[2], Schottky transistor[3] and Avalanche transistor[4], the metal-oxide-semiconductor field effect transistor (MOSFET) dominates the today's major digital circuits market due to its low static power consumption. However, the market of mobile electronic device and Internet of things (IoT) requires ultra-low power electronics, and its tremendous growth in past decade drives the supply voltage of MOSFET to its minimum value (from 1.2 V to 0.4 V)[5] because the dynamic power consumption is proportional to the third power of supply voltage[6]. Unfortunately, the scaling down of supply voltage can't continue as wished because of dramatic increase of static power consumption due to high leakage current at off state. The fundamental reason is an existing of minimum value (60 mV/dec) of subthreshold swing (SS) of MOSFET at room temperature, which fix the maximum slop of transfer curve at subthreshold area[7]. Thus, with the same On current, the leakage source drain current will exponentially increase if lowering the supply voltage. The subthreshold swing was imposed a physical limit because of Maxwell-Boltzmann distribution of electrons[8]. To break the limitation, transistor based on distinct mechanism is proposed, among which is the tunneling transistor. A tunneling transistor is switched by modulating the quantum tunneling current through a barrier rather than thermionic emission in traditional MOSFET. By controlling the band alignment, the gate can induce overlapping of conduction band and valance band in the source and channel region, which opens a quantum tunneling window[9]. The device could switch on and off by opening and closing the tunneling window. Because of distinct

switching mechanism, the minimum SS of tunneling transistor is not limited by any distribution, thus a SS below 60 mV/dec can be achieved and the leakage current could be suppressed.

A typical CMOS based tunneling transistor possess n-i-p doping profile, where the barrier at n-i junction is modulated to open or close a tunneling window[10]. Recently, a variety of two-dimensional semiconductors (2DSCs) was discovered and utilized for novel electronics and optoelectronics. Benefiting from several advantages of 2DSCs: absence of dangling bonds, ultra-thin body, strong electrostatic gate control, sharp turn on of density of states at the band edge, low interfacial density of states and plentiful band alignment options[11], people are designing and engineering 2DSCs heterostructure based tunneling transistors. By stacking two different doping type 2DSCs, a heterostructure diode is formed. With proper band offset, an optimized band alignment between two 2DSCs can be acquired for tunneling modulation. For example, p-type $WSe_2$ and n-type $MoS_2$ heterostructure possesses type II band alignment and forms a pn diode, which shows low saturated current due to high potential barrier[12]. By applying a positive and negative voltage on the gates on $WSe_2$ and $MoS_2$ sides respectively, one can induce type III alignment, which forms a tunneling window and allows carriers to transport through quantum tunneling to switch the device to On state. Several work on 2DSCs based heterostructure for tunneling transistor have been reported, including $MoS_2$-BP[13] and $SnSe_2$-$WSe_2$[14] etc. However, most of them fail to push the SS below 60 mV/dec, and even some claims SS around 55 mV/dec but the large gate leakage current diminishes the reliability of the transfer characteristics data. Here, we present a tunneling transistor based on SnSe/GeAs heterostructure. The achieved tunneling transistor shows negative differential resistance, which indicates a type III band alignment and proves an intrinsic Esaki type diode ideal for tunneling transistor. To evaluate the performance of tunneling transistor, gate coupling efficiency and SS is also discussed. Our work enriches the strategies for designing advanced 2DSCs heterostructure based tunneling transistor

and gives an insight in interlayer interaction in two-dimensional heterostructures.

**B. SnSe/GeAs tunneling transistor fabrication and characterization**

Traditional approach such as vapor deposition and epitaxial growth for heterostructure fabrication normally encounters lattice mismatch and interface disorder issues, which prohibit its performers for tunneling transistor. However, newly discovered two-dimensional semiconductors possess low interfacial density of states and no dangling bonds making them ideal materials for tunneling transistors. Here we chose n-type semiconducting SnSe flake and p-type GeAs flake for building the heterostructure. The multilayer SnSe has been well studied as n-type 2DSCs with bandgap of 0.86 eV[15] and exhibit excellent performance for thin film transistors. While the GeAs is a newly rediscovered p-type 2DSC with band gap of 0.59 eV[16] and little studies has been done for heterostructure. Due to the large band offset, the band alignment of the two 2DSCs can be type III. Benefited by layer structure and flexibility of 2DSCs, ultra-thin flakes can be exfoliated and transferred mechanically on other 2DSCs flakes to form van de Walls heterostructure. As shown in figure 4-1a, by using scotch tape few layer SnSe is exfoliated and transferred on dielectric material. Underlying the dielectric material is conducting material for gate electrodes. The dielectric material can either be 300 nm $SiO_2$ or 30 nm $Al_2O_3$. At the meantime, GeAs flakes is exfoliated using the same approach on thin PPMA layer which is spin coated on silicon wafer, 2000 rpm 40s (figure 4-1b). Since the silicon wafer has been treated by HMDS for a hydrophobic surface, the PMMA together with GeAs flakes can be peeled off. After that, the PMMA is transferred on a PDMS stamp, and using the stamp GeAs is further transferred on SnSe flake under an optical microscope (figure 4-1c). After dissolving the PMMA layer with acetone, Ni/Au 20 nm/50 nm is deposited by electron beam evaporation to form source and drain electrodes on SnSe and GeAs flake respectively (figure 4-1d). The typical finished heterostructure device is

shown in optical image in figure 4-1e. The SnSe flake on 300 nm $SiO_2$ has green color while the GeAs flake shows yellow color. The heterostructure present large overlapping area.

**C. Electrical transport of SnSe/GeAs tunneling transistor at room temperature**

Electrical transport studies were carried out at room temperature in vacuum. Before studying the transport of heterostructure, we examine the transfer characteristics of SnSe and GeAs transistor first. As shown in figure 4-2a and b, the $I_d$-$V_g$ curves of GeAs and SnSe transistors on 300 nm $SiO_2$ proves p-type and n-type semiconductor respectively. For GeAs transistors with thicker body, the transfer curve shows lower ON/OFF ratio due to finite depletion depth. Here, we choose low ON/OFF multilayer GeAs flake for heterostructure to minimize lateral series resistance. However, for SnSe, thin body is required to allow penetration of gate electric field from the bottom to tune the interface band alignment. Thus, we choose tin SnSe flakes with high ON/OFF ratio for heterostructure based tunneling transistor.

The output characteristics of the heterostructure on 300 nm SiO2 is shown in figure 4-2c with linear y axis and in figure 4-2d with logarithmic y axis. Obviously, the output curve shows rectifying behavior with current difference more than 4 orders (figure 4-2d). Considering that bias is applied on the GeAs side, the higher current on positive bias proves a pn diode with GeAs as p-type semiconductor and SnSe as n-type semiconductor, which is consist with the transfer characteristics of GeAs transistor and SnSe transistor in figure 4-2a and b. For positive bias, gate terminal has limited control of the current (figure 4-2d) due to the short channel effect at the lateral series transport. While at negative bias, the diode is opposite biased and potential barrier dominate the transport. With applied gate voltage change from -60 V to 60 V, the current can be well tuned

from 10 pA to 100 nA, which demonstrate a well-tuned hetero-interface. We also note that at bias around 0.2 V to 0.3 V we observe a trend of negative differential resistance behavior (red circle in figure 4-2d). The trend towards negative differential resistance is an important symbol of type III tunneling transistor. To confirm type III alignment of band structure and tunneling current we continue to examine the charge transport of heterostructure at cryo-temperature.

**D. Negative differential resistance in tunneling transistor at low temperature**

After observing the towards NDR effect at room temperature, we reexamine the DC characteristics of SnSe/GeAs transistor at cryo-temperature. After cooling the temperature down to 30 K, we observe true negative differential resistance at positive bias around 0.75 V and Vg=-10 V (figure 4-3a). Obviously, the current continues increasing when applying a positive bias, but a sharp drop is observed when it reaches 0.7 V. Such drop of current induced NDR at positive bias is only possible when the diode has type III band alignment. In detail, at zero bias, the p-type GeAs and n-type SnSe already forms a broken band alignment, in which the valence band of GeAs is higher than the conduction band of SnSe (figure 4-3d), which allows electrons tunneling from the conduction band of SnSe directly to the valence band of GeAs. With increasing positive bias, the electric drives more carrier from SnSe to GeAs through tunneling while the thermal emission current is minimal because of the large potential barrier. However, the electric field also lower the band offset of the p-type and n-type semiconductor, which means the conduction band of SnSe will shift upwards relative to the valence band of GeAs. In this case the tunneling window will be closed at some bias point. This is what exactly happens when bias reach 0.75 V in SnSe/GeAs transistor (figure 4-3c) when we observe a drop of current. But if continuing to increase the bias voltage, the thermionic emission become prominent and dominate the whole transport due to lowered potential barrier (figure 4-3b), thus the current keep increasing thereafter. Our observation

of NDR justify the broken band alignment of SnSe and GeAs at zero bias, which proves the existing of tunneling current in intrinsic heterostructure interface.

By varying the gate voltage, we can shift the position where NDR happens. As shown in figure 4-4a, the NDR voltage shift from 0.75 V to 1.4 V when applied gate voltage decrease from 7 V o -15 V. This is because the fermi level of GeAs is easier to be tuned, as a result, the more negative gate voltage shift the valence band of GeAs to a higher position relative to conduction band of SnSe and the tunneling window is wider, which means a higher bias would be required to shut down the tunneling window. This illuminates us a method to evaluate the gate coupling efficiency on the interface. By plotting the NDR voltage as function of gate voltage and determine the slope, we can estimate coupling efficiency of 2.19%, which makes sense since most gate voltage drop on the dielectric layer.

**E. Subthreshold swing in SnSe/GeAs transistor**

The ultimate goal of designing tunneling transistor is t achieve a low SS. After confirming the existence of tunneling current in SnSe/GeAs heterostructure, we move on to examine the transfer characteristics using 30 nm $Al_2O_3$ as dielectric layer which owns higher gate coupling efficiency around 10%. As shown in figure 4-5b and f, an n-type transfer curve of SnSe/GeAs heterostructure indicates SnSe dominated transport which is consistent with the low ON/OFF ratio of multilayer GeAs flake. Please note that bias is applied on SnSe an GeAs is grounded in this case. One major difference of figure 4-5b from 4-5f is a much higher current at negative gate voltage, for example -2 V. This is because in figure 4-5b the diode is forward biased (figure 4-5a), the series SnSe channel dominates the transport. Thus, a more negative gate voltage is required to turn off the device. But for figure 4-5f, the diode is backwards biased, which means the potential

barrier dominate the device. At negative gate voltage around -2 V the device is turned off because high potential barrier and minimal tunneling current (figure 4-5e). When a higher gate voltage is applied, the conduction band of SnSe shift downwards and a tunneling window is open (figure 4-5d), thus, the current increases. Following this reasoning, we are supposed to see lower SS at backwards biased diode. As shown in figure 4-5c and d, the minimal value of SS (121 mV/dec) at backwards biased diode is lower than SS at forwards biased diode (400 mV/dec). We would like to note that the SS in figure 4-5c below 400 mV/dec is not reliable because of the gate leakage current. Even though we have not achieved an SS below 60 mV/dec, but a tunneling behavior has already been proved. The probable reason for high SS is the series semiconducting channel in our device and potential residuals at the heterostructure interface.

**F. Summary**

In summary, we propose a novel combination of 2DSCs for heterostructure based tunneling transistor. By exfoliating and stamping, we achieved multilayer GeAs and few layer SnSe heterostructure. The n-type and p-type semiconducting transport is confirmed by study the SnSe and GeAs transistor, respectively. For their heterostructure, rectifying behavior with high ON/OFF ratio and toward NDR effect is confirmed. To prove tunneling current existence in our device, we measure the current at cryo-temperature and true NDR is seen at temperature below 30 K. By varying the gate voltage, the NDR voltage can well shift and coupling efficiency is determined. At last the transfer characteristics is examined. Even though the SS around 120 mV/dec attained is not below 60 mV/dec, we believe our work could improve after overcoming the series channel problem and enrich the tunneling transistor family.

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## H. Figures and Legends

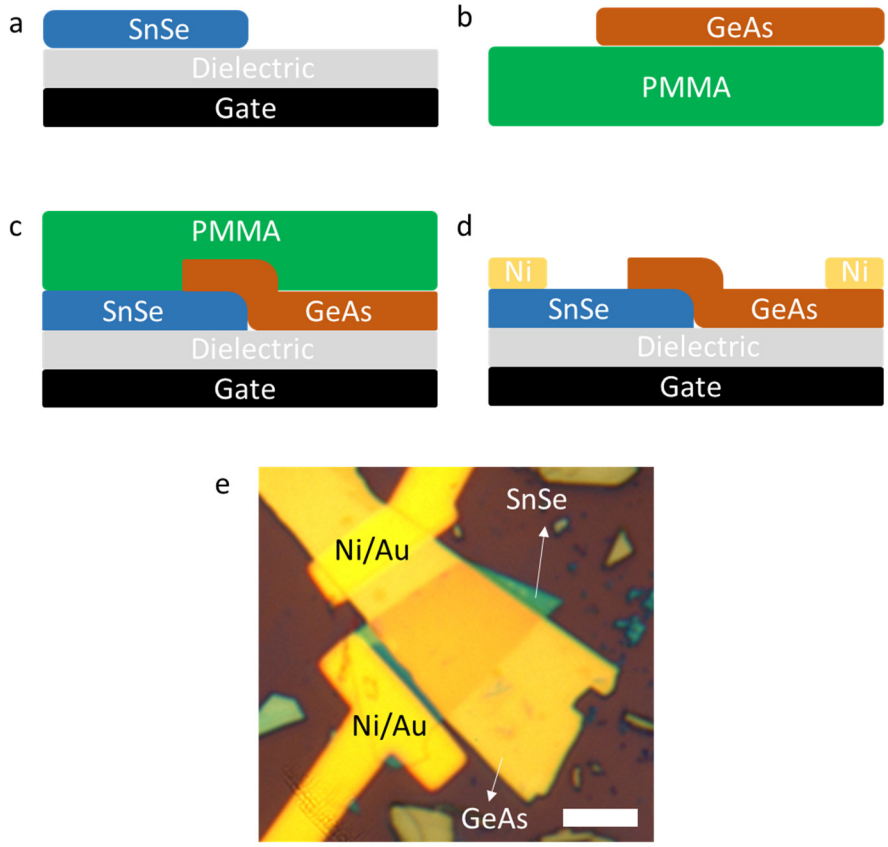


**Figure 4-1. Schematic illustration of fabrication for SnSe/GeAs heterostructure. a,** Exfoliation of SnSe thin flakes on dielectric material. **b**, Exfoliation of GeAs flakes on PMMA spin coated on silicon wafer. **c**, Transferring GeAs flake on SnSe flake using alignment transfer technique. **d**, Depositing Ni/Au 20/50 nm on SnSe and GeAs for source and drain electrodes. **e**, Optical image of completed heterostructure on 300 nm $SiO_2$. The scale bar is 5 μm.

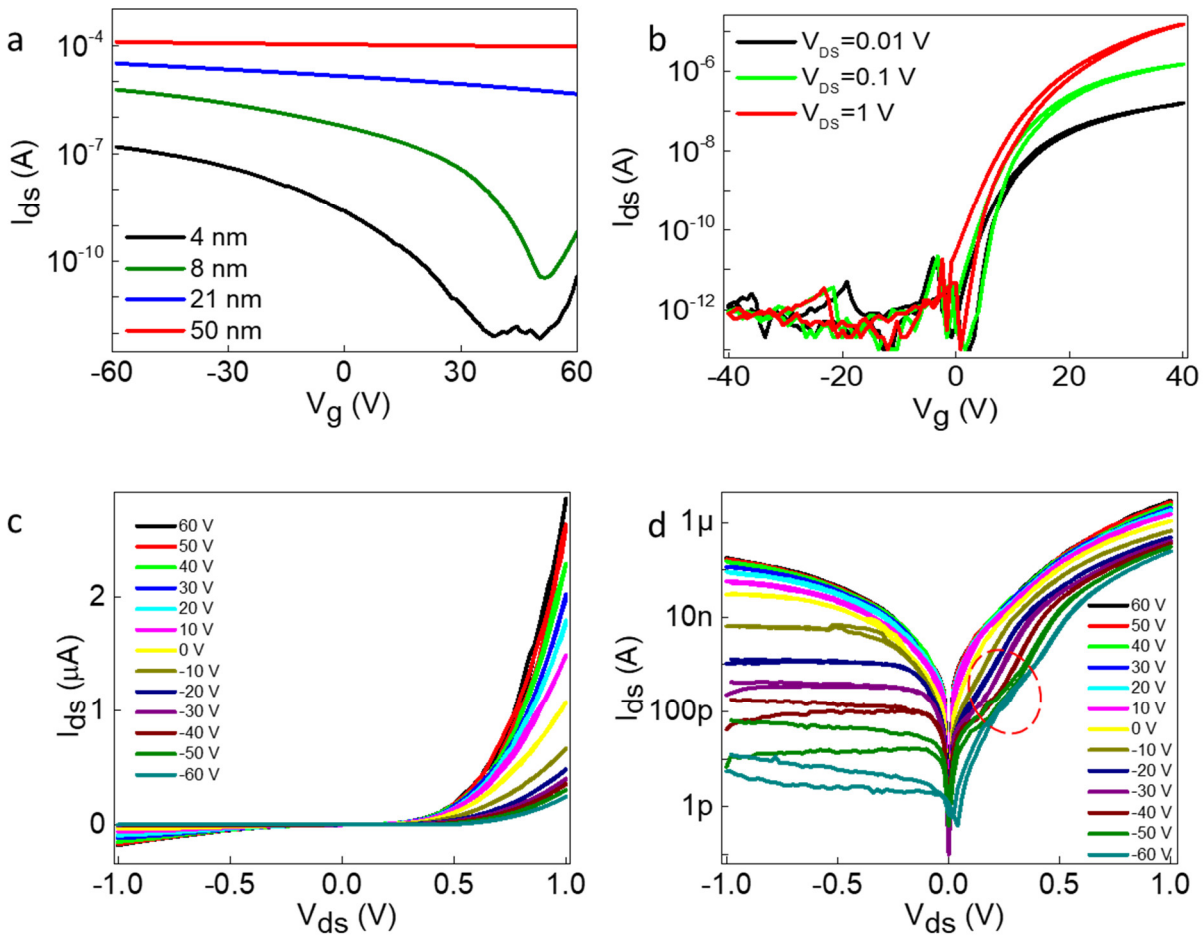


**Figure 4-2. Room temperature electrical properties of the GeAs, SnSe FET and their heterostructure**. **a,** Transfer characteristics of GeAs FET with various thickness. Thicker GeAs flakes show lower ON/OFF ratio. **b**, Transfer curve of SnSe FET at different source drain bias. **c**, Current-Voltage curve of SnSe/GeAs heterostructure at various gate voltage. Bias is applied on GeAs end. **d**, Current-Voltage curve of heterostructure in semi-log plot. The dashed circle marks towards NDR phenomena.

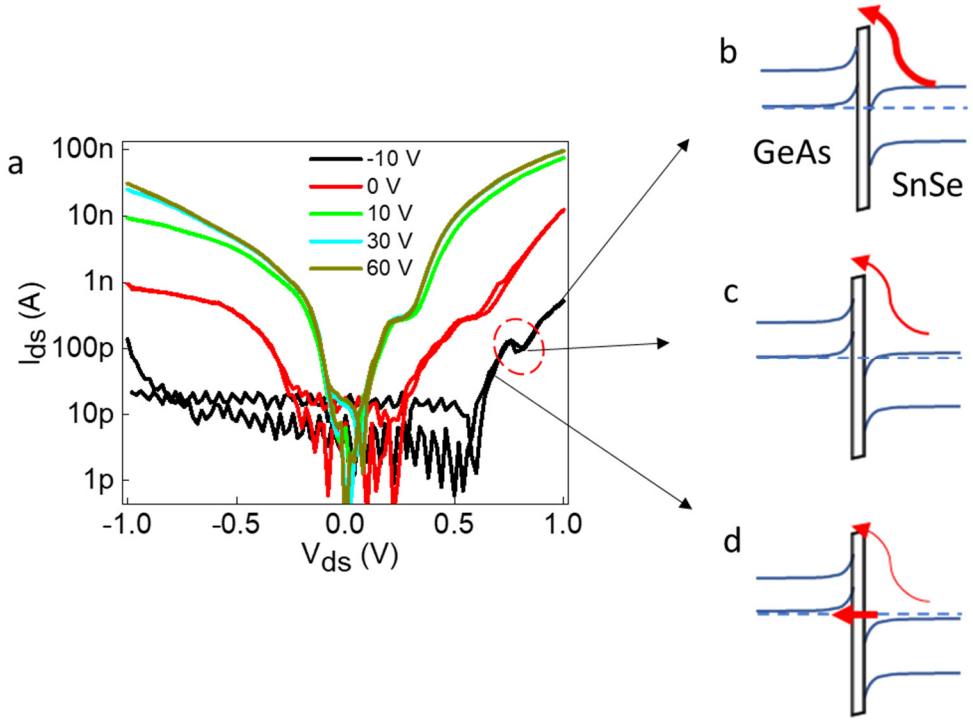


**Figure 4-3. Observing NDR of SnSe/GeAs heterostructure at low temperature and theory. a,** Source drain curve of SnSe/GeAs heterostructure at various gate voltage at temperature 30 K. The dashed circle notes the true NDR happens at Vg=-10 V. Bias is applied on GeAs terminal. **b**, Band structure of SnSe and GeAs at high positive bias. Thermionic emission dominate transport. **c**, Band structure of SnSe and GeAs at moderate positive bias. The tunneling window is closed and only low thermionic emission current stays. **d**, Band structure of SnSe and GeAs at low positive bias. Tunneling current dominant the transport because of significant tunneling window.

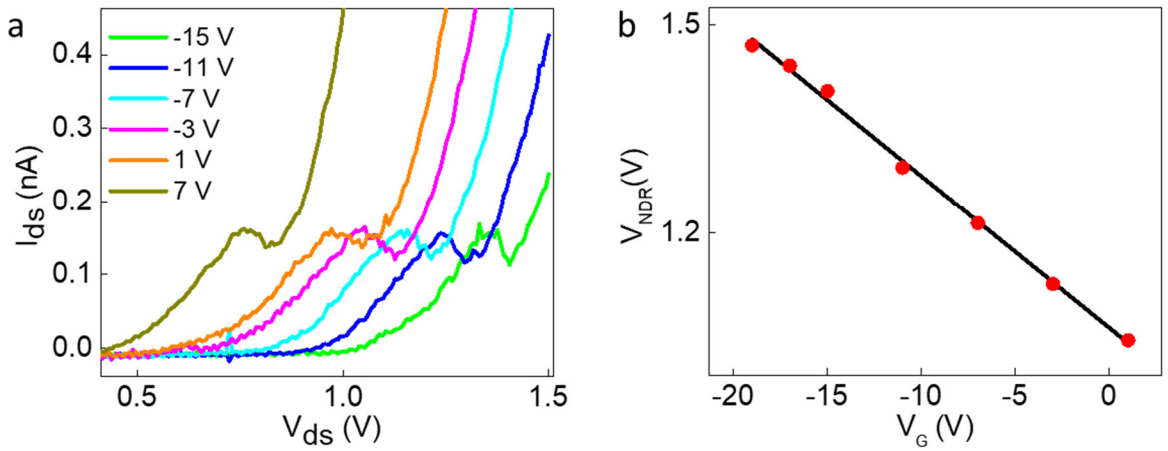


**Figure 4-4. Shifting of NDR at various gate voltage. a,** Source drain curve of SnSe/GeAs heterostructure at various gate voltage. The position of NDR shift with applied gate voltage. b, By plotting the NDR voltage as function of gate voltage, we could estimate the gate coupling efficiency.

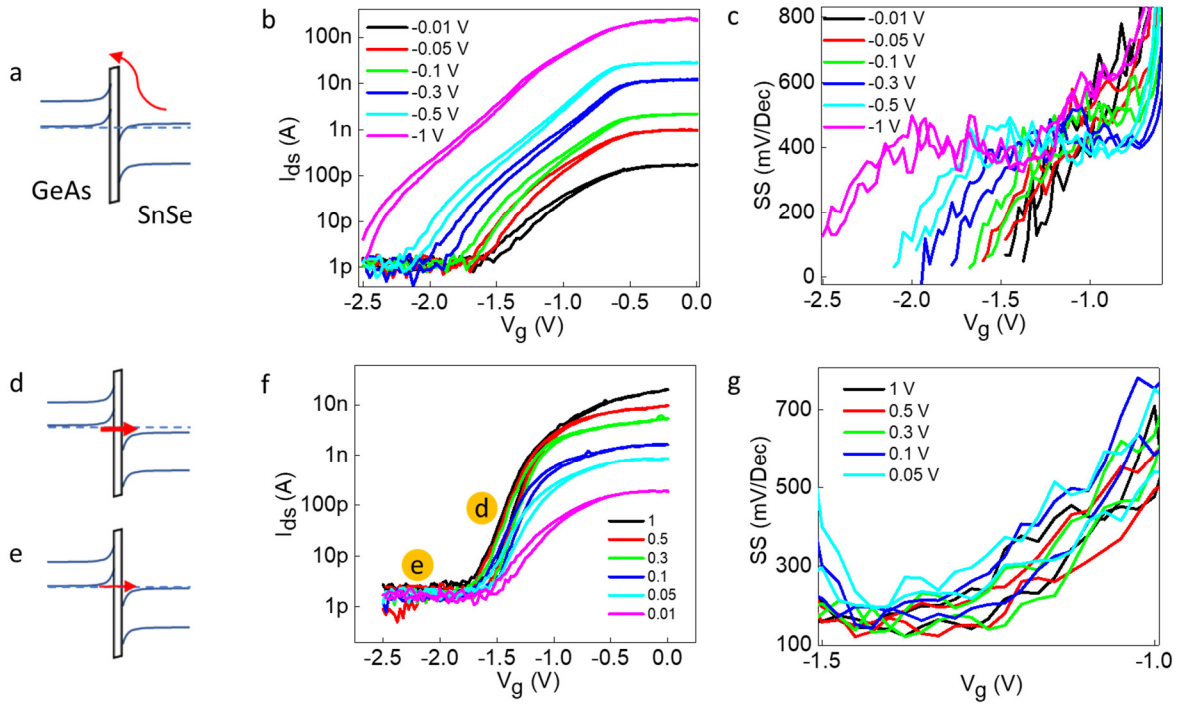


**Figure 4-5. Transfer characteristics of SnSe/GeAs heterostructure at room temperature. a,** Band alignment of SnSe and GeAs at forward bias. Thermionic emission dominates the transport. b, Transfer curve of heterostructure at various forward bias. Bias is applied on SnSe

side. c, Extracted SS from figure b. The data below 400 mV/dec is not reliable because of gate leakage current. d, Band structure of heterostructure at backwards bias and -1.5 V gate voltage. The tunneling window is widened due to more positive gate voltage. e, Band structure of heterostructure at backwards bias and -2.5 V gate voltage. The tunneling window is small due to more negative gate voltage. f, Transfer curve of heterostructure at various backward bias. Bias is applied on SnSe side. g, Extracted SS from figure f. The lowest SS is 121 mV/dec.

## Chapter IV: Memristor based on Ag/Oxide/SnSe for memory and neuro inspiring computing

### A. Introduction of memristor for digital storage and neuromorphic computation

Memristor, a conceptual fundamental passive circuit element bridging magnetic flux and charge was proposed by Leon Chua[1] in 1971 and rediscovered by HP labs in 2008[2], has evoked tremendous interest in memory[3, 4] and neuro inspiring computation[5, 6] community until today. This two-terminal device possesses a resistance dependent on history of current, which behaves like a memory + resistor and was hence given the name memristor. The linear relationship between resistance variation and charge flowing through the memristor results in a highly nonlinear and hysteretic current-voltage curve. Interestingly, this behavior has been experimentally observed in resistive switching devices far before memristor was defined and rediscovered[7, 8], thus questioning of interpreted memristor and mixed usage of the two concepts memristor and resistive switch in community is still going on[9]. Here, we would like to claim that resistive switching and memristive behavior are identical for practical purpose to avoid misunderstanding.

The highly hysteretic current-voltage characteristics of memristor enables fascinating memory-analogous functions that CMOS based logic circuit would hardly achieve. Two examples are resistive random-access memory (RRAM) and neuromorphic computation[10]. For RRAM, it requires two switchable states of resistance for nonvolatile storage. To utilize memristor for RRAM, a simple metal/insulator/metal (MIM) structure is normally adopted[11], forward and reverse current is then applied through the two terminal devices to switch its resistance between high resistance state (HRS) and low resistance state (LRS). The switching is happening mostly because of i) the valence changes due to anion migration or ii) creation and dissolution of conducting bridge due to cation migration[11]. For the later case, the insulating layer is commonly metal oxide,

such as $TiO_2$, $HfO_2$ and $ZrO_2$[12]. Capped with active metal e.g. Ag or Ti, the metal oxide possesses conductive bridge of metal element or oxygen vacancy after electro formation step to LRS. A following up opposite electric field could dissolve the bridge by driving the ion and inducing electrochemical reaction and hence switching it back to HRS. The variation of resistance of two states could be up to several orders making memristor ready for high performance memory. However, such devices normally require high formation voltage and working voltage due to moderate insulating thickness[13, 14]. Thinner insulating layer is challenging because of introduction of undesired defects by traditional metal deposition method. Thus, a gentler approach is desired for integration with fragile insulating materials. For the neuromorphic computing, the behavior of memristor is essentially analogous to synaptic modulation: the connection between pre-synaptic neuron and post-synaptic neuron is strengthened or weakened whenever we have communication between two neurons by stimulus forward or backward[15]; while the conductance between two electrodes of memristor, which mimics the connection of two neurons, is enhanced or weakened when we applied an electric field with either direction. Thus, a memristor is ready for simulation of synaptic modulation and matrix of memristor arrays enable complex neuromorphic computing. Besides synaptic modulation, a memristor could simulate neuron firing behavior with proper configuration[16, 17], which is highly desirable for all memristor architecture for neuromorphic computing.

Here, we propose a novel approach, which enables integration of active metal electrodes on fragile insulating layers for low working voltage memristor. By mechanically transferring silver electrodes on natural SnSe surface, we create a van de Waals interface which persists the delicate insulating oxide layer. The as fabricated two-terminal device does not require electro formation step and shows stable switching behavior with low working voltage. RRAM based on Ag/Oxide/SnSe/Ni memristor is realized and proves satisfied performance. Utilizing the

semiconducting nature of SnSe, we can tune the current level of memristor by control the conductance of SnSe through gate electric field. Moreover, we demonstrate synaptic modulation and neuron firing in single memristor device with optimized bias.

**B. Device fabrication and optical characterization**

The idea of transfer metal technique is to create a sharp and clean metal/insulator interface which could protect the fragile oxide layer as well as avoid unexpected diffusion of metal ion. To begin with, Ag/Au 20/50 nm metal electrodes are prepared on sacrifice $SiO_2$ substrate by electron beam evaporation (figure 5-1a). The deposited silver has weak adhesion with $SiO_2$ substrate and is easy for peeling off using polymer film. Before peeling it off, the hydrophilic $SiO_2$ substrate need to convert to hydrophobic surface to lower the adhesion between substrate and polymer. To do so, we treat the substrate in HMDS vapor at 120 ˚C for 5 to 10 min dependent on size of electrodes. After that, we spin coat PMMA A8 (2000 rpm) on substrate and peel the electrodes off on PMMA and then transfer to PDMS pad (figure 5-1b). At the meantime, thin SnSe flakes are mechanically exfoliated also on $SiO_2$ substrate using scotch tape. When SnSe is exposed to air, a thin layer of Tin oxide is formed on SnSe surface due to natural oxidation at room temperature[18]. An oxide layer based memristor normally requires one active electrode and one inert electrode, here, before transferring the active silver electrodes, we deposit Ni/Au 20/50 nm on SnSe flakes to serve as inert electrodes. To move on, we align the peeled off electrodes (on PMMA/PDMS) using optical microscope on the exfoliated Oxide/SnSe flake, by lowering and stamping the electrodes on SnSe (figure 5-1c), we can aligned transfer the electrodes on target Oxide/SnSe flakes (figure 5-1d). This gentle and aqueous solution free transfer technique brings formation of ultra-clean interface between active metal and delicate oxide layer, which enables resistive switching inside the fragile oxide layer.

The optical image of finished two terminal memristor is shown in figure 5-1e, with deposited Ni electrode on one side and transferred silver electrode on the other side, the charge transport of the whole device would include both lateral part in lateral SnSe and vertical part through SnSe/Oxide/Ag, which could dominate the transport when resistive switch happens. An SEM image also confirm the uniform thickness of SnSe flake (figure 5-1f). We also exam the Raman spectrum of SnSe flake (Figure 5-1g), the peak present $A_g^1$, $B_{3g}$, $A_g^2$ and $A_g^3$ polarization mode from left to right respectively, of which the $B_{3g}$ is normally highly dependent on alignment of excitation polarization and crystal axis.

**C. Resistive switching of Ag/Oxide/SnSe memristor**

The memristor we achieve includes two parts considering transport type, one is the lateral SnSe, which is a typical semiconductor and the other is SnSe/Oxide/Ag vertical structure, which is supposed to exhibit resistive switching characteristics. Thus, we are expecting a memristive switch connected with a transistor serially. To study pure memristive behavior, the lateral SnSe channel will be turned by applying a positive voltage on back gate since our SnSe is naturally n-type doped. All electrical transport studies are carried out in a dark environment. The fingerprint of a memristor is the current-voltage hysteresis. Thus, we sweep the DC voltage on Ni/Au electrode and ground silver electrode while keeping lateral SnSe transistor open, then we observe an obvious IV hysteresis (figure 5-2a). Originally, the device shows low current (below 10 nA) and exhibit HRS before switched to any state. When voltage sweeps from negative value to positive value the current is switched to high value at $V_{set}$=0.4 V and indicates LRS; when the voltage goes back to negative value, the current drops back to lower value at $V_{reset}$=-0.1 V and shows HRS. The switching varies resistance up to three orders, which opens a window for storing binary information. Note that the device is turned on (LRS) when the electric field goes from Ni electrode to Ag electrode. We could observe the same hysteresis in linear plot of IV (figure 5-2b), which

also indicates a linear IV characteristics at LRS. Interestingly, we are not seeing the same stable and observable memristive behavior in deposited Ni contact or deposited Ag contact. As shown in figure 5-2d, the IV of SnSe transistor with pure deposited Ni contact shows a linear relationship without any hysteresis, which behaves as a typical transistor at on state. While the pure deposited Ag contacted SnSe transistor shows minimum hysteresis, which is much less significant than what we observe in transferred Ag SnSe transistor. The only difference in terms of processing is the method of metallization: the deposited Ag electrode is done by electron beam evaporation which normally induces doping, diffusion and damage to semiconductor especially to fragile two-dimensional semiconductors. In this case, the native Tin oxide was damaged and eliminated after metal evaporation, which hence reveals intrinsic semiconducting behavior of SnSe. While the transferred Ag electrodes has a van de Waals contact with underneath Oxide/SnSe, which retains the oxide on SnSe surface, as a result, the device shows memristive characteristics due to ion migration inside the oxide layer. To examine the robustness of the memristor, we carried out DC measurement at various temperature. As shown in figure 5-2c, the IV curve at 300 K to 400 K still present memristive characteristics but with smaller working window, i.e. the $V_{set}$ decreases when temperature increases. Thus, our memristor can work even at high temperature, which enable digital storage at high work stress. Since the memristor includes a lateral SnSe transistor, gate voltage can be applied to tune the current level of the memristor. At $V_g$ = -60, 0 60 V, we could change the current level by two orders (figure 5-2f). The introduction of gate as third terminal in memristor could inspire novel applications for memory and computation.

**D. Ag/Oxide/SnSe memristor for nonvolatile memory**

With resistance ON\OFF ratio up to three orders, our memristor can be utilized for nonvolatile binary memory. To test the memory performance, we perform writing, reading, erasing and reading operation repeatedly by applying voltage $V_{write}$=1 V, $V_{read}$=0.2 V and $V_{erase}$=-1 V on nickel electrode while monitoring the current level. As plotted in figure 5-3a, the black curve indicates the operation voltage (see left y axis) and red curve represent current (see right axis) during read operation. Obviously, the current level is below 10 nA at HRS and above 10 μA at LRS. The repeated write and erase operation and stable ON\OFF ratio demonstrates excellent performance of RRAM for digital memory.

Another important parameter for RRAM is endurance which is defined by the number of working cycles that memory can repeat before failure. By sweeping write and erase voltage on memristor and measure the current, we can monitor the resistance at HRS and LRS when cycling the operation. As shown in figure 5-3b, high resistance ratio of HRS and LRS is sustained even after 400 cycles which is comparable with state-of-the-art flash memory. We also extract the cumulative probability of resistance of memristor at HRS and LRS (figure 5-3c), the lower resistance mainly focusses around 0.1 MΩ while the higher resistance distributes around 100 MΩ with longer tail. The last figure of merit the retention of the memory cell which is defined by the longest time a memory can maintain on one state. To measure the retention of our memristor, we firstly switch the device to one of the two state, then we measure the resistance by applying a small $V_{read}$=0.2 V after each period. As shown in figure 5-3d, our memristor could sustain at either HRS or LRS after $10^5$ s without any sign of failure, which is among the highest retention record.

**E. Ag/Oxide/SnSe memristor for synaptic modulation and neuron firing**

Neuromorphic computation, a concept inspired by biology, math and computer science to build artificial neuron system by very large-scale integrated circuit, is of great importance for future computing. But CMOS based integrated circuit is not an ideal simulator to realize the technique because of its binary nature. Memristor, as an analog device, whose resistance can be continuously tuned by applied stimulus (voltage), is a perfect building block for neuromorphic computation. For example, the connection between pre-synapsis and post-synapsis could be well modulated by their communication; while, in a similar way, the resistance between memristor terminals can also be adjusted by the applied voltage. Thus, to test synaptic modulation in memristor, pulse mode is implemented. As shown in figure 5-4a, after applying stimulus with voltage pulse $V_{pulse}$=0.25 V with 2 ms width, we observe increased current, which demonstrates the potentiation process of synaptic modulation. Meanwhile, we apply negative voltage pulse $V_{pulse}$=-0.15 V with 2 ms width, then observe decreasing current level, which demonstrate depression process of synaptic modulation. The successful demonstration of potentiation and depression process of synaptic modulation enables memristor for future neuromorphic computation.

Another important building block for neuromorphic computing is stimulus firing source which generates width controllable pulse mode signal. This neuron firing behavior is normally realized using complex circuit combining capacitances and transistors. Here, we demonstrate identical function but with a single memristor. As shown in figure 5-4c, by applying a constant voltage 0.5 V, which close to $V_{set}$, to our memristor, the current level starts oscillating with four orders of magnitude difference. Each high current level represents an output signal and this oscillation could simulate neuron firing behavior. Importantly, the width of fired stimulus can be further tuned by applied voltage. With slightly higher applied voltage (0.51 V), the width of

pulse can be broadened (figure 5-4d), which could provide more flexibility for neuromorphic computing design.

### F. Working principle of Ag/Oxide/SnSe memristor

We have demonstrated stable memristive behavior in Ag/$SnO_2$/SnSe heterostructure and its application for RRAM and neuromorphic computing. However, the working principle for its memristive behavior has not been discussed yet. In this work, the transfer electrode technique for memristor is proposed for the first time. Thus, to uncover the mechanism of memristive behavior we must locate the resistive switching location first. In our structure, we have two interface Ni/SnSe and Ag/SnSe and one semiconducting channel SnSe by looking at the device structure. The resistive switching could happen anywhere including the two interfaces and channel. To locate the resistive switching place, we fabricate multiple terminal device: four nickel electrodes and one transferred silver electrodes on one single SnSe flake. By examining the current between two specific electrodes at HRS and LRS, we can determine the switching location. For example, as shown in figure 5-5a and inset, we applied a voltage on the Ni and Ag electrodes to switch it to HRS or LRS, then we measure the current by applied a low voltage. The black and red curve shows different currents after switched to ON and OFF state, which is the memristive behavior indeed. After switching the above two electrodes to one of the states, we examine the current between middle two Ni electrodes. Interestingly, the current is high and identical (figure 5-5b). Since the current is referring the resistance of SnSe channel, thus, it proves that resistive switching is not happening in the SnSe channel resistance. Then we continue to examine the current between the first and third Ni electrodes (figure 5-5c). Again, we observe identical current at both states, which means that the resistive switching is not happening in the Ni/SnSe interface either. At this point, there exists one last place where

resistive switching may happen: the Ag/SnSe interface. We would like to note that inside the Ag/SnSe there will be an oxide layer, which will be proved later, but we would like to label it by Ag/SnSe for the moment. To prove our assumption, we continue to measure the current between the Ag and rightest Ni electrode. Without surprise, we observe high current level at On state and low current at Off state (figure 5-5d). Since the rightest Ni electrode and SnSe channel at right side of Ag electrodes was not involved in the switching, we can conclude that the resistive switching is happening at Ag/SnSe interface.

After locating the resistive switching location, we continue to determine the charge transport at two states. One practical method to examine the transport type is to study the temperature dependent resistance. If the resistance is highly sensitive to temperature, thermal emission is involved in the charge transport, otherwise most case is just band-like transport. Figure 5-5e shows the resistance of our memristor as function of temperature at HRS and LRS. Obviously, the two resistance is just slightly dependent on temperature. By extracting the potential barrier (figure 5-5f), we found that the barrier height of 1.66 meV and 1.82 meV for LRS and HRS is even lower than thermal energy which is 25 meV, which means potential barrier is too low to induce significant thermal emission in memristor for both states. Thus, we can claim that the charge transport does not involve barrier induced thermal emission.

If Ag/SnSe interface is pure metal/semiconductor junction, the high resistance state should result from a Schottky barrier due. However, we have proved that there is not barrier in our memristor. Thus, we suspect that another material may exist at the interface. A previous study has been reported that natural tin oxide layer may form when SnSe is exposed to the air. The reported $SnO_x$ has 10 nm thickness and could induce resistive switching. But different from our memristor, their device switches at much higher voltage with much lower ON\OFF ratio, so we believe that except a natural oxide layer, the transferred Ag electrode plays important role in

our memristor. People also utilize tin oxide for RRAM[19]. After depositing Al electrodes on tin oxide, they manage to form an insulating $AlO_x$ layer. By applying opposite voltage, $AlO_x$ insulating layer can be dissolved and regenerated and induce resistive switching behavior.

Inspired by the reported works, we propose a similar assumption which will be confirmed by TEM data. As shown in figure 5-6b, e and f, we study the TEM image of cross section of three Ag/SnSe interface in three electronic state: pristine state, On state and Off state. Note that those three interfaces are from three transferred silver electrodes on the same SnSe flake, which is set to three states. So, they minimize unwanted variables between samples just keep electronic state difference. By combining the TEM image and EDX data (figure 5-6b and 4-6c), we could easily tell three different materials from top to bottom: Ag, SnSe and SnSe. But interestingly, the center SnSe has higher brightness and lower SnSe EDX signal, we would like to assume that this layer has been partially oxidized and contains $SnO_2$ by referring the reported natural tin oxide at the SnSe surface. Another important observation is a bright layer between Ag and $SnO_2$, We would like to assume this is $AgO_x$, because this assumption is going to explain all the TEM data and electrical behavior. The last important information here is a thin $Ag^+$ layer between $SnO_2$ and SnSe as inferred from the little peak in blue curve in EDX data (figure 5-6c). Thus, we infer that Ag is already partially oxidized and diffuse into the SnSe (figure 5-6a). But when the device is switched to On state, we observe that Ag is punching through the $AgO_x$ layer and reach $SnO_2$ layer. Since the $SnO_2$ contains high density of oxygen vacancies, it is intrinsically conductive. At the meantime, the thin $Ag^+$ layer disappear (figure 5-6f). Thus, we could infer that when the device is switched to On state, the $Ag^+$ is driven back to Ag metal and create a conducting channel through the insulating $AgO_x$ layer (figure 5-6d). When we switched back to Off state, we observe recreation of insulating layer as shown both in TEM image (figure 5-6h) and EDX curves (figure 5-6i), which block the carrier transport and

result in high resistance state.

By combining the TEM and EDX data, our inference and electrical switching behavior, we can explain the atomic level dynamics that determine the resistance in two states. As shown in figure 6-7a, the figures illustrate that a native tin oxide layer is formed when the SnSe is freshly exfoliated and exposed in air. After transferring the silver electrode, silver is oxidized and form an insulating oxide layer and diffuse into the SnSe. When we applied an electrical field from SnSe to the silver electrode (figure 5-7b), the $Ag^+$ is driven back to Ag electrode and reduced and forms conducting bridge, which turn the device to LRS. When we apply an electric field from Ag electrode to SnSe (figure 5-7c), Ag is oxidized again and diffuse back to SnSe as $Ag^+$ and form an insulating $AgO_x$ layer and turn the device to Off state. To conclude, the formation and dissolution of $AgO_x$ layer result in the HRS and LRS of device and enable memristive behavior.

## G. Summary

In summary, we have demonstrated for the first time a memristive device achieved by transferring silver electrode on two-dimensional SnSe semiconductor. The memristor exhibit stable resistive switching behavior and excellent memory performance for RRAM. Importantly, the RRAM can work at high temperature and the current of which is tunable by gate bias. Neuromorphic computing has been demonstrated using our memristor by simulating the synaptic modulation and neuron firing. To uncover the working principle of the memristive switching we locate the switching position and examining the TEM image and EDX data. A theory is proposed: the formation and dissolution of $AgO_x$ is the key reason that the charge transport can be switched between HRS and LRS respectively.

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## H. Figures and Legends

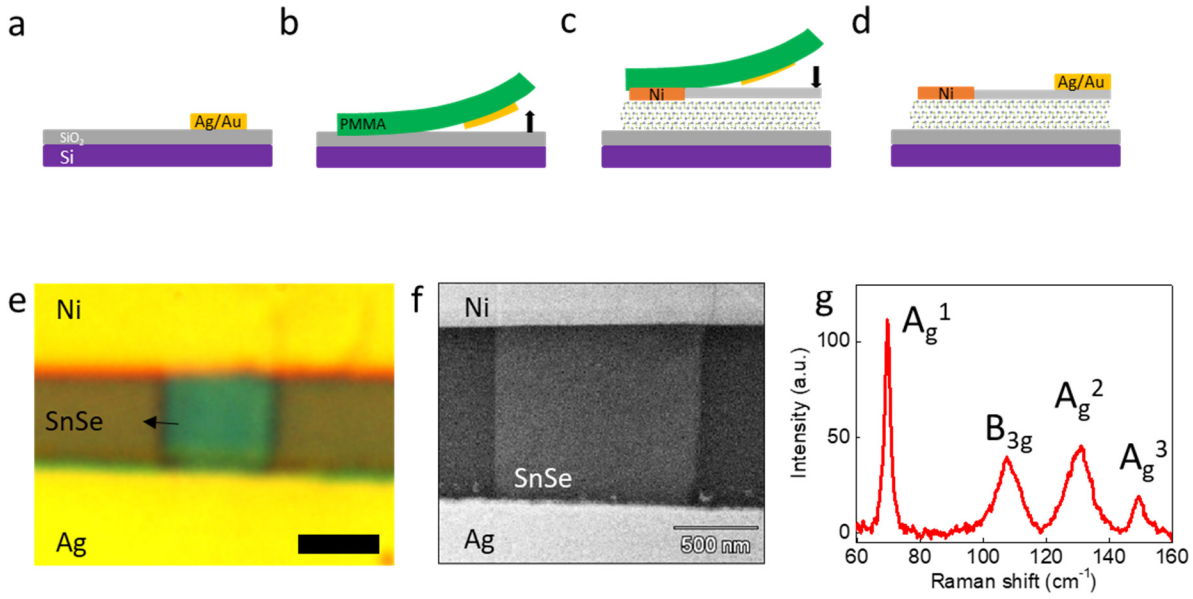


**Figure 5-1. Device fabrication and characterizations. a-d,** Transferring silver electrode on SnSe for memristor. a, Depositing Ag/Au electrodes on $SiO_2$ substrate. b, Peeling off the Ag/Au electrode using spin coated PMMA. c, Transferring Ag/Au electrodes on exfoliated SnSe flake. d, Finished device structure. **e,** Optical image of finished two terminal memristor. The scale bar is 1 μm. **f**, SEM image of completed device. **g**, Raman spectrum of SnSe flake with 633 nm excitation.

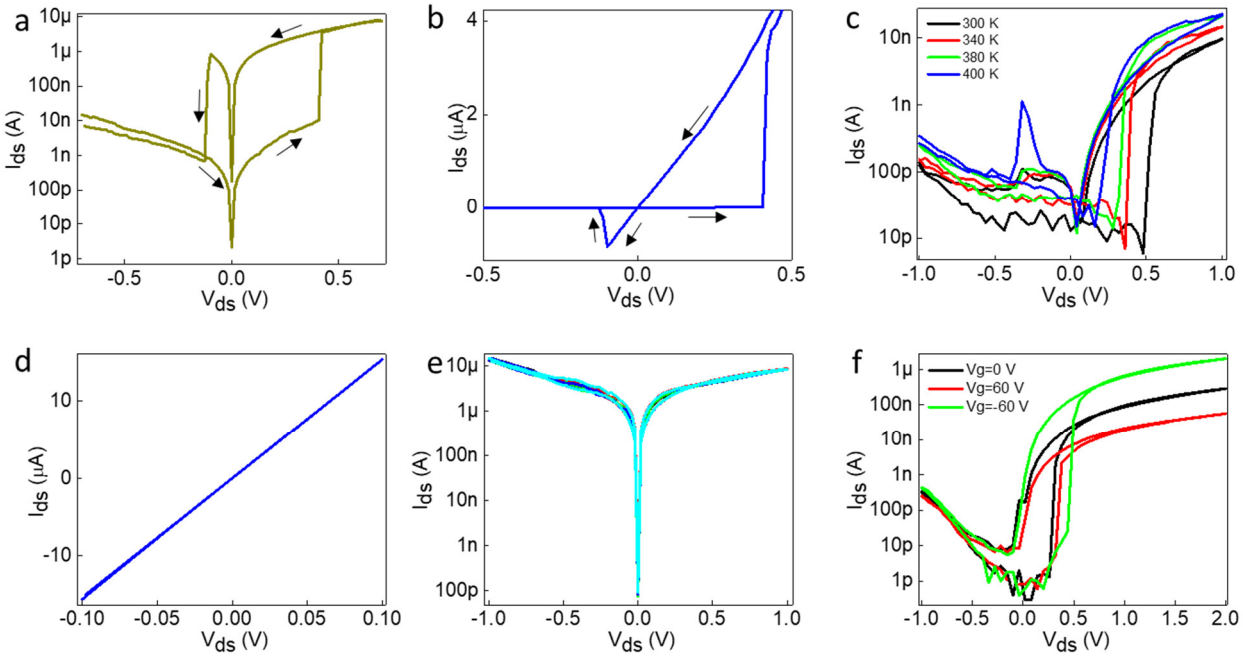


**Figure 5-2. Resistive switching performance of memristor. a**, Hysteretic IV of transferred silver contacted memristor. The arrows label the sweeping direction. **b**, Linear plot of IV characteristics of memristor. **c**, IV characteristics of memristor at various temperature from 300 K to 400 K. **d**, IV curve of two Ni contacted SnSe flake. **e**, IV curve of two deposited Ag contacted SnSe flake. **f**, IV curve of memristor at various gate bias.

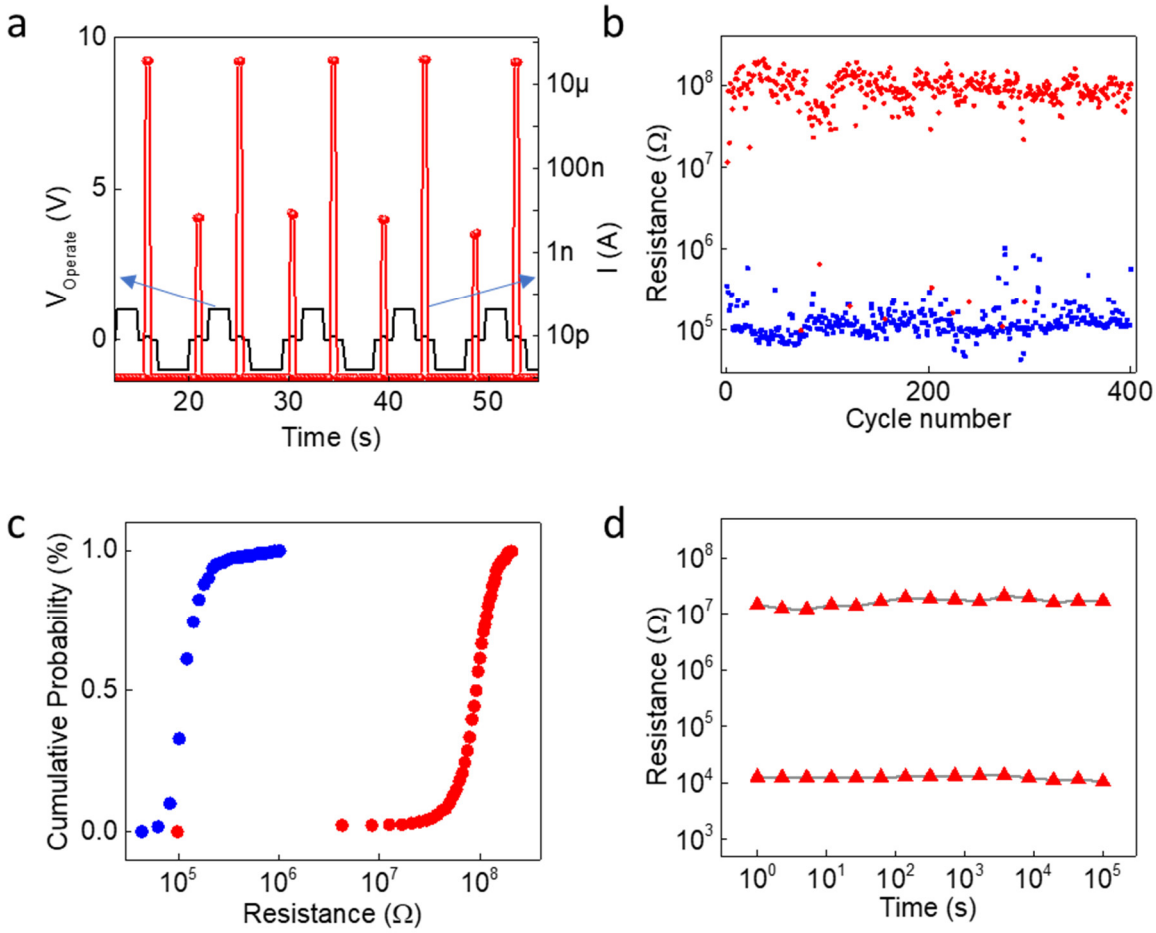


**Figure 5-3. Electrical performance of memristor for RRAM. a**, Repeated write, erase and read operation of memristor for RRAM. **b**, Endurance test of memristor for RRAM. The maximum cycle number reach 400. **c**, Cumulative probability of memristor resistance at two states. **d**, Retention test of memristor for RRAM. The maximum lifetime reaches $10^5$ s.

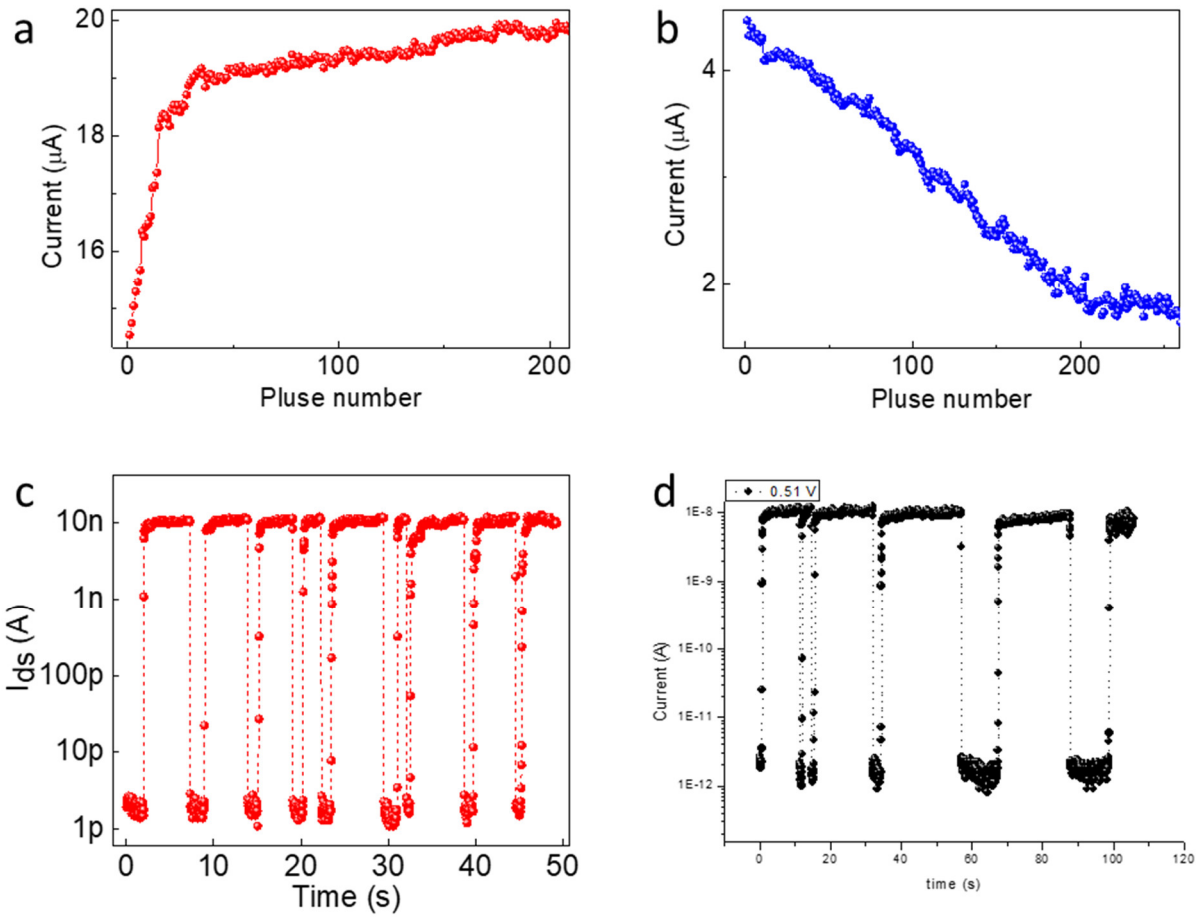


**Figure 5-4. Artificial synapse for neuro inspired computing. a**, Potentiation test of memristor for synaptic modulation. **b**, Depression test of memristor for synaptic modulation. **c**, Neuron firing simulation by applying constant voltage V=0.5 V. **d**, Width controllable neuron firing simulation by applying higher voltage V=0.51 V.

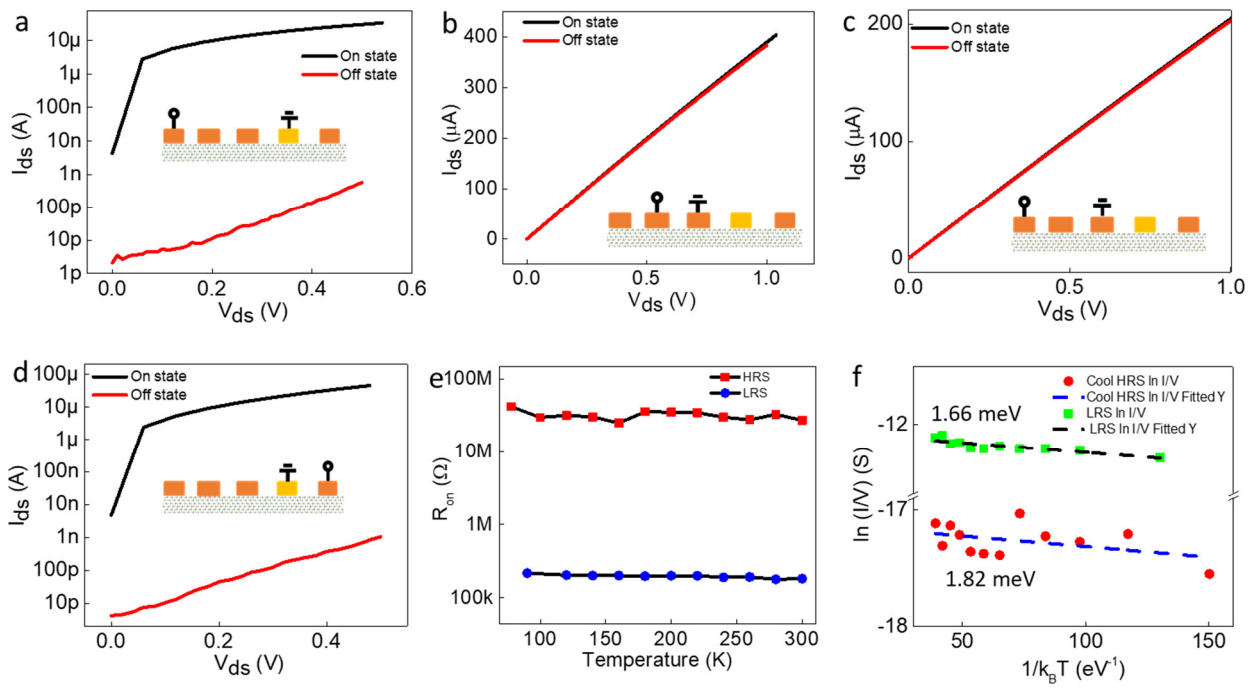


**Figure 5-5. Locating switching position by studying multiterminal device. a**, Current and voltage curve of left Ni and Ag electrodes after they switch to either states. **b**, IV curve of two centered Ni electrodes when electrodes in figure a is switched to either state. **c**, IV curve of first and third Ni electrodes when electrodes in figure a is switched to either state. **d**, IV curve of rightest Ni and Ag electrodes when electrodes in figure a is switched to either state. **e**, Resistance of HRS and LRS at various temperature. **f**, Arrhenius plot of current at two states to extract barrier height if there is any.

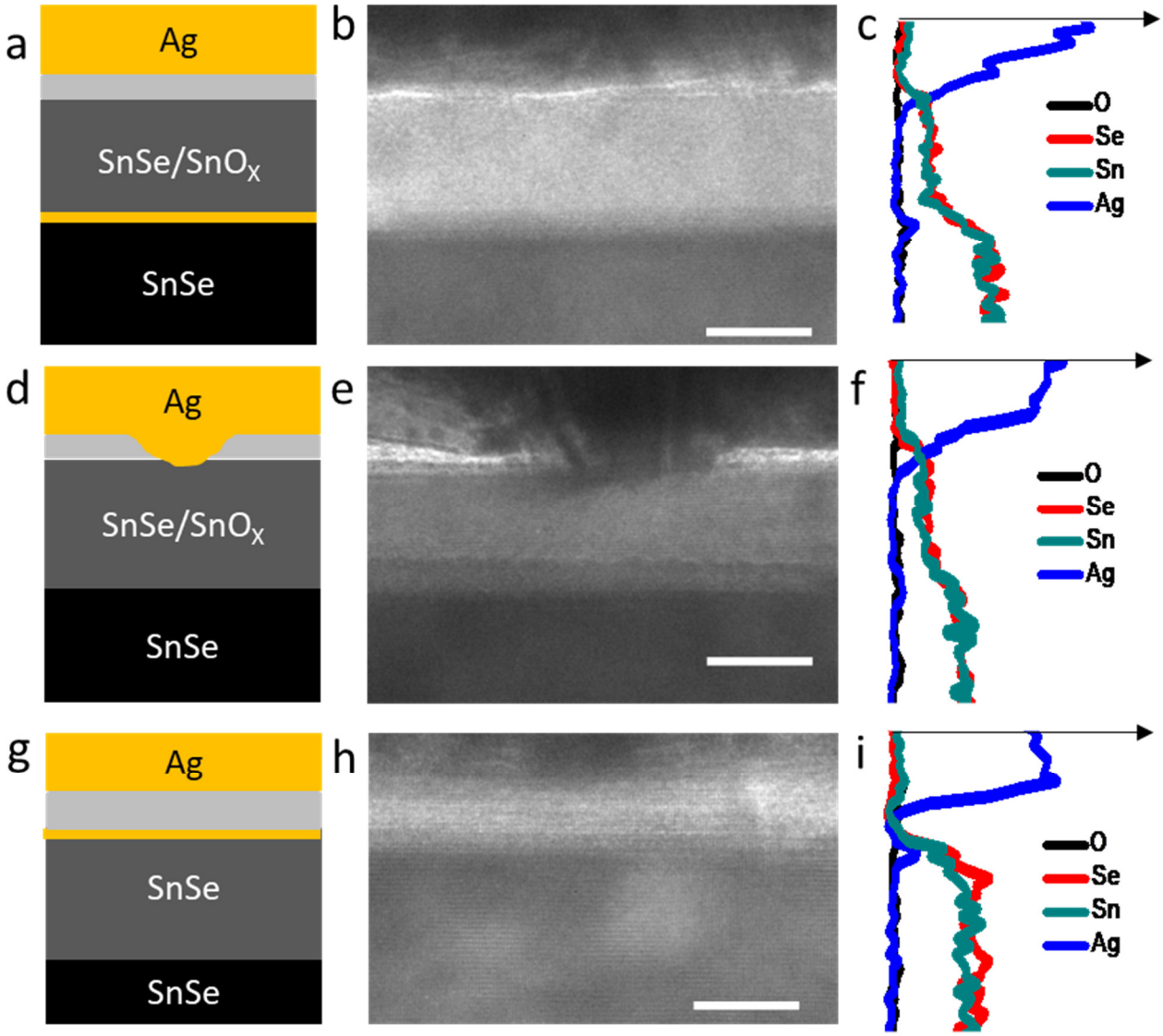


**Figure 5-6. Identifying materials at transferred silver contacted SnSe surface. a, d and g,** Illustration of materials at silver and SnSe surface. **b, e and h**, TEM image of cross section of interface. Scale bar is 20 nm. **c, f and i**, EDX line profile of four elements: O, Se, Sn and Ag in figure b, e and h.

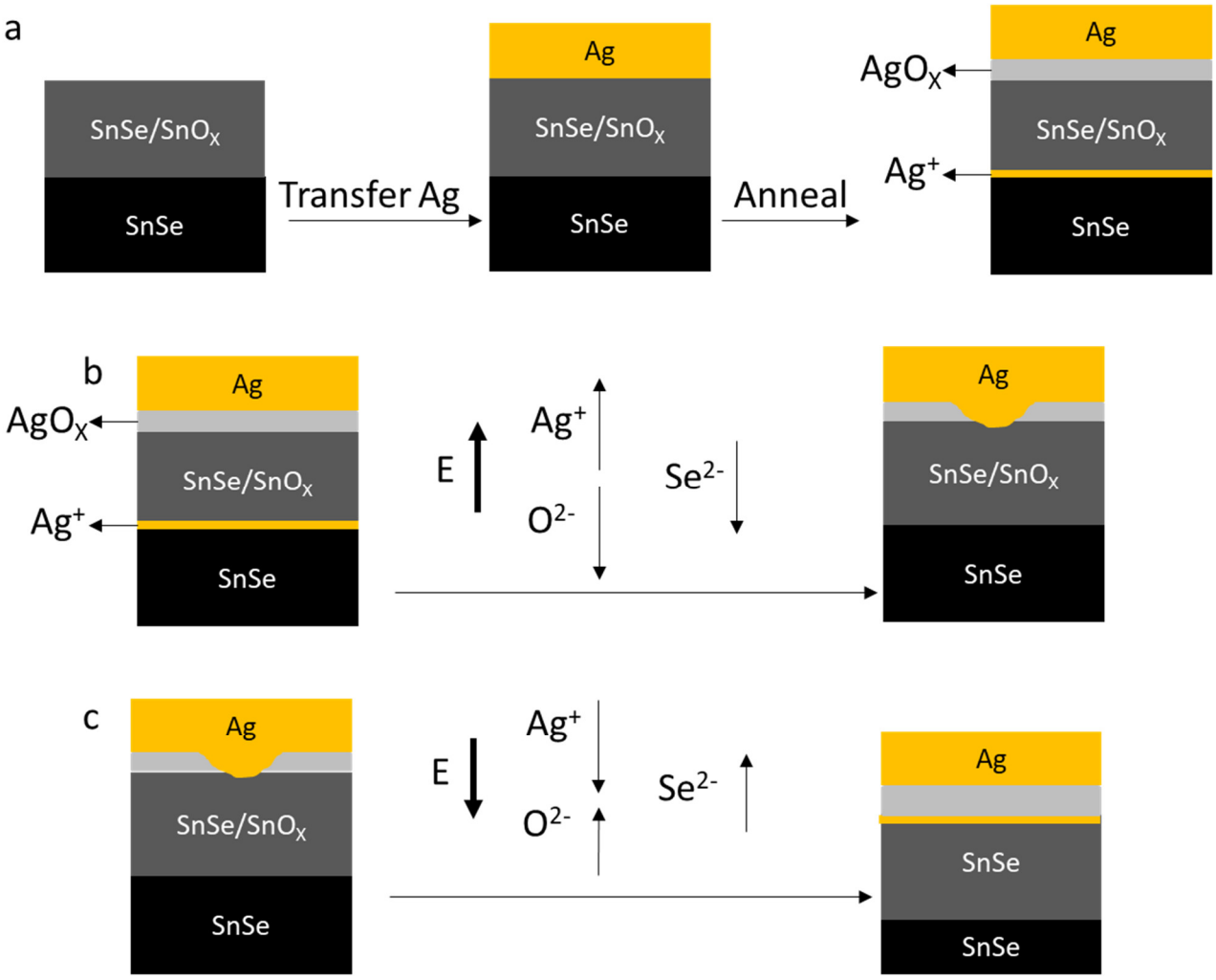


**Figure 5-7. Atomic dynamics for resistive switching mechanism. a,** Formation of native oxide layer on exfoliated SnSe flake and diffusion of Ag ion after transferring Ag electrodes. b, Migration of ions at electrical from SnSe to Ag and induced formation of conducting Ag bridge. c, Migration of ions at electrical from Ag to SnSe and induced formation of conducting $AgO_x$ insulating layer.