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Digital Calibration of Wide Bandwidth Open-Loop Phase Modulator

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Digital Calibration of Wide Bandwidth Open-Loop Phase Modulator

A dissertation submitted in partial satisfaction of the

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in Electrical Engineering

by

Nitin Nidhi

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ABSTRACT OF THE DISSERTATION

Digital Calibration of Wide Bandwidth Open-Loop Phase Modulator

by

Nitin Nidhi

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2015

Professor Sudhakar Pamarti, Chair

The rapid rise in demand for high data rates has led to communication standards like LTE that use signals with wide signal bandwidth and high peak-to-average power ratio. Since, total power consumption is largely determined by the efficiency of the power amplifier used, high efficiency architectures like polar and out-phasing, are preferable for future transmitter designs. Such architectures require a phase modulator (PM) as one of their key building blocks. The recent developments in phase modulator design have demonstrated superior wide-bandwidth performance of open loop modulation techniques. However, currently the resolution is limited by systematic errors inherent in the phase modulator circuit and random errors due to inevitable component mismatches.

In this dissertation, a phase-interpolator based open-loop phase modulator is proposed, which leverages a digital calibration technique to mitigate the sources of phase errors and achieves excellent phase resolution. At the heart of this technique, a time-to-digital converter performs high resolution measurement of phase errors of the phase modulator. These measurements are used to continuously pre-distort the modulation data, so that the linearity of the overall transfer function is enhanced, thereby resulting in low out-of-band emission and low in-band noise. A prototype IC was implemented in 0.13 μm CMOS process. Measurements on the prototype show that out-of-band quantization noise is 56-dB lower than the signal when transmitting 20-Mb/s GFSK signal and the r.m.s. error is only 3.2%. The power consumption of the phase modulator is 18 mW. Since the IC was implemented in 0.13 μm CMOS process, the power is expected to reduce a lot, if it is implemented in finer process nodes. The dissertation also presents theory and measurement results on frequency synthesis using the open-loop phase modulator. New frequency can be synthesized with very fine frequency step size, by applying a digital phase ramp to the phase modulator. However, the non-linearity of the phase modulator results in strong spurious tones. Digital compensation is proposed to mitigate these spurs, and generate multiple low-jitter clocks.

The dissertation of Nitin Nidhi is approved.

Babak Daneshrad

Milos D. Ercegovac

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Sudhakar Pamarti, Committee Chair

University of California, Los Angeles

2015

Dedicated to my parents and wife

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Chapter 1

Introduction

1.1 MOTIVATION

The widespread growth in the communications industry is primarily characterized by rapid increase in data rates and improvements in power efficiency. Fig. 1.1 depicts the evolution of data rates from 40 kbps in the GPRS system to the current maximum rate of 100 Mbps in LTE systems. However, this positive trend demands circuits which process signals which are wider in bandwidth, have a high signal-to-noise ratio and a high peak-to-average power ratio. In addition to the growth in data rates, the power efficiency of the modern radio chip, which is immensely versatile in integrating several transceivers on a single die, must also improve. Unfortunately, the design of RF transmitters meeting these specifications in the traditional manner of I—Q up conversion can significantly increase the total power consumption of the RF frontend and therefore, current research is actively looking into high efficiency architectures like polar [16-20] and out-phasing [21,22] for future designs.

In the polar architecture (Fig. 1.2 (a)), the in-phase and quadrature components are transformed into amplitude and phase components; the out-phasing architecture (Fig. 1.2 (b)) transforms the signal into two phase components. By making these transformations, high efficiency switching power-amplifiers can now be used in the transmitter design, which have a theoretical maximum efficiency of 100%. Furthermore, recent works have demonstrated techniques to maintain this efficiency over large power back-off conditions as well [50]. However, in order to realize these wide-bandwidth and

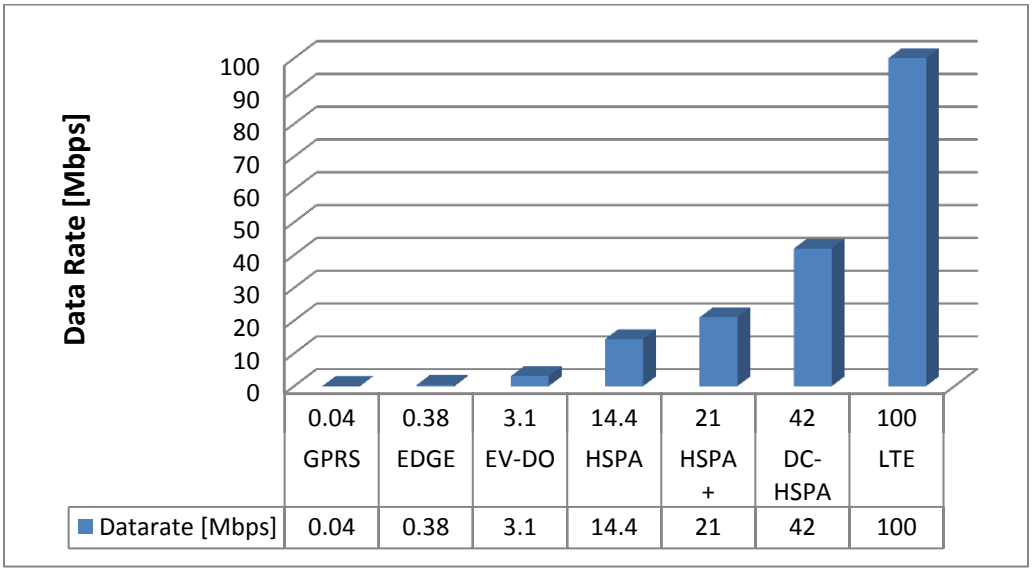

Fig. 1.1: Evolution of data rates in wireless communication standards

power-efficient transmitter circuitry, a corresponding wide-bandwidth and power efficient phase modulator is required, for both, the polar and the out-phasing topology. Besides this, the bandwidth of the phase modulated signal increases by 6-8 times the bandwidth of the RF signal, further accentuating the wide bandwidth requirement in phase modulator design. In addition to being wideband, the phase modulator must meet the stringent in-band noise and the out-of-band emission requirements.

Traditionally, for narrow bandwidth signals, PLL based architectures like $\Sigma - \Delta$ modulation of feedback divider [26], digital pre-emphasis [23], quantization noise cancellation [24], and two-point modulation have been used in the past [25,29]. More recently, for wider bandwidth signals, digital open loop modulation has reported the best performance [1—5]. A detailed overview of all the prior-art on phase modulators and their advantages and shortcomings is presented in Chapter 2. It will be shown that that phase errors due to inevitable random mismatches in the device components and

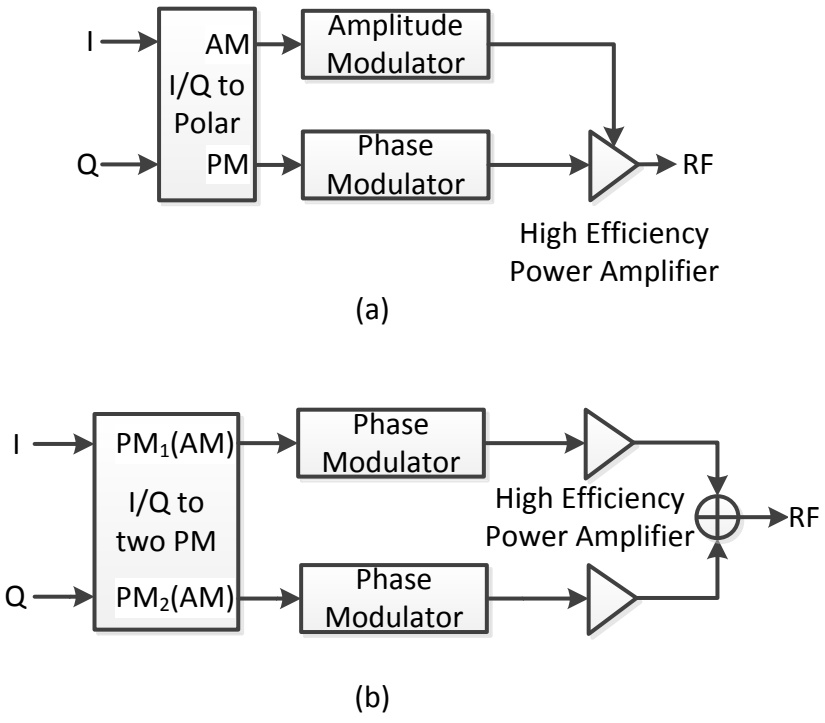

Fig. 1.2: (a) a polar transmitter, and (b) an outphasing transmitter.

systematic errors due to circuit topology, poses a challenging problem for achieving very high resolution phase modulation.

Closely related to phase modulation for digital communication is the challenge of designing low jitter, multiple output clock generation units. Such multiple output clock management unit is required in modern SOCs, which integrate several sub-systems like CPU cores, graphics, power management, high-speed I/O interface, ADC/DACs, modem, etc. The phase modulator which meets the high performance modulation requirements of RF phase modulation applications, is also suitable for low jitter clock synthesis. Furthermore, digital open-loop frequency generation techniques can generate multiple-outputs and have a fast response enabling dynamic frequency scaling.

In an attempt to solve the problem of low power, wide-bandwidth and high resolution phase modulation, a digital calibration technique is developed in this dissertation, to tackle performance degradation due to modulator topology and random component mismatches. To demonstrate its usefulness, the designed open loop phase modulator was tested for: (a) phase modulation in a GFSK and an out-phasing transmitter; and (b) low jitter, multiple output clock generation.

1.1 ORGANIZATION

Chapter 2 of this dissertation is a comprehensive review of all the architectures for achieving wide bandwidth phase modulation.

Chapter 3 of this dissertation is an extensive analysis of the design of an open loop phase modulator. Several key design challenges are identified in this chapter. A noise cancellation scheme for phase quantization noise of phase modulators was introduced in [2]. In this chapter, techniques for optimization of this scheme is discussed, which are supported with extensive simulation results. Additionally, a digital modulator is proposed to reduce the quantization noise in the receive band of the transmitter.

Chapter 4 of this dissertation introduces the proposed digital calibration technique for the estimation and correction of phase errors in a phase modulator. The signal processing details and the performance bounds of the technique are subsequently discussed.

Chapter 5 of this dissertation describes the IC implementation details of the prototype fabricated as a proof-of-concept of the proposed technique. Several circuit techniques for improvements in the wide-bandwidth capability of the circuit are

explained. Afterwards, the measurement results of the prototype IC are discussed and a comparison with the current state-of-the-art is presented in this chapter.

Finally, Chapter 6 concludes this dissertation with a summary of all the improvements achieved in this work.

Chapter 2

Wideband Digital Phase Modulation – Prior Art

In one of the simplest implementation of phase or frequency modulation, the modulation data is applied to the control voltage of a Voltage Controlled Oscillator (VCO) (Fig. 2.1). Although, this technique is open-loop and wideband, it suffers from frequency drift, VCO transfer function non-linearity and variations over PVT, high close-in phase noise and loss of transmission during periods of frequency lock. In order to find a solution for these problems, broadly two categories of phase modulators have emerged –

1. Closed loop phase modulators, and
2. Open loop phase modulators

2.1 Closed Loop Phase Modulators

If continuous feedback control is applied to a VCO, to arrive at a conventional PLL, close-in phase noise is improved and carrier frequency is tightly controlled. The phase modulation can, now, be injected from several ports of the PLL loop. In the popular offset-PLL (Fig. 2.2) [39, 40], the phase modulated data was obtained by an I-Q modulator running at a lower frequency and applied to the reference input port of the PLL. This topology can achieve excellent noise performance however modulation bandwidth is severely limited by the loop bandwidth of the PLL.

In other cases, digital modulation data has been successfully applied using a Multi-Modulus feedback Divider (MMD) in a fractional-N PLL (Fig. 2.3) [26, 41] to achieve phase modulation with low phase noise and very good control over the output

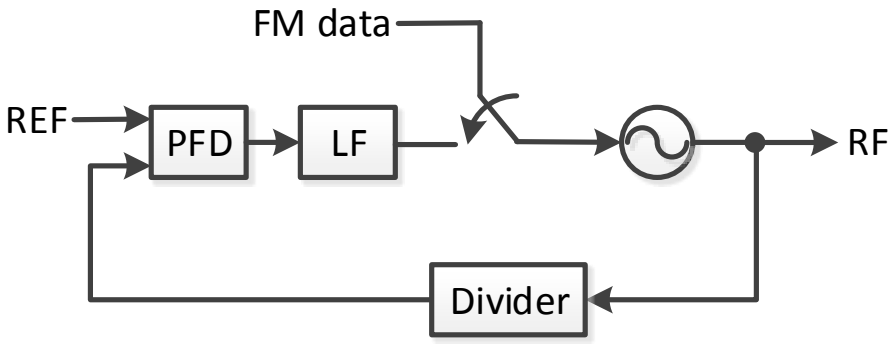

Figure 2.1: Direct VCO modulation requires periodic frequency re-locking.

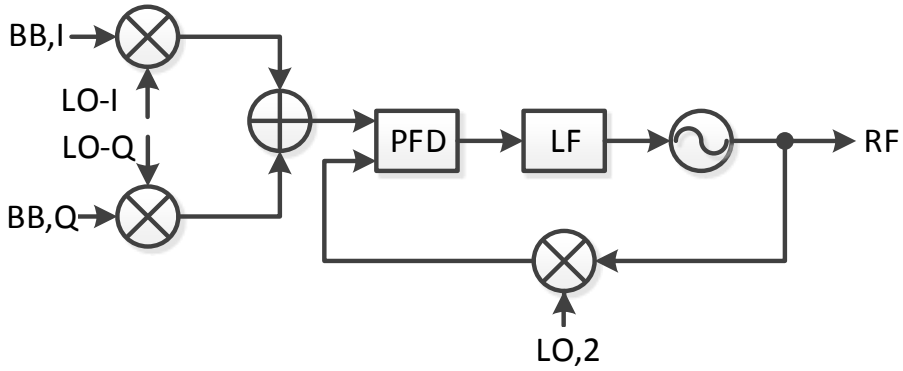

Figure 2.2: Offset PLL

carrier frequency. In this technique, however, the high frequency content of the modulation data is again filtered out by the loop filter of the PLL making it unsuitable for wide-bandwidth phase modulation. Additionally, the digital $\Delta - \Sigma$ modulator output, which controls the MMD, has high quantization noise and fractional spurs. Both of these sources of noise must be suppressed by the loop filter and therefore, the system bandwidth is further reduced.

Several bandwidth extension techniques have been proposed for closed loop phase modulators. The digital pre-emphasis as shown in Fig. 2.4 provided some extension beyond the PLL's loop bandwidth, but, it requires precise knowledge of PLL loop dynamics. In the quantization noise cancellation technique [24, 30—32, 42], the $\Sigma - \Delta$ quantization noise is estimated and cancelled by adding a second port at the input of the loop filter (Fig. 2.5). In [34], quantization noise reduction was achieved by

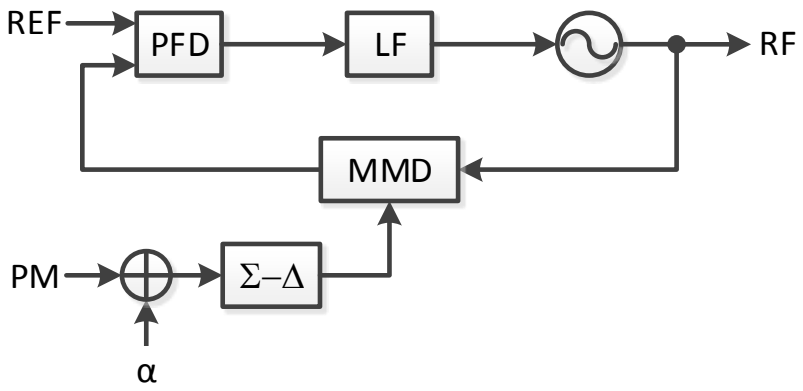

Figure 2.3: Frequency Modulation by Multi-Modulus Divider (MMD) of a Fractional-N PLL

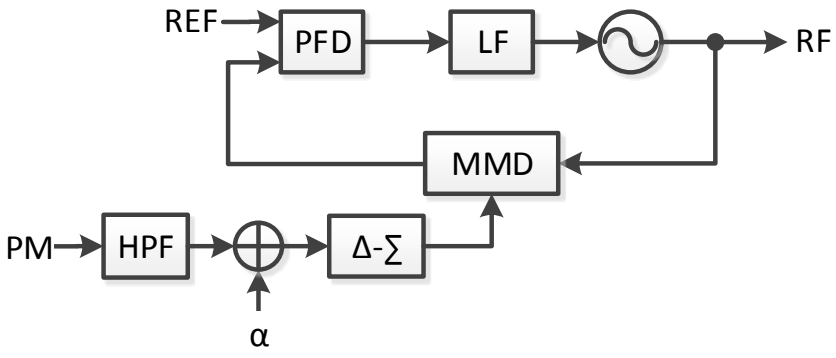

Figure 2.4: Fractional-N PLL with digital pre-emphasis

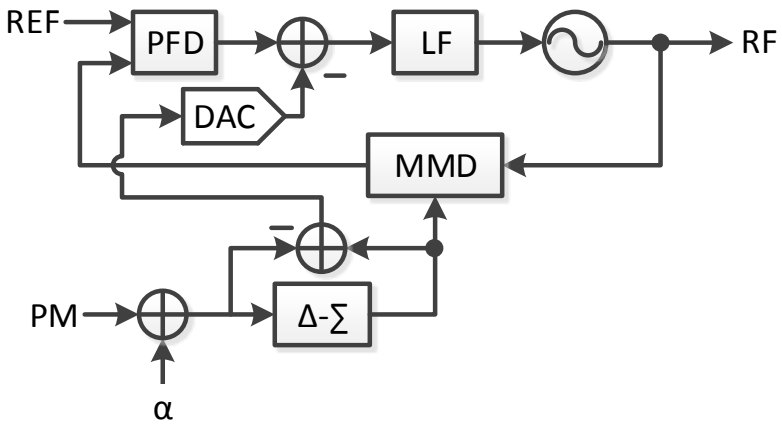

Figure 2.5: Fractional-N PLL with quantization-noise cancellation

employing a multi-phase generator for fractional frequency division in the feedback path. LMS based quantization noise cancellation [32], and type-I fractional-N PLL with sharp loop filter to suppress quantization noise [35] are other proposed techniques to extend the bandwidth of phase modulated signals. But, even the best in state-of-the-art designs have not exceeded 3 MHz. Additionally, these techniques can create low-frequency fractional spurs at PLL output which can lower output SNR or violate transmit spectrum mask.

In order to obtain further increase in bandwidth, the so-called two-point modulation has been often used [25, 29, 43—46]. Since the injection of modulation data at any node of the PLL loop is either high pass filtered or low pass filtered, it is injected at two nodes simultaneously such that the sum of the two transfer functions becomes wideband (Fig. 2.6). The most commonly used injection nodes are the MMD and the VCO control voltage to achieve wide bandwidth FM. A common problem encountered in this approach is the loss in SNR due to gain and phase mismatch between the two paths.

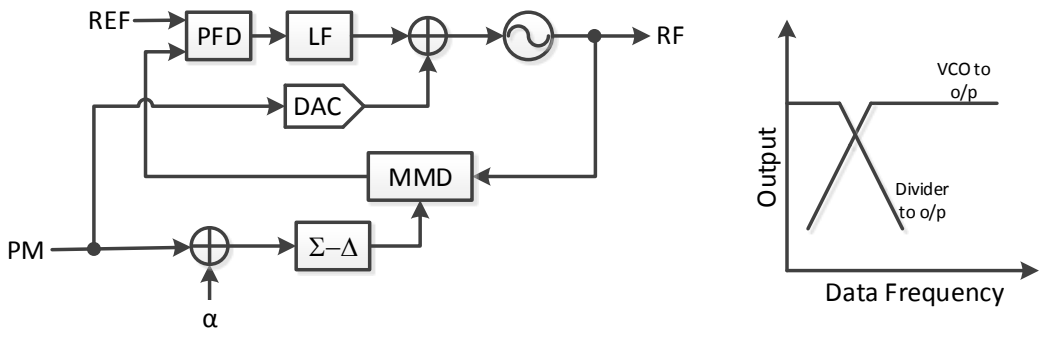

Figure 2.6: Two-point modulation

Before injecting the data signal at the VCO control voltage input, it must be attenuated by VCO gain, K_{VCO} and hence K_{VCO} must be known a priori in this technique. Since, K_{VCO} can vary over PVT, an on-chip K_{VCO} estimation method becomes important. Nonetheless, this technique has been successfully used to generate transmit signals meeting GSM/EDGE and WCDMA requirements.

In [36], gain matching was obtained by applying a square wave input to the two modulation input nodes, and the voltage across the resistor, which implements the zero of the loop filter, was monitored. The calibration loop then minimizes the error voltage developed across the resistor. The approach to measure Digitally Controlled Oscillator (DCO) gain and PLL loop gain, in [47], was to measure the phase error in response to a DCO control change. The PLL loop, reduced to type I operation by holding the digital integral path, compensates for the frequency error by adjusting the phase error at phase detector input. The calibration loop then senses the phase error using a bang-bang PFD and modulates the fractional part of the feedback divider until the phase error is reduced to a very small value. Using the new frequency divider value so obtained, the DCO gain

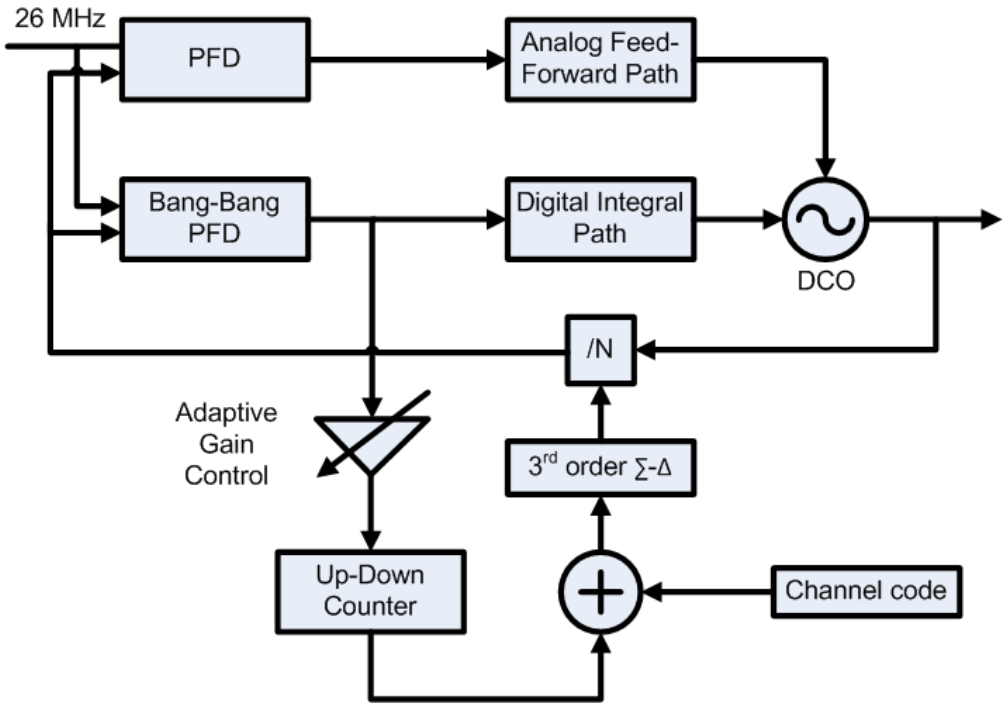

Figure 2.7: Block diagram of DCO gain calibration as used in [47]

can be calculated. For measuring loop gain, a current pulse was injected at the charge pump output and the resultant frequency change was measured using the same method.

The design presented in [43] introduced VCO transfer function linearization technique for two-point modulation for WCDMA. It utilizes a local negative feedback loop around the VCO to obtain a fairly constant K_{VCO}. This local loop employs an analog technique to measure the VCO frequency, which forms the feedback signal.

The development of an all-digital PLL (ADPLL) [6, 25, 37-38], has opened up new possibilities for accomplishing phase modulation, as the signals within the PLL loop have become more predictable. Besides this, injection of digital data can be readily achieved in the digital domain, at most of the internal nodes of the PLL. The design

presented in [25] took advantage of this feature of a digital PLL and injected the frequency modulation data to the control word of DCO and the carrier frequency control word of the PLL (Fig. 2.8). The second input was described as a compensating signal for the first one, but it can also be viewed as the low frequency path of a two-point modulation.

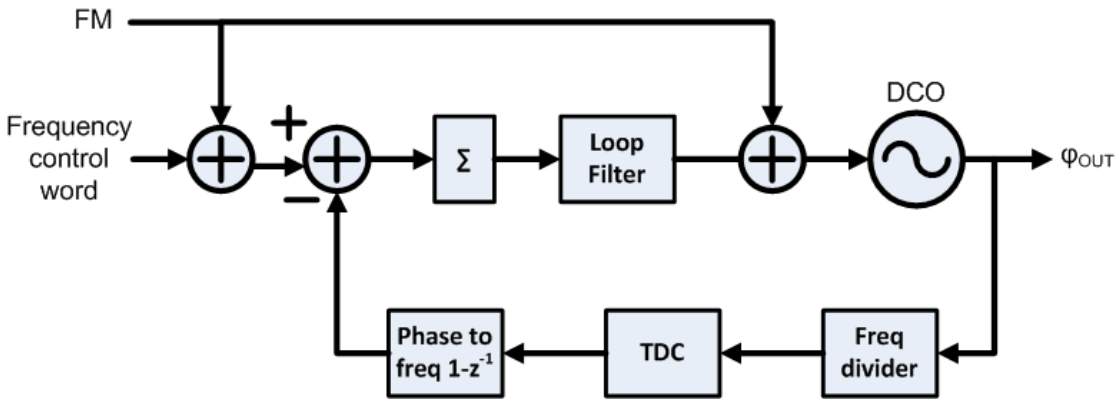

Figure 2.8: Two-point FM in an all-digital PLL [25]

In [22], a hybrid of many of the techniques mentioned earlier was designed for GSM and WCDMA. The outphasing angle was generated using an 8-bit phase interpolator, while phase modulation was generated by two-point modulation. However, it also used phase-to-digital converters in a negative feedback loop to correct for the non-linearity of phase interpolators, thereby reducing the available bandwidth. Phase modulation techniques at 60 GHz are also being researched. [52] implemented a novel method to obtain phase modulation at 60 GHz by digitally controlling the effective dielectric constant of a differential transmission line. This was achieved by digitally switching in and out a 4-bit bank of floating M6 and M7 strips placed underneath the

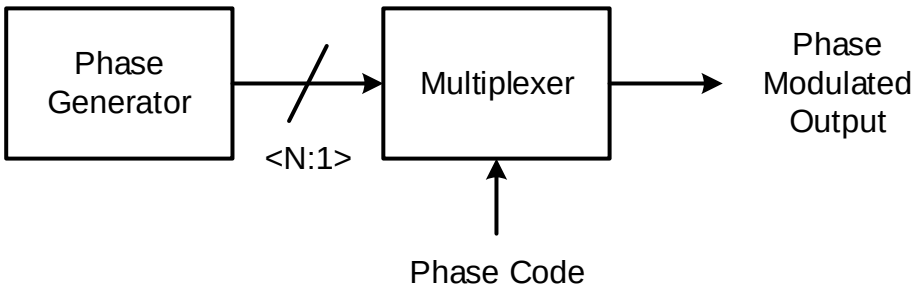

Figure 2.9: Conceptual open-loop phase modulator

transmission line, which leads to a digitally variable phase of S21. However, its dynamic performance under data transmission was not presented.

Although gain and phase calibration techniques have helped to increase the robustness and bandwidth of phase modulators, to the best of the author's knowledge, their application have not been demonstrated on even wider modulation standards such as WLAN, WiMAX and LTE.

2.2 OPEN LOOP PHASE MODULATORS

The bandwidth limitation and gain and phase mismatch issue associated with two-point modulation techniques can be avoided by using open-loop modulation techniques, where modulation is performed outside the frequency synthesizer loop. Essentially, it isolates the carrier frequency generation block from the data modulation block, yielding a modulator which does not involve a low-pass filter (the loop filter) in its path. Hence, these modulators can achieve very wide bandwidth.

In a typical open-loop phase modulator, a phase generator block produces multiple phases at the carrier frequency. It is followed by a phase multiplexer whose

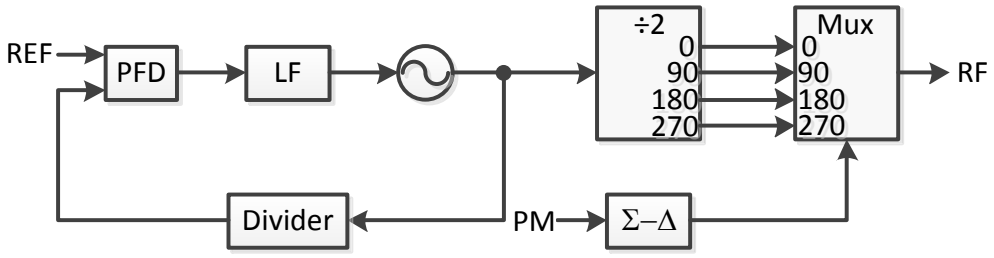

Figure 2.10: Frequency divider based open loop phase modulator [1]

output is controlled by the phase modulation data (Fig. 2.9). The operation is similar to a digital-to-analog converter, but the analog quantity of interest is the phase of the carrier signal. Due to a digital implementation of the modulator, this technique easily lends itself for quantization noise shaping, digital pre-distortion to compensate for errors due to PVT variation, dynamic element matching and other similar digital techniques.

In these modulators, the bank of reference phases are commonly generated by: frequency division [1], delay-locked loops (DLL), digitally controlled delay-line (DCDL) [3,4], and on demand, using phase interpolation [2,5].

Frequency division [1] results in very few phases at GHz carriers, resulting in high quantization noise (Fig. 2.10). With $\Sigma - \Delta$ quantization noise shaping, the in-band noise was lowered at the expense of large out-of-band noise (-25 dBr observed from the measured spectrum). The number of discrete phases can be increased by using a large division modulus, but output frequency is reduced by doing so. A segmented topology with CMOS inverter based delay locked loop (DLL), followed by digitally controlled delay lines (DCDL) was used in [3] to realize 9-bit phase modulators (Fig. 2.12). The DCDL suffered from phase errors and the required calibration was performed using

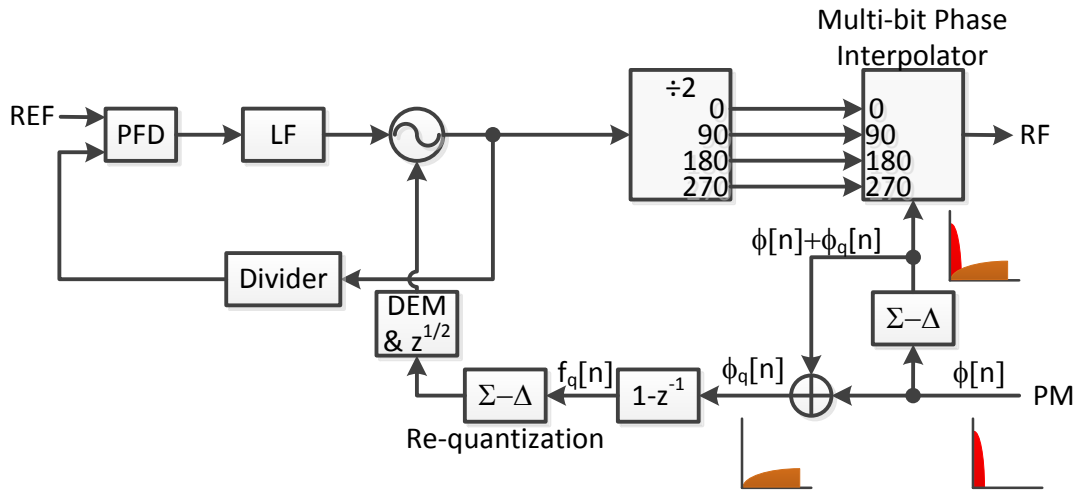

Figure 2.11: Phase quantization noise cancellation [2]

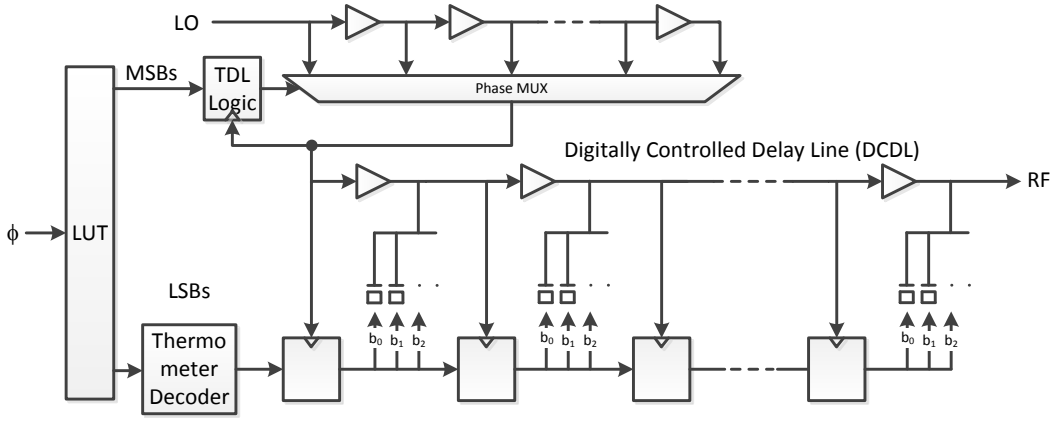

Figure 2.12: Open loop phase modulator with segmented topology using a combination of DLL and DCDL [3]

external equipment. However, the reported power consumption in inverter based phase modulators has remained high, even in an advanced process node. Furthermore, the inverter based phase modulators can be sensitive to supply noise.

Phase interpolation offers a low power alternative that eschews the phase multiplexer and generates the desired phase on demand [2,5]. It generates a weighted sum of two reference phases of the carrier. It is fully differential, consumes low power and offers wide bandwidth. The quantization noise of a 6-bit phase interpolator was increased by a quantization noise cancellation technique in [2], where, the quantization noise, which is known *apriori*, is digitally computed and subtracted from the output by adjusting the VCO phase. Even if quantization noise cancellation is not used, excellent phase resolution can be achieved with phase interpolators, if not for systematic and random errors.

Phase interpolators have a non-linear transfer function from the phase control code to output phase. In [2], the non-linearity was reduced by using two stages of interpolation and applying systematic pre-distortion. However, the accuracy of this type of systematic correction worsens in the presence of higher order harmonics of the RF carrier, when the functional form of interpolated phase is not known precisely. In [5], the linearity and the effective resolution were improved by band-pass filtering the phase interpolator inputs. The band-pass filters employ inductors that make it unattractive to applications that need multiple open loop modulators. Furthermore, this approach requires a tunable filter to accommodate changes in carrier frequency and/or redesign of the filter for a change in process node.

Irrespective of the kind of phase modulator circuit employed (phase interpolator or delay line based), digital calibration is generally essential to achieve high resolution, particularly in the face of random circuit mismatches. For digitally controlled delay lines,

[4] had devised a calibration method based on measuring the frequency of a ring-oscillator formed with the delay line PM. However, this method is not suitable for phase interpolator based modulators.

In this work, a phase interpolator based open loop phase modulator with a TDC based digital calibration is presented. Systematic non-linearity and random errors caused by mismatches are both estimated and corrected using a look-up table using the proposed calibration technique.

2.2.1 Multiple Output Clock Generation

The phase modulator which meets the high performance modulation requirements of RF phase modulation applications, is also suitable for low jitter clock synthesis. Although, several of the phase modulation techniques described earlier can synthesize clocks with low-jitter, they are not capable of generating multiple clock outputs. In particular, all the closed loop PLL techniques and their offshoots for bandwidth extension, including two-point modulation, can only generate a single phase modulated, or clock output. For example, a second clock output from a fractional-N PLL requires a "second" PLL, doubling the total area and power consumption. Besides this, if the design requires an LC oscillator then the magnetic coupling of the two LC tanks further aggravates the design challenges. On the other hand, digital open-loop frequency generation techniques can generate multiple-outputs by only requiring a second digital phase modulator, resulting in power and area savings of several shared circuit blocks, like VCO, PLL, and frequency divider. In addition to this, owing to their open-loop operation,

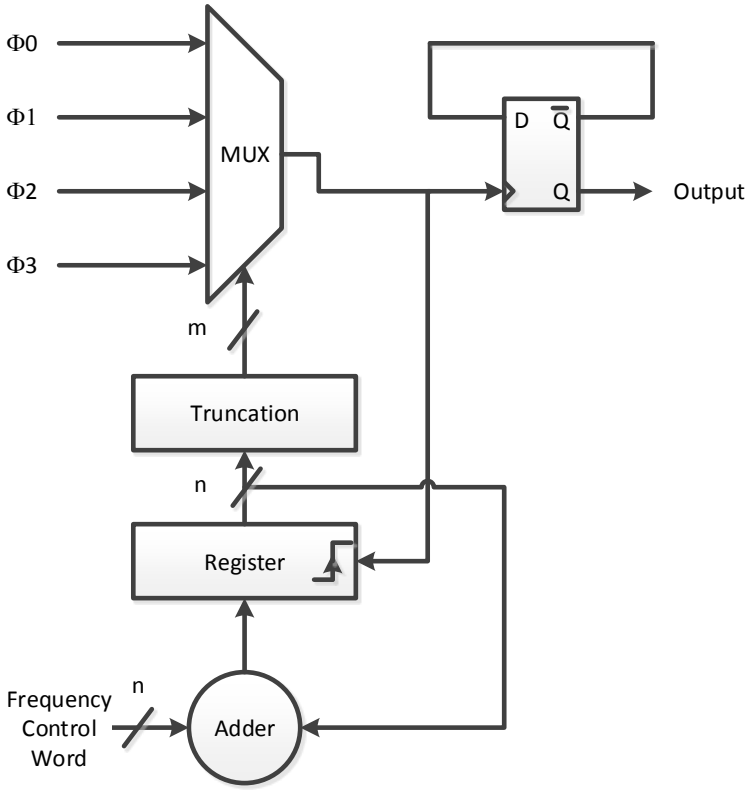

Figure 2.13: Flying adder architecture for clock generation [48]

they have a fast settling response to changes in output frequency, thereby, enabling dynamic frequency scaling, for power reduction in a digital processor.

Traditionally, direct-digital synthesizer (DDS) is popular for low frequency clock synthesis; however, they require high resolution DACs for phase-to-amplitude conversion, and high roll-off analog filters, which becomes challenging at RF frequencies. Flying-adder architecture [48] for direct-digital clock synthesis (Fig. 2.13), simplifies the analog design by selecting the desired output phase of a phase generator, but they suffer from strong spurious tones in their output.

Recently, several other techniques utilizing advances in PLL techniques and open loop modulation were proposed for application in multiple output clock generators. However, their jitter performance is unacceptable for performance critical applications like high speed I/O, data converters and RF transceiver.

In [10], multiple fractional-N PLLs sharing a common crystal clock input was proposed for multiple clock requirements. Multiple LC-oscillators in each PLL becomes exorbitantly area intensive, therefore, ring oscillators are the only feasible alternative in this approach (Fig. 2.14). However, the clock jitter of such a topology using ring VCOs, and the area requirement for multiple PLLs tends to be high. The VCO noise can be filtered by the PLL loop of a wide-bandwidth PLL, but this comes at the cost of increased TDC quantization noise and increased $\Sigma - \Delta$ quantization noise of a digital fractional-N PLL.

The phase noise of the digital ring oscillator based PLL was improved by injection locking. In the integer-N mode of injection locking, the output is an integer multiple of the reference clock and the clean edge of the reference is injected to the ring oscillator at an integer multiple. This injection locking technique was extended to fractional ratios in [9], to improve the resolution of achievable frequency steps in a digital PLL. Although, the technique addresses the issues due to high noise of the digital ring oscillator and improves the frequency resolution, the frequency resolution is still limited by the number of stages in the ring oscillator. Increasing the number of phases in the ring

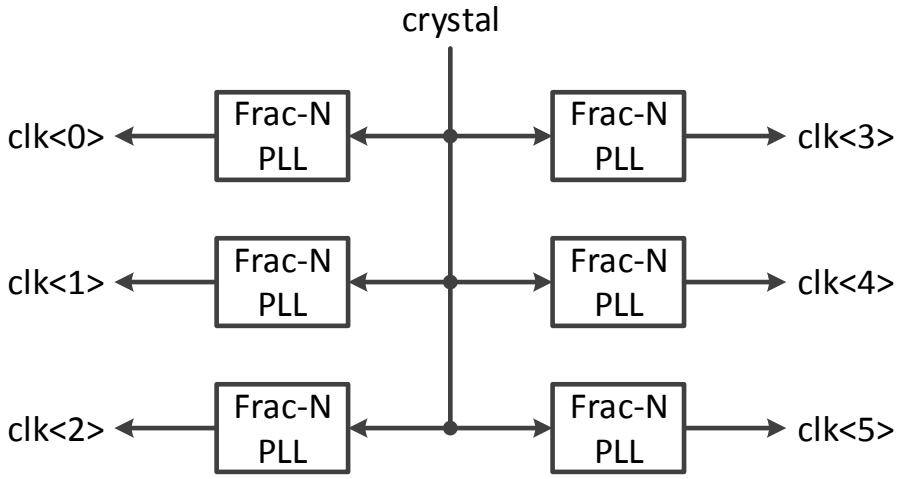

Figure 2.14: Multiple digital fractional-N PLL

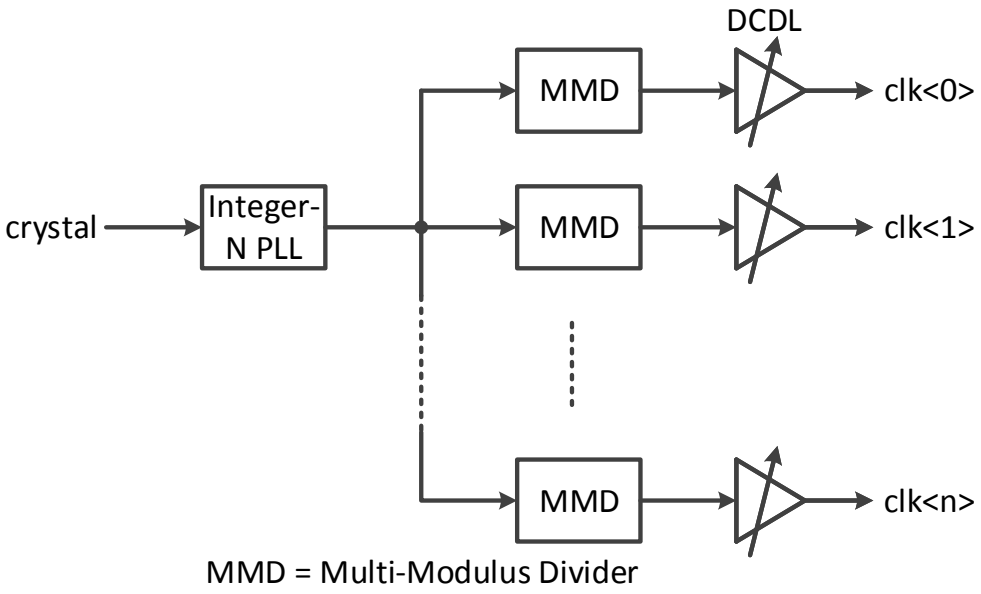

Figure 2.15: Open loop clock generation using fractional dividers

oscillator to improve the frequency resolution has the drawback of reducing the oscillator frequency. The supply sensitivity of the ring oscillator is also drastically degraded.

The order of the frequency control loop was reduced in a delay-locked loop (DLL) simultaneously reducing, both the complexity of the control loop and the response time of the clock generator. Additionally, the drawbacks of the closed-loop topology were removed by using open-loop generation in [11]. The circuit used digitally controlled delay lines (DCDL) driven by a digital modulator to synthesize the output waveform. However, it suffers from the phase errors in the delay line, and the reported power consumption was quite high.

The range of available frequencies was extended by preceding the digitally controlled delay line by a fractional frequency divider in [13] (Fig. 2.15). It, however, did not address the issue of phase errors in the delay line. Furthermore, the inverter based topology is very sensitive to power supply noise.

In conclusion, all the prior-art on clock generation are either not suitable for multiple output generation, or have degraded jitter and/or power performance due to phase errors in the phase modulator. The digital inverter based techniques suffer from high power supply noise sensitivity, as well. In this work, the errors in the phase modulator are compensated, to demonstrate the generation of clean output signal from an RF phase modulator. The open loop topology enables the generation of multiple clock outputs. In addition, the differential topology benefits from improved power supply noise sensitivity.

Chapter 3

Open Loop Phase Modulation

This chapter presents a formal introduction to open loop phase modulation, followed with a detailed discussion on the design considerations for achieving high resolution. Subsequently, a few optimization techniques for the phase noise cancellation technique [2] are discussed. Finally, an optimization for the digital quantizer is discussed for improving the noise performance in the receive band of the system.

3.1 INTRODUCTION

In a typical open loop phase modulator, a phase generator block produces multiple phases at the carrier frequency. It is followed by a phase multiplexer whose output is controlled by the phase modulation data (Fig. 3.1). For a given sequence of desired digital phase values φ[n], a $\Sigma - \Delta$ modulator quantizes each phase sample φ[n] to one of the M available phases, $2\pi \times \frac{k}{M}$, $k = 0, 1, \ldots, M - 1$. The output of the $\Sigma - \Delta$ modulator controls a digital-to-phase converter, whose inputs are M phase signals, $s_k = \cos\left(\omega_c + 2\pi \times \frac{k}{M}\right)$. Note that ω_c is the carrier frequency in rad/s. The digital-to-phase converter can be a phase multiplexer with M phase inputs or a digital phase interpolator. The resultant synthesized signal can be written as:

$$s_s(t) = \cos\left(\omega_c t + \sum_{n=1}^{\infty} (\phi[n] + \phi_q[n]) \cdot p(t - nT_s)\right) \tag{3.1}$$

where pulse-shaping function, p(t) is nominally a rectangular pulse of unit amplitude with duration Ts, and $\phi_q[n]$ is the error in quantizing $\phi[n]$. By employing a large number of

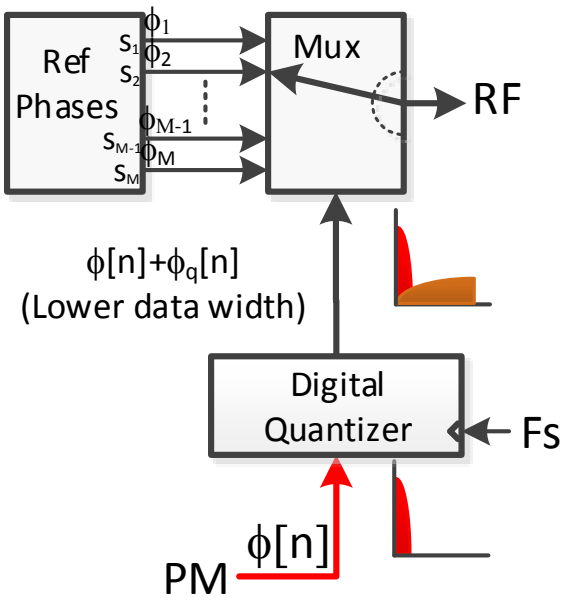

Figure 3.1: Digital open loop phase modulation (DPM)

phases, M, and a high switching frequency, $F_S = 1/T_S$, desired angle modulation, e.g., PSK, GMSK etc. can be realized with good EVM and ACPR.

Alternatively, if $\phi[n]$ were a ramp, i.e. $\phi[n] = \Delta\phi.n$, as shown in Fig. 3.2, a periodic signal with frequency:

$$F_{OUT} = F_C - \frac{F_S \cdot \Delta\phi}{2\pi} \tag{3.2}$$

is synthesized; i.e., frequency synthesis is possible by choosing an appropriate $\Delta\phi$. The frequency resolution may seem to be limited by the smallest phase step, $\Delta\phi$, that can be achieved. However, arbitrarily fine frequency synthesis can be achieved by employing a Σ–Δ modulator ("Digital Quantizer" in Fig. 3.1) to quantize the phase ramp. Note also

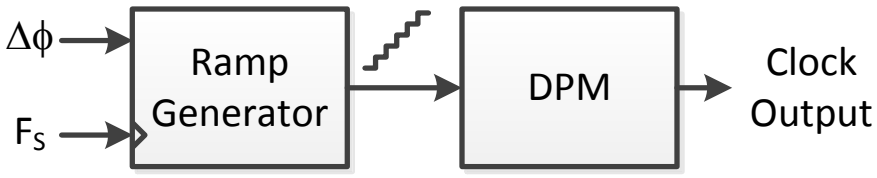

Figure 3.2: Application of DPM in frequency synthesis

that the range of frequency which can be synthesized by this method is bounded by $\pm F_S/2$ around F_C [28] but can be extended further by employing frequency dividers after the multiplexer.

Note that the clock source for phase switching, F_S can be derived synchronously either from the reference phase input to PM, F_C or from the DPM's RF output, F_{OUT}, with significant implications on output frequency, quantization noise, spectral purity and ease of implementation. These are discussed in section 3.2.4 in more detail.

3.2 Design Considerations In Digital Phase Modulation

The design of an open loop phase modulator must address the following challenges for achieving high resolution:

1. Generation of discrete phases
2. Phase quantization noise
3. Spectral images due to digital switching
4. Synchronization of phase switching
5. Phase errors in the phase generator

A detailed discussion of each of the above challenges is presented in the following subsections.

3.2.1 Generation of Discrete Phases

The bank of discrete phases are commonly generated by:

1. Frequency division [1],
2. Ring oscillators,
3. Delay-locked loops [3]
4. Digitally controlled delay-line (DCDL) [3,4]
5. Phase interpolation [2,5]

The simplest method for generating discrete phases is by using a frequency divide-by-2 circuit [1]. A divide-by-2 circuit readily generates the quadrature phases at a lower frequency. This commonly used circuit block can achieve very high frequencies. However, it only generates four discrete phases. For many applications, the quantization noise of the four phases overwhelms the circuit performance. Quantization noise shaping was used in [1]. With $\Sigma - \Delta$ quantization noise shaping, the in-band noise was lowered at the expense of large out-of-band noise (-25 dBr observed from the measured spectrum). In [1], while transmitting at 403.2 MHz, the measured FSK errors at 6 Mb/s data rate was

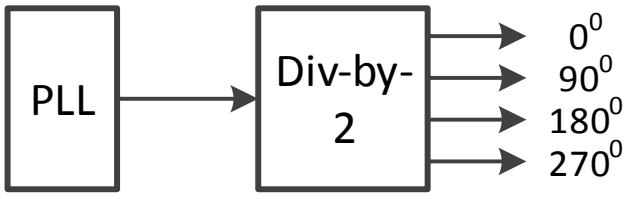

Figure 3.3: Phase generation by a divide-by-2 circuit

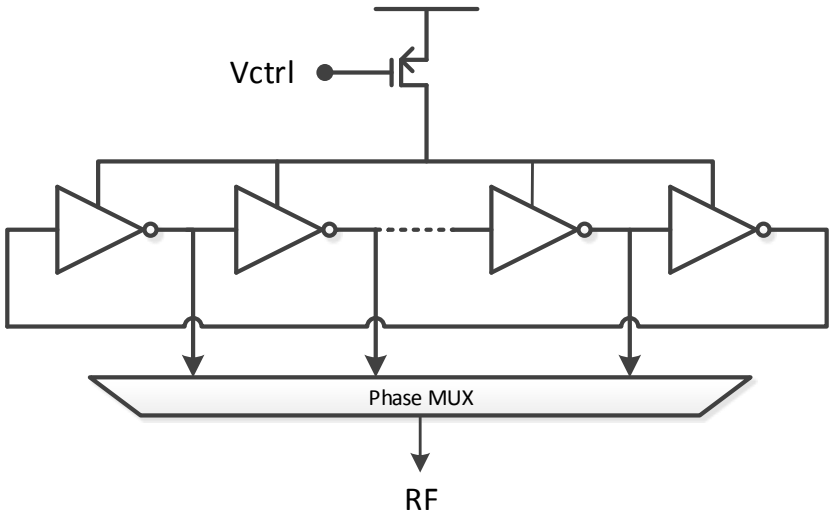

Figure 3.4: Ring oscillator based phase generator

4.1 % and 11.6 % for 2-FSK and GFSK modulations, respectively.

The number of discrete phases can be moderately increased by using a ring oscillator. The available number of phases increases as the number of inverter stages are increased, although, at the expense of reducing the oscillator speed. The trade-off between oscillator speed, f_{osc}, number of available phases, N and process-dependent inverter delay, t_{inv} is expressed by:

$$f_{osc} = \frac{1}{2 \times N \times t_{inv}} \tag{3.3}$$

Ring oscillators also suffer from high phase noise of the oscillator. The approach is, still, useful for low frequency, low resolution applications, like generation of clocks for digital circuits. Ring oscillators with LC stages are also possible for an improvement in phase noise, although their design will be highly constrained by the area requirement of an inductor.

Phase noise in the reference phases can be moderately improved by using a low phase noise oscillator for generating a reference phase and using it to drive a chain of inverters for generating the discrete phases as shown in Fig. 3.5. The discrete phases are inverter delay apart and varies with process, voltage and temperature. In this implementation, if a phase range of 360^0 is required, this variation results in large errors at the 360^0 to 0^0 phase transition.

The static delay variation is improved by controlling the inverter delay chain inside a delay-locked loop (Fig. 3.6). The delay-locked loop forces the total variation across the inverter chain to equal once clock cycle of the reference phases. The issues due to inverter delay variation are fixed by this approach, although at the expense of additional control circuitry for adjusting inverter delays. The phase resolution is, however, still limited by an inverter gate delay.

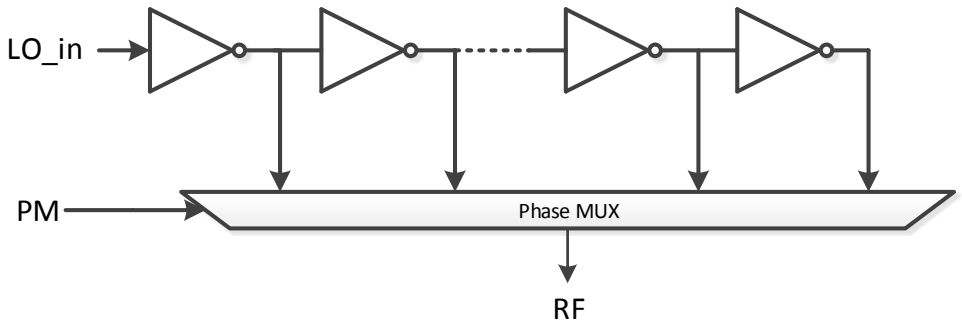

Figure 3.5: Inverter-delay line based phase generator

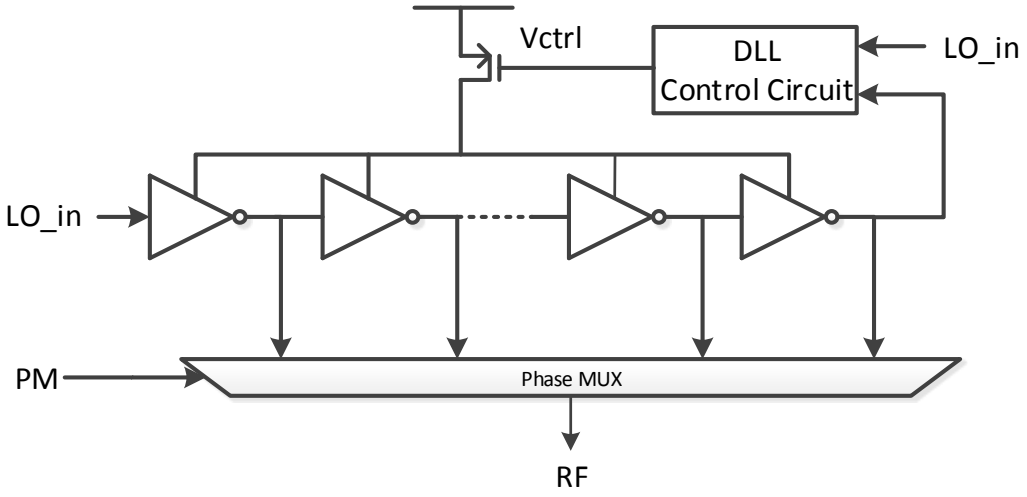

Figure 3.6: DLL based phase generator

In [3], the number of available discrete phases was further increased by adding a bank of digitally controlled capacitors for generating fine steps in the phase generator (Fig. 3.7). The capacitor bank enables very fine inverter gate delay control, which is, usually, about 10x better than one inverter delay. The phase modulator in [3] had 9 bit resolution for phase control. The digital logic was simplified by splitting the inverter delays between a coarse delay stage and a fine delay stage. It should be noted that such splitting of phase control results in added complexity due to the gain and timing mismatch between the two stages.

Irrespective of improvements in resolution, all of the inverter based phase generator have high sensitivity to supply noise, necessitating the use of a supply regulator in high resolution applications. The supply noise added by the inverter stages can be reduced by using differential stages at all levels. Although, not as good as a differential analog circuit, differential inverting stages contribute lower power supply noise than a

corresponding single ended stage. Additionally, the impact of power supply noise on the output phase of an inverter delay depends on the slew rate of the signal:

$$\Delta t_n = \frac{v_n(t)}{SR} \tag{3.4}$$

where $v_n(t)$ is power supply noise, SR is slew rate of inverter output, and Δt_n is the timing noise added to inverter output. Clearly, a high slew rate is desirable to combat the impact of power supply noise in inverter based phase generators.

Phase interpolation offers a low power alternative that eschews the phase multiplexer and generates the desired phase on demand [2,5]. Fig. 3.8 shows a conceptual interpolation circuit. It generates a weighted sum of two reference phases of the carrier. It is fully differential, consumes low power and offers wide bandwidth. Excellent phase resolution can be achieved if not for systematic and random errors.

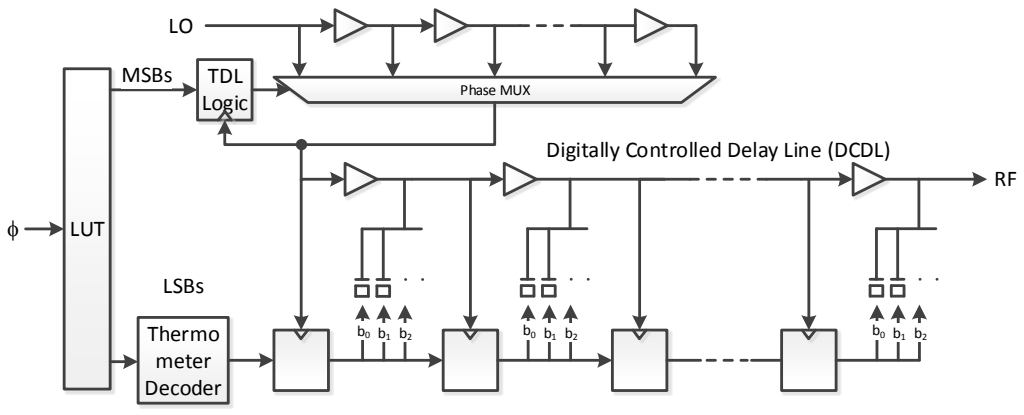

Figure 3.7: Digitally controlled delay line

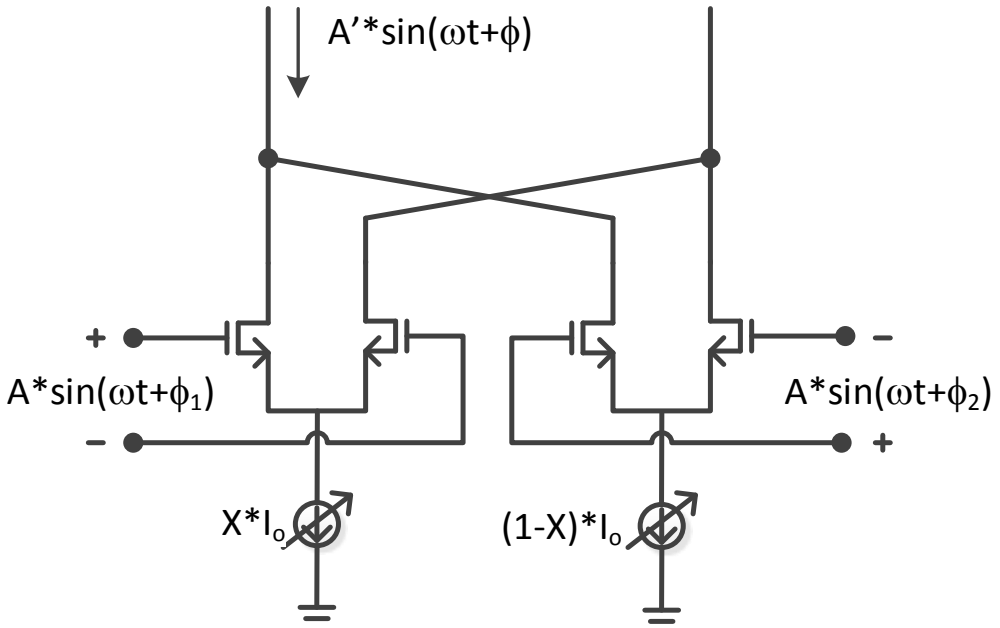

Figure 3.8: Phase Interpolation

For example, for sinusoidal inputs, phase interpolation of two reference phases at ϕ_1 and ϕ_2 results in an output signal with phase, ϕ given by:

$$\phi = \sin^{-1}\left(\frac{X \cdot \sin(\phi_1) + (1-X)\cdot \sin(\phi_2)}{X \cdot \cos(\phi_1) + (1-X)\cdot \cos(\phi_2)}\right) \tag{3.5}$$

where X and (1-X) are the weights applied to the interpolating phases. For $\phi_1 = 90^0$ and $\phi_2 = 0^0$, Eq. 3.5, reduces to:

$$\phi = \tan^{-1}\left(\frac{X}{1-X}\right) \tag{3.6}$$

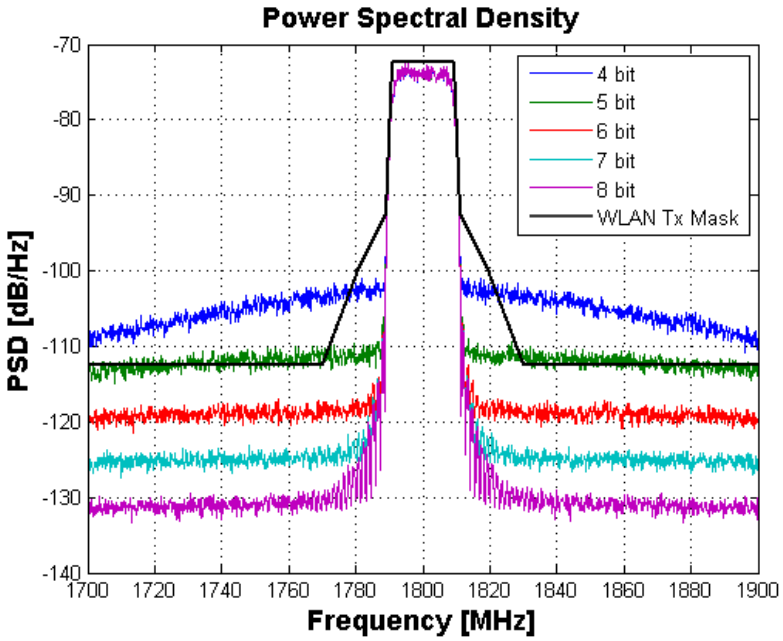

Figure 3.9: Power spectral density of phase quantization noise vs. number of bits (for 16 QAM modulation, at a data rate of 18 Mbps and switching frequency of 450 Mbps).

3.2.2 Phase Quantization Noise

Phase quantization noise (PQN) can be contrasted with the quantization noise added by baseband DACs in an I—Q architecture. In the latter, out-of-band quantization noise and spectral images of baseband DACs can be removed by baseband low pass filters, although the total power consumption also gets increased. Furthermore, the noise generated by the low pass filters adds on top of the contributions from the mixer and amplifiers in the transmit chain. Such a filter in a digital phase modulator will have to be RF band pass, requiring high Q passive components or a SAW filter. Such a filter is both area and power hungry, therefore, other circuit and system techniques are desired to reduce phase quantization noise.

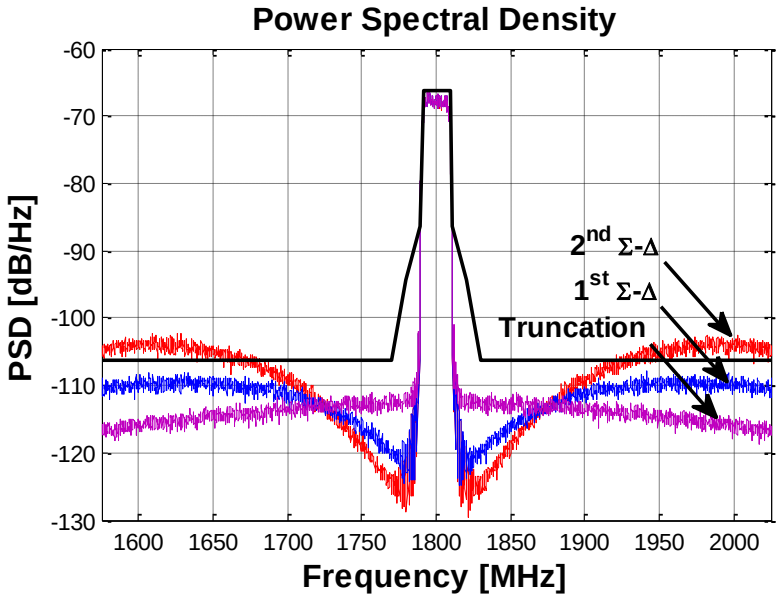

Figure 3.10: Power spectral density of phase quantization noise for digital truncation, 1st order $\Sigma - \Delta$, and 2nd order $\Sigma - \Delta$ modulated output (for 64 QAM modulation, at a data rate of 18 Mbps and switching frequency of 450 Mbps).

3.2.2.1 Power Spectral Density of Phase Quantization Noise

Similar to a voltage DAC, the output spectrum of phase quantization noise improves by 6 dB per bit increase in phase resolution. The simulated phase quantization noise when transmitting 18 Mbps, 64 QAM modulation and switching at 450 MHz, is plotted in Fig. 3.9.

3.2.2.2 Phase Quantization Noise Shaping

The shape of phase quantization can be shaped to meet the requirements on spectral mask, while requiring minimal level of quantization. For example, a 1st order $\Sigma - \Delta$ modulated quantization has low in-band noise, while the noise at high-offset

frequencies are elevated. As the order of noise shaping is increased, the noise at high-offset frequencies increases rapidly (Fig. 3.10). The trade-offs become evident as we look at the ACPR and EVM plots for the simple truncation, 1st order $\Sigma - \Delta$ and 2nd order $\Sigma - \Delta$ modulated outputs. For low quantization level, 1st order $\Sigma - \Delta$ results in better EVM than digital truncation without much impact on ACPR. Also, in the 2nd order $\Sigma - \Delta$ modulator, the quantization noise can fold in-band, when the level of noise is relatively high, as seen in a 4-bit phase modulator.

3.2.2.3 Phase Quantization Noise Cancellation

A quantization noise cancellation path can be added to the modulator output, through a second VCO control port as shown in Fig. 3.13 [2]. The required cancellation signal is obtained by first subtracting the input signal, $\phi[n]$ from the quantized signal, $\phi[n] + \phi_q[n]$. Thus, the quantized phase data $\phi[n] + \phi_q[n]$ is applied through the digital-to-phase converter, while the PQN cancellation signal of $-\phi_q[n]$ is applied through a cancellation path through the VCO.

Frequency of the VCO output can be controlled in a straightforward manner through an analog control signal, or through a digital word in the case of a Digitally Controlled Oscillator. Its phase, on the other hand, is the outcome of an integration of the resultant frequency. Since the cancellation signal is a phase quantity, while the VCO input port controls its frequency, the required cancellation phase is differentiated, $(1 - z^{-1})$ to obtain an equivalent VCO frequency deviation. It must also be attenuated by VCO's control voltage-to-frequency gain, K_{VCO}.

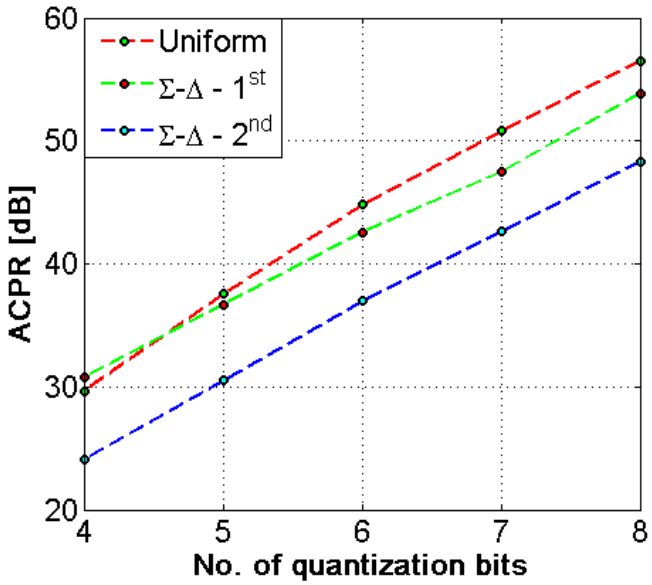

Figure 3.11: ACPR of digital truncation, 1st order $\Sigma - \Delta$, and 2nd order $\Sigma - \Delta$ modulated output

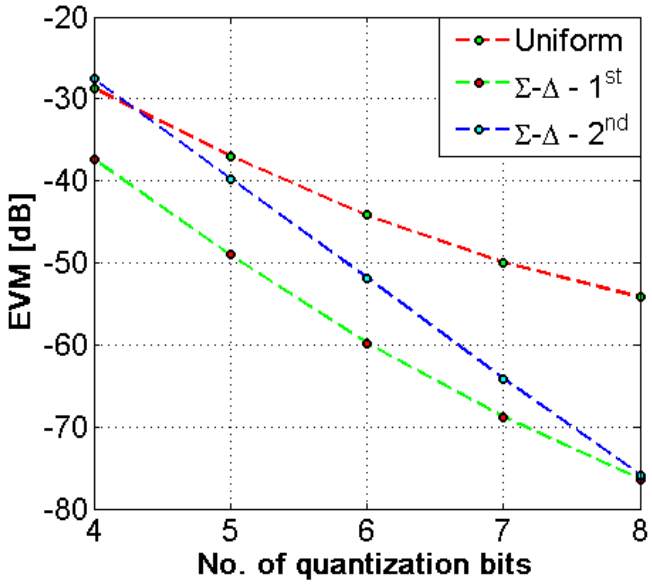

Figure 3.12: EVM of digital truncation, 1st order $\Sigma - \Delta$, and 2nd order $\Sigma - \Delta$ modulated output

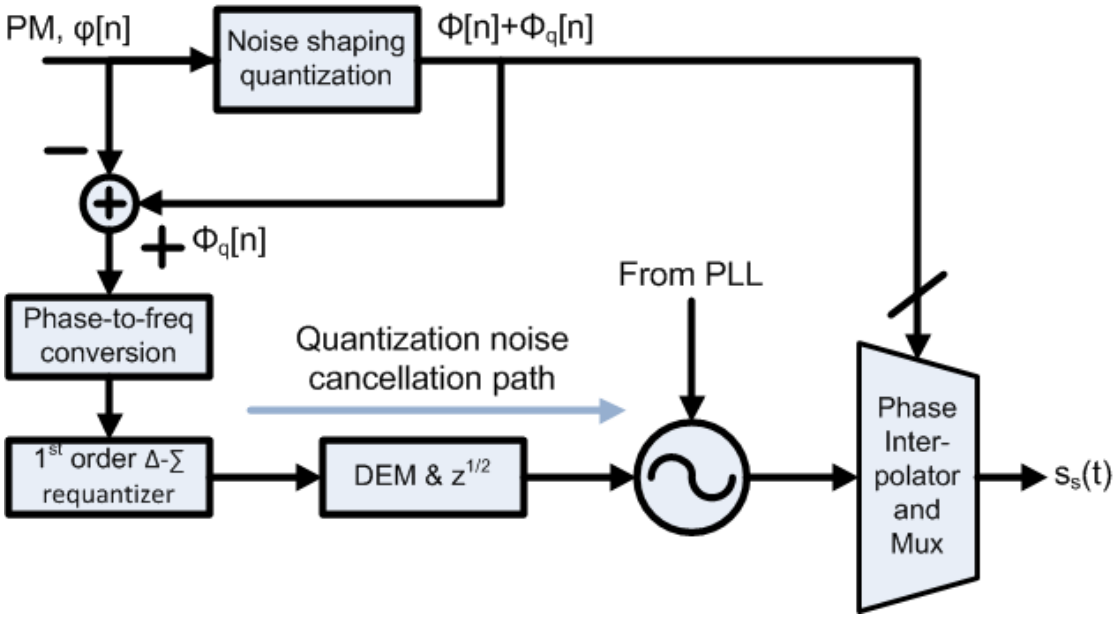

Figure 3.13: Block diagram of phase quantization noise cancellation [8]

In [2], a state-of-the-art implementation of PQN cancellation was presented on a 2.4 GHz wide-bandwidth open-loop GFSK transmitter IC. The phase cancellation path was implemented by adding a second VCO port to control a 4-bit capacitor bank, with DEM logic incorporated in the selection process. In [2], 9 dB improvement was the measured while transmitting 20 Mb/s GFSK modulation output spectrum, after enabling the phase noise cancellation technique.

3.2.3 Spectral Images

Due to the digital implementation of the phase modulator, the digital data is held constant for one clock cycle of the switching clock (Fig. 3.14). This zero-order hold imparts a square pulse shape, as the phase modulation data transitions from the digital to

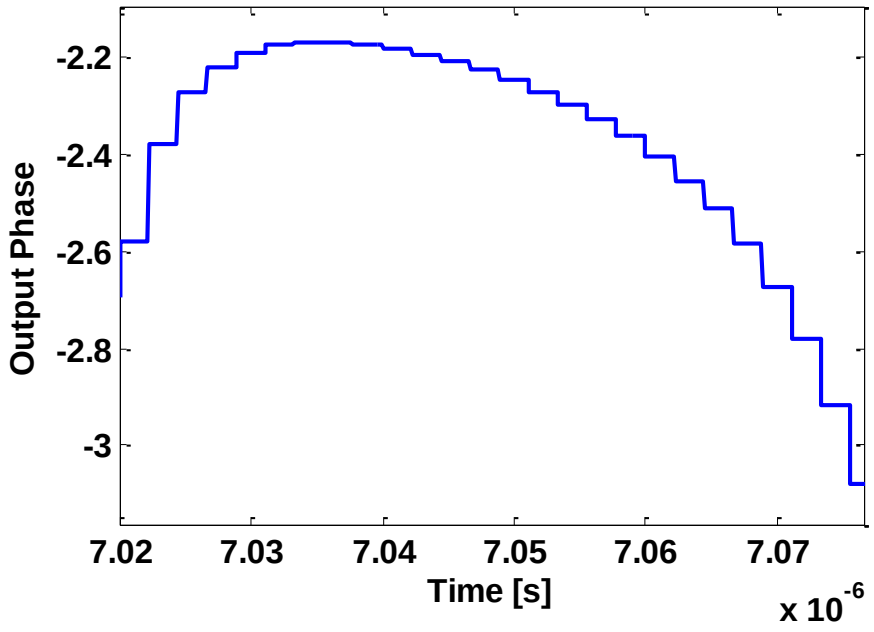

Figure 3.14: Typical sample and held waveform of PM data

the analog domain. In the frequency domain, this operation is equivalent to convolution of the spectrum of the digital data with that of the square pulse.

In the analog domain, spectral images are created at multiples of the switching frequency. Additionally due to the zero order hold, the input signal, quantization noise and spectral images are filtered by a sinc-shaped filter resulting from the convolution with the square pulse shape. The level of spectral images after the sinc filtering can be expressed as:

$$Min.Rejection = 10 \times \log_{10}\left(sinc^2\left(\pi \times \left(1 - \frac{F_B}{2F_S}\right)\right)\right) \qquad (3.7)$$

where F_B is the bandwidth of the input signal, F_S is the switching frequency, and rejection is the minimum difference in levels between the input signal and spectral images as

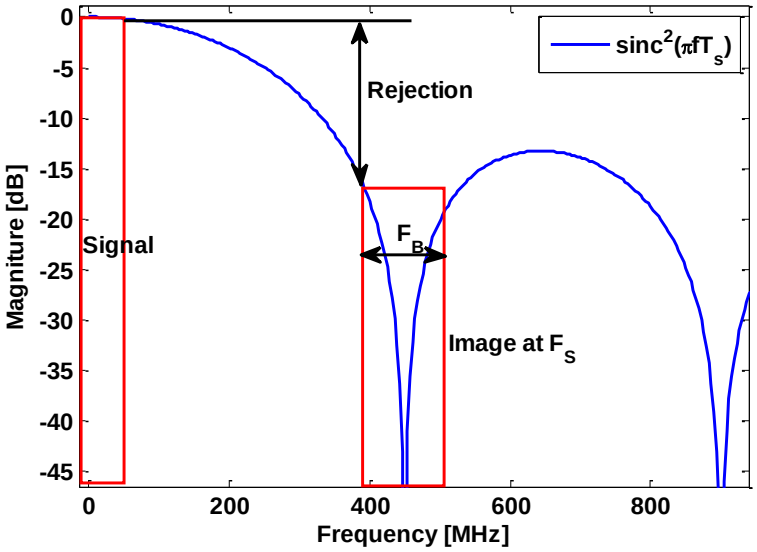

Figure 3.15: Minimum rejection due to sinc filtering

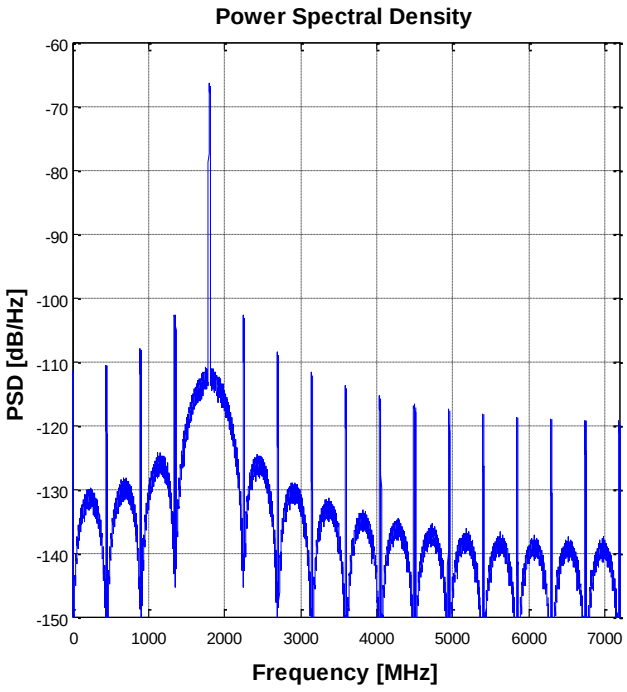

Figure 3.16: Typical output spectrum after sinc filtering due to zero-order hold

shown in Fig. 3.15. As the ratio (F_B/F_S) is reduced by increasing F_S, the rejection also improves. As F_S is increased, the spectral images are also pushed farther away from the RF output, making image filtering by a passive filter easier. The spectral images after sinc filtering in a typical output of the phase modulator is depicted in Fig. 3.16.

3.2.4 Synchronization of Phase Switching

As mentioned before, the phase switching clock, F_S (see Fig. 3.1) can be derived from: (a) the clean, unmodulated PLL output, or (b) the phase modulated RF output. In this work, the former approach was employed. This simplifies the digital interface between the DSP generating the phase modulation data and the phase modulator itself, as both can run from a single clock domain. In contrast, the latter approach could have degraded EVM and ACPR performance because the phases would have been switched

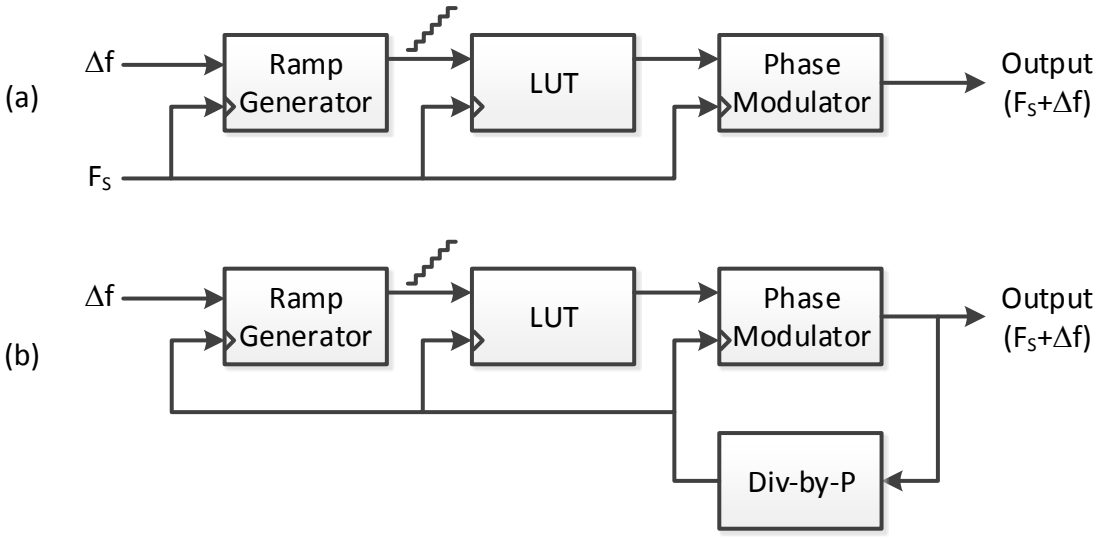

Figure 3.17: Phase synchronization clock, F_S for frequency generation derived from: (a) Clean, unmodulated PLL output; or (b) Phase modulated output of phase modulator

non-uniformly owing to the use of a phase modulated clock.

It is important to note that our choice comes with certain disadvantages particularly when performing frequency synthesis (Fig. 3.17). In this case, F_{out} may not be harmonically related to F_S, the rate of phase jumps. So, strong fractional spurs will result. For example, for a desired output at $F_{out} = F_C + \Delta f$, there would be a very strong spur at $F_C - \Delta f$. The magnitude of this spur is computed in Appendix 3.5.2 and its magnitude for $\Delta\phi \ll 2\pi$, is approximated by:

$$P_{fund} - P_{imag} = 20 \times \log_{10}\left(\frac{\Delta\phi}{2k\pi}\right) \tag{3.8}$$

where $k = 2F_C/F_S$, F_C, P_{fund} and P_{imag} are strengths of the RF carrier, fundamental output and image tone, respectively. Additionally, the harmonics of the fundamental carrier also cause spurs at close-in frequencies. For example, the third harmonic of the RF carrier causes a spur at $F_C \pm 3\Delta f$. The magnitude of this spur is computed in Appendix 3.5.3 and its magnitude is given by:

$$P_{fund} - P_{3x} = 20 \times \log_{10}\left(\alpha_3 sinc\left(k \pm \frac{3\Delta\omega}{2\pi F_S}\right)\right) \tag{3.9}$$

where P_{3x} is the strength of the tone at $F_C \pm 3\Delta f$ and α_3 is the magnitude of third harmonic of RF carrier relative to fundamental.

In contrast, if F_S were derived from F_{out} (e.g., is a subharmonic of F_{out}) these fractional spurs would be theoretically absent. The reader is referred to an excellent analysis of so-called "flying adders" that employ such a synchronization strategy [14-15].

3.2.5 Phase Errors in the Phase Generator

The primary sources of static phase errors in the phase generator can be classified into:

1. Systematic errors
2. Random errors
3. Dynamic errors

We discuss each of these errors in detail in the following sub-sections.

3.2.5.1 Systematic Errors

Systematic sources of phase errors include circuit non-linearity and phase errors due to higher harmonics in the reference phase input. In a phase interpolator based phase generator (see section 3.2.1), the expression for output phase (Eq. 3.5) is sinusoidal and therefore output will have strong spurs, if this sinusoidal non-linearity is not compensated. For a phase interpolator with two reference phases that are 90^0 apart, the output phase vs input control code is plotted in Fig. 3.18. The distortion caused due to systematic errors is evident from elevated levels of out-of-band noise in Fig. 3.19. This error is one of the most dominant source of performance limitation for achieving high resolution and techniques to improve systematic linearity will be discussed in greater detail in Chapter 3.

3.2.5.2 Random Errors

Aside from the systematic errors, the inevitable component mismatches due to component fabrication is another source of phase errors in a phase modulator. They are un-avoidable in any architecture. The device mismatch (both threshold and beta) is

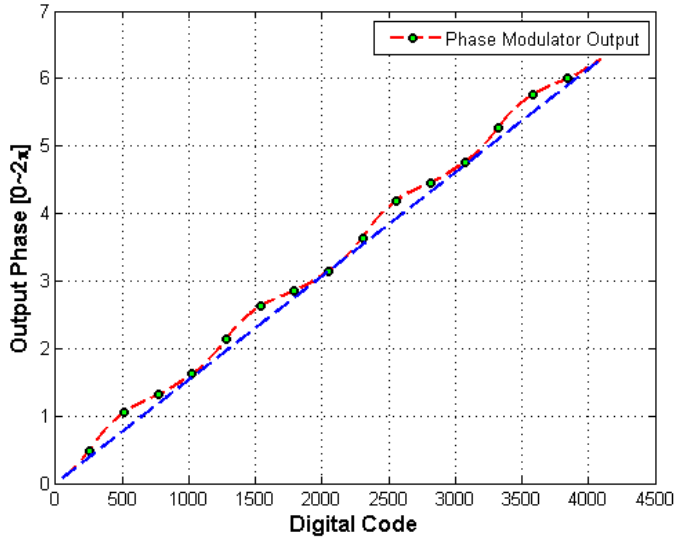

Figure 3.18: Output phase vs input digital code for phase interpolator with input 90° phase offset between reference phases

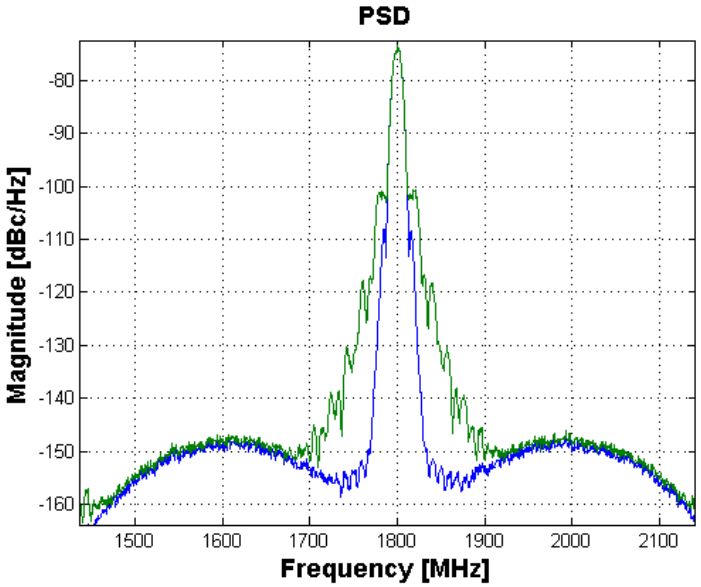

Figure 3.19: Output distortion due to systematic non-linearity of a phase interpolator (simulated output of 18 Mbps GFSK data, switching at 450 Mbps)

proportional to device area and the standard deviation of the mismatch coefficient can be expressed as:

$$\sigma = \frac{A}{\sqrt{W \times L}} \tag{3.10}$$

where A is a constant, W and L are the width and length of the transistor, respectively. Additionally, the current mismatch is also dependent on the overdrive voltage, and it becomes worse as the overdrive voltage is lowered. Therefore, at constant bandwidth, both the area and the power consumption of the transistor must be increased. This leads to a proportional increase in power consumption of the driving stages as well.

3.2.5.2 Dynamic Errors

Dynamic errors include errors due to incomplete settling, code dependent settling time of the phase modulator, and supply noise due to digital activity. Supply noise can be reduced by ensuring differential signals for most of the circuits connected to the same supply as that of the phase modulator. For a well-designed, high bandwidth phase modulator, issues due to incomplete settling can be minimized. However, these sources become the dominant source of error once the random and systematic sources are compensated. In this work, dynamic errors were avoided by careful circuit and layout design and it is surmised, that system solutions for tackling dynamic errors can further improve the performance of the phase modulator.

3.3 QUANTIZATION NOISE CANCELLATION: OPTIMIZATION TECHNIQUES

One of the subtle features of the cancellation path is the implication of discrete-time differentiation applied to obtain the required VCO frequency deviation. The integration of frequency inherent in a VCO is, on the other hand, continuous. Consider the case of rectangular pulse shape for the input phase and cancellation signal, where both of them are applied at a frequency, Fs = 1/Ts. Since, the cancellation signal is updated every Ts time period, while VCO frequency is continuously being integrated, perfect cancellation is obtained only at the end of each time period, which is not very effective. Fig. 3.21(b) depicts the timing diagram of phase quantization noise, the applied cancellation signal and the un-cancelled PQN. In order to improve the effectiveness of noise cancellation, two techniques are described in the following subsections – advancement of cancellation signal and reduction in integration time. Since the techniques are applicable to all forms of PQN shaping algorithm and for any resolution in the phase data path, a 2nd order $\Sigma - \Delta$ noise shaping with a 5-bit quantizer in the forward path is used to illustrate these techniques. For all system simulations in this sub-section, input data is 20 Mb/s GFSK modulated.

3.3.1 Advancement of Cancellation Signal

The control voltage-to-frequency response of VCO to a cancellation signal was found to be low pass with a very high cutoff frequency (>Fs). Hence, it was modeled as a rectangular pulse shape. The transfer function of un-cancelled PQN can be expressed mathematically as:

$$S_{\phi_n,un-cancel} = NTF_1(f) \times P_1(f) \times K_1(f) \tag{3.11}$$

where $NTF_1(f)$ is the NTF of $\Sigma - \Delta$ modulator quantizing $\phi[n]$, $P_1(f)$ models the pulse shaping function of un-cancelled $\phi_q[n]$ and $K_1(f)$ models the effect of PQN cancellation. When PQN cancellation is off, $P_1(f)$ is a sinc function, $\sin(\pi fTs)\,/\,(\pi fTs)$, representing zeroth-order hold and $K_1(f)$ is 1. However when a cancellation signal is applied through the VCO control port, two changes take place: (1) pulse shape of un-cancelled quantization noise becomes saw-tooth; and (2) magnitude of quantization noise is a first order difference, $(1 - z^{-1})$ of the initial quantization noise. These changes can be easily observed in the timing plot of Fig. 3.21(b). As a result, $P_1(f)$ attains a DC value of -6 dB and $K_1(f)$ becomes $4 \times \sin^2(\pi fTs)$. Saw-tooth pulse shape for PQN and

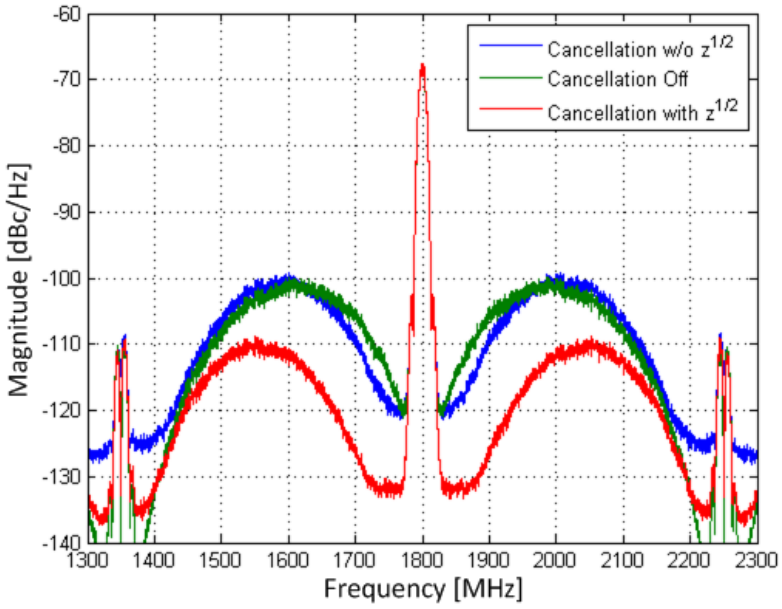

Figure 3.20: The simulated PSD of a GFSK modulated signal showing PQN cancellation obtained with and without Ts/2 advancement

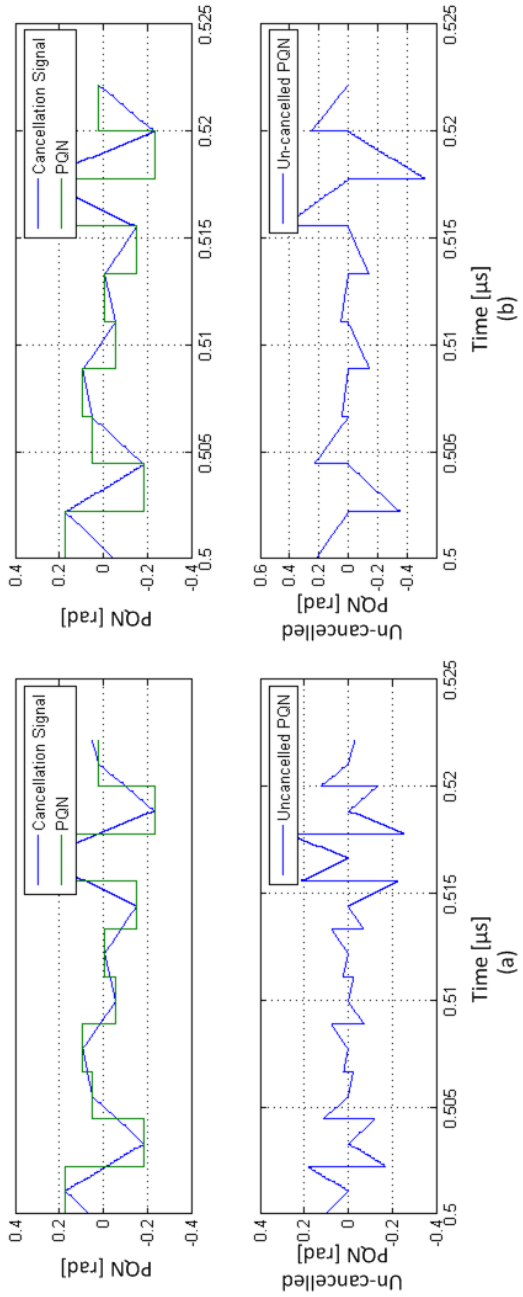

Figure 3.21: Timing diagram for PQN cancellation technique for (a) Ts/2 advancement in cancellation signal, and (b) no advancement in cancellation signal.

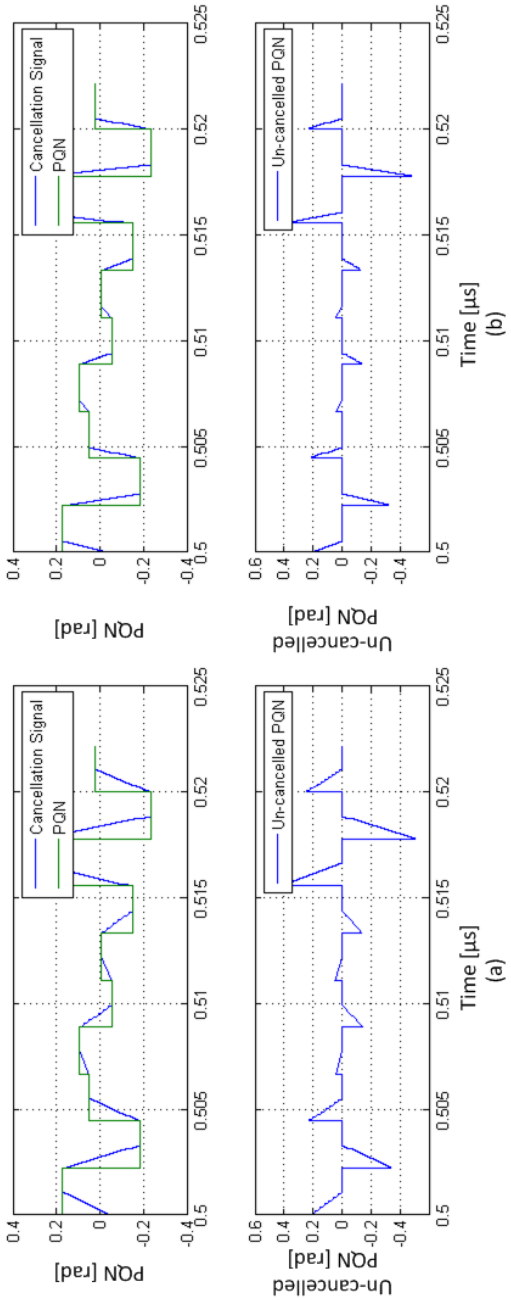

Figure 3.22: Timing diagram for PQN cancellation technique for (a) integration time of Ts/2 and (b) integration time of Ts/4, within each time period.

the additional first order noise shaping results in lower quantization noise at low frequencies, but higher noise at high frequencies (Fig. 3.20). Hence noise cancellation is limited to frequencies below 40 MHz offset; while it increased by 2 dB at higher offset frequencies due to the additional first order noise shaping.

In order to improve the PQN cancellation mechanism, the cancellation signal can be advanced by Ts/2. As a result, the residual quantization noise rises to only half of the value attained in the earlier case and afterwards its sign gets flipped (Fig. 3.21(a)). Hence, $P_1(f)$ has a zero at DC and $K_1(f)$ is reduced by 6 dB. The combined effect of these two changes is a reduction in peak quantization noise by 10 dB, along with a maximum improvement of 17 dB, at a lower frequency (Fig. 3.20). $P_1(f)$ and the expression of un-cancelled PQN, $S_{\phi_n,un-cancel}(f)$ for the three cases are plotted in Appendix 3.5.1. It should be noted that half period advancement results in the highest achievable noise cancellation, compared to other values for signal advancement.

3.3.2 Reduction in Integration Time

Further improvement in PQN cancellation can be obtained by using a return-to-zero (RZ) DAC or an equivalent DCO to control the deviations in VCO frequency. In this case, integration of frequency input to the VCO is performed for a shorter duration of time and hence perfect phase cancellation is obtained for a longer duration as opposed to one time instant. The required frequency deviation must also be increased in proportion to the reduction in integration time, such that the phase accumulated in one time period equals the required cancellation phase value. Figs. 3.22(a) & (b) depict the time waveforms for the cases when integration time is reduced to Ts/2 and Ts/4, respectively.

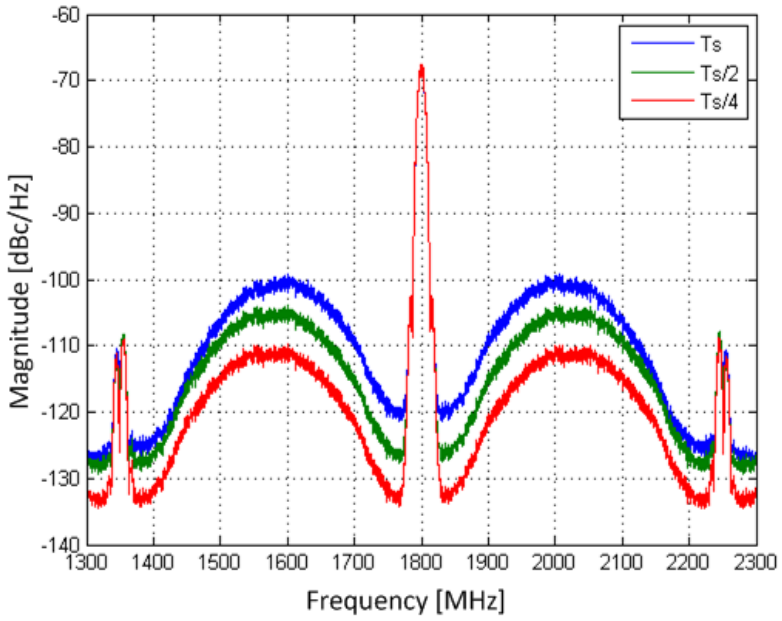

Figure 3.23: The simulated PSD of a GFSK modulated signal showing PQN reduction with decrease in integration time.

The resultant improvement in PQN cancellation is 6 dB for an integration time of Ts/2 as shown in Fig. 3.23. If the integration time is reduced further while simultaneously increasing the cancellation frequency signal, output PQN reduces by 6 dB for each octave reduction in integration time. In the limit of an impulse in frequency cancellation signal, perfect cancellation is obtained at all times. Since shorter integration time requires a larger frequency deviation from the VCO, there exists a trade-off between noise-cancellation and VCO frequency deviation. The minimum integration time, and the resultant noise-cancellation, is limited by the maximum frequency deviation that can be linearly obtained from the VCO. For instance, for a maximum achievable frequency deviation of 100 MHz and a 4 bit phase interpolator, the minimum integration time is 625

ps. In this example, 4 bit phase interpolator requires a maximum cancellation phase of 0.4 radians.

3.3.3 Combination of Cancellation Signal Advancement and Reduction in Integration Time

The improvement in noise cancellation can be further increased by combining both signal advancement and reduction in integration time. When integration time is reduced to Ts/2, the optimal signal advancement changes from Ts/2 to Ts/4, so that the peak magnitude of PQN splits equally in its positive and negative cycle.

In general, the optimal clock advancement reduces by a factor of 2, when the integration time is reduced by a factor of 2. The PSD of the output signal when Ts/4

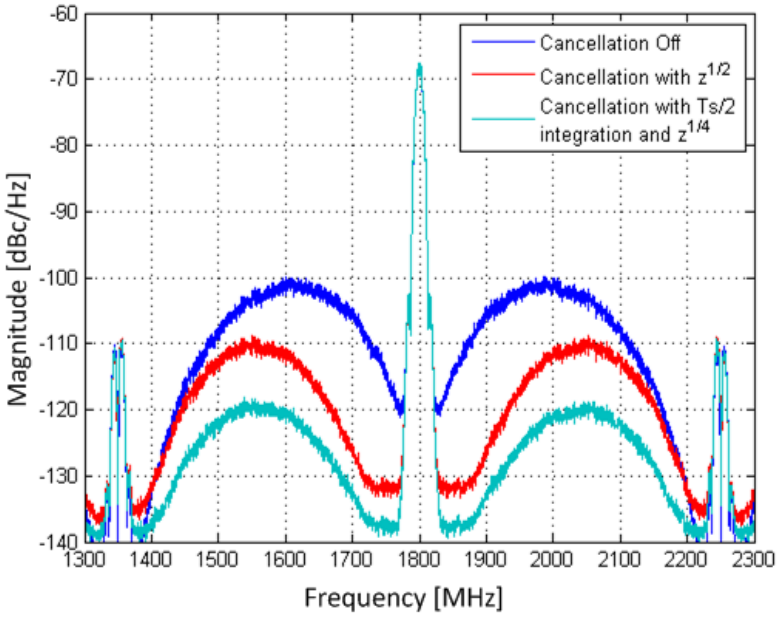

Figure 3.24: The simulated PSD of a GFSK modulated signal showing PQN reduction with optimized cancellation signal advancement and integration time.

clock advancement and Ts/2 integration time are used is plotted in Fig. 3.24. For comparison, PSD plots for zero clock advance and Ts integration time and Ts/2 clock advance and Ts/2 integration time are also plotted. The peak PQN has reduced by an additional amount of 10 dB due to simultaneous application of the two techniques.

3.3.4 Optimized Modulator for PQN Shaping

A second order $\Sigma - \Delta$ modulator results in excessive quantization noise at a frequency offset of Fs/2. This increase can lead to spectral mask violation. By including a pair of complex poles in the NTF [51], the high frequency noise can be reduced at the expense of higher noise at low frequencies. The improvement in noise reduction after the inclusion of a pair of complex poles in the NTF is depicted in Fig. 3.25(c). In addition, the low frequency noise degradation observed in 2^{nd} order $\Sigma - \Delta$ modulator due to the advancement of cancellation signal, has also improved resulting in lower noise for the optimized NTF.

3.3.4 Quantization of Cancellation Signal

Since in a digital implementation of the cancellation path, the frequency data fed to the second VCO port must go through a quantization process, its impact also requires a careful attention. If the frequency data is uniformly quantized within the input dynamic range of VCO control port, its quantization noise has a constant PSD between -Fs/2 and +Fs/2. Within the loop bandwidth of PLL, this noise will be tracked by the negative feedback loop and its impact will be nullified. Outside the loop bandwidth, VCO integrates this noise due to frequency to phase conversion and hence an amplified version

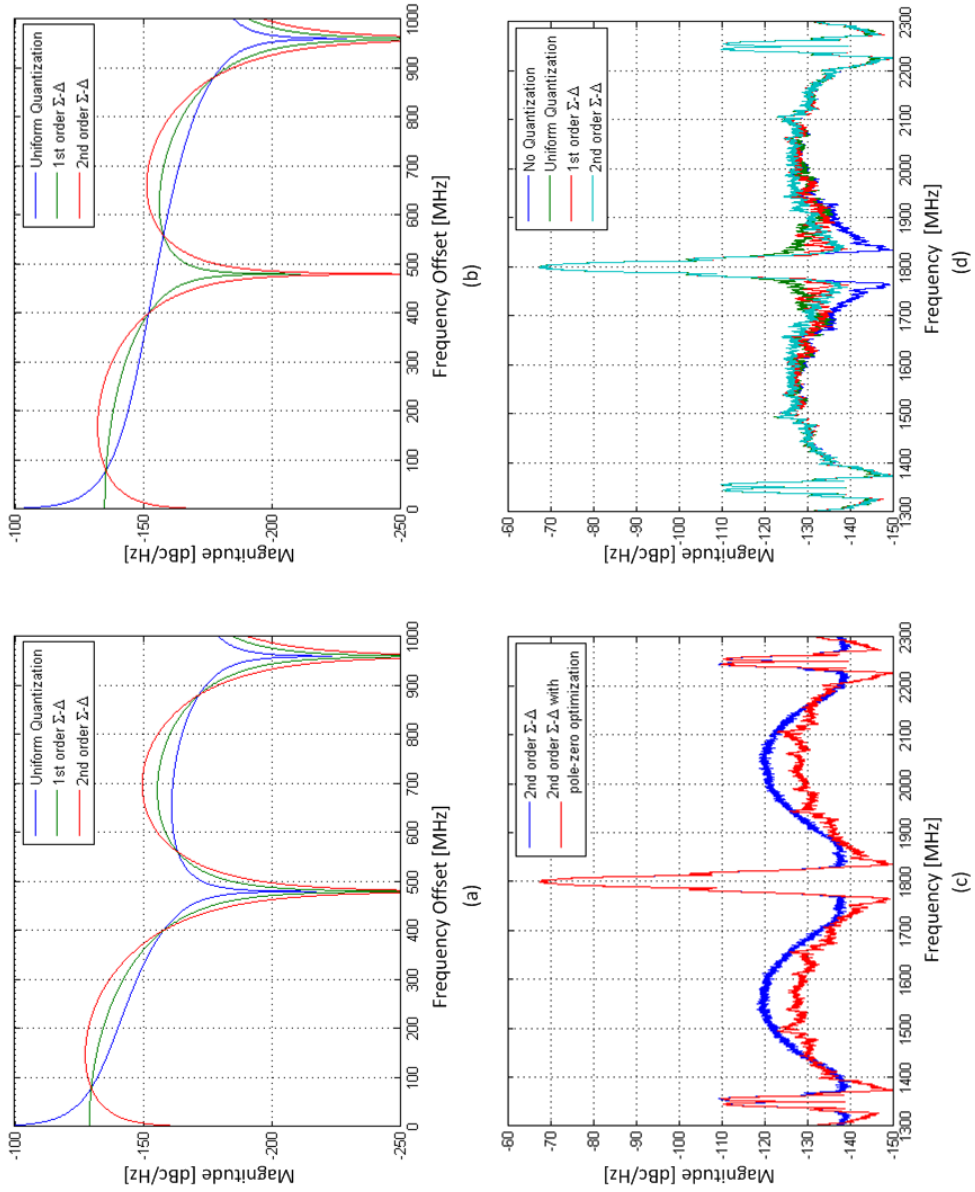

Figure 3.25: Plot of analytical expression for output quantization noise due to quantization in the cancellation path for (a) integration time of Ts, and (b) integration time of Ts/2. The simulated PSD of a GFSK modulated signal showing (c) PQN reduction with poles in the NTF of phase path, and (d) impact of quantization in the cancellation path using three types of quantizers.

will appear at its output. Mathematically, the PSD of quantization noise at VCO output can be expressed as:

$$S_{\varphi_{n,freq}}(f) = \frac{1}{4}\frac{\Delta^2}{12F_s} sinc^2\left(\frac{\pi f}{F_s}\right)\frac{K_{VCO}^2}{f^2} NTF_2(f) \tag{3.12}$$

where Δ is quantization step-size in VCO control voltage, F_S is sampling frequency, f is frequency offset from carrier, K_{VCO} is VCO gain and $NTF_2(f)$ is noise transfer function.

For an example case with K_{VCO} of 100 MHz/V, F_S of 450 MHz and Δ of 41 mV (5 bit quantization), the calculated output noise is plotted in Fig. 3.25(a) for uniform quantization, and 1st order and 2nd order $\Sigma - \Delta$ noise shaping. If the integration time is reduced to Ts/2, the expression for quantization noise changes to (Fig. 3.25(b)):

$$S_{\varphi_{n,freq}}(f) = \frac{1}{16}\frac{\Delta^2}{12F_s} sinc^2\left(\frac{\pi f}{2 \times F_s}\right)\frac{K_{VCO}^2}{f^2} NTF_2(f) \tag{3.13}$$

Clearly, for both cases, the noise at VCO output will suffer from both EVM and ACPR degradation if uniform quantization is applied. In order to cancel the pole in the VCO transfer function, a first or higher order zero is required in the NTF of the cancellation signal quantizer. First order noise shaping results in a flat noise PSD close to DC, while second order noise shaping has a zero at DC in its noise transfer function. Hence, the noise shaping employed must be of at least second order.

The impact of quantization in cancellation path while transmitting GFSK modulated data is shown in Fig. 3.25(d). It follows the behavior expected from the analytical expression.

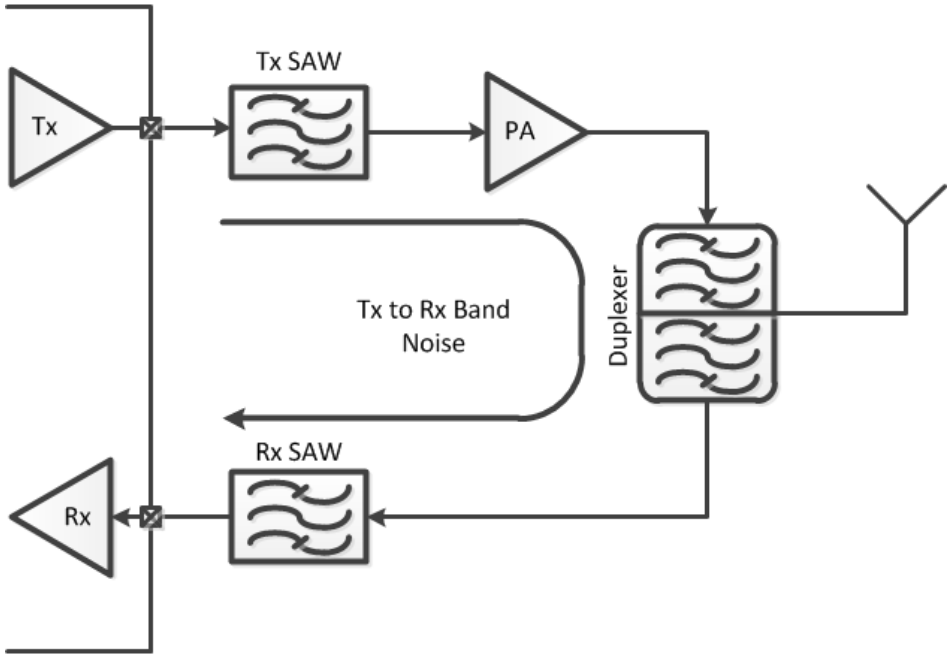

Figure 3.26: Diagram showing Tx signal leakage in a conventional transceiver.

3.4 RECEIVE BAND NOISE

In a Frequency Division Duplexing (FDD) system, both transmitter and receiver are operational simultaneously. For instance, in the LTE-FDD frequency planning Tx-Rx separation varies from 30 MHz in band XII (700 MHz), to 400 MHz in band X (Tx in 1710-1770 MHz and Rx in 2110-2170 MHz). Due to a finite duplexer Tx to Rx isolation, the transmitter noise in the receive frequency band leaks into the receiver, which can desensitize the receiver (Fig. 3.26). If the transmitter noise in the receive band is -160 dBc and the duplexer Tx-to-Rx isolation in the receive band is 47 dB, then noise power at LNA input is given by:

$$N_{Rx} = -160\ dBc - 47\ dB + (24 + 1.5 + 1.0)\ dBm$$
$$= -180.5\ \text{dBm} \tag{3.12}$$

assuming 24 dBm power at the antenna, 1.5 dB of duplexer Tx insertion loss and 1.0 dB of antenna switch insertion loss. As a result of this additional noise at LNA input, the receiver noise figure can degrade by 0.5 dB, if it was 3 dB in the beginning (without including switch and duplexer loss). In the phase path of a polar transmitter, this noise is composed of PLL phase noise and quantization noise added by the digital phase modulator**.** In practice, the phase noise of the PLL can be reduced to meet the requirement in the receive band. Consequently, the quantization noise of the modulator becomes the dominant source of noise.

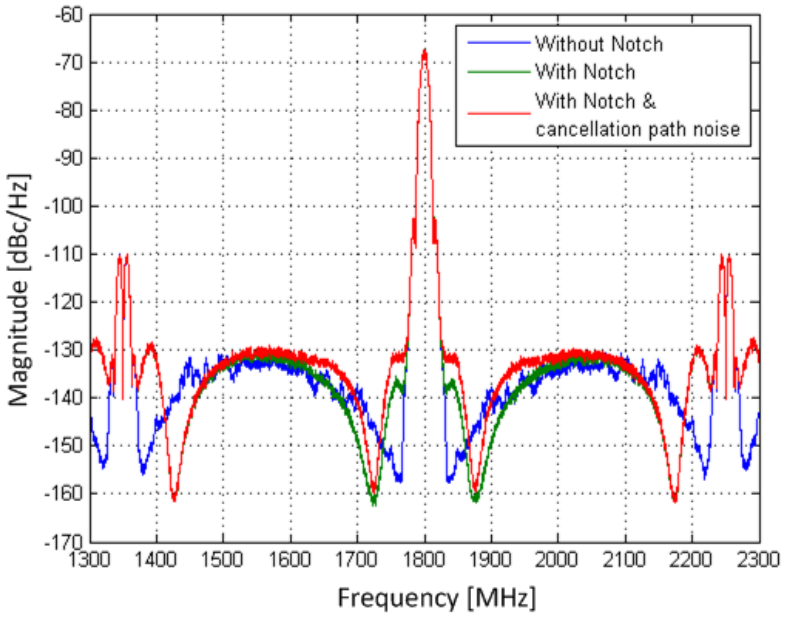

Figure 3.27: The simulated PSD of a GFSK modulated signal before and after the inclusion of a notch at 80 MHz offset. Degradation by 2 dB is observed due to quantization noise in the cancellation path.

However, the additional components can be avoided by positioning a quantization Noise Transfer Function (NTF) notch at the receive band frequency. The quantizer of the phase modulator can be modified to include a zero in the quantization noise transfer function. Due to high pass shaping of quantization noise, the 30-70 MHz Rx band offset poses less design challenge. Improvement in noise at the receive band due to NTF notch at 80 MHz is shown in Fig. 3.27. The resolution of digital phase modulator was increased from 5 bits to 6 in this simulation, to lower its noise contribution. The modulator also employs PQN cancellation technique with Ts/4 advancement in the cancellation path for an integration time of Ts/2. For comparison, the transfer function without the notch, but including the same PQN cancellation technique, is also shown. An improvement of 12 dB is obtained due to the notch in the transfer function. When the cancellation path is quantized to 5 bits, the noise performance degraded by 2 dB due to the additional noise of the cancellation path. The ACPR performance of the modulator is better than 62 dB in the out-of-band region which meets the requirement of both LTE and WiMAX. Although the ACPR specification can be met with a lower resolution, atleast 4 bits are generally required to keep the frequency deviation in the cancellation path within a reasonable range.

3.5 CHAPTER APPENDIX

3.5.1 Noise Transfer Function in Phase Quantization Noise

Pulse shaping function for a rectangular pulse, saw-tooth pulse (saw-tooth1) and modified saw-tooth pulse obtained after advancing cancellation signal by Ts/2 (saw-tooth2):

$$P_1(f)_{rect} = sinc^2(\pi f T_s) \tag{3.13}$$

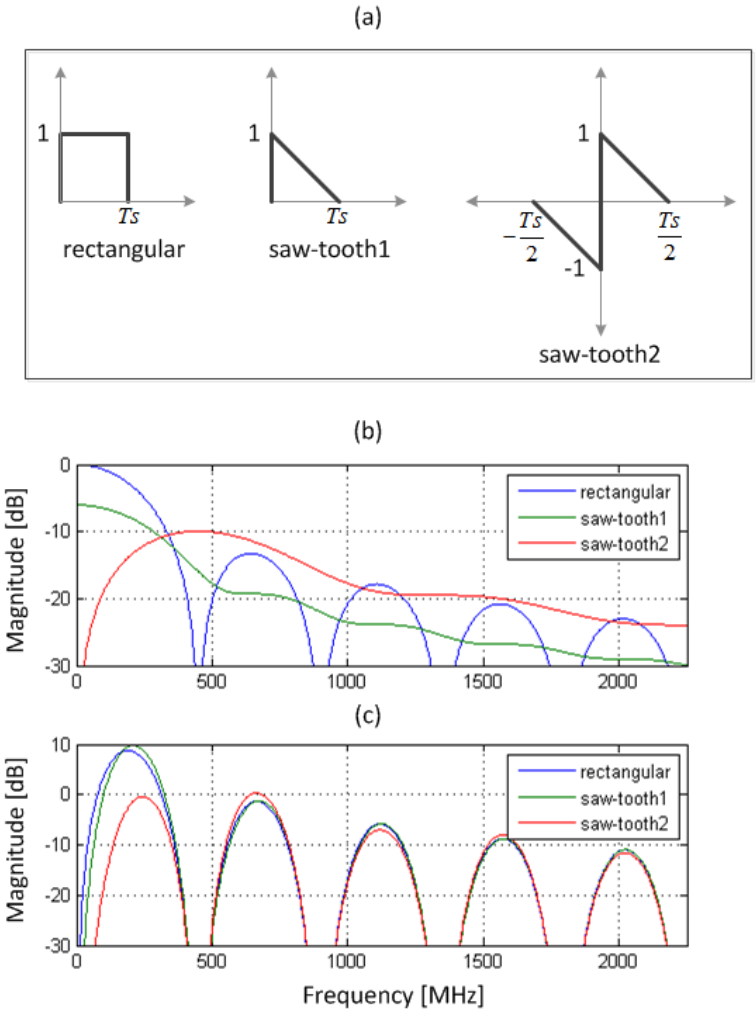

Figure 3.28: (a) Pulse shapes for rectangular, saw-tooth1 and saw-tooth2. (b) Pulse shaping function $\boldsymbol{P_1(f)}$ for rectangular, saw-tooth and modified saw-tooth functions. (c) Calculated transfer function of un-cancelled PQN for the three cases. (Ts = 1/450MHz).

$$P_1(f)_{saw-tooth1}$$

$$= \frac{1}{4\pi^2 f^2 T_s^2}\Big((1 - sinc(\pi f T_s))^2 + 4 \times sinc(\pi f T_s) \sin^2\left(\frac{\pi f T_s}{2}\right)\Big) \quad (3.14)$$

$$P_1(f)_{saw-tooth2} = \frac{4}{4\pi^2 f^2 T_s^2}\big(1 - sinc(\pi f T_s)\big)^2 \quad (3.15)$$

For a 2nd order $\Sigma - \Delta$ modulator quantizing $\phi[n]$, $NTF_1(f)$ is given by:

$$NTF_1(f) = 16 \times \sin^4(\pi f T_s) \quad (3.16)$$

$K_1(f)$, which models the effect of noise-cancellation, for the three cases can be written as:

$$K_1(f)_{rect} = 1 \quad (3.17)$$

$$K_1(f)_{saw-tooth1} = 4 \times \sin^2(\pi f T_s) \quad (3.18)$$

$$K_1(f)_{saw-tooth2} = \frac{4 \times \sin^2(\pi f T_s)}{4} \quad (3.19)$$

Fig. 3.28(b) depicts the pulse shaping functions $P_1(f)_{rect}$, $P_1(f)_{saw-tooth1}$ and $P_1(f)_{saw-tooth2}$. Fig. 3.28(c) depicts the calculated transfer function of un-cancelled PQN $P_1(f) \times NTF_1(f) \times K_1(f)$ for the three cases.

3.5.2 Spectral Images of Phase Ramp

Without loss of generality, the higher harmonics of the fundamental and quantization noise are excluded in the analysis of this subsection. Substituting $\phi[n] + \phi_q[n] = n\Delta\phi$ in (3.1), the expression for DPM output can be written as:

$$y(t) = \sin\left(\omega_C t + \sum_{n=0}^{\infty} p(t - nT_S).n.\Delta\phi\right) \tag{3.20}$$

Eq. 3.20 represents the desired tone at $F_C + \Delta f$ where $\Delta f = F_S\Delta\phi/(2\pi)$. The staircase ramp waveform of $\sum_{n=0}^{\infty} p(t - nT_S).n.\Delta\phi$ in (3.20) is the sum of a desired continuous phase ramp with a slope of $\Delta\omega$ and an error waveform, e(t) (Fig. 3.29(a),(b)) represented by the expression:

$$e(t) = \sum_{n=0}^{\infty} p_0(t - nT_S).\ \Delta\phi \tag{3.21}$$

For a rectangular pulse shape, $p(t)$ for DPM output, the error waveform assumes a saw-tooth pulse shape, $p_0(t)$ with a height of $\Delta\phi$. Using (3.21), (3.20) can be re-written as:

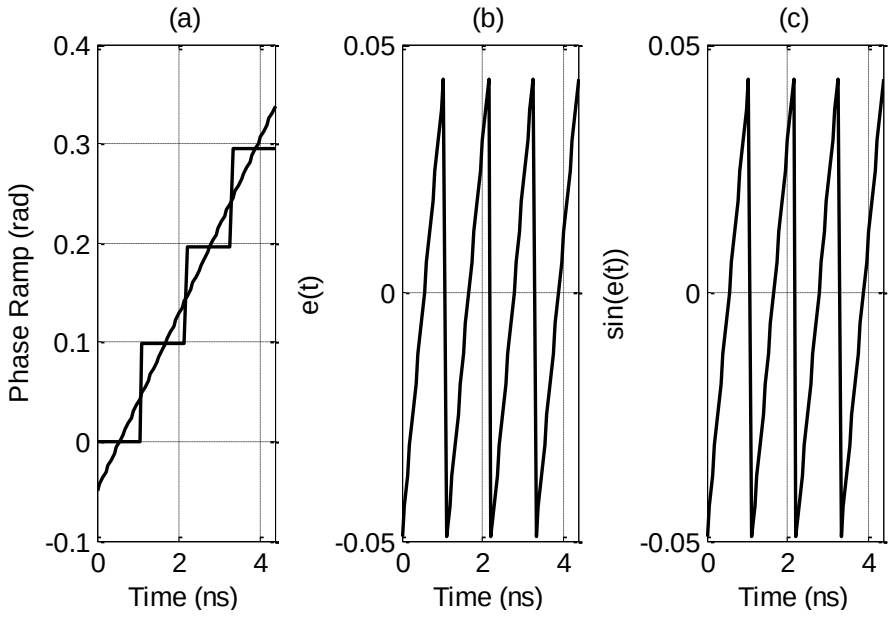

Figure 3.29: Timing diagram of error signal in frequency generation: (a) Phase ramp and continuous time ideal ramp; (b) Error waveform, e(t); and (c) sin(e(t)).

$$y(t) = \sin(\omega_C t + \Delta\omega t + e(t)) \tag{3.22}$$

$$\cong \sin\big((\omega_C + \Delta\omega)t\big) + \cos\big((\omega_C + \Delta\omega)t\big) \cdot \sin\big(e(t)\big) \tag{3.23}$$

Typical waveforms of input phase ramp, e(t) and sin(e(t)) for $\Delta\phi = 0.1$ are depicted in Fig. 3.29. The Fourier series expansion of sin(e(t)), $P_1(t)$ can be written as:

$$P_1(t) = \sum_{n=1}^{\infty} \Bigg((-1)^n \cdot 2sin\frac{\Delta\phi}{2} \cdot \frac{4n\pi}{(\Delta\phi)^2 - (2n\pi)^2} \cdot \sin(2\pi n F_S t) \Bigg) \tag{3.24}$$

$P_1(t)$ has frequency contributions at $F_S,\ 2F_S, 3F_S$ and so on. Clearly, from (3.23) and (3.24), the mixing product of sin(e(t)) with $\cos((\omega_0 + \Delta\omega_0)\, t)$ results in tones at $F_C + \Delta f \pm F_S, F_C + \Delta f \pm 2F_S$, and so on, which form the spectral images at the output. However, the mixing product of the frequency component at $2F_C$ in $P_1(t)$, results in an undesired, close-in tone at $F_C - \Delta f$. This undesired tone can be viewed as an image term about the frequency of reference phase at F_C. The magnitude of the image tone, for $\Delta\phi \ll 2\pi$, is approximated by:

$$P_{fund} - P_{imag} \cong 20 \times \log_{10}(\frac{\Delta\phi}{2k\pi}) \tag{3.25}$$

where $k = 2F_C/F_S$, and P_{fund} and P_{imag} are strengths of the fundamental output and image tone, respectively.

3.5.3 Harmonic Mixing of RF Carrier Harmonics and Phase Ramp

Extending (3.20) to include the third harmonic of the reference input, the expression for phase modulator output can be written as:

$$y(t) = \sin\left(\omega_0 t + \sum_{n=0}^{\infty} p(t - nT_S).n.\Delta\phi\right) + \alpha_3 \sin\left(3\omega_0 t + \sum_{n=0}^{\infty} p(t - nT_S).n.3\Delta\phi\right) \quad (3.26)$$

where α_3 is the magnitude of third harmonic relative to fundamental. It should be noted that the phase modulation term in (3.26) for the 3rd harmonic ($3\Delta\phi$) is three time the phase modulation term in the fundamental ($\Delta\phi$). The factor of 3 arises due to the fact that phase modulator has a constant time delay leading to proportionally higher phase delay as frequency increases. As a result of this, the generated frequency for the 3rd harmonic lies at three times the offset frequency, Δf for the fundamental tone. Since the spectral images of the signal created by the 3rd harmonic are also present at all multiples of $F_S$and on both the upper sidebands and the lower sidebands, one of the spectral image of the lower sideband falls close to the fundamental output at $F_C + \Delta f$. However, since the offset frequency is three times for the third harmonic, it is present at 3x offset from the phase reference frequency, i.e., at $F_C \pm 3\Delta f$. Similar to the spectral images of fundamental, the spectral images of the 3rd harmonic of the RF carrier are filtered by sinc(x). For $k = 2F_C/F_S$ and rectangular pulse shaping of phase modulator output, the two side bands of the 3x offset tone can be expressed by:

$$P_{fund} - P_{3x} = 20 \times \log_{10}\left(\alpha_3 sinc\left(k \pm \frac{3\Delta\omega}{2\pi F_S}\right)\right) \quad (3.27)$$

where P_{3x} is the strength of the tone at $F_C \pm 3\Delta f$.

Chapter 4

Digital Calibration of Phase Modulator

This chapter starts with a discussion on the issues with prior art on linearity improvement techniques. It then describes the proposed digital calibration method for the estimation and correction of phase errors. The signal processing details of the proposed method and the performance bounds of the proposed method are subsequently discussed.

4.1 PRIOR ART ON PHASE MODULATOR LINEARITY IMPROVEMENT

In this section, we discuss the prior art of methods to improve phase linearity of a phase modulator, and their advantages and limitations.

4.1.1 Phase Interpolation with Low Offset Reference Phases

In [2], non-linearity was moderately reduced by using two stages of interpolation (Fig. 4.1) and applying systematic pre-distortion. However, the accuracy of this type of systematic correction worsens in the presence of higher order harmonics of the RF carrier. The approach is also power hungry as the number of additional stages increases exponentially as interpolation depth is increased. Besides this, the mismatch errors are not addressed in this approach.

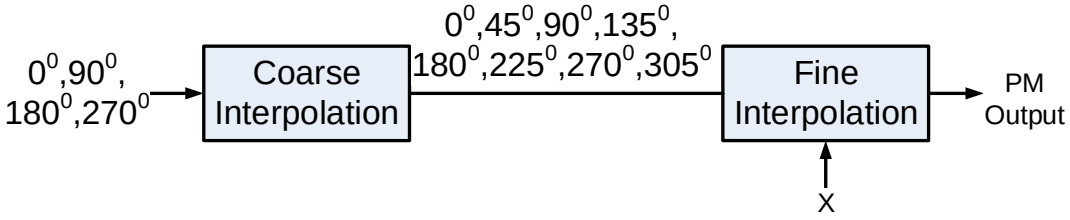

Figure 4.1: Two stage phase interpolation [2]

4.1.2 LC Filtering of LO Input

In [5], the linearity and the effective resolution were improved by band-pass filtering the phase interpolator inputs (Fig. 4.2). The filter helps in removing the higher harmonics of the LO, as these harmonics contribute to phase errors. However, the band-pass filters employ inductors that make it unattractive to applications that need multiple open loop modulators. Furthermore, this approach requires a tunable filter to accommodate changes in carrier frequency and/or redesign of the filter for a change in process node. The errors due to component mismatch are not addressed, in this work, also.

4.1.3 Digital Pre-distortion

Irrespective of the kind of phase modulator circuit employed (phase interpolator or delay line based), digital calibration is generally essential to achieve high resolution, particularly in the face of random circuit mismatches. For digitally controlled delay lines,

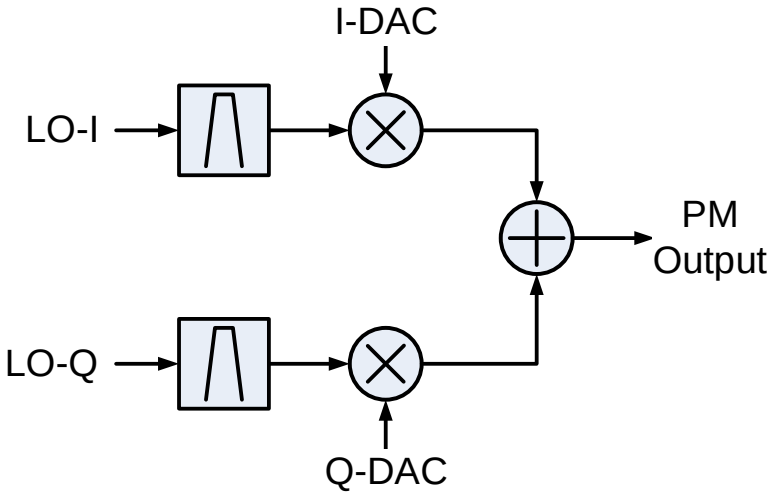

Figure 4.2: LC filtering of LO input [5]

[4] had devised a calibration method based on measuring the frequency of a ring-oscillator formed with the delay line PM (Fig. 4.3). However, the extension of such method to phase interpolator based phase modulator results in a complex oscillator topology, which requires careful design.

In this work, a low-power, low-area and digital technique is proposed to estimate both systematic non-linearity and random errors caused by mismatches. Subsequently, those errors are compensated in the digital domain using a look-up table based pre-distortion.

4.2 PROPOSED NON-LINEARITY CALIBRATION TECHNIQUE

4.2.1 Proposed Technique: Concept

The proposed technique employs a high precision on-chip system for measuring the phase errors of the phase modulator during an initial calibration period. Subsequently,

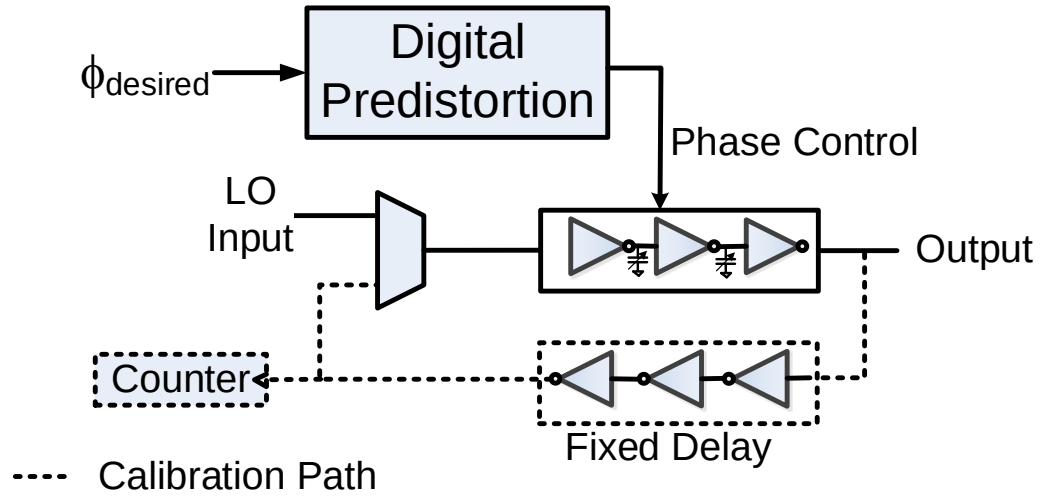

Figure 4.3: Estimation of phase errors in [4]

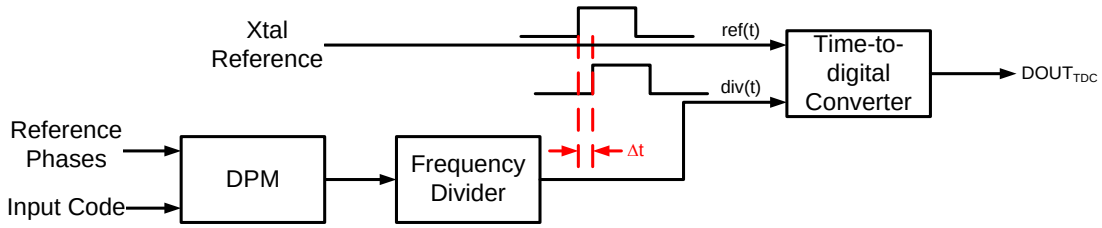

Figure 4.4: Conceptual diagram of the proposed technique

pre-distortion is applied to modulated data, by populating a look-up table based on the measured phase errors. This pre-distortion can correct for non-linearity due to both circuit transfer function and mismatch. Furthermore, it will be shown in section 4.2.2.3 that the performance degradation due to temperature variation is not significant.

Conceptually, the output of DPM is divided down and compared to a clean reference source using a TDC, as depicted in Fig. 4.4. In the actual implementation, we re-used the feedback divider and the TDC of a digital PLL for this purpose, resulting in savings in chip-area.

Fig. 4.5 shows a block diagram of implementation of the proposed technique. During normal operation, the multiplexer control *cal_en* is set to '0', and the system behaves simply like a digital PLL followed by one or more open loop phase modulators. Note that the "div-by-2" block generates the necessary quadrature phases for the phase modulators, DPM1, DPM2, etc. During calibration, a particular phase modulator that needs to be calibrated is included in the PLL loop by setting *cal_en* to '1'. Note that the fractional division ratio, N_{SD}, is adjusted accordingly to account for the division by 2 following the VCO.

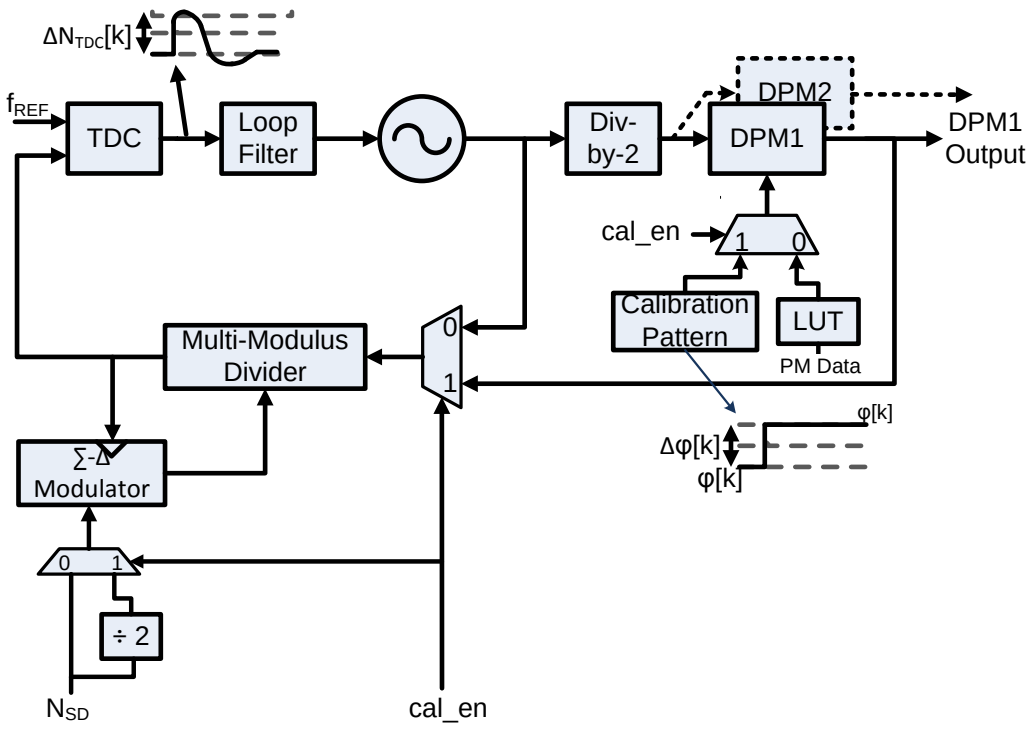

Figure 4.5: Block diagram of DPM calibration

With the DPM1 output phase locked to the PLL reference, if a phase disturbance ($\Delta\Phi$) is introduced by changing the digital control code of the modulator (n1 → n2), the wideband path between DPM1 and the TDC will respond with a step that eventually dies out according to the PLL bandwidth as shown in Fig. 4.9.; Fig. 4.6 also shows the simulated TDC output for a phase jump. The height of the TDC output step is proportional to the phase disturbance, $\Delta\Phi$. So, the digital output of the TDC is recorded before it starts to die out.

Since, the raw TDC resolution is, in general, not sufficient to measure very fine phase errors e.g., in the sub-ps range, averaging is employed. Specifically, the locked PLL is disturbed several times by the same phase disturbance ($\Delta\Phi$) and TDC output step

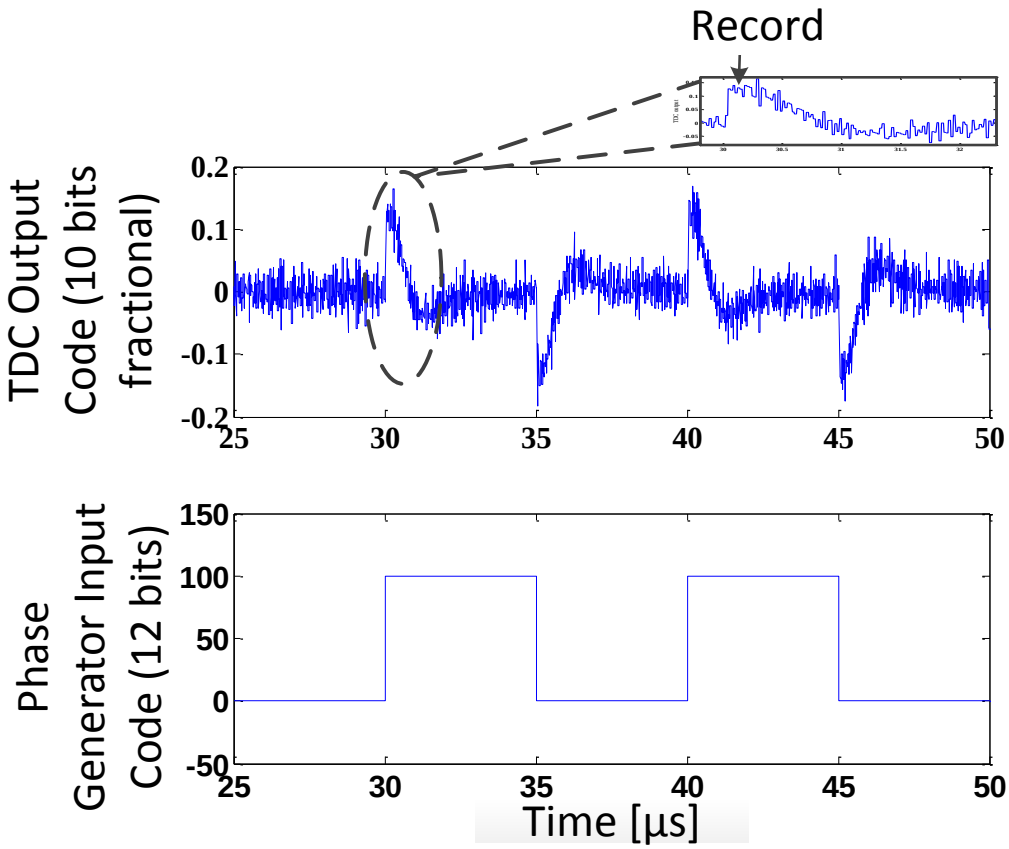

Figure 4.6: Timing diagram of DPM calibration

height recorded each time, and the recordings averaged (see Section 4.2.2.1 for more details). The averaging process is re-started with a new set of input codes for DPM1. If the averaged output step responses for all sets of input codes, appropriately chosen to span the DPM input range, are combined, the overall phase modulator transfer function can be calculated. Finally, an LUT is generated based on measured errors and the input data is continuously pre-distorted in accordance with the LUT.

The process can be repeated for multiple other phase modulators (like DPM2 in Fig. 4.5) using the same digital PLL. It should be noted that TDC non-linearity doesn't

play a significant role in this technique, as the phase steps, at its input, are relatively constant. Additionally, the technique is equally applicable for any other PM topology, including delay line based PM.

4.2.2 Proposed Technique: Design Considerations

In this section, we investigate the performance bounds and other key features of the proposed technique.

4.2.2.1 Averaging and Residual Noise

The height of TDC output step, $\Delta N_{TDC}[k]$ in the k-th iteration of phase measurement, for a phase step of $\Delta\phi$ applied to PM modulator is:

$$\Delta N_{TDC}[k] = N_{TDC,p}[k] - N_{TDC,s}[k] \tag{4.1}$$

where $N_{TDC,s}[k]$ and $N_{TDC,p}[k]$ are the TDC outputs at the *start* and at the *peak* of the TDC output step response:

$$N_{TDC,s}[k] = Q(\alpha\phi_s[k]) = \alpha\phi_s[k] + t_{q,s}[k] \tag{4.2}$$

$$\begin{aligned} N_{TDC,p}[k] &= Q\big(\alpha\phi_p[k] + \Delta\phi\big) \\ &= \alpha\big(\phi_p[k] + \Delta\phi\big) + t_{q,p}[k] \end{aligned} \tag{4.3}$$

where α is the TDC gain, $\phi[k]$ is the relative phase between the TDC inputs in the absence of the phase jump, $\Delta\phi$, $Q(.)$ represents the TDC's quantization operation, $t_q[k]$ is the quantization error, and (s, p) are subscripts denoting *start* and *peak* instants respectively. Effectively,

$$\Delta N_{TDC}[k] = \alpha\Delta\phi + \alpha\phi_p[k] - \alpha\phi_s[k] + t_{q,p}[k] - t_{q,s}[k] \tag{4.4}$$

The terms $\phi_s[k]$ and $\phi_p[k]$ are due to: (a) instantaneous phase errors in the fractional-N PLL resulting from the ΔΣ modulator quantization noise, and (b) reference and circuit noise. Since phase measurements are conducted at a rate much lower than even the PLL's bandwidth[1], it is reasonable to assume that $\alpha\phi_s[k]$ and $\alpha\phi_p[k]$ are zero-mean, white sequences, each with a variance of:

$$t_{PLL}^2 = t_{\Delta\Sigma}^2 + t_{INT}^2 \tag{4.5}$$

where t_{INT} is the r.m.s. jitter in the PLL output when operating in integer-N mode and $t_{\Delta\Sigma}$ is the r.m.s. value of the instantaneous time error at the TDC input due to ΔΣ modulator quantization noise. Note that t_{PLL} usually spans several TDC quantization steps, particularly when the PLL is operating in fractional-N mode.

Now, consider the TDC quantization errors. Since $\phi_s[k]$ and $\phi_p[k]$ are zero-mean random variables that span several TDC quantization steps, it follows that the TDC quantization errors, $t_{q,s}[k]$ and $t_{q,p}[k]$, are also zero-mean, white sequences, each with a variance of:

$$t_{\mathrm{q}}^2 = \frac{T_{res}^2}{12} \; or \; \frac{2T_{res}^2}{12} \tag{4.6}$$

depending on whether a simple or a GRO based TDC are employed and where T_{res} is the nominal TDC quantization step. Random mismatch errors in the TDC can also be included and similarly modeled as zero-mean, white sequences, with a variance of t_{mis}^2.

[1] After all, for each measurement, one has to wait for the PLL to "remove" the introduced the phase jump, Δφ.

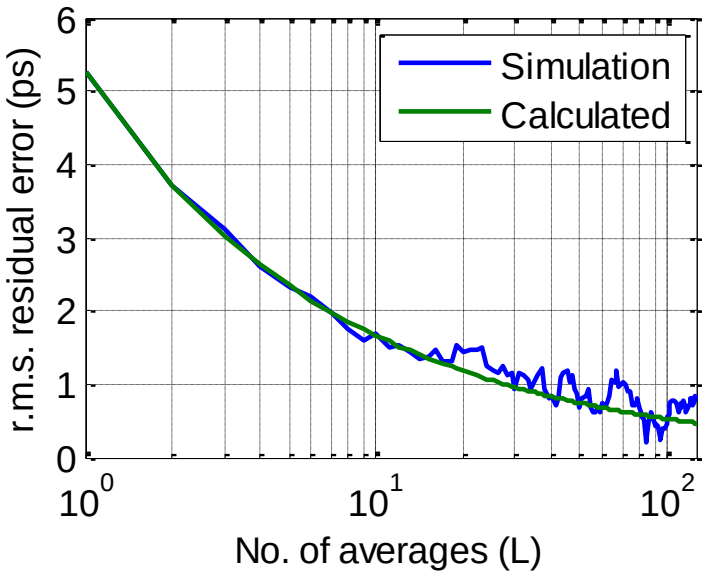

Figure 4.7: Residual noise of phase measurement, t_{err} vs. number of averages, L

Since all the error terms in $\Delta N_{TDC}[k]$ are white and zero-mean, averaging $\Delta N_{TDC}[k]$ significantly improves the phase measurement accuracy. For L averages, it can be shown that the residual error in phase measurement has an r.m.s. value of:

$$t_{err}(L) = \sqrt{\frac{2}{L}\left(t_{\Delta\Sigma}^2 + t_{INT}^2 + t_{\mathrm{q}}^2 + t_{\mathrm{mis}}^2\right)} \tag{4.6}$$

The number of averages, L, can be chosen to get to a target acceptable measurement error, t_{err}. In Fig. 4.7, the residual error in integer-N mode is plotted as a function of L. The TDC mismatch error is 15% in these simulations.

Note that, while desired measurement accuracy can be achieved even in fractional-*N* mode, it is preferable to perform the phase calibration in integer-*N* mode so that L and hence, the calibration time, can be low. To illustrate, note that, for a well-dithered, *K-th* order ΔΣ fractional-*N* PLL,

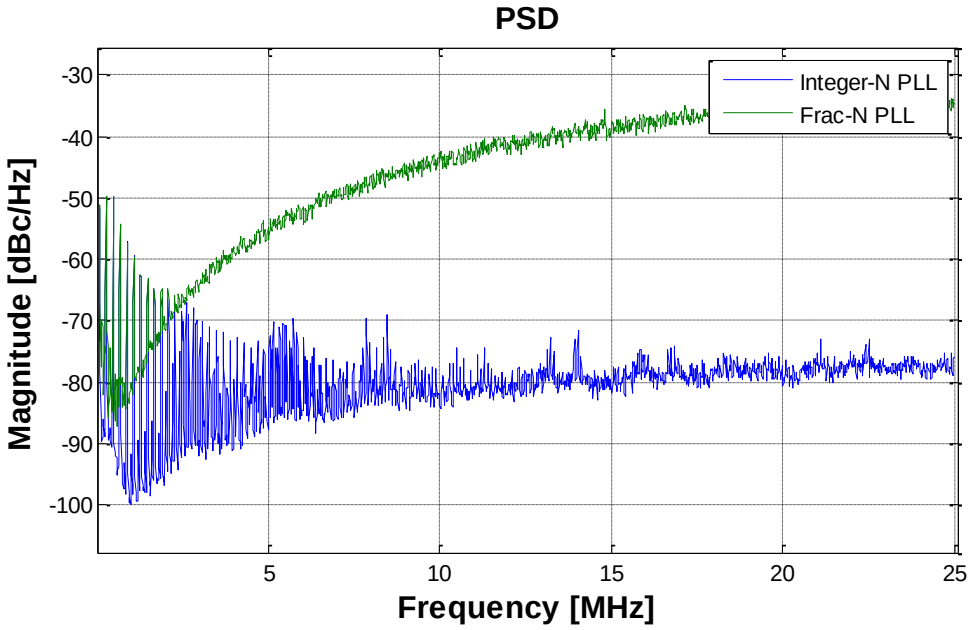

Figure 4.8: Power spectral density of TDC output during calibration in integer-N mode and fractional-N mode

$$t_{\Delta\Sigma}^2 = 2^{K-1}\frac{T_{VCO}^2}{12} \tag{4.7}$$

where T_{VCO} is the period of the VCO. For example, for a 3rd order ΔΣ fractional-*N* PLL, $t_{\Delta\Sigma} = T_{VCO}/\sqrt{3}$ ~320ps for a 1.8 GHz PLL. Fig. 4.8 illustrates this strong, additional ΔΣ noise at TDC output (note that the calibration tone at low-frequency in the spectrum are constant in the two modes). So to get sub-ps accuracy in phase measurement in a fractional-N PLL, $L > 10^6$ may be needed!

In integer-*N* mode, t_{PLL} is very small thereby allowing calibration with only a few averages. For example, sub-ps r.m.s. jitter is not uncommon in PLLs used in wireless communications. However, if t_{PLL} is lower than the TDC quantization noise step, the TDC quantization errors may be correlated. This can happen when a simple TDC such as

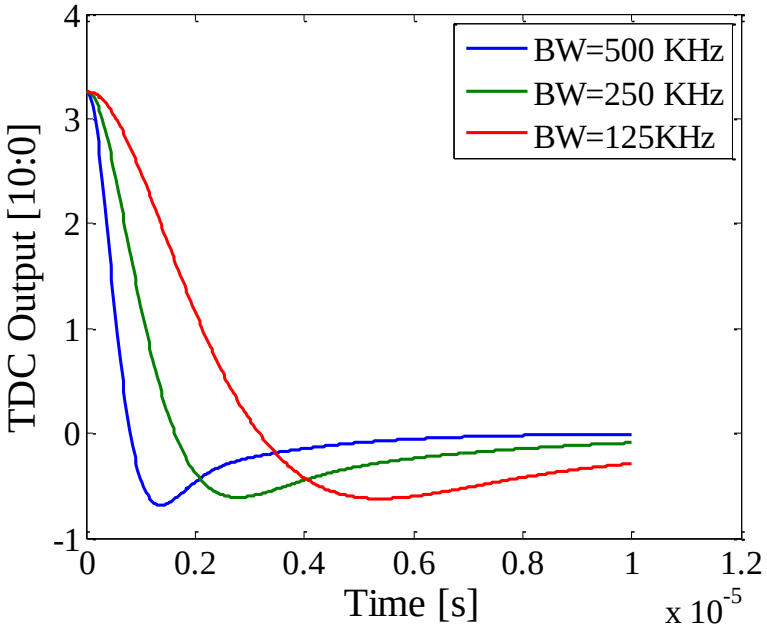

Figure 4.9: Step response from DPM input to TDC output as a function of PLL loop bandwidth

inverter-based TDC is employed. However, a GRO based TDC, will ensure that the TDC quantization errors will be uncorrelated even when t_{PLL} is very small.

4.2.2.2 Calibration Speed

The PLL loop dynamic dictates the rate at which the cycle of phase error measurement can be restarted for the collection of multiple data points. Fig. 4.9 depicts the step response from DPM input to TDC output as a function PLL loop bandwidth. Specifically, after a phase disturbance of $\Delta\phi$ is introduced (going from code n1 to code n2), enough time needs to elapse for the disturbance to die out. Furthermore, an equal but opposite phase disturbance, $-\Delta\phi$, must be applied to return the PM to the original code, n1, so that the experiments are nominally replicated. So, low PLL bandwidth results in a

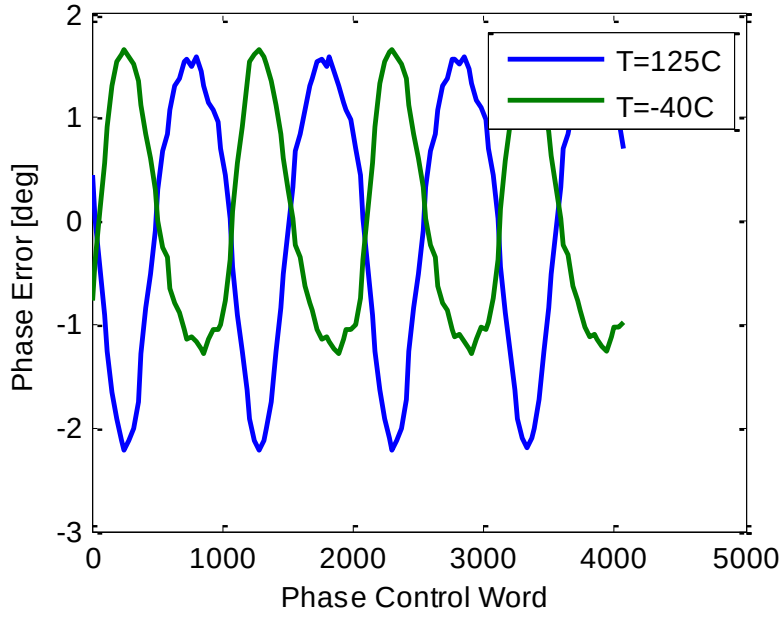

Figure 4.10: Simulated phase error at 125C and -40C

slow settling response, which, in turn, results in slower calibration speed. However, this also results in a longer time for which the TDC output stays flat, thereby, providing a wider window for recording TDC data.

4.2.2.3 Temperature Sensitivity

Since the proposed approach is not a background calibration approach, it is important to consider the effect of temperature variation on the code-phase transfer function of the phase modulator.

Note that phase errors caused by random mismatches do not change much with temperature. However, systematic errors do change with temperature primarily because of trans-conductance and capacitance sensitivity to temperature. Fig. 4.10 depicts the simulated phase errors over temperature variation from -40°C to 125°C, while using the

same look-up table generated with room temperature simulations. The approximately ±1% phase error can limit the phase modulator to less than 7 bits. However, simulated EVM and out-of-band emission performance degradation for GFSK modulation, over this temperature variation is less than 3 dB. This was deemed sufficient for the target prototype IC described in Chapter 5.

Note that, since the temperature sensitivity is not expected to change from chip-to-chip, if needed, a temperature dependent phase correction could be included in the digital pre-distortion design. A coarse on-chip temperature sensor is the only required extra circuit component for this enhancement.

4.2.2.4 Dynamic Errors

The proposed calibration approach measures the static errors in the phase modulator, primarily caused by circuit non-linearity and component mismatch. The dynamic errors due to: (a) supply noise; (b) digital switching; and (c) bandwidth of the phase modulator, can become significant as the RF signal bandwidth is increased.

The impact of supply noise can be suppressed by the use of differential circuits for all stages of the phase modulator. The phase interpolator based phase modulator has a clear benefit in this regard. Additionally, since the analog power and ground can be relatively far from the digital power and ground, it is very crucial to have both $data$ and $\overline{data}$ at the digital domain crossing between the analog and digital circuits. The differential digital data ensures that the return current from the interface is greatly minimized, thereby, suppressing the ground bounce.

Secondly, errors in the phase switching clock originate from — variations in $t_{ck\text{-}2\text{-}q}$ of flip-flops driving the unit cells of the phase modulator; clock jitter and systematic variation in the clock edge arriving at each flip-flop due to layout mismatches. The $t_{ck\text{-}2\text{-}q}$ varies as, for instance, the capacitive loading on flip-flops for MSB can be different from the capacitive loading on LSB. In this work, dummy mos capacitors are used to equalize the loading on all the data bits. Systematic variation on the clock edge due to layout parasitics on the clock route pose another challenge in a high resolution phase modulator and can become significant at high switching frequency. The clock routing was optimized to minimize this variation and the approach is discussed in Chapter 5. Spectre simulations including layout parasitics, show negligible impact on performance due to errors in phase switching circuitry.

Thirdly, errors due to an in-complete settling of the phase modulator can also lead to phase errors in the output signal. However, since the phase interpolator is designed for a bandwidth greater than the RF carrier frequency and the RF phase bandwidth is, in most applications, much lower in bandwidth than the carrier frequency, the performance impact due to settling time was quite low. This error can be modelled by a low pass transfer function in the phase modulator input. Fig. 4.11 shows the DPM output phase when the non-ideal phase switching pulse response is included in a behavioral simulation.

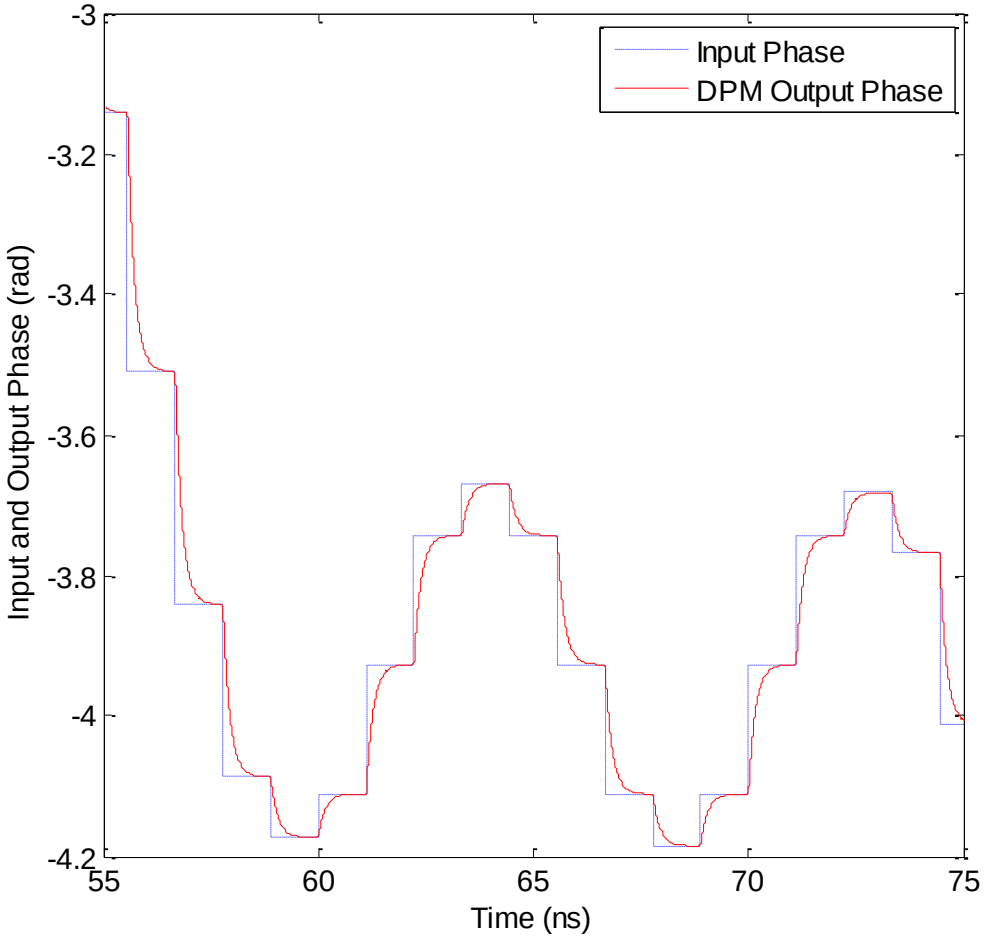

Figure 4.11: Behavioral simulation depicting transient phase response of DPM output due to non-ideal phase switching pulse response

Chapter 5

Phase Modulator Circuit Design and Measurement Results

In this chapter, we discuss the design of circuit components required to realize the phase modulator and the calibration circuits. A proto-type IC was fabricated in 0.13 um IBM CMOS process. The measurments results of the proto-type are discussed and compared with the recent state-of-the-art in phase modulator and clock generator design.

5.1 CIRCUIT DESIGN

A 1.8-GHz wide bandwidth open-loop phase modulator based on the proposed calibration technique was designed to provide proof of concept. A 2x VCO running at 3.6 GHz followed by a divide-by-2 circuit generates quadrature reference phases at 1.8 GHz. As described later, the prototype IC allows for demonstrating the feasibility of both a wide bandwidth phase modualtor and a high resolution frequency synthesizer.

5.1.1 Phase Generator Design

The phase interpolator based phase generator is shown in Fig. 5.1. The reference phases for the phase interpolator are derived from the outputs of a divide-by-two circuit driven by VCO buffers. The output phase range 360^0 was obtained by interpolation in four quadrants of 0^0 and 90^0; 90^0 and 180^0; 180^0 and 270^0 and 270^0 and 0^0. The interpolation is carried out in a single stage, by controlling the weights of each reference phase by a 10 bit digital control for each phase. The control bits are derived from a 12 bit DPM control code, where the two MSBs represent the quadrant of operation. The remaining 10 bits are decoded into a 4 bit thermometer control and a 6 bit binary weighted control for the two phases which are active in that quadrant. The digital data

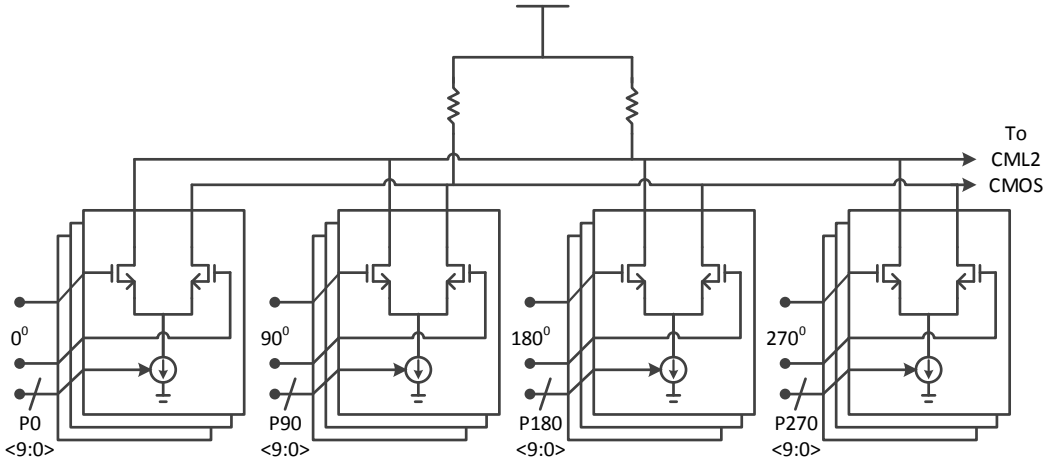

Figure 5.1: Phase generator architecture

was received inside the phase modulator by high speed dynamic flip-flops, driven by a low-jitter clock.

5.1.1.1 Digital Data Interface

Careful design of the interface between the digital data driving the DPM and the analog blocks of the DPM is required to ensure no performance degradation occurs due to the sources of dynamic errors. Some of the major sources of these errors are variation in the $t_{ck\text{-}2\text{-}q}$ of flip-flops between each data line, ground bounce, clock jitter and errors due to clock routing. $t_{ck\text{-}2\text{-}q}$ was equalized between all the digital data lines by adding dummy capacitors on data lines which drive smaller mos devices of the phase interpolator. Additionally, the wiring parasitic at the output of all the flip-flops are matched by using a single array of flip-flops and unit-cells of the phase interpolator. The single row of

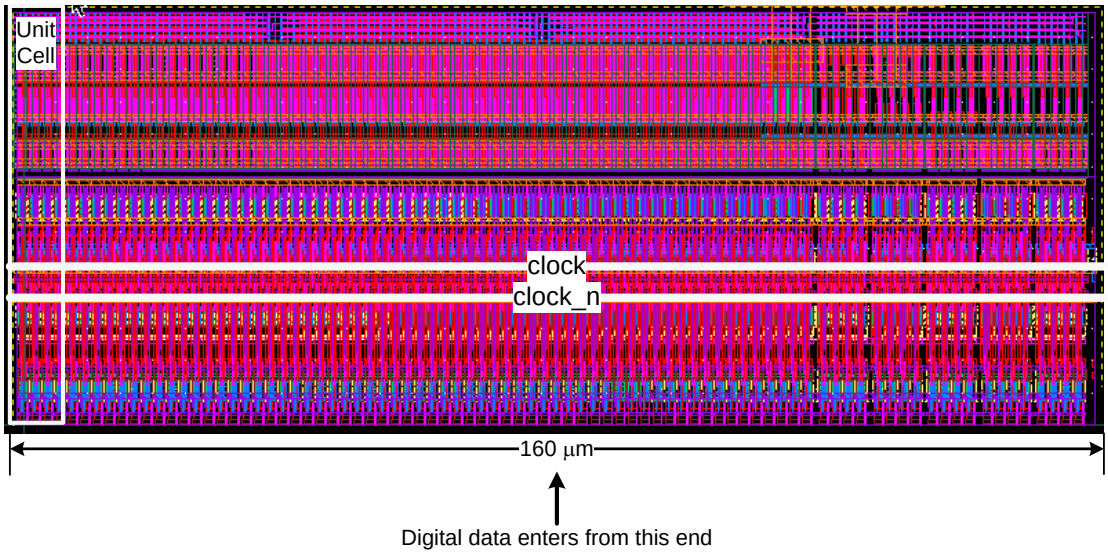

Figure 5.2: Phase generator layout showing arrangement of layout cells and digital data interface

devices also helps in minimizing the wiring parasitic on the clock route (Fig. 5.2). The wiring parasitic on the clock route is further minimized by utilizing the top thick metal of the process, which yields the minimum parasitic capacitance and resistance. The short clock route ensured that the wire delay from one end of the clock route to the other end was negligible. Finally, in order to minimize, ground bounce at the interface, only complementary data lines are used at the interface. By doing so, the ground return current is significantly reduced, thereby, reducing ground bounce.

5.1.2 Digital PLL

The digital PLL used in this design is discussed in [6], and includes a noise shaping TDC with a quantization step size of 6 ps. The closed loop bandwidth of the PLL is 500 KHz and the corresponding low-pass filtering provided by the PLL reduces the

TDC contribution to PLL's output jitter, to less than 100 fs. As such, noise shaping of the TDC quantization error is very effective in reducing the impact of this noise on the PLL output. However, for the calibration approach proposed here, the more important property of the TDC is that it scrambles the quantization noise so that averaging of measurements leads to a reduction in error as discussed in Chapter 4.

5.1.3 Reference Phase Buffer Design

The load of the phase interpolators and the associated wiring parasitics is large enough to impact the frequency divider performance; therefore, low-power voltage buffers are used to drive the phase interpolators. An analog complementary mos buffer topology was chosen, that has a better signal driving capability than nmos or pmos only buffer (Fig. 5.3). In this topology, a combination of nmos and pmos source followers is used to increase the bandwidth of the voltage buffer. We can get an estimate of the improvement by comparing the bandwidth of the complementary buffer, with that of an nmos source follower. The bandwidth of an nmos source follower is given by:

$$BW_{nmos} = \frac{g_{m,NMOS}}{2\pi(C_{LOAD} + C_{NMOS} + C_{BIAS})} \tag{5.1}$$

where $g_{m,NMOS}$ is transconductance of nmos device, C_{LOAD} is total load on the source follower, C_{NMOS} is the total capacitance contributed by nmos device and C_{BIAS} is the total capacitance contributed by the biasing device. For a complementary mos buffer, the circuit bandwidth, BW_{comp} at fixed current, can be expressed as:

$$BW_{comp} = \frac{g_{m,NMOS} + g_{m,PMOS}}{2\pi(C_{LOAD} + C_{NMOS} + C_{PMOS})} \tag{5.2}$$

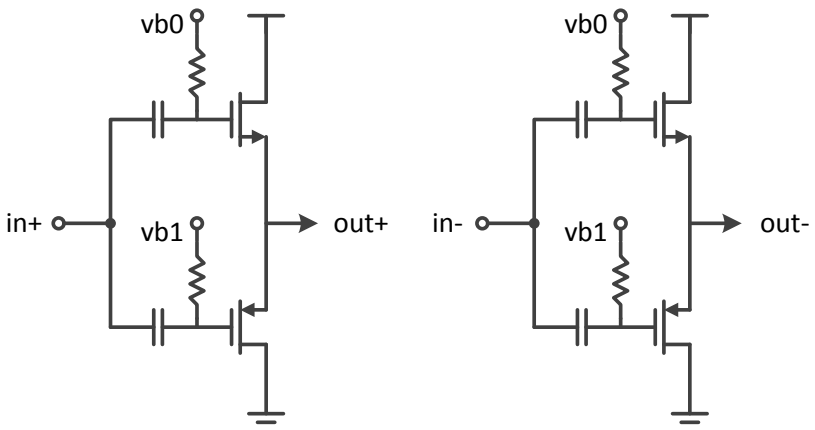

Figure 5.3: Analog complementary MOS voltage buffer

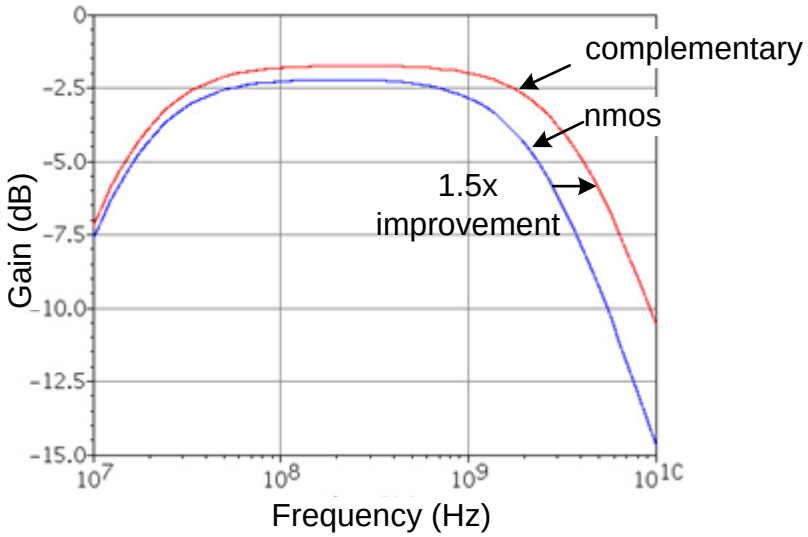

Figure 5.4: Bandwidth comparison of complementary buffer with nmos source follower

where $g_{m,PMOS}$ is transconductance of the PMOS devices and C_{BIAS} is the capacitance contributed the PMOS device. Although, the total load capacitance can increase if $C_{PMOS} > C_{BIAS}$, the combined power consumption of the frequency divider and the voltage buffer is still lowered. The bandwidth enhancement obtained in this design is

50% over a NMOS source follower (Fig. 5.4). The input signal is ac-coupled so that the nmos and pmos are independently biased. The output signal swing of the phase buffer was restrained to 600 mV peak-to-peak differential, as any larger voltage swing suffers from degradation in power supply-rejection.

5.1.4 CML-to-CMOS Design

Fig. 5.5 shows the CML-to-CMOS converter circuit. Its design is complicated by the fact that the phase interpolator output exhibits a variable amplitude that is dependent on the interpolation code. For example, if two input reference phases with an offset of 90^0 are linearly interpolated, the output amplitude modulation, y_{amp} is represented by:

$$y_{amp} = \sqrt{x^2 + (1-x)^2} \tag{5.3}$$

where x and $(1-x)$ are the weights applied to the two interpolating reference phases.

The CML-to-CMOS converter will translate this undesired "amplitude modulation" into an additional code-dependent, non-linear, phase error. In this design, the non-linear phase error is accounted for by calibrating the CMOS output (rather than the CML signals).

The undesired "amplitude modulation" will also induce a code-dependent duty cycle error in the CMOS output. Fig. 5.6 depicts the simulated duty cycle modulation observed in this design, as a function of the phase code. Although, the rising edge of the phase modulator output is compensated for phase errors by the look-up table, the errors in

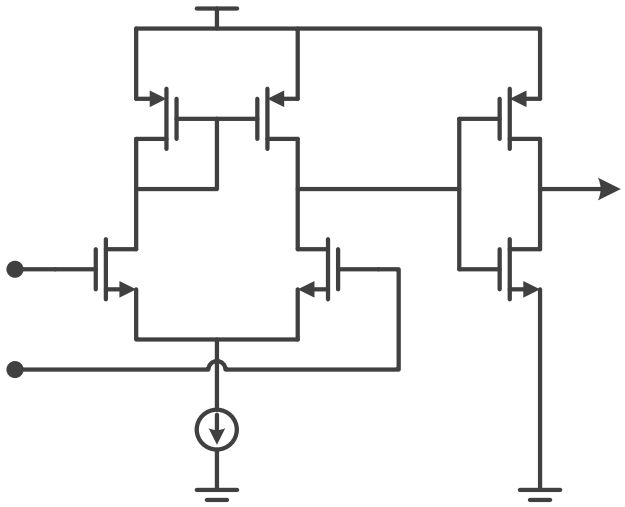

Figure 5.5: CML-to-CMOS circuit

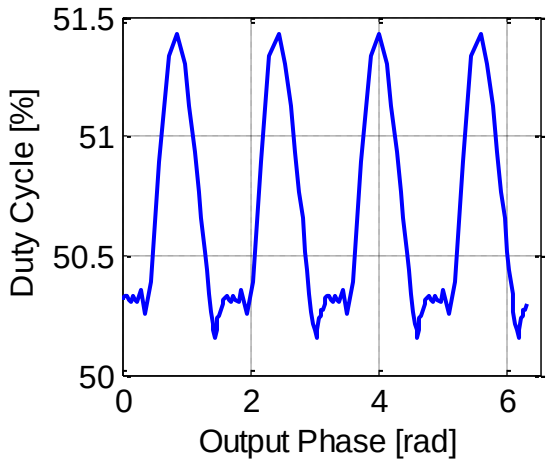

Figure 5.6: Simulated output duty cycle vs output phase

the falling edge due to duty cycle modulation pass through uncorrected. This error is not particularly problematic when generating an angle modulated signal. However, in frequency synthesis, strong spurs can be seen, as described in the measurements section.

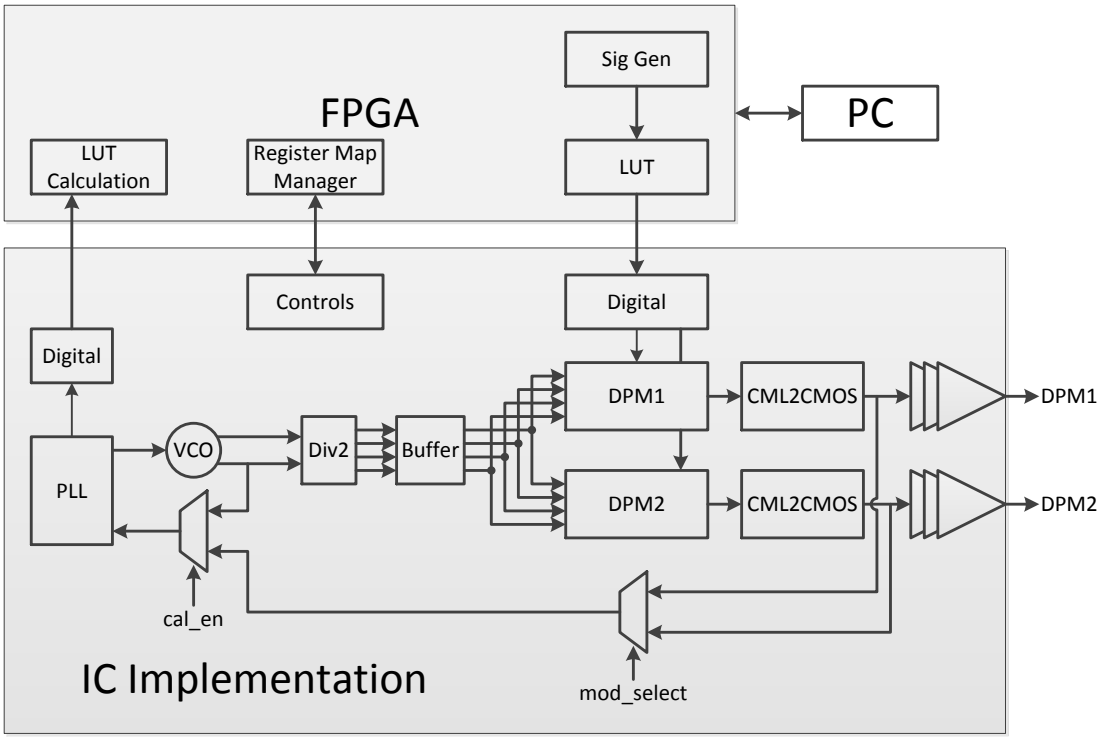

Figure 5.7: System architecture of phase modulator

5.1.5 System Design

The prototype-IC implements two phase modulators as proof-of-concept of multiple output phase modulation and frequency generation. The overall architecture is depicted in Fig. 5.7. The PLL and frequency divider are shared by the two DPMs and the number of phase modulators can be extended by increasing the driving strength of the voltage buffer. The output of CML2CMOS connected to the phase modulators can be connected to the feedback path of the PLL during calibration. Either of the phase modulators is selected by the control signal *'mod_select'* for digital calibration. To demonstrate the capabilities of the technique, the IC can be configured as: (a) a phase modulator, (b) an outphasing transmitter, and (c) a frequency generator. For phase

modulation and frequency generation, the measurement was performed on one of the phase modulator. For measurements on outphasing transmitter, the outputs of both the DPMs were combined off-chip to generate the final output for measurement.

The modulation data for all the applications were generated on a FPGA. The look-up table coefficients for digital pre-distortion were also stored on the FPGA. Before sending the signal to the board, the data was serialized by 4-to-1 ratio on the FPGA and then transmitted via LVDS drivers present on the FPGA. The link was running at 1.8 Gbps and the on-chip LVDS receivers deserialized the data to 450 Mbps before applying to the phase modulator. The digital spectral images were pushed to 900 MHz offset from the RF signal by upsampling the data to 900 Mbps on-chip via linear interpolation.

5.2 MEASUREMENT RESULTS

5.2.1 Measurement Setup

The prototype IC was realized in 0.13 μm IBM CMOS process, with a core voltage of 1.5V (die photo in Fig. 5.9). The chip has two independent phase modulators sharing a common PLL and the reference phases. The total power consumed by each DPM is 11.3 mW in the analog domain and 6.7 mW in the digital domain. The breakdown of power consumption by each block of the phase modulator is depicted in Table 5.1. The total power consumption of the PLL is 50 mW. The measurement setup is depicted in Fig. 5.8. The reference frequencies for the PLL , FPGA and the on-chip clock

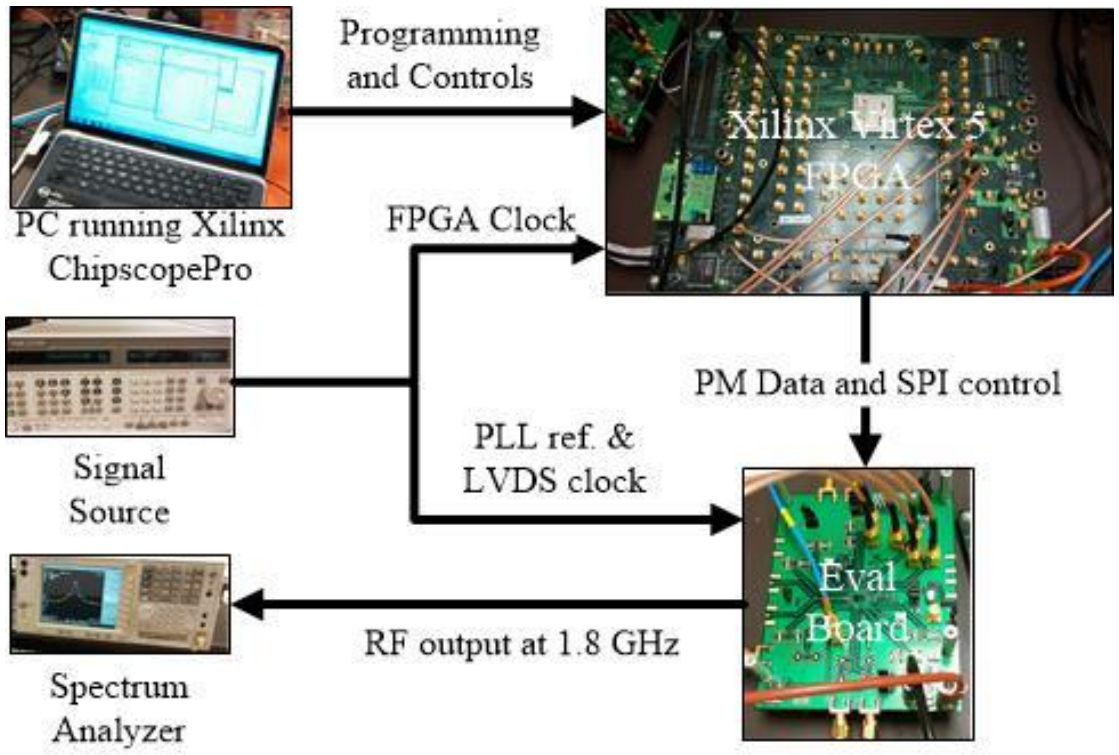

Figure 5.8: Measurement setup

receiver for LVDS data were provided externally through synchronized signal sources. Modulator input data generation and digital pre-distortion was done off-chip on a Xilinx Virtex 5 FPGA. The 12 bit output for each modulator from the FPGA was connected through LVDS transmitters after 4-to-1 serialization. The TDC output was recorded after on-chip serialization by the LVDS receivers of the FPGA board. Fig. 5.10 depicts the look-up table generated from the measured DPM transfer function. The LUT was limited to 9 bits on the FPGA and the measured phase characteristic after pre-distortion is plotted in Fig. 5.11.

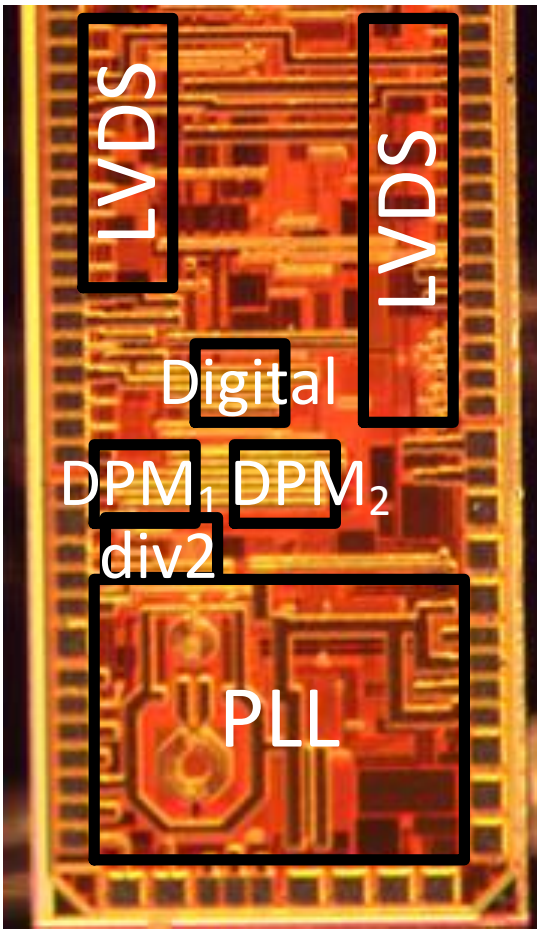

Figure 5.9: Die photo

5.2.2 GFSK Modulated Data

The measurement results of the phase modulator when transmitting GFSK modulated data is shown in Fig. 5.12-5.15 The out-of-band emission of the standalone phase modulator for 20 Mb/s GFSK is an excellent -56 dB, with an r.m.s. phase error of only 3.2%. The phase modulator also shows excellent wideband performance, shown in Fig. 5.13. Table 5.2 presents a comparison with the recent prior art on RF phase modulators ([1] and [2]), polar([5]) and outphasing transmitters([3] and [4]). As evident,

this work represents better performance and/or lower power consumption than all prior art except for [5]. Note that while [5] consumes lower power, it is built in a much finer process node. Furthermore, this work does not require inductors in the phase modulators and as a result, occupies a smaller die area.

Table 5.1: Breakdown Of Power Consumption By Each Block

Block	Power [mW]
Frequency Divider	2.6
Voltage Buffer	2.0
Phase Interpolator	5.7
CML2CMOS	0.9
Output Buffer	8.4
Digital	6.7
Total (excluding output buffer)	18.0

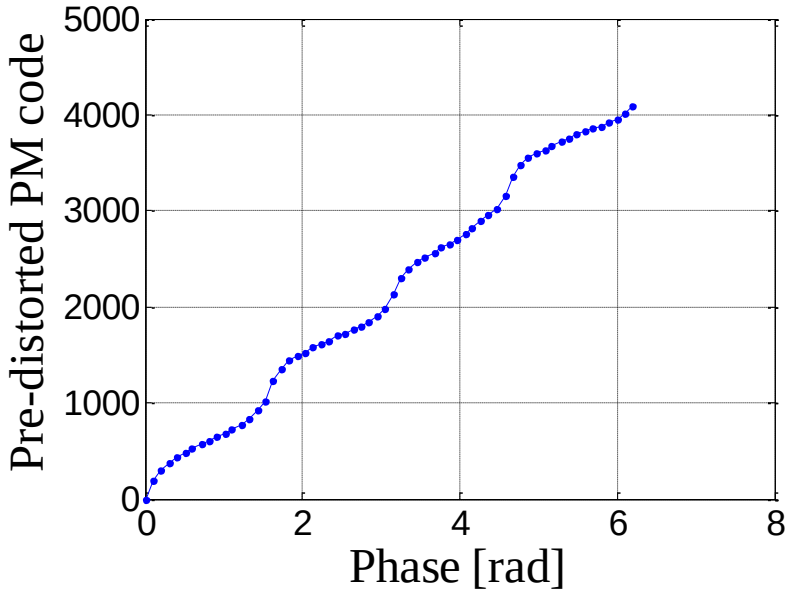

Figure 5.10: Phase LUT

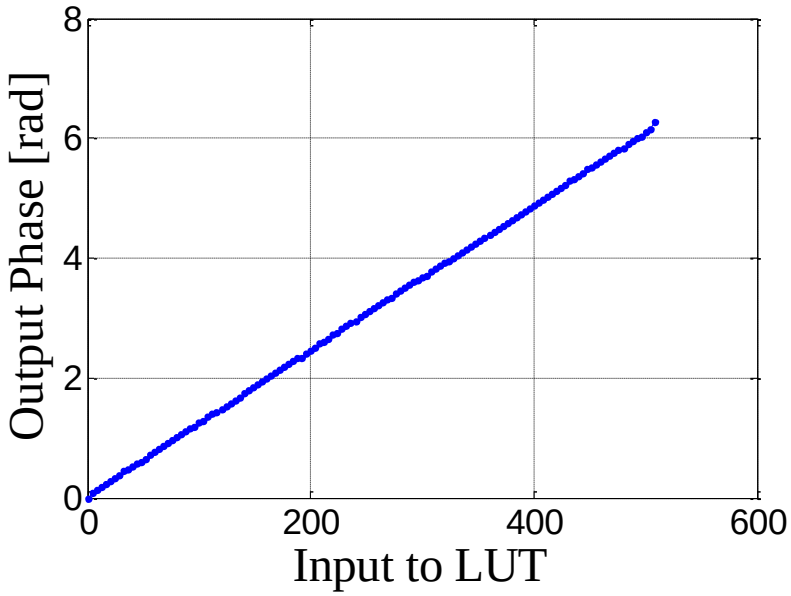

Figure 5.11: Output phase vs pre-distorted input

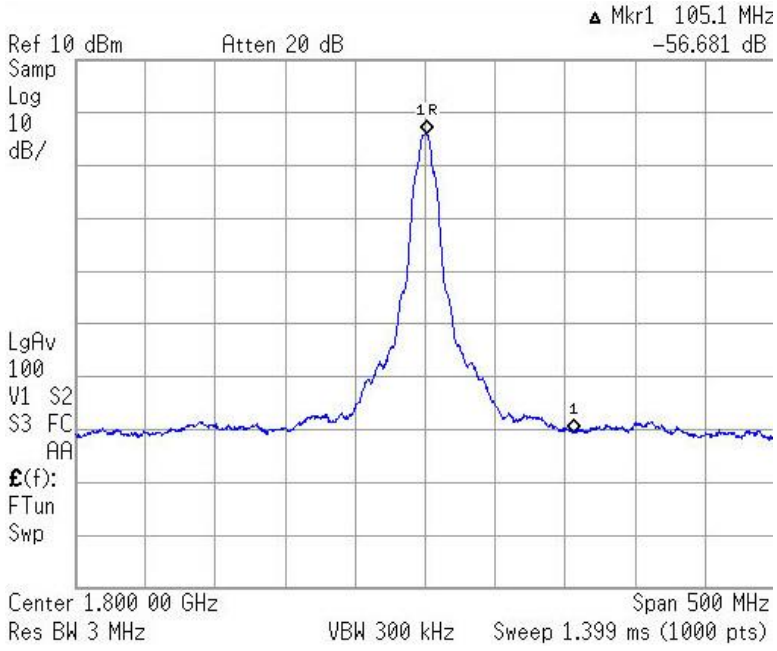

Figure 5.12: Measured output spectrum of 20 Mb/s GFSK data

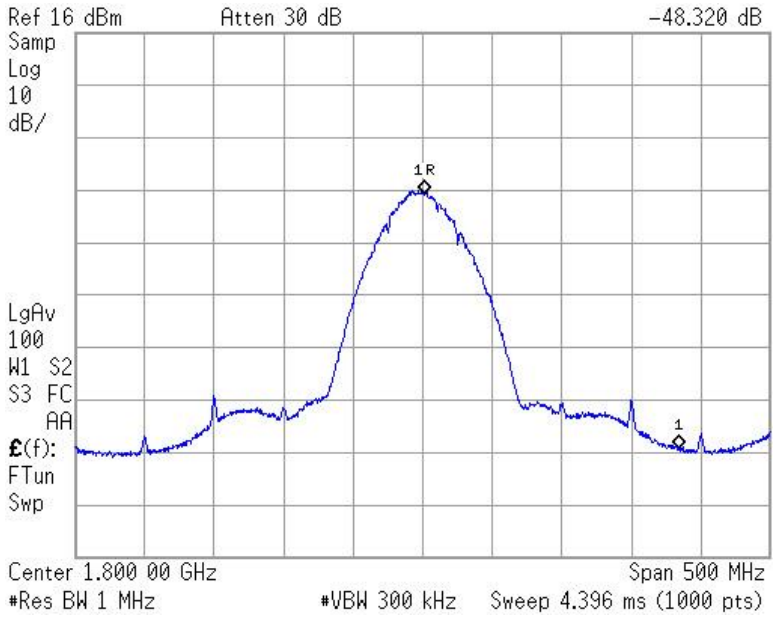

Figure 5.13: Measured output spectrum of 100 Mb/s GFSK data

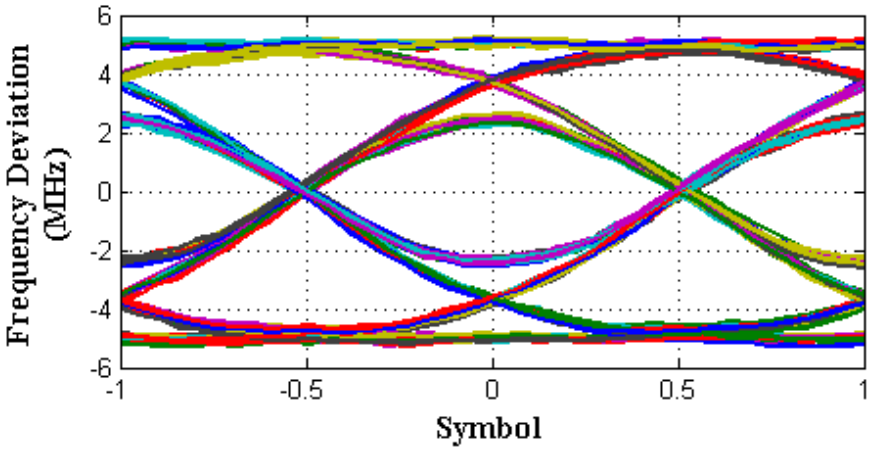

Figure 5.14: Measured transmitted eye-diagram of 20 Mb/s GFSK data

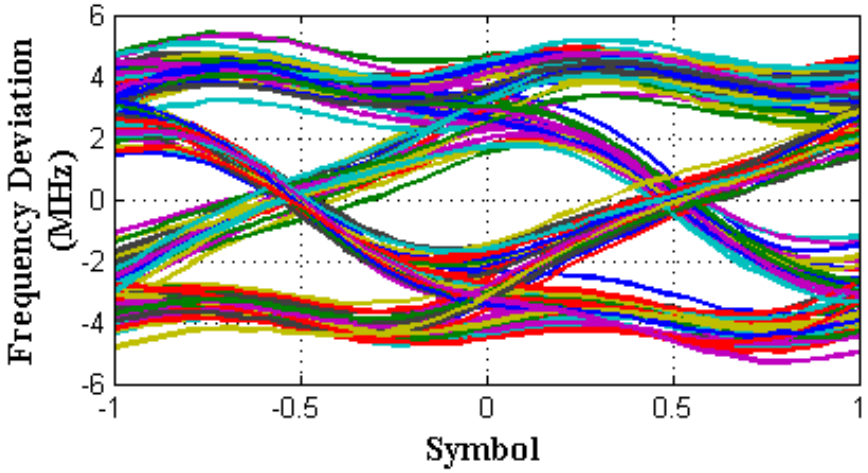

Figure 5.15: Measured transmitted eye-diagram of 100 Mb/s GFSK data

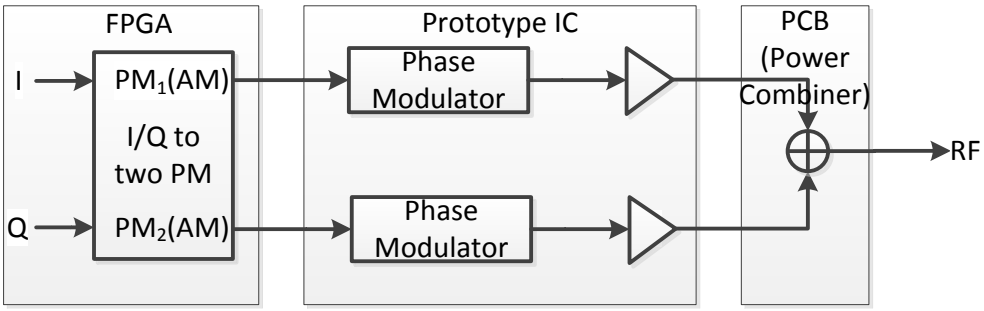

Figure 5.16: Measurement setup for output-phasing transmitter

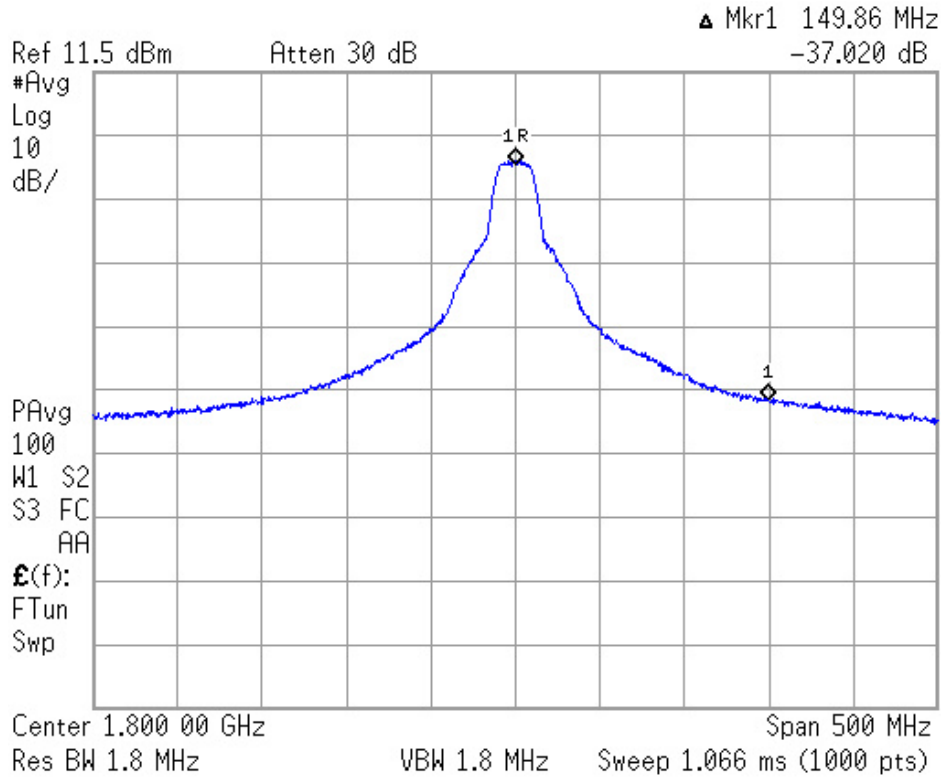

Figure 5.17: Measured output spectrum of 20 Mb/s 16-QAM data

Table 5.2: Comparison with Prior Art on Phase Modulators

Parameter	[1]	[2]	[3]	[4]	[5]	This Work		
Technology [nm]	180	180	45	32	65	130		
RF Carrier Frequency [GHz]	0.38	2.4	2.4	2.4	2.4	1.8		
Area [mm^2](1)	0.47	0.21	1.6	0.5	0.2	0.09		
Inductor in Phase Modulator	No	No	No	No	Yes	No		
Integrated PLL	No	Yes	No	No	No	Yes		
Bandwidth [MHz]	6	120	20	20	20	20 (GFSK)	100 (GFSK)	20 (16-QAM)
ACPR [dB]	-25	-49(2)	-42	-42	-60	-56	-40	-30
EVM [dB]	-26	-26(2)	-25	-28	-28	-30	-22	-20
Power [mW](1)	8.8	32	130	82	9	18	20	36

(1) Phase modulator only.
(2) ACPR and EVM measured for 20 Mbps.

5.2.3 16-QAM Modulated Data

The phase modulators were also tested in an outphasing configuration to illustrate their use in a transmitter with both phase and amplitude modulation. The outputs were combined off-chip using passive power combiners. The measurement setup is depicted in Fig. 5.16. The outphasing transmitter has an out-of-band emission of -35 dB (Fig. 5.17), with an EVM of -20 dB and is found to be limited only by signal leakage between the two paths, due to bondwire coupling.

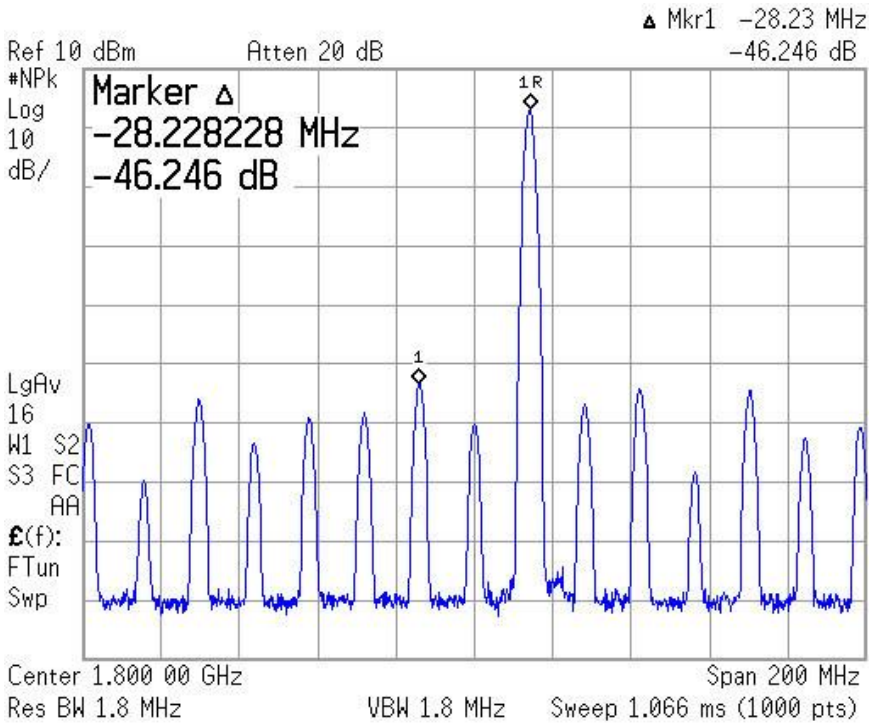

Figure 5.18: Measured output spectrum to show frequency synthesis at 1.8141 GHz

5.2.4 Frequency Generation

The open-loop modulator was tested with a phase ramp to demonstrate its use in frequency synthesis. The input phase ramp was clocked with a fixed clock frequency. In this work, the primary focus was on the generation of phase modulated signals and the ability to generate digitally pre-distorted phase ramp with PM output synchronous clock was not integrated on-chip. Fig. 5.18 depicts the output spectrum when a phase ramp with a ramp step size of $2\pi/64$ is applied to the phase modulator. The phase modulator output shows the desired tone at 1.8141 GHz. All the spurious tones at multiples of the offset frequency of 14.1 MHz are lower than -46 dBc.

The image tone at $F_C - \Delta f$ resulting from harmonic mixing of the phase ramp and the reference phase input, is 1.9 dB higher than calculations predict (Eq. 3.8). This may be due to second order effects like couplings due to supply noise or due to dynamic errors which could not be accounted for in the simulations. The sidebands at $F_C \pm 3\Delta f$ are contributed by 3rd harmonic of input phase reference to PM. An expression for the image tone and sidebands at $F_C \pm 3\Delta f$ in the output spectrum is computed in Appendix 3.5.2 and 3.5.3, respectively. The rms jitter in the output is 1.3 ps, which is the best among all prior art for clock generation units. Table 5.3 summarizes the performance comparison with other state-of-the-art fractional-N clock generation units. Although the power consumption is comparatively high, it is expected to improve significantly, when implemented in a finer process node.

Table 5.3: Comparison with Prior Art on Clock Generators

Parameter	[9]	[10]	[11]	[12]	[13]	This Work
Technology [nm]	65	22	65	65	65	130
Clock Frequency [GHz]	0.58	3.6	1.27	0.75	1	1.8
Area [mm^2]	0.03	0.03	0.044	0.038	0.017	0.09
Architecture	Frac-N ILO	Frac-N PLL	DDS	Frac-N PLL	Frac-N divider	Phase Modulator
RMS Jitter [ps]	8.05	10	12.8	5.51	3	1.3
Power [mW]	10.5	18.5	19.8	3.4	3.2	18

Chapter 6

Conclusion

In this dissertation, a wide bandwidth, low noise, open-loop phase modulator, whose non-linearity is improved by the use of digital calibration, is proposed. The design aspects of open loop phase modulators are discussed in detail, along with performance optimization of the phase quantization noise technique of [2]. The successful development of the proto-type IC, for solving the challenge of high resolution and wide-bandwidth phase modulation, involved several improvements, in both the overall system and the underlying circuits.

Firstly, a new calibration technique was developed for estimating the dominant sources of phase errors in the phase interpolator. These errors will only become more problematic as we scale to more advanced process nodes. The digital approach is low-power and easily scalable to newer process nodes. An elaborate discussion on the performance bounds of the technique is described in this dissertation. Although, temperature variation did not pose a serious problem for the present application, further research on background calibration to reduce temperature sensitivity is needed for a robust solution.

Secondly, the usefulness of the technique was demonstrated with performance improvements while transmitting wide-bandwidth GFSK modulated signal, as well as in low spurious content clock generation for multiple clock-output system. The theory behind the spurious tones in the spectrum of generated clock, when phase switching is not synchronized with modulator output, was explained and a closed form expression for

these tones was derived. The proto-type IC integrated dual phase modulators, which enabled the demonstration of amplitude modulation, in an out-phasing transmitter topology.

Thirdly, several circuit techniques were adopted to achieve the desired performance. The complementary mos buffer had 50% higher bandwidth than an nmos source follower at constant current, resulting in power savings. The raw phase interpolation quantization step-size was increased to 12 bits in a single stage of phase interpolation. Granted that two stage interpolation has lower systematic non-linearity, but the concomitant gain and timing mismatch between the two paths severely degrades the achievable performance. Furthermore, the additional non-linearity was easily compensated by the proposed technique. Among other circuit improvements, the switching frequency was increased to 900 MHz; the associated switching spurs will be further attenuated when the phase modulator is embedded inside a polar or out-phasing transmitter. Finally, the sources of dynamic errors were carefully addressed in the design of mixed-signal data interface and the layout of clock lines for low jitter and variability between unit cells of the phase modulator.

To conclude, the prototype IC based on the proposed technique, was able to achieve 56 dB lower out-of-band emission and 3.2% r.m.s. error while transmitting 20 Mb/s GFSK signal. Using only one PLL, the phase modulator was also able to generate multiple low noise clock outputs in an efficient manner.

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