UNIVERSITY OF CALIFORNIA, SAN DIEGO

High Performance Channelizers, Tunable Notch Filters, and Silicon-Based Antennas for RF to Millimeter-Wave Communication Systems

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor Kevin B. Quest

2011

The dissertation of Yu-Chin Ou is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

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DEDICATION

To my family

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The material in this dissertation is based on the following papers which are either published, or under final process for publication.

Chapter 2 is mostly a reprint of the material as it appears in IEEE MTT-S International Microwave Symposium Digest, 2010. Yu-Chin Ou and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

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PUBLICATIONS

Yu-Chin Ou and Gabriel M. Rebeiz,"A 20-90 MHz 26-Channel Cochlear-Based Channelizer," *IEEE Int. Microw. Symp. Dig.*, May 2010, pp. 213-216.

Yu-Chin Ou and Gabriel M. Rebeiz,"Lumped-Element Fully Tunable Bandstop Filters for Cognitive Radio Applications," *IEEE Trans. Microw. Theory Tech.*, (in review).

Yu-Chin Ou and Gabriel M. Rebeiz,"On-Chip Slot-Ring and High-Gain Horn Antennas for Millimeter-Wave Wafer-Scale Silicon Systems," *IEEE Trans. Microw. Theory Tech.*, accepted for publication in March 2011.

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ABSTRACT OF THE DISSERTATION

High Performance Channelizers, Tunable Notch Filters, and Silicon-Based Antennas for RF to Millimeter-Wave Communication Systems

by

Yu-Chin Ou

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2011

Professor Gabriel M. Rebeiz, Chair

This thesis first presents a 26-channel channelizer based on the mammalian cochlea and covering the 20-90 MHz band. Each channel has a 6-pole frequency response with a constant absolute bandwidth of 1.4 MHz at 20-30 MHz, and a constant fractional bandwidth of 4.5$\pm$0.6% at 30-90 MHz, and is built entirely using lumped elements. Measurements show an S_{11} $<$ -12 dB at 20-90 MHz, a loss of 4-7 dB, $>$ 40 dB isolation between the channels, and agree well with simulations. The applications areas are in communication systems with very high levels of interferes and in defense systems.

In another project, tunable lumped-element bandstop filters for the UHF-band cognitive radio systems are presented. The 2-pole filters are implemented using lumped elements with both single- and back-to-back silicon varactor diodes. The single diode

filter tunes from 470 to 730 MHz with a 16-dB rejection bandwidth of 5 MHz and a filter quality factor of 52-65. The back-to-back diode filter tunes from 511 to 745 MHz also with a 16-dB rejection bandwidth of 5 MHz and a quality factor of 68-75. Both filters show a low insertion loss of 0.3-0.4 dB. Nonlinear measurements at the filter null with Δf = 2 MHz show that the back-to-back diode filter results in 12-dBm higher third-order intermodulation intercept point (IIP3) than the single diode filter. A scaling series capacitor is used in the resonator arm of the back-to-back diode filter and allows a power handling of 25 dBm at the 16 dB rejection null. The cascaded response of two tunable filters is also presented for multi-band rejection applications, or for a deeper rejection null ($>$ 36 dB with 0.6 dB loss at 600 MHz). The topology can be easily extended to higher-order filters and design equations are presented.

The third project presents on-chip slot-ring and horn antennas for wafer-scale silicon systems. A high efficiency is achieved using a 100 μm quartz superstrate on top of the silicon chip, and a low loss microstrip transformer using the silicon back-end metallization. A finite ground plane is also used to reduce the power coupled to the TEM mode. The slot-ring and 1-λ_0^2 horn achieve a measured gain of 0-2 dBi and 6-8 dBi at 90-96 GHz, respectively, and a radiation efficiency of $\sim$50%. The horns achieve a high antenna gain without occupying a large area on the silicon wafer, thus resulting in a low cost system. The designs are compatible with either single or two-antenna transceivers, or and with wafer-scale imaging systems and power-combining arrays. To our knowledge, this is the highest gain on-chip antenna developed to-date.

Finally, differential on-chip microstrip and slot-ring antennas for wafer-scale silicon systems are presented. The antennas are fed at the non-radiating edge which is compatible with differential coupled-lines, and are built on a 0.13-μm CMOS process with a layout which meets all the metal density rules. A high radiation efficiency is achieved using a 100 μm quartz superstrate placed on top of the silicon chip. Both antennas achieve a measured gain of $\sim$3 dBi at 91-94 GHz, with a -10 dB S_{11} bandwidth of 7-8 GHz and a radiation efficiency of $>$50%. The designs are compatible with single and multi-element transceivers, and with wafer-scale imaging systems and power-combining arrays. To our knowledge, this is the first demonstration of high-efficiency on-chip differential antennas at millimeter-wave frequencies.

Chapter 1

Introduction

1.1 Filter Banks and Channelizer

A multiplexer is a $N + 1$ port device which sub-divides a wideband signal at the common port into N signals with smaller bandwidth at the channel ports. The circuit topology is a collection of separate bandpass filters with each filter connected to a common port. Multiplexers are used in wideband communication systems for frequency channelization, and they enable a receiver or transmitter to accommodate multiple signals and channels at the same time. A channelizer is a multiplexer with contiguous adjacent channel passbands. It is especially used for frequency dividing due to its usage in channelizer receiver front-ends (Fig. 1.1).

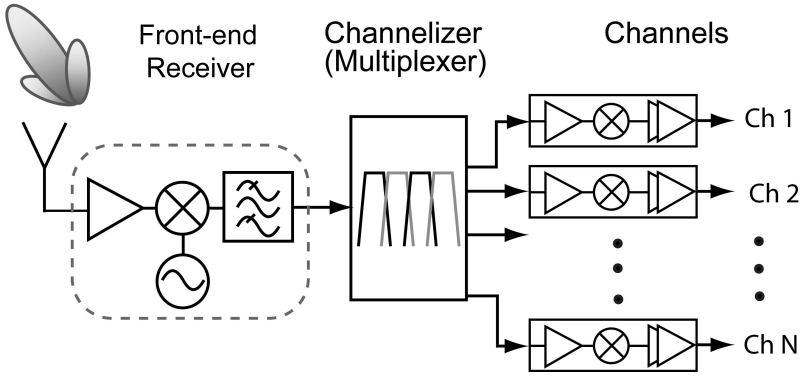


Figure 1.1: Detailed block diagram of a communication receiver system employing continuous multiplexer scheme.

For applications in satellite and military communication radios [1] [2] [3], channelizers composed of multi-mode waveguide filters are used for high quality and reliable performance, but this results in a very complex filter network when a large number of higher order channels are considered. It implies simultaneously optimization of a large number of variables on a huge and massive microwave circuit device. Previously, the implementation is done with a lot of effort and time by manually tuning and optimization based on practical experience through observing the filter shape on the oscilloscope. However, with the advent of Computer Aided Design (CAD) software providing accurate circuit simulation response, the design on more complicated and huge circuits are possible [4].

The noise figure in a receiver is mostly governed by the front end section, and any loss after the receiver contributes very little to the noise figure such that a few dBs insertion loss on the channelizer is tolerable in the radio architecture [1]. The signal magnitude distorted in the filter passband could be compensated through cascading amplifiers after the channelizer. In another word, a variety of lower quality factor components could be used for filter implementation. This provides the maximum of flexibility at low frequency applications where the tradeoffs are made between the frequency performance and the physical mass and volume of a circuit.

[5] [6] [7] present passive RF channelizers based on an equivalent circuit of a mammalian cochlea implemented with surface mount technology (SMT) devices on the printed circuit board (PCB). The electronic circuit topology is an analogy of the biological basilar membrane. The cochlear-like channnelizer based on the theoretical analysis, could cascade unlimited number of channels together with a systematic design and optimization method. As a result, an electronically and physically small and lightweighted channelzier is implemented with lumped-element components and the high performance is achieved with higher order channel filter response.

1.2 Frequency Agile Bandstop Filter

Multi-band and multi-mode devices are changing the paradigm of modern wireless radio systems due to the ability to cover different communication standards with

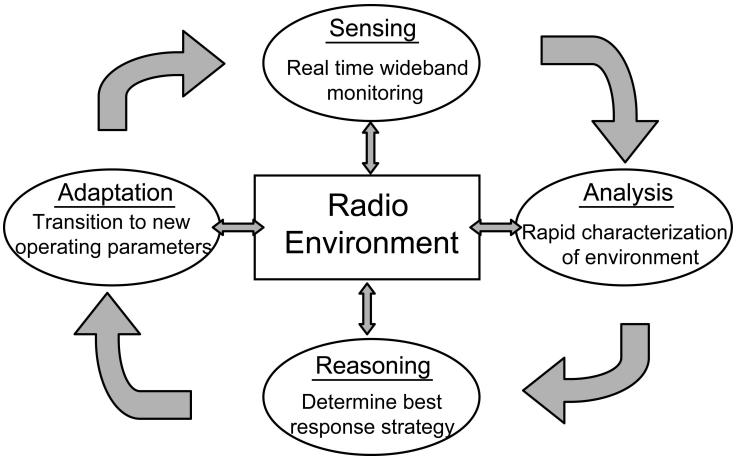


Figure 1.2: Typical duty cycle of cognitive radio and software-defined radio systems [10].

one single device. As the microwave system evolving, software-defined radio (SDR) and cognitive radio (CR) have been introduced for dynamic spectrum access and co-existence [8]. With frequency agile filters, the communication systems are intelligent and can sense the frequency environment and modify their spectrum usage based on the detection.

Operation principles of a SDR or CR system consist of spectrum sensing and analysis, management and handoff, and spectrum allocation and sharing. An intelligent communication system will have both cognitive capability and reconfigurability. The radio system first scans the available spectral environment to gain necessary information from the radio environment. This characteristic is called cognitive capability which enables the device to analyze and determine the acceptable behaviors under current circumstances. A reasoning engine then makes the decision based on its database of communication standards. The system changes its operating mode (frequency, bandwidth, modulation) to adjust to the environment variations and the optimal data transfer is achieved. This ability is referred to the reconfigurability [9] [10].

Bandstop filters are used for spectrum management by compressing jammer level in the receiver radio and are essential in the SDR and CR systems. Filters can be tuned mechanically [11] or electronically by magnetic field controlled ferrites such as BST (Barium Strontium Titanate) filters [12] and YIG (Yttrium-Iron-Garnet) filters [13], by plasma crystals [14], by RF-MEMS switches [15] [16], and by varactors [17] [18].

Among these canonical filter topologies which reflect back the undesired signals, high quality factor resonators are essential to the filter selectivity and bandwidth. Low unloaded Q_u components are vital to the bandstop filter selectivity. Another absorptive type filters are therefore proposed to improve the signal rejection with orders of magnitude more selective than reflective bandstop filters with with identical resonator Q_u.

Tunable absorptive notch filters [19–23] equally split the input signal to two different circuit paths with 180° phase difference and re-combining the signals together back again at the output port. As a result, the power of the stop band frequencies is diddipated in, rather than reflected from the lossy resonators.

Recently, a new bandpass-to-bandstop tunable filter [24] is presented to integrated a bandstop filter into a bandpass filter. The filter response can be dynamically switched between a bandpass and bandstop. In modern communication architecture, such multi-function filters can be used to providing flexibility to a system.

1.3 Millimeter-Wave On-Chip Integrated Antennas

Millimeter-wave systems provide better resolution than microwave systems and are less affected by atmospheric conditions than infrared systems. Millimeter-wave antennas are used for scientific and military applications in areas such as remote sensing, radio astronomy, plasma diagnostics, radar. A common requirement on mm-wave antennas is a high directivity. Traditionally, mm-wave antennas are categorized into 3 types: antennas derived from open and closed waveguide, printed circuit antennas, and the integrated antennas [25].

The waveguide type antennas radiate through the energy leakage from the guiding structure such as: periodic dielectric antennas, uniform waveguide leaky-wave antennas, arrays of leaky-wave antennas, and tapered slot antennas. The advantage of this type of antenna is their compatibility with the waveguides from which they are derived, thus facilitating integrated design. Since the radiation angles changes with frequencies, the antennas are used as frequency scanning.

Printed antennas are simple in structure and easy for fabrication. The geometry

is low profile, light weight that are suitable for array application. Microstrip antennas, printed dipoles, and substrate-superstrate configuration antennas.

The term integrated antennas is used for a class of radiating structures when devices such as solid-state oscillators, detectors, phase shifters and filters are integrated with the radiating elements on the same substrate, typically in monolithic form. At the small dimensions in the mm-wave region, wafer-scale integration becomes feasible and an entire phased array antenna of fairly high gain can, in principle, be fabricated on a single ”chip”. Integrated antennas have the obvious advantages of compactness, reliability, reproducibility and if fabricated in large numbers, of low cost [26].

1.4 Goal and Contents of Thesis

In this thesis, the objective is to develop hardware solutions for microwave and millimeter-wave communication systems. This includes antenna and filter designs for applications in simplified architectures, based on or compatible with the PCB and CMOS/SiGe technologies.

Chapter 2 presents lumped-element cochlear-based channelizers with 6^{th} order channel filtering response. 26 channels are designed to cover the 20-90 MHz with a $>$ 40 dB channel-to-channel isolation. The channelizer shows flexibility by designing with a combination of constant fractional bandwidth channels and constant absolute bandwidth channels. Each channel filter is implemented with a semi-lumped capacitor approach such that the 2% error tolerance in the lumped component is compensated. In the end, 2 channelizers are developed and with very identical frequency responses.

Chapter 3 presents a tunable bandstop filter for cognitive radio application. The analytic synthesis procedure is given for lumped-element filter implementation. The circuit is implemented with SMT lumped-element circuits such that the electrically and physically small circuit size is practical for applications in mobile devices. The bandwidth and center frequency of filters are tunable at 500-700 MHz and the circuits are designed to operate under high input power conditions.

In chapter 4, a single-ended SiGe/CMOS on-chip slot-ring antenna and high-gain horn integrated antennas are designed and implemented at 94 GHz. The design

of antenna, input impedance, superstrate thickness, mutual coupling is discussed. A metallic horn is placed on top of the superstrate antenna and this results in high antenna radiation gain. The on-chip antennas show the state-of-art performance with high radiation efficiency among on-chip integrated antennas and they are compatible with either single or two-antenna transceivers, or and with wafer-scale imaging systems and power-combining arrays.

In chapter 5, differential on-chip microstrip and slot-ring antennas are presented at 94 GHz for millimeter-wave applications. The antennas are fed at the non-radiating edge with a differential feed-line by fringing field coupling. Amplitude and phase imbalance and mixed mode analysis are studied to analyze the differential antenna performance. The antennas in this chapter is compatible with the metallic horn extension design in chapter 4 for high gain applications.

Chapter 6 concludes the thesis and presents ideas for future work.

Chapter 2

A 20-90 MHz 26-Channel Cochlear-Based Channelizer

2.1 Introduction

Cochlear channelizers are passive wideband multiplexers with contiguous channels whose operation are based on the mamalian cochlea. The cochlea is an electro-mechanical transducer located in the inner ear that converts acoustical energy (sound waves) into nerve impulses sent to the brain, resulting in hearing [27], [28], [29], [30]. The cochlear channelizer circuit topology is derived from an electrical-mechanical analogy of the basilar membrane (Fig. 2.1(a)). Previously, single-order cochlear channelizers were first demonstrated for both constant fractional bandwidth and constant absolute bandwidth channels at 20-90 MHz [5]. Galbraith $et\ al.$ [7] then demonstrated a 10-channel 3-pole design with 17% fractional bandwidth at 200-1000 MHz with 1.1 dB loss and 20 dB adjacent-channel isolation.

Hunter demonstrated a 10-channel and a 27-channel channelizers with lumped-element 6-pole filters at 600-1300 MHz using filter banks constructed as even and odd channel multiplexers connected using a 3-dB Wilkinson power divider [31]. The ”lossy manifold” technique enables a large number of channels to be coupled from a single manifold due to the wide frequency spacing between the channels in the even and odd paths.

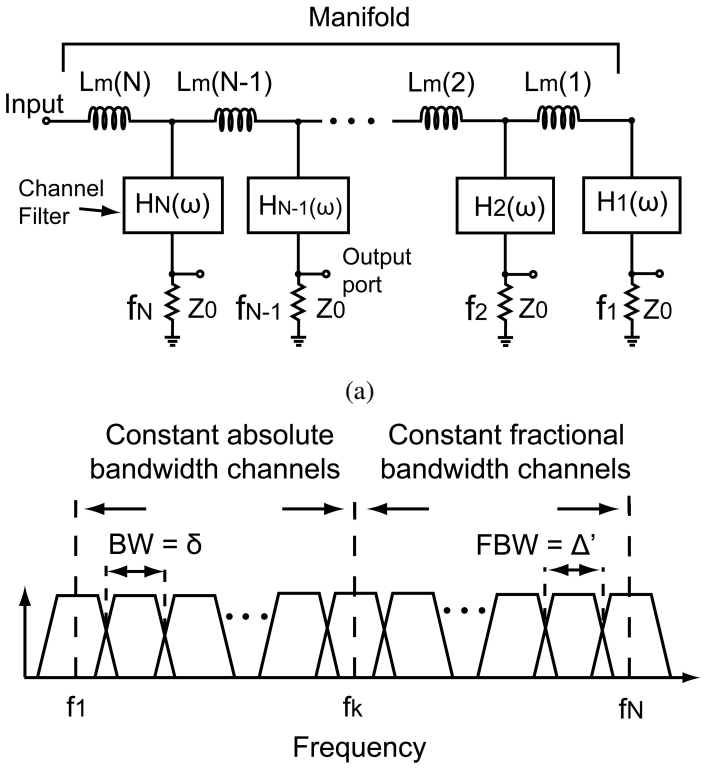


Figure 2.1: (a) Higher-order cochlear channelizer circuit model. (b) Channelizer composed of constant absolute bandwidth and constant fractional bandwidth filters.

In this chapter, we present an improved cochlear channelizer that implements 6^{th}-order filters in each channel [27]. This version retains the inductive manifold of the single-order cochlea channelizer, but offers improved stopband rejection and passband shape. A 26-channel design covering a 5:1 frequency range from 20 to 90 MHz is presented. The design is based on lumped elements and is built on a single-layer Teflon board.

2.2 Design

The channelizer design procedure includes determining the filter order, the number and bandwidth of each channel, synthesis of each channel filter, and designing the manifold. The channelizer presented in this chapter uses a combination of channels of constant fractional bandwidth and constant absolute bandwidth at 20-90 MHz (Fig. 2.1(b)).

2.2.1 Channel Filter Design Parameters

In this chapter, each channel filter is designed based on a Chebyshev (equal-ripple) response. The minimum stopband attenuation S dB located at Ω = Ω_S for a lowpass filter prototype with a cutoff frequency Ω_c =1 is [11], [32]

$$\Omega_s = cosh\left(\frac{1}{M} cosh^{-1}\sqrt{\frac{10^{\frac{S}{10}}-1}{10^{\frac{r}{10}}-1}}\right), \quad \Omega_s \geq 1 \tag{2.1}$$

where M is the filter order and r is the passband ripple in dB.

Equation (2.1) is used to determine the necessary filter order, M, based on a specific attenuation that each channel must provide at its adjacent channel center frequency. The fractional bandwidth for the 3 dB attenuation point with respect to the bandpass filter center frequency ω_0 is therefore given by:

$$\Delta_{3dB} = \Delta_{rdB} \cdot \Omega_3 \tag{2.2}$$

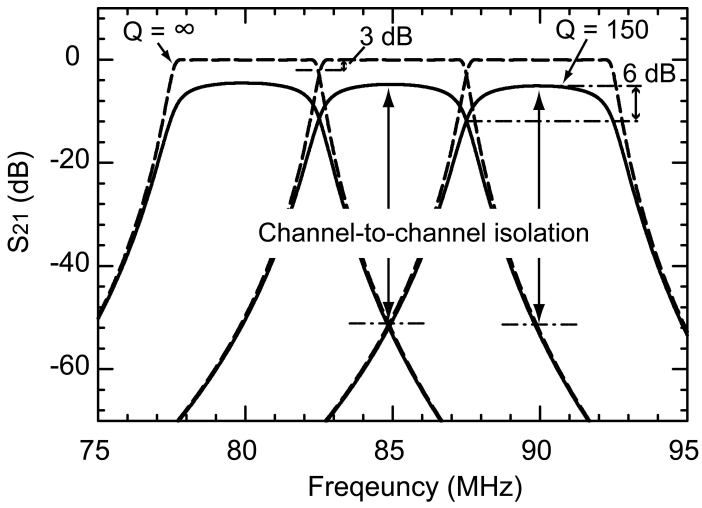


Figure 2.2: Cross-over points of 6-pole filters with $Q = \infty$ and Q = 150 cases. The ideal 3-dB filter cross-over point drops to $>$ 6 dB for Q = 150 case.

The filter loss, ΔL, is given by:

$$\Delta L = \frac{4.343}{Q} \sum_{i=1}^{M} g_i \ \ (\mathrm{dB}) \tag{2.3}$$

where g_i are the element values of the lowpass prototype and Q is the resonator unloaded quality factor.

The number of channels, N, to cover the total required bandwidth is given by

$$N \simeq 1 + \frac{\ln\left(\frac{f_N}{f_k}\right)}{\ln\left(\frac{1+\Delta'/2}{1-\Delta'/2}\right)} + \frac{f_k - f_1}{\delta} \tag{2.4}$$

where f_N and f_1 are the maximum and minimum channel center frequencies and f_k is the frequency separating constant fractional bandwidth and constant absolute bandwidth channels (Fig. 2.1(b)). The fractional bandwidth Δ' and the constant bandwidth δ are defined from the crossover points which are chosen as 3 dB below the channels' maximum response. This empirical value provides enough inter-channel coupling for the cochlea-like response and achieves a wideband input match by absorbing nearly all of the power in the total channelizer bandwidth. Equations (2.2) and (2.3) can then be applied to determine the channel bandwidth based on the allowable filter loss which is, in turn, dependent on Q.

It is important to note that, in the finite resonator Q case, the crossover point will drop due to the introduction of filter insertion loss and the rounded-off filter edges as shown in Fig. 2.2. A ∼6 dB crossover point is shown under the Q = 150 case for 6-pole filters with a 3-dB bandwidth of 5 MHz. The difference between the transmission response of any two adjacent channels is defined as the channel-to-channel isolation (or rejection).

The center frequency of each channel filter is then determined as

$$\begin{cases} f_{n-1} = f_n \left(\frac{1-\Delta_{3dB}/2}{1+\Delta_{3dB}\ 2} \right) & n = N, N-1, ...k+1 \\ \\ f_{n-1} = f_n - \delta & n = k, k-1, ...1 \end{cases} \tag{2.5}$$

2.2.2 Channel Filter Synthesis

The impedance behavior of each channel filter over the entire bandwidth is an important parameter. In particular, the channel filter response has to be resistive in its passband, capacitive at frequencies lower than its center frequency, and inductive at higher frequencies. The channel also requires to be an open circuit at both very low and very high frequencies which is analogous to the frequency response of a series RLC network, shown in Fig. 2.3(a), where A is the 3-dB cross-over point.

The channelizer composed of such filters with $Q = \infty$ has the equivalent circuit shown in Fig. 2.3(b). For a specific resonant filter f_o, the higher frequency capacitive filters in conjunction with the series inductive manifold act as an up-converting ladder matching network. This transforms the load impedance, composed of the resistive resonant filter at f_o and other lower frequency inductive filters, to the input port with an impedance-match condition. Therefore, the input signal propagates without distortion in the ladder matching network until it reaches the resonant f_o channel and the signal is absorbed by Z_0 at the output port. The up-converting ladder-type matching network also implies that the input impedance Z_{ch} of the resonant filter should be smaller than the terminal impedance Z_{in} (usually 50 Ω).

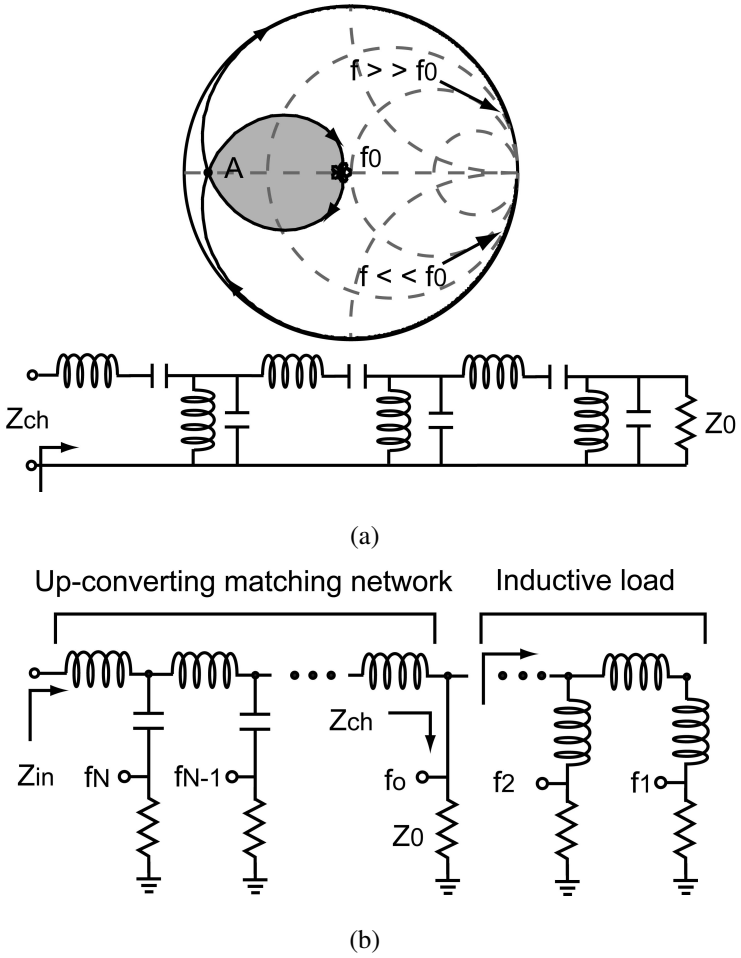


Figure 2.3: (a) Required channel filter input impedance characteristic (Smith chart of impedance Z_{ch}) and the corresponding bandpass filter prototype for a cochlear channelizer (response for sixth order shown). (b) Simplified cochlear channelizer equivalent circuit at the resonant frequency f_o.

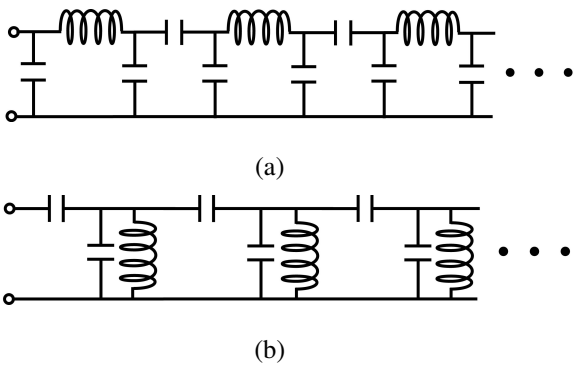


Figure 2.4: Bandpass filter prototypes of (a) tubular, and (b) top-C topology suitable for cochlear-like channelizer implementation.

Both "tubular" and "top-C coupled" (Fig. 2.4) topologies have similar frequency responses as the ideal series RLC filter and are good candidates for 20-90 MHz. The main difference is the inductor position: shunt to ground in "top-C coupled" and in-series in the "tubular" topology. The tubular topology is chosen due to the lower level of cross coupling between the inductors and this leads to a more compact circuit. The tubular filter synthesis is readily performed using Agilent's Advanced Design System (ADS) [33].

2.2.3 Manifold

The coupling inductance $L_m(n)$ of the manifold is designed based on the following equation in terms of channel number n [7]

$$L_m(n) = L_0 e^{a\left(1-\frac{n}{N}\right)}, \quad 1 \leq n \leq N. \tag{2.6}$$

One first connects all the channel filters with series inductances $L_m(n)$ and varies L_0 and a in the simulation to achieve the best input return loss. A good starting point is given in [7] which the reactance of $L_m(n)$ is 5-8 Ω at the lowest channel center frequency.

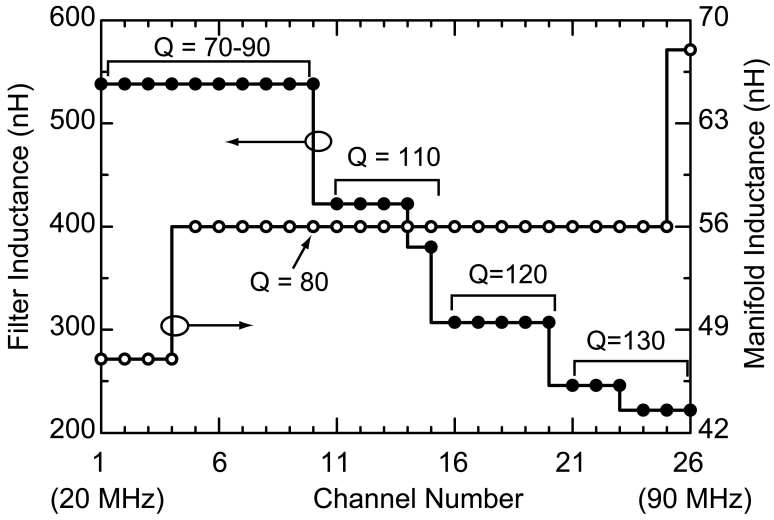


Figure 2.5: Lumped inductor values and Q for the channel filters and manifold sections.

2.2.4 Design

The 26-channel channelizer (N = 26) is designed to cover 90-20 MHz. A 40 dB channel-to-channel isolation requirement results in a 6^{th} order filter choice. Due to the available inductor Q of 130-70 within this frequency range, a 3-dB channel fractional bandwidth of Δ_{3dB} = 5.6% is chosen to cover 90-30 MHz with filter loss of 4.9-7.1 dB, respectively. From 30-20 MHz, constant absolute bandwidth filters of 3-dB bandwidth δ = 1.8 MHz are used with a filter loss of 7.1-6.4 dB, respectively. The filter center frequencies are calculated using (2.5). Since the finite resonator Q narrow the realized filter bandwidth, the ideal filter spec of Δ_{3dB} = 5.6% and δ = 1.8 MHz result in the realizable filter bandwidth of Δ_{3dB} = 4.5% and δ = 1.4 MHz.

Commercially available inductors ranging from 246-538 nH for 90-20 MHz are used, and each filter is synthesized with Z_{ch} = 8 Ω and Z_0 = 50 Ω (Fig. 2.5). Z_{ch} = 8 Ω is chosen to yield a 6-pole tubular filter response with reasonable component values. This results in a resonator inductor impedance, X_L, $<$ 130 Ω at the center frequency of every filter, and the lumped-element inductors do not suffer from parasitic capacitive effects. Since the lumped capacitors are only available in discrete values, the shunt capacitance of every channel filter is realized by a combination of lumped-element capacitors and parallel-plate capacitors composed of the microstrip top-metal layer and the ground plane in the teflon board.

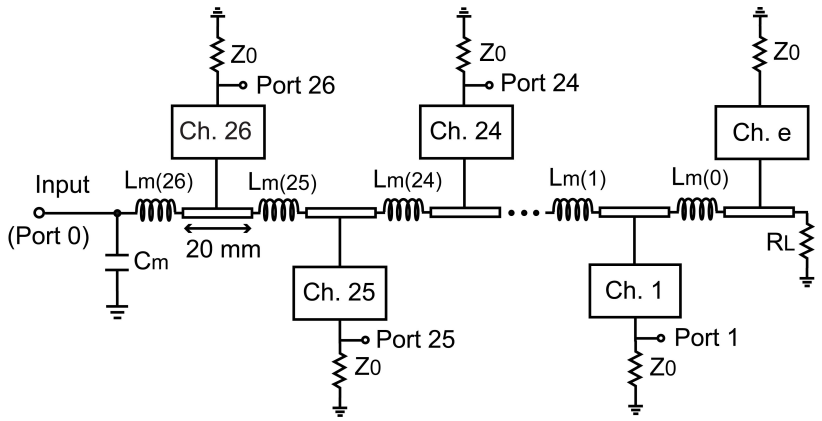


Figure 2.6: Block diagram for the 26-channel channelizer with additional matching networks.

For small-value shunt capacitances, with the EM simulator (Sonnet [34]) providing accurate estimation of the parallel-plate capacitance, the value of printed capacitance is chosen to minimize the overall error in the capacitance value. For example, the 28 pF capacitance is realized as a 16 pF printed capacitance in shunt with a 12 pF lumped capacitance, reducing the original component error of $\pm 2\%$ to $\pm 0.8\%$. As for the lower center frequency filters with large capacitance values, multiple small-value lumped capacitors are used instead of a single large value capacitance so as to minimize the capacitance error. For example, a 110 pF capacitance is realized with an 11 pF printed capacitance in conjunction of three 33 pF lumped capacitors. A similar method is applied to series capacitors with large values.

The inductive manifold is designed to facilitate higher power operation as well as to provide proper physical spacing between the channels (this is needed to obtain low cross-coupling). As a result, a combination of 50 Ω transmission line sections (20 mm for every section) and series lumped-element inductors $L_m(n)$ are realized based on (2.6) with L_0 = 56 nH and a = 0.1. This results in a gradual change in the manifold inductor values which can be approximated by a constant inductance of 56 nH.

The first and the last channel have different matching networks at resonance compared to the other channels. To further improve the input matching, a shunt capacitor C_m = 33 pF is placed at the channelizer input to match the slightly inductive input impedance of resonance at Ch.26 and a 3-pole tubular filter (Ch.e) loaded with 50 Ω is

attached to the end of the manifold to match the capacitive input impedance of resonance at Ch.1. This 3-pole filter must act as an inductive load and its center frequency is 19 MHz. With these additional matching networks, the series inductances in the manifold can then be optimized further using Agilent ADS and the component values are shown in Fig. 2.5. A load resistor R_L = 10 Ω is also attached to the end of the manifold to dampen manifold resonances within the channelizer bandwidth. A final circuit schematic is shown in Fig. 2.6.

2.2.5 Layout, Simulation and Tuning

The circuit is implemented in a microstrip form using a 0.787 mm thick board with ε_r = 2.20, (Rogers RT/Duroid 5880), two 53.3-μm-thick copper layers and 0.25 mm diameter plated thru-hole vias. An ε_r = 2.2 board was chosen since it results in a very stable dielectric constant and accurate parallel-plate capacitance. This simplifies the channelizer tuning, but results in a physically large board size (29 inches $\times$16 inches). The channel filters use surface-mount technology (SMT) devices, including Coilcraft Maxi/Midi Spring air coil inductors and Dielectric Laboratories multilayer capacitors, all with $\pm$2% or better tolerance. The filter inductors are chosen to be high-Q (70-130), while the manifold inductors are chosen to have a Q of 80 and a small physical size. The SMT capacitors have a $Q > 500$ at 20-90 MHz.

The filter layout is folded by arranging the series capacitors in the vertical direction. This results in off-center resonator inductors, minimizing the mutual coupling. The output of each channel is routed to an edge-launch SMA connector using 50 Ω transmission lines. Adjacent channel filters are placed on opposite sides of the manifold to reduce the electromagnetic coupling through the substrate. The channelizer is passive (no bias lines). A close-up view of the 26-channel cochlea-like channelizer is shown in Fig. 2.7.

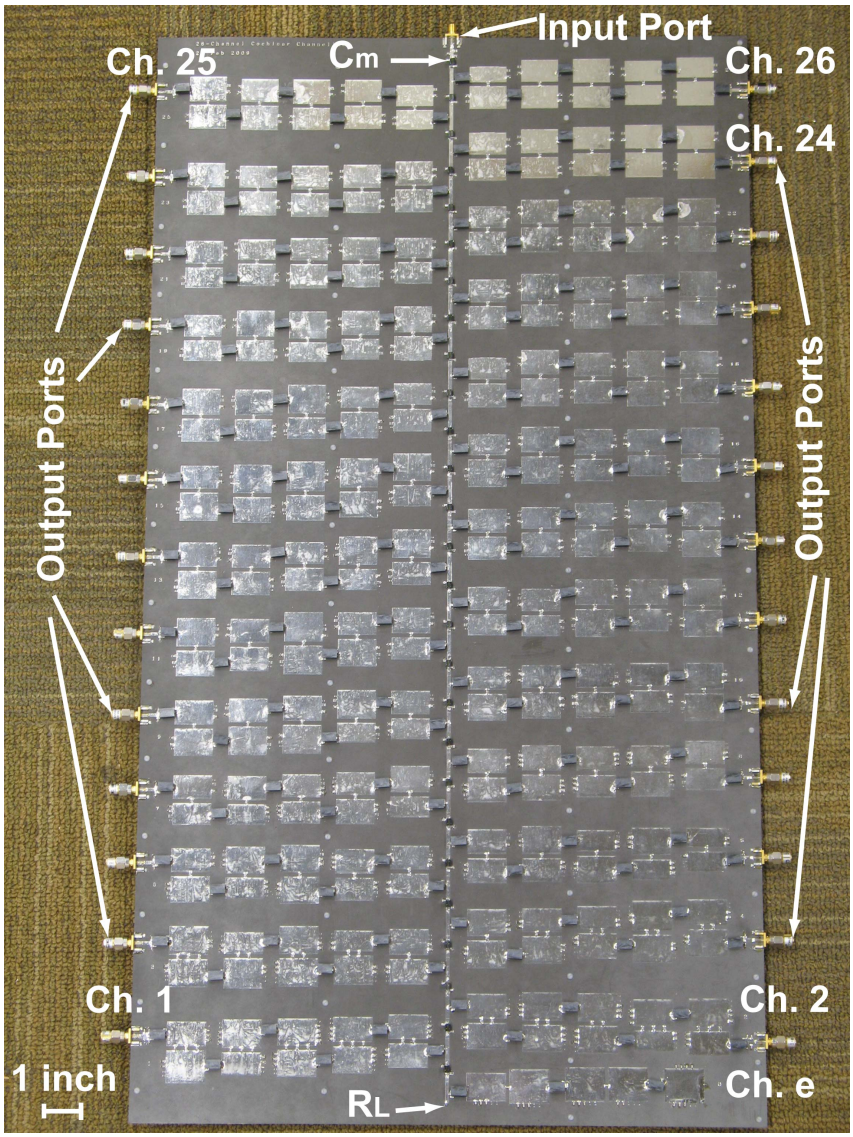


Figure 2.7: Photograph of the 26-channel channelizer and its corresponding ports ($29'' \times 16''$).

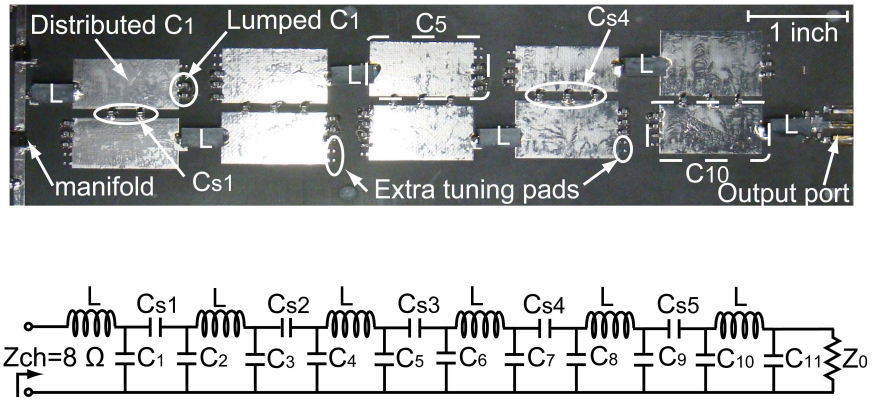


Figure 2.8: Photograph of channel filter 1 (f_0 = 20 MHz) and its equivalent circuit impedance versus frequency (Q = 70).

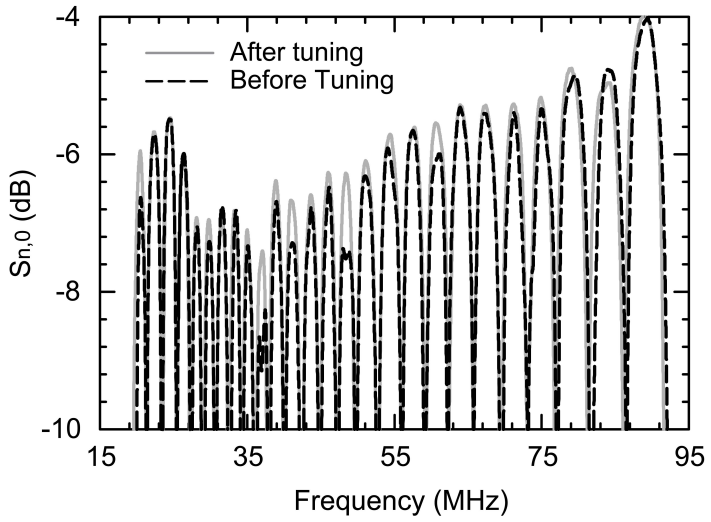


Figure 2.9: The measured transmission responses of the 26-channel channelizer before and after tuning.

The simulation is done with circuit models from Modelithics CLR Library [35]. Also, each channel layout, including component pads, printed parallel-plate capacitors, transmission-lines and surface-mount ports, are first simulated in Sonnet, and the resulting S-parameters are exported into ADS and simulated together with the Modelithics lumped-element models. The SMT models for the inductors and capacitors include the component pads and parasitic capacitance to ground and these shunt capacitances are absorbed into the filter design.

It is important to note that once the channel filters are connected to the manifold, the impedance at the manifold-filter junction is highly inductive, and the channel filters therefore require another optimization to yield a good channelizer response. This is done mostly by changing C_1, C_2 and C_3 of every filter while keeping L and $C_{s1} - C_{s5}$ constant. Each channel took 2-4 iterations to obtain the expected filter response and the final component values and layout dimensions are found. Overall, 186 inductors and 673 capacitors are used in the cochlear channelizer.

The channelizer board is first populated with the lumped-element components and the shunt capacitance is manually tuned for component error compensation. Several extra capacitor pads are included in advance for the shunt elements (Fig. 2.8) and the tuning is done by soldering lumped capacitors and checking the S_{11} response at every frequency band until the overall return loss meets the 12 dB level. This process of tuning results in a slight shift in the frequency response due to the additional shunt capacitance. However, it improves the S_{21} frequency response by 0.25-2 dB as shown in Fig. 2.9.

2.3 MEASUREMENTS

2.3.1 S-Parameters and Group Delay

The channelizer's S-parameters are measured using an Agilent E5071B vector network analyzer. A two-port short-open-load-thru coaxial line calibration sets the reference planes at the coaxial connectors. Each channel's transmission response is measured by connecting the VNA to the channelzier input (port 0) and to the n^{th} channel output (port n) with all other channels terminated in a 50 Ω load $(S_{n,0})$. The channelizer's input reflection coefficient $(S_{0,0})$ is obtained in the same way (each channel output terminated

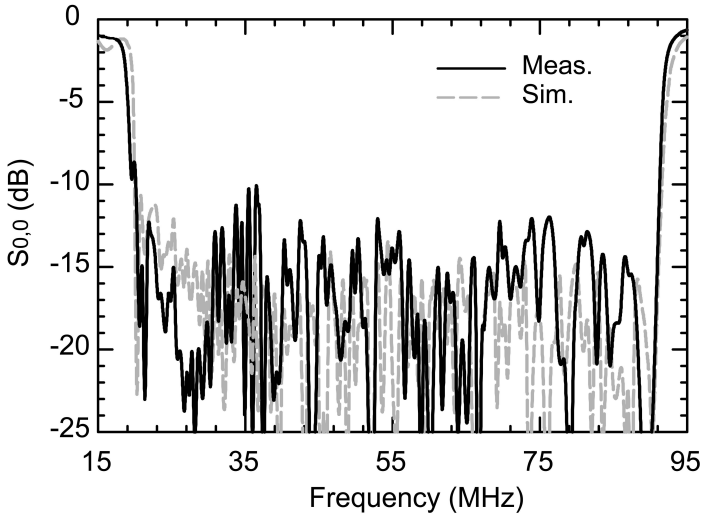
in 50 Ω).

Two 26-channel chanelizers were fabricated and resulted in near identical performance. The measured and simulated S-parameters of the channelizer are shown in Figs. 2.10 and Fig. 2.11 and a summary is presented in Table 2.1. The channels have an average 3-dB fractional bandwidth of 4.5±0.6% from 90 MHz to 30 MHz and an average 1.5 MHz absolute 3-dB bandwidth for the rest of the channels (Fig. 2.12). The insertion loss varies between 4.0 dB and 7.0 dB. The highest loss is obtained at Ch.10 for 3.8% bandwidth and an inductor Q of 70. The crossover points between each channel are $\sim$ 6 dB as expected for a finite Q of 70-130. The measurements agree very well with the simulations.

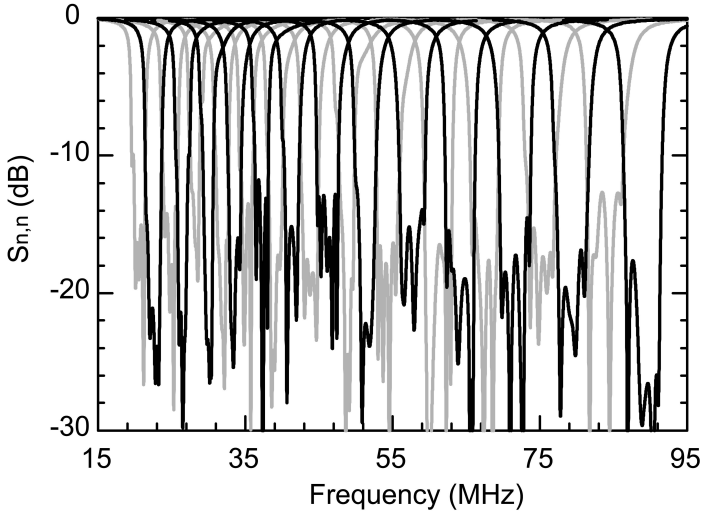
The micro-view of the transmission response and group delay of Ch.4 are shown in Fig. 2.13(a) along with the simulated response for a stand-alone tubular six-pole filter with the topology shown in Fig. 2.8. The channelizer response has slightly higher rejection and an altered phase response. The additional 0.1 μs group delay at the center of Ch.4 is due to the manifold. Since every filter in the cochlea-channelizer is located at a different position at the manifold, the additional group delay in each channel is proportional to the distance from the input port. The macro-view of the transmission response of Ch.22 with the simulated responses are shown in Fig. 2.13(b).

Measurements of $S_{n,m}$ for n$\neq$m are therefore performed to characterize the channelizer's channel-to-channel isolation. The measured response between channels 23 and 24, and channels 24 and 25, located on the opposite side of the manifold, is shown in Fig. 2.14(a). Each curve follows its corresponding filter's stopband skirts. This implies that the additional lower level "humps" present in every channel response are due to interactions with channels located on the same side of the manifold.

The measured isolation between channel 24 and adjacently-placed channels 26 and 22, located on same side of the manifold, is shown in Fig. 2.14(b). The curves show low-level EM coupling causes these additional humps on the transmission response due to the tight channel spacing with an average gap of 0.5 inches in the 26-channel channelizer design. The measured energy coupling through substrate is about -40 dB and this levels up the stopband response of the channel filter to -50 dB at these physical adjacent channels. Fig. 2.15 presents the measured isolation between Ch.24 (f_0 = 79 MHz) and



(a)



(b)

Figure 2.10: (a) Measured and simulated input return loss ($S_{0,0}$) of the 26-channel channelizer. (b) Measured output return loss ($S_{n,n}$) of each channel.

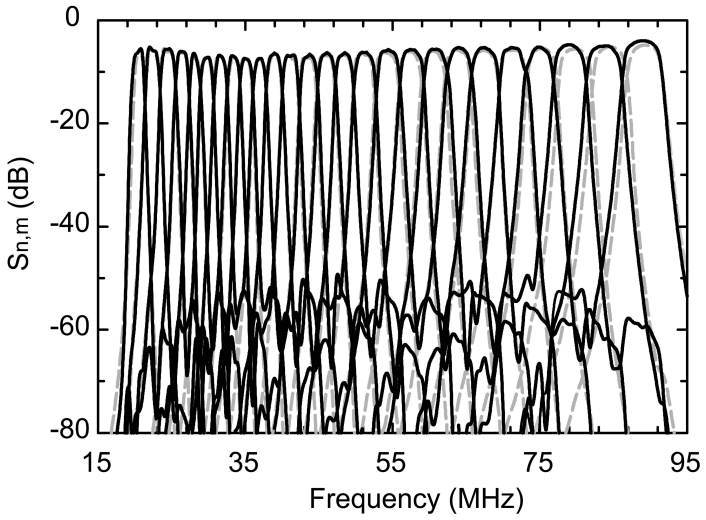


Figure 2.11: Measured (solid line) and simulated (dashed line) transmission response ($S_{n,0}$) of each channel.

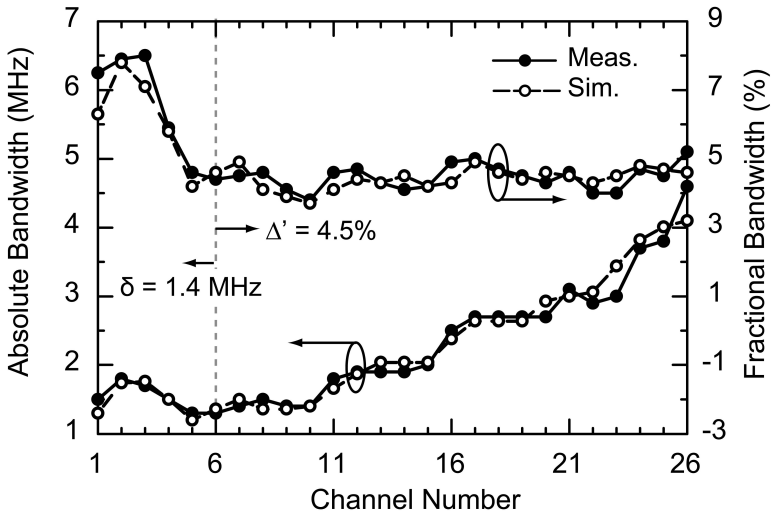
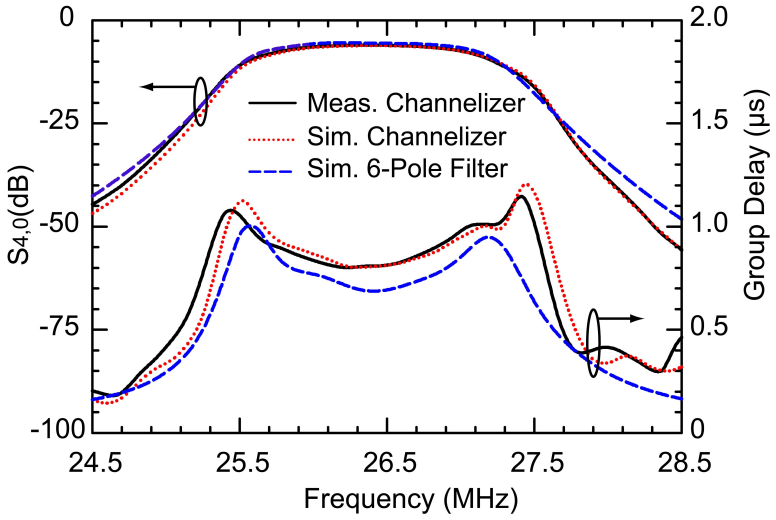
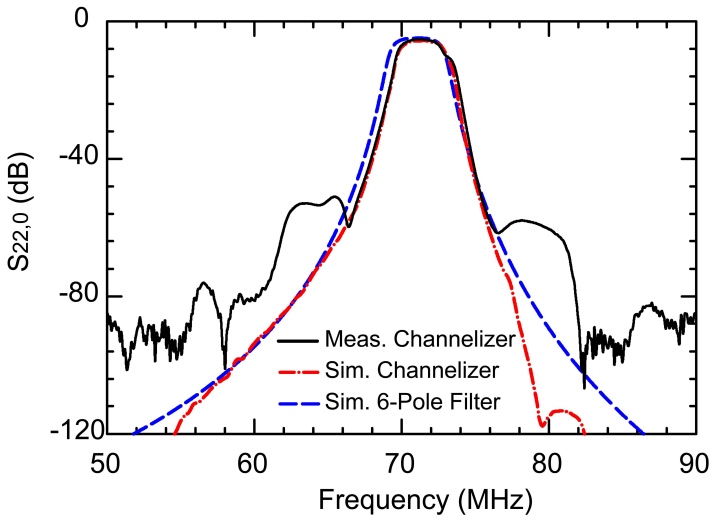


Figure 2.12: Measured and simulated results of the filter bandwidth of each channel compared with the initial design spec.

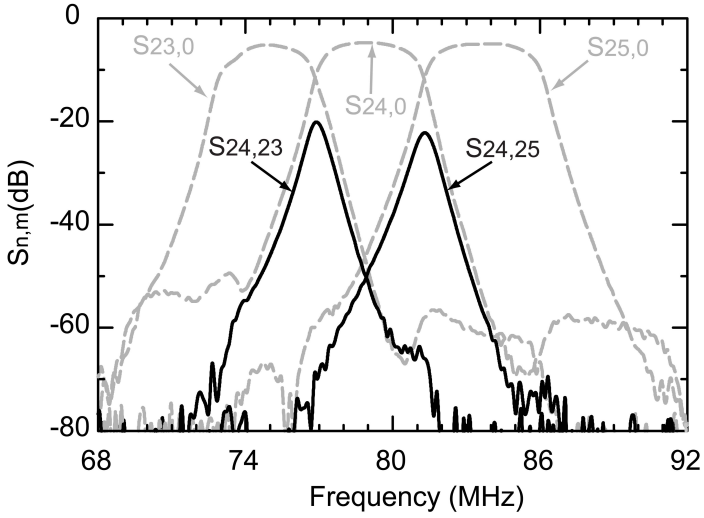


(a)

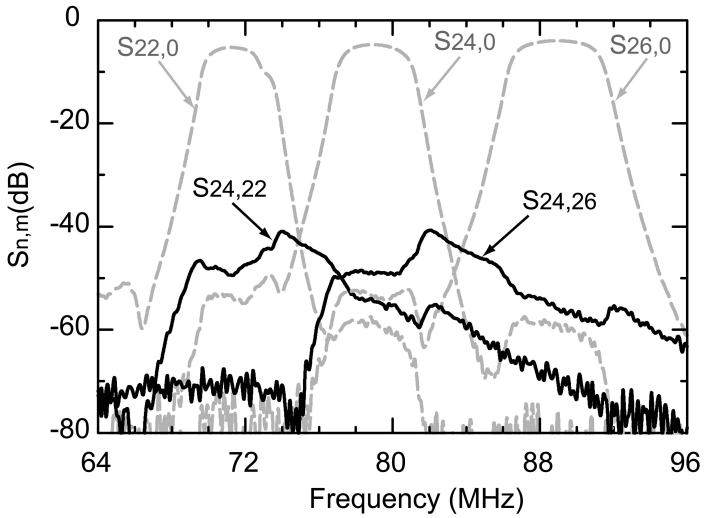


(b)

Figure 2.13: Transmission response and group delay of (a) Ch.4, and (b) Ch.22 of the 26-channel channelizer (simulated and measured) and the corresponding stand-alone 6-pole filter (simulated).



(a)



(b)

Figure 2.14: (a) Measured isolation of channel 24 between frequency adjacent channels (channels placed on opposite sides of the manifold). (b) Measured isolation of channel 24 between physically adjacent channels (channels placed on the same side of the manifold).

its neighboring channels.

The EM coupling is mainly through the substrate and the channel isolation can be improved by either providing metal housing to shield each channel or increasing the physical spacing between filters. An improved isolation design is demonstrated in section 2.4.

2.3.2 Power Handling

The power handling is limited by the the current carrying capacity of inductors in each channel and in the manifold. For $L_m(26)$ = 68 nH and I_{max} = 2.5 A_{rms} [36], the maximum power which can pass in the manifold is 200 W. The manifold has a loss of 0.1-0.5 dB at 90-20 MHz and therefore there are no thermal considerations. The 6-pole filters have lower power ratings due to the narrowband response of each channel. For L = 222, 422, 538 nH with corresponding I_{max} = 3, 2.5, 2 A_{rms} [37], the power handling is 63, 40, 28 W, respectively. Measurements done on Ch.20 (implemented with L = 222 nH) show that prolonged operation ($>$1 hr) with 50 W of input power is possible with no degradations (Fig. 2.16).

2.3.3 Back-to-Back Cascaded Measurement

Measurement of the two 26-channel channelizers cascaded together are performed to compare the yield rate of the channelizers implemented with $\pm 2\%$ error tolerance lumped components. The cascaded response of Ch.7 is measured through the input ports of 2 channelizers by connecting Ch.7 of each circuit together and terminating the rest of the output ports with 50 Ω loads. The measured result is shown in Fig. 2.17(a) and, with excellent agreement of the 2 channelizers, the filter performance is equivalent to a 12^{th} order bandpass filter. The back-to-back channelizer response is plotted in Fig. 2.17(b) and shows the performance of a wide-band signal first being subdivided into 26 smaller channels by channelizer 1 and then these narrower signals being collected and combined back again through channelizer 2.

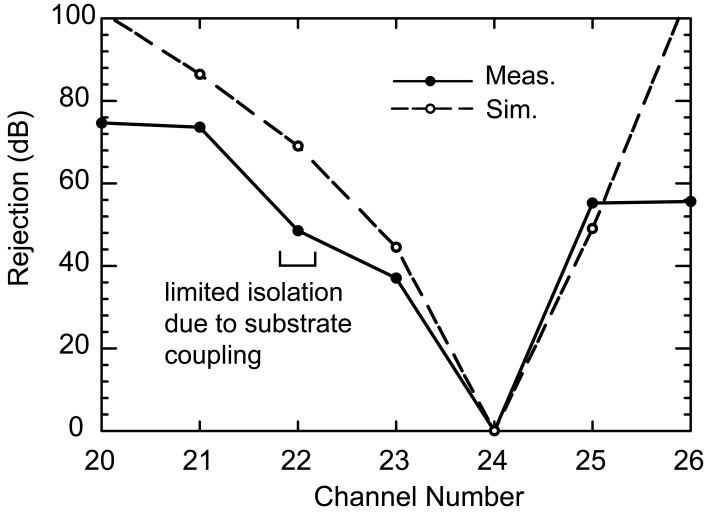


Figure 2.15: Measured and simulated channel-to-channel rejection of Ch.24 (f_0 = 79 MHz) between other channels.

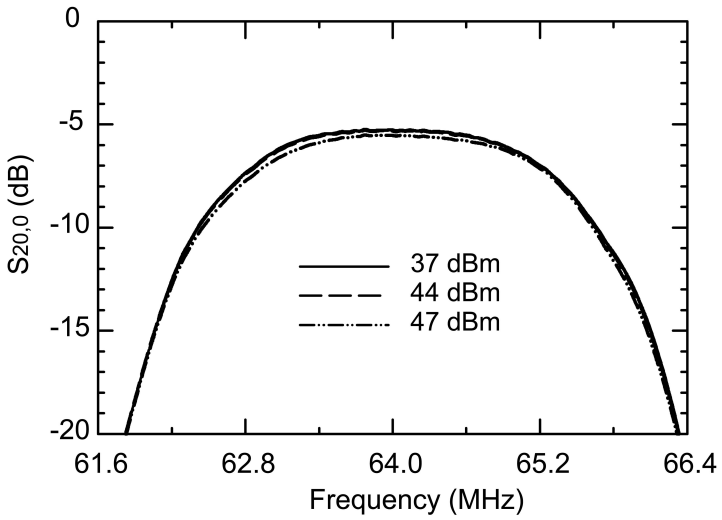
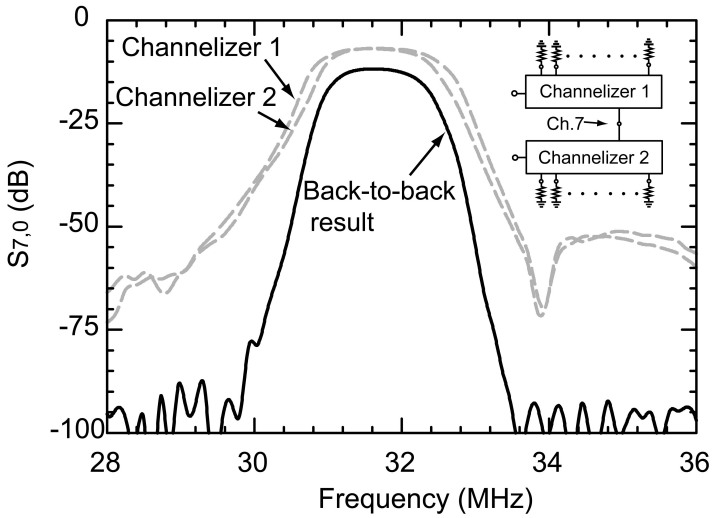


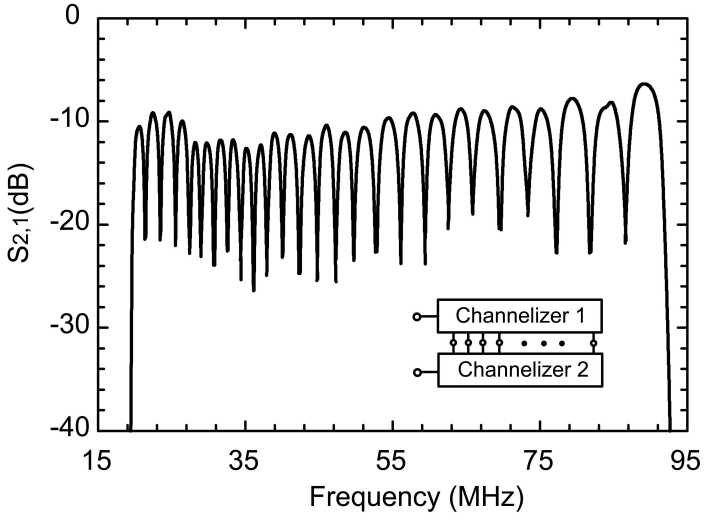
Figure 2.16: Measured power handling for Ch.20 under input signal at 5, 25, and 50 W power levels.

Table 2.1: Measured frequency characteristics of the two 26-channel cochlear-based channelizers

Ch	f_n (MHz)	I.L. (dB)	Δ_{3dB} (%)	Iso.(n+1) (dB)	Iso.(n-1) (dB)
26	88.9	4.0 (4.1)	5.2 (4.9)	NA	35.3 (34.6)
25	84.2	5.0 (4.3)	4.5 (5.0)	49.0 (40.1)	39.5 (41.3)
24	79.1	4.7 (4.7)	4.7 (4.8)	55.1 (55.4)	37.4 (40.6)
23	74.9	5.2 (5.1)	4.0 (4.5)	45.0 (48.8)	35.6 (35.4)
22	71.2	5.3 (5.2)	4.0 (4.3)	36.6 (39.0)	41.9 (43.8)
21	67.4	5.3 (5.3)	4.6 (4.6)	48.4 (50.5)	35.1 (34.0)
20	63.9	5.3 (5.4)	4.3 (4.2)	39.0 (32.2)	37.5 (35.3)
19	60.6	5.5 (5.5)	4.5 (4.6)	36.0 (36.4)	35.9 (39.6)
18	57.8	5.6 (5.5)	4.7 (4.7)	39.2 (41.2)	36.6 (38.6)
17	54.4	5.7 (5.7)	5.0 (4.8)	45.3 (45.0)	44.2 (44.1)
16	51.1	6.1 (6.4)	4.9 (4.9)	51.1 (53.5)	37.6 (33.9)
15	48.5	6.3 (6.5)	4.2 (3.9)	42.3 (39.0)	38.6 (44.3)
14	46.0	6.3 (6.1)	4.1 (4.3)	37.4 (44.6)	38.9 (36.6)
13	43.6	6.6 (6.7)	4.3 (4.3)	41.2 (42.0)	46.5 (42.3)
12	41.0	6.7 (6.7)	4.7 (4.4)	47.5 (46.3)	36.9 (35.3)
11	39.0	6.4 (6.6)	4.6 (3.8)	35.8 (35.6)	33.3 (34.4)
10	37.1	7.4 (6.9)	3.8 (3.8)	42.7 (35.5)	38.1 (35.1)
9	35.0	7.1 (7.2)	4.1 (3.7)	41.6 (40.2)	38.2 (37.1)
8	33.2	6.8 (6.9)	4.6 (3.9)	32.9 (37.2)	35.9 (39.0)
7	31.6	6.9 (6.8)	4.5 (4.4)	34.1 (34.6)	37.2 (39.9)
6	29.8	7.0 (7.1)	4.4 (5.0)	42.1 (39.2)	35.5 (33.9)
5	28.1	6.9 (7.1)	4.6 (4.6)	37.4 (39.2)	43.4 (40.3)
4	26.3	6.0 (6.0)	5.9 (6.0)	36.2 (36.6)	37.8 (39.9)
3	24.6	5.5 (5.5)	8.0 (7.3)	34.0 (38.1)	40.3 (40.0)
2	22.4	5.7 (5.6)	7.9 (7.2)	49.3 (42.9)	38.0 (40.0)
1	20.5	5.9 (6.4)	7.5 (7.6)	52.3 (46.9)	NA



(a)



(b)

Figure 2.17: Measured back-to-back transmission responses of (a) Ch.7, (b) the 2 cascaded channelizers.

2.4 Improved Isolation Design

A simplified 7-channel channelizer (N = 7) is designed with a constant δ = 5 MHz at 60-90 MHz and is shown in Fig. 2.18. Each channel filter is designed with a 6^{th}-order bandpass filter response and a $\sim$40 dB channel-to-channel isolation. However, the physical channel spacing is increased to 2 inches to reduce the EM coupling between physically adjacent channels. This is done by using longer transmission line sections (38 mm) in the manifold and the total board size is 15 inches $\times$15 inches.

Fig. 2.19 presents the measured and simulated S-parameters of the 7-channel channelizer. The channels have an average 3-dB absolute bandwidth of 4.5 MHz from 90 MHz to 60 MHz. The insertion loss varies between 3.5 dB and 4.1 dB.

Fig. 2.20 presents detailed mutual coupling measurements on Ch.7 and Ch.1 versus the other channels. The isolation to other channels closely follows the stopband skirts of a particular channel filter. In this case, the coupling between the different channels is mostly through the inductive manifold, and the energy leakage through the substrate is minimized.

Fig. 2.21 presents the measured and simulated transmission responses of Ch.5. Compared with Fig. 2.13(b) which both channel filters are with the same f_0 = 70 MHz, the additional hump level on both sides of the filter stopband is as improved from -50 dB to -80 dB by increasing the channel physical spacing. Fig. 2.22 summaries the channel-to-channel isolation of Ch.5.

2.5 Summary

This chapter presents a 26-channel channelizer based on the mammalian cochlea and a 7-channel improved mutual coupling channelizer design. A 6-pole response is synthesized in each channel, and results in $\sim$40 dB isolation between adjacent channels. The design is scalable and can be extended to cover 20-3000 MHz for wideband EW applications.

Chapter 2 is mostly a reprint of the material as it appears in IEEE MTT-S International Microwave Symposium Digest, 2010. Yu-Chin Ou and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

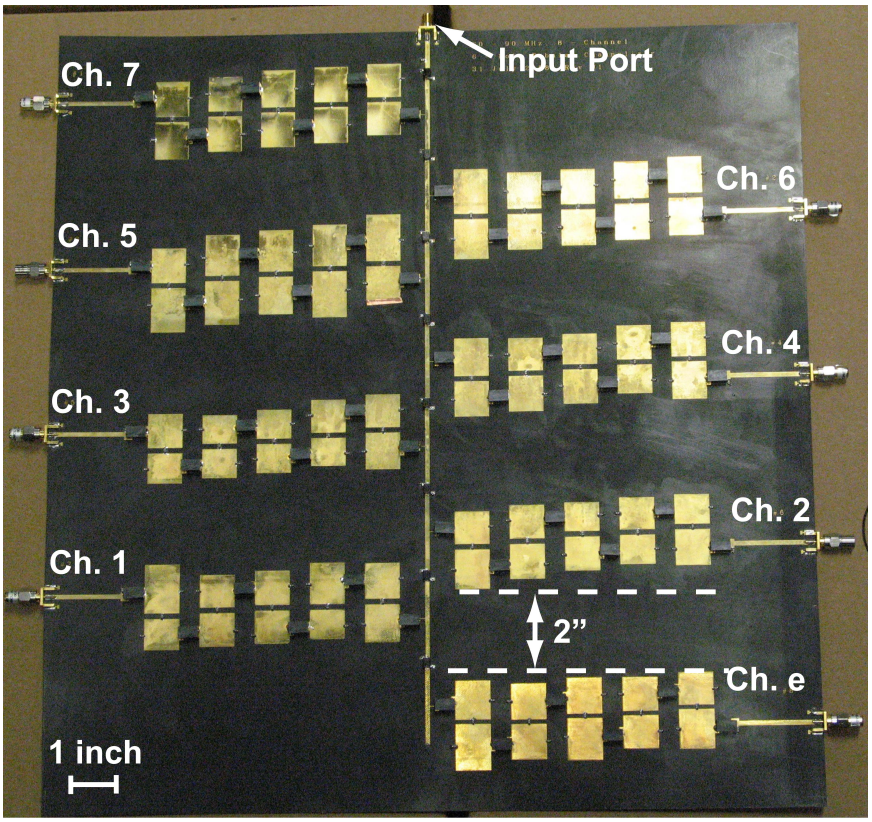
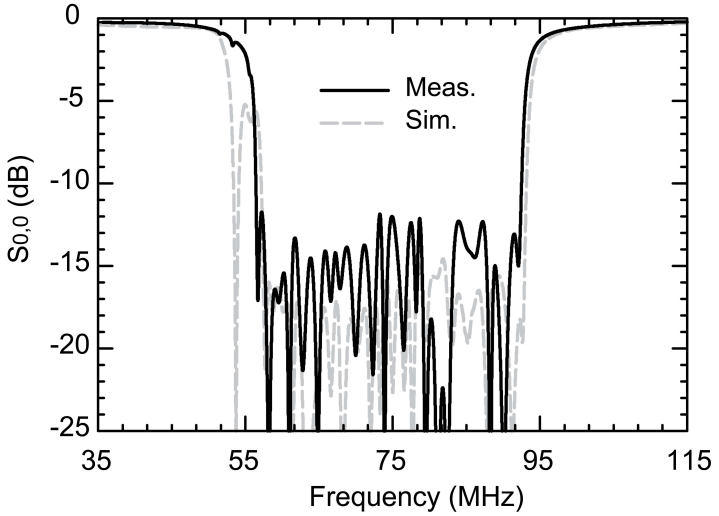
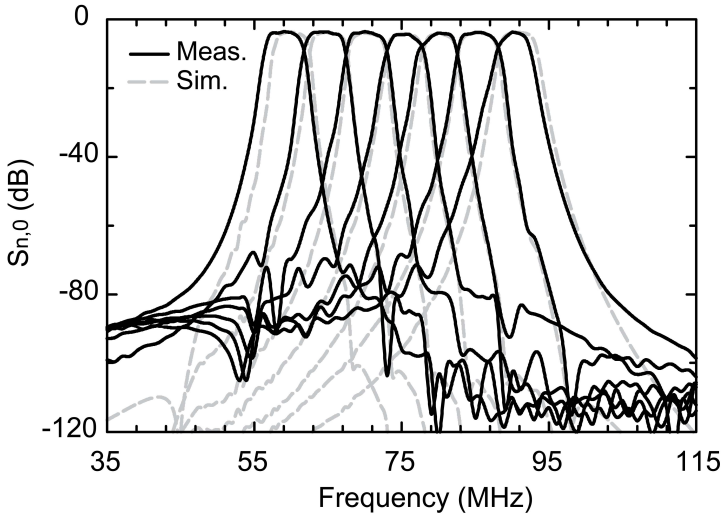


Figure 2.18: Photograph of the 60-90 MHz 7-channel channelizer and its corresponding ports ($15'' \times 15''$).

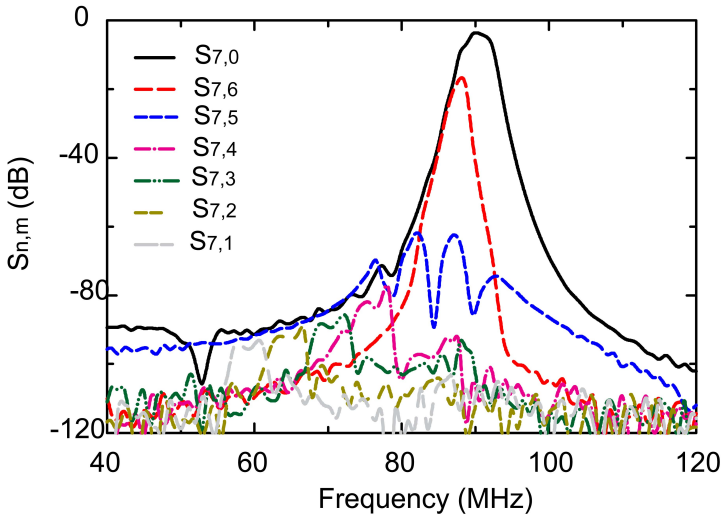


(a)

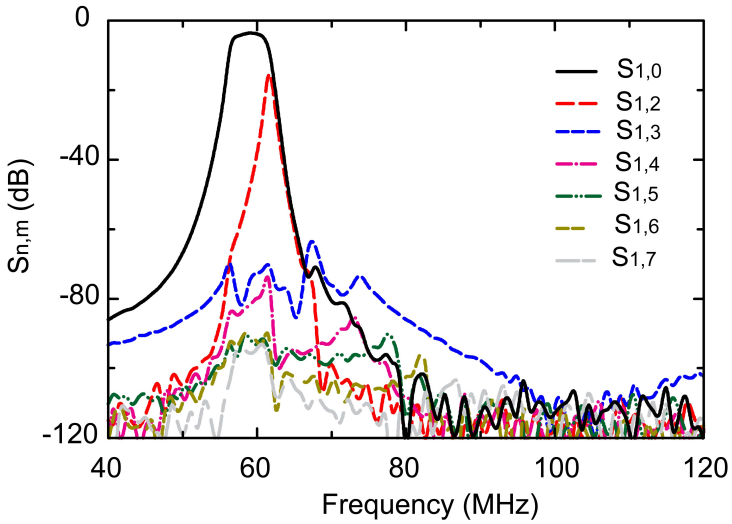


(b)

Figure 2.19: (a) Measured and simulated (a) input return loss ($S_{0,0}$), and (b) transmission response ($S_{n,0}$) of each channel in the 7-channel channelizer.



(a)



(b)

Figure 2.20: (a) Measured isolation between Ch.7 and other channels. (b) Measured isolation between Ch.1 and other channels.

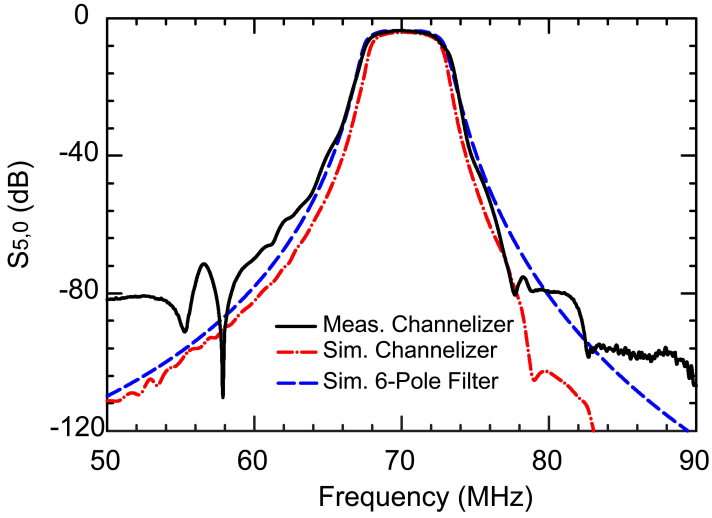


Figure 2.21: Transmission response of Ch.5 of the 7-channel channelizer (simulated and measured) and the corresponding stand-alone 6-pole filter (simulated).

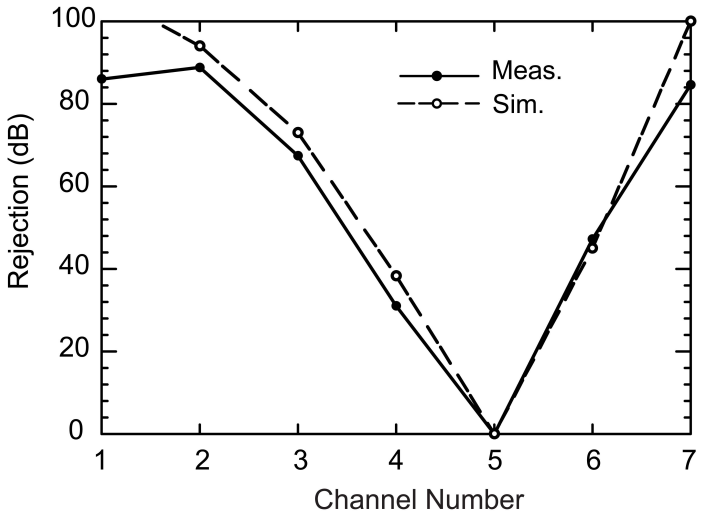


Figure 2.22: Measured and simulated channel-to-channel rejection between Ch.5 (f_0 = 76 MHz) and other channels.

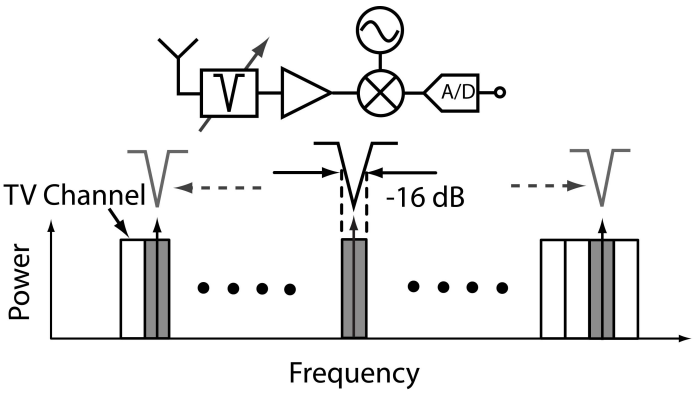
Chapter 3

Lumped-Element Fully Tunable Bandstop Filters for Cognitive Radio Applications

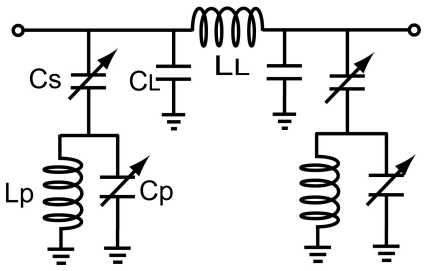
3.1 Introduction

Cognitive radios have the potential to improve the efficiency of spectrum deployment by using frequency agile and dynamic frequency-selecting front-end receivers [10] [38]. The operation principle of a cognitive radio circuit is to detect a particular spectrum which is currently in use and immediately switch to an unused spectrum without interfering with the authorized users. The recent release of the TV white space makes the UHF band (512-698 MHz) a popular choice for cognitive radio applications with constant channel bandwidth in the TV spectrum. However, due to the large number of potential transmitters in this band and due to the third-order Intermodulation products in the front-end elements, it is important to use low-loss tunable bandstop filters to reduce the out-of-band interference signals (see Fig. 3.1(a)). The reconfigurable bandstop filter should provide a minimum rejection of -16 dB for a bandwidth of 5 MHz to notch out the entire TV channel. This requires a tunable notch filter with decreasing fractional bandwidth (8.1-5.8%) as the filter is tuned from 500 MHz to 700 MHz.

In this chapter, we present fully tunable lumped-element bandstop filters cover-



(a)



(b)

Figure 3.1: (a) Tunable bandstop filter specification for cognitive radio application. (b) Lumped-element model for a two-pole tunable bandstop filter.

ing 500-700 MHz (Fig. 3.1(b)). Unlike distributed microwave filters based on coupled-lines to control filter bandwidth versus center frequency [15,39,40], the lumped-element filters use variable capacitors to achieve both frequency and bandwidth control. In this work, two different tunable filters are implemented: one with single varactor diodes and the other with back-to-back diodes. A nonlinear study of the tunable filters is also done, and the measured power handling and intermodulation products are presented in both cases. The cascaded performance of the two filters are presented and show high rejection in the 500-700 MHz band.

3.2 Filter Design

3.2.1 Synthesis

The lumped-element filter synthesis procedure starts with a standard two-pole Chebyshev low-pass ladder network [11] with immittance inverters inserted to convert a series inductance into an equivalent circuit with shunt capacitance (Fig. 3.2(a)). Next, the inverter and the load conductance are combined together to result in a symmetrical network with resistive terminations. Fig. 3.2(b) is then obtained by applying the bandstop transformation, and the element values are calculated from [41]:

$$J_{12} = \frac{Z_0}{\sqrt{g_0 g_3}} \tag{3.1}$$

$$C_{BS} = \frac{\Delta g_1}{\omega_0 Z_0} \tag{3.2}$$

$$L_{BS} = \frac{Z_0}{\omega_0 \Delta g_1} \tag{3.3}$$

where ω_0 is the bandstop filter center frequency, Δ is the fractional bandwidth, Z_0 is the characteristic impedance, and g_0-g_3 are element values from the low-pass prototype filter. This bandstop prototype is not appropriate for filter implementation due to the fact that shunt resonator branch always results in physically un-realizable inductance and capacitance values especially for narrow bandwidth applications. Therefore, additional immittance inverters, J_s, are introduced to provide an arbitrary scaling factor to produce

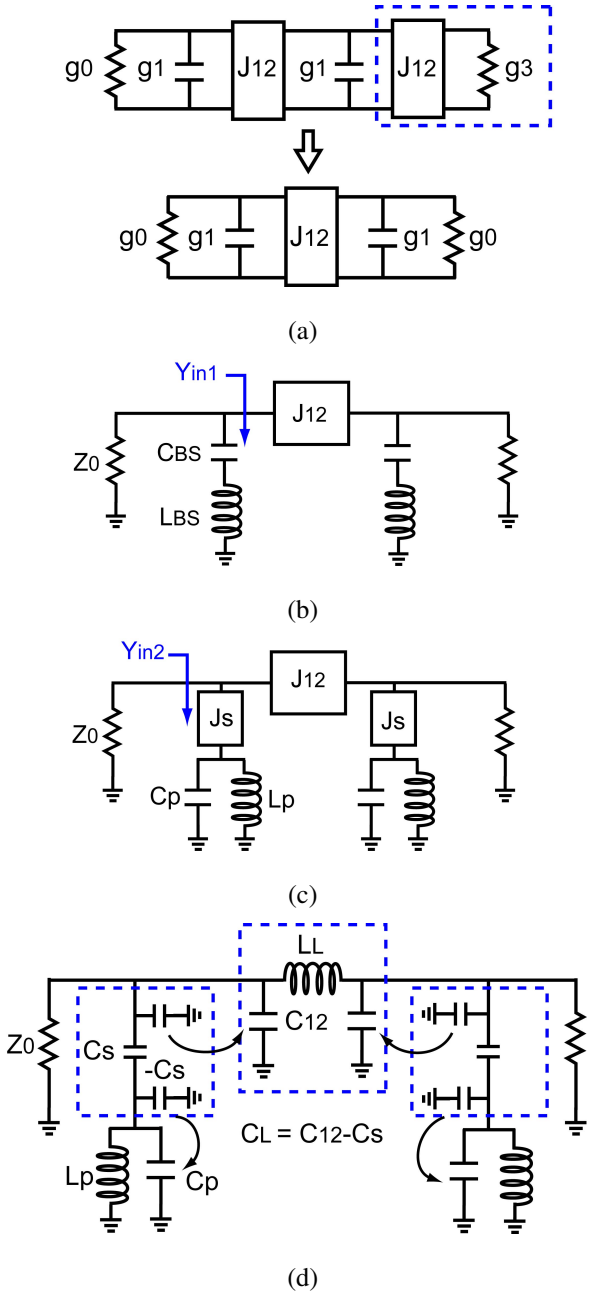


Figure 3.2: (a) Standard 2-pole lowpass prototype. (b) Transformed 2-pole bandstop filter. (c) Inserting the scaling inverters and transforming to shunt L_pC_p resonator. (d) Practical inverter realization using lumped-element equivalent circuits.

realizable component values, and as a result, this transforms the series resonator into a shunt LC resonator (see Fig. 3.2(c)). The values of the LC resonator can be found by solving the equation $Y_{in1} = Y_{in2}$ and

$$L_p = \frac{C_{BS}}{J_s^2} \tag{3.4}$$

$$C_p = L_{BS} J_s^2 \tag{3.5}$$

The J-inverter, J_{12}, connecting the input and output ports is realized using a lumped-element (L_L, C_{12}) circuit and is equivalent to a quarter-wave transmission line. The scaling inverter, J_s, is implemented with an equivalent π-model circuit of capacitances of C_s and $-C_s$, and the negative capacitors are absorbed into C_p and C_{12} (Fig. 3.2(d)). This results in

$$L_L = J_{12}/\omega_0 \tag{3.6}$$

$$C_{12} = 1/J_{12}\omega_0 \tag{3.7}$$

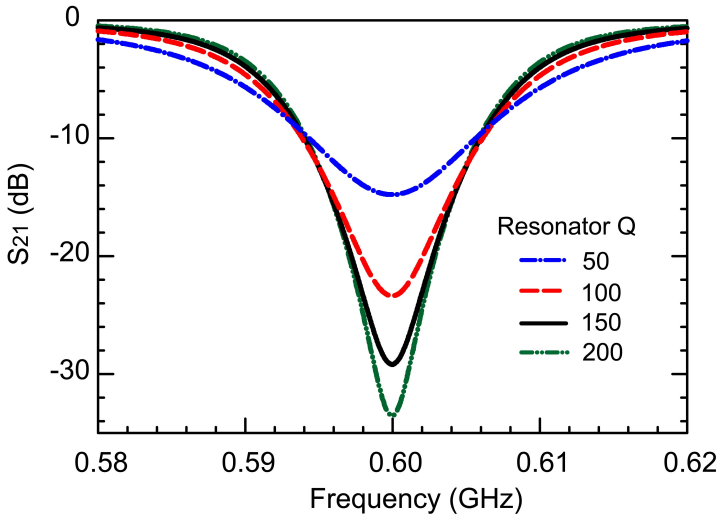
$$C_s = \frac{J_s}{\omega_0} \tag{3.8}$$

The scaling factor, J_s, is obtained by pre-setting L_p (or C_p) to be a physically realizable component value. As a result and using (3.1)-(3.8) and the values of C_s, C_p, L_L, and C_L can be calculated based on ω_0, Z_0, L_p and g_0-g_3 for a specific frequency. The closed-form equations for the lumped elements of the bandstop filter of Fig. 3.1(b) are therefore:

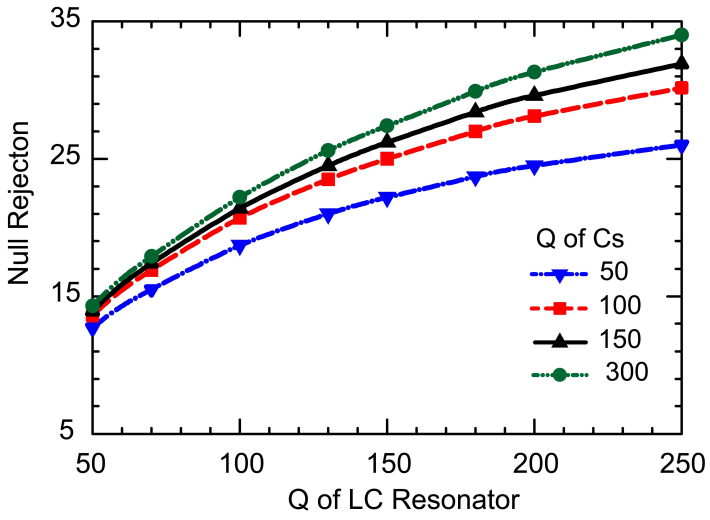
$$C_s = \sqrt{\frac{\Delta g_1}{L_p Z_0 \omega_0^3}} \tag{3.9}$$

$$C_p = \frac{1}{\omega_0^2 L_p} - C_s \tag{3.10}$$

$$L_L = \frac{Z_0}{\omega_0 \sqrt{g_0 g3}} \tag{3.11}$$



(a)



(b)

Figure 3.3: (a) Simulated passband response and null of a standard 2-pole bandstop filter vs. resonator Q. (b) Simulated null rejection of the proposed 2-pole bandstop filter vs. Q of the C_s and LC resonator.

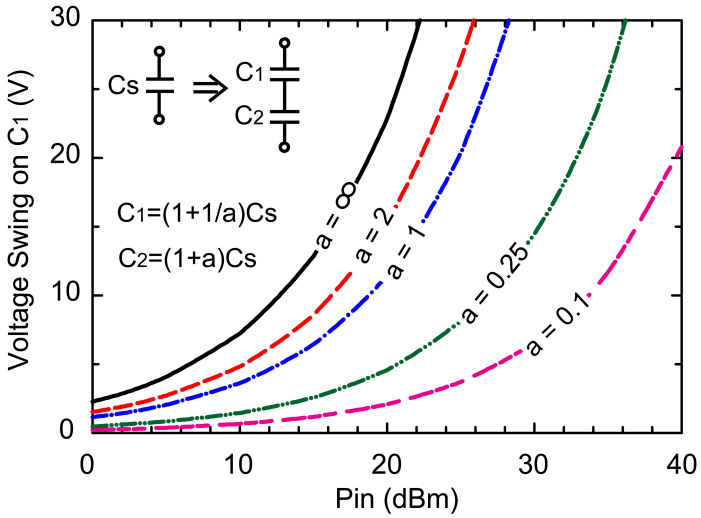


Figure 3.4: Simulate RF voltage swing across the decomposed capacitor vs. input power.

$$C_L = \frac{\sqrt{g_0 g_3}}{Z_0 \omega_0} - C_s \tag{3.12}$$

3.2.2 Effect of Q on Filter Response

The filter null rejection level is highly dependent on the resonator Q (50∼200) [32] but, on the other hand, the 10-dB and 20-dB rejection bandwidths are not highly dependent on Q as shown in Fig. 3.3(a). The effect of the finite component Q on the proposed topology is presented in Fig. 3.3(b), and it is seen that the Q of L_pC_p has a much larger effect on the null rejection than the Q of C_s.

3.2.3 RF Voltage Swing

Smaller portion of RF voltage swing across a capacitor can be obtained by factoring a capacitor into combinations of multiple capacitors in series. Fig. 3.4 presents the simulated input power vs. voltage swing across one of the decomposed capacitors, C_1, with different decomposition ratio a. For example, under the same voltage swing level, a 6 dB improvement in input power is obtained with $a = 1$ (half voltage drop across C_1) compared with the original non-decomposed capacitance ($a = \infty$).

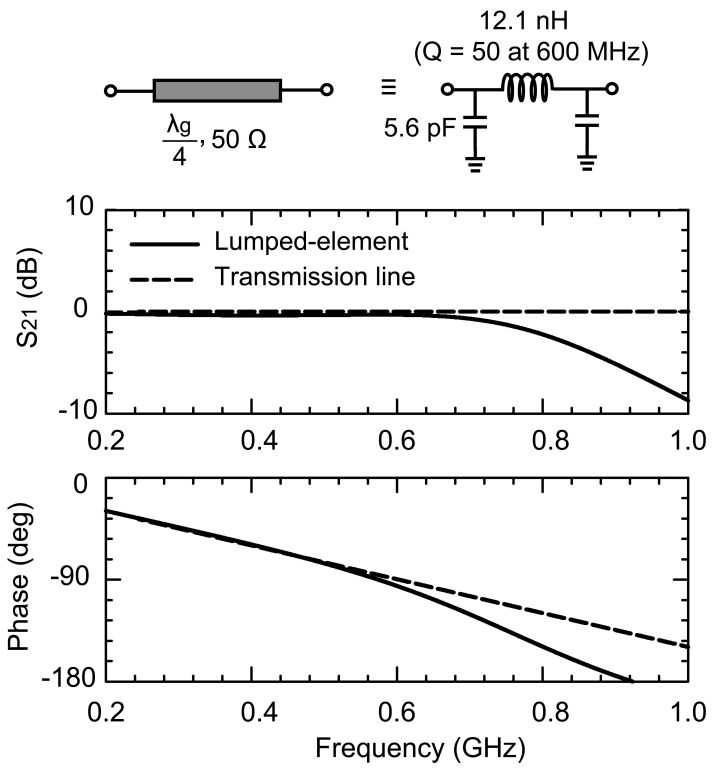
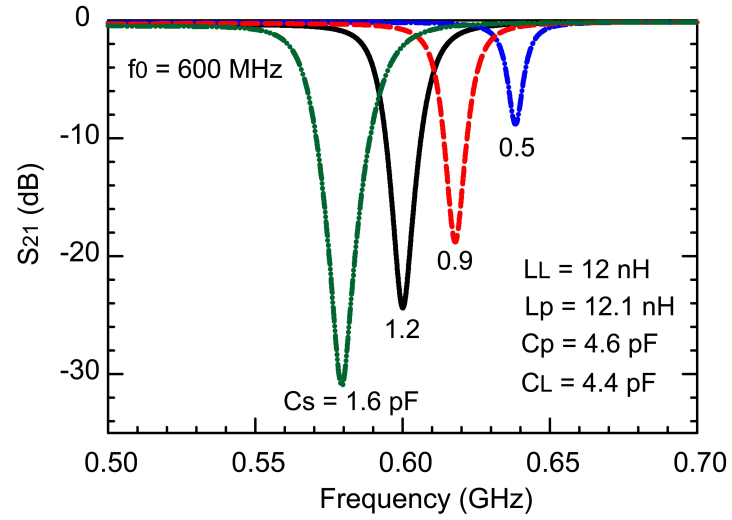


Figure 3.5: Lumped-element equivalent circuit of a quarter-wave microstrip line and simulated amplitude and phase vs. frequency.

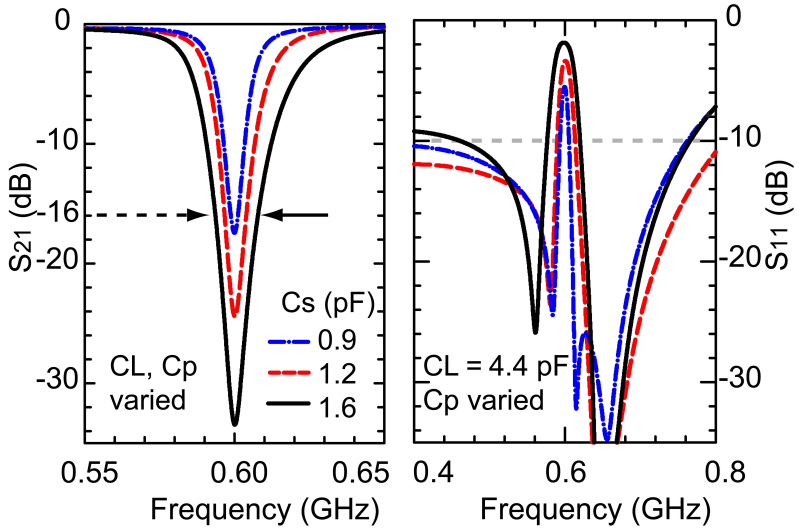
3.2.4 Lumped Inverters

Fig. 3.5 presents the comparison of an ideal quarter-wave transmission line and its lumped equivalent circuit. The π-model is a 3^{rd}-order lowpass filter which limits the bandstop filter usable passband bandwidth to $\sim$750 MHz with a 0.5 dB loss. A C-L-C-L-C (C = 3.3 pF, L = 7 nH) multi-section inverter could be used to extend the inverter bandwidth to 900 MHz.

The filter bandwidth is mostly controlled by C_s, and Fig. 3.6(a) presents the simulated filter tuning performance of C_s with a fixed C_p and C_L (filter Q = 100). The filter is originally designed at f_0 = 600 MHz with a L_p = 12.1 nH and C_p = 1.2 pF. Since the negative capacitance of the lumped scaling inverter ($-C_s$) is absorbed by C_{12} and C_p, any increase in C_s results in a higher effective C_p, but since C_p is fixed in the simulation, this results in a lower resonant frequency.



(a)



(b) (c)

Figure 3.6: (a) Simulated tuning performance vs. C_s for the bandstop filter, simulated filter bandwidth tuning performance (b) with and (c) without C_L varied with C_s.

When C_p and C_L are varied in each state to take into account the different values of $-C_s$, the filter f_0 remains unchanged at 600 MHz while different 16 dB rejection bandwidth tuning performance (14, 7, 2.5 MHz) is simulated and shown in Fig. 3.6(b). This topology also allows frequency and bandwidth control with varying C_s and C_p only and a fixed C_L. In this case, a tunable bandwidth notch response is still achieved as in Fig. 3.6(b) but with an $S_{11} >$ -10 dB at $f < 500$ MHz and $f > 700$ MHz (Fig. 3.6(c)).

3.3 Fixed Frequency Filter

A fixed two-pole 600 MHz bandstop filter is first designed and implemented on a 0.787-mm-thick Duroid substrate (ε_r = 2.2, Roger RT/Duroid 5880) with 53.3-μm-thick copper layers on both sides and 0.25-mm-diameter plated thru-hole vias. The simulation is done in Agilent ADS with circuit models from Modelithics CLR Library [35]. The SMT models of commercially available inductors and capacitors include the component pads and body parasitic capacitance to ground, and these parasitic capacitances are absorbed into nearby shunt capacitances which reduces the component values. High-Q Coilcraft square air-coil inductors (L_p) [42], Coilcraft 0402 chip inductors (L_L) [43], and Murata 0402 GRM ceramic capacitors are used, all with 2% or better tolerance. The component values are listed in Table 3.1.

The filter is measured using an Agilent E5071B network analyzer with the reference planes defined at the SMA connectors. The simulated and measured center frequency are shown in Fig. 3.7 with f_0 = 614 MHz, a 16-dB rejection bandwidth of 5.5 MHz, and a fixed filter resonator Q of 135. The insertion loss is 0.2-0.3 dB in the passband frequencies (the passband is defined as f_0-40 MHz and f_0+40 MHz).

Table 3.1: Lumped component values and the corresponding Q at 600 MHz of the fixed bandstop filter

Comp.	L_L	C_L	C_s	L_r	C_r
Value	12 nH	4 pF	1 pF	12.1 pF	4 pF
Q	50	> 300	> 300	150	> 300

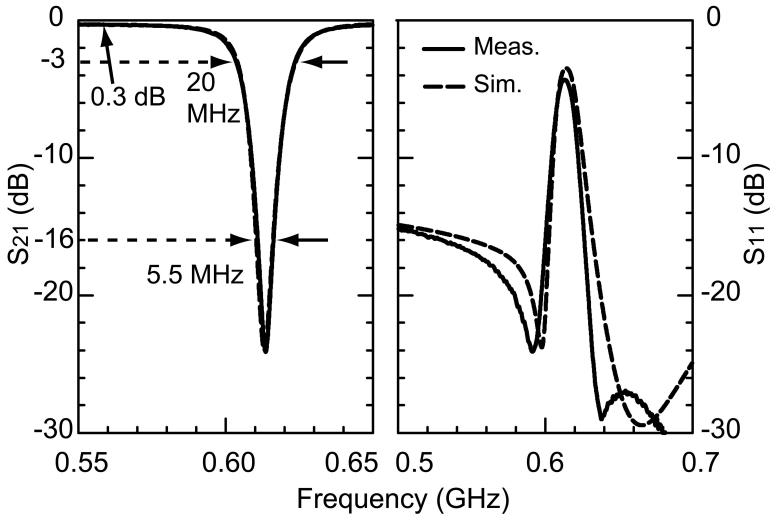


Figure 3.7: Measured and simulated S-parameters of the fixed frequency bandstop filter of -16 dB rejection for 5 MHz bandwidth performance.

3.4 Tunable Bandstop Filters

3.4.1 Tunable Filter with Single Varactor Diodes

Fig. (3.8) shows the fabricated single-diode tunable filter with dimension 9×9 mm^2. The filter was designed based on Lp = 16.6 nH with a Q = 150 at 600 MHz. Silicon abrupt junction diodes SMV1405 [44] (C_j = 2.9 pF, n = 0.47, R_s = 0.8 Ω) are used for the tunable scaling inverters, $D_1 \& D_2$, and result in 1.58-0.76 pF when placed in series with a fixed 5 pF DC-block capacitor. SMV1413 (C_j = 9.2 pF, n = 0.45, R_s = 0.35 Ω) are used for the tunable resonator capacitors, D_3 and D_4, with C_p = 4.7-2.3 pF for V_b = 4 to 30 V (Q = 200-340) at 500-700 MHz. Two short sections of trapezoid transmission lines are used for the filter terminals to 50 Ω microstrip lines with negligible effects (length is electrically small compared to the guided wavelength). The DC biasing is done using two 100 kΩ resistors connected in series to reduce the RF-signal leakage in the bias network.

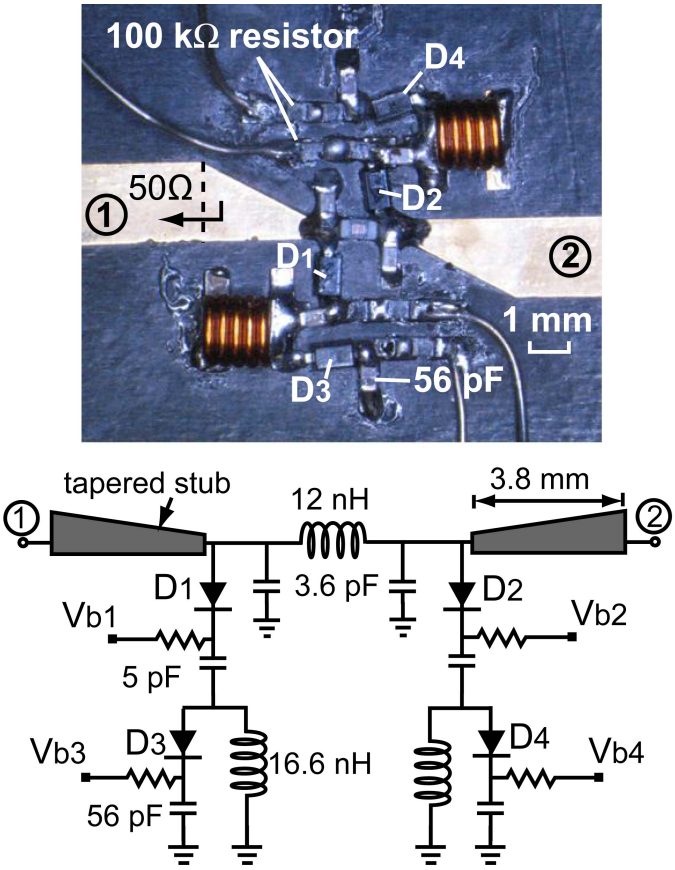


Figure 3.8: Picture and schematic of the single-diode tunable filter on a Duroid substrate (ε_r = 2.2, 0.787-mm substrate thickness) with bias circuits.

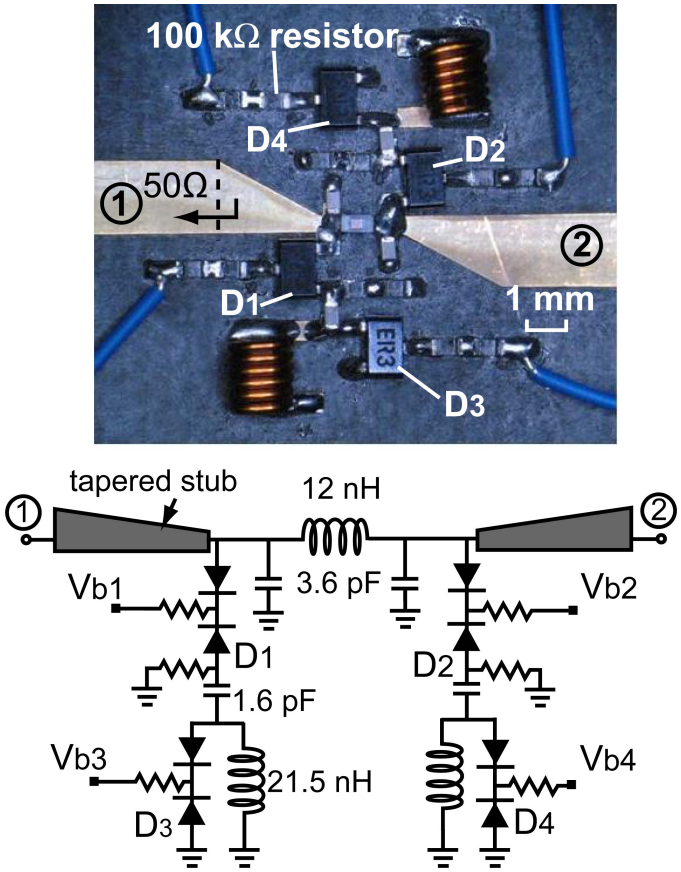


Figure 3.9: Picture and schematic of the back-to-back diode tunable filter on a Duroid substrate (ε_r = 2.2, 0.787-mm substrate thickness) with bias circuits.

3.4.2 Tunable Filter with Back-to-Back Varactor Diodes

The fabricated tunable filter with back-to-back diodes, designed with L_p = 21.5 nH (Q = 150 at 600 MHz) and of dimensions 8×11 mm^2 is shown in Fig. 3.9. The tuning was implemented using varactor diodes SMV1413 (2 diodes per package) for all tunable capacitors (D_1-D_4). The diode results in C_p = 0.9-4.6 pF for V_b = 1-30 V. Similarly, two series 100 kΩ resistors are used for DC biasing and a 1.6 pF capacitor is placed in series with the inverter diode for DC bias separation and higher power handling ability.

3.4.3 Measurements

Excellent agreement between measurements and simulations is obtained for both tunable filters (Fig. 3.10). The measured 16-dB rejection S-parameters for the tunable filters are shown in Fig. 3.11. The single-diode filter covers 0.47-0.72 GHz and the back-to-back diode filter covers 0.51-0.75 GHz both with an average passband insertion loss of 0.3-0.5 dB. The passband loss is mostly determined by the chip inductor L_L (Q = $\sim$50). The overall filter Q is fitted using the insertion loss response in ADS and results in 52-65 for the single-diode and 68-75 for the back-to-back diode filters respectively at 500-700 MHz.

Due to over-estimated body parasitic capacitance from the back-to-back diode package, the back-to-back diode filter response is slightly shifted to higher frequencies and this is compensated using a lower bias voltage (Fig. 3.12). Fig. 3.13 summarizes the filter performance with 16 dB rejection. The constant 1.5-2 MHz 20-dB rejection of both filters is presented in Fig. 3.14 and demonstrates the tuning capability of this topology.

3.5 Non-Linear Measurements

The nonlinear behavior of these filters is due to the large voltage swing across the silicon varactors and is contributed mostly by the resonator varactors, D_3 and D_4. At resonance, the shunt L-C tanks behave as open circuits with high impedance and have $\sim$90% of the voltage at node 1. On the other hand, the inverter varactors, D_1 and D_2,

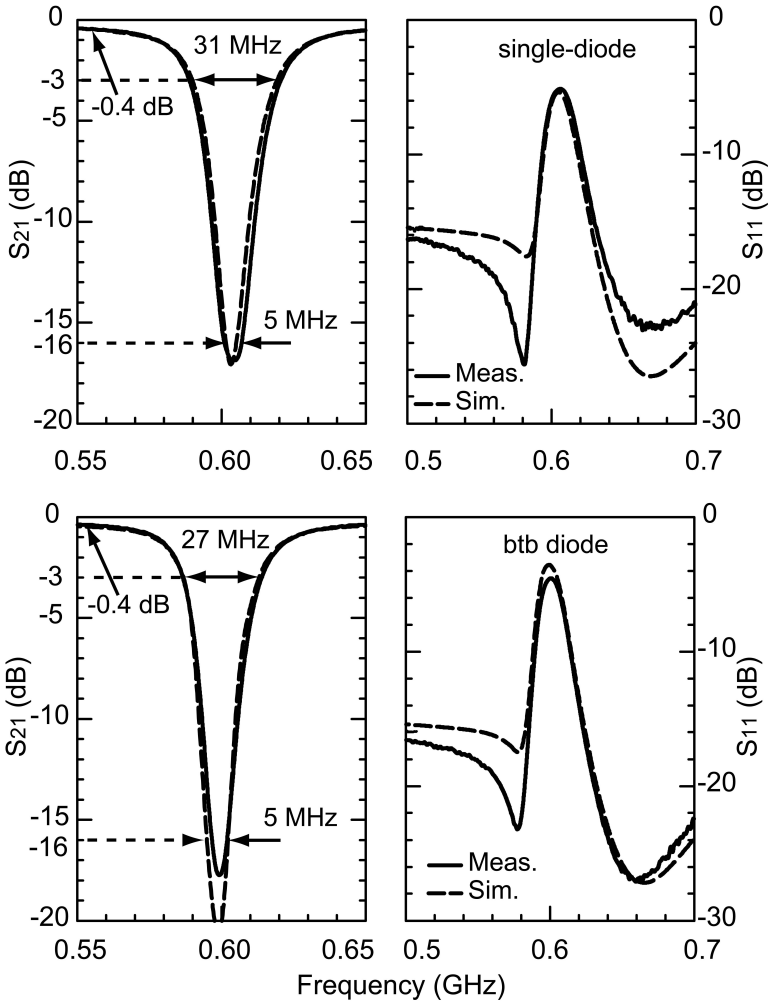


Figure 3.10: Measured and simulated S-parameters of the tunable bandstop filters with a rejection of 16 dB at a 5 MHz bandwidth.

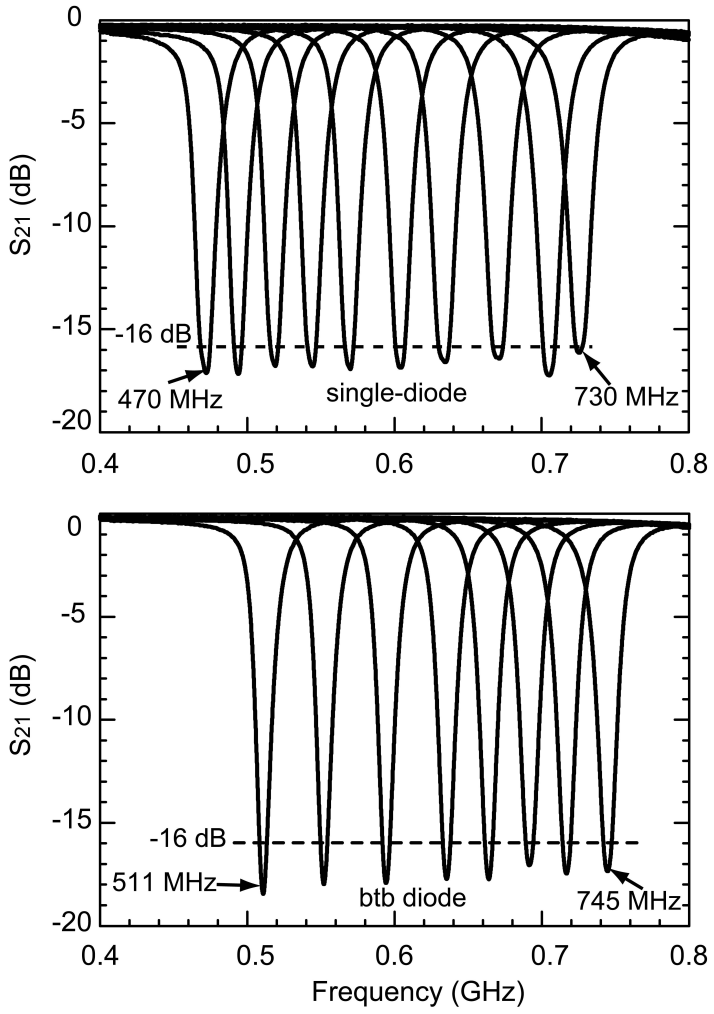


Figure 3.11: Measured S-parameters of the single-diode and back-to-back diode tunable bandstop filters for a constant 5 MHz with a rejection of 16 dB.

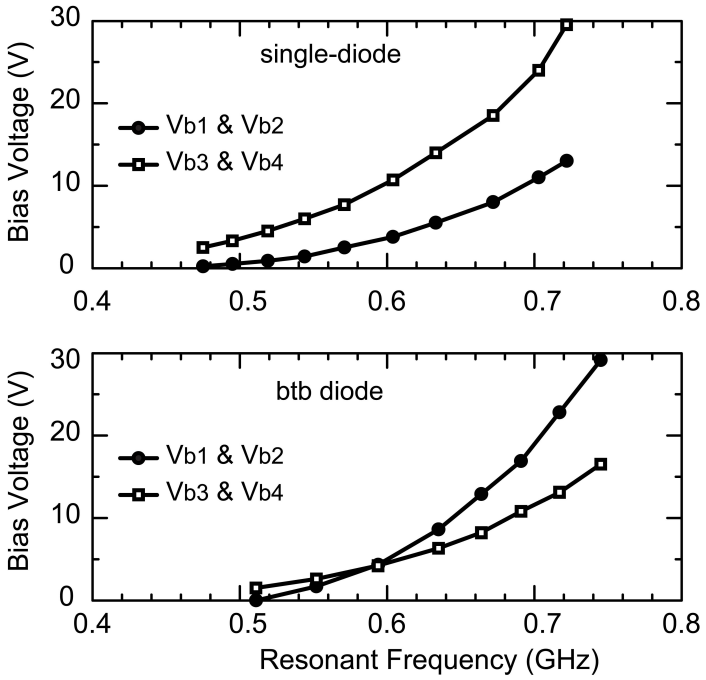


Figure 3.12: Bias voltage on each diode in the single-diode and back-to-back diode tunable bandstop filters.

have virtually no contribution to the overall nonlinear performance. The measured and simulated third-order-intermodulation intercept point (IIP_3) for the single and back-to-back diode tunable filters are shown in Fig. 3.15 with Δf = 2 MHz under different bias voltages. It is clear that the back-to-back diode design has significantly improved performance (10-14 dB better) over the single diode design.

The power handling capability of a tunable filter is affected by the voltage swing across each varactor diode and improves as the bias voltage increases. Under the same bias conditions, a back-to-back diode can operate at +6 dB power level as compared to a single diode due to presence of half the RF voltage drop on each diode. The power handling ability can be further enhanced by alleviating the voltage drop across the varactors and this is demonstrated with a careful design of C_s in the bandstop filters. The tuning of C_s in the single-diode filter is controlled mostly by the low varactor capacitance (D_1, 2.3-0.9 pF, in series with a fixed 5 pF capacitor), but the back-to-back diode filter is designed to have a large portion of the RF voltage drop occur across the 1.6 pF passive capacitor (placed in series with the 4.2-1.1 pF variable diode). This enhances the filter

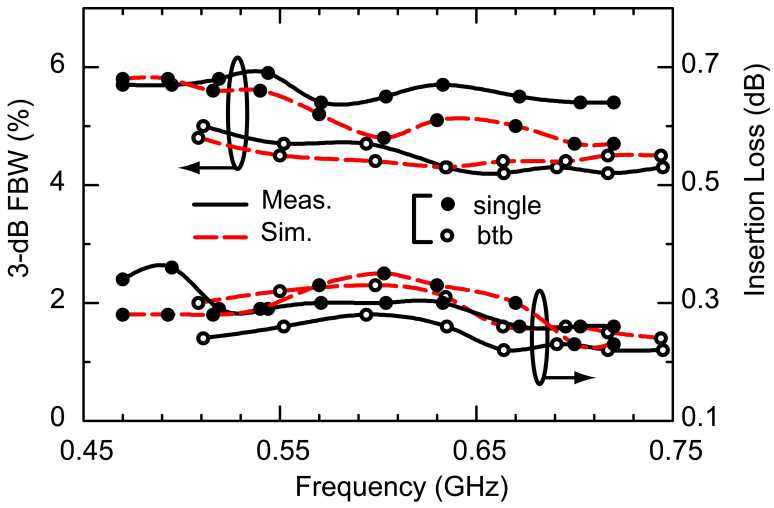


Figure 3.13: Measured and simulated 3-dB bandwidth and insertion loss of the single and back-to-back diode tunable filter for a rejection of 16 dB at a 5 MHz bandwidth.

performance under high RF power.

The large signal S-parameters for the two filters are presented in Fig. 3.16. The measured results show that the single-diode filter can handle 5-10 dBm at 500-700 MHz but the back-to-back diode filter can operate properly at $>$ 25 dBm for $V_b > 4$ V.

3.6 Cascaded Response

The two tunable filters are connected together to demonstrate the cascaded response at 470-710 MHz (Fig. 3.17(a)). The passband loss between the two rejection notches is dependent on the center frequencies, and this indicates that there is a minimum spacing between the two filters with a usable intermediate bandwidth (S_{21} $<$ -3 dB). This limitation could be improved by using higher Q components and is fundamental to filter networks. The low-pass characteristics of the lumped transmission line is also enhanced by cascading two filters and this affects the higher frequency response ($>$ 700 MHz) as seen in Fig. 3.17(a). Both filters can be operated separately to notch 2 different interferers (Fig. 3.17(b)) or at the same frequency to provide a high null rejection as a 4-pole bandstop filter with $\sim$0.6-0.7 dB insertion loss (Fig. 3.17(c)).

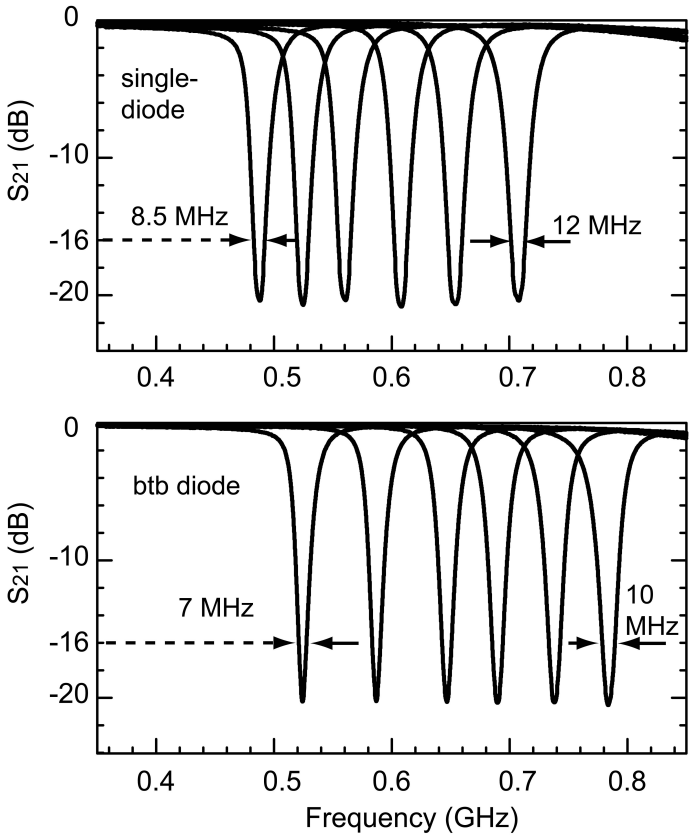


Figure 3.14: Measured S_{21} of the tunable bandstop filters for a constant 20 dB null rejection with a 1.5-2 MHz bandwidth.

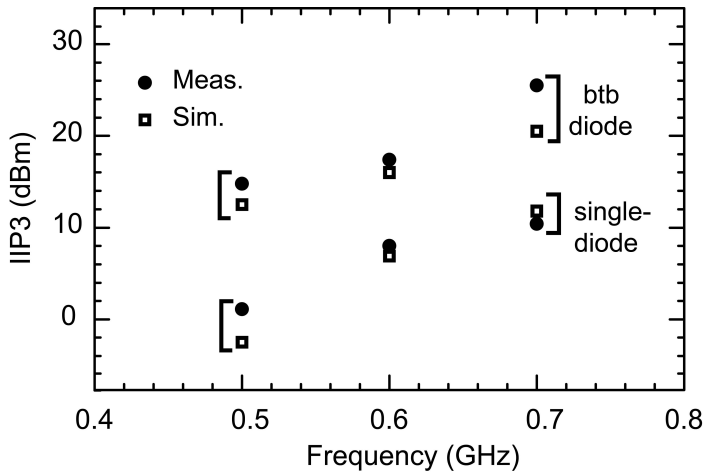


Figure 3.15: Measured and simulated IIP3 vs. resonant frequencies for the two tunable bandstop filters.

3.7 Higher order Lumped-Element Bandstop Filter

The design procedure described in section 3.2.1 is applied to an n^{th}-order design for the synthesis of a generalized lumped-element bandstop filter (Fig. 3.18). The series inductance is transformed to a shunt capacitance in between a pair of immitance inverters J_L=$1/\sqrt{g_0 g_{n+1}}$, and results in a symmetric filter network structure, namely, g_1=$g_{n'}$, $g_{2'}$=g_{n-1} (illustrated with n=even). The scaling inverters are then inserted to transform the resonant branches into shunt L_pC_p resonators with J_{si} properly chosen for a pre-designated inductance, L_p (Fig. 3.18(b)). Finally, the inverters are substituted with lumped-element equivalent circuits and the design equations in Fig. 3.18(c) are summarized as:

$$L_L = \frac{Z_0}{\omega_0 \sqrt{g_0 g_{n+1}}} \tag{3.13}$$

$$\begin{cases} C_{si} = \sqrt{\frac{\Delta g_i}{L_p Z_0 \omega_0^3}} & , i = odd \\ \\ C_{si} = \sqrt{\frac{\Delta g_i g_{n+1}}{L_p Z_0 \omega_0^3}} & , i = even \end{cases} \tag{3.14}$$

$$C_{pi} = \frac{1}{\omega_0^2 L_p} - C_{si} \tag{3.15}$$

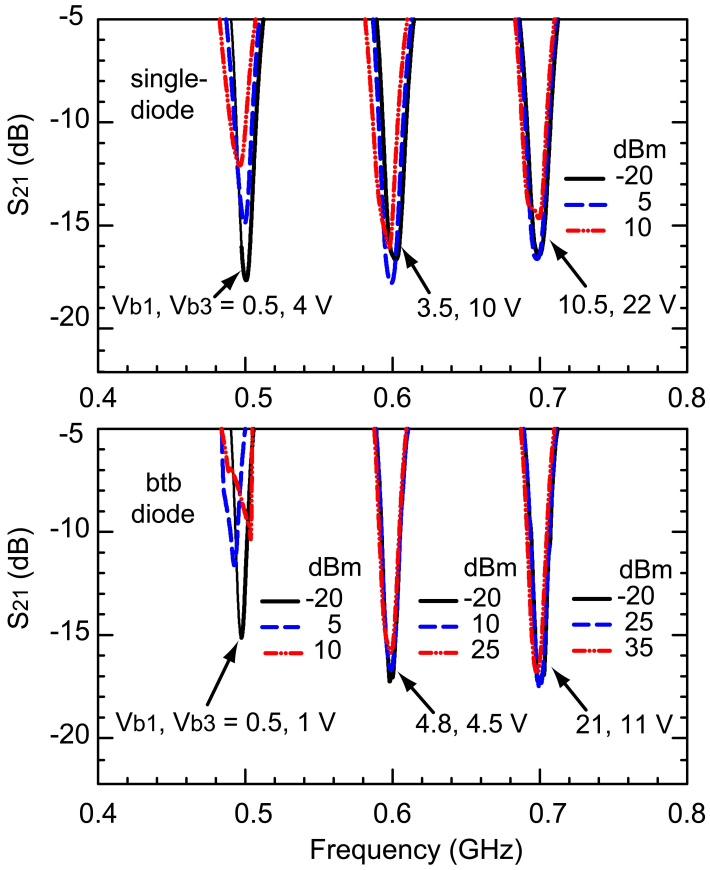
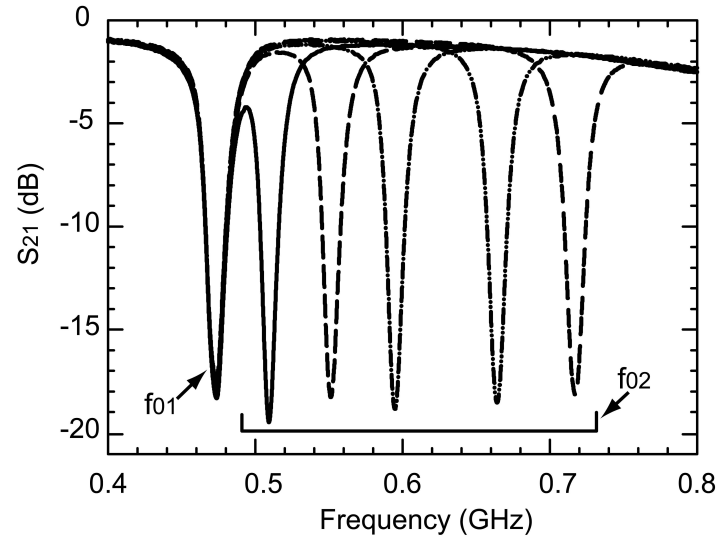
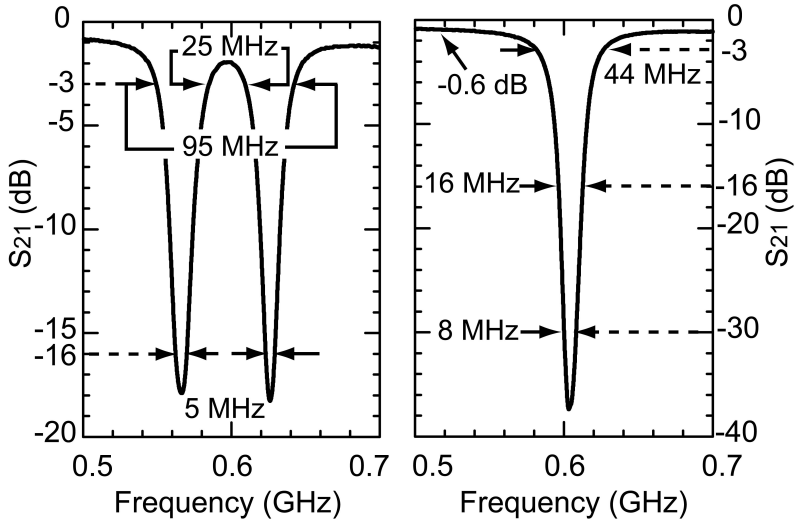


Figure 3.16: Measured large signal responses of the single-diode and back-to-back diode filters.



(a)



(b) (c)

Figure 3.17: Measured S-parameters of two series cascaded tunable bandstop filters at (a), (b) separate frequencies, (c) identical frequency.

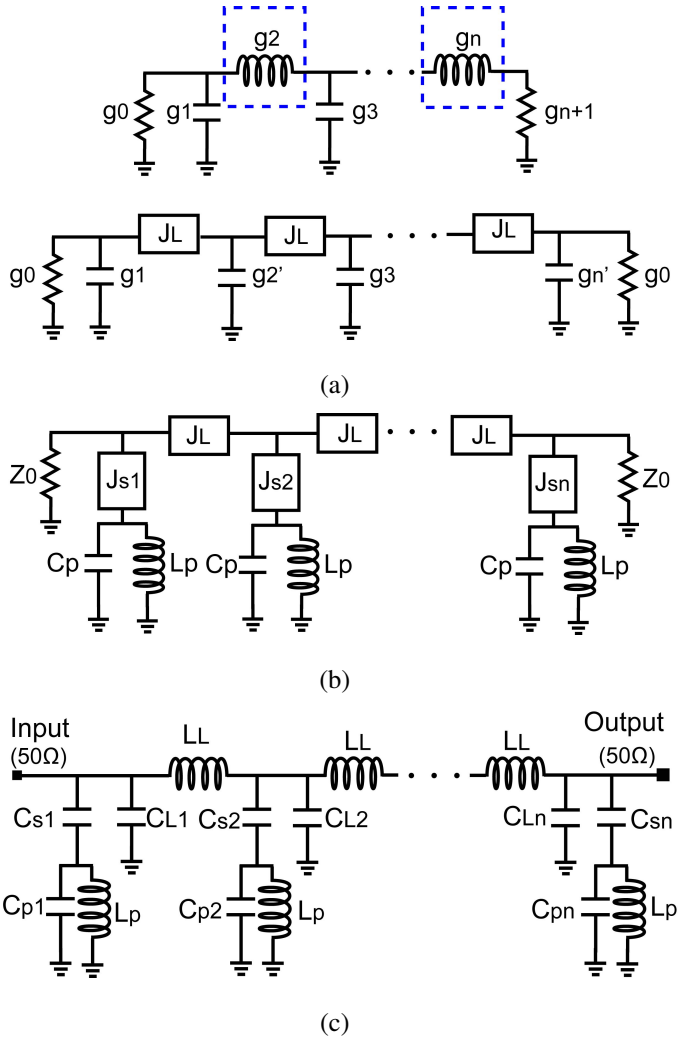


Figure 3.18: (a) Standard n-pole lowpass prototype with the series inductance transformed with immitance inverter J_L (illustrated with n=even), (b) insert scaling inverters and apply frequency and impedance transformation, (c) schematic of lumped-element n^{th}-order bandstop filter.

$$\begin{cases} C_{Li} = \frac{\sqrt{g_0 g_{n+1}}}{Z_0 \omega_0} - C_{si} & , i = 1, n \\ \\ C_{Li} = 2\frac{\sqrt{g_0 g_{n+1}}}{Z_0 \omega_0} - C_{si} & , i \neq 1, n \end{cases} \tag{3.16}$$

3.8 Summary

This chapter presented tunable bandstop filters with a synthesis design method using lumped-element equivalent circuits. Both the center frequency and bandwidth cab be controlled using two varactors per resonator arm. When properly designed, the topology can also result in high power handling using a fixed capacitor in series with the varactor diodes. In the future, the use of RF MEMS switched capacitors will significantly enhance the power handling and linearity of the filters [45].

Chapter 3 is mostly a reprint of the material that is submitted for publications in IEEE Transactions on Microwave Theory and Techniques, 2011. Yu-Chin Ou and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

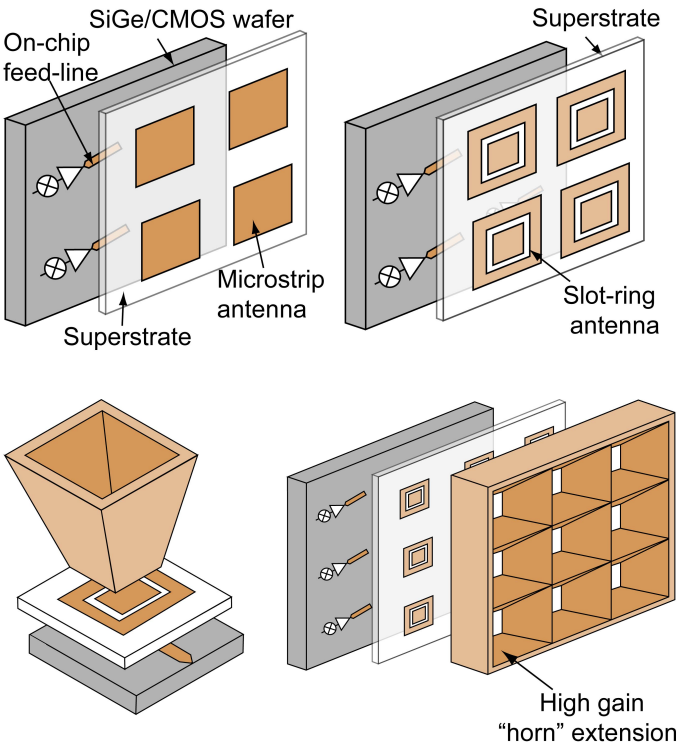
Chapter 4

On-Chip Slot-Ring and High-Gain Horn Antennas for Millimeter-Wave Wafer-Scale Silicon Systems

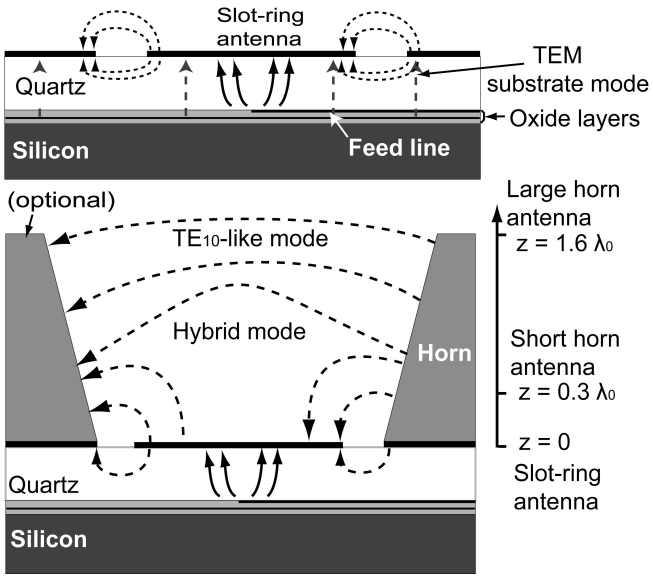
4.1 Introduction

Integrated millimeter-wave antennas on SiGe and CMOS silicon substrates have been challenging due to the low resistivity silicon wafers and the relatively thin metallization structure (5-9 μm) above the silicon substrate. On-chip high-efficiency antennas are essential for mm-wave communication systems since they eliminate the complex RF transitions in and out of the silicon chip, and they can greatly reduce the overall system complexity and cost. However, the efficiency of on-chip antennas must be 40-60% so as to be competitive with a chip-to-board transition and transmission-line loss (1-1.5 dB loss) and an off-chip antenna on a low dielectric constant substrate (0.5-1 dB loss). Also, the size of the on-chip antenna size must be small to result in a small silicon chip and a low overall system cost. Several antennas have been attempted on low-resistive SiGe and CMOS substrates such as microstrip antennas, dipole antennas, inverted-F antennas, Yagi-Uda antennas, slot-ring antennas with an efficiency of 5-10% at 20-140 GHz [46–51].

Different on-chip antennas have been proposed to solve this problem. At mm-



(a)



(b)

Figure 4.1: (a) Stack-up view of the wafer-scale electromagnetically-coupled antenna arrays. (b) Cross-section view and corresponding radiation mode of the slot-ring antenna and the on-chip horn antenna with different extensions.

wave frequencies, bond-wires can be used as efficient antennas, and V-type [52], multi-element Yagi-Uda antennas [53] and single bond-wire radiators [54–56] have all been demonstrated with varying success. These antennas have low gain (V-type, single bond-wire) or are not scalable to multiple elements on a chip (Yagi-Uda). Dielectric resonator antennas have also been used and with good results, but they require a high dielectric constant material and precise machining of the resonator [57, 58]. Dielectric-lens antennas on top of the silicon substrate have been used [59, 60], but they are relatively expensive, and for the case of silicon lenses, require a $\lambda_g/4$ matching layer to avoid a 2-3 dB reflection loss [61].

Microstrip antennas based on quartz superstrates on top of SiGe and CMOS silicon substrates have been shown to result wide bandwidth (90-100 GHz), high efficiency (40-50%), and a gain of 0.7-3.9 dBi at 90-98 GHz [62]. In fact, a 3 Gbps communication system was demonstrated by May et al. using this antenna [63], and Bosch demonstrated a two-antenna radar transceiver at 77 GHz using a similar approach [64].

This chapter presents a high efficiency W-band slot-ring antenna on SiGe and CMOS silicon substrates using a quartz superstrate. Single and dual-polarized slot-ring antennas have been demonstrated before at 90-100 GHz using dielectric lenses with high efficiency [59] [60], and this work removes the dielectric lens requirement. The slot-ring antenna is also used with a metallic horn extension to result in a 1-λ_0^2 pyramidal horn with a gain of 6-8 dBi at 90-99 GHz. The idea of the on-chip horn antennas was first demonstrated in [65–67] using dipole antennas and silicon micromachining techniques, and quasi-integrated horn antennas with a gain of 17-23 dBi were presented in [68–70]. However, a dipole antenna requires a differential feed line, and is not compatible with single-ended circuits. A planar end-fire horn was also demonstrated in [71].

The on-chip horn antenna results in a large aperture area ($1 \times 1\lambda_0^2$ to $> 3 \times 3\lambda_0^2$) and high antenna gain (7-20 dBi) but at the same time, requires a small footprint on the silicon substrate ($\sim 0.5 \times 0.5\lambda_0^2$), and this results in an efficient low-cost mm-wave transceiver. Furthermore, the horn antenna can be arrayed in a one- or two-dimensional arrays with 100% collecting efficiency while still allowing ample space for the transceiver electronics (see Fig. 4.1(a)) [65]. In fact, a 1-λ_0^2 horn aperture and a $0.5 \times 0.5\lambda_0^2$ feed size results in 75% of the chip area available for the transceivers and

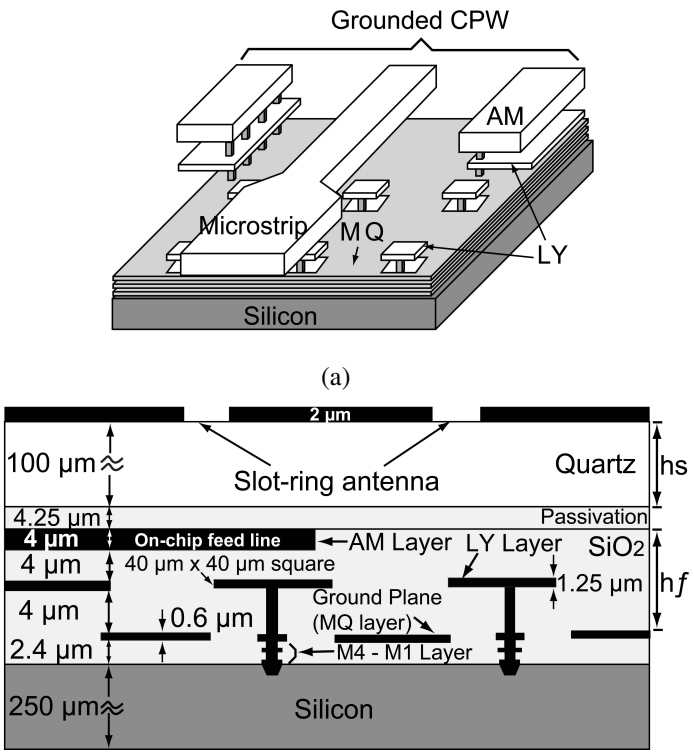


Figure 4.2: (a) The layout of the on-chip microstrip line and the ground plane, (b) The cross-view and boundary condition on the CMOS chip.

can be used in high-efficiency wafer-scale imaging systems [65] or free-space power combining arrays on silicon substrates [62]. The on-chip horn antenna can be scaled for 60 GHz and > 100 GHz applications, but operation at < 60 GHz may result in a large area occupied on the silicon wafer.

4.2 Antenna Concept

4.2.1 Antenna

Fig. 4.1(a) presents the stack-up of the slot-ring and horn antennas and shows a feed-line on the SiGe/CMOS chip, a radiator printed on the superstrate, and an optional metallic horn extension. The excitation between the on-chip feed-line and the superstrate radiator is achieved using electromagnetical coupling. The slot-ring radiator can

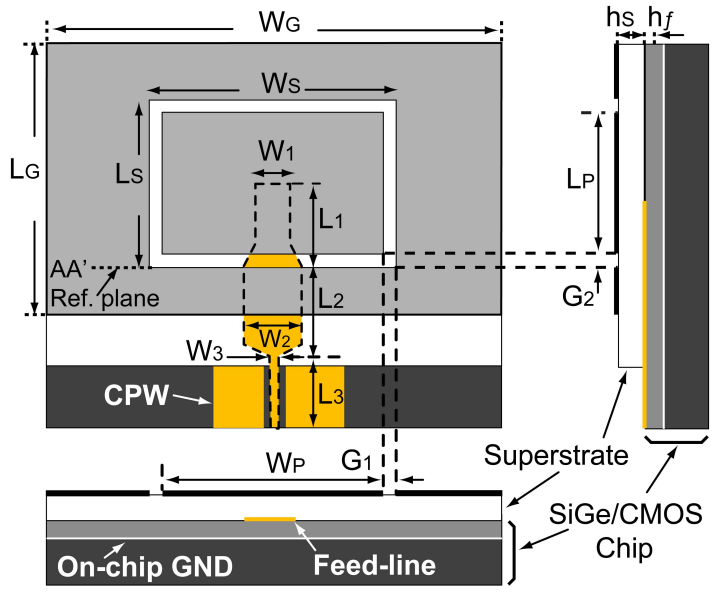


Figure 4.3: Geometry of the EM-coupled conductor-backed finite ground plane slot-ring antenna.

be operated alone or as a secondary source inside a metallic horn. The horn extension converts the slot-ring fields into a TE_{10}-mode distribution and results in a high-gain horn antenna.

In this work, different types of on-chip antennas are demonstrated (Fig. 4.1(b)). With zero height, the boundary condition on the superstrate forms a slot-ring antenna and care must be taken to reduce the power coupled to the TEM substrate mode. With a horn length of $0.3\lambda_0$, an electrically short horn antenna is realized with a hybrid radiating mode including the primary radiation mode from the slot-ring antenna and the short horn as a director. The last antenna is a $1.6\lambda_0$-long horn with tapering in the E and H planes. This results in a standard pyramidal horn antenna with an aperture of λ_0^2 and a directivity of 10 dBi. All 3 antennas use the same on-chip feed-line and the input impedance is optimized by modifying the slot-ring boundary and the horn taper angle.

The silicon chip is designed using the 0.13-μm IBM8HP BiCMOS process [72], but any process with a thick metallization layer can be used. First, an on-chip grounded CPW feed-line with a 9.25 μm total dielectric thickness is realized with dimensions of GSG = 60/18/60 μm. The CPW line transforms into a microstrip line over a large meshed ground plane (1.3×1.3 mm^2) and this feeds the microstrip antenna (Fig. 4.2(a)).

The on-chip ground plane (MQ layer) isolates the lossy silicon substrate (ρ = 1-10 Ω-cm) from the antenna radiation. To satisfy the metal density rules, 40×40 μm metal squares are introduced on the LY layer and are connected to the silicon substrate using very small reverse bias diodes. These metal patches need to be simulated for proper antenna design and will be discussed in Section 4.3.

4.3 Slot-Ring Antenna Design

4.3.1 Mode Analysis

Fig. 4.3 shows the geometry of the rectangular slot-ring antenna. The quartz superstrate (ϵ_r = 3.8) is $h_S < \lambda_d/4$ to suppress higher-order surface wave modes [26,73]. The slot width is kept narrow ($G_1; G_2 < \lambda_0$) so that the magnetic current contains only an azimuthal component. A parallel-plate environment is created between the slot-ring ground plane on the top and the on-chip ground plane at the bottom, but the RF energy is coupled to a *non-radiating* TEM mode. This is explained using even and odd-mode analysis [74]: The odd-mode excitation results in an efficient slot-ring radiating mode with perfect phase cancelation of the dominant TEM mode (Fig. 4.4(a)). The even-mode excitation cannot couple to the TEM mode distribution due to the distribution of charges at the feed and the finite ground plane (Fig. 4.4(b)). This effectively turns the on-chip microstrip feed line into an asymmetrical stripline structure which couples efficiently to the slot-ring antenna on the superstrate, and Fig. 4.4(c) shows the electrical field distribution of the excited fields at the slot-ring antenna.

Table 4.1: Dimension of the W-band on-chip slot-ring antenna (all dimensions are in μm)

W_1	W_2	W_3	L_1	L_2	L_3	W_G	L_G
180	230	18	350	310	1100	1500	1100
W_S	L_S	W_p	L_p	G_1	G_2	h_s	h_f
900	780	760	700	60	40	100	9.25

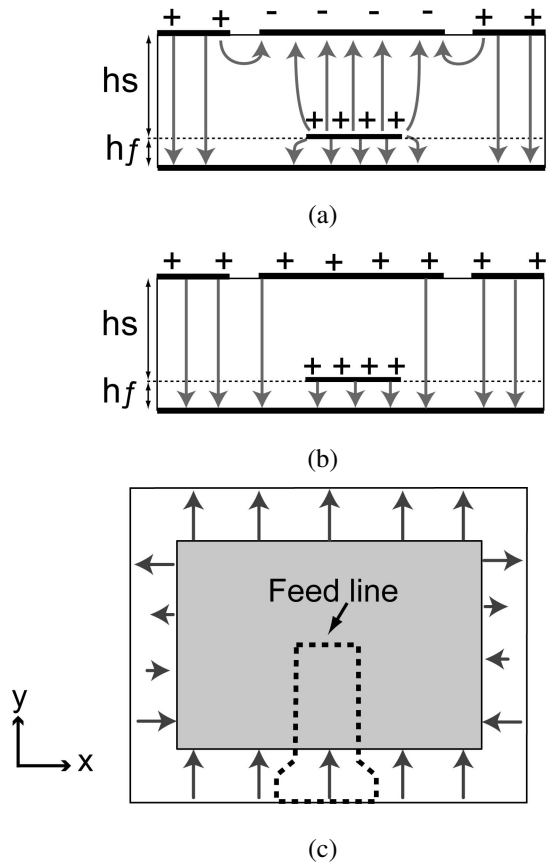


Figure 4.4: Field distributions for the slot-ring antenna: (a) odd-mode excitation, (b) even-mode excitation, (c) radiating mode.

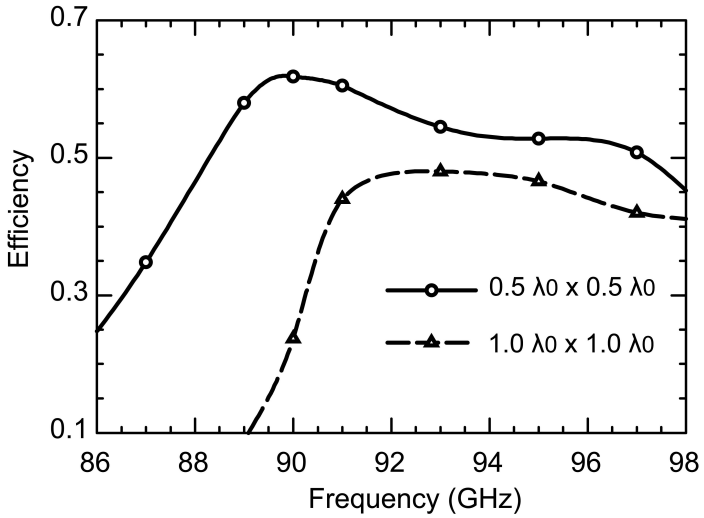


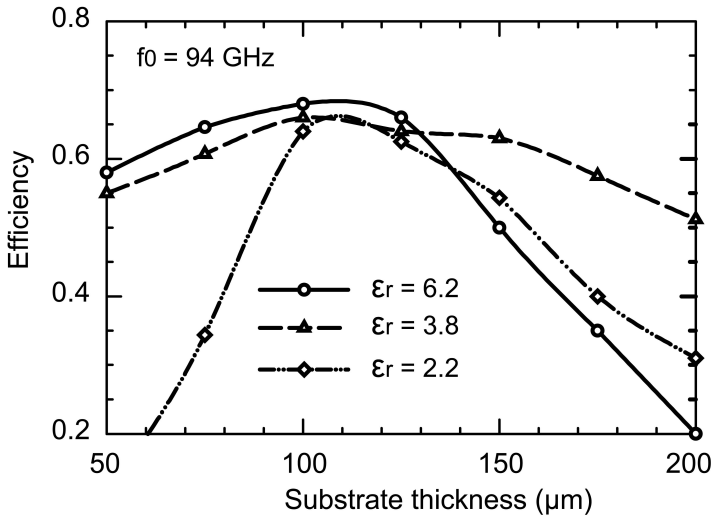
Figure 4.5: HFSS simulated radiation efficiency vs. 1-λ_0-long slot-ring antenna at 94 GHz on various ground plane size ($W_G \times L_G$) with h_s = 100 μm.

4.3.2 Finite Ground Plane Effects

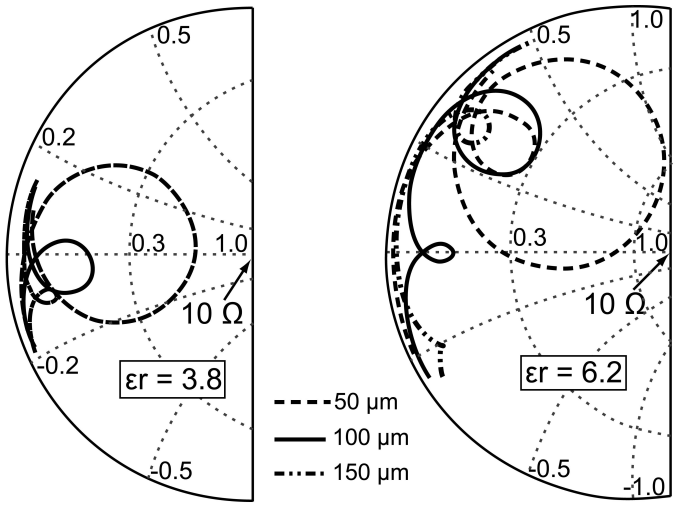
The finite ground plane is essential to the proper operation of the antenna since the TEM substrate mode is the dominant parallel plate mode, but it can only be well sustained in an infinite ground plane [75]. Fig. 4.5 presents the simulated radiating efficiency of a slot-ring antenna at 94 GHz with different ground plane size and a 100 μm-thick quartz superstrate. The simulations show that an efficiency of 60% is achieved with a ground plane dimension of 0.5^2 to $0.75^2\lambda_0^2$. Larger ground planes result in lower radiating efficiency due to power coupled to the TEM substrate mode. Also, higher order modes are triggered and shift the antenna impedance. In an array environment, care should be taken so that the ground planes of the different antennas do not touch each other$-$otherwise via holes must be introduced in the superstrate to supress the TEM mode [76].

4.3.3 Superstrate Design

The coupling from the feed-line to the antenna increases as superstrate height decreases and ϵ_r increases [77]. On the other hand, the surface-wave TEM mode power of a printed slot on a parallel plate is proportional to ϵ_r and inversely proportional to the superstrate thickness [75]. Also, thicker superstrates can trigger higher-order substrate



(a)



(b)

Figure 4.6: HFSS simulated: (a) radiation efficiency vs. h_s for different ϵ_r, (b) input impedance for h_s = 50-150 μm with ϵ_r = 3.8 and 6.2.

modes [73] and result in low antenna gain. The fringing field coupling is enhanced by reducing the dielectric constant and increasing the thickness underneath the feed line, but in this case, it is fixed by the SiGe or CMOS process. As a result, there is an optimized superstrate ϵ_r and thickness for an EM-coupled slot-ring antenna with a backed conductor.

Fig. 4.6(a) presents the simulated radiation efficiency of the slot-ring antenna vs. superstrate thickness for ϵ_r = 2.2, 3.8, and 6.2. A tanδ = 0.001 (quartz) is assumed for all cases for comparison purposes. The antenna dimensions were modified for each case so that the radiation efficiency peaks at 92-94 GHz. For $h_s < 125$ μm, increasing the dielectric constant improves the radiation efficiency by enhancing the fringing-field coupling. For $h_s > 125$ μm, the antenna performance is affected by the impedance matching network, and requires a more complex feeding structure to maintain the radiation efficiency.

Fig. 4.6(b) presents the simulated input impedance of the slot-ring antenna referenced to plane AA$'$ vs. h_S for ϵ_r = 3.8 and 6.2 (Smith chart Z_0 = 10 Ω for clarity purpose). The input impedance increases as h_s decreases and also for a higher ϵ_r due to higher fringing-field coupling. The low antenna impedance necessitates a 10 Ω quarter-wave matching network (L_2 = 310 μm), which is done using a wide microstrip line (W_2) with a simulated loss of 0.66 dB/mm at 94 GHz. The quarter-wave matching loss is therefore 0.2 dB.

4.3.4 On-Chip Feed-line

The antenna radiation efficiency is affected by changing the coupling region length L_1 of the feed line, and also by changing the width, W_1, underneath the antenna (Fig. 4.7). The coupling reaches a maximum when a wide feed-line is chosen, and its open-end approaches the middle of the antenna. Under this condition, the boundary condition underneath the slot-ring antenna does not trigger a TEM mode and results in the best antenna radiating efficiency.

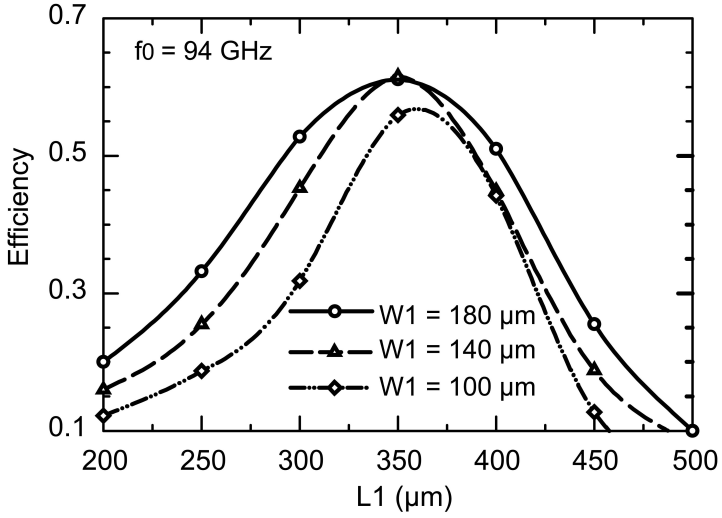


Figure 4.7: HFSS simulated radiation efficiency vs. L_1 and W_1 for h_s = 100 μm and ϵ_r = 3.8 (W_2 = 230 μm, L_2 = 310 μm).

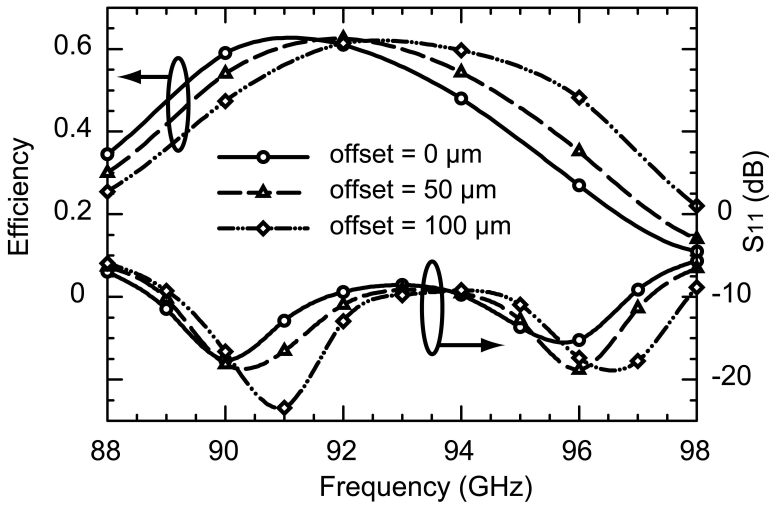


Figure 4.8: HFSS simulations of the antenna performance vs. x-direction alignment offset (h_s = 100 μm and ϵ_r = 3.8, W_1 = 180 μm, L_1 = 350 μm, W_2 = 230 μm, L_2 = 310 μm).

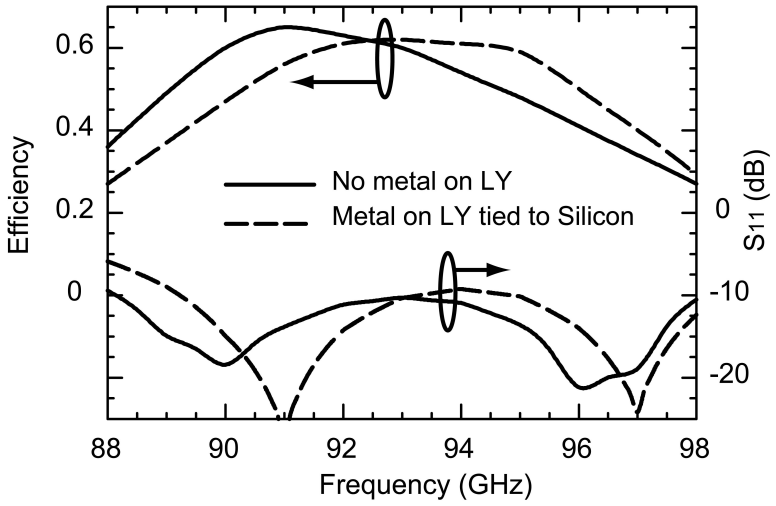


Figure 4.9: HFSS simulations with and without metals on LY layer (h_s = 100 μm, ϵ_r = 3.8, W_1 = 180 μm, L_1 = 350 μm, W_2 = 230 μm, L_2 = 310 μm).

4.3.5 Antenna Alignment

Antennas excited through energy coupling have less dependence on accurate alignment, especially when fed with a very wide feed-line. Fig. 4.8 shows the effect of feed offset in the x-direction, and a y-direction offset also results in a similar performance. The non-symmetric geometry also has a larger cross polarization level which is due to higher-order modes. The feed offset results in a higher efficiency at 94 GHz because the same feed-line is designed for all antennas, and better impedance matching is occurring at 94 GHz for the offset case. This shows the robustness of the antenna to misalignment.

4.3.6 Effect of the LY-layer

Fig. 4.9 presents the simulated S_{11} and radiation efficiency of the antenna with and without the metal squares on the LY layer. The LY metal results in a shift in the simulated S_{11} due to the effective shorter substrate thickness for the microstrip line. The radiation efficiency is also slightly reduced due to the tighter coupling between the on-chip ground plane and the feed line. Since the metal density rules on the MQ layer do not allow for a continuous metal sheet, the case with openings in the MQ layer and with the LY metal layer tied to the silicon substrate is chosen for our design.

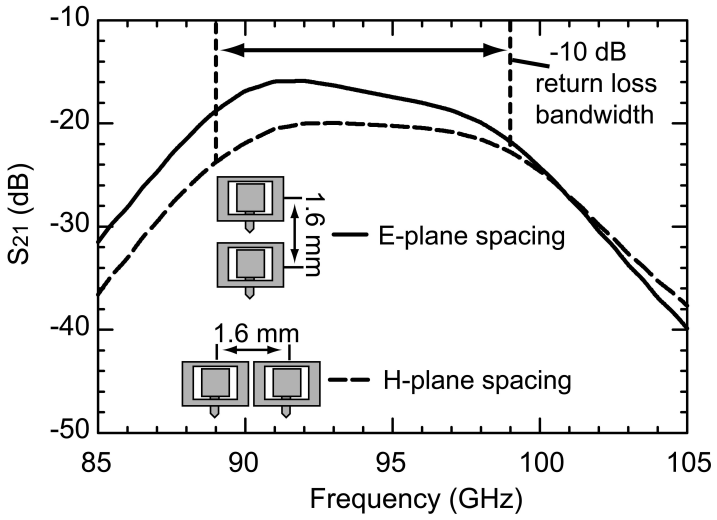
4.3.7 Mutual Coupling

Fig. 4.10 shows the simulated E- and H-plane coupling coefficient (S_{21}) between two antennas with a center-to-center spacing of d = 1.6 and 3.2 mm ($0.5\lambda_0$ and $1\lambda_0$ at 95 GHz). For H-plane coupling, the antenna spacing dominates the isolation with $S_{21} <$ -16 dB with a 0.1 mm gap (d = 1.6 mm) and $S_{21} <$ -30 dB with a 1.6 mm gap. On the other hand, the E-plane coupling is dominated by the excited surface wave mode (TM_0) due to the 100 μm thick quartz superstrate. The TM_0 mode propagates mostly in the transverse direction of a radiating slot resulting in little improvement in the E-plane isolation by increasing spacing from $0.5\lambda_0$ to $1\lambda_0$. The S_{21} in E-plane spacing is $<$ -20 dB in both spacings.

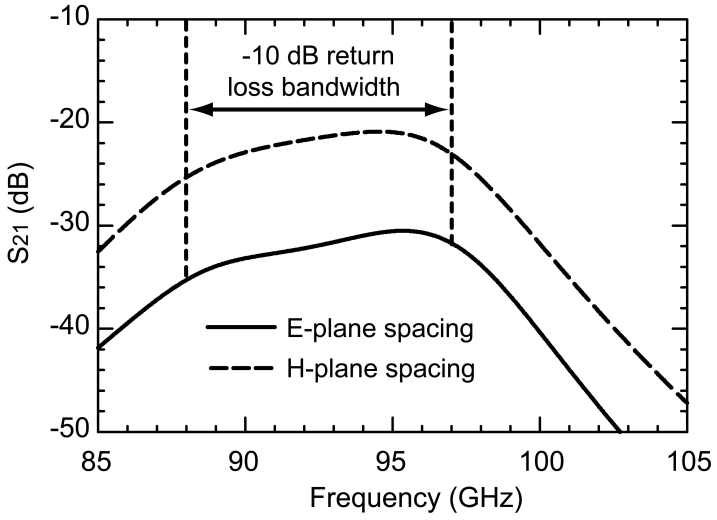
4.4 Extension to Horn Antenna Designs

The silicon-based horn antennas are built using metallic horn extension which is placed on top of the rectangular slot-ring (Fig. 4.11). The horns are optimized using HFSS [78] and Table 4.2 presents all dimensions of the small horn and pyramidal horn antenna. With the fixed boundary condition on the superstrate, the introduction of the horn extension only changes the antenna impedance, and the small horn is tapered only in the H-plane with an aperture size of $0.2\lambda_0 \times 1\lambda_0$ results in a directivity of 7.7 dBi at 92-95 GHz. The simulated gain is 5.8 dBi referenced to the CPW feed line on the silicon substrate. The large horn is based on a pyramidal design with an aperture size of $1\lambda_0 \times 1\lambda_0$. In this case, a short H-plane transition of height h_{H1} is first introduced to generate the desirable field distribution and then a pyramidal tapering is used. The simulated directivity and gain at 92-95 GHz are 10.6 dBi and 8.3 dBi, respectively.

The horn section shows tolerance to misalignment with the slot-ring aperture since the boundary condition is pre-defined by the printed slot-ring geometry. The antenna performance remains unchanged with a larger aperture ($W_p + 2G_1$) even with an offset of $\pm$100 μm since the metallic horn is mainly a gain director for the slot-ring antenna. Smaller apertures reduce the slot width (G_1, G_2) and can be detrimental to the antenna response. Therefore, it is always advisable to fabricate the horn opening to be slightly larger than $W_p + 2G_1$.

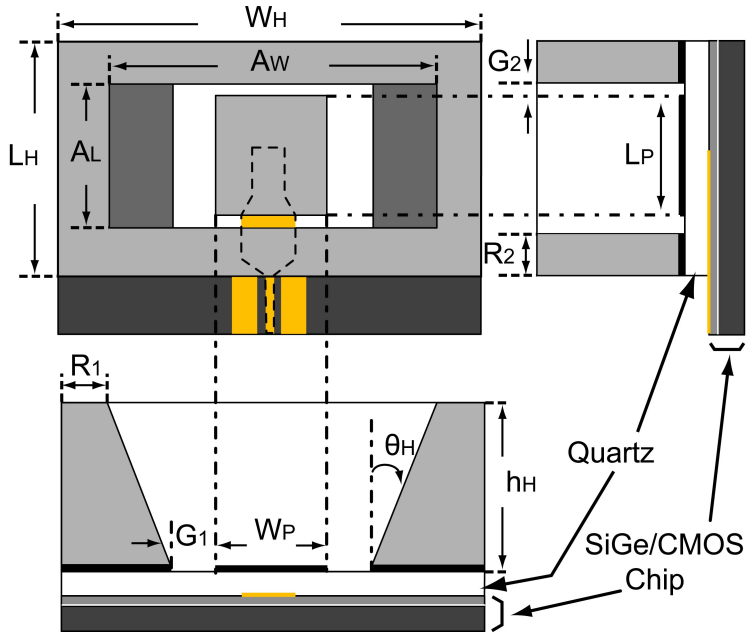


(a)

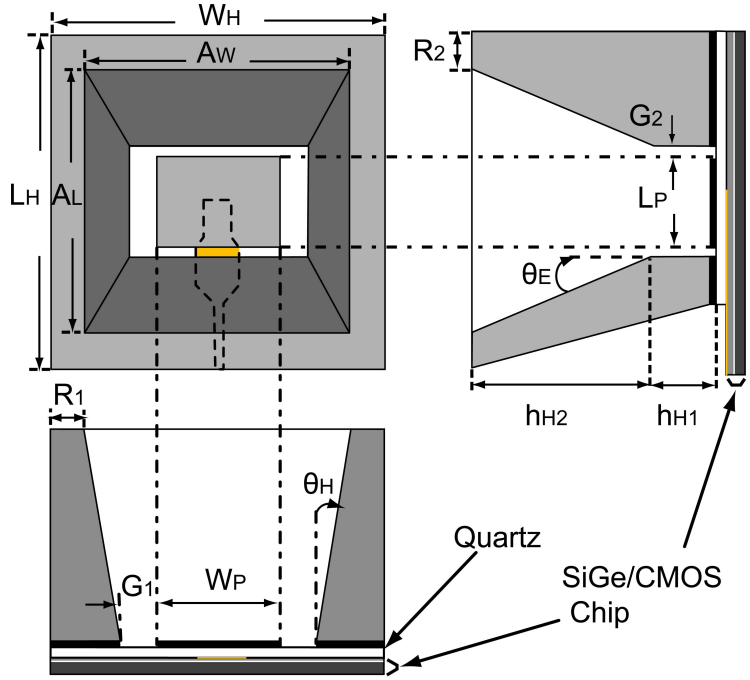


(b)

Figure 4.10: HFSS simulated coupling coefficient (S_{21}) in the E- and H-plane for antenna center-to-center spacing d = (a) 1.6 mm ($0.5\lambda_0$ at 95 GHz) and (b) 3.2 mm ($1\lambda_0$ at 95 GHz).



(a)



(b)

Figure 4.11: Geometry of the EM-coupled on-chip horn antennas:(a) short horn antenna, (b) large horn antenna.

Table 4.2: Dimension of the W-band on-chip horn antennas (all dimensions are in μm)

(a) Short Horn Antenna

W_H	L_H	A_W	A_L	W_p	L_p	G_1
5200	1700	3200	730	900	650	200
G_2	R_1	R_2	h_H	θ_H	–	–
40	1000	280	1000	43.5°	–	–

(b) Large Horn Antenna

W_H	L_H	A_W	A_L	W_p	L_p	G_1
5200	5200	3200	3200	900	650	250
G_2	R_1	R_2	h_{H1}	h_{H2}	θ_H	θ_E
40	1000	1000	1000	4000	10.2°	17.2°

4.5 MEASUREMENTS

4.5.1 Measurement Setup

The input impedance of the antennas are measured with a mm-wave Agilent network analyzer, and a coaxial probe (GSG = 100 μm pitch) with SOLT calibration at the probe tip. The loss of the GSG RF pads and the 1.1 mm-long CPW line is included in the measurements. The antenna is placed on a metalized chuck and allowed to radiate into free space with absorbers placed around the antenna.

The pattern and gain of the on-chip antennas are then measured using a far-field waveguide-only setup on a standard probe station (Fig. 4.12). The transmit signal is fed to the AUT (antenna under test) by a WR-10 waveguide-to-GSG probe with a loss of 1.5 dB at 90-100 GHz [79]. A W-band standard horn antenna with a measured gain, G_r, of 22.5-23.5 dBi at 75-110 GHz is used for the receive antenna at a far-field distance R = 30 cm (62 dB path loss at 94 GHz). The receive horn antenna is connected to a W-band amplifier with a gain of 20-30 dB at 88-98 GHz (P_{in} = -27$\sim$-30 dBm) and the LNA gain is measured accurately using a WR-10 waveguide network analyzer. Care is taken so that the LNA is operated in the linear region. The received RF power is detected using an Agilent W8486A power sensor, and the same power sensor is used to

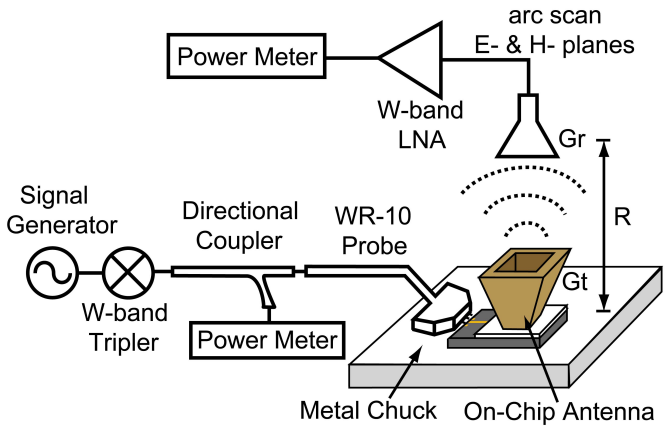


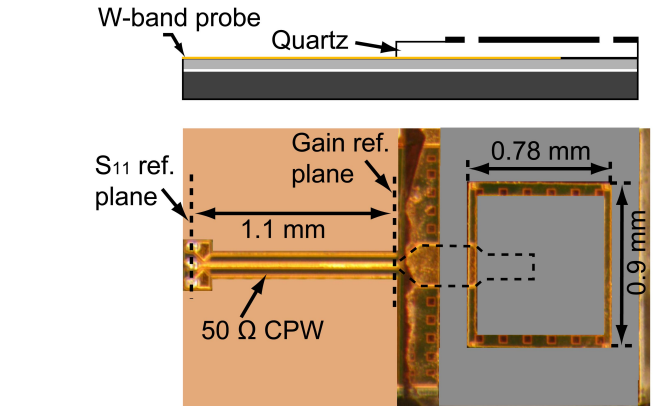
Figure 4.12: W-band measurement setup for the radiation patterns of the on-chip antennas.

measure the transmitted power. RF absorbers are used around the chip antenna and the probe station so as to reduce the standing waves due to the large metal chuck. The gain is referenced to the antenna (see Fig. 4.13(a)) and the CPW line loss is de-embedded from the measurements. The line loss is measured independently and is 0.5 dB at 90-100 GHz.

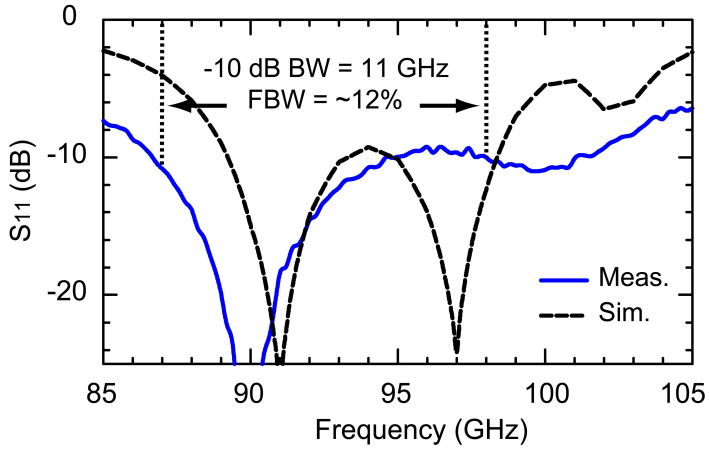
The antenna gain is obtained using the Friis transmission formula with a distance R [**?**]:

$$\frac{P_r}{P_t} = (\frac{\lambda_0}{4\pi R})^2 G_t G_r \tag{4.1}$$

where P_t and P_r are the transmitting and receiving power and G_t and G_r are the gains of the antennas at the respective part. Due to the presence of the metal chuck and many different calibrations needed for this set-up (transmit power, W-band LNA gain, waveguide to GSG transition), the accuracy of the measured gain is estimated to be $\pm$1 dB at 90-100 GHz.



(a)



(b)

Figure 4.13: (a) Fabricated on-chip EM-coupled slot-ring antenna, (b) measured and simulated S_{11}.

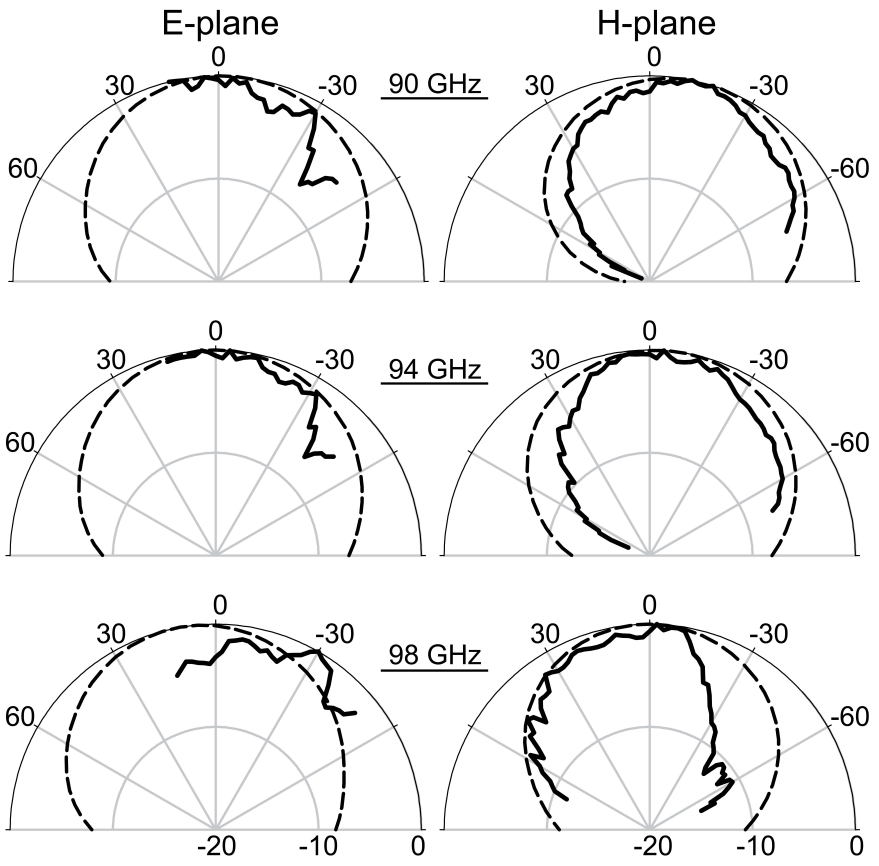


Figure 4.14: Measured (——) and simulated (− −) E and H-plane radiation patterns of the on-chip slot-ring antenna.

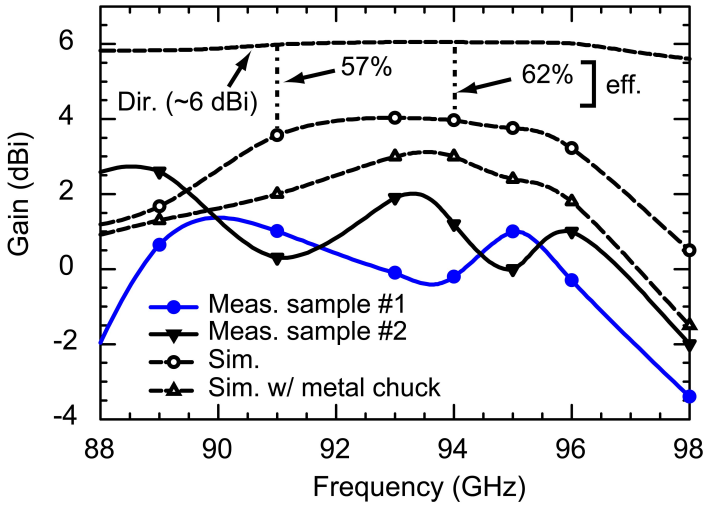
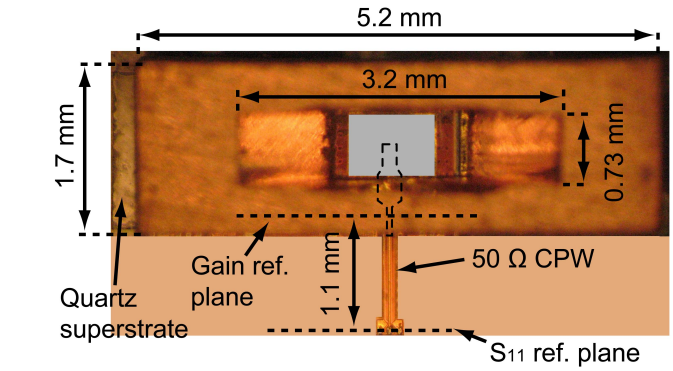


Figure 4.15: Measured and simulated radiation gain of the on-chip rectangular slot-ring antenna.

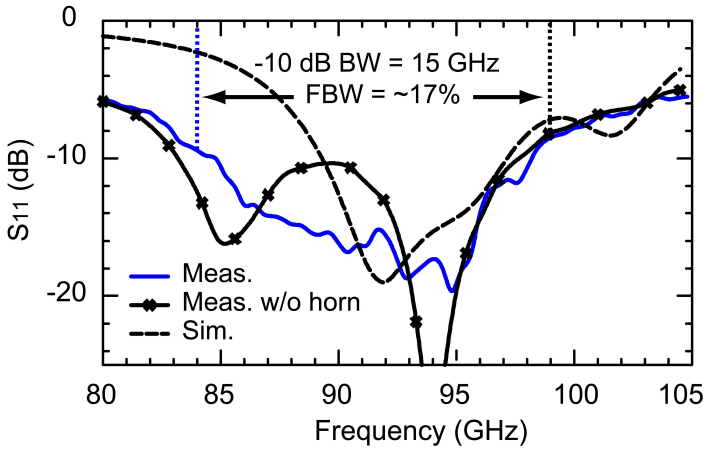
4.5.2 Slot-Ring Antenna

The fabricated quartz superstrate with a printed slot-ring antenna is placed on top of the silicon chip using a dot of glue (Cyanoacrylate) at the corners (Fig. 4.13(a)). The measured and simulated S_{11} agree well at 85-105 GHz, and the -10 dB bandwidth is 88-98 GHz. The simulated and measured radiation patterns are shown in Fig. 4.14. Due to the probe location, the E-plane pattern can only be measured up to +15°. One can also notice some standing and scattering waves in the measured E-plane patterns due from metal-chuck and the probe positioner. On the other hand, the measured H-plane patterns are smooth and symmetrical. The measured cross polarization in both principle planes is $<$ -20 dB and is not shown.

Fig. 4.15 presents the measured antenna gain at 87-98 GHz and agrees well with simulations. Note that the antenna efficiency on an infinite metal chuck is lower than an antenna on a silicon substrate alone due to the triggering of a surface wave on the metal chuck. The slot-ring antenna has a simulated efficiency 57-62% (no metal chuck) and 44-56% (metal chuck) at 91-96 GHz and the measured gain is $\sim$0-2 dBi.



(a)



(b)

Figure 4.16: (a) Fabricated on-chip EM-coupled short horn antenna, (b) measured and simulated S_{11}.

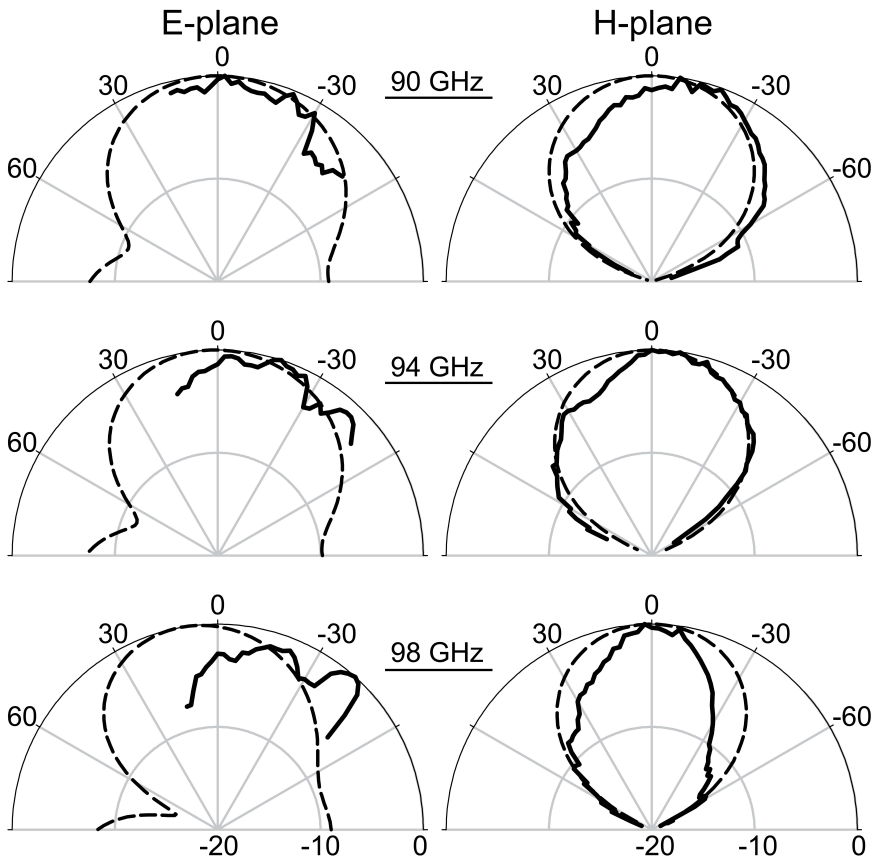


Figure 4.17: Measured (——) and simulated (− −) E and H-plane radiation patterns of the on-chip short horn antenna.

4.5.3 Horn Antennas

Fig. 4.16(a) presents a picture of the short horn antenna on a silicon substrate. The quartz superstrate is first attached to the silicon chip and then the horn is placed on top of the quartz without any adhesive. The mounting of the horn on the superstrate is done manually under a low-power microscope and aligned with the printed metal layout of the slot-ring antenna on the quartz substrate. The quartz substrate and horn antennas could be attached together with gold thermocompression bonding which is commonly used for wafer-to-wave scale application [80].

The measured input impedance is shown in Fig. 4.16(b) and agrees well with simulations. There is no significant change in the measured S_{11} with and without a horn. The measured patterns are shown in Fig. 4.17 and one can clearly notice that the H-plane pattern has a narrower beamwidth than the E-plane pattern. The cross-polarization is $<$-20 dB and is not shown.

The large horn antenna on a silicon substrate is shown in Fig. 4.18(a) and the measured S_{11} also agrees well with simulations. The antenna patterns show a half-power-beam-width (HPBW) of 36° and 50° in the E- and H-planes. Due to the high directivity of the large horn antenna, the effect of the metal chuck is minimized and excellent agreement is obtained with simulations. This antenna fits couples well into an f/0.8-f/1 lens or reflector resulting in a wafer-scale diffraction-limited imaging system [65].

Fig. 4.20 presents the measured gain of both horn antennas. The metal chuck reduces the small horn antenna efficiency, but has virtually no effect on the large horn antenna. The measured gain is 3-6 dBi and 6-9 dBi for the small and large horn antennas at 91-96 GHz respectively. Table 4.3 presents a comparison of the different antennas. These antennas would be ideal for short-range point-to-point communication systems providing a relatively high gain for a transceiver on a silicon substrate.

4.6 Summary

This chapter presented W-band high-gain on-chip slot-ring and horn antennas. The achieved on-chip gains are the highest reported to-date and allow the construction

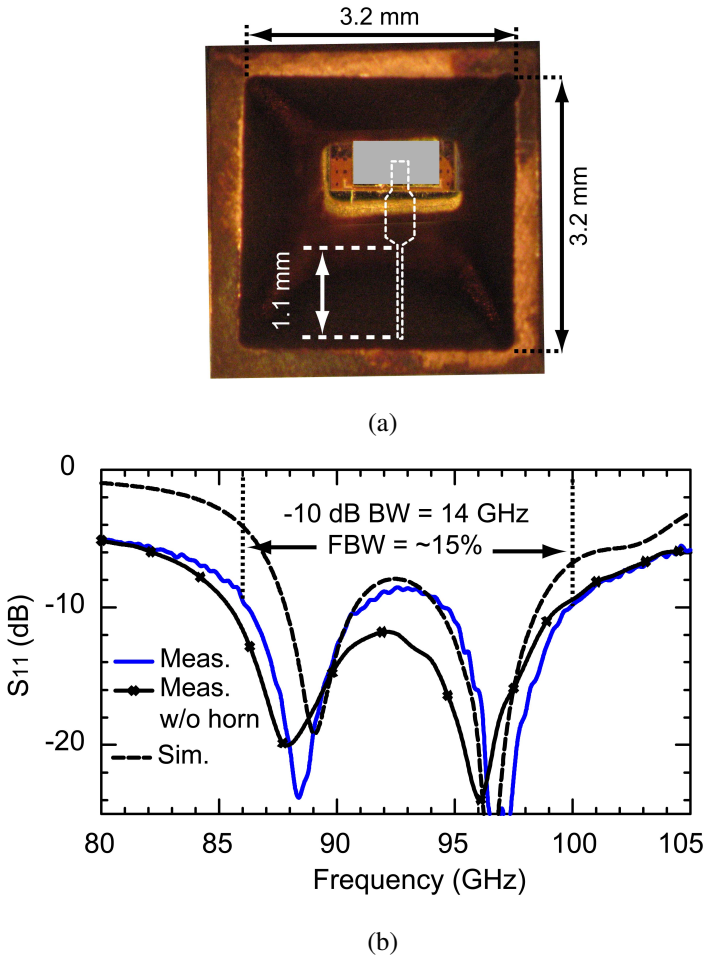


Figure 4.18: (a) Fabricated on-chip EM-coupled large horn antenna, (b) measured and simulated S_{11}.

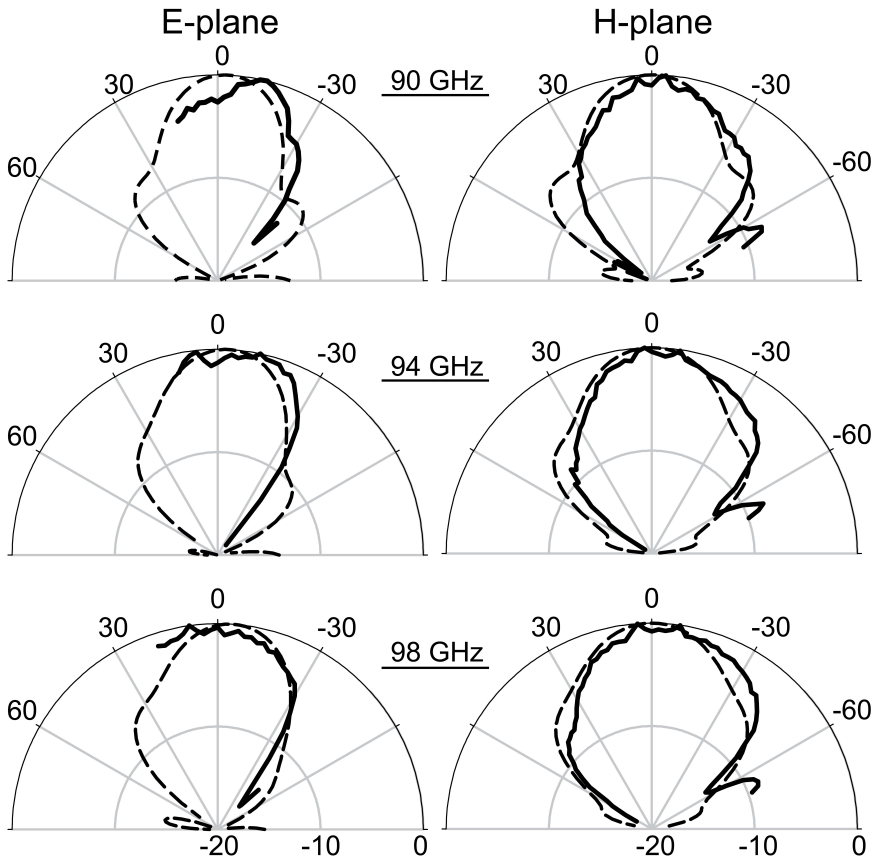
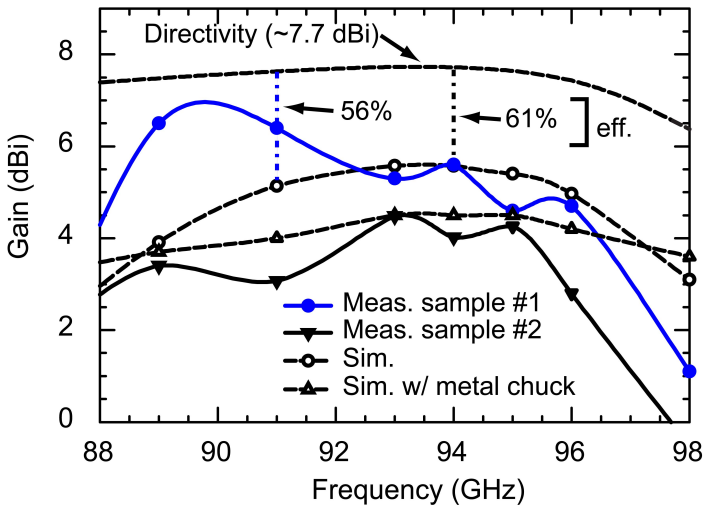
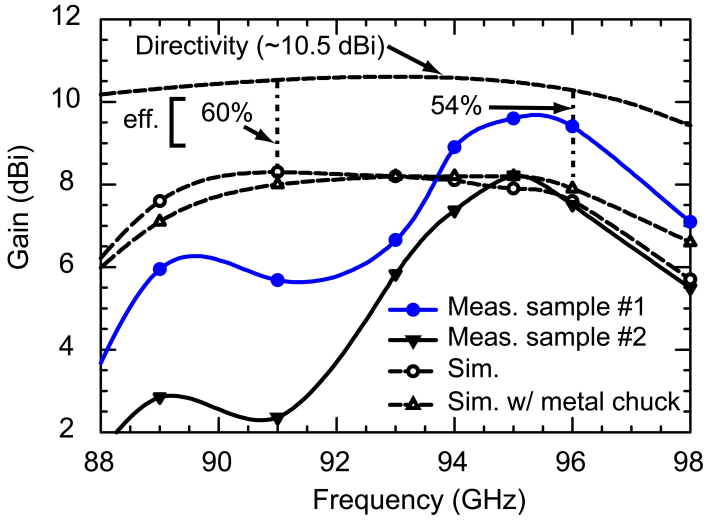


Figure 4.19: Measured (——) and simulated (− −) E and H-plane radiation patterns of the on-chip large horn antenna.



(a)



(b)

Figure 4.20: Measured and simulated gain of the: (a) short horn antenna, (b) large horn antenna.

Table 4.3: Measured performance of the slot-ring and horn antennas at 90-96 GHz

	Slot-ring	**Short horn**	**Large horn**
Aperture size	NA	$0.2\lambda_0 \times 1\lambda_0$	$1\lambda_0 \times 1\lambda_0$
Gain (dBi)	0-2	3-6	6-9
H-plane 3-dB BW	59°	46°	50°
E-plane 3-dB BW	70°	62°	36°
H-plane 10-dB BW	$> 122^\circ$	102°	98°

of two-dimensional imaging arrays or power-combining arrays with efficient use of the silicon chip area. The slot-ring antenna also allows for a dual-polarized design which could be beneficial in communication and polarimetric radar systems. The horn is not limited to $1\lambda_0^2$, but could be as large as $4\lambda_0 \times 4\lambda_0$ resulting in gain of $\sim$20 dBi and a small silicon chip.

Chapter 4 is mostly a reprint of the material as it will appear in IEEE Transactions on Microwave Theory and Techniques, 2011. Yu-Chin Ou and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Table 4.4: Comparison table of the proposed antennas with current published on-chip integrated antennas on SiGe/CMOS process

Catagory	**Process**	**Antenna Architecture**	f_0 (GHz)	**-10dB-BW** (GHz)	**Aperture size** (λ_{eff}^2)	**Gain** (dBi)	**Efficiency** (%)	**Reference**
Antennas on Silicon Substrate	BEOL	Inverted-F	60	55-68	0.9×0.05	-19	3	[46]
	NA	Dipole	24	20-30	0.6×0.1	-8	NA	[47]
	0.18 μm CMOS	Inverted-F	60	57-64	0.4×0.3	-15.5	6	[48]
	0.18 μm CMOS	Quasi-Yagi	60	55-65	0.5×0.4	-10	10	[49]
	0.18 μm CMOS	Microstrip	65	63-65	0.6×0.5	-10	4	[50]
	0.13 μm BiCMOS	Slot-ring	94	88-92	0.7×0.4	-5	6$\sim$9	[51]
	0.65 μm CMOS	Taper Slot	140	NA	NA	-25	NA	[52]
Bond-wire Antennas	SiGe/CMOS	Yagi-Uda	40	36-37	1.1×0.4	8	82	[53]
	NA	Triangular Loop	60	NA	0.5×0.3	1	NA	[54]
	SiGe/CMOS	Large Wire-bond	40	38-44	0.5×0.3	-1.5	51	[55]
	NA	Monopole	55	55-58	0.16	0.5	33	[56]
DRA	CMOS	Cylindrical DRA	60	59-61	$^{*}\pi \cdot 0.3^2$	3	51	[57]
	SiGe MMIC	Rectangular DRA	35	33-37	$^{**}0.8 \times 0.6$	1	48	[58]
Lens-based Antennas	0.13 μm BiCMOS	*Slot-ring	94	88-94	0.7×0.4	17	50	[51]
	Silicon/GaAs	**Slot-ring Array	94	15%	$\pi \cdot 12.8^2$	27	> 80	[59]
Superstrate Antennas	0.13 μm BiCMOS	Microstrip	94	92-98	0.5×0.3	3	57	[63]
	0.13 μm BiCMOS	Microstrip	77	NA	NA	NA	> 50	[64]
	0.13 μm BiCMOS	Slot-ring	94	87-97	0.7×0.4	2	50-60	This work
	0.13 μm BiCMOS	Short Horn	94	84-99	$^{\dagger}1.0 \times 0.2$	5	50-60	This work
	0.13 μm BiCMOS	Pyramid Horn	94	86-100	$^{\dagger\dagger}1.0 \times 1.0$	8	50-60	This work

* 12 mm diameter quartz lens without dielectric matching layer

** 22 mm diameter high-resistivity silicon lens with dielectric matching layer

* DRA height is $0.3\lambda_{eff}$ ** DRA height is $0.25\lambda_{eff}$ † horn height is $0.3\lambda_{eff}$ †† horn height is $1.6\lambda_{eff}$

Chapter 5

Differential Microstrip and Slot-Ring Antennas for Millimeter-Wave Silicon Systems

5.1 Introduction

Integrated on-chip antennas are becoming an important design aspect of low-cost millimeter-wave systems since they remove the loss and cost associated with transitions in and out of the silicon chip. In recent years, a large number of on-chip antennas have been proposed, but most have shown high loss and low gain due to the low silicon conductivity or the proximity of a very close ground plane to the radiating structure [81]. Recently, a number of efficient single-ended antennas have been demonstrated based on dielectric resonators [58], superstrate resonators [64], planar quartz superstrates on top of the silicon wafer (with and without a focusing horn) [62, 63, 82], and dielectric lens [51]. The planar superstrate design is not limited to quartz, and efficient operation can be obtained using any low loss dielectric substrate with ϵ_r between 3 and 12.

Differential circuits have the advantage of high immunity from crosstalk and noise which is important in dense millimeter-wave architectures. A high-efficiency on-chip differential antenna is fully compatible with a differential front-end and eliminates the single-ended to differential balun and its associated loss [83–85]. Traditionally,

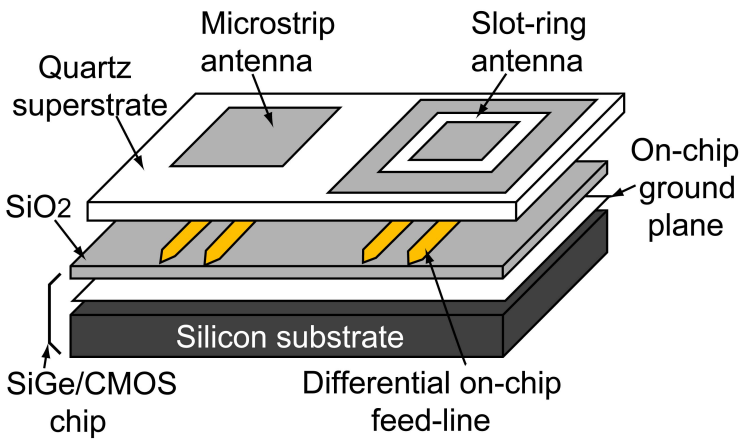


Figure 5.1: The stack-up view of the edge-fed electromagnetically coupled differential superstrate microstrip and slot-ring antennas.

differential microstrip antennas are fed at the opposite radiating edges using two single-ended feed-lines with 180° phase difference [86]. This method requires additional feed-line transitions and extra line routing resulting in increased path loss, and does not lead to compact differential circuits. Microstrip antennas fed with differential feed-lines using probes [87] and apertures [88] were also demonstrated, but the multi-layered topology is suitable for a printed-circuit board (PCB) or an LTCC process and not for silicon on-chip integrated antennas since the thin dielectric thickness in the on-chip implementation results in a low antenna efficiency.

Recently, [62,63,82] presented integrated antennas excited using proximity coupling from on-chip feed-lines, and with one layer of quartz superstrate above the chip. In this paper, this high efficiency ($> 50\%$) single-ended feeding method is generalized to differential on-chip microstrip antennas with balanced feed-line coupling at the non-radiating antenna edges. A conductor-backed rectangular slot-ring antenna is also presented with the same feeding technique.

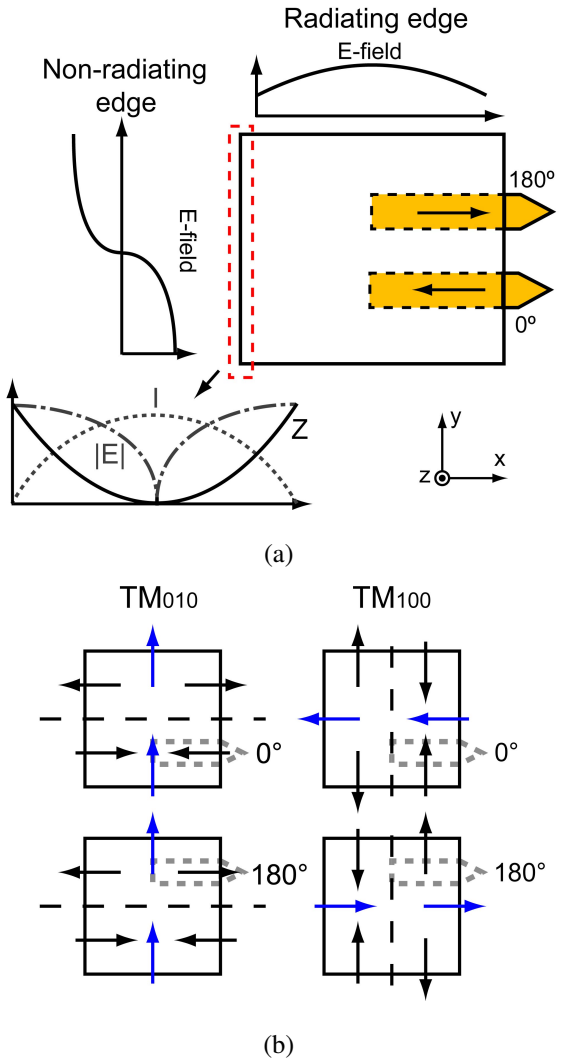


Figure 5.2: (a) Differentially-fed microstrip antenna with electromagnetically-coupling at the non-radiating edge (origin defined at the antenna center), and (b) resonant modes of the edge-feeding EM-coupled microstrip antenna.

5.2 Antenna Concept

5.2.1 Antenna

Fig. 5.2(a) presents the electric field on the non-radiating edge of the differential microstrip antenna. The electric field is anti-symmetric with zero at the center and maximum at the two terminals. The antenna input impedance on the non-radiating edge would ideally vary from 0 to ∞ from the center to both ends of the antenna. As a result, the antenna can be excited either using single-ended or differential [89] feed-lines connected to the proper position at the non-radiating side. Note that with this approach, the antenna resonant current and feed-line current are orthogonal to each other.

For a single-ended EM-coupled microstrip antenna, feeding at the non-radiating edge is equivalent to off-center feeding which results in TM_{100} and TM_{010} modes being unequally excited on the microstrip antenna. This results in an elliptical polarized microstrip antenna. On the other hand, with a differential feed-line feeding at the non-radiating edge, the superposition of the resonant modes excited individually by two equal-amplitude but out-of-phase feed-lines is summarized in Fig. 5.2(b), and results in single resonant mode. A similar feeding technique is applicable to a conductor-backed slot-ring antenna with a finite ground plane. The E-field and resonant current distribution of both antennas are similar, but this antenna has a ground plane which is located on top of the quartz superstrate (Fig. 5.1).

5.2.2 Silicon Feed and Its Boundary Conditions

Fig. 5.3 presents the stack-up of the proposed antenna with differential feed-lines on the SiGe/CMOS chip. The silicon chip is designed using the 0.13-μm IBM8SF CMOS process [90], but any process with a thick metallization layer can be used. The on-chip feed-line is based on a 20 μm wide microstrip line (MA layer, 4 μm thick) and 11 μm total dielectric thickness over a continuous ground plane. The on-chip ground plane (LY layer, 0.5 μm thick) isolates the lossy silicon substrate (ρ = 1-10 Ω-cm) from the antenna radiation. To satisfy the metal density rules of this process (metal must be present on all layers), 40×25 μm^2 metal squares are introduced on the intermediate E1 layer and are connected to the ground plane through vias (Fig. **??**). These small metal

patches are carefully placed to be > 44 μm (4 times the substrate thickness) away from the edges of the microstrip lines in order not to affect the line impedance. This prevents the effective ground plane from raising to the E1 layer which reduces the coupling between feed-lines and the superstrate antenna. As a result, the high radiation efficiency is enhanced along with a continuous on-chip ground plane (LY layer).

For practical considerations, the differential feed-line is approximated by two unbalanced microstrip lines. A meandered rat-race coupler (Fig. 5.4(a)) is used to provide differential signals for antenna excitation and any non-ideal amplitude and phase offset which can be pre-simulated on a stand-alone coupler. The Σ port of the coupler is internally terminated with a 50 Ω on-chip resistor to absorb any common-mode signal reflected from the antenna. The circuit is optimized at 94 GHz in Sonnet [34] and results in $\pm 3^{\circ}$ phase error and 0.6 dB insertion loss at 90-96 GHz. Fig. 5.4(b) presents a picture of the 180° coupler and a detailed layout of the terminating resistor with inductive vias. The resistor is characterized in Sonnet as shown in the Smith chart.

5.3 Antenna Design

Fig. 5.5 presents the geometry of the microstrip and rectangular slot-ring antennas with the antenna dimensions given in Table 5.1. The dimension of the microstrip antenna is first designed in HFSS [78] to be $\sim 0.5\lambda_{eff} \times 0.7\lambda_{eff}$ and the slot-ring length is $\sim 1\lambda_{eff}$. The antenna length, L_p, may be modified later for impedance matching and secondary mode control. The quartz superstrate (ϵ_r = 3.8) is $h_s < \lambda_d/4$ to suppress higher-order surface wave modes [26, 73].

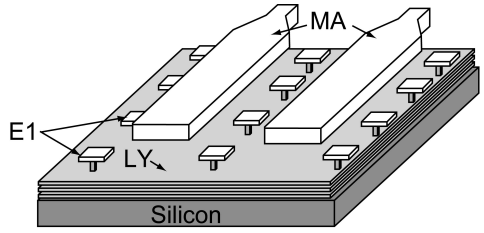
Table 5.1: Dimensions of the on-chip differential antennas (all dimensions are in μm)

(a) Differential microstrip Antenna

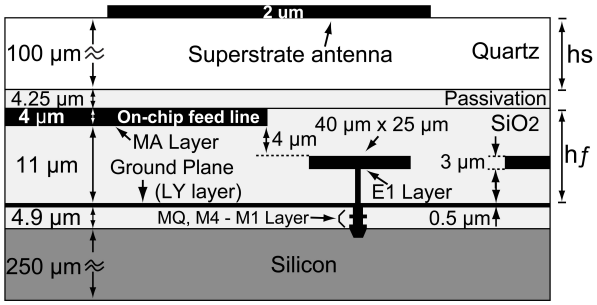
W_1	W_2	W_3	L_1	L_2
140	200	20	375	400
W_P	L_P	G	h_s	h_f
700	840	400	100	15

(b) Differential Slot-ring Antenna

W_1	W_2	W_3	L_1	L_2	W_G
140	200	20	360	400	1200
L_G	W_P	L_P	S_W	G	–
1240	700	850	50	400	–

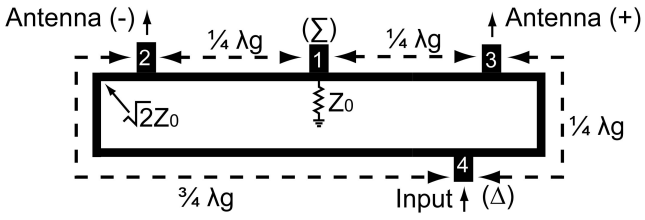


(a)

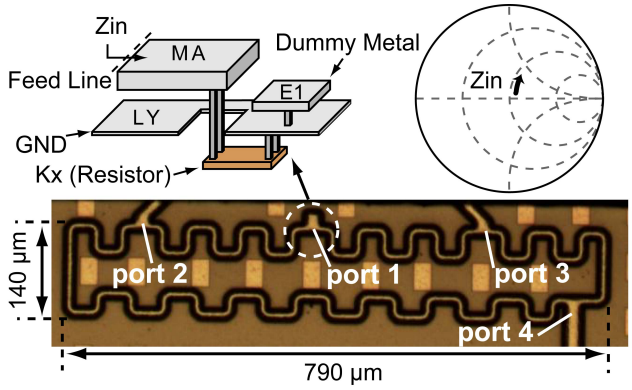


(b)

Figure 5.3: (a) The layout of the on-chip differential feed-line and the ground plane, (b) the cross-view and boundary condition on the IBM8SF CMOS chip.



(a)



(b)

Figure 5.4: Meandered miniaturized rat-race coupler: (a) schematic, and (b) photograph and terminating resistor impedance at 90-96 GHz.

5.3.1 Superstrate Design

The coupling from the feed-line to the antenna increases as superstrate height decreases and ϵ_r increases [77]. On the other hand, the surface-wave mode power is proportional to ϵ_r and inversely proportional to the superstrate thickness [75]. Also, thicker superstrates can trigger higher-order substrate modes [73] and result in low antenna gain. The fringing field coupling is enhanced by reducing the dielectric constant and increasing the thickness underneath the feed line, but in this case, it is fixed by the SiGe or CMOS process. As a result, there is an optimized superstrate ϵ_r and thickness for an EM-coupled superstrate antenna.

Fig. 5.6 presents the simulated radiation efficiency of the microstrip and slot-ring antenna vs. superstrate thickness for ϵ_r = 2.2, 3.8, and 6.2. A tanδ = 0.001 (quartz) is assumed for all cases for comparison purposes. The antenna dimensions and feed-lines were modified for each case so that the radiation efficiency peaks at 93-96 GHz. In general, increasing the dielectric constant improves the radiation efficiency by enhancing the fringing-field coupling. Also, the efficiency increases with the superstrate thickness from 0 μm to 100 μm until the superstrate becomes too thick to support efficient coupling.

5.3.2 Antenna Feeding Location

Fig. 5.7 presents the simulated real part of the input impedance (referenced to plane AA') vs. feeding location G on the non-radiating edge. G is defined as the distance between the middle of each feed-line and Z_{in} is defined as $Z_{11} - Z_{12}$. The input impedance is very low (0.5-2.5 Ω) and as expected, decreases as the feed location gets closer to the antenna center. Similar impedance response is obtained for the rectangular slot-ring antenna and the lower frequency hump is from the finite superstrate ground plane resonance.

5.3.3 On-Chip Differential Feed-lines

Fig. 5.8 presents the microstrip antenna input return loss, defined as $S_{11} - S_{12}$, when transformed by a quarter-wave-long ideal coupled lines with an odd-mode

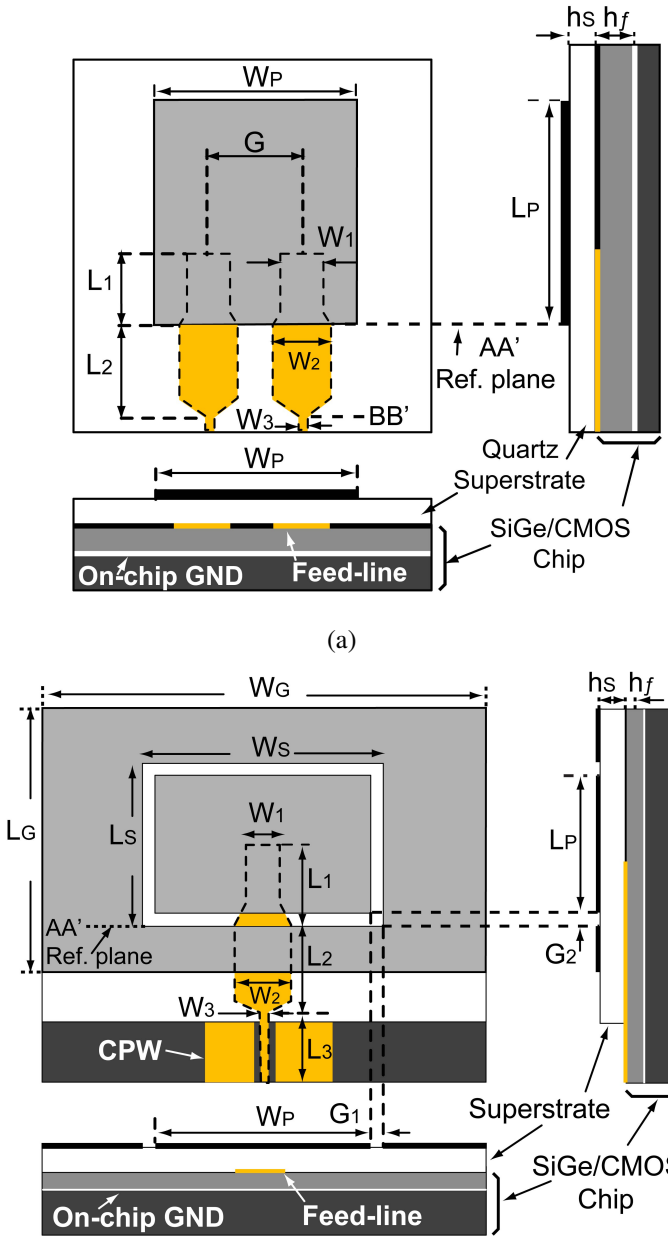
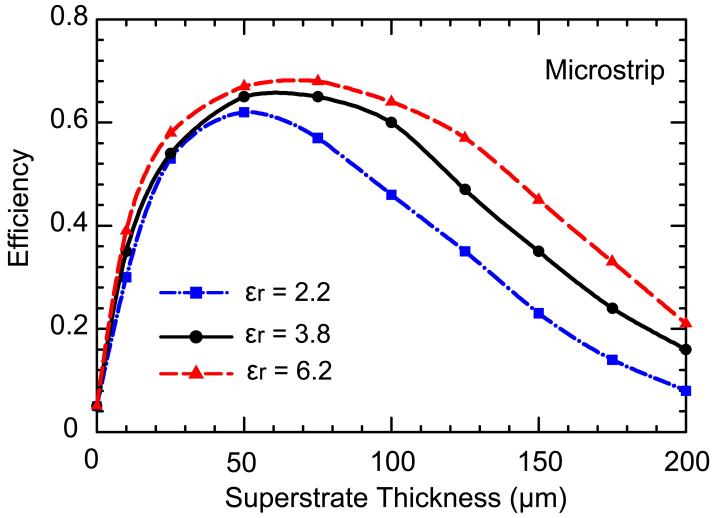


Figure 5.5: Geometry of the innovative EM-coupled differential on-chip (a) microstrip, and (b) slot-ring antenna.



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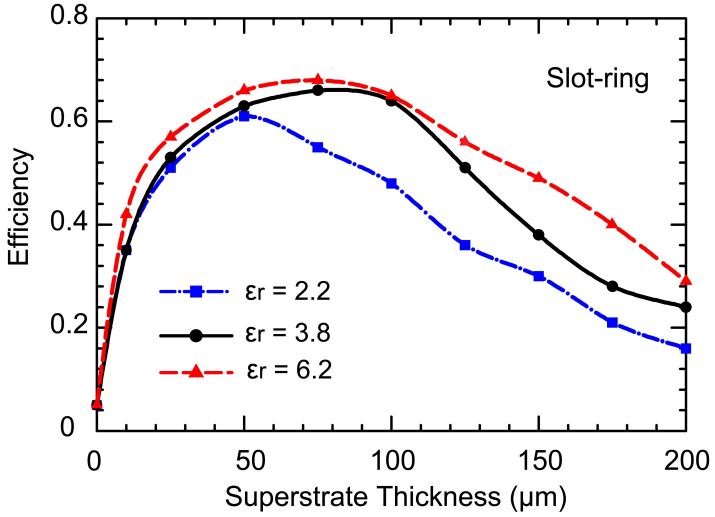


(b)

Figure 5.6: HFSS simulated radiation efficiency vs. h_s with different ϵ_r for differential (a) microstrip, and (b) slot-ring antenna.

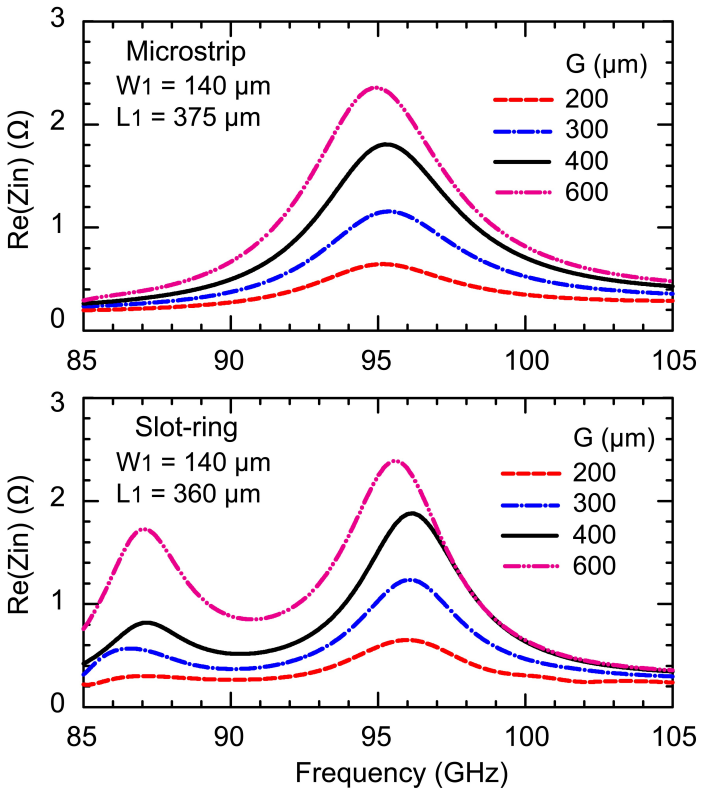


Figure 5.7: HFSS simulated antenna input impedance vs. feeding location G of the differential antennas fed at the non-radiating edge with 100 μm quartz superstrate.

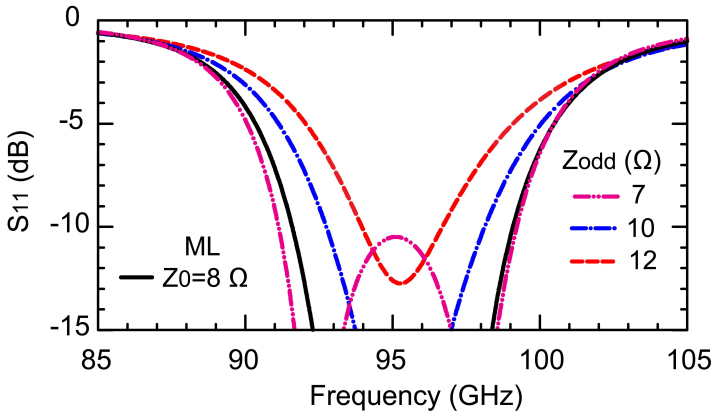


Figure 5.8: HFSS simulated return loss of the differential microstrip antenna connecting to a quarter-wave-long coupled line with G = 400 μm.

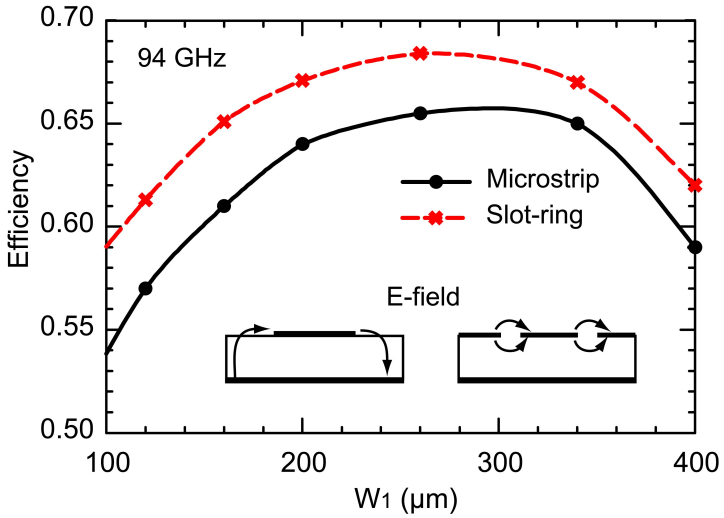


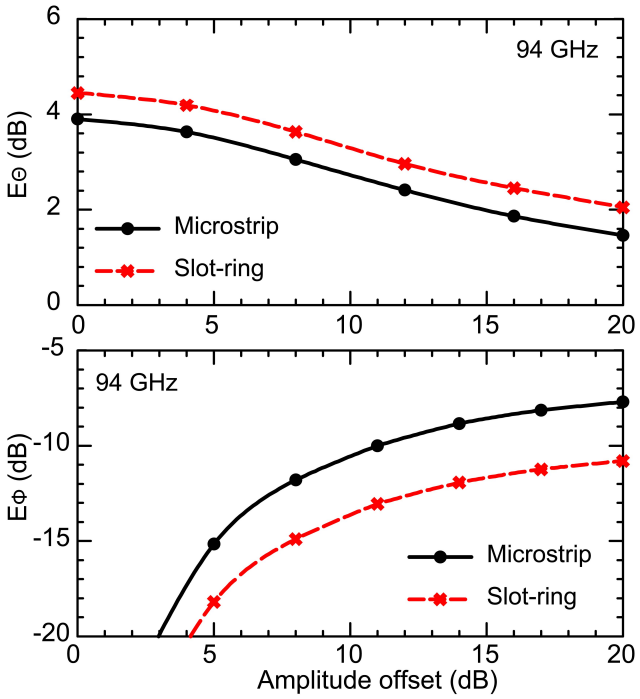
Figure 5.9: HFSS simulated antenna radiation efficiency vs. W_1 at 94 GHz with $G = 400$ μm.

impedance of 7-12 Ω (between ref. plane AA' and BB' in Fig. 5.5). Also, the antenna return loss transformed by a pair of un-coupled 8 Ω microstrip lines is included to validate the antenna designs in this work which use uncoupled lines with 180° phase difference. Similar results are obtained for slot-ring antennas and thus are not presented. The wide lines ($W_2 = 200$ μm) of length $L_2 = 400$ μm have a simulated loss of 0.66 dB/mm at 94 GHz and the overall matching loss is therefore 0.3 dB.

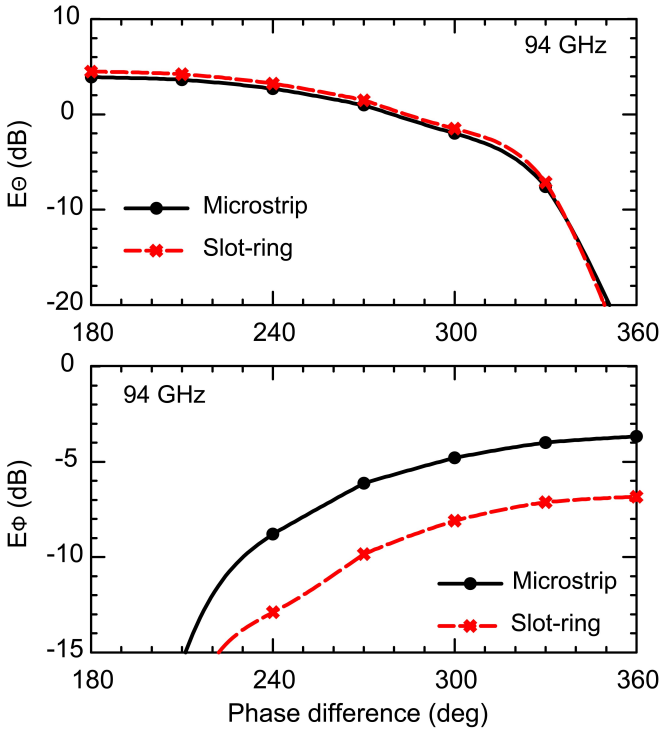
Fig. 5.9 presents the simulated antenna radiation efficiency vs. feed-line width, W_1, underneath the antenna. The coupling reaches a maximum when a wide feed-line is chosen such that TEM surface mode is not triggered between the antenna metal on the superstrate and the on-chip ground plane [82]. The slot-ring antenna has slightly higher efficiency (+4%) than the microstrip design for the same feeding/impedance conditions.

5.3.4 Phase and Amplitude Imbalance of Feed-lines

The differential feed-lines are approximated by a pair of unbalanced microstrip lines, and the antenna performance degrades as the input signal amplitude and phase diverges from the ideal differential condition. Fig. 5.10 presents the radiation gain variation on the E-plane (y-z plane) at $\theta = 0°$ with either amplitude or phase imbalance on the feed-lines.



(a)



(b)

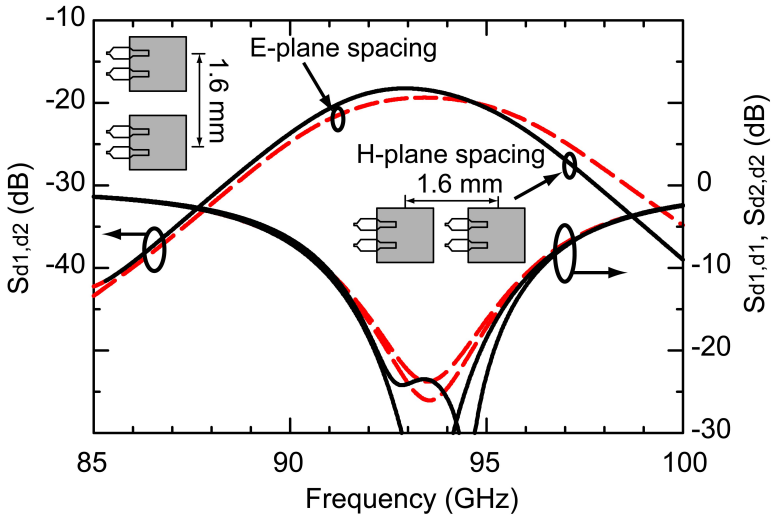
Figure 5.10: (a) E-plane gain variation vs. amplitude offset with 180° phase difference feed-lines. (b) E-plane gain variation vs. phase offset with equal amplitude feed-lines.

A 20 dB amplitude offset on feed-lines is equivalent to an antenna off-center fed with a single-ended line, and it results in radiation patterns composed of two orthogonal radiating modes (see Fig. 5.10(a)). On the other hand, the case of common-mode feeding (360° phase difference with equal amplitude in Fig. 5.10(b)) changes the microstrip antenna resonant mode from the original TM_{010} mode to TM_{100} mode. The common-mode patterns are therefore orthogonal to the differential-mode patterns. Similar results are obtained for the slot-ring antennas.

5.3.5 Mutual Coupling

Mixed mode analysis [91] is applied to analyze the mutual coupling between 2 differential antennas (a 4-port system). $S_{d1,d1}$ denotes the differential-mode return loss of antenna 1 when the input and reflected signals are all differential. On the other hand, $S_{c1,c1}$ represents the common-mode return loss. Also, $S_{d1,d2}$ and $S_{c1,c2}$ denote the differential- and common-mode mutual coupling between two antennas respectively.

The simulated E- and H-plane coupling coefficient versus differential-mode and common-mode excitation with an antenna center-to-center spacing of 1.6 mm ($0.5\lambda_0$ at 95 GHz), and is shown in Fig. 5.11 and Fig. 5.12 for both antennas. For a differential-mode excitation case, the isolation in the H-plane direction is dominated by the antenna spacing and is $>$ 20 dB for microstrip antennas (0.76 mm gap between antennas) and is $>$ 16 dB for slot-ring antennas (0.36 mm gap). The E-plane isolation is dominated by the excited surface-wave TM_0 mode due to the 100 μm thick quartz superstrate and is $>$ 20 dB for both cases. On the other hand, the isolation for both type of antennas is $>$ 25 dB in the common mode excitation. The energy conversion between differential- and common-mode ($S_{d1,c1}$, $S_{d1,c2}$, etc.) is as low as -35 dB and is not shown in the discussion.



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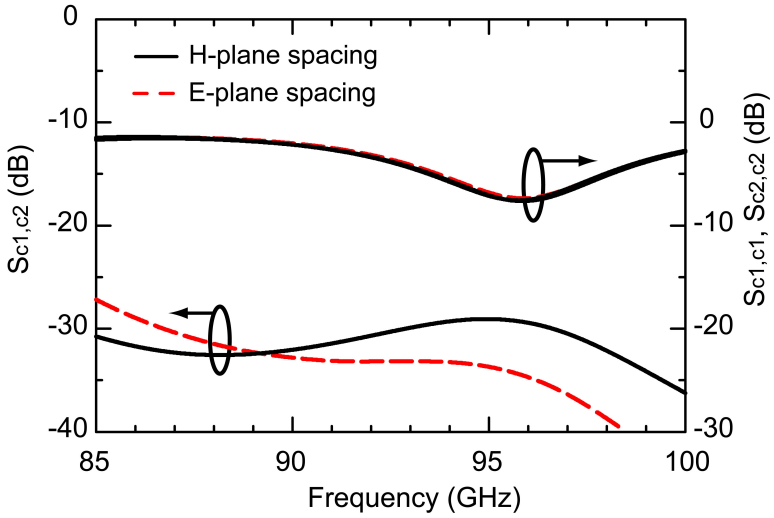
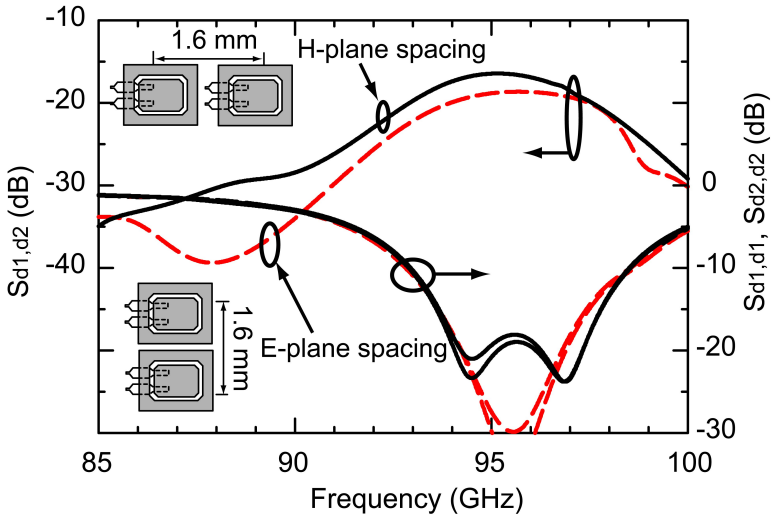
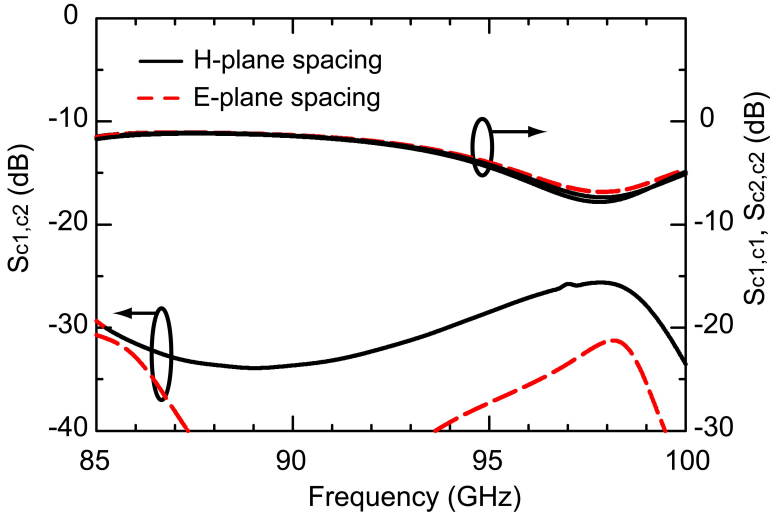


(b)

Figure 5.11: Mixed-mode S-parameters of the differential microstrip antennas: (a) differential mode, and (b) common mode.



(a)



(b)

Figure 5.12: Mixed-mode S-parameters of the differential slot-ring antennas: (a) differential mode, and (b) common mode.

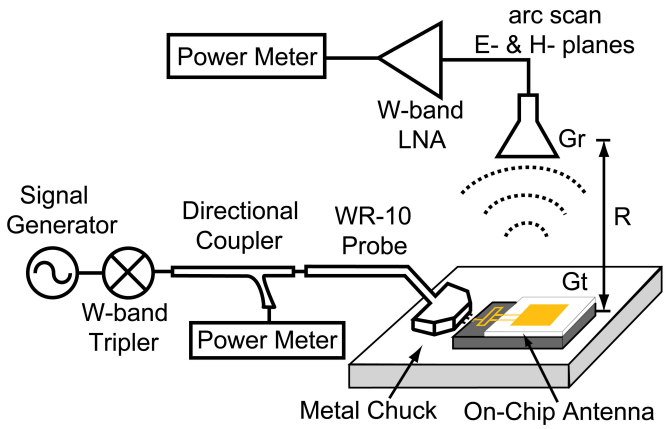


Figure 5.13: W-band measurement setup for the radiation patterns of the differential antennas.

5.4 MEASUREMENTS

5.4.1 Measurement Setup

The input impedance is measured with a mm-wave Agilent network analyzer, and a coaxial probe (GSG = 100 μm pitch) with TRL (Thru-Reflection-Load) calibration at the probe tip. The loss of the on-chip GSG to microstrip transition (0.3 dB) and the on-chip rat-race coupler is included in the measurements. The antenna is placed on a metalized chuck and allowed to radiate into free space with absorbers placed around the antenna.

The pattern and gain of the on-chip antennas are then measured using a far-field waveguide-only setup on a standard probe station (Fig. 5.13). The transmit signal is fed to the AUT (antenna under test) by a WR-10 waveguide-to-GSG probe with a loss of 1.5 dB at 90-100 GHz [79]. The receive antenna is a W-band standard-gain horn antenna with a gain, G_r, of 22.5-23.5 dBi at 75-110 GHz placed at a far-field distance R = 30 cm (62 dB path loss at 94 GHz), and connected to a W-band amplifier with a gain of 20-30 dB at 88-98 GHz (P_{in} = -27$\sim$-30 dBm). The LNA gain is measured accurately using an independent WR-10 waveguide network analyzer. The received RF power is detected using an Agilent W8486A power sensor, and the same power sensor is used to measure the transmitted power using a calibrated waveguide coupler. RF absorbers are used around the chip antenna and the probe station so as to reduce the standing waves

due to the large metal chuck. The gain is referenced to the antenna port (see Fig. 5.15) and the loss of the rat-race coupler is de-embedded from the measurements. The coupler loss is measured independently and is ∼0.8 dB at 90-100 GHz.

The antenna gain is obtained using the Friis transmission formula [**?**]:

$$\frac{P_r}{P_t} = (\frac{\lambda_0}{4\pi R})^2 G_t G_r \tag{5.1}$$

where P_t and P_r are the transmitting and receiving power and G_t and G_r are the gains of the antennas at the respective ports. Due to the presence of the metal chuck and many different calibrations needed for this set-up (transmit power, W-band LNA gain,waveguide coupler, waveguide to GSG transition), the accuracy of the measured gain is estimated to be ±1 dB at 90-100 GHz.

5.4.2 Rat-Race Coupler

The measured S-parameters of the rat-race coupler are shown in Fig. 5.14. The insertion loss measurement is done on 2 different test circuits with one port terminated using an on-chip load. The rat-race coupler shows S_{44} < -20 dB at 88-98 GHz range, with a measured S_{42} = -3.7 dB and S_{43} = -4.0 dB at 94 GHz. There is a constant 3° phase deviation from the simulated phase difference between each path, which is negligible.

5.4.3 Microstrip Antennas

The antenna input impedance is measured by landing the probe at the Δ port of the rat-race coupler with its Σ port 50 Ω terminated, and the other 2 out of phase ports extending as the differential feed-lines. The fabricated quartz superstrate with a printed microstrip antenna is placed on top of the silicon chip using a dot of glue (Cyanoacrylate) at the corners. The simulated antenna S_{11} is a cascaded response of the 180° hybrid and the differential antenna.

The measured S_{11} of sample 1 agrees well with simulations at 86-100 GHz with a -10 dB bandwidth of ∼8 GHz. The shift in the S-parameters of sample 2 is due to the adhesive glue (ϵ_r ∼81) overflowing underneath the antenna and increasing the equivalent dielectric constant.

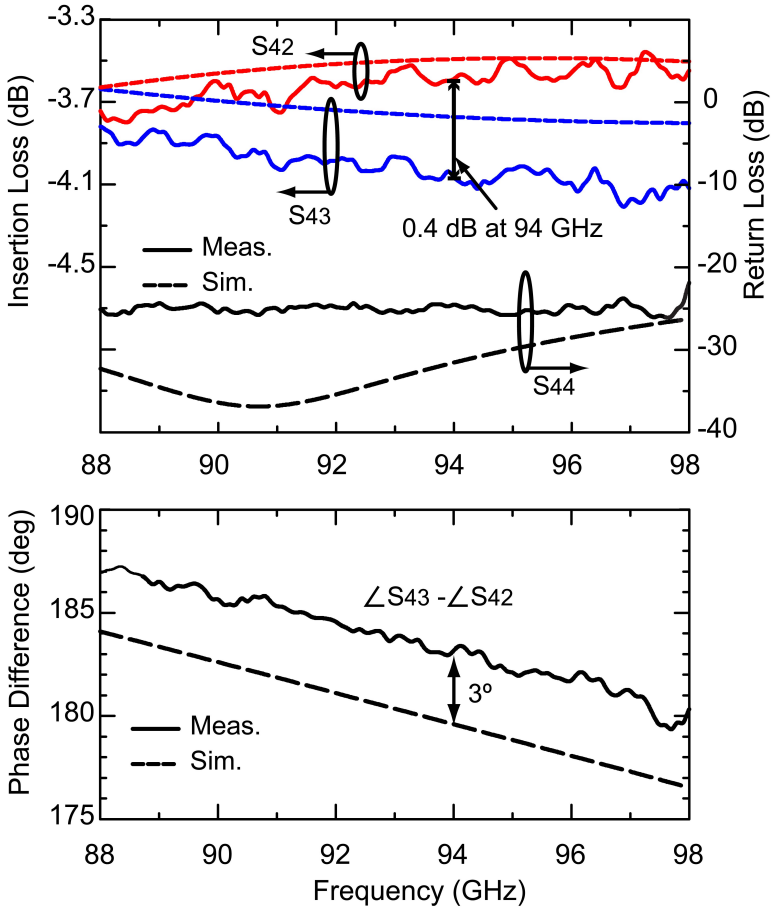


Figure 5.14: Measured and simulated return loss, insertion loss, and phase difference performance of the on-chip miniaturized rat-race coupler.

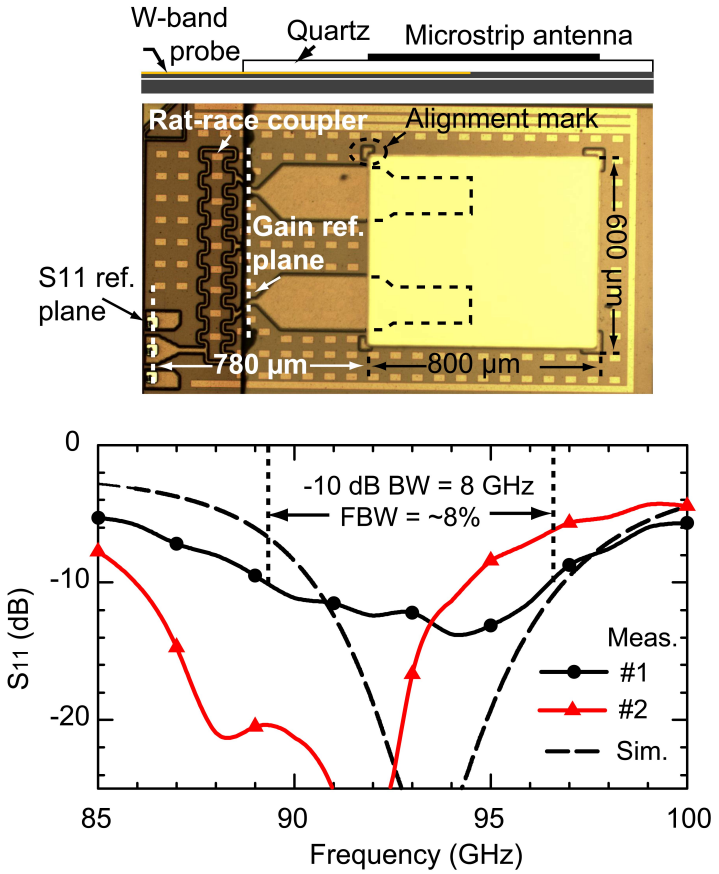


Figure 5.15: Fabricated on-chip EM-coupled microstrip antenna and measured and simulated S_{11}.

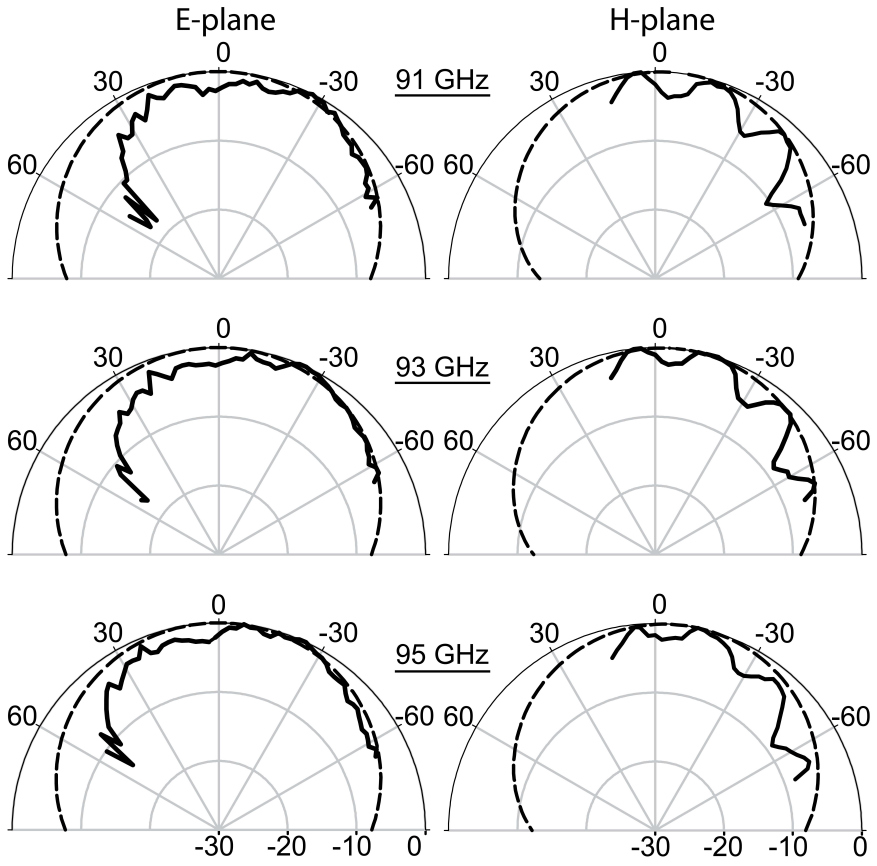


Figure 5.16: Measured (——) and simulated (– – –) E and H-plane radiation patterns of the differential microstrip antenna.

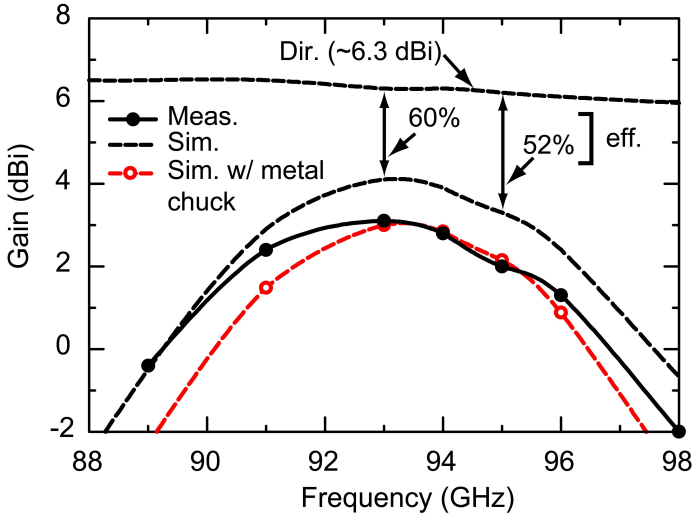


Figure 5.17: Measured and simulated gain of the differential on-chip microstrip antenna.

The simulated and measured radiation patterns are shown in Fig. 5.16. Due to the probe location, the H-plane pattern can only be measured up to $+15°$. One can also notice some scattering in the measured H-plane patterns from the metal-chuck and probe positioner. On the other hand, the measured E-plane patterns are smooth and symmetrical and agree well with simulations. The measured cross-polarization is $<$ -20 dB and is not shown. Fig. 5.17 presents the measured antenna gain at 89-98 GHz. Note that the antenna efficiency on an infinite metal chuck is lower than an antenna on a silicon substrate alone due to power lost to a surface wave on the metal chuck [82]. The microstrip antenna has a simulated efficiency 44-60% (no metal chuck) at 91-96 GHz. The measured gain is 2-3 dBi at 91-95 GHz and agrees well with simulations.

5.4.4 Slot-Ring Antennas

Fig. 5.18 presents a micro photograph of the slot-ring antenna on a silicon substrate and shows the measured input impedance of a -10 dB bandwidth of 89.5-97 GHz. The shift in the measured S_{11} is due to a slight overflow of the adhesive glue. The measured patterns are shown in Fig. 5.19. The cross-polarization is $<$ -20 dB and is not shown. Fig. 5.20 presents the measured gain of the slot-ring antenna. The measured gain is 0-3 dBi at 90-96 GHz. The simulated efficiency is 47-63% at 93-97 GHz.

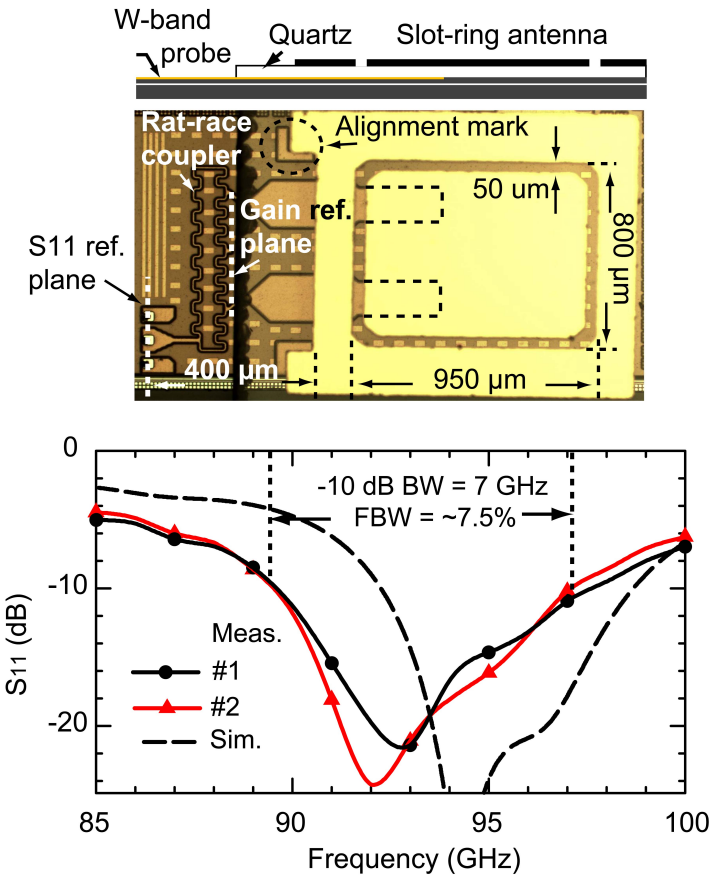


Figure 5.18: Fabricated on-chip EM-coupled slot-ring antenna and measured and simulated S_{11}.

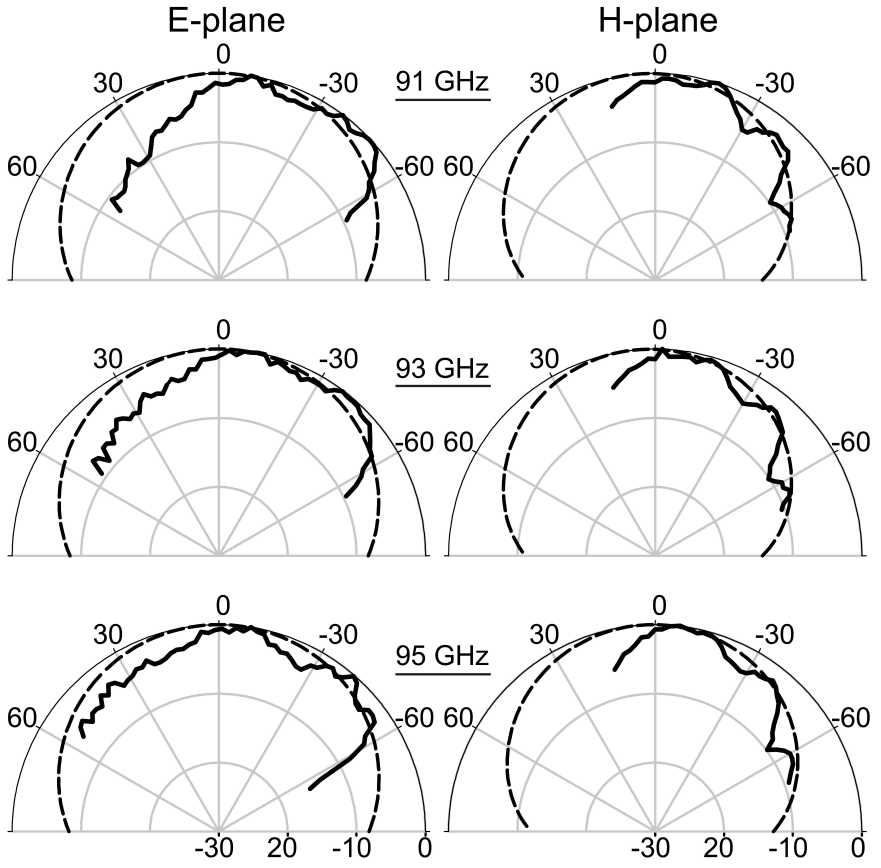


Figure 5.19: Measured (——) and simulated (– – –) E and H-plane radiation patterns of the differential slot-ring antenna.

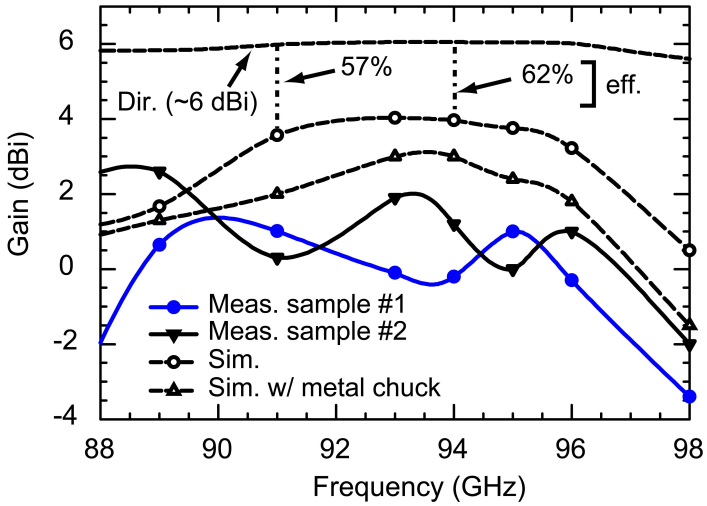


Figure 5.20: Measured and simulated gain of the differential on-chip rectangular slot-ring antenna.

5.5 Summary

High efficiency W-band differential on-chip microstrip and slot-ring antennas have been demonstrated for wafer-scale silicon systems. These antennas are compatible with the new generation of differential LNAs and power amplifiers which are becoming prevalent at millimeter-wave frequencies. The design is not limited to planar superstrates, and can be used with on-chip integrated horn antennas [82] and dielectric lenses [51]. The designs can also be scaled to THz frequencies but with thinner dielectric superstrates, and are ideal for silicon-based focal-plane imaging arrays.

Chapter 5 is mostly a reprint of the material that is submitted for publications in IEEE Transactions on Antennas and Propagation, 2011. Yu-Chin Ou and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 6

Conclusion

6.1 Summary of Work

This thesis presents a high-performance 26-channel channelizer at 20-90 MHz, the first lumped-element tunable bandstop filter with full control of bandwidth and rejection at 500-700 MHz, a on-chip single-ended antenna with a metallic horn extension resulting in the highest gain at W-band to our knowledge and the first high-efficiency differential on-chip antennas at 94 GHz.

Chapter 2 presents a 26-channel channelizer based on the mammalian cochlea and covering the 20-90 MHz band. Each channel has a 6-pole frequency response with a constant absolute bandwidth of 1.4 MHz at 20-30 MHz, and a constant fractional bandwidth of 4.5$\pm$0.6% at 30-90 MHz, and is built entirely using lumped elements. Measurements show an S_{11} $<$ -12 dB at 20-90 MHz, a loss of 4-7 dB, $>$ 40 dB isolation between the channels, and agree well with simulations. The applications areas are in communication systems with very high levels of interferes and in defense systems.

Chapter 3 presents tunable lumped-element bandstop filters for the UHF-band cognitive radio systems. The 2-pole filters are implemented using lumped elements with both single- and back-to-back silicon varactor diodes. The single diode filter tunes from 470 to 730 MHz with a 16-dB rejection bandwidth of 5 MHz and a filter quality factor of 52-65. The back-to-back diode filter tunes from 511 to 745 MHz also with a 16-dB rejection bandwidth of 5 MHz and a quality factor of 68-75. Both filters show a low insertion loss of 0.3-0.4 dB. Nonlinear measurements at the filter null with Δf = 2 MHz

show that the back-to-back diode filter results in 12-dBm higher third-order intermodulation intercept point (IIP3) than the single diode filter. A scaling series capacitor is used in the resonator arm of the back-to-back diode filter and allows a power handling of 25 dBm at the 16 dB rejection null. The cascaded response of two tunable filters is also presented for multi-band rejection applications, or for a deeper rejection null ($>$ 36 dB with 0.6 dB loss at 600 MHz). The topology can be easily extended to higher-order filters and design equations are presented.

Chapter 4 presents on-chip slot-ring and horn antennas for wafer-scale silicon systems. A high efficiency is achieved using a 100 μm quartz superstrate on top of the silicon chip, and a low loss microstrip transformer using the silicon back-end metallization. A finite ground plane is also used to reduce the power coupled to the TEM mode. The slot-ring and 1-λ_0^2 horn achieve a measured gain of 0-2 dBi and 6-8 dBi at 90-96 GHz, respectively, and a radiation efficiency of $\sim$50%. The horns achieve a high antenna gain without occupying a large area on the silicon wafer, thus resulting in a low cost system. The designs are compatible with either single or two-antenna transceivers, or and with wafer-scale imaging systems and power-combining arrays.

Chapter 5 presents on-chip differential microstrip and slot-ring antennas. The antennas are fed at the non-radiating edge which is compatible with differential coupled-lines, and are built on a 0.13-μm CMOS process with a layout which meets all the metal density rules. A high radiation efficiency is achieved using a 100 μm quartz superstrate placed on top of the silicon chip. Both antennas achieve a measured gain of $\sim$3 dBi at 91-94 GHz, with a -10 dB S_{11} bandwidth of 7-8 GHz and a radiation efficiency of $>$50%. The designs are compatible with single and multi-element transceivers, and with wafer-scale imaging systems and power-combining arrays.

6.2 Future Work

The channelizer topology is readily extended to other frequency ranges and bandwidths. Surface mount technology can be used up to about 2 GHz, while lumped-element planar monolithic or hybrid circuits can be used from 2 to 6 GHz. Higher frequency applications could be extended with distributed microwave filters. The chan-

nelizer performance, limited by the resonator Q of the components and the insertion loss of the channel filters, could be enhanced using high-Q inductors and metallic shielding to reduce the energy leakage loss.

Opportunities of future work in the tunable bandstop filter involve the increase of compactness and linearity. The filter prototype could be improved with MEMS switching capacitors which provides high linearity and high power handling capacity.

On-chip antennas electromagnetically coupled through superstrate has shown a > 50 % efficiency which are suitable for W-band applications. End-fire radiation antennas and wider bandwidth antennas are the next goals in order to explore this feeding technique further. In the end, a very high level of integration with all RF active and passive circuits on an IC chip, as single elements or arrays, with high performance and low cost, is the ultimate goal for millimeter-wave radios.

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