Title
A MULTICHANNEL, HIGH LINEARITY CURRENT DIGITIZER FOR DIGITAL SUBTRACTION ANGIOGRAPHY

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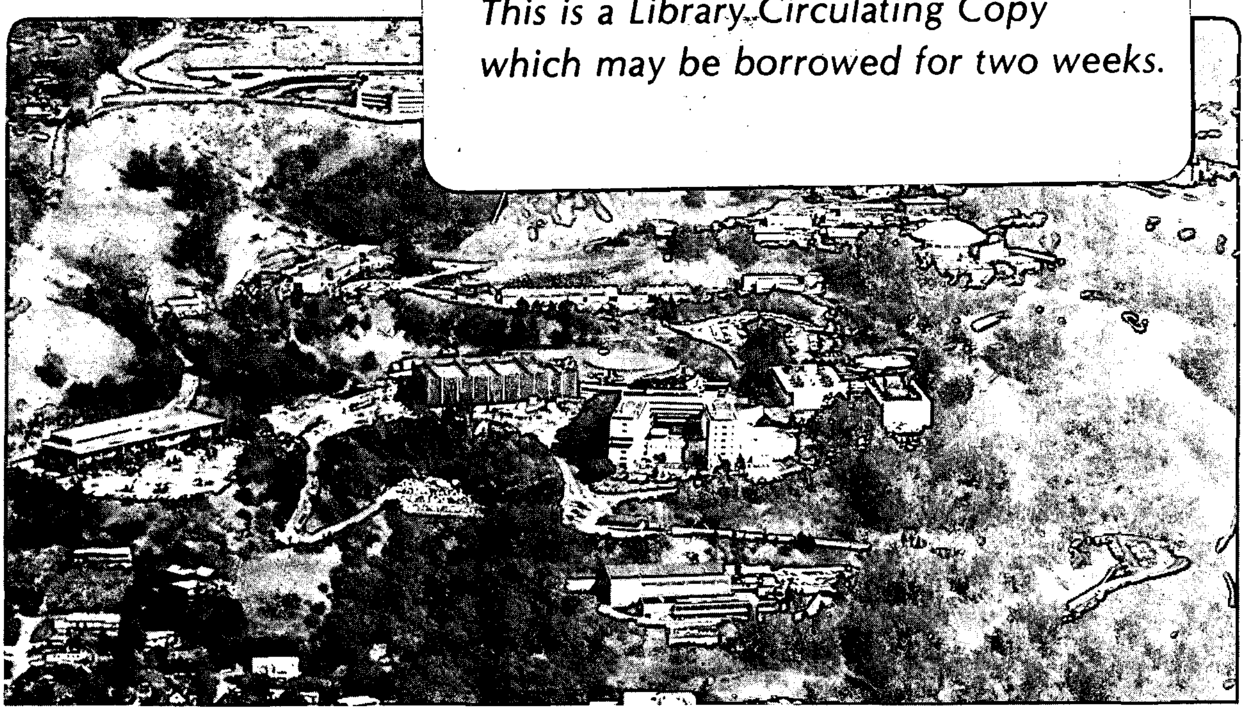

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DISCLAIMER

A MULTICHANNEL, HIGH LINEARITY CURRENT
DIGITIZER FOR DIGITAL SUBTRACTION ANGIOGRAPHY

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Abstract

An experiment studying the application of synchrotron radiation for transvenous coronary angiography requires special electronics to read out a 600 element Si(Li) detector. To obtain high image quality, the electronic system must digitize the current in all 600 elements every 2 ms with a dynamic range of 40,000 and a maximum non-linearity of 0.02%. Each channel of electronics contains a current-to-voltage amplifier with computer controlled gain and offset followed by a voltage-to-frequency converter used in the reciprocal counting mode. A high speed digital readout method using a lookup table, digital multiplier and direct memory interface was developed. The entire system has been designed to have a low cost per channel and to be easily expanded to 1200 signal channels.

Introduction

The only viable method that currently gives diagnostic quality images of the coronary arteries requires the insertion of an arterial catheter until the catheter tip is near the orifice of the coronary artery and then the injection of undiluted contrast agent while a series of x-rays are taken. This procedure is much too dangerous for routine medical use and is used only when significant medical problems are indicated. A less invasive method to visualize coronary arteries would be a significant medical advance.

The monochromatic, high intensity, collimated x-ray beams available at synchrotron radiation facilities permit the acquisition of x-ray radiographs at different x-ray energies. This allows enhancement of the contrast in x-ray images due to the contrast agent. Using these x-ray sources it may be possible to obtain diagnostic quality coronary angiograms using a venous injection of contrast agent. If successful this method would be much safer and would then allow serial studies of the coronary circulation in patients. The natural development of the atherosclerotic process and its response to preventive measures could then be studied. The technique used with synchrotron radiation is based on the fact that the contrast agent is an iodine containing compound. Two images are acquired above and below the iodine K x-ray absorption edge at 33.17 keV where the x-ray absorption cross-section of iodine jumps by a factor of 6. The logarithmic difference image of these two images then has greatly enhanced contrast to iodine and minimal sensitivity to intervening tissue and bone.

A prototype system using a 300 element detector has produced very promising results.[1,2,3,4] Figure 1 shows shows a set of images that were obtained by the Stanford/LBL/SSRL/Brookhaven group at the Stanford Synchrotron Radiation Laboratory in April 1986. The dog was placed in a lateral position, and the images shown were taken 6 seconds after venous injection of contrast agent (0.75 ml per kg) in the superior vena cava. The total exposure time for each pair of line images was 4 ms, and the time to acquire an image, including starting and stopping the scanning chair, was 2 seconds. The average x-ray fluence was 1×10^9 photons per second per pixel, and the x-ray exposure of the dog was therefore 89 mrad per frame. Figure 1a is the image taken with an x-ray energy just below the iodine K edge, Fig. 1b is a similar image just above the edge and Fig. 1c is the difference image in which the arteries are clearly visible. The new electronic system described in this paper is designed for use at a new angiography facility that is being built as part of a new superconducting wiggler beamline at the Brookhaven National Synchrotron Light Source. It will be used with a 600 element Si(Li) that is being fabricated by the Silicon Detector Group of the Lawrence Berkeley Laboratory.[4]

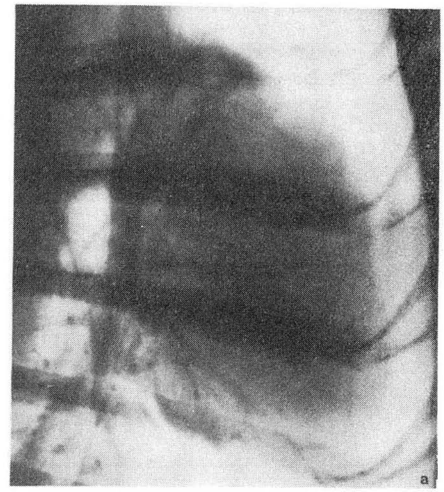

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Fig. 1a. X-ray radiation below the iodine K absorption edge for a dog's heart.

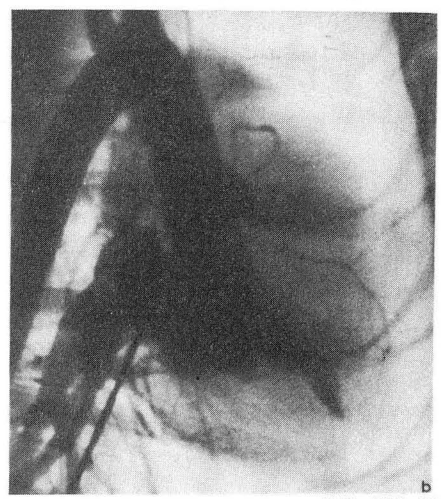

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Fig. 1b. X-ray radiation above the iodine K absorption edge for a dog's heart.

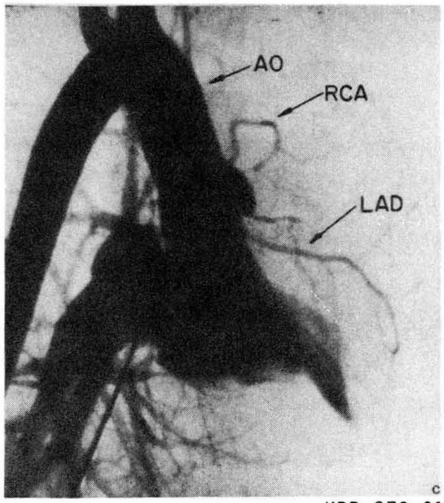

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Fig. 1c. Logarithmic difference image for a dog's heart.

Imaging System

Figure 2 is a schematic drawing of the new imaging system. Images are obtained in a line scan fashion (much like a focal plane camera) by moving the patient vertically at constant speed. The system is therefore an electronic system with "snap shots" from the two linear arrays being recorded digitally.

The transmitted x-rays will be measured with a 600 element Si(Li) detector that is being made from a single crystal of silicon. The device has an active area 150 mm long, 10 mm wide and 5 mm thick. It has a dual array of detector elements 0.4 mm wide and 4 mm high with a center-to-center spacing of 0.5 mm. There are 300 elements in each row and each element is separately connected to a contact strip on a circuit card by wire bonding. The detector is mounted in a vacuum cryostat so that the device can be cooled to -30° C to lower the average leakage current per element to less than 300 pA.

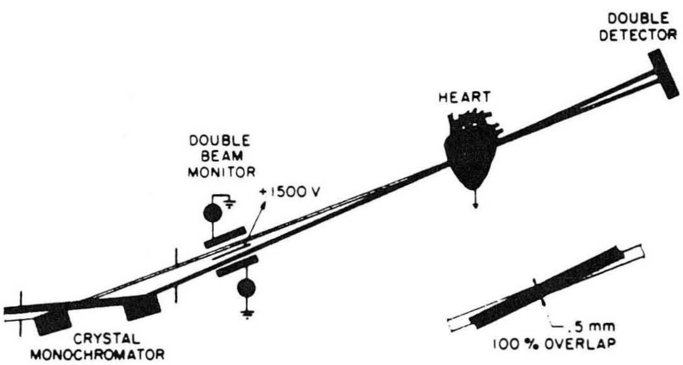

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Fig. 2. Schematic drawing of dual array detector imaging system.

Electronic Readout System

Since the patient is moved vertically at speeds up to 24 cm/s, the electronic readout system must be capable of accurately measuring the current in all 600 elements in less than 2 ms.

The requirements for the electronic system are:

1. Low input noise when compared to the thermal noise of the detector.
2. High processing speed since the current in all 600 elements must be measured every 2 ms.
3. Large dynamic range since the current is reduced dramatically when the beams are going through a bone.
4. Very high linearity since the important signal is the logarithmic difference between pairs of detector elements.

An individual channel of the current-to-frequency circuit is shown in Fig. 3. The low noise requirement is met by using a pair of OP-07's, an industry-standard operational amplifier. This is demonstrated in Fig. 4 where the noise contribution of the OP-07 is shown to be very small when compared to the thermal noise of the detector interelement surface resistance which is approximately 70 kΩ. A set of three FET switches is used to set the gain from the control computer. The full scale current can be varied in 8 steps from 40 to 5000 nA. A calibration input is provided by the buffered output of a 16 bit digital-to-analog converter so that the linearity and current gain of each channel can be measured by the computer.

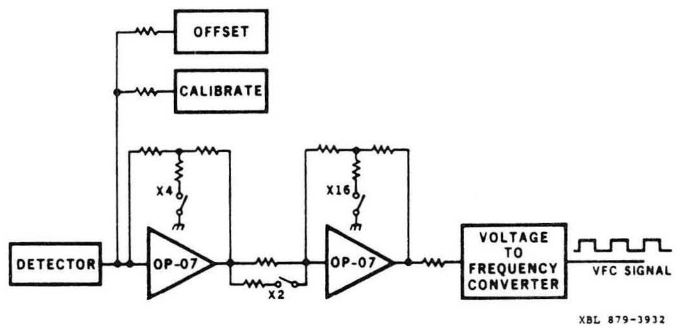

Fig. 3. Individual channel current-to-frequency converter circuit.

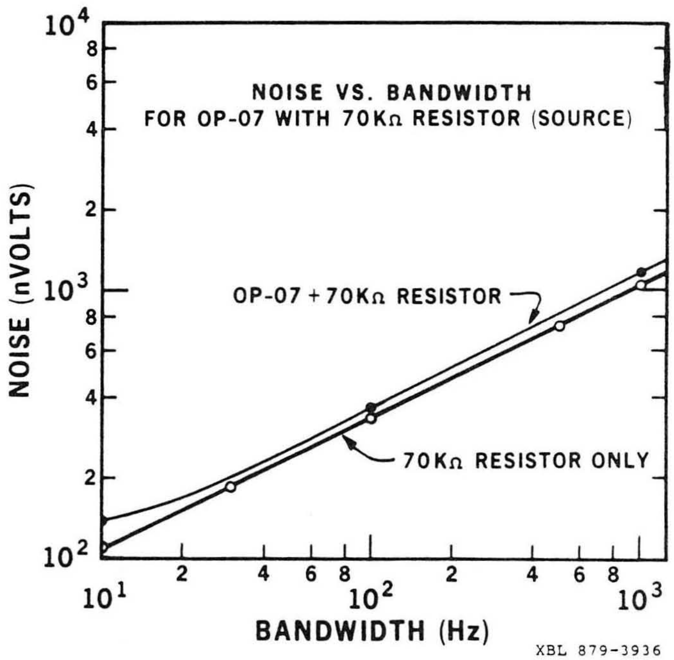

Fig. 4. Op-07 and 70 kΩ resistor noise plot.

The high speed, wide dynamic range and low non-linearity requirements are met by using a voltage-to-frequency converter (VFC) on each channel. However, rather than using an expensive 20 MHz VFC with a conventional counter readout, a low cost 500 kHz VFC is used in the reciprocal counting mode.[5,6] In this mode two counters are used. One counter measures the number of VFC pulses during a gate period. The other counter measures the number of high frequency clock pulses that occur during the same gate period. Reciprocal counting essentially measures the average period of the VFC output and uses the reciprocal of the period to compute the frequency.

The digital circuit to implement the reciprocal counting technique is shown in Fig. 5a. An external timing gate (Gate1) is connected to the D-input of a synchronizing flip flop on every channel. On the next positive going edge of the VFC signal, the output of the synchronizing flip flop will set to gate the master clock (M count) and the VFC signal (V count) to the M and V counters, respectively. The master clock, at 20 MHz, is many times the maximum frequency of the VFC. Since the internal gate (Gate2) is synchronized with the VFC signal, only an integer number of V counts will occur during Gate2, see Fig. 5b. The M count is not synchronized and therefore will have an uncertainty of plus or minus 1 count.

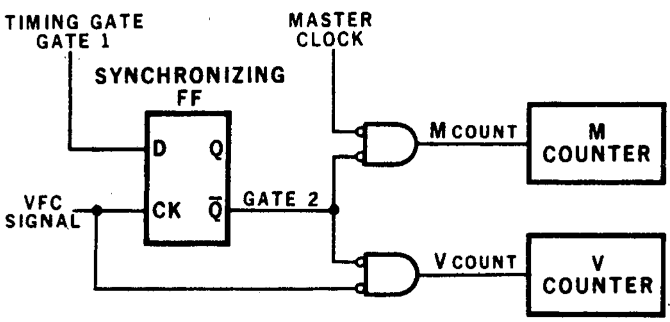

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Fig. 5a. Digital circuit to implement reciprocal counting technique.

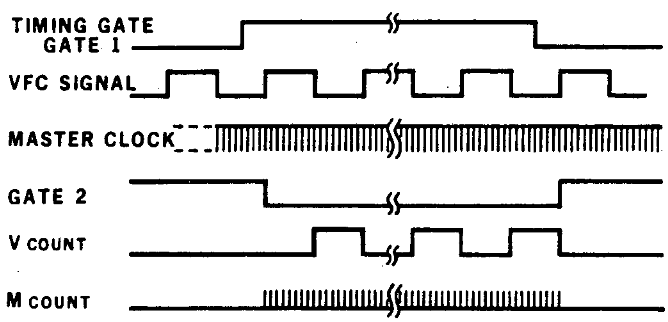

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Fig. 5b. Reciprocal counting technique timing diagram.

The frequency of the VFC signal is given by:

$$\text{Freq. of VFC} = \frac{(\text{V count/Gate2})}{(\text{M count/Gate2})} \times \text{Freq. of master clock}$$

Note that, in the above equation, Gate2 cancels algebraically. Therefore the VFC frequency is proportional only to the ratio of the accumulated V and M counts. If a stable high frequency master clock is used, we are able to compute the VFC frequency with very good resolution, even for very short gate times. For example, during a gate period of 2 ms, a 20 MHz master clock will generate 40,000 M counts. Hence, the VFC frequency can therefore be computed to an accuracy of +/- 1 part in 40,000.

Figure 6 is a block diagram of the digital electronics system which computes an equivalent VFC frequency for each channel and transfers the result to the computer. Both counters have tri-state output buffers so data for one image line can be taken while the data from previous line is processed. This system has the capability to transfer a data word in a time as short as one microsecond. Therefore, even a 1200 element line image can be processed in less than 2 ms. To compute an equivalent VFC count, the data from each pair of M and V counters is sequentially accessed. The M count data, which varies around 40,000 counts by +/- 5%, is used to compute an EPROM address. The EPROM (4k by 16 bits) is programmed with a lookup table consisting of a multiplier constant divided by M counts. Both the V count and EPROM output data are then latched into a 16 x 16 multiplier. The 16 most significant bits of the 32 bit product are then transferred via the DMA FIFO interface to the computer. Finally, the channel address is incremented to initiate a DMA transfer and start processing data from the next channel.

A prototype of the electronic readout system has been built and tested with a precision current source. A maximum non-linearity of 0.02% and a resolution of 1 part in 40,000 was achieved. In addition, the ability to transfer 1200 channels in less than 2 ms was demonstrated.

Conclusions

This readout system, using the reciprocal counting technique, has proven to provide excellent performance at reasonable cost. The system has a dynamic range of 40,000 and a maximum non-linearity of 0.02%. Using a buffered direct memory access interface, one can process and transfer up to 1200 channels every 2 ms. Since the system is modular in design, an arbitrary number of channels is possible. Expansion of the current system from 600 to 1200 signal channels to achieve higher spatial resolution is planned.

This method of data acquisition and transfer may be useful in other applications where many channels are to be measured at high speed with good resolution, large dynamic range, and excellent linearity.

Acknowledgments

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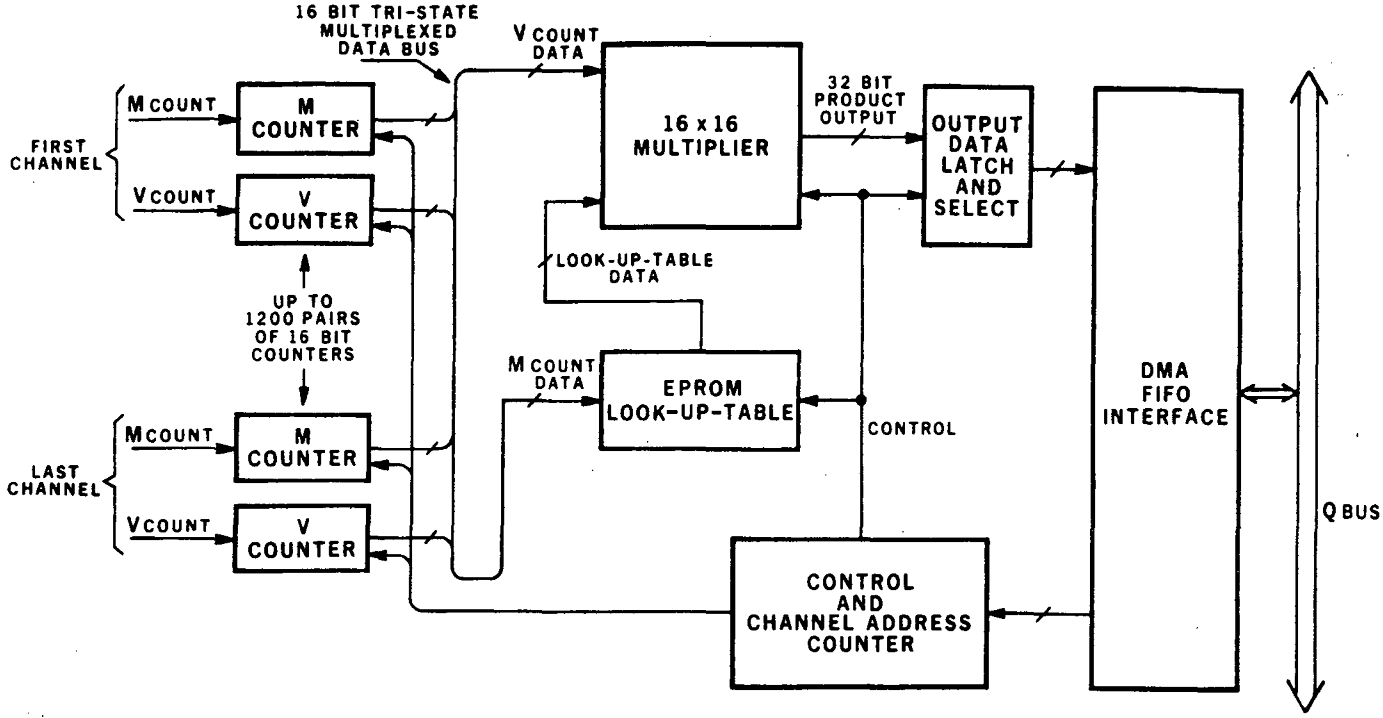

Fig. 6. Block diagram of electronics to compute equivalent VFC frequency and transfer the result for each channel by DMA to computer digital circuit to implement reciprocal counting technique.

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