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Interference-Resilient CMOS Receiver Front-Ends for Next Generation Radios

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Interference-Resilient CMOS Receiver Front-Ends for Next Generation Radios

by

Sashank Krishnamurthy

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Committee in charge:

Professor Ali M. Niknejad, Chair
Professor Borivoje Nikolić
Professor Martin White

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Abstract

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Doctor of Philosophy in Engineering - Electrical Engineering and Computer Sciences

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In accordance with the trend of one generation of wireless mobile telecommunications technology every decade since the 1980s, the 2020s belong to 5G, the fifth generation. 5G is expected to provide a diverse range of services from enhanced mobile broadband at multi-gigabit per second, to supporting the massive Internet of Things revolution. While all the generations up to 4G used the frequency spectrum below 3GHz, 5G is expected to support communication on a wide range of spectrum, ranging from low-bands from 0.6-6GHz and mm-wave bands greater than 24GHz. Forecasts of hundreds of billions of connected devices by 2030 mandate the need for circuit-level techniques to mitigate the increasing interference that comes with this proliferating number of devices. To this end, we investigate techniques to make highly linear, interference resilient CMOS radio receiver front ends for three different application thrusts: sub-mW IoT applications, sub-6GHz 5G applications and mm-wave digital beamforming applications.

The need to operate radios connected to the IoT off tiny coil cell batteries has driven the recent research on sub-mW radio receivers. While existing work has focused on improving sensitivity of the receivers in a power efficient manner, there has been little focus on making them interference resilient. In the first part of this dissertation, we demonstrate a 2.4GHz radio receiver with 10x better interference resilience than the state-of-the-art sub-mW radios in the 2.4GHz ISM band, without compromising much on the sensitivity. We present a proof-of-concept integrated circuit in 28nm bulk-CMOS process and present the in-silicon results.

The ever-increasing number of bands with the advent of sub-6GHz 5G calls for high linearity receiver front-ends, with extremely high tolerance for blockers, both in close-in channels and far-out channels. Current solutions in mobile phones involve the use of multiple SAW and FBAR filters for different bands, making them extremely bulky. The re-discovery of N-path filters, with their impedance translational property, provides a path to SAW-less receivers. In the second part of the dissertation, we demonstrate enhanced N-path filter based receivers, achieving 40dB/decade, 60dB/decade and 80dB/decade RF selectivity. Techniques

to synthesize higher order driving point impedances, including the first ever known synthesis of a third order driving point impedance, are presented. Coupled with distortion cancellation techniques, record performance is achieved with respect to close-in blocker resilience. Experimental results from three separate integrated circuit prototypes in 28nm bulk CMOS confirm the benefits of our techniques.

Millimeter-wave massive MIMO arrays are expected to be an enabler of 5G. To this end, it is desirable to have digital beam-forming arrays with high spatial flexibility. This calls for highly linear RF front-ends to cope with in-band interferers. In the last part of the dissertation, we present a 10-35GHz passive mixer-first receiver for use in digital beamforming arrays. Circuit techniques are proposed to enhance the linearity of such receivers, both at baseband and the RF mixer switches. Experimental results from an integrated circuit prototype in 28nm bulk CMOS demonstrate record in-band linearity at these frequencies.

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I would not have been attracted to the field of IC design during my undergraduate days, if not for Prof. Shanthi Pavan and Prof. Nagendra Krishnapura of IIT Madras. Today, while it is the trend d'jour to be attracted to greener pastures, it was impossible not to be smitten with the way famed duo of Prof. Shanthi and Prof. Nagi made circuits come alive on the blackboard. Prof. Shanthi was also my advisor for my undergraduate thesis. Apart from the solid technical grounding I gained, Prof. Shanthi also instilled in me a sense of professionalism in the way I present my results to others. Every year when we meet at ISSCC, he takes a deep interest in my research and spends a significant time discussing my work. I have been lucky to be advised by the world's leading expert in data converters during my undergraduate studies and the world's leading expert in RF and mm-wave circuits during my PhD. Also, I wish to thank Prof. Borivoje Nikolic, Prof. Martin White and Prof. Elad Alon for taking the time to serve on my qualifying exam committee and dissertation committee, and provide feedback.

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It is well-known that during a PhD, you learn as much from your labmates as from your advisor. I had the good fortune of being able to learn from some very solid IC designer

colleagues. First and foremost, I wish to thank Andrew Townley, who took me under his mentorship for the first year and a half of my PhD, and taught me the ropes of doing good circuit layout. Despite his busy schedule as a senior PhD student, he always had time for me. I wish to thank Lorenzo Iotti, with whom I have had several fruitful collaborations in N-path filter work. I am grateful for all the auxiliary circuit IP which he graciously shared with me, knocking a good few months off my PhD. I also wish to thank Nima Baniasadi, for all his help on anything to do with electromagnetic simulations and teaching me how to use a probe station. I wish to thank Kosta Trotskovsky for taking an active interest in my development as a PhD student during my early years and Filip Maksimovic for a fruitful collaboration on the low-power work. I wish to thank Ali Ameri, who was my partner for all the course projects during the first year in addition to being a good friend and my ping-pong partner. Finally, I wish to thank other seniors in our lab, Greg LaCaille, Lucas Calderin and Nai-Chung Kuo.

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Chapter 1

Introduction

In accordance with the trend of one generation of wireless mobile telecommunications technology per decade since the 1980s [7], the 2020s belong to 5G, the fifth generation. 5G is expected to provide a diverse range of services from enhanced mobile broadband at multi-gigabit per second, to supporting the massive Internet of Things revolution. While all the generations up to 4G used the frequency spectrum below 3GHz, 5G is expected to support communication on a wide range of spectrum, ranging from low-bands from 0.6-6GHz and mm-wave bands greater than 24GHz. Forecasts of hundreds of billions of connected devices by 2030 [8] mandate the need for circuit-level techniques to mitigate the increasing interference that comes with this proliferating number of devices.

At the network level, this problem is solved by re-transmitting packets which are not transmitted successfully in the presence of an interferer [9]. However, re-transmissions increase latency and therefore, it is desirable to build RF front-ends which are interference resilient. Additionally, with the growing number of bands with the advent of 5G, mobile devices need to support all the new bands [7] in addition to existing 3G, 4G and Wi-Fi bands. Also, different parts of the world have different bands, making multi-band support even more challenging.

Current solutions involve the use of multiple surface acoustic wave (SAW) and thin-film bulk acoustic resonator (FBAR) filters. Both of these work on the principle of transduction of acoustic waves, where piezoelectric materials are used for the transduction from electrical to mechanical energy [10]. While SAW filters typically support only frequencies up to around 1.5GHz [10], FBAR filters can be used for frequencies up to 10GHz. However, since these filters are not tunable, multi-band support would require a large increase in the number of such filters on the mobile device. Apart from the cost and the area footprint, these filters are also quite lossy and can exhibit up to 3dB insertion loss [1]. However, they do provide extremely sharp front-end filtering as evidenced by the transfer functions of some commercial SAW filters, shown in Fig. 1.1.

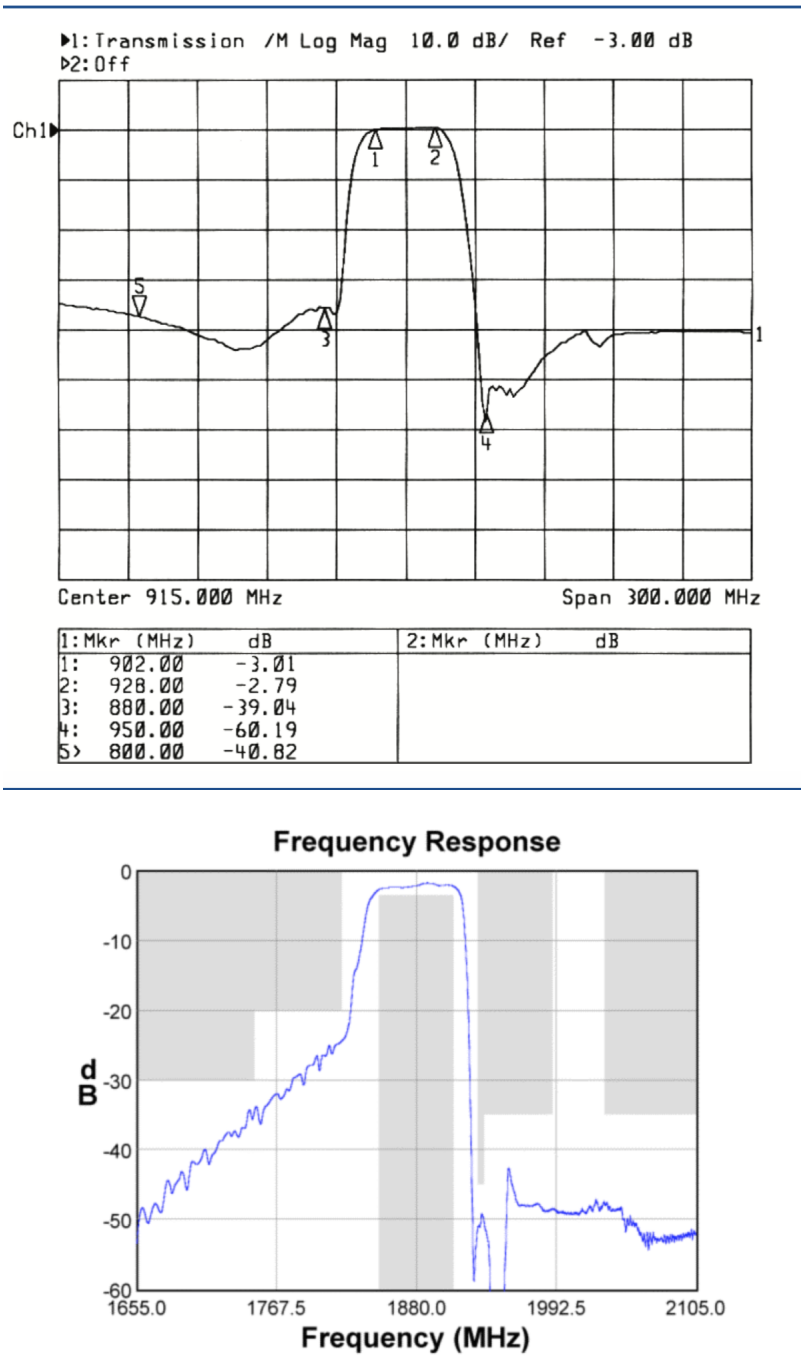


Figure 1.1: s_{21} transfer functions of some typical commercial SAW filters [1, 2].

The N-path filter was first demonstrated as early as the 1950s [11, 12]. It was re-discovered a decade back [13, 14], and is the ideal candidate for the SAW-less receiver. In essence, the N-Path filter consists of N paths of switched-RC kernels. As analyzed extensively in [15–18],

this switched-RC circuit behaves as a passive mixer, when switched at a frequency ω_S much higher than $1/RC$, the time constant of the switched-RC kernel. The N-path filter has the interesting property of impedance translation, as illustrated in [19]. A conventional N-path filter (see Fig. 1.2), like the one described in [19] translates a shunt RC impedance from baseband to RF, enabling the realization of programmable band-pass filters, whose center frequency is exactly equal to the LO frequency f_{LO} at which the mixer switches are driven. However, while promising, these can achieve only 20dB/decade RF selectivity and are no match to the superior filtering provided by SAW filters.

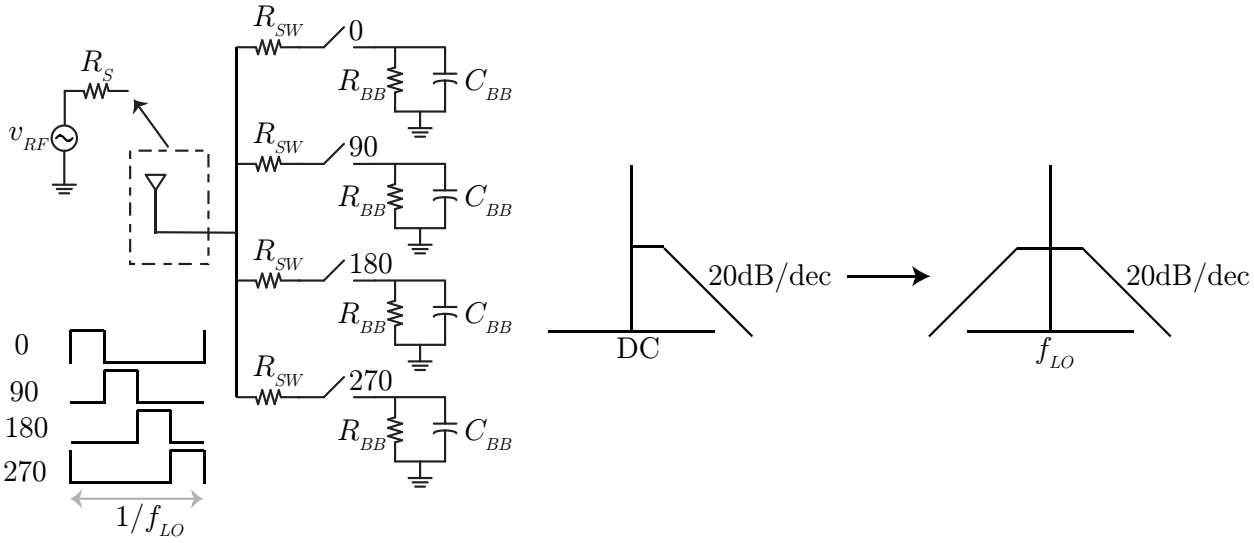


Figure 1.2: Schematic of an N-path filter based receiver illustrating impedance translation property.

An important "promise" of 5G is to offer enhanced user experience with 100x end user data rates and lower latency, by exploiting the spatial dimension of communication using multiple antennas at the transmitter and receiver [20, 21]. To serve multiple users (K) simultaneously, massive MIMO (Multiple-Input Multiple-Output) systems have base-stations with large number of antennas M, with $M \gg K$ [22]. MIMO systems with a small number of concurrent beams [23–25] have used RF phase shifters for spatial filtering, in an attempt to save LO and baseband power. However, for massive MIMO arrays which serve a larger number of users, higher degree of spatial flexibility is desired. The $K \times M$ number of phase shifters required in multi-user MIMO systems makes the implementation of vector interpolator based active RF phase shifters [23, 24] prohibitively power hungry. Use of passive transmission line based phase shifters [25] results in loss and a large area penalty.

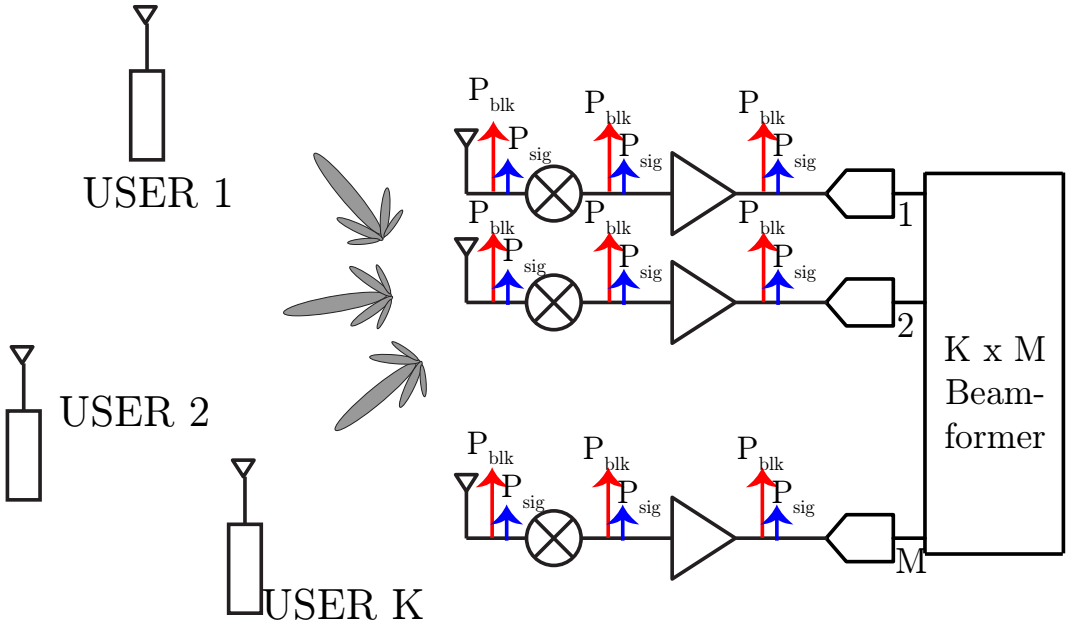


Figure 1.3: Digital beamforming receiver array for massive MIMO systems.

To this end, it is desirable to have massive digital beam-forming arrays for systems with high spatial flexibility. As spatial filtering of out-of-beam, in-band interferers is performed at the baseband, the RF front-end needs to be highly linear to handle these interferers (see Fig. 1.3), posing yet another circuit design challenge.

This dissertation attempts to provide some solutions to several of the problems described thus far by building N-path filter based interference resilient RF receiver front-ends. The five different receiver front-end ICs (integrated circuits) demonstrated in this dissertation target three separate application thrusts: one front-end for sub-mW IoT applications, three front-ends targeting sub-6GHz 5G applications and one targeting mm-wave digital beam-forming applications.

The first part of this dissertation deals with interference resilient CMOS receiver front-ends for low power internet-of-things (IoT) applications. In Chapter 2, a sub-mW 2.4GHz receiver front-end is presented. The front-end consists of a capacitively cross-coupled common gate LNA, with translational positive feedback from baseband to RF through a 4-phase switching mixer, providing RF filtering and matching, in conjunction with an input transformer. A detailed analysis of the architecture is presented, highlighting the design trade-offs between noise, out-of-band filtering and power. A prototype integrated circuit, fabricated in 28nm CMOS, demonstrates a record out-of-band IIP3 of +3.3dBm for sub-mW 2.4GHz receiver front-ends. The content in Chapter 2 is an extended version of the content presented in [26].

The second part of this dissertation, covering chapters 3 through 5, presents enhanced N-path filter-based receivers. These consist of N-path filters loaded by driving point impedances

with a steeper roll-off than the 20dB/decade presented by a shunt RC impedance, which is the load for a conventional N-path filter. These provide a pathway to the SAW-less receiver for sub-6GHz 5G applications. In Chapter 3, a "second order" passive mixer-first receiver is proposed to improve channel selectivity, linearity and noise figure in the presence of out-of-band blockers, by presenting an impedance which rolls off at 40dB/decade as the load to an N-path filter. The synthesis of this impedance is described in a step-by-step manner starting from the required impedance transfer function to its actual circuit realization. Various trade-offs and limitations of the architecture are described in detail, and layout related techniques are also provided. Two integrated circuit prototypes were fabricated in 28nm bulk CMOS as proof of concept for this circuit, including a low-power version. The receiver, capable of broadband operation from 0.2-2GHz, achieves an out-of-band IIP3 of +33dBm and a blocker P1dB of +12dBm. Chapter 3 contains the material found in [5].

Chapter 4 presents a "third-order" passive mixer-first receiver to improve channel selectivity and resilience to close-in blockers, by building an N-path filter which drives an impedance with 60dB/decade roll-off. A step-by-step derivation is provided for the synthesis of the first ever driving point impedance with 60dB/decade roll-off. An integrated circuit prototype was fabricated in 28nm bulk CMOS as proof-of-concept, and characterized. The receiver front-end, capable of broadband operation from 0.2-4.5GHz, demonstrates third-order filtering of close-in blockers and achieves an out-of-band IIP3 of +21dBm and B1dB of greater than 6dBm for blockers at the alternate channel. Chapter 4 contains the material found in [6]

Chapter 5 extends the work on the third order N-path filter of Chapter 4, by demonstrating an enhanced N-path filter-based receiver with 80dB/decade RF selectivity and distortion cancellation to improve channel selectivity and resilience to adjacent channel blockers. An integrated circuit prototype is fabricated in 28nm CMOS as proof-of-concept, and characterized. The front-end, capable of operation from 0.2-3.5GHz, shows a close-in roll-off of 80dB/decade. It achieves a record adjacent channel B1dB of +8dBm, alternate channel B1dB of +10dBm and adjacent channel IIP3 of +23dBm.

The last part of this dissertation focuses on building high linearity receiver front-ends for mm-wave digital MIMO applications. In Chapter 6, a 10–35GHz passive mixer-first receiver is proposed for use in digital beam-forming arrays. Techniques are proposed to enhance the linearity of such receivers, both at baseband and the RF mixer switches. Techniques to mitigate charge sharing due to LO overlap are also proposed. Detailed simulation results are provided to illustrate the benefits of these techniques. An integrated circuit prototype is fabricated in 28nm bulk CMOS and fully characterized. The receiver has built-in programmability to trade-off gain for linearity. The receiver achieves a peak in-band IIP3 of +14.1dBm, a peak gain of 14.5dB and a noise figure of 12.5dB, in its nominal setting. Chapter 6 is an extended version of the material presented in [27]

In Chapter 7, we conclude by presenting the key academic contributions of this dissertation and also providing several avenues for future research to build on the work done in this dissertation.

Chapter 2

Sub-mW Interference-Resilient Receivers for IoT Applications

2.1 Introduction

With the advent of the Internet-of-Things (IoT) revolution, the number of connected devices is expected to surge up to 500 billion by 2030 [8]. This rapid increase calls for the use of radios with extended battery lives, leading to research in radios with sub-mW power consumption. Additionally, the large number of devices also leads to mutual interference between them. Therefore, there is a need for sub-mW interference tolerant radio receivers.

There is an abundance of work in enhancing interference resilience of receiver front-ends, based on N-path filters [13, 28–30]. However, these are targeted at SAW-less LTE and sub-6GHz 5G applications, and hence consume tens to hundreds of milliwatts of power.

The state-of-the-art sub-mW receiver front-ends [31–35], for the 2.4GHz and 915MHz ISM bands, all have LNA based front-ends, and use techniques to achieve improved noise figure (and sensitivity) at low power. While [32, 33] consume power as low as 64μW and 282μW and show modest noise figures of $<$ 9dB, their IIP3 is as low as -21 to -28dBm. [34] demonstrated a receiver with moderately better IIP3 (-15.8dBm) and much higher gain (55dB) at a power consumption of 600μW. However, the NF was worse at 15.1dB. [31, 35] demonstrated the possibility of noise cancellation at low power, demonstrating noise figures of 6.55dB and 2.8dB respectively at powers as low as 230μW and 475μW respectively. While [31, 35] did demonstrate improved linearity with an IIP3 of -10dBm, all of [31–35] had broadband input matching. The only RF filtering, if any, was provided by the finite bandwidth of the input matching network. Therefore, up to such frequencies where the matching network starts to cause input attenuation, the out-of-band IIP3 of [31–35] are as low as -28 to -10dBm (approximately the same as their in-band IIP3).

RF filtering is a characteristic of any passive mixer due to the translation of the first order low-pass impedance from baseband to RF [19]. However, the amount of RF filtering is determined by the size of the switches used in the passive mixer, and hence the LO power.

The far-out attenuation cannot be lower than $R_{SW}/(R_{SW}+R_S)$ [36], where R_{SW} is the ON resistance of the mixer switch and R_S is the source impedance. [37] used a transformer to step-up the source impedance from 50Ω, enabling the use of smaller switches in the passive mixer which followed. This work exhibited an IIP3 of +2.6dBm, and benefited from the RF filtering that comes with the use of passive mixers before any active circuit. However, this was designed for 5GHz WLAN applications and had a power consumption as high as 11.6mW. More recently, [38] demonstrated a 0.6mW (at 1GHz) mixer-first receiver front-end, with as high as +25dBm OOB IIP3. The high IIP3 was a result of the mixer-first architecture used. However, the gain of this front-end is limited by the gain of the off-chip input matching network and 6dB passive gain from the capacitive read-out. Additionally, the power of this front-end is expected to scale proportional to f_{LO}, to more than a milliwatt at the desired 2.4GHz ISM band.

In [26], we proposed an architecture for a direct-conversion receiver at 2.4GHz which achieves moderate NF, gain, in-band linearity and most importantly improved out-of-band linearity due to RF filtering, while keeping the power consumption of the entire front-end under a milliwatt. Compared to [26], this chapter delves into greater depth on analyzing the translational-feedback-based architecture and design trade-offs with respect to noise, linearity and RF filtering. With the aim of building a complete receiver front-end, it also includes the design and measurement results of a baseband amplifier with programmable gain and bandwidth.

This chapter is organized as follows. Section 2.2 describes the front-end architecture. It starts off with a commonly used low-power LNA, and builds up to our proposed architecture. Section 2.3 presents the results of the LTI equivalent circuit for the receiver, and describes the design of the N-path filters in the circuit to achieve the desired transfer function. Section 2.4 provides a detailed analysis of the noise from various sources and compares it against more traditional architectures. It also provides an analysis of both in-band and out-of-band non-linearity, from a design perspective. Section 2.5 provides design details of the transformer, LNA and the baseband filter. Section 2.6 provides measurement results of the front-end and the baseband filter. Section 2.7 compares this work against the state-of-the-art and provides some key takeaways of the work.

2.2 Receiver Architecture

To keep the power consumption of the receiver under a milliwatt, it is desirable to have a front-end matching network with gain. Additional to providing gain, the matching network transforms the antenna resistance from 50Ω to a higher value, relaxing the power budget on the subsequent blocks. Similar to [31, 35, 37] and many other works in literature, a transformer-based matching network is used in the front-end. Differential outputs, passive gain and ESD protection are some of the advantages of using transformer-based matching networks. To meet the sub-mW targets, is also desirable to use techniques to lower the power consumption of the LNA. To this end, g_m boosting in a common-gate LNA is a commonly

used technique. A simple power-efficient method of doing this is to use passive inverting amplification by using capacitively cross-coupling in a differential CGLNA (see Fig. 2.16 for schematic), as demonstrated in [39]. A passive mixer at the output of the LNA completes the receiver front-end.

While the transformer-based input matching is not broadband, the bandwidth (100s of MHz) is still much higher than the channel bandwidth ($1-10$ MHz) required for the modest data rates in IoT applications. Consequently, such a receiver front-end has little or no frequency selectivity. In order to be instantaneously narrowband and frequency selective at the RF input, but still support operation over the entire range of bandwidth of the input matching network, an N-path filter may be added in shunt with the CC-CGLNA at the input, as shown in Fig. 2.1(a). The N-path filter, first seen in [11, 12] and re-discovered in [13, 14], has an important property of impedance translation from baseband to RF. Consequently, it can be used to realize high-Q tunable RF band-pass filters (with center frequency equal to ω_{LO}, the frequency at which the mixer is switched).

The receiver front-end shown in Fig. 2.1(a) is a linear periodic time varying (LPTV) system, with a linear time invariant (LTI) half-circuit equivalent representation at frequencies around ω_{LO} (See Fig. 2.1(b)). Note that this LTI equivalent representation also includes the common gate LNA. As seen in [19], harmonic re-upconversion losses in the N-path filter are represented in the LTI equivalent circuit with a shunt resistance R_{sh}. The re-radiation resistance R_{sh} is a function of the impedance seen by the shunt N-path filter Z_{TH} (see Fig. 2.1). Z_{TH} may be modeled as a shunt LCR network with $Q_{match} = R_{TH}/(\omega_0 L_{sec})$, where the equivalent resistance R_{TH} is given by

$$R_{TH} = \frac{n^2 R_S}{1 + \frac{n^2 g_{m,eff} R_S}{2}} \tag{2.1}$$

where R_S is the source impedance of the antenna, n is the electrical turns ratio of the transformer, L_{sec} is the secondary inductance of the transformer and $g_{m,eff}$ is the effective transconductance of the capacitively cross-coupled CG LNA, and is given by $g_{m,eff} = 2g_{m,LNA}$. Note that in traditional N-path filters such as the one in [19, 37], R_{TH} is given by $n^2 R_S$. That is, the impedance seen by the N-path filter is exactly equal to the transformed source impedance. However, in the circuit in Fig. 2.1, an additional dependence on $g_{m,eff}$ is seen due to the use of a common-gate LNA, as seen in equation (2.1). For the extremal cases of infinitely broadband ($Q_{match} = 0$) and infinitesimally narrowband ($Q_{match} = \infty$), R_{sh} for the circuit in Fig. 2.1 [19] is given by,

$$R_{sh} = \begin{cases} \frac{8}{\pi^2 - 8} \left(\frac{\frac{n^2 R_S}{2}}{1 + \frac{n^2 g_{m,eff} R_S}{2}} + R_{SW2} \right) & \text{Broadband} \\ \frac{8}{\pi^2 - 8} R_{SW2} & \text{Narrowband} \end{cases} \tag{2.2}$$

where R_{SW2} is the ON resistance of the mixer switches in the shunt N-path filter.

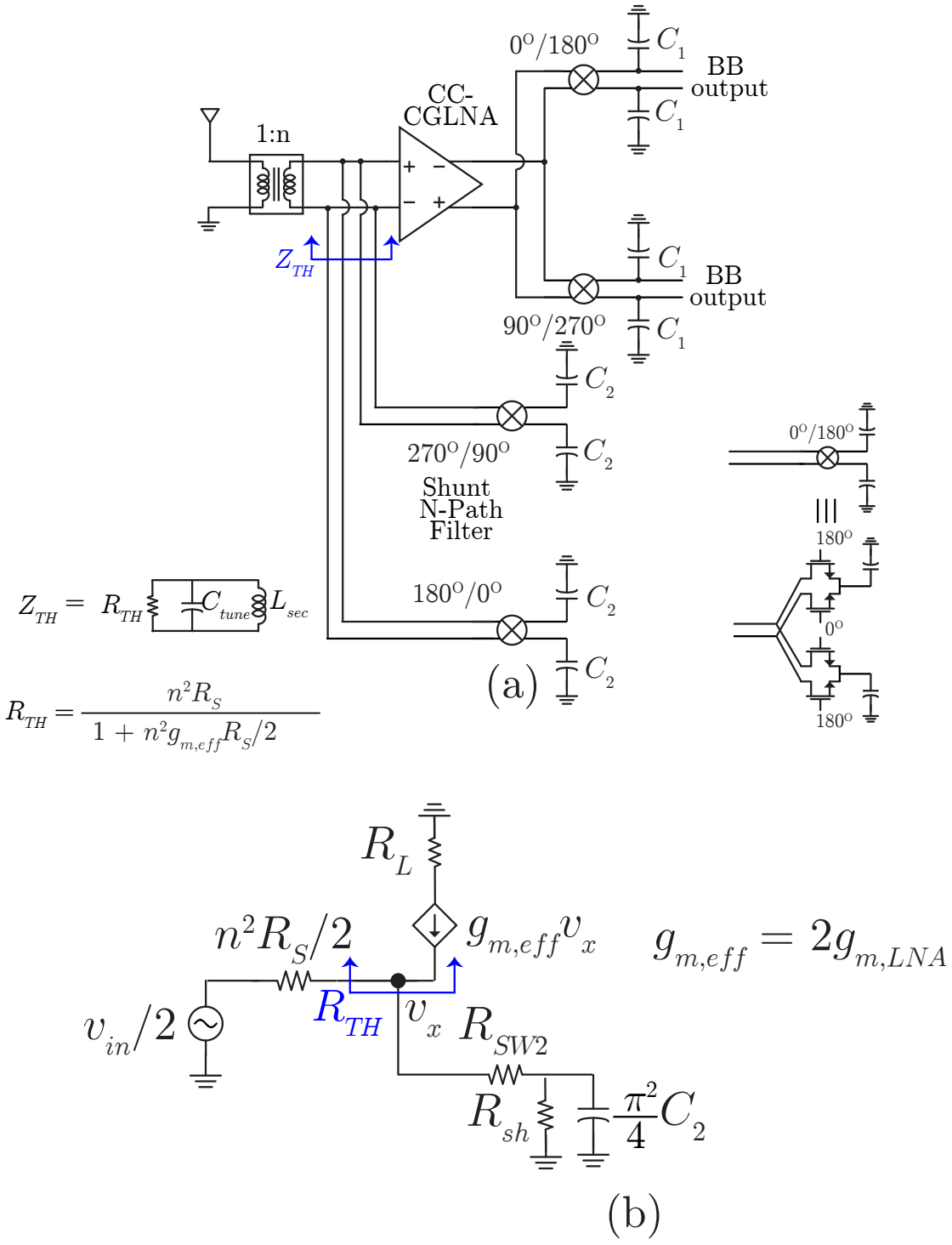


Figure 2.1: (a) Simplified schematic of CC-CGLNA based receiver front-end with shunt N-path filter, in conjunction with transformer-based input matching network. (b) LTI equivalent half circuit to illustrate the matching at the LNA input.

For input match at ω_{LO} with the circuit in Fig. 2.1, the condition for matching can be derived as

$$\frac{\frac{n^2 R_S}{2}}{R_{SW2} + R_{sh}} = 1 - n^2 g_{m,eff} \frac{R_S}{2} \tag{2.3}$$

Clearly, it is impossible to match for $n^2 g_{m,eff} R_S/2 > 1$. This is the well-known g_m versus matching trade-off in a common gate LNA [39]. In a conventional common-gate LNA, the value of g_m required for matching is $1/R_S$ and this yields a noise factor of $1 + \gamma/\alpha$[1]. When effects of re-radiation losses in the shunt N-path filter are considered, the input impedance of the circuit drops. Therefore, an even lower value of g_m is needed to match, exacerbating the noise versus matching trade-off of the LNA.

This is illustrated with a representative example by considering the case of matching with a $1:4$ transformer matching network, transforming the 50Ω to 800Ω. To match with a broadband LNA, an effective $g_{m,eff}$ equal to $2/(n^2 R_S) = 2.5$mS is required. When an N-path filter with switch ON resistance $R_{SW2} = 80\Omega$ is placed in shunt at the input of the LNA, the input impedance reduces to 600Ω at ω_{LO}, for an ideal broad-band transformer matching network. Z_{in} reduces further to 400Ω for $Q_{match} = 2.5$.

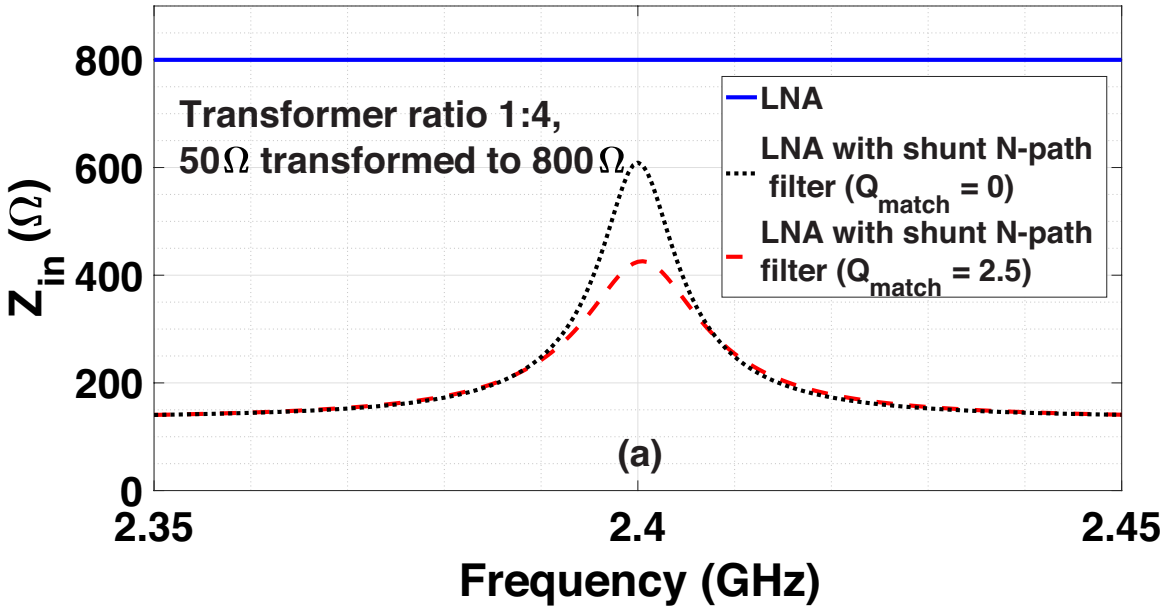


Figure 2.2: Plot of input impedance v/s frequency for matching with broad-band LNA in shunt with N-path filter for different Q_{match}, for a fixed $R_{SW2} = 80\Omega$.

[1] γ/α is the noise coefficient of the transistor. The noise factor is lower for a matched capacitively cross coupled CG-LNA, and is equal to $1 + \gamma/2\alpha$.

In order to break the trade-off between noise and matching of the capacitively cross-coupled common gate LNA with a shunt N-path filter, Z_{in} at ω_{LO} must be boosted, while keeping Z_{in} outside the band constant. One obvious solution to boost the in-band impedance at the RF input is to have a negative resistance as the load to the shunt N-path filter, as shown in Fig. 2.3(a). Clearly, such a solution consumes power, as active g_m circuits are required to synthesize the negative resistance. However, by exploiting translational positive feedback from baseband to RF, power consumption of the active g_m may be lowered by an amount equal to the gain of the LNA, leading to the proposed circuit shown in Fig. 2.3(b).

To summarize, the proposed circuit of Fig. 2.3(b) leverages N-path filter-based translational positive feedback to achieve highly selective narrow-band matching, and breaks the noise figure versus input matching trade-off imposed by the g_m of the common gate LNA, while adding a small overhead to the receiver power consumption. As described in the subsequent sections, there is negligible degradation in noise figure and linearity due to the transconductance used in the positive feedback.

In addition to breaking the noise figure versus input matching trade-off imposed by the the common gate LNA, the proposed architecture of Fig. 2.3(b) also helps break a trade-off between input matching and out-of-band attenuation through the mixer switch resistance R_{SW2}, when the transformer matching network is narrowband. As illustrated by the plot in Fig. 2.4, using smaller values of R_{SW2} results in improved out-of-band attenuation but lower in-band impedance. The lower in-band impedance results from the smaller shunt re-radiation resistance R_{sh}, which is proportional to R_{SW2} when the transformer matching network is narrowband (see equation (2.2)). Impedance boosting due to the positive feedback in our proposed architecture in Fig. 2.3 also breaks this trade-off.

In the subsequent sections, we derive the performance and design trade-offs of the proposed circuit of Fig. 2.3 quantitatively.

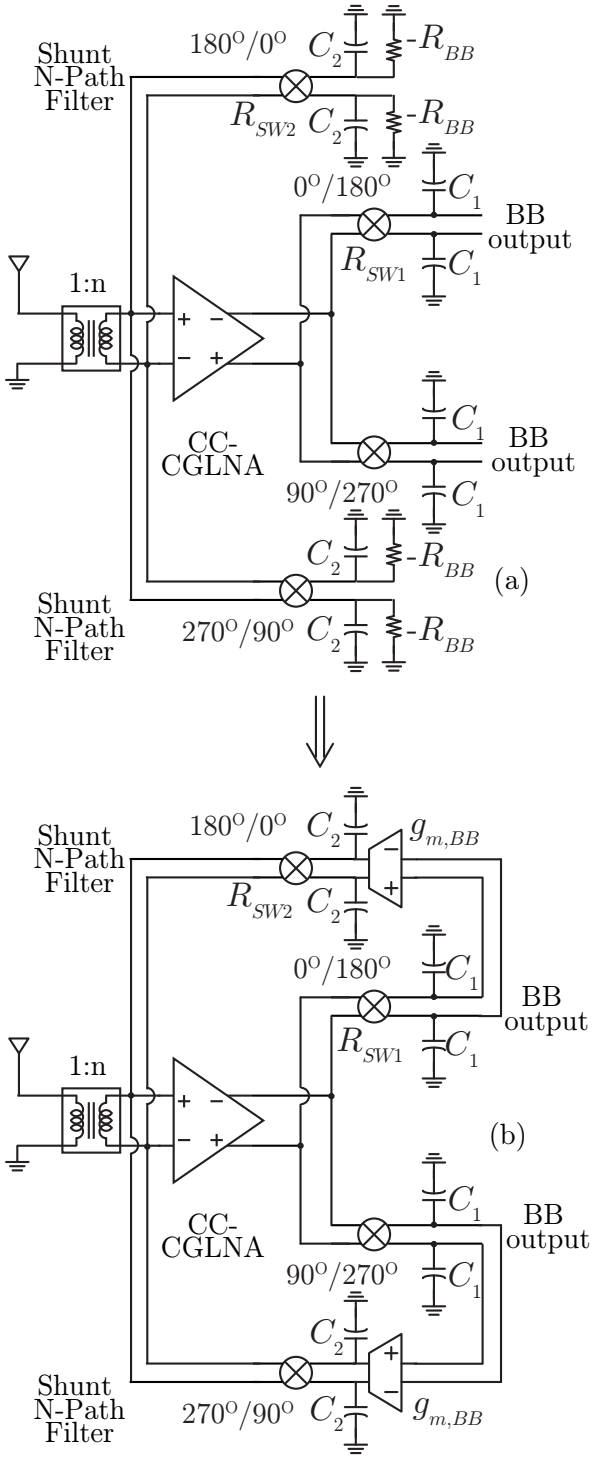


Figure 2.3: Receiver front-end with translational positive feedback from baseband to RF to boost input impedance.

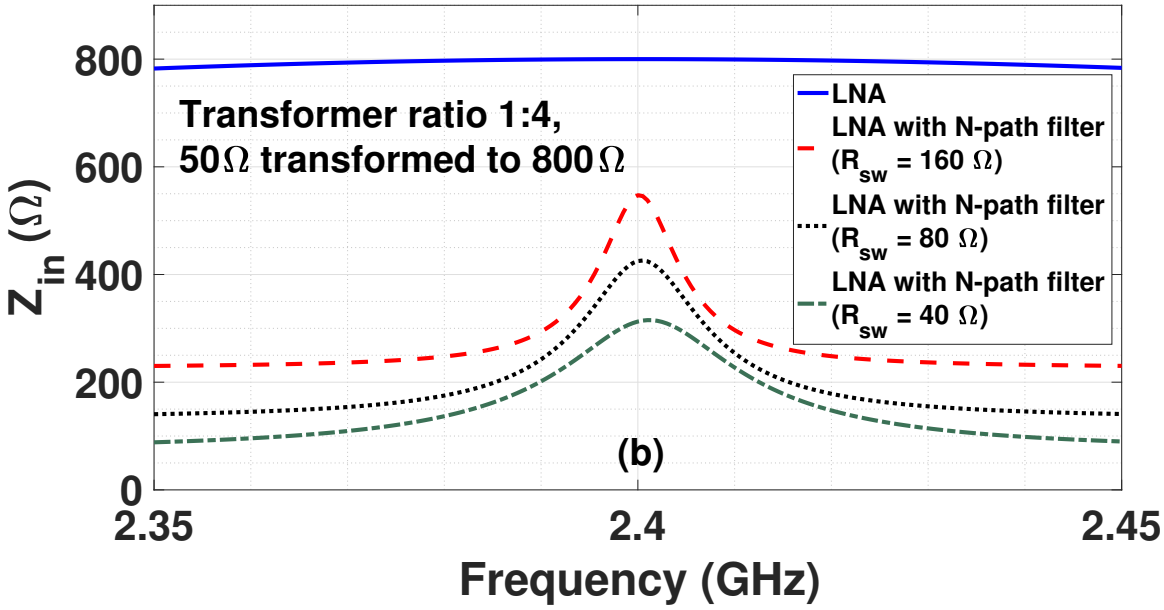
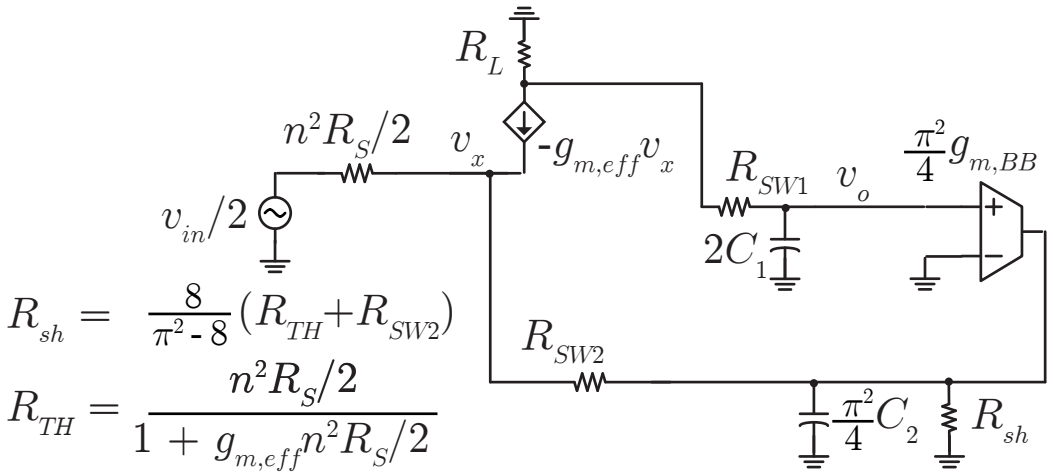


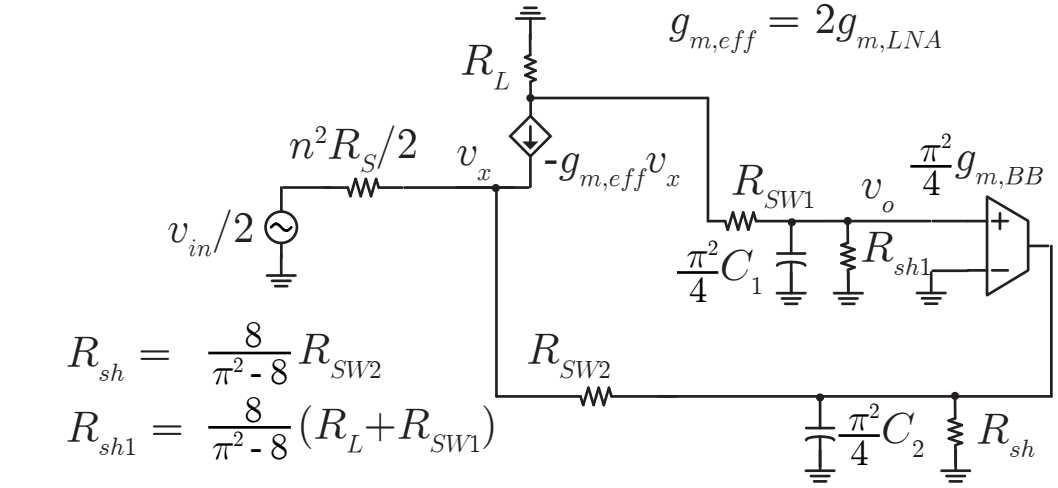
Figure 2.4: Plot of input impedance v/s frequency for matching with broad-band LNA in shunt with N-path filter for different R_{SW2}, for a fixed $Q_{match} = 2.5$.

2.3 Feedback and Filtering

A rudimentary analysis of translational feedback based receivers may be found in [40], and a slightly more detailed analysis is presented in [41], with a large focus on the baseband low-pass filter implemented in that work. In [42], we analyzed another translational feedback based receiver, which used negative feedback to reduce input impedance. However, there has been no detailed treatment of the design of two separate N-path filters in translational feedback systems to achieve the desired RF and baseband transfer functions. The comprehensive analysis in this chapter attempts to do that for the case of the translational feedback receiver implemented in our work, but the analysis may be extended to any other architecture with translational feedback. The analysis, which uses the fact that switched RC-kernels of both N-path filters are operated in their "mixing region" of operation [15], is derived in detail in appendix A. A derivation is provided for the two extremal cases, one where the input resistance R_S is infinitely broadband, the other where it is infinitesimally narrow-band. The input matching network in our architecture is in between the two extremal cases. Therefore, we analyze both to gain some design insights.



(a) Infinitely broadband input match



(b) Infinitesimally narrowband input match

Figure 2.5: LTI equivalent half-circuit of the receiver at ω_{LO} for (a) Broadband approximation for input matching network (b) Narrowband approximation for input matching network.

Fig. 2.5 shows the equivalent LTI equivalent half-circuit of the LPTV receiver around ω_{LO}, as derived in Appendix A. To simplify notation while accounting for the frequency translation by ω_{LO}, we denote $s - j\omega_{LO}$ by s', a frequency translated variable. It can be shown that for the LTI equivalent shown in Fig. 2.5(a), the transfer functions from $v_{in}/2$ to

v_x and v_o are given by equation (2.4).

$$
\begin{aligned}
\frac{v_x}{\frac{v_{in}}{2}}(s) &= \frac{1}{1+n^2 g_{m,eff}\frac{R_S}{2}} \frac{1}{1+\frac{R_{TH}}{R_{SW2}+R_{sh}}\left(1-\frac{\pi^2}{4}A_{LNA}g_{m,BB}R_{sh}\right)} \frac{\mathrm{Num}(s')}{\mathrm{Den}(s')} \\
\frac{v_o}{\frac{v_{in}}{2}}(s) &= \frac{\pi}{2\sqrt{2}} \frac{A_{LNA}}{1+n^2 g_{m,eff}\frac{R_S}{2}} \frac{1}{1+\frac{R_{TH}}{R_{SW2}+R_{sh}}\left(1-\frac{\pi^2}{4}A_{LNA}g_{m,BB}R_{sh}\right)} \frac{\mathrm{Num}_1(s')}{\mathrm{Den}(s')} \\
\mathrm{Num}(s') &= (1+2s'C_1(R_L+R_{SW1}))\left(1+s'\frac{\pi^2}{4}C_2(R_{sh}||R_{SW2})\right) \\
\mathrm{Num}_1(s') &= 1+s'\frac{\pi^2}{4}C_2(R_{sh}||R_{SW2}) \\
\mathrm{Den}(s') &= 1+s'\frac{2C_1(R_L+R_{SW1})(R_{SW2}+R_{sh}+R_{TH})+\frac{\pi^2}{4}C_2R_{sh}(R_{TH}+R_{SW2})}{R_{SW2}+R_{sh}+R_{TH}(1-\frac{\pi^2}{4}A_{LNA}g_{m,BB}R_{sh})} \\
&\quad + s'^2\frac{\frac{\pi^2}{2}C_1C_2(R_L+R_{SW1})(R_{TH}+R_{SW2})R_{sh}}{R_{SW2}+R_{sh}+R_{TH}(1-\frac{\pi^2}{4}A_{LNA}g_{m,BB}R_{sh})} \\
\text{where,}\quad R_{TH} &= \frac{\frac{n^2R_S}{2}}{1+\frac{n^2g_{m,eff}R_S}{2}} \qquad A_{LNA} = g_{m,eff}R_L
\end{aligned}
\tag{2.4}
$$

From the expressions for $\mathrm{Num}(s')$ and $\mathrm{Den}(s')$ in equation (2.4), we see that the LTI equivalent transfer function has 2 poles and 2 zeros. It is important to understand the sizing of the capacitors C_1 and C_2 to ensure that we get the desired RF filtering.

It is known that the far-out attenuation of this N-path filter based architecture is determined by the switch resistance of the feedback mixer R_{SW2} [36]. The corresponding zero in the transfer function is given by $-1/(\frac{\pi^2}{4}C_2(R_{sh}||R_{SW2}))$, as observed in equation (2.4).

There are two N-path filters in our system, one in the feedforward path after the LNA, one in the feedback path, each with different RC time-constants for the baseband load. To gain some insight into the choice of the time constants, consider the circuit in Fig. 2.5(a), with $n^2R_S = 800\Omega$, $R_{SW2} = 40\Omega$, $g_{m,eff} = 5\text{mS}$, $R_L = 2.5\text{k}\Omega$, and $R_{SW1} = 200\Omega$. Consider the following 2 cases, (I) $C_1 = 2\text{pF}, C_2 = 85\text{pF}$. In this case, the time constant τ_2 associated with the feedback N-path filter is much higher than that associated with the feedforward N-path filter τ_1. (II) $C_1 = 6.5\text{pF}, C_2 = 2\text{pF}$. In this scenario, $\tau_1 \gg \tau_2$. The values were chosen such that the 3-dB bandwidth (2.5MHz in this example) at the output node v_o is the same in both cases. However, as we can clearly see from the transfer function to the node v_x, the input of the LNA, (see Fig. 2.6), case I is a much better RF filter for nearby blockers than case II, and is therefore desirable. For blockers which are very far out (at a higher frequency than both the poles and zeros), the out-of-band attenuation ρ is determined by

$R_{SW2}||1/g_{m,eff}$, and is given by equation (2.5).[2]

$$\begin{aligned}\rho &= 2\frac{R_{SW2}||1/g_{m,eff}}{R_{SW2}||1/g_{m,eff}+\frac{n^2R_s}{2}} \\ &\approx \frac{2R_{SW2}}{R_{SW2}+\frac{n^2R_s}{2}} \qquad \left(\frac{1}{g_{m,eff}} \gg R_{SW2}\right)\end{aligned} \tag{2.5}$$

All the expressions in this section are for the case of a broadband input matching network. The expressions and analysis regarding the position of poles and zeros are qualitatively similar for the case of a narrow-band input matching network, and may be derived by solving the circuit in Fig. 2.5(b).

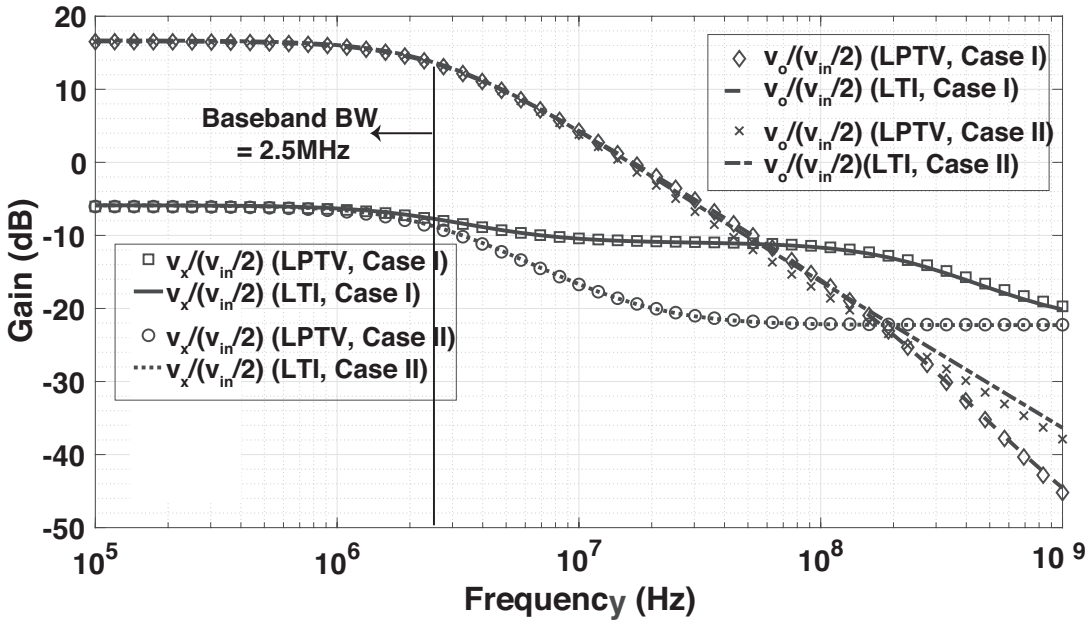


Figure 2.6: Transfer functions to node v_x and output node v_o (see the half-circuit equivalent of Fig. 2.5) for different choice of capacitors C_1, C_2, the capacitors in the feed-forward and the feedback N-path filters, respectively. Transfer functions from a PAC analysis of the LPTV circuit, as well as frequency translated transfer functions based on the equation (2.4) are provided. Excellent agreement is seen between the LPTV simulation and the results from the LTI model.

[2]The attenuation is with respect to the peak of 1/2 in the center of the band, and hence the factor of 2 in equation (2.5). The peak of 1/2 comes from the input match condition.

2.4 Noise Figure and Linearity

2.4.1 Noise

The noise figure can be derived from the LTI equivalent circuit in Fig. 2.5 [19] and is given by equation (2.6). The terms in equation (2.6) denote the contribution due to the transistors of the CC-CGLNA, the re-radiation losses, the baseband feedback transconductance and the mixer switches on the feedback path, R_{SW2}, respectively. We briefly take a look at each of these terms. The noise contributions from the feedforward switch resistance R_{SW1} and the load resistance R_L are insignificant, and hence not shown in equation (2.6).

$$\begin{aligned} \mathrm{F} &= 1 + \frac{\gamma}{2\alpha n^2 g_{m,LNA} R_S}\beta + \frac{\frac{n^2 R_S}{2} R_{sh}}{(R_{sh}+R_{SW2})^2}\left(1 + \frac{\pi^2}{4} g_{m,BB} R_{sh} \frac{\gamma}{\alpha}\right) + \frac{\frac{n^2 R_S}{2} R_{SW2}}{(R_{sh}+R_{SW2})^2} \\ \beta &= \begin{cases} \frac{\pi^2}{8}\left(1 + \frac{\frac{n^2 R_S}{2}}{R_{SW2}+R_{sh}}\right)^2 & \text{Broadband} \\ \left(1 + \frac{\frac{n^2 R_S}{2}}{R_{SW2}+R_{sh}}\right)^2 + \left(\frac{\pi^2}{8} - 1\right)\left(1 + \frac{\frac{n^2 R_S}{2}}{R_{SW2}+R_{sh}} + g_{m,LNA} R_S\right)^2 & \text{Narrowband} \end{cases} \end{aligned} \tag{2.6}$$

The contribution of the transistors of the CC-CGLNA to the noise factor is shown in Fig. 2.7 for three different cases: without a shunt N-path filter, with a shunt N-path filter having broadband input match, and with a shunt N-path filter having narrowband match. Fig. 2.7 plots the noise factor as a function of $g_{m,LNA}R_S$, where R_S is the fixed source resistance, for the three different cases.[3] The simulations (SpectreRF pnoise) show excellent agreement with the analysis developed in this section.

The contribution to the noise figure due to the transistors of a CC-CGLNA, without a shunt N-path filter, is given by $\gamma/(2\alpha n^2 g_{m,LNA} R_S)$. While our architecture enables us to break the matching-NF trade-off of a CC-CGLNA, the transistor noise is worse compared to a standalone CC-CGLNA due to the harmonic noise folding associated with the N-path filter in shunt with the LNA. This degradation is given by the factor β in equation (2.6). A detailed discussion of this phenomenon is provided in Appendix B. The analysis, supported by the simulation results in Fig. 2.7, highlight the importance of making the input matching network as wideband as possible, in order to minimize the harmonic noise folding of the common-gate LNA.

[3]It must be re-iterated that in the case of a stand-alone CC-CGLNA, input match is possible for only a single value of $g_{m,LNA}$, i.e., $n^2 g_{m,LNA} R_S = 1$. However, with the translational feedback architecture proposed here, input match is possible for any value of $g_{m,LNA}$.

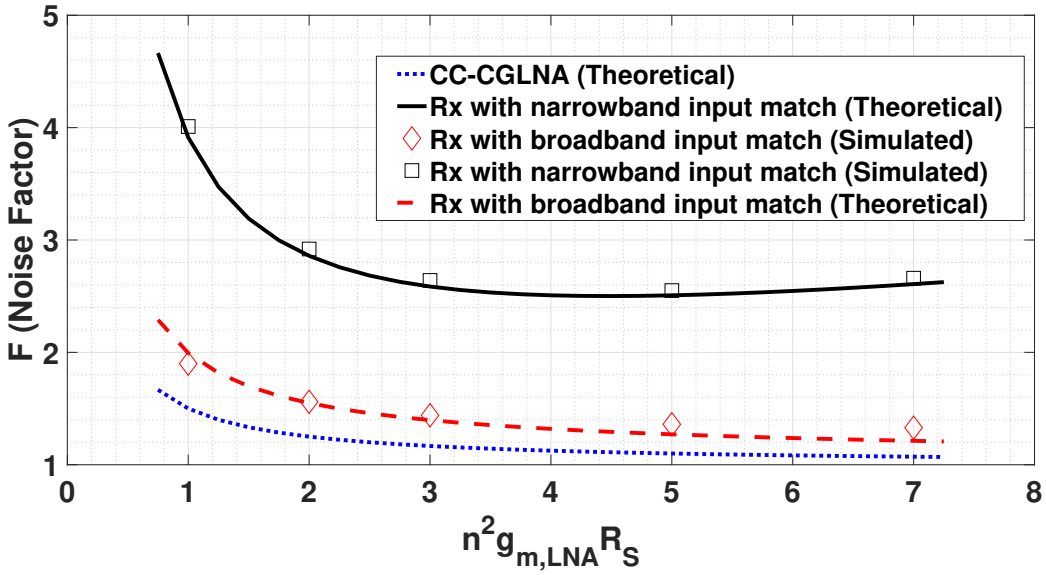


Figure 2.7: Noise factor due to the transistor in the common-gate LNA (other noise sources are not considered). The degradation due to the shunt N-path filter is observed.

Now, we compare this architecture to the one proposed in [37], which is a mixer-first receiver with a transformer input matching network (see Fig. 2.8), purely from a noise perspective. The noise figure due to the noise of the baseband amplifier alone is given by

$$\begin{aligned} \mathrm{F} &= 1 + \frac{\gamma}{\alpha}\frac{8}{\pi^2 n^2 g_{m,LNA-BB} R_S}\left(1 + \frac{\frac{n^2 R_S}{2} + R_{sw}}{R_{sh}}\right)^2 \\ R_{sh} &= \begin{cases} \frac{8}{\pi^2-8}\left(\frac{n^2 R_S}{2} + R_{sw}\right) & \text{Broadband} \\ \frac{8}{\pi^2-8} R_{sw} & \text{Narrowband} \end{cases} \end{aligned} \tag{2.7}$$

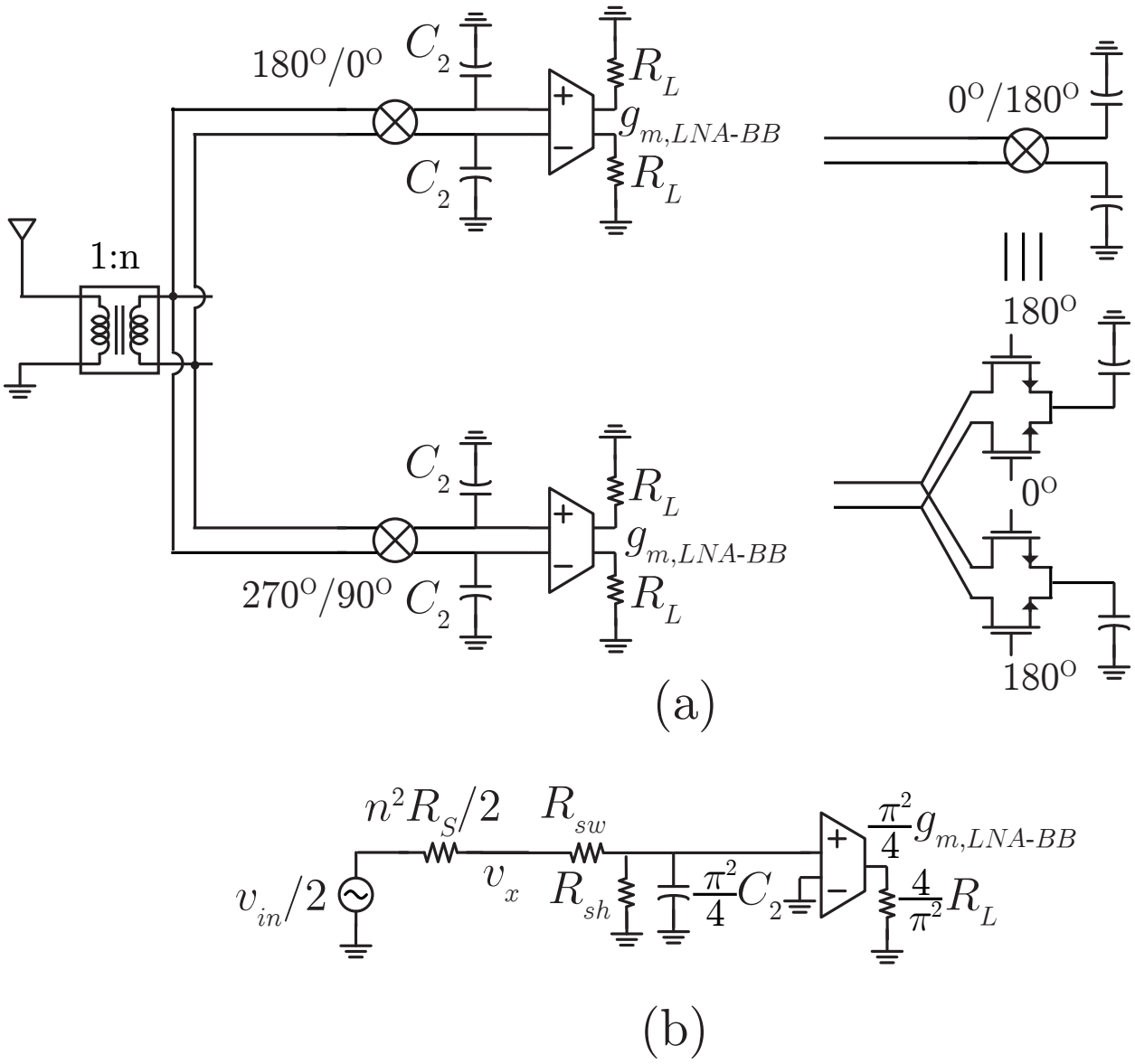


Figure 2.8: A mixer-first receiver front-end with a transformer input matching network, and a baseband low-noise amplifier.

For the architecture in Fig. 2.8, we obviously cannot exploit the benefit of lower noise figure at lower power, like in a CC-CGLNA. However, there is no noise folding of the transistor current noise. Fig. 2.9 compares the noise figure (due to amplifier transistors alone) for our proposed architecture (see Fig. 2.3) and the mixer-first architecture of [37] (see Fig. 2.8). For a fair comparison, it is ensured that the overall amplifier power consumption is the same in both cases ($g_{m,LNA}$ of Fig. 2.3 is twice $g_{m,LNA-BB}$ of Fig. 2.8). It is seen that for

lower power consumption (smaller $g_{m,LNA}$), the noise factor of our proposed architecture is significantly better due to the benefit derived from capacitive cross-coupling in the RF LNA. However, for higher values of $g_{m,LNA}$ the noise folding in the RF LNA starts dominating. Since there is no transistor noise folding in the architecture of Fig. 2.8, for higher values of g_m, it turns out to be better from a noise perspective.

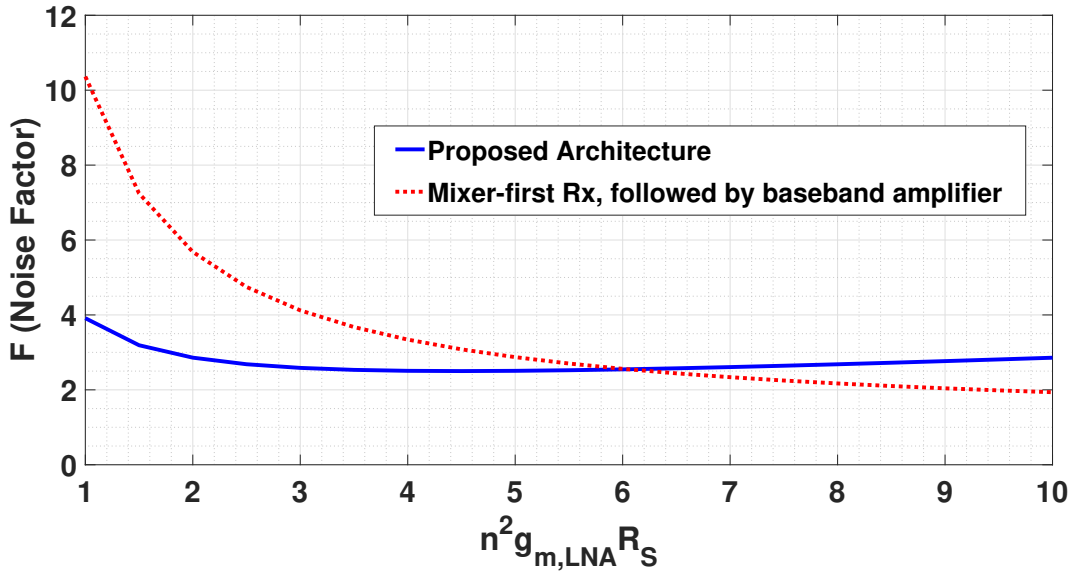


Figure 2.9: Noise factor due to the transistor in the amplifier alone (other noise sources are not considered). Our proposed receiver architecture (see Fig. 2.3) is compared against the mixer-first architecture of Fig. 2.8. The comparison is done such that the overall amplifier power consumption is the same in both cases. In both cases, the input matching network is assumed to be narrowband, with $R_{SW2}/(n^2 R_S) = 0.1$.

The noise contributions from the feedback switch resistance R_{SW2} and the re-radiation losses R_{sh} are similar to those in [19]. That is, for a broadband input match, noise figure is a monotonically decreasing function of R_{SW2}. However, for narrowband input match, there exists an optimal value of R_{SW2} for minimal noise figure. Also, reducing R_{SW2} for narrowband input match increases the β factor in equation (2.6). That is, it increases the noise figure contribution from the transistors themselves due to higher harmonic noise folding.

Now, we consider the only remaining noise contributor, the baseband feedback $g_{m,BB}$. For values of $g_{m,BB}$ required for input-matching, $\pi^2 g_{m,BB} R_{sh}/4$ is much less than unity (see equation (2.6)). Therefore, the contribution of the feedback transconductance to noise figure is insignificant. If a negative baseband resistance was used for input matching instead of exploiting positive feedback (see Figs. 2.3(a) and (b)), the value of baseband negative

transcoductance required would approximately be $A_{LNA}g_{m,BB}$, thereby increasing the noise contribution of the feedback transconductance by approximately a factor of A_{LNA}. This highlights yet another benefit of our proposed architecture.

2.4.2 Non-Linearity

The main source of in-band non-linearity is the CC-CGLNA at the RF front end. The in-band non-linearity may be analyzed under the weak non-linearity assumption, using the method of distortion-current injection. For convenience, we assume that the transistor has only a third order non-linearity. [4] Consider an input with two tones at frequencies f_1 and f_2, both in-band such that $2f_1 - f_2$ is also in band. To compute in-band IIP3, first we solve the half-circuit in Figs. 2.5(a) and (b) at the fundamental. Under the condition for matching v_x is equal to $v_{in}/4$. Now, to compute the IIP3, we inject a third order device non-linearity[5] equal to $g_3(v_{in}/2)^3$ at a frequency $2f_1 - f_2$, as shown in Fig. 2.10(a) and (b). The IIP3 (differential input voltage) hence computed turns out to be

$$\begin{aligned} V_{IIP3-IB} &= \sqrt{\left|\frac{4g_m}{3g_3}\right|}\sqrt{\frac{2}{1+\frac{\frac{n^2R_S}{2}}{R_{SW2}+R_{sh}}}} \\ &\approx \begin{cases} \frac{4}{\pi}\sqrt{\left|\frac{4g_m}{3g_3}\right|} & \text{Broadband} \\ \frac{2\pi}{\sqrt{\pi^2-8}}\sqrt{\left|\frac{4g_m}{3g_3}\right|}\sqrt{\frac{\rho}{1+\frac{2\pi^2\rho}{\pi^2-8}}} & \text{Narrowband} \end{cases} \end{aligned} \tag{2.8}$$

where R_{sh} is the shunt re-radiation resistance, given by equation (2.2). The translational positive feedback has negligible detrimental effect on the linearity, as it is used only for matching. Regardless of the extent of positive feedback, the LNA's differential input swing is $v_{in}/2$, which is set by the constraint for input match. However, it is seen that the in-band IIP3 depends on the value of the mixer switch resistance R_{SW2} in the feedback N-path filter. The dependence on R_{SW2} is very weak for a broadband source impedance R_S, and the IIP3 is approximately just a function of the V_{GS} bias voltage (see equation (2.8)). However, for a narrowband source impedance R_S, the in-band IIP3 depends on the mixer switch resistance R_{SW2}. Equation (2.8) expresses this dependence terms of the far-out attenuation ρ (see equation (2.5)). For small values of ρ, the in-band IIP3 worsens with out-of-band attenuation, and is proportional to $\sqrt{\rho}$.

To compute the out-of-band IIP3, the 2 tones are placed at frequencies f_1 and f_2 outside the band, such that the IM3 product falls at $2f_1 - f_2$, which is in the band of interest.

[4] For the value of gain A_{LNA} and the bias (with low transconductance efficiency) chosen for the feedback transconductance, its non-linearity is negligible compared to the front-end LNA.

[5] The node v_x is $v_{in}/4$. The distortion injected is $g_3(2 \times v_{in}/4)^3$. The factor of $2\times$ comes from the effective doubling due to capacitive cross-coupling in the CGLNA.

The input-referred IM3 is computed by dividing the IM3 by the in-band gain of the receiver at frequency $2f_1 - f_2$. At far-out frequencies, where the input resistance looking into the receiver is approximately equal to R_{SW2} and the attenuation ρ is given by equation (2.5), the IM3 product is attenuated by a factor of ρ^3. The out-of-band IIP3 is therefore given by

$$\begin{aligned} V_{IIP3-OOB} &= V_{IIP3-IB}\rho^{-\frac{3}{2}} \\ &\approx \begin{cases} \frac{4}{\pi}\sqrt{\left|\frac{4g_m}{3g_3}\right|}\rho^{-\frac{3}{2}} & \text{Broadband} \\ \frac{2\pi}{\sqrt{\pi^2-8}}\sqrt{\left|\frac{4g_m}{3g_3}\right|}\frac{\rho^{-1}}{\sqrt{1+\frac{2\pi^2\rho}{\pi^2-8}}} & \text{Narrowband} \end{cases} \end{aligned} \tag{2.9}$$

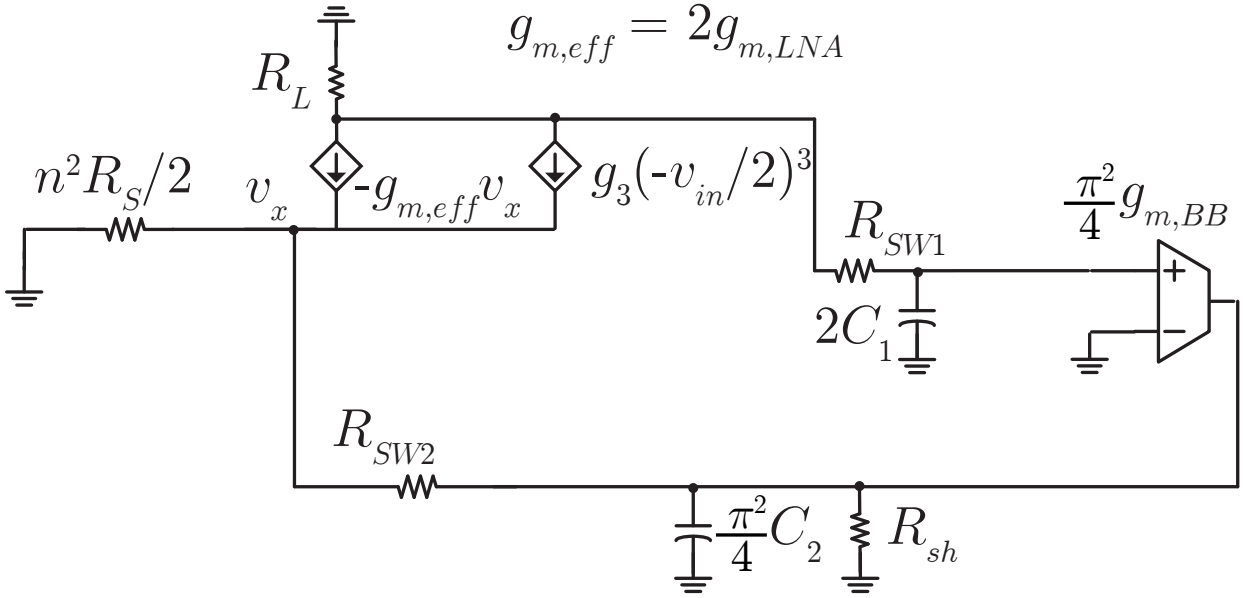
Out-of-band IIP3 increases with out-of-band attenuation, and is proportional to $\rho^{-\frac{3}{2}}$, if the source impedance R_S is broadband. However, for a narrowband source impedance, the out-of-band IIP3 is approximately proportional to ρ^{-1} due to the degradation of in-band IIP3 with increasing attenuation. To verify this analysis, the LNA was modeled using polynomial voltage controlled current sources with $g_{m,LNA} = 2\text{mS}$ and $g_3 = -25\text{mA/V}^3$. These values were chosen based on linearity simulations of the actual transistors used in the circuit. The feedback transconductance $g_{m,BB}$ and the switches were assumed to be ideal for this simulation. The simulation plots in Fig. 2.11 confirm our analysis.

This analysis assumes that the mixer non-linearity is not dominant even for out-of-band signals. This approximation is reasonably valid for our circuit, as verified by simulation of actual transistor schematics. For high linearity mixer-first front-ends like the one in [30], neglecting the mixer-switch non-linearity is not a valid assumption. Fig. 2.12 shows the simulated IIP3 as a function of tone offset frequency for a complete transistor level schematic for all the amplifiers and switches used in the circuit. The simulation was performed at $f_{LO} = 2.4\text{GHz}$ and using a switch resistance of 53Ω, equivalently a ρ of around 10.6dB. To validate our assumption of neglecting the non-linearity of the feedback transconductance $g_{m,BB}$, two simulations were performed. One with actual transistors in the feedback g_m and the other where the feedback g_m consists of ideal voltage controlled current sources. As seen from the simulation plots in Fig. 2.12, there is negligible difference in the simulated IIP3 in the two cases, validating our assumption of neglecting the non-linearity of the feedback transconductance in the non-linearity analysis.

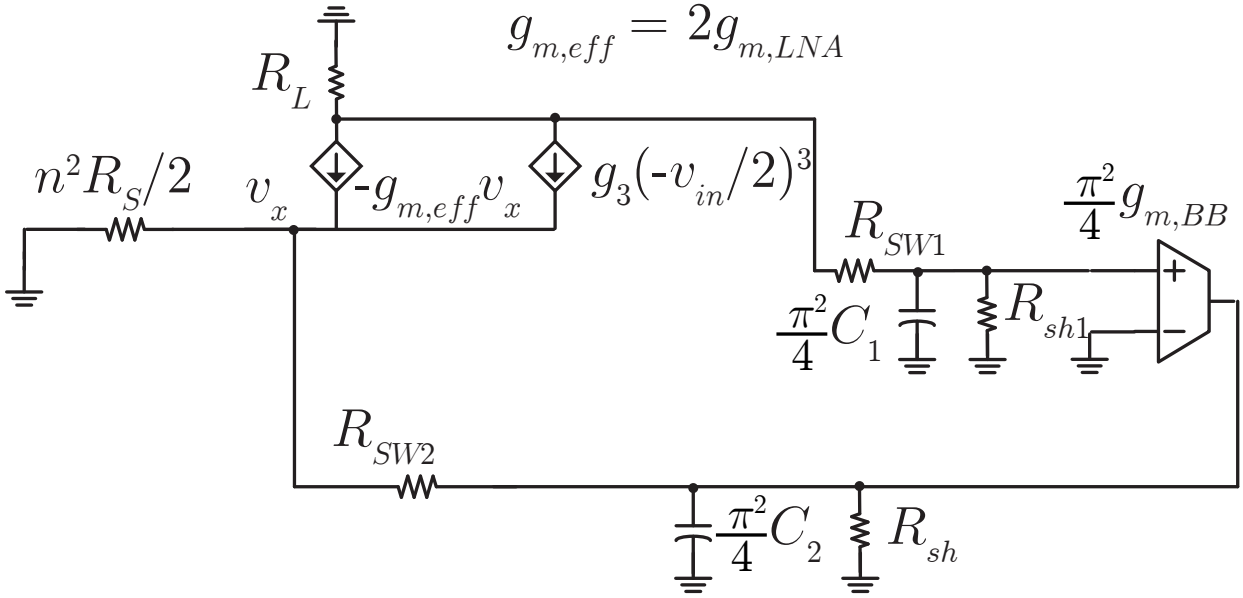
2.5 Circuit Design

2.5.1 Transformer Design

As seen in the previous sections on matching, linearity and noise figure, the co-design of the transformer (Figs. 2.13, 2.14) plays an extremely critical role in achieving the best performance at the lowest possible power. The following are some key points in this regard. 1) For low-power active circuits and switches, it is desirable to transform the 50Ω antenna



(a) Broadband R_S



(b) Narrowband R_S

Figure 2.10: Equivalent circuit to compute third order non-linearity.

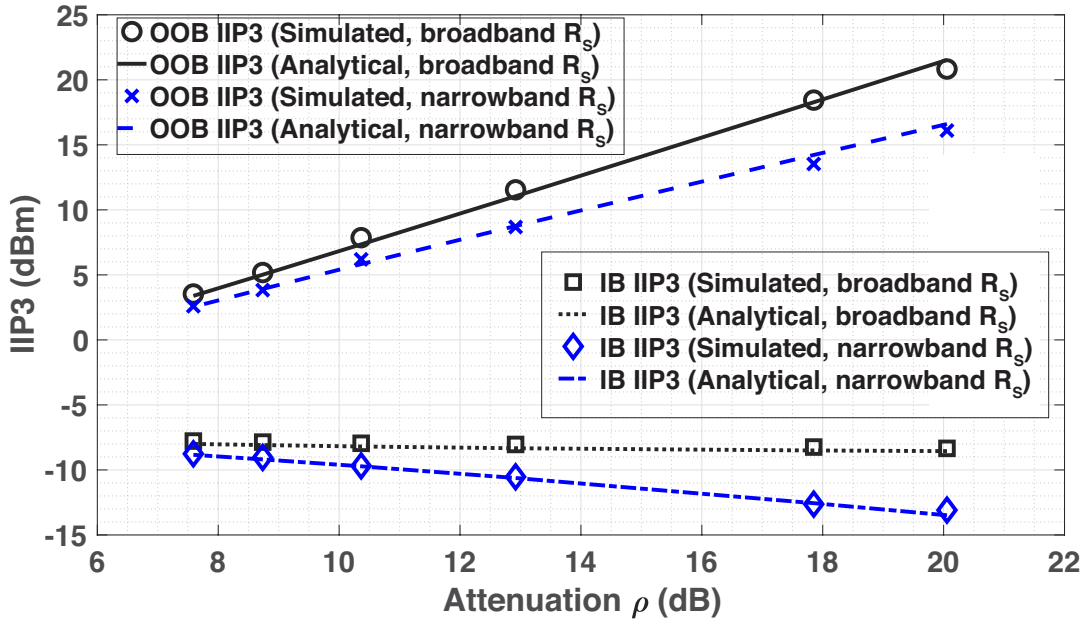


Figure 2.11: Simulated plot of in-band and far-out out-of-band IIP3 for different values of R_{SW2}. IIP3 is plotted against the far-out OOB attenuation ρ (in dB), as computed in equation (2.5). The plot is for a transformer with electrical turns ratio n of 3.3.

resistance R_S to as high a value as possible. That is, a high physical turns ratio is desired. 2) To achieve higher transformation ratio, the large physical turns ratio must be combined with a coupling k factor as close to 1 as possible. 3) The self resonance frequency (SRF) of the transformer structure must be higher than the desired frequency of operation. 4) The more tightly bound L_p and L_s are, the closer k is to unity. However, this lowers the SRF. 5) As discussed in the previous section, the antenna resistance R_S must appear broadband to the circuit. Therefore, the network quality factor Q_{match} must be as low as possible. 6) The quality factor Q_p of the primary inductance L_p must be as high as possible to minimize insertion loss IL. 7) It is important to note that the quality factor of the secondary inductance is not very significant. The series resistance $R_{ser,s}$ is in series with the input resistance looking into the chip, and its contribution to degrading the NF is minimal, as long as $Q_{match} > 0.5\sqrt{Q_p/Q_s}$. This may be inferred from equations (2.10) and (2.11), which give expressions for the noise figure due to the series resistance of the primary and secondary of the transformer, respectively. Therefore, on fixing a value of L_p, the turns ratio can be increased by increasing the secondary inductance L_s without any significant degradation in insertion loss due to degradation of Q_s (due to the use of narrower traces). However, L_s may not be increased arbitrarily as this causes a degradation in SRF.

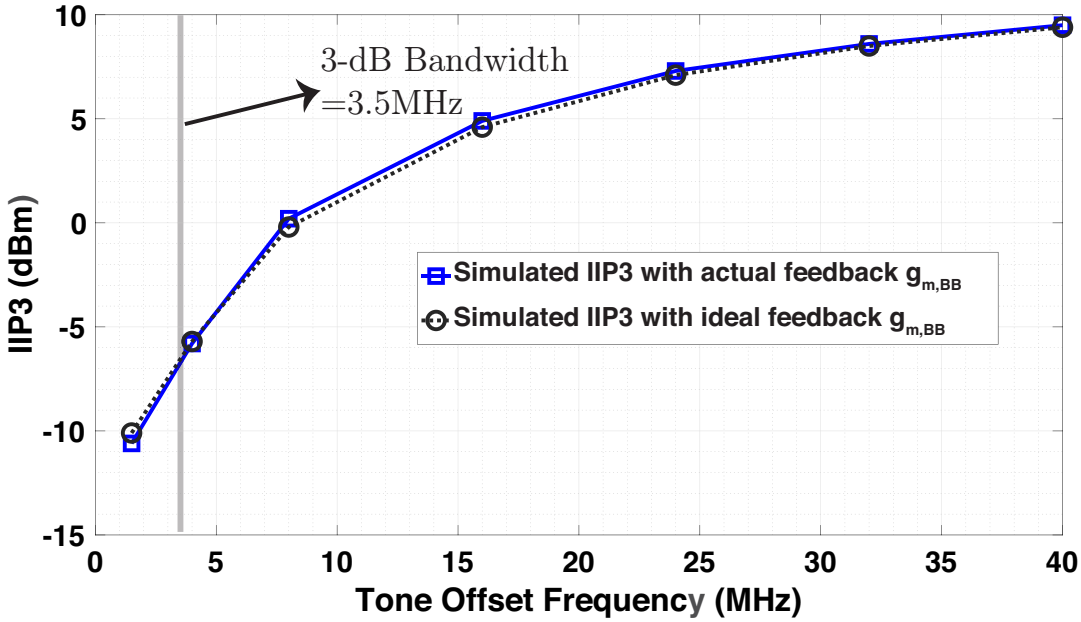


Figure 2.12: Simulated plot of 2-tone IIP3 as a function of tone offset. The plot is for a mixer switch resistance $R_{SW2} = 53\Omega$, transformer electrical turns ratio n of 3.3.

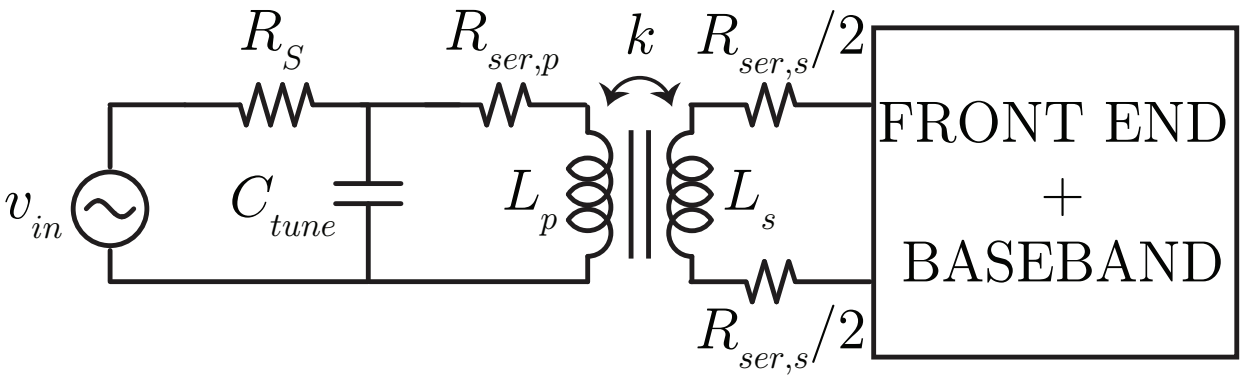


Figure 2.13: Schematic of the transformer

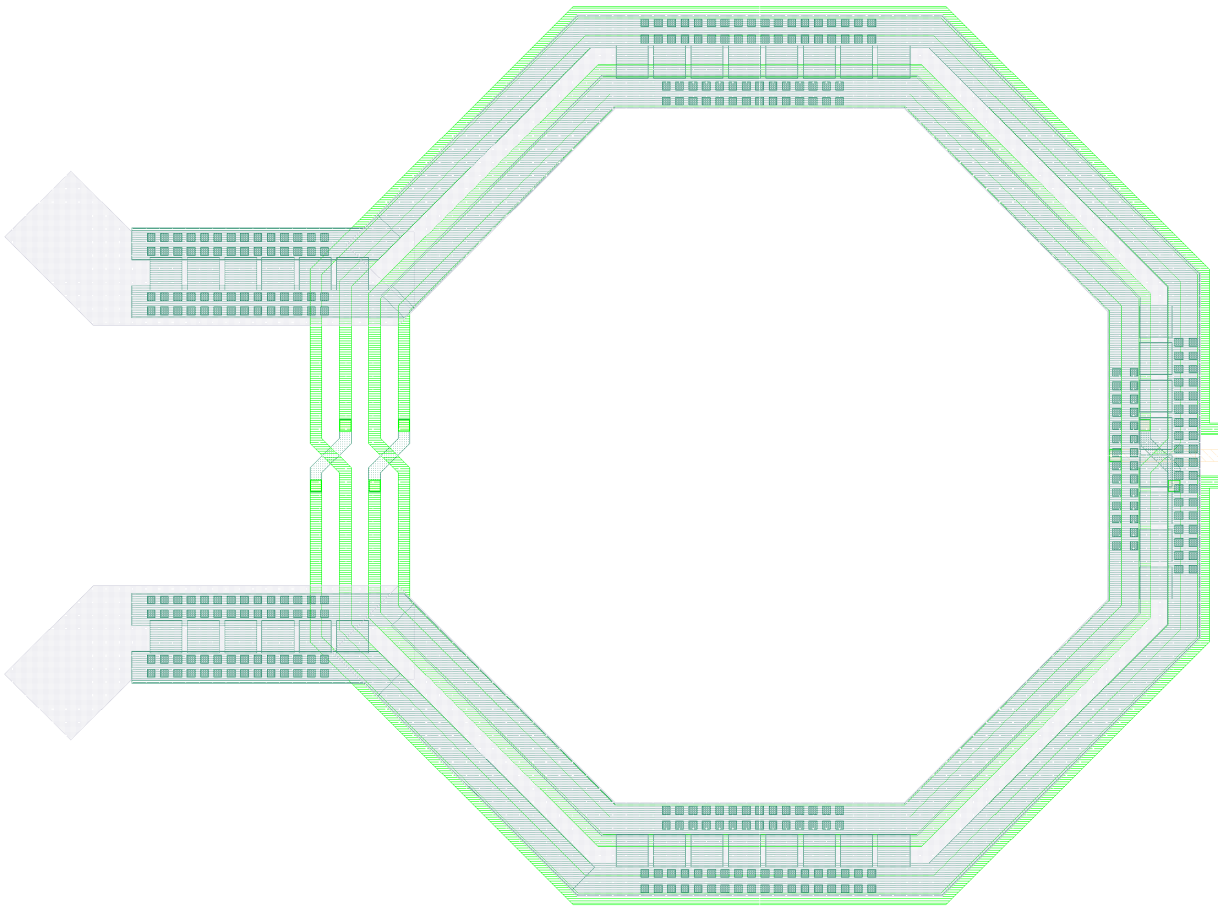


Figure 2.14: Layout of the transformer

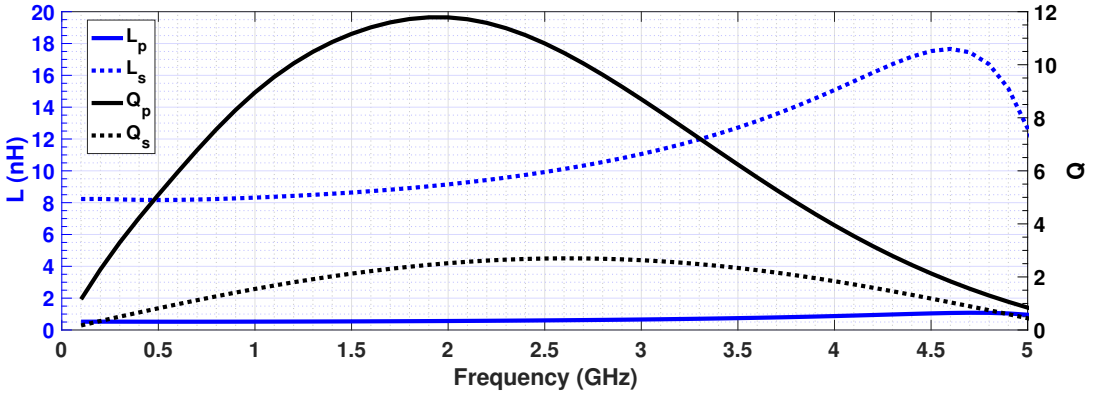


Figure 2.15: Simulated inductance and Q of the primary and secondary of the transformer

$$\mathrm{NF}|_{R_{ser,p}} = 1 + \frac{2Q_{match}}{Q_p} \tag{2.10}$$

$$\begin{aligned} \mathrm{NF}|_{R_{ser,s}} &= 1 + \frac{R_{ser,s}}{n^2 R_S} \\ &= 1 + \frac{1}{2Q_{match}Q_s} \end{aligned} \tag{2.11}$$

The transformer was designed taking all these factors into consideration. As seen in Fig. 2.14, the primary of the transformer is a single turn ($165\mu m$ radius) octagonal inductor. It was designed using 2 metal layers strapped together, a $35\mu m$ wide Al redistribution layer, strapped together with 2 parallel "shorted" turns of the highest metal layer (M10), each of which is $12\mu m$ wide. The secondary is a 4 turn ($165\mu m$ outer radius) octagonal inductor, each turn on the second highest metal layer (M9), each of width $4\mu m$. The absence of ultra-thick metal layers present in some RF processes, limits the inductor quality factor achieved. From the EMX-simulated results shown in Fig. 2.15, we observe that at 2.4GHz, an L_p of 0.59nH, a Q_p of $\sim$ 11, an L_s of 9.74nH and a Q_s of $\sim$ 2.5 are achieved. A k factor of $\sim$ 0.83 means that the effective electrical turns ratio ($n = k\sqrt{L_s/L_p}$) of 3.3 is achieved in simulation. The simulated SRF is $\sim$ 4.8GHz, which is 2$\times$ our frequency of operation.

2.5.2 Front-End LNA and Mixers

Fig. 2.16 shows the schematic of the capacitively cross coupled CG-LNA and the switching mixers used for down-conversion in the forward path and up-conversion in the feedback path, with transistor sizes indicated in μm. The CG-LNA has a resistive load and is broadband in nature. A channel length of 90nm was chosen as a compromise between intrinsic gain and f_T. The DC output of the LNA is isolated from the DC input of the first baseband stage through a coupling capacitor. The g_m of the LNA was biased at a low transconductor efficiency of 10 for better V_{GS} limited linearity. The choice of 5kΩ as the load resistor was a compromise between gain on one hand and bandwidth and V_{DS} limited linearity on the other. The down-conversion mixer switches (R_{SW1} = 220Ω) in the forward path are biased with a V_{GS} = 0.65V when they are on. The up-conversion feedback mixer switches (R_{SW2} = 55Ω) are not only 3 times bigger but are also biased with V_{GS} = 1V when they are on, to ensure best possible RF filtering given the power constraints.

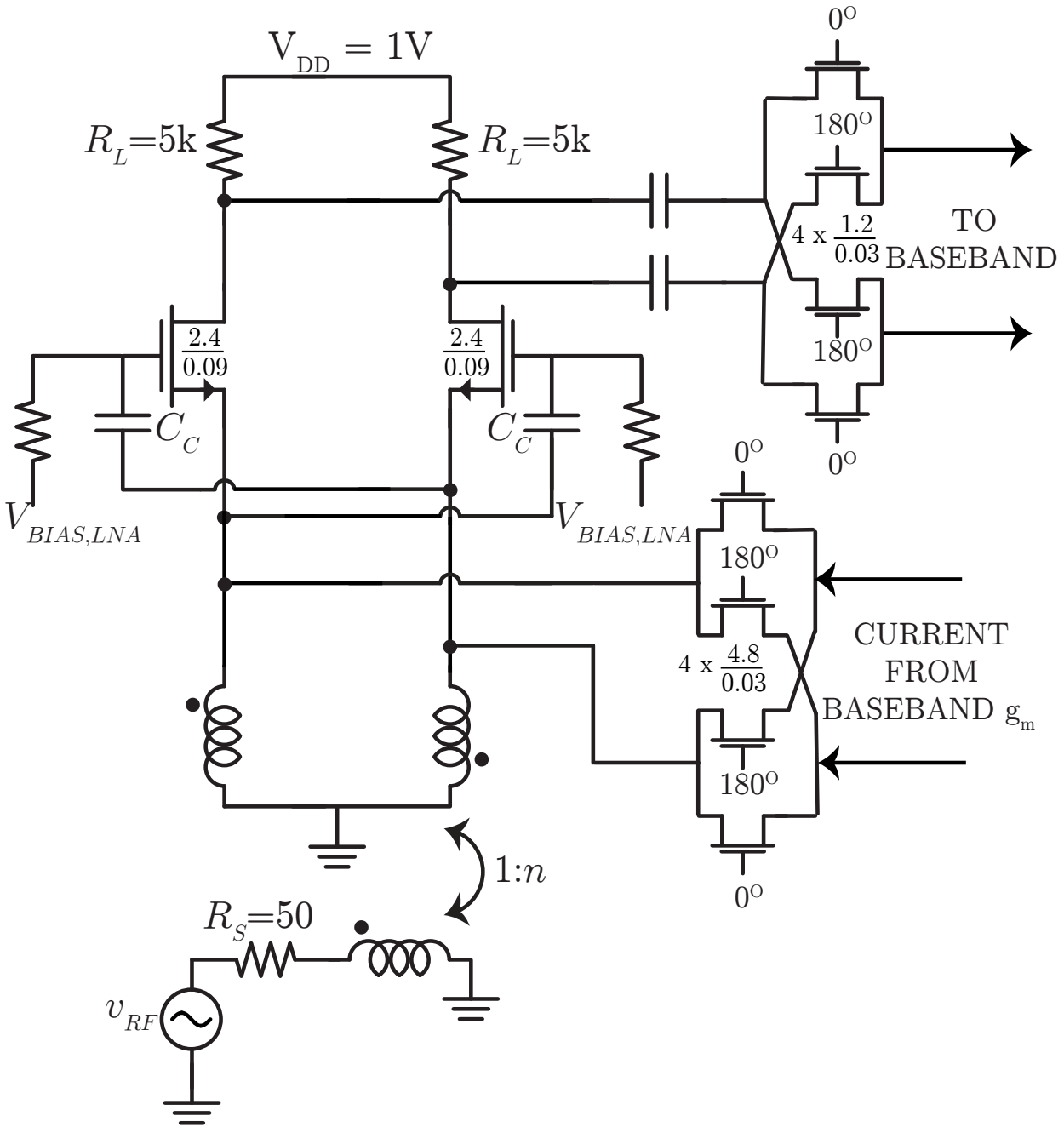


Figure 2.16: CCC-CG-LNA and passive mixers, I-path shown

2.5.3 Baseband Filter

A baseband amplifier with variable gain and bandwidth was also integrated into the system, to provide more gain and enhanced selectivity through higher order filtering. To this end,

a passive switched capacitor implementation was chosen to ensure low-power operation. Tapping into some recent work in passive switched capacitor filters [43], we have built a second-order baseband filter, with complex conjugate roll-off, whose gain and bandwidth can be varied with the frequency at which they are clocked (f_{CLK}). The expressions for gain, natural frequency of second order transfer function ω_0 and quality factor of the filter for the architecture shown in Fig. 2.17, are derived in [43], and are given by

$$\begin{aligned} \text{DC Gain} &= \frac{g_m}{f_{CLK} C_S} \\ \omega_0 &= \frac{2 f_{CLK} C_S}{\sqrt{C_{I1} C_S + C_{I2} C_S + 2 C_{I1} C_{I2}}} \\ Q &= \frac{\sqrt{C_{I1} C_S + C_{I2} C_S + 2 C_{I1} C_{I2}}}{C_{I1} + C_{I2} + C_S} \end{aligned} \tag{2.12}$$

It was shown in [43] that the maximum possible quality factor of such a passive switched capacitor filter is $1/\sqrt{2}$. Component values were chosen to achieve the maximum Q. It is known that for a second order low-pass transfer function with $Q = 1/\sqrt{2}$, the bandwidth is equal to ω_0. With this choice of Q, we notice from equation (2.12) that the DC gain varies linearly with the clock period T_{CLK} and the bandwidth varies linearly with the clock frequency f_{CLK}.

Due to the significantly worse flicker noise corner of NMOS devices in this process, we decided to use only long-channel PMOS devices in the baseband. To this end, high output resistance for the input g_m of the filter was achieved by boosting the output resistance of a simple resistively loaded PMOS differential pair using a cross-coupled g_m shown in Fig.2.17.

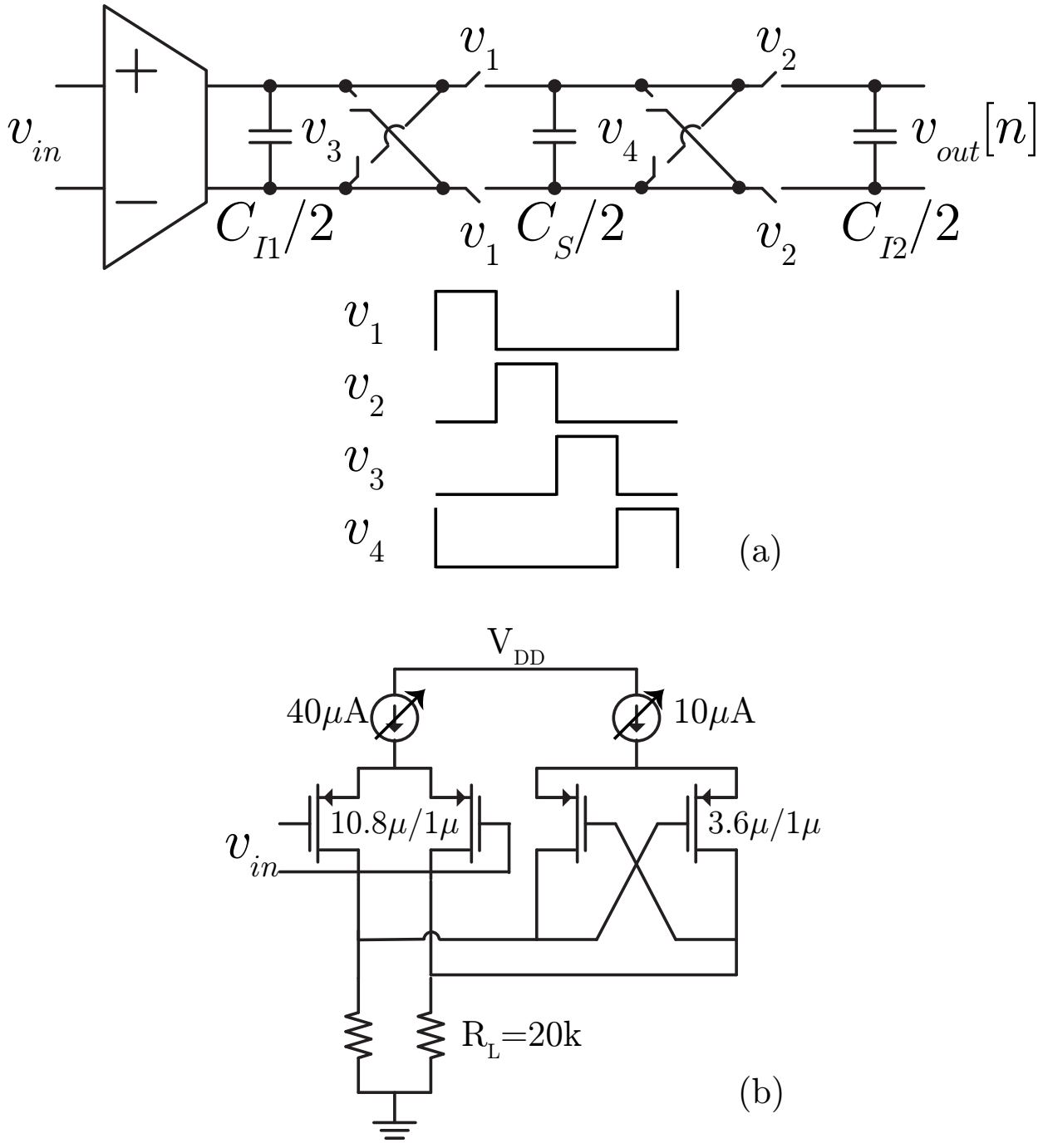


Figure 2.17: (a) Switched capacitor filter driven by g_m. (b) Transconductance driving the filter.

2.6 Measurement Results

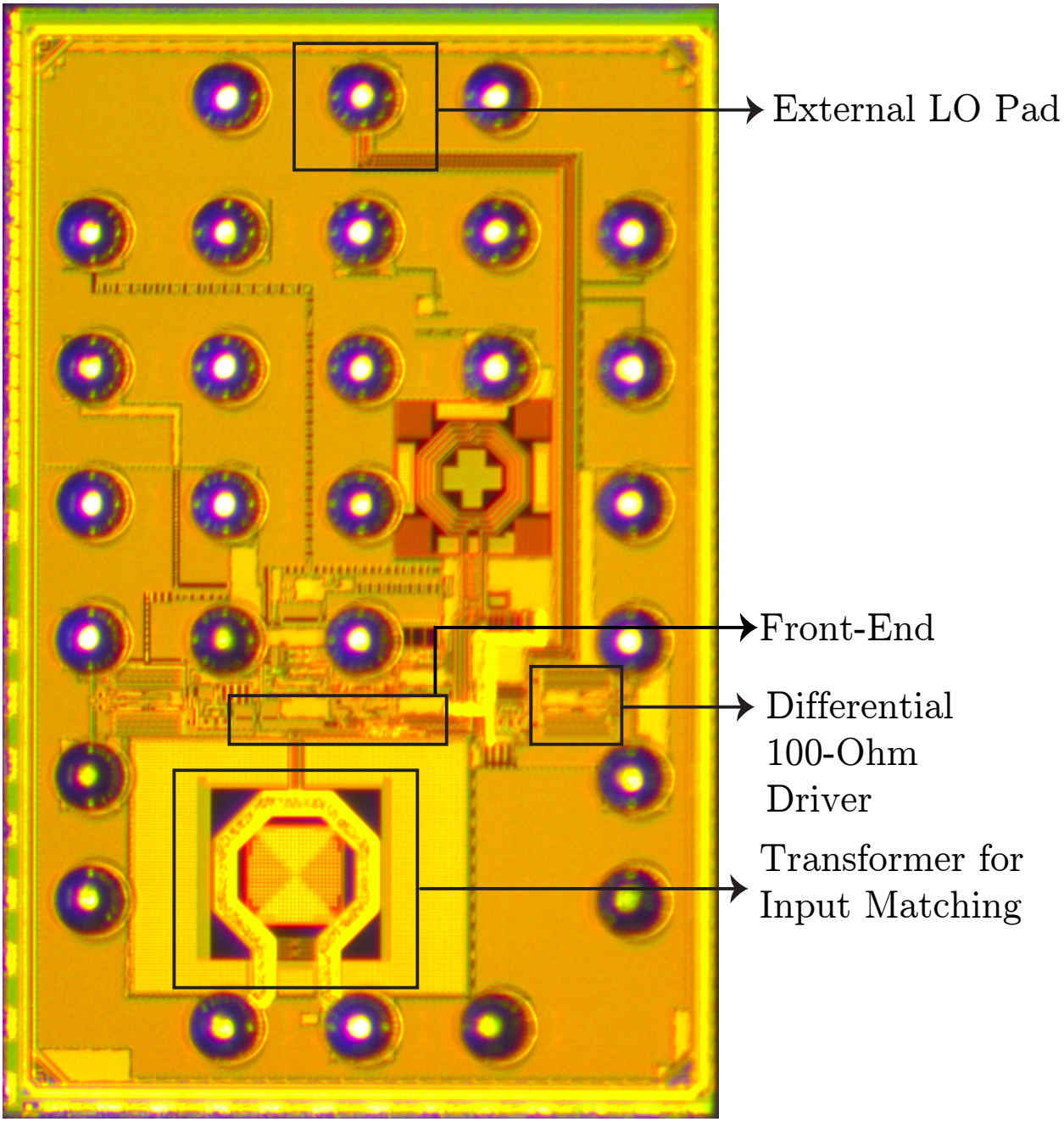
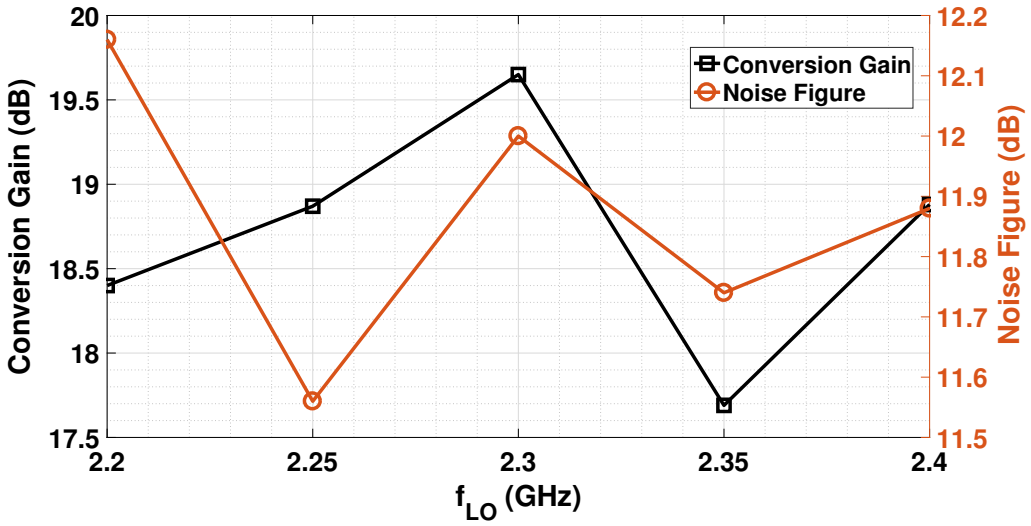


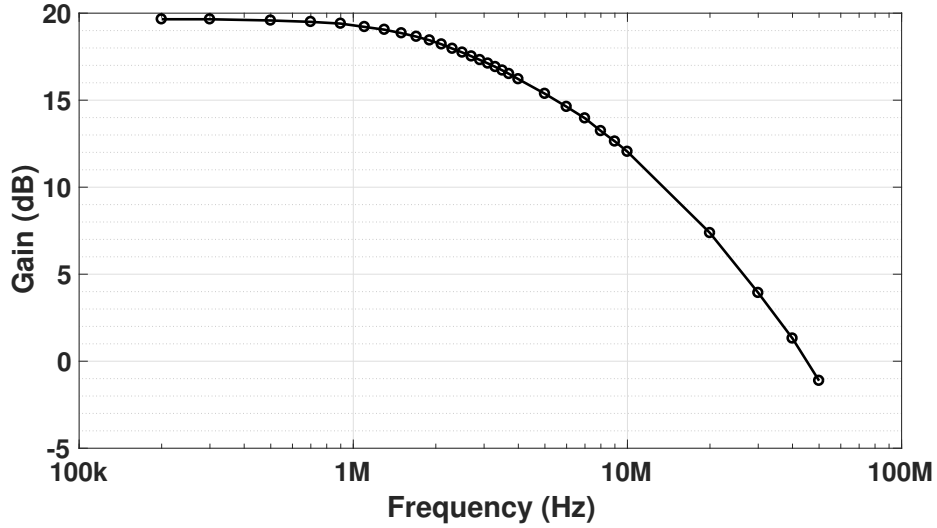
Figure 2.18: Chip Micrograph

The receiver front-end shown in Fig. 2.3 was fabricated in a 28nm bulk CMOS process. The die micrograph of the front-end is shown in Fig. 2.18. The receiver was characterized using

a flip-chip on board assembly with a 1V supply. The chip was characterized both using an external LO input.



(a) Conversion Gain and NF v/s f_{LO}



(b) Measured transfer function

Figure 2.19: Measured Gain, Noise Figure and Transfer function

The transfer function of the conversion gain of the front-end was characterized by sweeping the input tone from $f_{LO} + 0.2$MHz to $f_{LO} + 50$MHz. A maximum conversion gain of 19.65dB (including a loss of ∼2dB from the 50-ohm driver on chip, based on simulations) from the input to the differential I/Q output and a maximum bandwidth of 3.6MHz, were

achieved for $f_{LO} = 2.3$GHz. The noise figure was measured using a spectrum analyzer using the Y-factor method. A noise figure of 11.56dB was achieved in the best case. This is roughly 2dB higher than simulation. The mismatch could be due to incorrect noise models or more overlap in the LO. The conversion gain, noise figure and transfer function are plotted in Fig. 2.19.

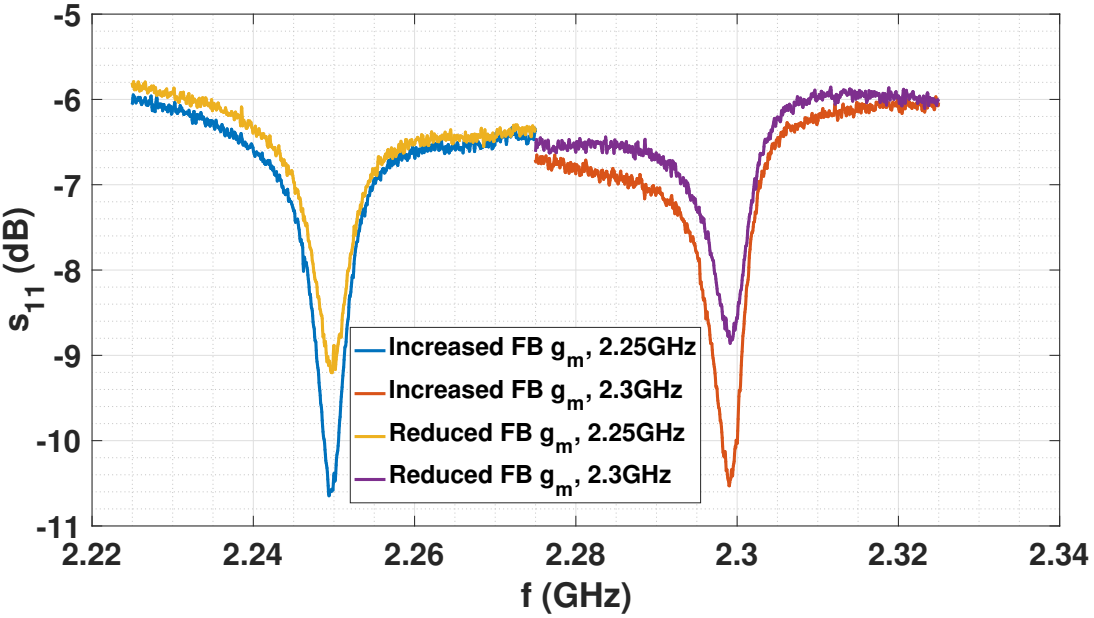
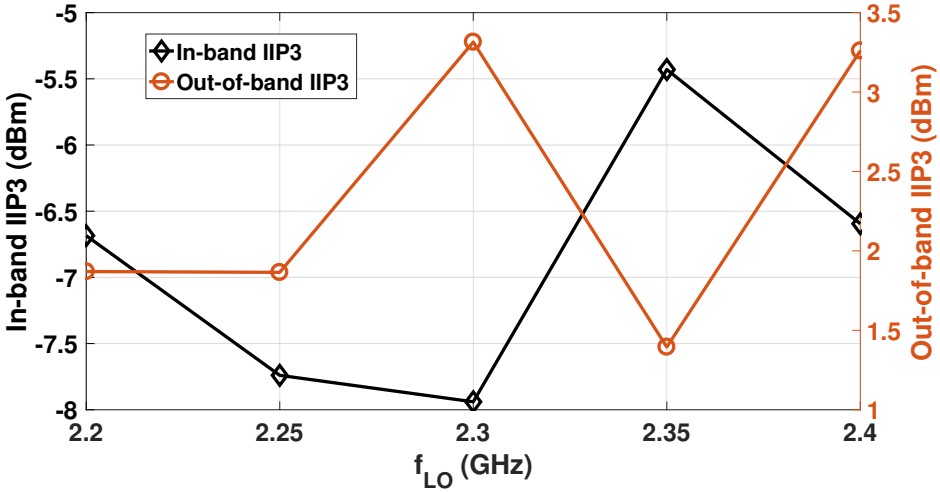


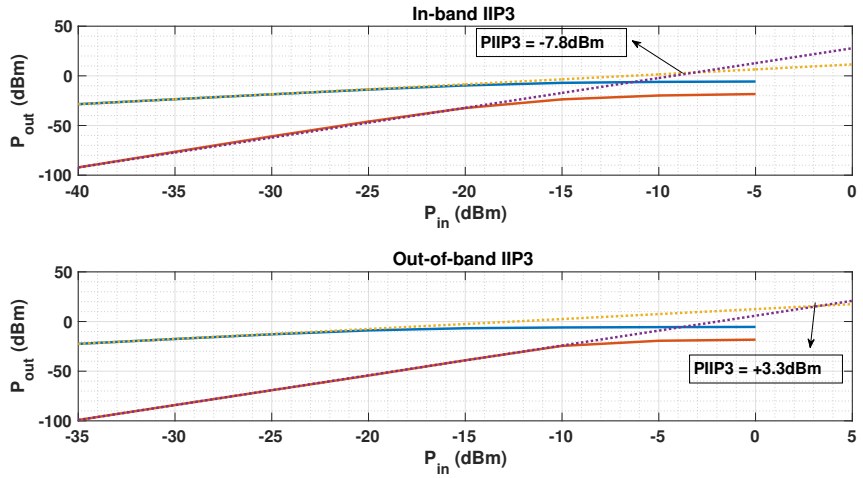
Figure 2.20: Effect of positive FB on matching from s_{11}

The effect of positive feedback on matching is illustrated in Fig. 2.20, which shows the plot of s_{11} with a lower and increased value of feedback g_m. The s_{11} at optimal matching was $3-4$dB worse than simulations.

The measured linearity is shown in Fig. 2.21. The IIP3 was characterized using 2 tones of equal power at $f_1 = f_{LO} + \Delta f + 1$MHz and $f_2 = f_{LO} + 2\Delta f + 1$MHz. For in-band IIP3, Δf was chosen to be 1MHz, and for out-of-band IIP3, it was chosen to be 50MHz. The IIP3 was extrapolated using another tone of same power placed at the same frequency as the in-band IM3 tone. In the best case, -5.5dBm and $+3.3$dBm IIP3 were achieved in and out-of-band, respectively. The measured in-band linearity matches simulation to within 1dB accuracy, but the out-of-band IIP3 was 3-4dB worse. This mismatch could be due to the well-known BSIM modeling issue while simulating the linearity of mixer switches [44]. The logic to generate the 4-phase non-overlapping LO and the buffer chain consumes a power of 290μW at 2.4GHz.



(a) IIP3 v/s f_{LO}



(b) Extrapolated In-band and out-of-band IIP3

Figure 2.21: Measured IIP3 v/s f_{LO} and measured IM3 v/s input power P_{in}

Finally, the on-chip baseband filter was also characterized for different values of f_{CLK}. As described in equation (2.12), an increase in measured bandwidth and a decrease in gain is observed with f_{CLK} (see Fig. 2.22). The roll-off also indicates that the desired second-order transfer function was achieved. The power consumption of the g_m driving these filters is 100μW.

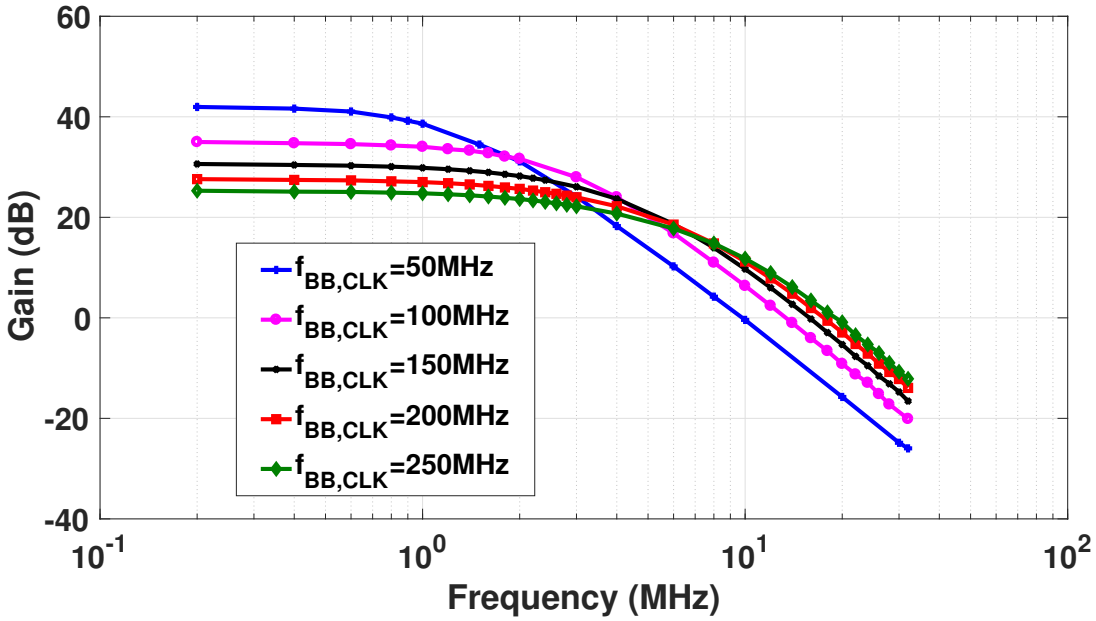


Figure 2.22: Measured transfer function of baseband switched capacitor filter for different values of f_{CLK}.

Table 2.1: Comparison With State-Of-Art sub-milliwatt 2.4GHz Receiver Front-Ends

Ref.	Gain (dB)	NF (dB)	IB IIP3 (dBm)	OOB IIP3 (dBm)	Power (mW)
This	**19-42**	**11.6**	**-6.5**	**+3.3**	**0.58**
[32]	22.9	8	-21	-	0.064
[34]	55.5	15.1	-15.8	-	0.6
[31]	20.6	6.55	-9.2	-	0.23
[45]	10-65	6.5	-20	-0.9	0.64
[35]	17.4	2.8	-10.7	-	0.475

Out-of-band (OOB) IIP3 expected to be equal to in-band (IB) IIP3 for other work, up to frequencies where broad-band matching networks may start causing attenuation

2.7 Conclusion

A sub-milliwatt 2.4GHz direct conversion receiver front-end has been demonstrated. The receiver is significantly more tolerant to out-of-band blockers than the state-of-the-art sub-mW receivers in the 2.4GHz ISM band (Table 2.1). Additionally, a detailed analysis of the proposed translational-feedback-based receiver front-end was provided, including detailed design oriented analysis of noise and non-linearity. Details of scaling this architecture to

obtain higher performance with power and the limitations thereof, were provided. The optimization of the transformer-based input matching network was also detailed.

Chapter 3

N-Path Filters with 40dB/decade RF selectivity

3.1 Introduction

With the proliferating number of bands with the advent of sub-6GHz 5G, mobile devices need to support many new bands. In this scenario, one of the strongest sources of interference is the leakage from a co-located transmitter. As detailed in [28, 46], this places extremely stringent requirements on linearity and interference resilience (Fig. 3.1). In the case of diversity receivers, whose antennas have as low as 15dB isolation, the leakage from a co-located transmitter can be as high as +8dBm, placing very stringent requirements on the blocker P1dB of the receivers. Additionally, in case of FDD systems, cross modulation between the transmitter leakage and a close in continuous wave blocker (typically -45 to -40dBm) causes a third order non-linearity. The resultant specification for IIP3 can be as high as $31 - 36$dBm. Both the B1dB and IIP3 specifications can be extremely challenging to meet in scaled CMOS processes with lower supply voltages.

The N-path filter is the ideal candidate to solve this problem due to its property of impedance translation, as illustrated in [19]. Consider an N-path filter in the passive mixer mode (Fig. 3.2(a)), driving a baseband impedance $Z_{BB}(s)$ and switched at frequency f_S. This linear periodic time varying (LPTV) circuit has a linear time invariant (LTI) representation for frequencies around f_S. The impedance translation manifests in this LTI equivalent in the impedance $Z_{BB}(s')$, where $s' = s - j\omega_{LO}$. In Fig.3.2(a), R_{sh} represents the losses due to harmonic re-upconversion.

In the last decade, there has been a vast volume of research attempting to improve the performance of N-path filters. [29, 40, 47–49] represent efforts made to improve the noise figure, selectivity and linearity (both in-band and out-of-band) of passive mixer-first receivers. N-path filters with notches were demonstrated in [49, 50], in order to improve selectivity. While the presence of notches definitely improved the selectivity, linearity suffered in the presence of blockers (-4.8dBm IIP3, -4dBm B1dB), due to the LNTA preceding the

N-path filter in [49]. N-path filters were cascaded through coupling RF transconductance in [48], in an attempt to improve selectivity and linearity, but the improvements in linearity were again limited by the presence of the RF transconductance. Discrete time switched capacitor techniques were investigated to enhance blocker tolerance in [51–53], but these suffered >7dB of noise figure. Some other notable works in this space include [46], which achieved enhanced blocker resilience (35dBm IIP3, 17dBm B1dB), but with a boosted supply voltage (2V), and [29] which introduced the concept of bottom-plate mixing to enhance linearity in the presence of blockers (44dBm IIP3, 13dBm B1dB). However, in [29], the parasitic capacitance of the capacitor used in the switch RC-kernel is seen at the RF input. This parasitic capacitance could potentially hurt the noise performance at higher RF frequencies.

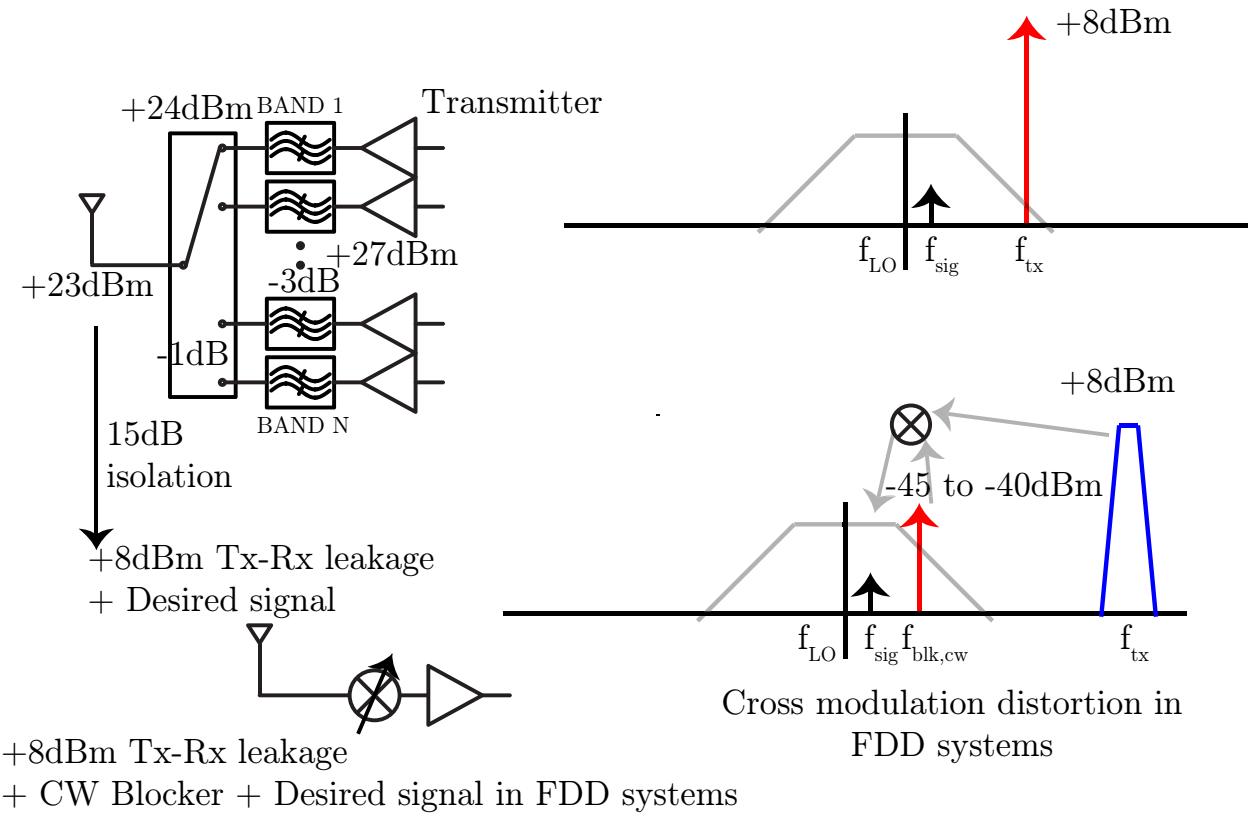


Figure 3.1: System diagram showing need for stringent linearity due to transmitter leakage to receiver.

One common theme among most of the works described thus far is that the N-path filter drives an impedance with 20dB/decade roll-off, or in the case of the notches, an impedance which peaks after the transmission zero. Therefore, while these do have selectivity in their baseband response, the transfer function at the RF node v_x has a limited 20dB/decade roll-off. The natural question that arises is if it is possible to synthesize a baseband impedance with 40dB/decade roll-off, as shown in Fig. 3.2(b). If such an impedance is presented as the

load to the N-path filter, it is expected that the RF filtering profile at the node v_x would have a sharper roll-off than a conventional N-path filter driving a shunt RC impedance. The benefits of such a topology were investigated in [28, 30, 54]. [28, 54] implemented the impedance with 40dB/decade roll-off using positive capacitive feedback. The implementation leads to undesirable zeros in the transfer function, limiting the range of frequencies up to which the 40dB/decade roll-off benefits are observed. As seen in equations (4) - (6) of [28], both the zeros and the poles depend on the same parameters C_1 and r_o, the feedback capacitance and output resistance of the amplifier, respectively.

In [30], we proposed a method of synthesizing the impedance with 40dB/decade roll-off, which breaks the tightly coupled trade-off between the location of the poles and zeros, at the expense of power. Compared to [30], this chapter goes into greater detail about the impedance synthesis and analyzes the transfer function, noise figure and non-linearity contributions from different sources. In addition, details about stability and layout techniques to minimize sensitivity of stability to changes in component values, are presented. A lower power version of the circuit demonstrated in [30], where power is traded off for some linearity while maintaining selectivity, is also presented.

The content of this chapter is organized as follows. Section 3.2 describes the receiver front-end architecture. It uses LTI models to build from the desired transfer function to the desired impedance to achieve the same, in a step-by-step fashion. Section 3.3 delves into the details of circuit implementation, stability and analyzes other performance metrics. Section 3.4 shows the measurement results and comparison with state-of-the-art, and Section 3.5 concludes by providing the key takeaways of the work.

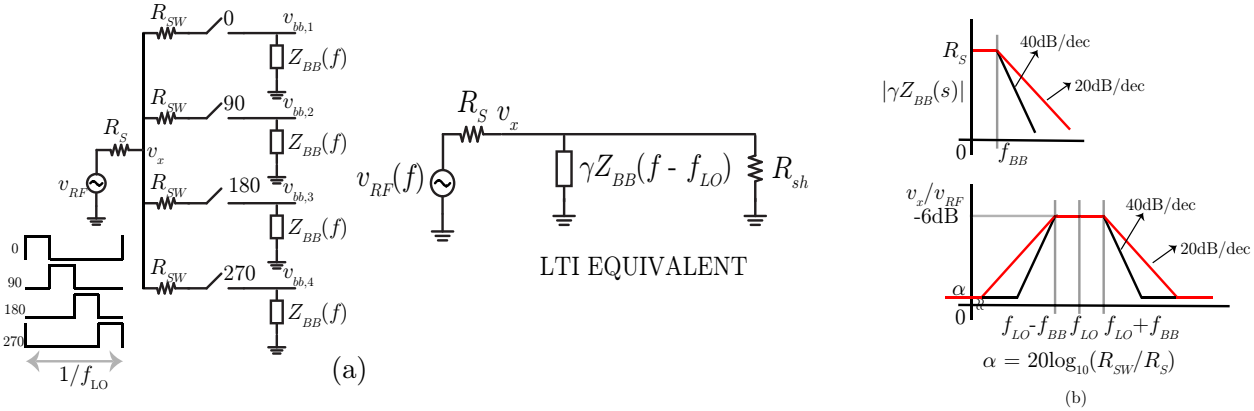


Figure 3.2: (a) LTI equivalent of N-path filters at f_{LO} (b) Impedance translation in N-path filters.

3.2 Receiver Architecture

As motivated in the previous section, the goal of this work is to achieve improved blocker tolerance, by building an N-path filter which drives an impedance with 40dB/decade roll-off.

Using the standard notation s for complex frequency and $s' = s - j\omega_{LO}$ for the frequency-translated complex frequency, the transfer function required at node v_x of Fig. 3.2(b), is given by

$$\frac{v_x}{v_{RF}}(s) = \frac{1}{2}\frac{1}{1 + \frac{s'}{\omega_0 Q} + \frac{s'^2}{\omega_0^2}} \tag{3.1}$$

The factor of $\frac{1}{2}$ comes from the requirement for input matching. The other term is the standard representation of a second order low-pass transfer function in the frequency translated variable s'. Equivalently, it represents a band-pass transfer function with 40dB/decade roll-off and centered at f_{LO}. In this work, our target is to build a second order Butterworth filter. Any other second order transfer function may also be realized with appropriate choice of component values. It is easy to back-calculate the impedance $Z_{BB}(s)$ required to achieve the desired transfer function in equation (3.1). The required $Z_{BB}(s)$ is given by

$$\begin{aligned} \gamma Z_{BB}(s) &= \frac{R'_S}{1 + \frac{2s}{\omega_0 Q} + \frac{2s^2}{\omega_0^2}} \\ R_S &= R'_S || R_{sh} \end{aligned} \tag{3.2}$$

γ is the scaling factor associated with impedance translation in an N-path filter and is given by $\gamma = 2/\pi^2$ in the case of an N-path filter driven by four non-overlapping phases. The second condition on R_S comes from the requirement for input matching. It is observed that the impedance $Z_{BB}(s)$ is a second order all-pole impedance.

Electrical network theory [55] tells us that such $Z_{BB}(s)$ is not realizable using only passive elements. One particular active synthesis of a second order all pole impedance has been explored in [56]. However, till [28, 54], second order all-pole impedances haven't been used in N-path filters. This work provides a new method of synthesizing a second order all-pole driving point impedance, which acts as the load to an N-path filter.

3.2.1 Impedance Synthesis - "Super-cap"

The desired $Z_{BB}(s)$ is given by equation (3.2). Decomposition of the corresponding $Y_{BB}(s)$ gives insights on how to go about synthesizing the impedance.

$$\frac{Y_{BB}(s)}{\gamma} = \frac{1 + \frac{2s}{\omega_0 Q} + \frac{2s^2}{\omega_0^2}}{R'_S} = \frac{1}{R'_S} + Y_1(s) \tag{3.3}$$

$$Y_1(s) = \frac{\frac{2s}{\omega_0 Q} + \frac{2s^2}{\omega_0^2}}{R'_S} = sC_1\left(1 + \frac{s}{\omega_1}\right) \tag{3.4}$$

There are two key observations from equations (3.3) and (3.4). First, we observe that the desired admittance $Y_{BB}(s)$ may be expressed as a shunt combination of a realizable conductance given by $\frac{1}{R'_S}$ and an admittance $Y_1(s)$. From equation (3.4), we observe that

$Y_1(s)$ asymptotically behaves like a capacitance C_1 upto frequency ω_1, and has a steeper 40dB/decade roll-off for frequencies higher than ω_1. We refer to this admittance as a "super-cap" to emphasize its enhanced roll-off. $Y_1(s)$ too does not have a passive realization. Now, consider the impedance $Z_1(s)$.

$$Z_1(s) = \frac{1}{sC_1\left(1 + sC_1R_1\right)} = \frac{1}{sC_1} - \frac{R_1}{1 + sC_1R_1} \tag{3.5}$$

By design, we choose $\omega_1 = 1/R_1C_1$, where R_1 and C_1 are a realizable resistance and capacitance, respectively. The partial fraction decomposition in equation (3.5) is a central idea in realizing the "higher-order" impedance. $Z_1(s)$ may be interpreted as a series combination of a capacitance C_1 and another impedance $Z_2(s)$, where $Z_2(s)$ is given by

$$Z_2(s) = -\frac{R_1}{1 + sC_1R_1} \tag{3.6}$$

$Z_2(s)$ is a shunt combination of a negative resistance $-R_1$ and a negative capacitance $-C_1$. $Z_{BB}(s)$ thus derived, as described in equations (3.3) - (3.6) and summarized in Fig. 3.3, when driven by an N-path filter, yields the desired 40dB/decade roll-off at the RF node v_x (Fig. 3.2). One may also observe an additional shunt capacitance C_2 in Fig. 3.3. This does not change the nature of the transfer function in any way, but provides additional flexibility, especially with respect to pushing out zeros associated with the circuit implementation, to a higher frequency. The current source i_n in Fig.3.3 represents the noise and non-linearity due to the negative R and will be discussed in detail in a subsequent section.

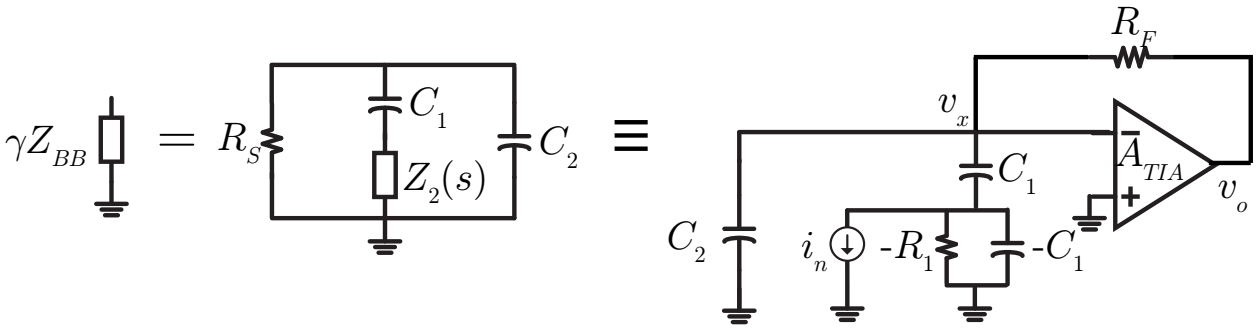


Figure 3.3: Impedance with 40dB/dec. roll-off.

The resistive component of $\gamma Z_{BB}(s)$, which is given by R_S, is not realized using a physical resistor, as this places a 3dB limit on the NF. Rather, it is realized by having a resistor R_F in feedback across an amplifier of gain A_{TIA}. By consuming sufficient power in the amplifier, the noise figure can be lowered below 3dB (as seen from equation (33) in [19]). The physical realization of every element in Fig. 3.3 is quite obvious, except for the negative resistance $(-R_1)$ in shunt with the negative capacitance $(-C_1)$. The details of the active circuit implementation of $Z_2(s)$, given by equation (3.6), forms a large part of the next section.

3.3 Circuit Design, Analysis and Trade-offs

3.3.1 Amplifier for Shunt Negative RC Synthesis

The main challenge, thus far, is the implementation of $Z_2(s)$, given by equation (3.6). A driving point impedance of a negative resistance $-R_1$ in shunt with a negative capacitance $-C_1$, is implemented by putting a resistor $R_1(A-1)$ and a capacitance $C_1/(A-1)$ in positive feedback around an amplifier of gain A. The most obvious way to implement this would be to cross-couple the desired resistance and capacitance across a differential pair (Fig. 3.4(a)). Note here that the output resistance of the amplifier A is positive R_{out}. We will contrast this with the actual implementation later. The input impedance $Z_2'(s)$, as marked in Fig. 3.4 (b), is given by

$$\begin{aligned} Z_2'(s) &= -\frac{R_1}{1+sC_1R_1}\frac{1+\frac{R_{out}}{(A-1)R_1}+s(\frac{C_1}{A-1}+C_{par})R_{out}}{1-\frac{sC_{par}R_{out}}{A-1}} \\ &\approx -\frac{R_1}{1+sC_1R_1}\frac{1+s(\frac{C_1}{A-1}+C_{par})R_{out}}{1-\frac{sC_{par}R_{out}}{A-1}} \end{aligned} \tag{3.7}$$

It is seen that while we wanted to implement $Z_2(s)$ as given by equation (3.6), we ended up with $Z_2'(s)$, which has an additional pole and a zero. The approximation that $R_{out}/(A-1) \ll R_1$ was used in the above equation. On replacing $Z_2(s)$ in Fig. 3.3 with $Z_2'(s)$, computing the corresponding baseband impedance $\gamma Z_{BB}(s)$, and finally plugging this into the LTI model shown in Fig. 3.2(b), the transfer function $v_x/v_{RF}(s)$ is given by equation (3.8). For an ideal implementation of the amplifier A, with $R_{out} = 0$ and $C_{par} = 0$, it may be seen that the transfer function in equation (3.8) resembles the form of the desired transfer given by equation (3.1), for appropriate choice of component values. However, with a non-zero R_{out}, the transfer function is a 2-zero, 3-pole transfer function. By minimizing R_{out}, C_{par} by design, U and V, the coefficients of s' and s'^2 respectively, in equation (3.8), may be made positive. However, the coefficient W of s'^3 is negative. Routh-Hurwitz stability criterion tells us that this transfer function will have a right-half plane pole, and hence is unstable. On careful observation of the coefficients U, V and W, it is apparent that if all the R_{out} terms were replaced by $-R_{out}$, the coefficients U, V and W are now always positive. Now, the system can be made stable according to Routh-Hurwitz stability criterion.

$$\begin{aligned}
&\frac{v_x}{v_{RF}}(s) = \frac{1}{2}\frac{1 - s'\frac{(C_{par}+C_1)}{A-1}R_{out} - s'^2 R_1 R_{out}\left(C_1\frac{C_{par}}{A-1} + C_1\frac{C_1}{A-1} + C_{par}C_1\right)}{1 + Us' + Vs'^2 + Ws'^3} \\
&U = \frac{C_1 R_S}{2} - \frac{(C_{par}+C_1)R_{out}}{A-1} \\
&V = \frac{R_1 R_S C_1^2}{2} - R_1 R_{out}\left(C_1\frac{C_{par}}{A-1} + C_1\frac{C_1}{A-1} + C_{par}C_1\right) - \frac{R_S R_{out} C_1 C_{par}}{2(A-1)} \\
&W = -\frac{C_1^2 C_{par} R_1 R_{out} R_s}{2(A-1)}
\end{aligned} \tag{3.8}$$

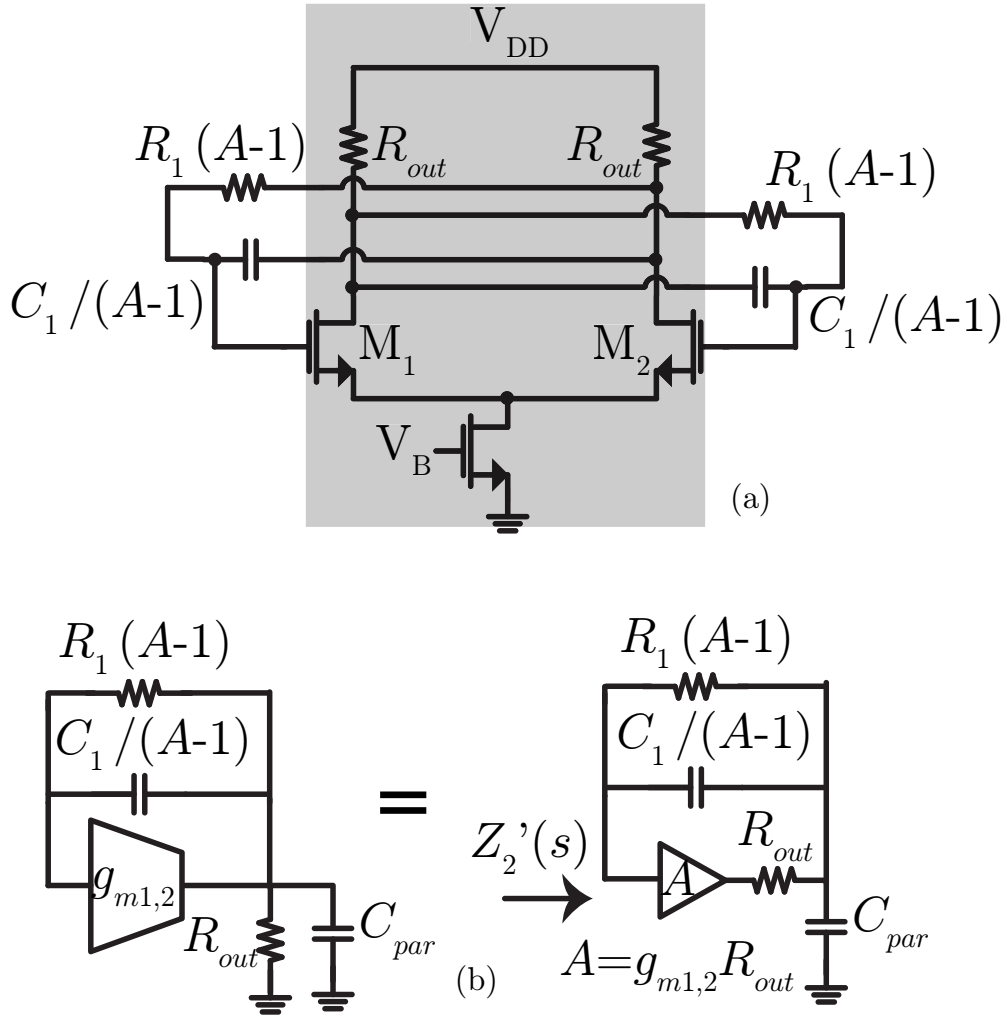


Figure 3.4: (a) Cross-coupling resistance and capacitance across a differential pair to realize negative shunt RC. (b) Small-signal equivalent.

To obtain the shunt negative RC impedance, the resistor $R_1(A-1)$ and the capacitance $C_1/(A-1)$ must be connected in positive feedback around an amplifier of positive gain A but negative output resistance $-R_{out}$ (Fig. 3.5(a)). Such an amplifier may be implemented by a differential pair driving a cross-coupled load, as shown in Fig. 3.5(b).

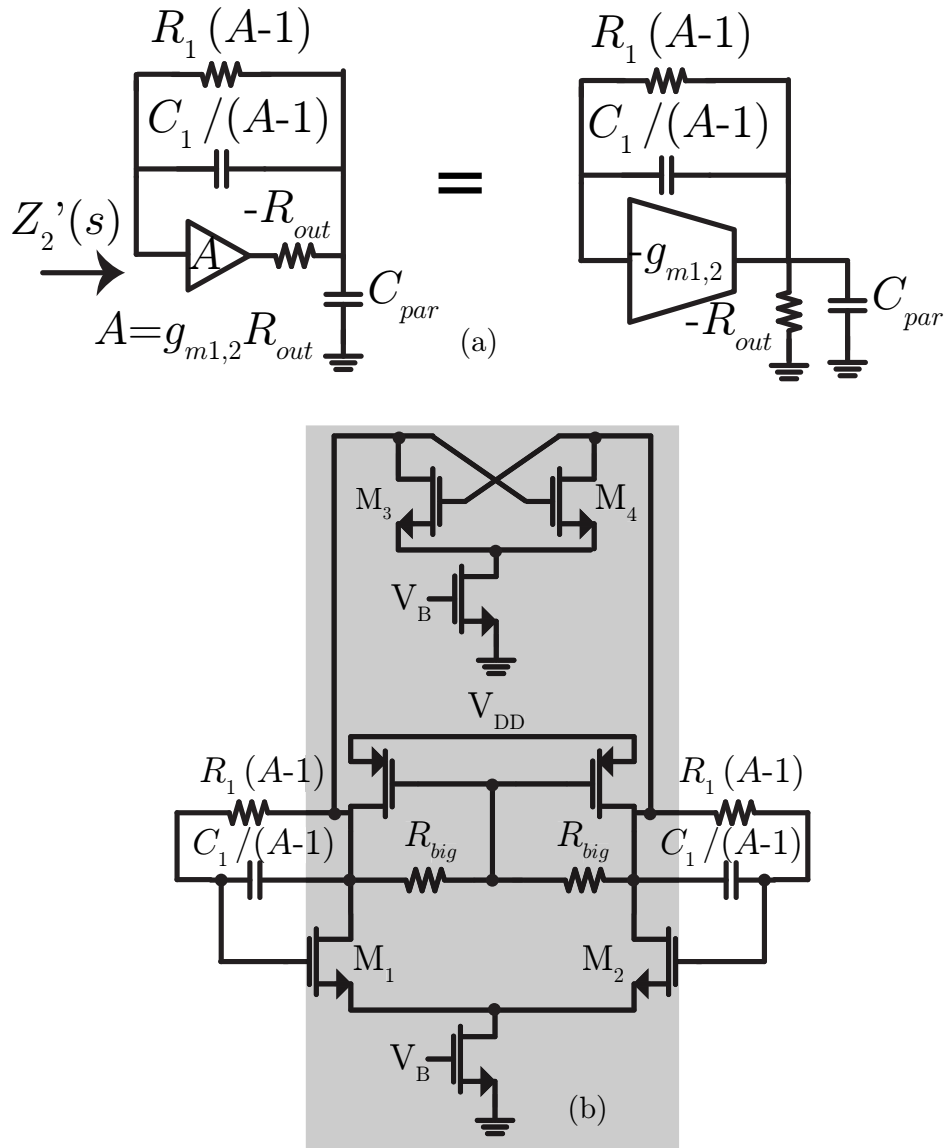


Figure 3.5: (a) Small-signal equivalent of desired implementation. (b) Transistor level schematic of negative RC implementation.

3.3.2 Implementation Zeros - Trade-offs and Solution

It may be observed from the transfer function v_x/v_{RF} in equation (3.8), that there are 2 undesired zeros in the transfer function, the magnitude of which is proportional to $1/R_{out}$. In other words, reducing R_{out} pushes out the zeros, thereby enhancing the range of frequencies over which the 40dB/decade roll-off is obtained. For the implementation shown in Fig. 3.5,

$$\begin{aligned} R_{out} &= \frac{1}{g_{m3,4}} \\ A &= \frac{g_{m1,2}}{g_{m3,4}} \\ |\omega_z| &\propto g_{m3,4} \end{aligned} \tag{3.9}$$

From equation (3.9), we make a few inferences. To push the zeros out to higher frequencies, $g_{m3,4}$ and consequently, power consumption must be increased. For a fixed power consumption, the highest value of $g_{m3,4}$ (and consequently, higher frequency zeros), means A should be as small as possible. Also, $A > 1$ to ensure that positive feedback is actually exploited. In this design, a gain of $A = 2$ was chosen. However, this does mean the value of capacitance $C_1/(A-1)$ in feedback is actually C_1. Therefore, by choosing a gain of $A = 2$, area of capacitance used is traded off for higher frequency zeros in the transfer function. The value of the capacitance in feedback may also be offset slightly from $C_1/(A-1)$ to account for the parasitic capacitance at the input node of the amplifier A.

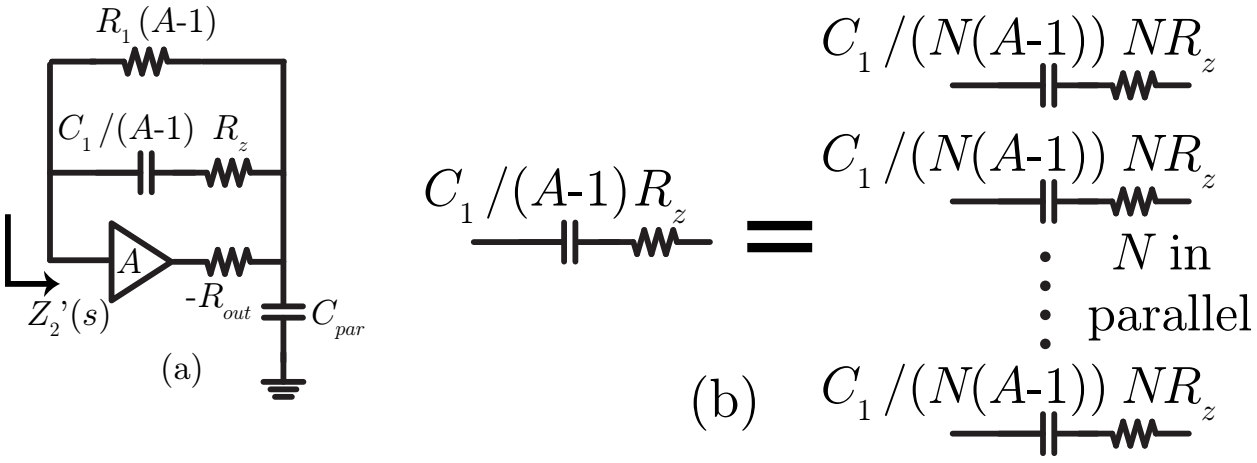


Figure 3.6: (a) Series resistance R_z to push the location of zeros further out. (b) Actual implementation.

The trade-off between power consumption and the location of the zeros may be broken by introducing a resistance R_z in series with the capacitance $C_1/(A-1)$ in feedback (Fig. 3.6(a)), an idea inspired by pole-zero cancellation resistances in op-amp cancellation. The

impedance $Z_2'(s)$ looking into the input node (Fig. 3.6(a)), is given by,

$$\begin{aligned} Z_2'(s) &\approx -\frac{R_1}{1+sC_1R_1}\times \\ &\frac{1-s((\frac{C_1}{A-1}+C_{par})R_{out}-R_Z\frac{C_1}{A-1})-s^2C_{par}\frac{C_1}{A-1}R_zR_{out}}{1+sC_{par}\frac{R_{out}}{A-1}} \\ &\approx -\frac{R_1}{1+sC_1R_1}\frac{1-s\frac{C_1}{A-1}(R_{out}-R_z)}{1+sC_{par}\frac{R_{out}}{A-1}} \end{aligned} \tag{3.10}$$

In the second step of equation (3.10) above, we neglect C_{par} with respect to $C_1/(A-1)$. Neglecting the parasitic capacitance C_{par} and the other far-out zero of $Z_2'(s)$ in equation (3.10), are reasonable approximations, which will give intuition about the role of the resistance R_z. The approximate form of $Z_2'(s)$ in equation (3.10) is very similar to that in equation (3.7), except now, R_{out} in the numerator is replaced by $-(R_{out}-R_z)$. Without the series resistance, it was observed that $|\omega_z| \propto 1/R_{out}$. Now, $|\omega_z| \propto 1/(R_{out}-R_z)$. Therefore, the zero in the transfer function v_x/v_{RF} is now pushed to a higher frequency.

Another intuitive way to look at this is as follows. Neglecting the effect of C_{par}, in Fig. 3.5(a), the capacitance $C_1/(A-1)$ is connected in positive feedback around an amplifier of gain A and output resistance $-R_{out}$. In Fig. 3.6(a), the capacitance $C_1/(A-1)$ is connected in positive feedback around an amplifier of gain A but a smaller output resistance $-(R_{out}-R_z)$. By putting R_z in series with the capacitance $C_1/(A-1)$, the magnitude of the effective output resistance of the amplifier A has been reduced. This also tells us the approximate limits to increasing R_z. If $R_z > R_{out}$, the effective output resistance of the amplifier is now positive, and hence similar to the case of cross-coupling a resistor and capacitor across a differential pair (Fig. 3.4), which was shown to be unstable. Therefore, care needs to be taken about the value of R_z used. It may be noted that the proportionality of $|\omega_z|$ to $1/(R_{out}-R_z)$ is only an approximation that serves to provide intuition, as observed from the root locus plot in Fig. 3.7.

Consider a case where the values of components in Figs. 3.3 and 3.5, are given by, $R_1 = 170\Omega, C_1 = 100\text{pF}, C_2 = 75\text{pF}, A = 2, R_{out} = 10\Omega, C_{par} = 10\text{pF}$. When $R_z = 0$, that is, there is no series resistance, the transfer function $v_x/v_{RF}(s')$ has one far-out non-dominant pole as seen in equation (3.8). However, for $R_z \neq 0$, it can be shown that there are 2 non-dominant poles. The root locus of these non-dominant poles as a function of R_z is shown in Fig. 3.7(b). It is seen that for values of R_z beyond a certain threshold, the circuit becomes unstable. Fig. 3.7(a) shows the small signal low-pass transfer function as R_z is varied, only for cases where the circuit is stable. It can be observed that the frequency of the zeros is indeed pushed out further as R_z is increased. However, it may also be observed that the quality factor of the zeros reduces. Therefore, if one desires to have a shunting notch akin to the circuit in [54], then a higher quality factor zero-pair is desired. However, for having an extended range of 40dB/decade roll-off without peaking in response, a higher value of R_z is desired. The transfer function from the equivalent noise current source of R_z to the

baseband output v_o is high-pass. Hence, there is no impact of R_z on the noise figure at the lower frequencies of the band. It can also be shown that impact of R_z on noise at the edge of the band is negligible.

Finally, some layout related techniques are described regarding the implementation of R_z. It was seen from the root locus plot in Fig. 3.7(b) that a change in few ohms of resistance could lead to instability. Therefore, the relevant routing on chip was done on a higher metal layer with lower sheet resistance. Additionally, the series combination of $C_1/(A-1)$ with R_z was implemented as a parallel combination of N paths, each of capacitance $C_1/(N(A-1))$ in series with a resistance NR_z (Fig. 3.6(b)). Now, the series resistance in each path is N times higher, therefore reducing the sensitivity of stability to routing resistance variations. In this case, $N = 28$ was used, thereby implementing the effective $R_z = 10\Omega$ using 280Ω in each of the 28 paths.

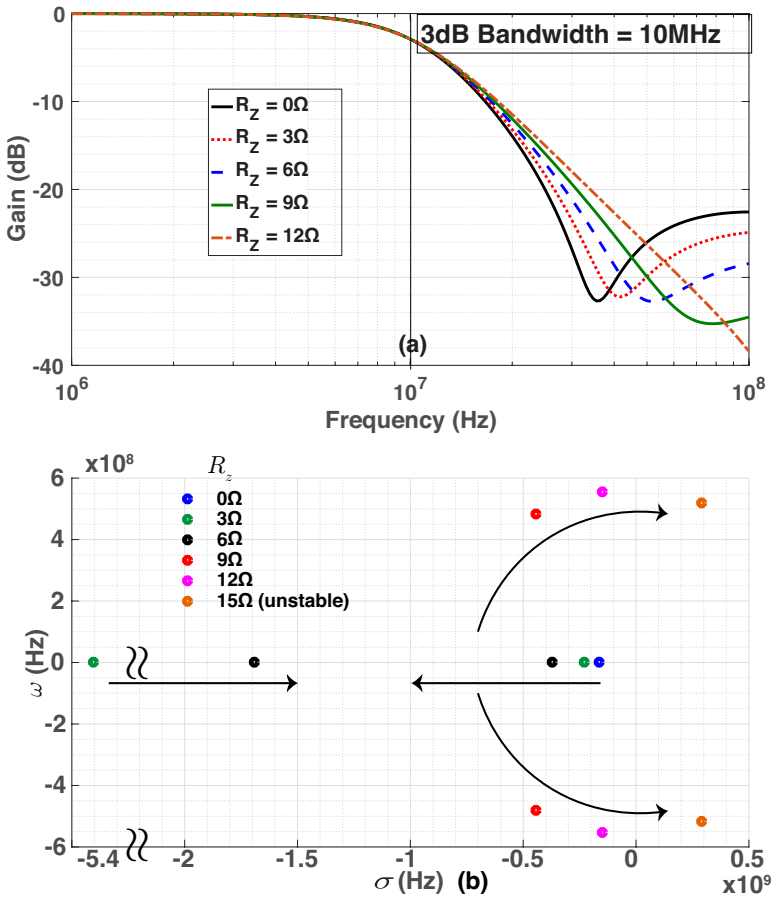


Figure 3.7: (a) Low-pass function v_x/v_{RF} for different values of $R_z(\Omega)$. (b) Root locus of non-dominant poles as $R_z(\Omega)$ varies.

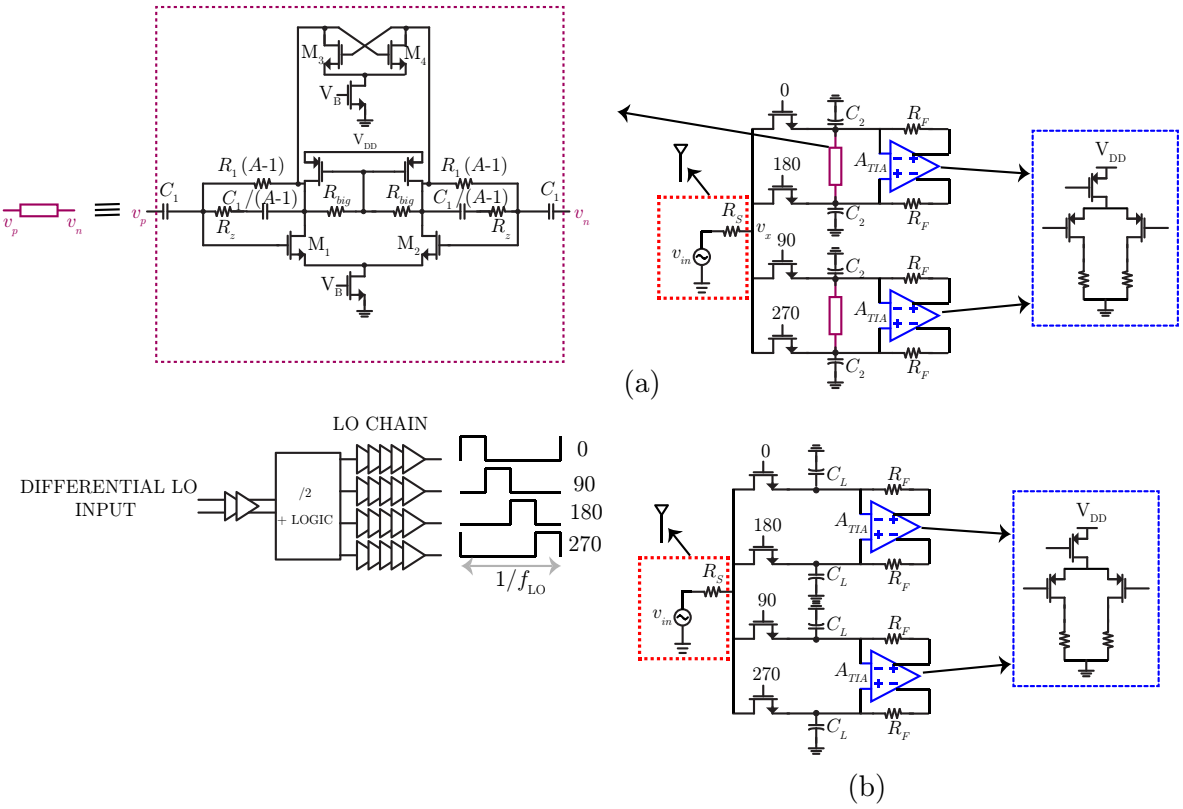


Figure 3.8: (a) Block diagram summarizing the entire receiver front-end with "second-order" N-path filter, and the LO chain. (b) Receiver front-end with conventional N-path filter.

3.3.3 Simulated Performance and Comparison with Conventional N-Path Filters

Fig. 3.8 summarizes the architecture and circuit details of the proposed receiver. Fig. 3.8(a) shows our architecture, an N-path filter driving an impedance with 40dB/decade roll-off. Fig. 3.8(b) shows the architecture of the conventional N-path filter against which our architecture is compared in this subsection. For all comparisons made in this subsection and subsequent portions of this chapter, the same switch size of 150μm/30nm (corresponding to a switch ON resistance of 1.5Ω) were used for both the conventional N-path filter and the enhanced N-path filter. Additionally, to ensure a fair comparison, the capacitance load for the conventional N-path filter was chosen such that a baseband bandwidth of 10MHz was achieved in both the cases. Finally, the resistive portion of the input match was done using the same TIA and the same feedback resistance R_F (Fig. 3.3) in both cases, to ensure uniformity in comparison.

Fig. 3.9 compares the simulated small-signal transfer function of an N-path filter driving an impedance with 40dB/decade roll-off and a conventional N-path filter. It shows the

transfer function both to the RF input node v_x (as marked in Fig. 3.2(a)) and to the baseband output node. As emphasized in the introduction, one of the main aims of this work is to achieve a higher order roll-off at the RF input, so that interferers are rejected right at the front end. The small signal transfer function v_x/v_{RF} shows a 40dB/decade roll-off in case of the enhanced N-path filter, as opposed to a 20dB/decade roll-off in the normal N-path filter. However, a main limitation may be noted from the plot in Fig. 3.9. The far-out rejection (at 200MHz offset) at the node v_x is similar in both the cases. This occurs because the far-out attenuation is eventually limited by the mixer switch resistance, and is given by $R_{SW}/(R_{SW}+R_S)$. There is a slight asymmetry around f_{LO} in the transfer function to the node v_x (Fig. 3.9). This asymmetry is due to the parasitic capacitance of the mixer switches, and may be corrected with complex feedback resistors around the TIA [19, 28].

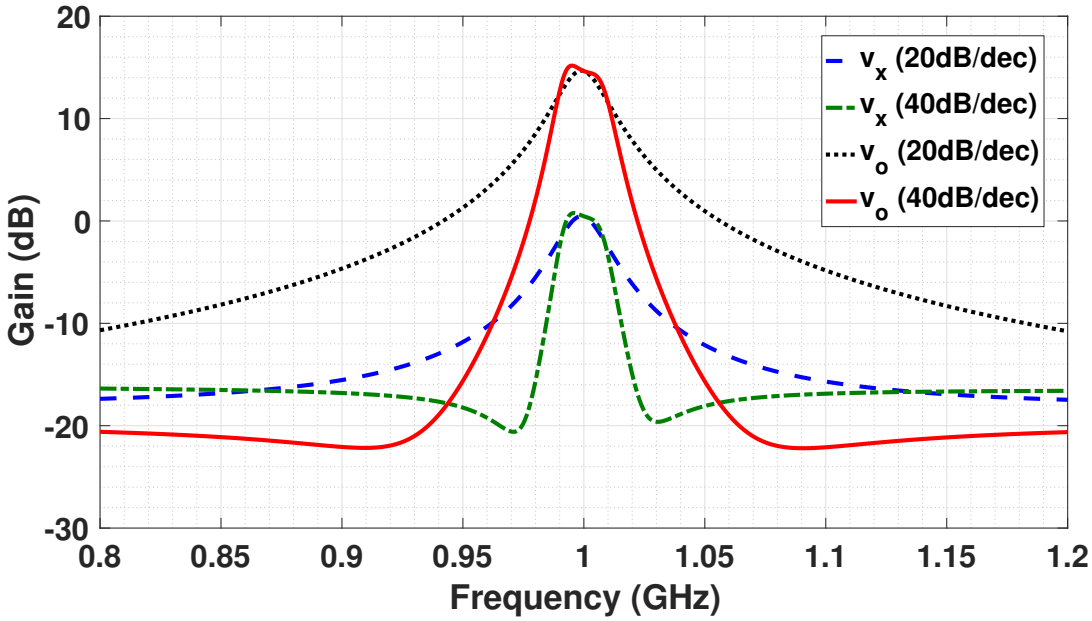


Figure 3.9: Small-signal PAC transfer function to node v_x (see Fig. 3.8(a)) and PXF transfer function to the output for conventional N-path filter and enhanced N-path filter.

Fig. 3.10 shows that the benefits of enhanced N-path filters are not restricted only to small-signal filtering. Fig. 3.10 shows the simulated blocker P1dB (or B1dB) as a function of tone offset frequency. At the edge of the band (10MHz offset), it is seen that both topologies have similar blocker performance. However, for close-in out-of-band blockers, the enhanced N-path filter shows a $4-5$dB higher blocker power tolerance while compared to conventional N-path filters. It may be noted that for very far-out blockers (200MHz offset), the B1dB performance of the conventional N-path filter starts approaching that of the enhanced N-path filter, with the eventual limitation due to the size of the mixer switches.

Fig. 3.11 compares the simulated IIP3 and IIP3 enhancement compared to band-edge (10MHz) as a function of tone-offset frequency (IM3 at 500kHz). While the enhanced N-path filter shows a marked improvement ($6-7$dB) over its conventional counterpart in the IIP3 enhancement compared to band-edge, the improvement is less marked in the absolute value of IIP3. This is because the IIP3 at the edge of the band (10MHz) is slightly less for the enhanced N-path filter than a conventional N-path filter. A detailed explanation of this is provided in the following subsection.s

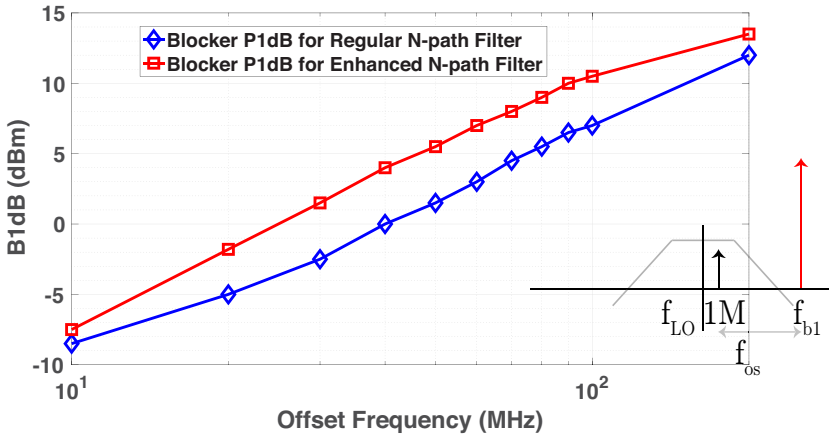


Figure 3.10: Simulated blocker P1dB as a function of tone offset frequency f_{OS} for conventional N-path filter and enhanced N-path filter.

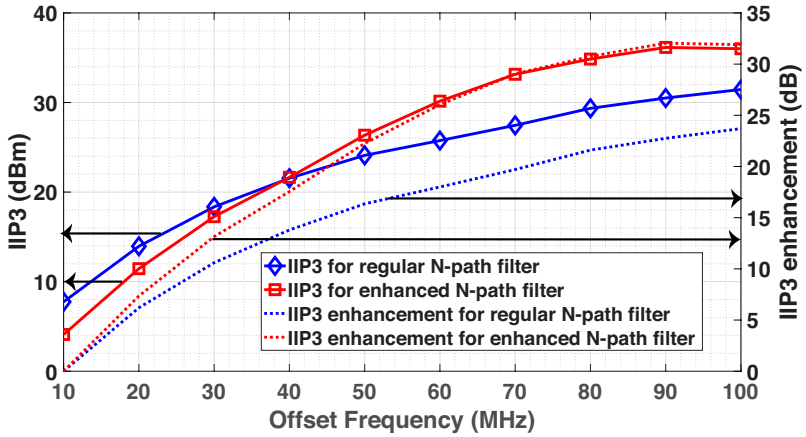


Figure 3.11: Simulated out-of-band IIP3 as a function of tone offset frequency f_{OS} for conventional N-path filter and enhanced N-path filter.

3.3.4 Impact on Noise and Non-Linearity

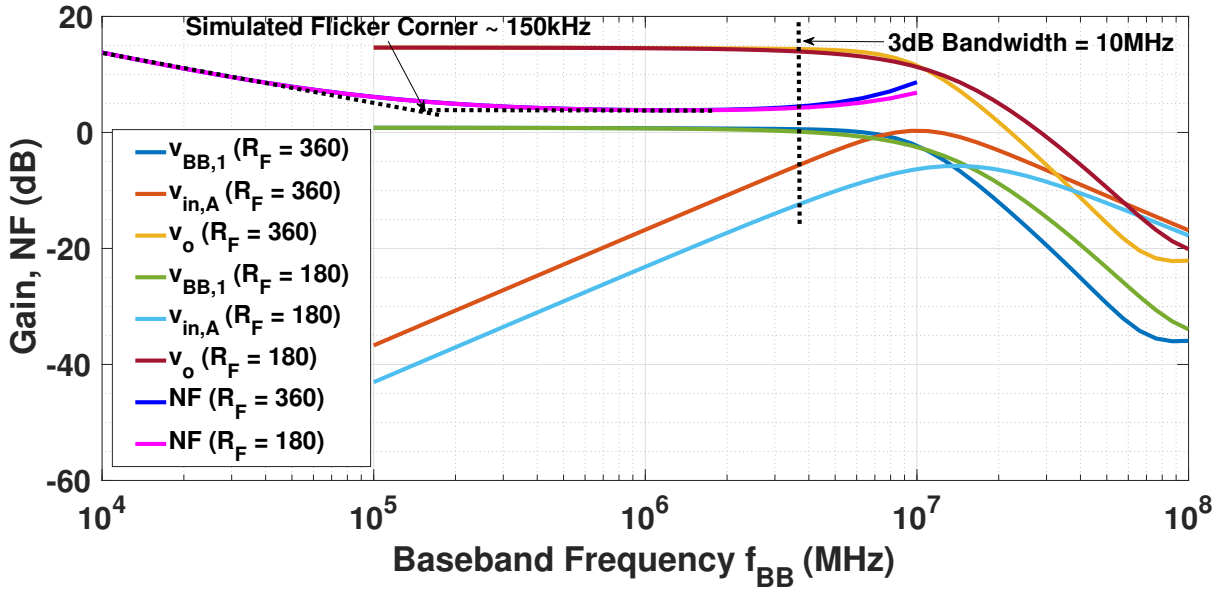


Figure 3.12: Translated transfer function from input at RF to baseband node $v_{BB,1}$, input of the Z-synthesizing amplifier $v_{in,A}$, the output node v_o and the noise figure. $R_F = 360\Omega$ corresponds to $Q = 1/\sqrt{2}$, $R_F = 180\Omega$ corresponds to $Q = 1/2$

.

This subsection explains in detail, the effects of the amplifiers used to synthesize the Z with 40dB/dec. roll-off, on both the noise and non-linearity of the circuit. The effect of mixer switches, TIA and the feedback resistance R_F on the noise figure of the circuit are well studied in [19] and other works. To study the noise of the Z-synthesizing amplifiers, consider the simplified model shown in Fig. 3.3. The noise of the entire negative RC circuit is modeled as a single current source. A more detailed model may be used, but this suffices to get some insights. Now, consider $Z_{BB}(s)$ from Fig. 3.3 placed in the LTI model in Fig. 3.2. The transfer function from the noise source i_n to the output v_o is given by

$$\left|\frac{v_o}{i_n}(s)\right| = \frac{R_F - \frac{R_S}{\gamma}}{2} \frac{sC_1R_1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{3.11}$$

This function is band-pass, which may also be noted from the observation that the noise source i_n is capacitively coupled to the node v_x. Therefore, this noise source has no effect on the noise figure deep in the band of interest. However, due to a high-pass corner close to the 3-dB bandwidth of the circuit, the noise figure starts degrading near the edge of the band, as seen from the plot in Fig.3.12.

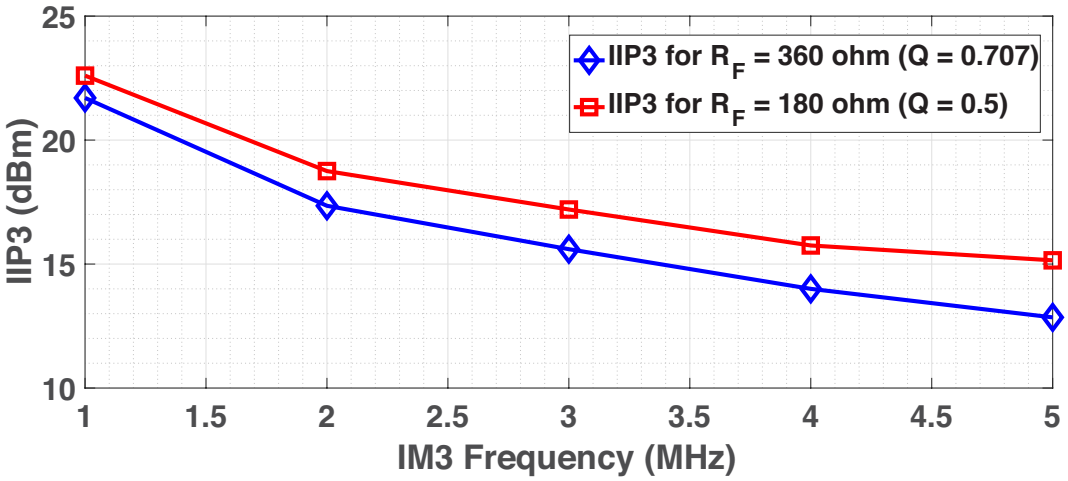


Figure 3.13: Simulated out-of-band IIP3 at a tone offset of 50MHz as a function of the IM3 product frequency (MHz). The 2 plots are for the cases of a filter with $Q = 1/2$ and $Q = 1/\sqrt{2}$.

Now, consider the transfer function from the input of the circuit to the input of the amplifier A used to synthesize the negative RC impedance. As seen from Fig. 3.12, this function has a band-pass nature too, with a high-pass corner close to the 3-dB bandwidth of the circuit. The corresponding peaking in the response close to the 3-dB bandwidth leads to the slightly worse IIP3 performance for blockers at the band-edge as seen in the previous subsection. Now, consider the scenario for out-of-band IIP3, where 2 tones are placed at frequencies $f_{LO} + f_{IM3,IB} + f_{OS}$ and $f_{LO} + f_{IM3,IB} + 2f_{OS}$, such that the IM3 product falls in-band at the frequency $f_{LO} + f_{IM3,IB}$. The previous discussion on the transfer function implies that the IM3, and consequently out-of-band IIP3, depends on $f_{IM3,IB}$, the frequency at which the IM3 product falls in-band. This is indeed verified by simulation in Fig. 3.13, which shows that the IIP3 becomes worse when the IM3 product falls closer to the edge of the band. Finally, it may also be noted that if a transfer function with a gentler roll-off is synthesized ($Q = 1/2$), the transfer function from the input of the circuit to the input of the amplifier A used to synthesize the negative RC impedance, has a smaller peaking compared to the case of a transfer function with steeper roll-off ($Q = 1/\sqrt{2}$). Therefore, while the selectivity is definitely better for transfer functions with higher Q, the linearity across the band is better for transfer functions with lower Q. This trade-off of noise and non-linearity versus Q closely resembles what is seen in active filters like the one in [57].

3.3.5 Pre-Amplifier for Power Savings

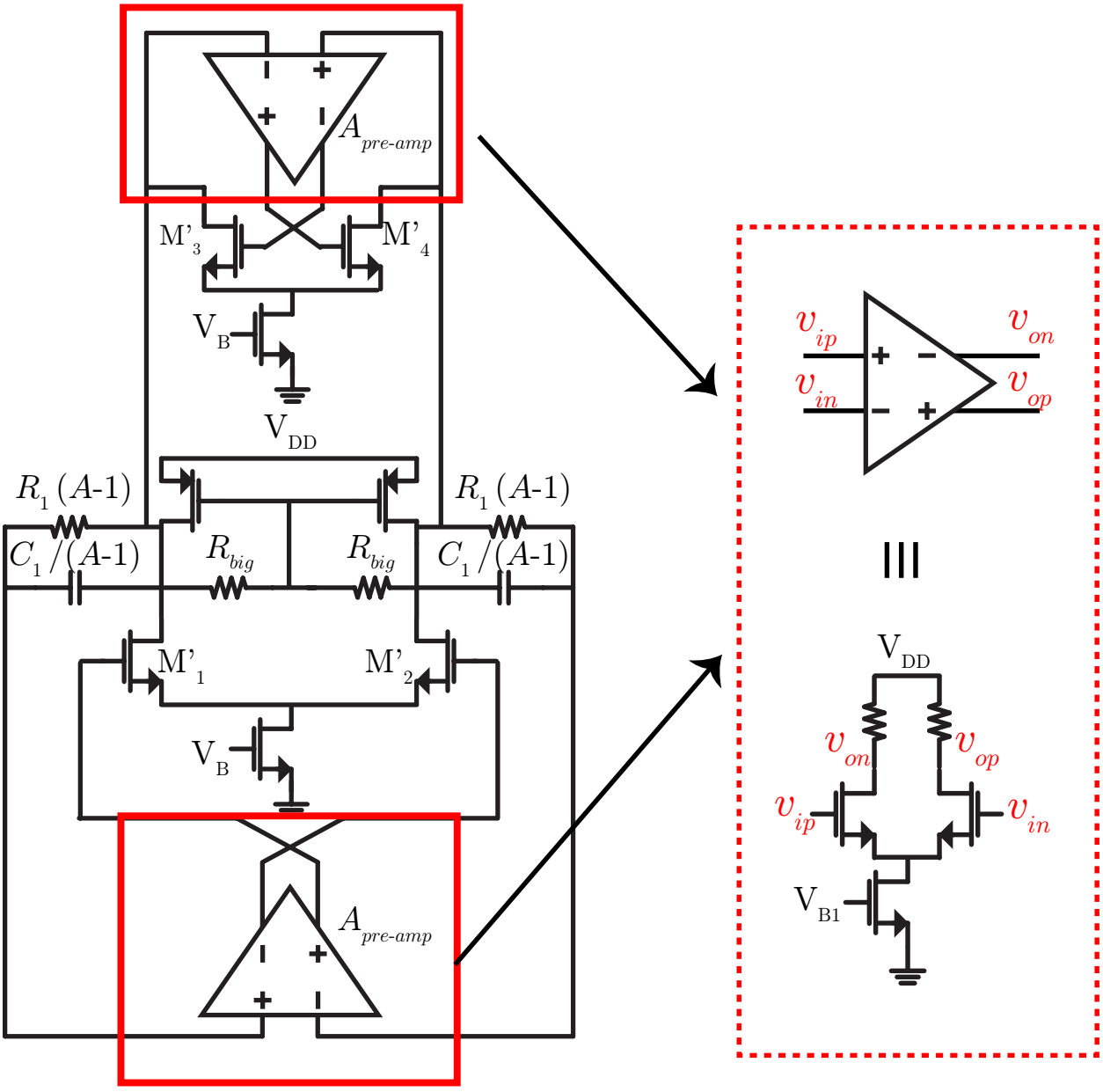


Figure 3.14: Z synthesized with lower power using a pre-amplifier.

It was seen in Fig. 3.5 that a resistor and capacitor were connected in positive feedback around an amplifier of gain $A = g_{m1,2}/g_{m3,4}$. Now, if a pre-amplifier of gain $A_{pre,amp}$ is placed ahead of both the input trans-conductance $g'_{m1,2}$ and the cross-coupled pair $g'_{m3,4}$ (as shown in Fig. 3.14), the resistor and capacitor are now in positive feedback around a

2-stage amplifier of gain $A' = A_{pre,amp}g'_{m1,2}/A_{pre,amp}g'_{m3,4}$. To maintain the same small-signal transfer function and the same location of zeros as in the circuit in Fig. 3.5, the same gain and the same effective output resistance must be maintained. That is,

$$\begin{aligned} g_{m1,2} &= A_{pre,amp}g'_{m1,2} \\ g_{m3,4} &= A_{pre,amp}g'_{m3,4} \end{aligned} \tag{3.12}$$

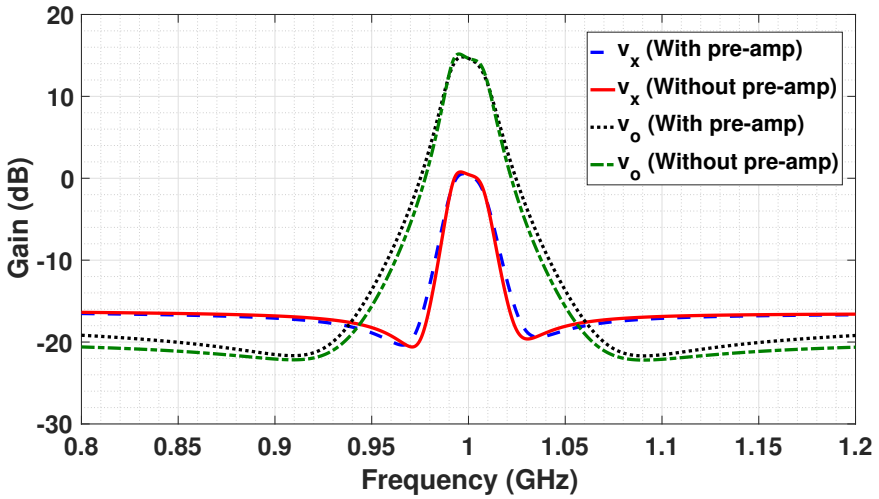


Figure 3.15: Small-signal PAC transfer function to node v_x and PXF transfer function to the output for enhanced N-path filter with and without pre-amplifier.

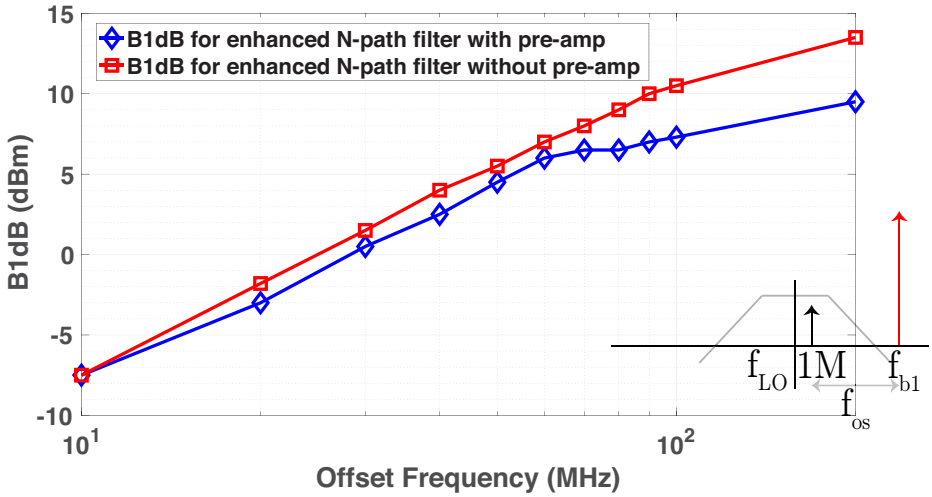


Figure 3.16: Simulated B1dB v/s tone offset frequency f_{OS} for enhanced N-path filter with and without pre-amp.

In other words, both the input and the cross-coupled trans-conductance, and consequently the power consumption of the circuit in Fig. 3.5 is reduced by a factor $A_{pre,amp}$. The pre-amplifier, of course, introduces an additional pole and zero in the transfer function. But these are quite far-out, and hence their effects in the band of the interest may be neglected. The pre-amplifiers also consume power, but the total power consumption is still reduced compared to the circuit in Fig. 3.5. The introduction of another amplifier obviously hurts the non-linearity, but the degradation in non-linearity is much less for a pre-amplifier added in the shunt path of the synthesized Z , than when added to the main signal chain. This may be explained by the high-pass transfer characteristic of the non-linearity of the Z-synthesizing amplifiers, described earlier. For this design, a pre-amplifier gain of $A_{pre,amp} = 5.6$ was chosen. Fig. 3.15 shows that with careful design, the small-signal transfer function may be maintained similar to the case without a pre-amplifier. However, as seen from Fig. 3.16, the reduction in power by using a pre-amplifier, comes at the cost of large signal linearity.

3.4 Measurement and Comparison

A test chip was fabricated in 28nm bulk CMOS process (Fig. 3.17), and was wire-bonded directly onto a PCB. Two sub-chips were fabricated, one to prove the concept without the pre-amplifier (Fig. 3.17(b)), and another to reduce power consumption using a pre-amplifier (Fig. 3.17(a)). A common differential LO input was shared between the two sub-chips. The chip without the pre-amp occupied an area of $730\mu\text{m} \times 650\mu\text{m}$, and the chip with the pre-amp occupied a slightly higher area of $730\mu\text{m} \times 800\mu\text{m}$.

The measured conversion gain and input matching as a function of frequency is shown in Fig. 3.18 ($f_{LO} = 500\text{MHz}$). A gain of around 12.5dB and a bandwidth of 18MHz is achieved. As seen from the zoomed in plot of the gain, the attenuation at 30MHz is $> 20\text{dB}$, illustrating that the higher order roll-off is achieved. Also, Fig. 3.18 shows the ideal Butterworth response with the same gain and bandwidth. It may be observed that the measured baseband response agrees very well with the ideal Butterworth response until the flat region, which indicates the complex zeros discussed in a previous section. This test chip does not implement programmability for resistors and capacitors. Therefore, to compensate for I/Q mismatch, bias tuning was performed. This limitation and LO phase imbalance led to slightly different results for linearity and other measurements from the I/Q channels. For completeness, results from both channels are shown.

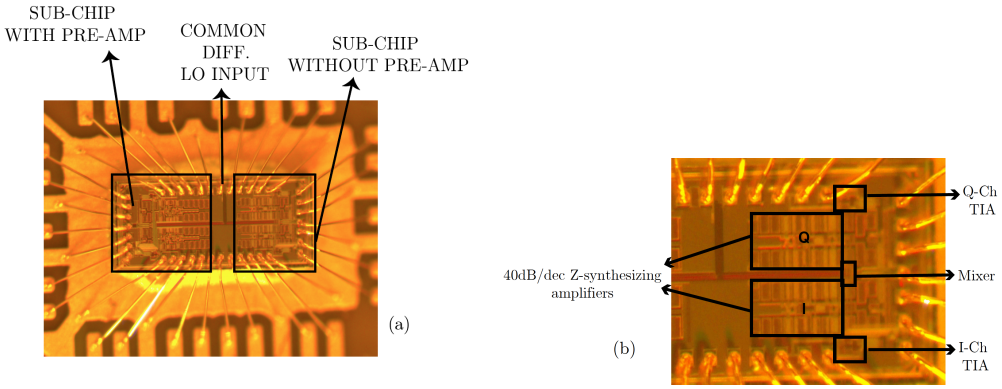


Figure 3.17: (a) Die micro-graph of 2 sub-chip implementations, one with a pre-amplifier, one without. (b) Zoomed in version of die micro-graph of sub-chip without the pre-amplifier.

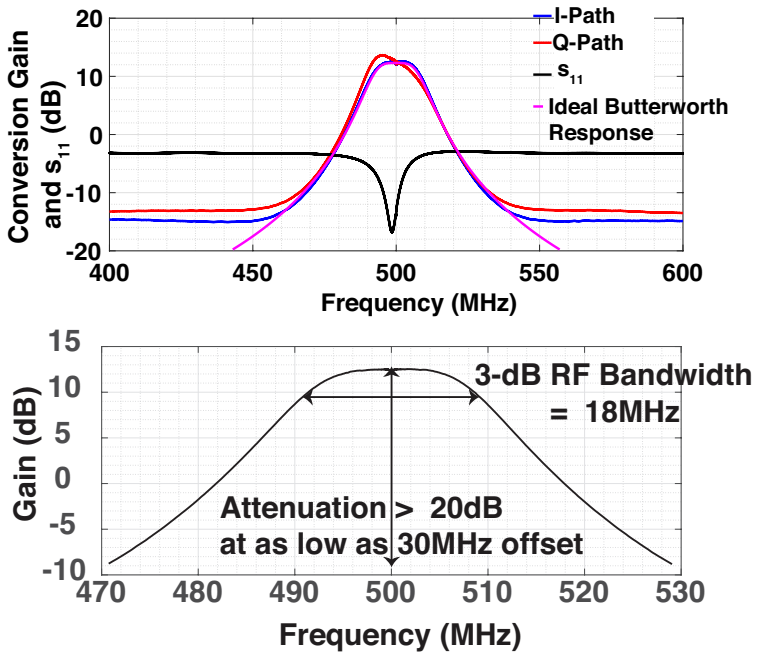


Figure 3.18: Plots of measured s_{11}, gain and zoomed-in gain without the pre-amp (f_{LO} = 500MHz).

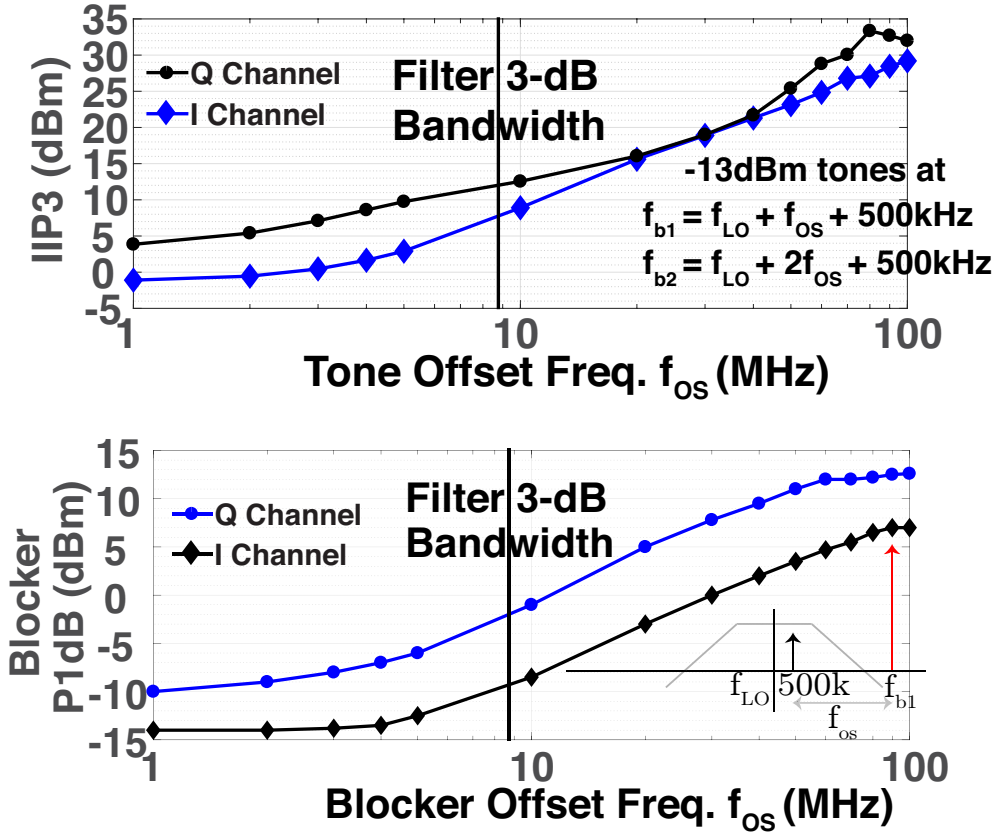


Figure 3.19: Plots of IIP3 and Blocker P-1dB v/s offset frequency, without the pre-amp, as measured from both I and Q channels ($f_{LO} = 500$MHz).

Fig. 3.19 shows the plots of IIP3 and B1dB as a function of tone offset frequency. IIP3 was measured using a 2-tone test where tones (power = -13dBm) were placed at $f_{LO} + f_{OS} +$ 500kHz and $f_{LO} + 2f_{OS} +$ 500kHz, such that their IM3 product fell in-band at $f_{LO} +$ 500kHz. For the blocker P1dB, the desired signal was placed at $f_{LO} +$ 500kHz, and P1dB was found as a function of the blocker offset frequency. A blocker P1dB of +12dBm at $f_{OS} = 60$MHz and IIP3 of +33.3dBm at $f_{OS} = 80$MHz confirm the benefits of the enhanced N-path filters. It may also be noted that these numbers are very close to the simulated values (difference of 2-3dB) in Figs. 3.10 and 3.11, if the I/Q asymmetry is neglected.

The noise of the on-board buffer IC, spectrum analyzer and the PCB losses are de-embedded, while measuring noise figure. A noise figure of around 4.3-5.1dB was measured for f_{LO} from 500MHz to 1.7GHz (Fig. 3.20). A degradation of $\sim$ 2.5dB is observed as f_{LO} is varied from 1.7GHz to 2GHz, as $f_{LO} = 2$GHz is very close to the edge of the divider lock range. The measured noise figure is 0.5-1dB higher than our simulations, and the discrepancy could be coming from 4-phase LO overlap due to imbalances in differential input LO or due to higher parasitics at the RF input. Fig. 3.20 also plots the measured blocker P1dB across

f_{LO} illustrating that linearity is largely unaffected by LO frequency of operation.

Fig. 3.21 illustrates the measured degradation in noise figure as a function of the blocker power. The noise figure in the absence of a blocker, was measured to be 4.4dB, and degrades by 2dB in the presence of a 0dBm blocker. The choice of $f_{LO} = 787.5$MHz and $f_{blk} = 881$MHz was prompted by the availability of high quality filters for the $2f_{LO}$ signal at 1.575GHz and the blocker. High-Q SAW filters were used to filter out the phase noise of the signal generator synthesizing the $2f_{LO}$ and f_{blk} signals, so that the degradation in noise figure is due to the phase noise of the LO chain on the chip alone. (This was designed to be -170dBc/Hz at 80MHz offset).

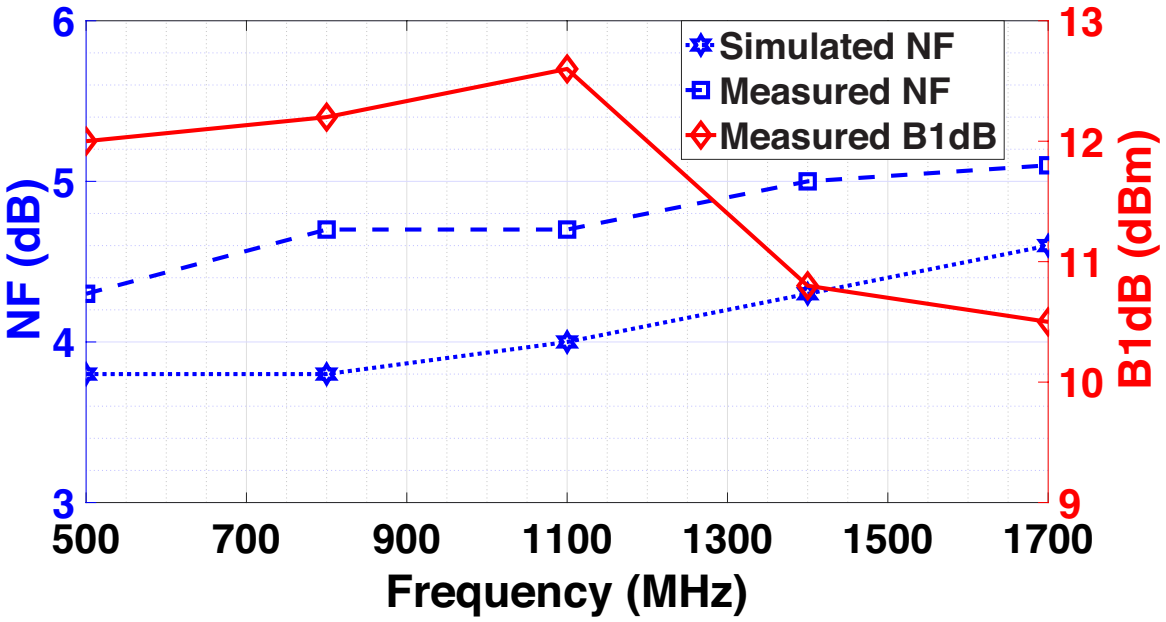


Figure 3.20: Plot of simulated noise figure, measured noise figure and B1dB (at 60MHz offset) v/s LO frequency, without the pre-amp.

Figures 3.22 and 3.23 provide measurement results for the implementation with a pre-amplifier. Fig. 3.22 illustrates the steeper roll-off in small-signal transfer function compared to a conventional N-path filter. Again, the limitation due to the implementation zeros in seen in the flatter region. Fig. 3.23 illustrates that the reduction in power while maintaining a similar shaped transfer function, comes at the cost of large-signal non-linearity (IIP3 and B1dB). Table 3.1 compares the performance metrics of the two enhanced mixer-first topologies, with and without the pre-amplifier, respectively. The power required for the active synthesis of the impedance with 40dB/decade roll-off has been lowered by a factor of 2 using a pre-amplifier. But this comes at the cost of reduced B1dB and IIP3. It is seen that the NF is also marginally higher for the design with the pre-amplifier. However, in simulation,

both versions had the same noise figure. The discrepancy could be due to different parasitics at the RF input of the different sub-chips or different bond-wire inductances.

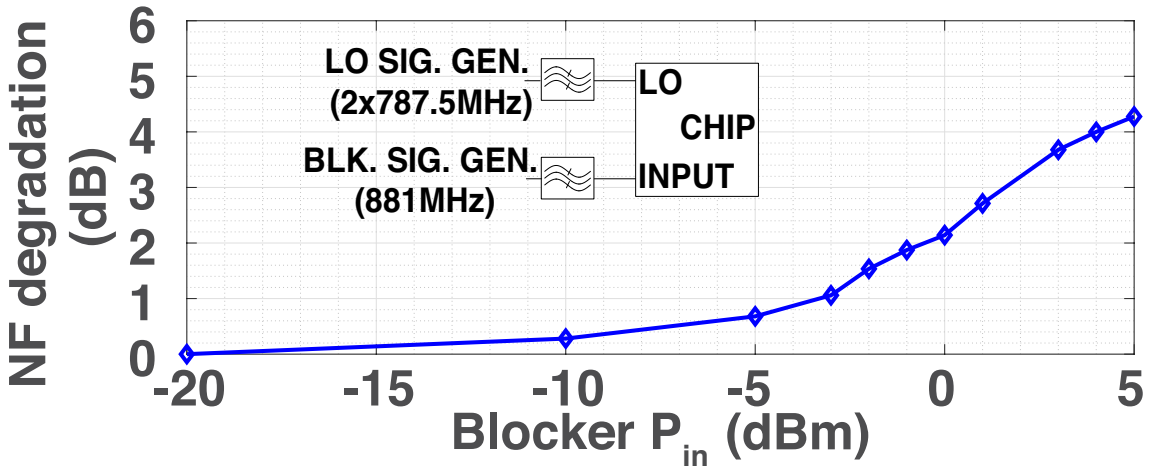


Figure 3.21: Plot of blocker NF degradation v/s blocker P_{in}, without the pre-amp (f_{LO} = 787.5MHz, f_{blk} = 881MHz).

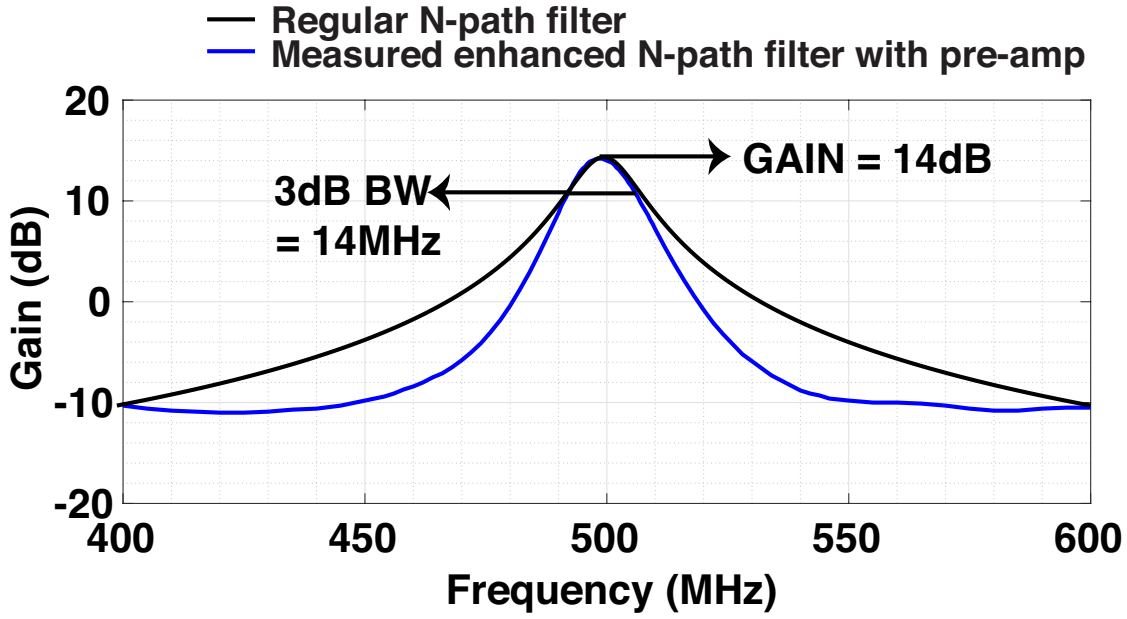


Figure 3.22: Plot of measured gain for implementation with the pre-amplifier.

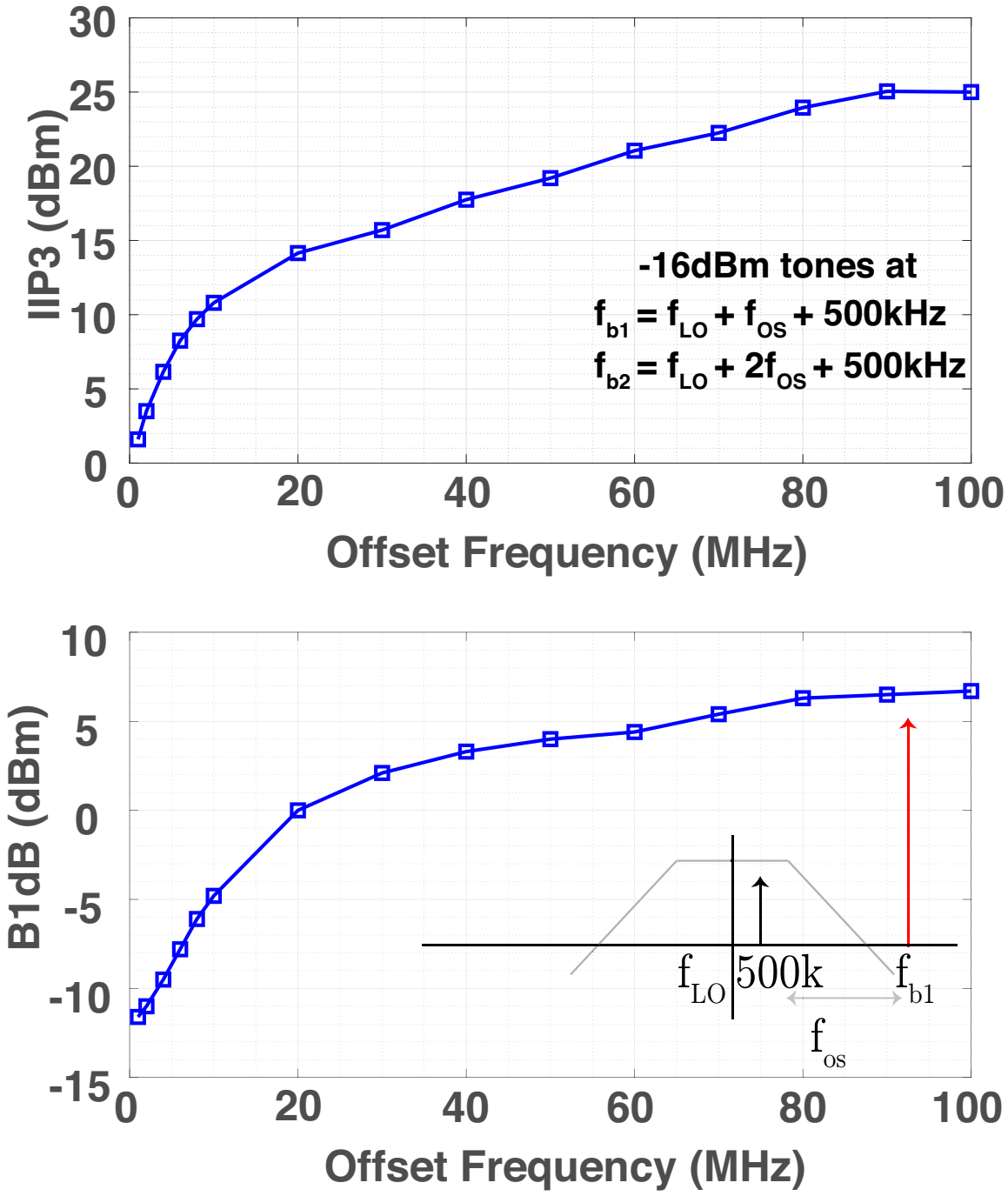


Figure 3.23: Plots of IIP3 and Blocker P-1dB v/s offset frequency for implementation with pre-amplifier (f_{LO} = 500MHz).

Table 3.1: Comparison of implementations with and without Pre-amplifier

Architecture	Without pre-amplifier	With pre-amplifier
Gain (dB)	13	14
Bandwidth (MHz)	18	14
IIP3 (80MHz offset) (dBm)	33.3	24
B1dB (80MHz offset) (dBm)	12	6.3
NF (dB)	4.3	5.2
Power for Z synthesizing amplifiers (mW)	100	50
Area (mm^2)	0.47	0.58

3.5 Comparison and Conclusions

Table 3.2 compares our work against the state-of-the-art mixer first receivers. [13, 46–49] show a 20dB/decade selectivity at the RF input. Our work, with 40dB/decade RF selectivity, exhibits significantly better interference resilience (B1dB and IIP3) than all of the above, except for [46], which achieves higher linearity numbers through supply boosting (to 2V). While [28, 54] implement impedances with 40dB/decade roll-off at baseband, [29] implements higher-order passive N-path filtering. Our work clearly exhibits higher blocker resilience than [54]. While [28, 29] exhibit better IIP3 and B1dB numbers than our work, [28] uses a differential input with a $1:\sqrt{2}$ off-chip balun at the input, and consequently derives a 3dB benefit in linearity metrics. Also, the parasitic capacitance of the capacitor used in each path of the N-path filter in [29] degrades the noise figure significantly at frequencies greater than 1GHz. Additionally, the implementation of the impedance with 40dB/decade roll-off, in both [28, 54], have a tightly coupled trade-off with respect to the location of the poles and zeros in the transfer function, limiting the range of frequencies for which 40dB/decade roll-off is obtained. Whereas, the solution proposed by us breaks this trade-off at the expense of power.

To summarize, this work presents a novel idea for a higher order enhanced N-path filter by providing a detailed synthesis of an impedance which rolls off at 40dB/decade. The trade-off between implementation zeros and power is detailed, and techniques to loosen the same, are proposed. It is found that the enhanced N-path filter helps improve both small-signal filtering and large signal blocker resilience, as compared to a conventional N-path filter. Additionally, some of the limitations of the topology are discussed in detail. Finally, a lower power version of Z-synthesizing amplifiers is proposed, where small-signal filtering is maintained, but large-signal linearity is traded off for power. The measurement results of this work are provided and it is seen that this work achieves highly competitive performance with respect to the state-of-the-art (Table 3.2), in blocker resilience, particularly, blocker P1dB, OOB IIP3 and 0dBm blocker noise figure desensitization.

Table 3.2: Comparison with State-of-Art

	JSSC10 [13]	JSSC12 [47]	JSSC13 [48]	JSSC15 [49]	JSSC2019 [29]	TMTT2016 [46]	JSSC18 [28]	RFIC18 [54]	**This work**
Architecture	Mixer-First	Frequency Translation Noise Canceling	Active N-path Filter	LNTA + Passive Mixer + Baseband notches	Bot. Plate Mixing in N-path filter	N-path BPF/BRF Feedback Filter	N-path Filter with positive cap. feedback	N-path filter with shunting notch	**N-path filter driving Z w/ 40dB/dec. roll-off**
Technology	65nm	40nm	65nm	65nm	28nm	32nm SOI	45nm SOI	130nm SiGe BiCMOS	**28nm**
f_{RF} (GHz)	0.1-2.4	0.08-2.7	0.1-1.2	0.5-3	0.1-2	0.4-6	0.2-8	2-11	**0.2-2**
RF Input	Single Ended	Single Ended	Differential	Differential	Differential	Differential	Differential	Single Ended	**Single Ended**
Gain(dB)	40-70	72	25	50	16	11	21	10-24	**13**
Bandwidth	20MHz	4MHz	8MHz	2-60MHz	13MHz	15MHz	20MHz	80-260MHz	**18MHz**
OOB-IIP3 (f_{OS}/BW)	25dBm (5)	13.5dBm (20)	26dBm (6.3)	-4.8dBm (4)	44dBm (6.3)	36dBm (3.3)	39dBm (4)	20dBm (1.75)	**33.3dBm (4.4)**
B1dB (f_{OS}/BW)	5dBm (5)	-2dBm (20)	7dBm (6.3)	-4dBm (4)	13dBm (6.3)	17dBm (6.7)	12dBm (4)	1.8dBm (1.75)	**12dBm (3.3)**
NF (dB)	4 ± 1	1.9	2.8	3.8-4.7	4.1-10.3	3.6-4.9	2.3-5.4	11 ± 1	**4.3-7.6**
0dBm Blocker NF (dB)	NA	4.1 (f_{OS}/BW = 20)	NA	NA	6.9 (f_{OS}/BW = 6.1)	NA	4.7 (f_{OS}/BW=4)	NA	**6.4** (f_{OS}/BW=5)
Power (mW)	37-70	35.1-78	18-57.4	Rx:76-168 LO:54-194	38-96	81-209	50 + 30/GHz	Rx:656 LO:1466 - 1494	**Active Z:100 TIA:43 LO:3.6-36**
Supply (V)	1.2/2.5	1.3	1.2	1.2/2.5	1.2/1	2	1.2	4.5/2.5	**1.2**
Area (mm^2)	2.5	1.2	0.27	7.8	0.49	0.28	0.8	3.4/5	**0.48**

Chapter 4

N-Path Filters with 60dB/decade RF selectivity

4.1 Introduction

As seen in the previous chapters, an ever increasing number of bands with the advent of sub-6GHz 5G calls for high linearity receiver front-ends, with extremely high tolerance for blockers, both in close-in channels and far-out channels. The impedance translation property of N-path filters helps to realize tunable band-pass filters, a very desirable property for SAW-less receivers. Various attempts were made to improve the noise, selectivity and linearity [29, 46–49] of N-path filter-based receiver front-ends. While techniques like cascade of N-path filters, frequency-translational noise canceling, bottom-plate mixing were used in these receivers, most of them had N-path filters driving impedances with 20dB/decade roll-off. More recently, attempts were made to synthesize N-path filters with 40dB/decade RF selectivity [28, 30, 54, 58] to make receiver front-ends with enhanced selectivity and linearity. The previous chapter delves into one such attempt in great detail. While the N-path filter in [59] had a driving point impedance with 40dB/decade roll-off, third-order current mode filtering helped achieve higher selectivity and better tolerance to close-in blockers. In this chapter, we demonstrate a higher order N-path filter which drives an impedance with complex-pole 60dB/decade roll-off for improved selectivity and tolerance to close-in blockers. To the best of our knowledge, this is the first ever synthesis of a driving point impedance with 60dB/decade roll-off. We illustrate impedance-synthesis, from writing out what transfer function is needed for the impedance to finding out a circuit realization of the same, in a step-by-step fashion. A prototype integrated circuit validates this concept.

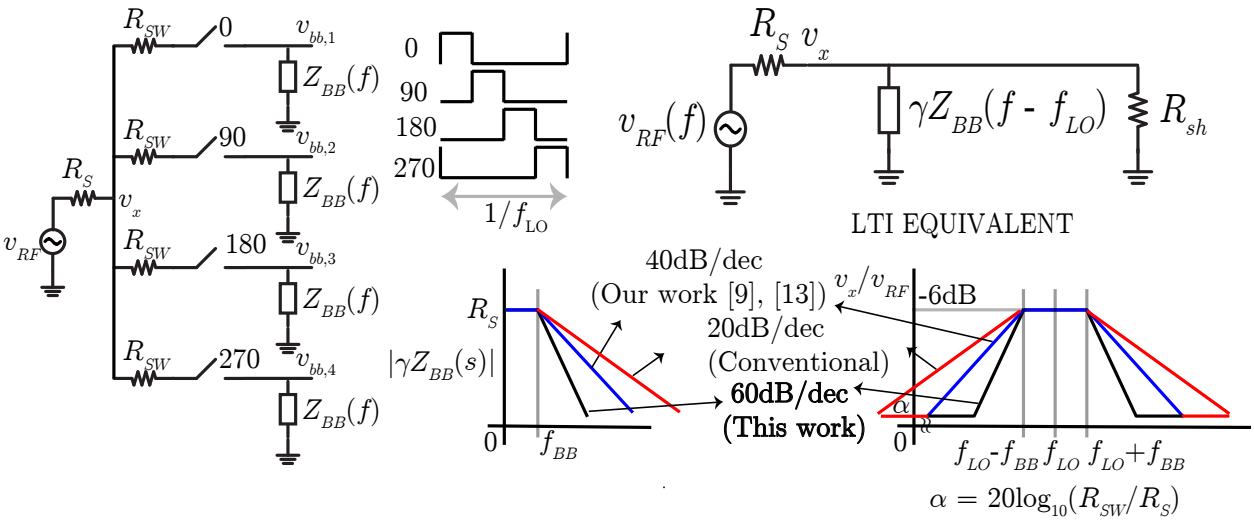


Figure 4.1: LTI equivalent of N-path filters at f_{LO}, illustrating impedance translation in N-path filters.

4.2 Impedance Synthesis

The goal of this work is to achieve improved RF selectivity and blocker tolerance by building an N-path filter which drives an impedance with 60dB/decade roll-off. In the LTI equivalent circuit of this LPTV system (see Fig. 4.1(a)), the transfer function $v_x/v_{RF}(s')$ needs to be of the form

$$\frac{v_x}{v_{RF}}(s') = \frac{1}{2}\frac{1}{1+as+bs^2+cs^3} \tag{4.1}$$

where s' is the frequency translated variable $s - j\omega_{LO}$. The factor of 1/2 comes from the requirement for input matching. To achieve this third order all-pole transfer function, the required impedance $Z_{BB}(s)$ needs to be

$$\gamma Z_{BB}(s) = \frac{R_S}{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2})} \tag{4.2}$$

where $\gamma = 2/\pi^2$ for an N-path filter driven by a four phase non-overlapping square wave LO. The transfer function in (4.1) may be realized using the impedance in (4.2) if,

$$2a = \frac{1}{\omega_1}+\frac{1}{\omega_0 Q} \quad 2b = \frac{1}{\omega_0\omega_1 Q}+\frac{1}{\omega_0^2} \quad 2c = \frac{1}{\omega_0^2\omega_1} \tag{4.3}$$

According to the results of [55], a third-order all-pole impedance like the one described in equation (4.2) is not realizable using passive elements only. This is also true for second-order all-pole impedances. However, active synthesis of impedances with 40dB/dec. roll-off have

been shown previously including in Chapter 3. To the best of our knowledge, there has been no prior work that synthesizes an impedance with 60dB/dec. roll-off. We now try to provide a step-by-step synthesis of the same.

With an appropriate choice of resistor, capacitor and inductor values, the impedance of equation (4.2) may be rewritten as

$$\begin{aligned}\gamma Z_{BB}(s) &= \frac{R_S}{(1+sR_SC_1)\left(1+\frac{sL_1}{R_S}+s^2L_1C_1\right)} \\ &= \frac{R_S}{1+sR_SC_1} - \frac{sL_1}{1+\frac{sL_1}{R_S}+s^2L_1C_1}\end{aligned} \tag{4.4}$$

The partial fraction decomposition in the second line of equation (4.4) is critical to the synthesizing the desired impedance. Clearly, the impedance $Z_{BB}(s)$ is a series combination of two impedances. One of them is a shunt combination of R_S and C_1, and the other is a shunt combination of $-R_S$, $-L_1$ and $-C_1$. By synthesizing an impedance thus derived, it is possible to realize an N-path filter with 60dB/decade RF selectivity. Note that in the impedance $\gamma Z_{BB}(s)$, the real part R_S may be realized as a parallel combination of R_1 and R_2, as shown in Fig. 4.2. This allows for some flexibility in optimizing noise and the transfer function. The noise of the negative resistance $-R_1$, modeled as i_n, has a low-pass transfer function to the node v_x and the output node v_o, thereby degrading the in-band noise of the receiver.

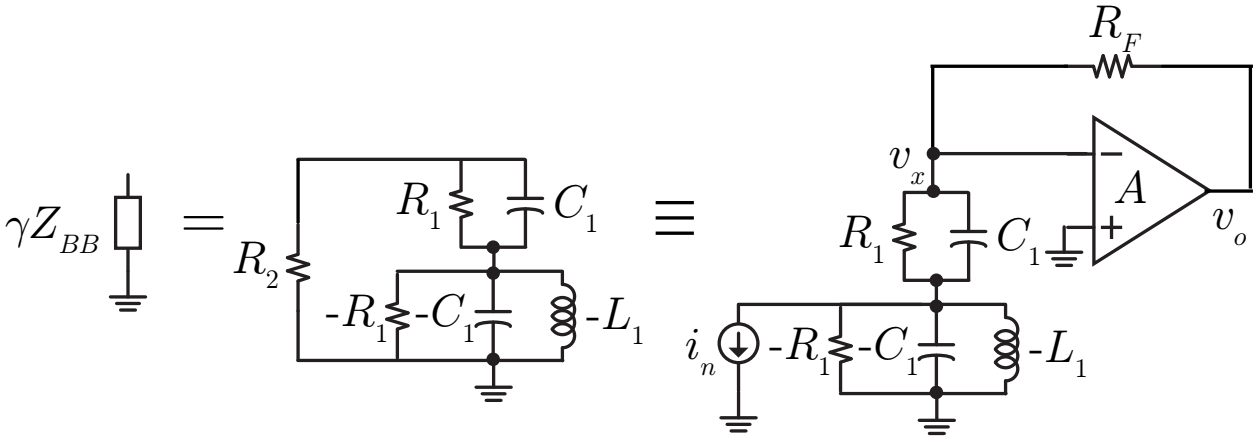


Figure 4.2: Third order driving impedance.

To ensure that the noise of the negative resistance $-R_1$ does not have a DC path to the nodes v_x and v_o, the resistance R_1 of Fig. 4.2 may be replaced by a series combination of R_1 and C_2. The driving point impedance looking into the dashed box of Fig. 4.3 is given by

Z_{C3}

$$Z_{C3} = \frac{1 + \frac{sL_1}{R_1} + sC_2R_1}{s(C_1 + C_2)\left(1 + s\frac{C_1C_2}{C_1+C_2}R_1\right)\left(1 + \frac{sL_1}{R_1} + s^2L_1C_1\right)} \tag{4.5}$$

Z_{C3} is a capacitive impedance with 60dB/decade roll-off at higher frequencies, as opposed to the usual 20dB/decade roll-off of a simple capacitor (see the representative impedance plot in Fig 4.3). Note that an additional shunt capacitance C_S does not change the form of the transfer function [5], but allows for increased flexibility (see Fig 4.3). When R_S is added in shunt for input matching, the driving point impedance looking into node v_x of Fig. 4.3 has four poles and one zero. Consequently, if the impedance shown in Fig. 4.3 is used as the load to the N-path filter in Fig. 4.1, the transfer function $v_x/v_{RF}(s')$ will also have four poles and one zero (see the plot in Fig 4.3). The zero positioned inside the band of interest, leads to an in-band ripple in the desired transfer function. By appropriate choice of components, this in-band ripple may be minimized. With this circuit, the noise contribution of the negative resistance is reduced deep inside the band, but increases at the band-edge, similar to [5]. Also, realizing R_S by using a resistor R_F in feedback around an amplifier (see Fig. 4.3) as opposed to an explicit resistor helps improve noise performance and obtain receiver gain.

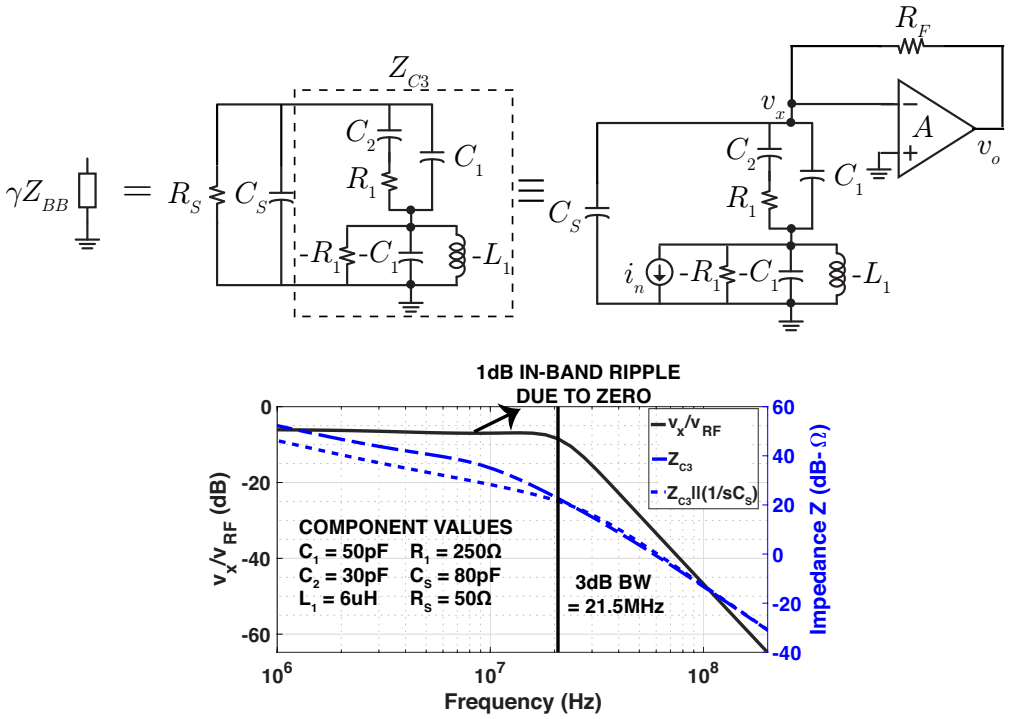


Figure 4.3: Driving point impedance with four poles and one zero. Also, representative simulation plots for the "third" order capacitive impedances and transfer function from v_{RF} to v_x (see Fig. 4.1) are shown for the component values indicated in the figure.

4.3 Circuit Design

Most of the components required to synthesize the impedance $Z_{BB}(s)$ described in Fig. 4.3 are common knowledge. In this section, we focus on the synthesis of the negative impedances, $-R_1$, $-C_1$ and $-L_1$. The negative RC is synthesized using a resistor and capacitor in positive feedback around an amplifier of gain $A = 2$ (see Fig. 4.4(a)), as described in [5]. A detailed analysis of the stability of the circuit is presented in [5]. While a negative RC impedance is desired, the actual implementation shown in Fig. 4.4(a) has undesirable zeros, which can be pushed to a higher frequency by consuming more power in the amplifiers and by using a series resistance R_z.

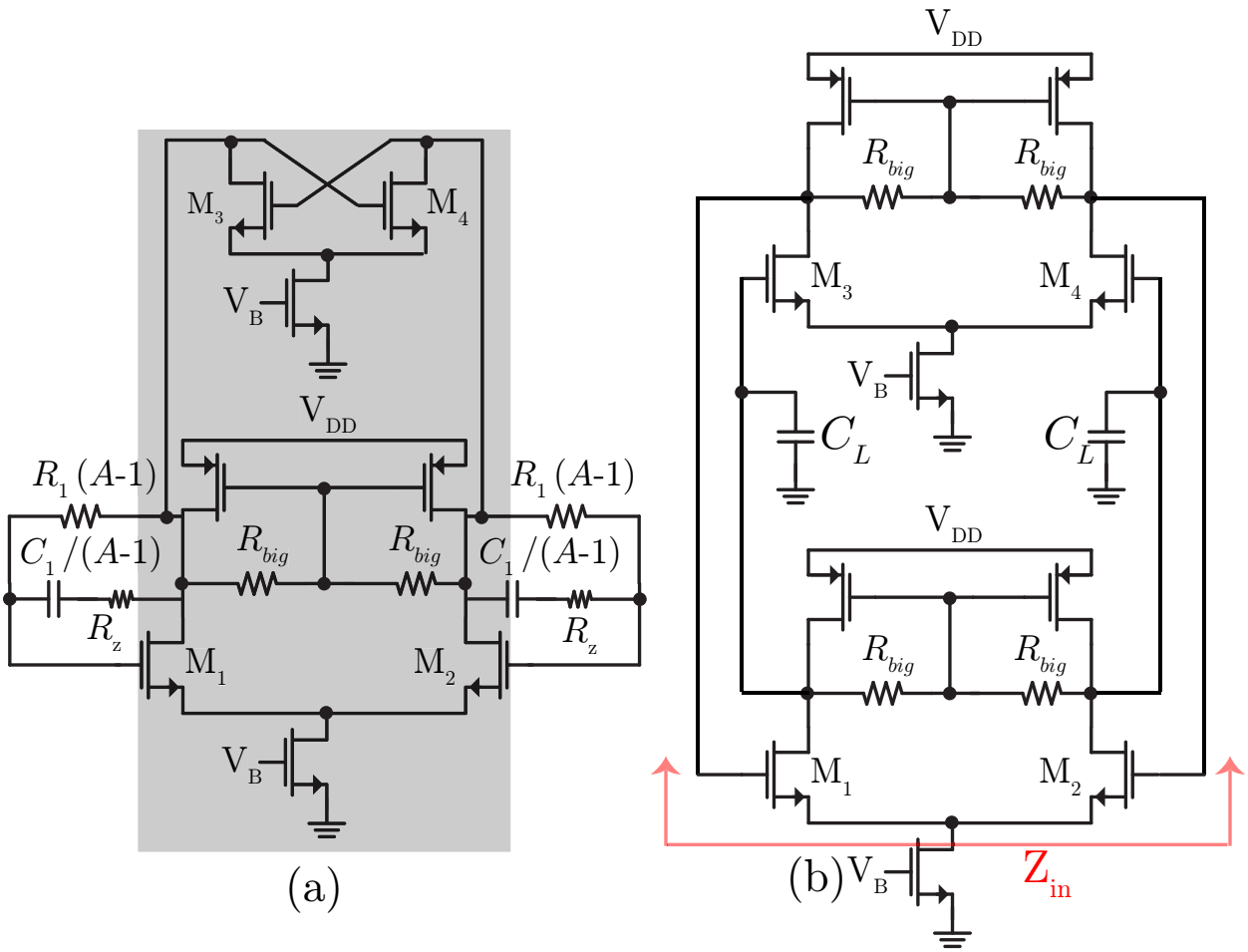


Figure 4.4: (a) Amplifier to realize negative RC. (b) "Negative gyrator" to realize negative inductance.

The negative inductance $-L_1$ of Fig. 4.3 may be realized using a "negative gyrator" as shown in Fig. 4.4(b). Gyrators have been used to synthesize active tunable inductors using

transconductances and capacitors, including in [49]. A positive inductor is realized when there is differential mode negative feedback in the loop, and a negative inductor may be realized using differential mode positive feedback in the loop. Note that in either case, there is common mode positive feedback. However, the loop gain of the common mode positive feedbak is much less than unity due to the tail current source degeneration. The effective negative inductance synthesized is given by

$$-L_{in} = -\frac{C_L}{g_{m1,2}g_{m3,4}} \tag{4.6}$$

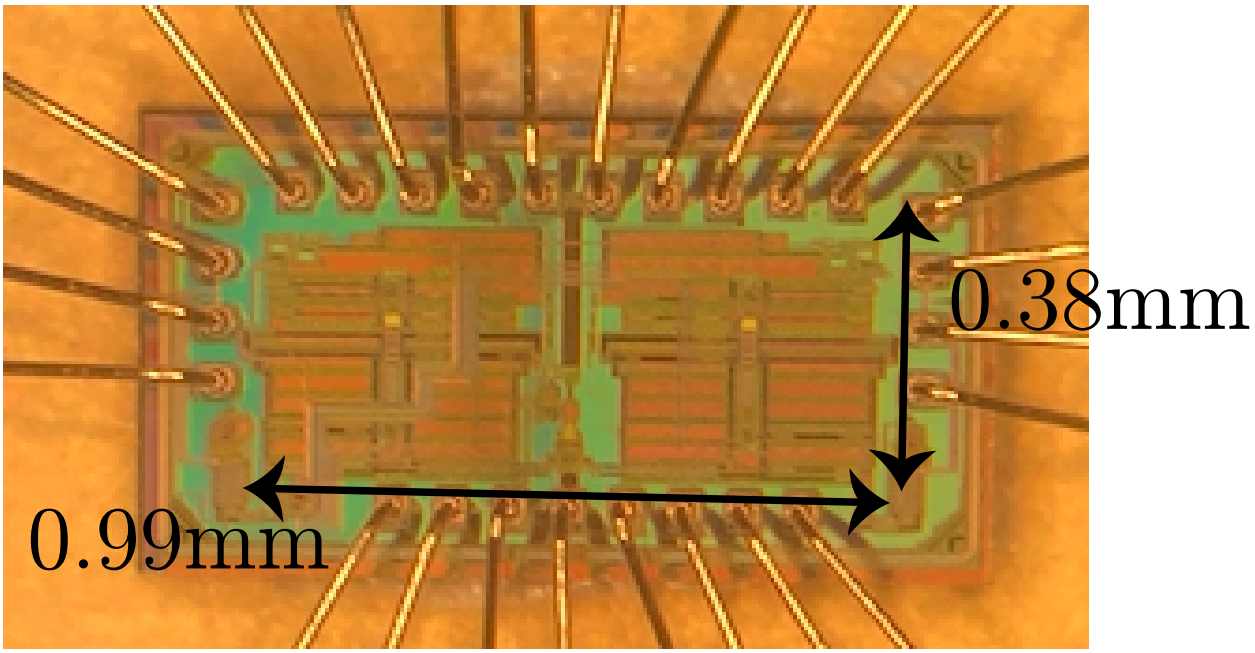


Figure 4.5: Die micrograph.

4.4 Measurement

A test chip was fabricated in 28nm bulk CMOS (see Fig. 4.5) and directly bonded to a PCB. The active area of the chip is 990μm $\times$ 380μm.

The measured conversion gain and input matching as a function of frequency is shown in Fig. 4.6 for three different LO frequencies. A zoomed-in plot of the conversion gain at f_{LO}=1GHz is also shown (Fig. 4.7). A gain of around 15.3dB and a bandwidth of 35MHz is achieved, with a close-in roll-off of 18dB/octave, illustrating third order filtering. The far-out flat region is due to the zeroes in the implementation of the higher order impedance. The

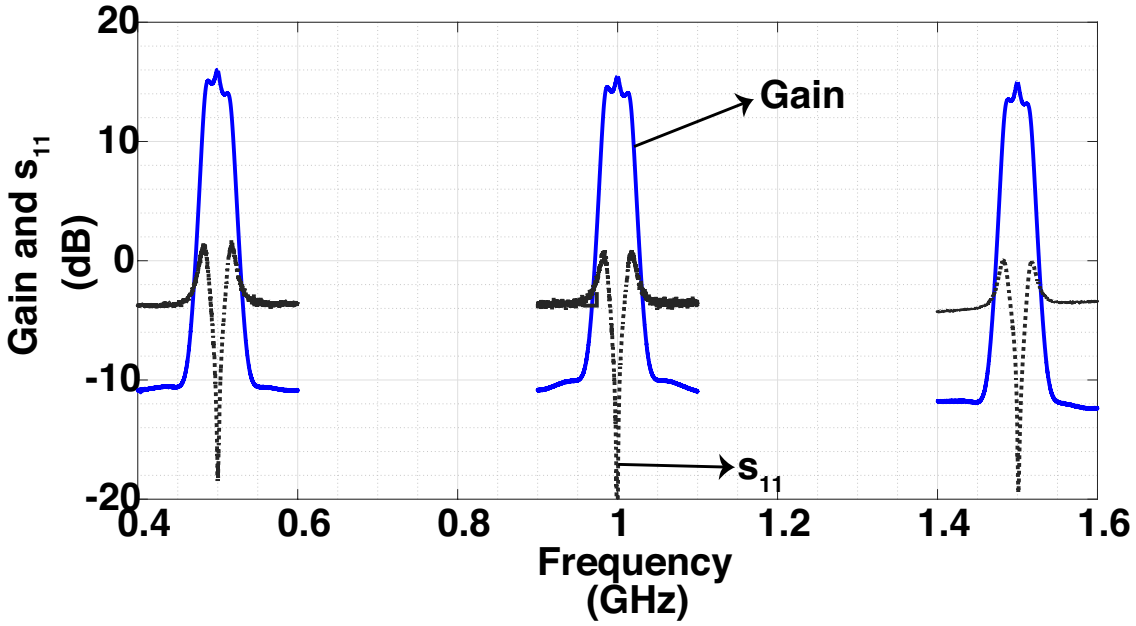


Figure 4.6: Measured s_{11}, gain for three different LO frequencies.

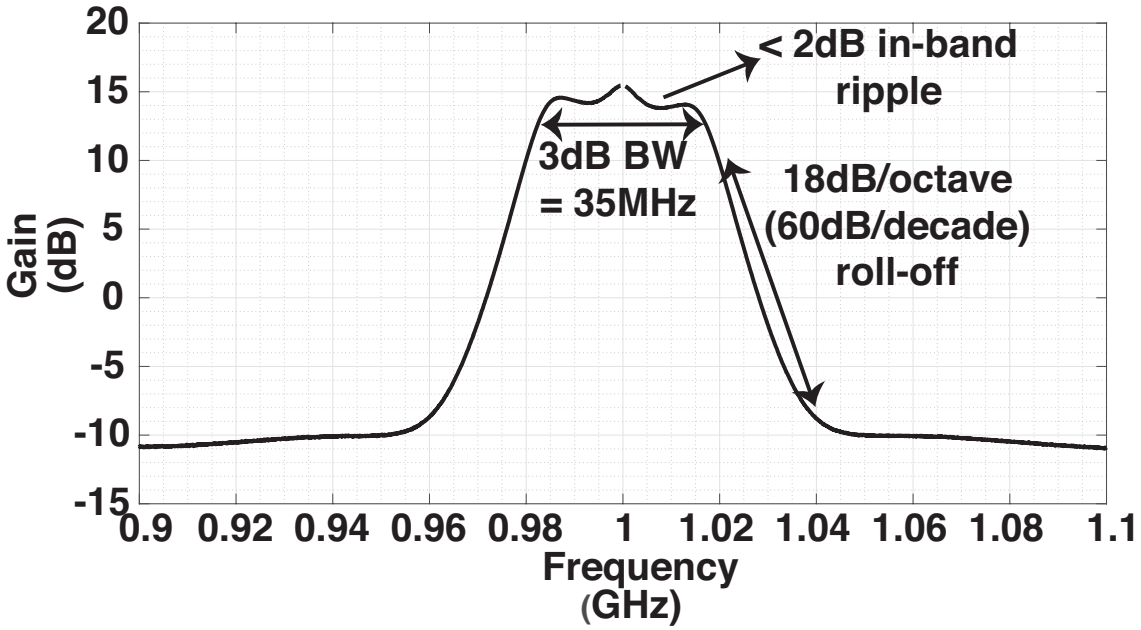


Figure 4.7: Zoomed-in gain for $f_{LO} = 1$GHz.

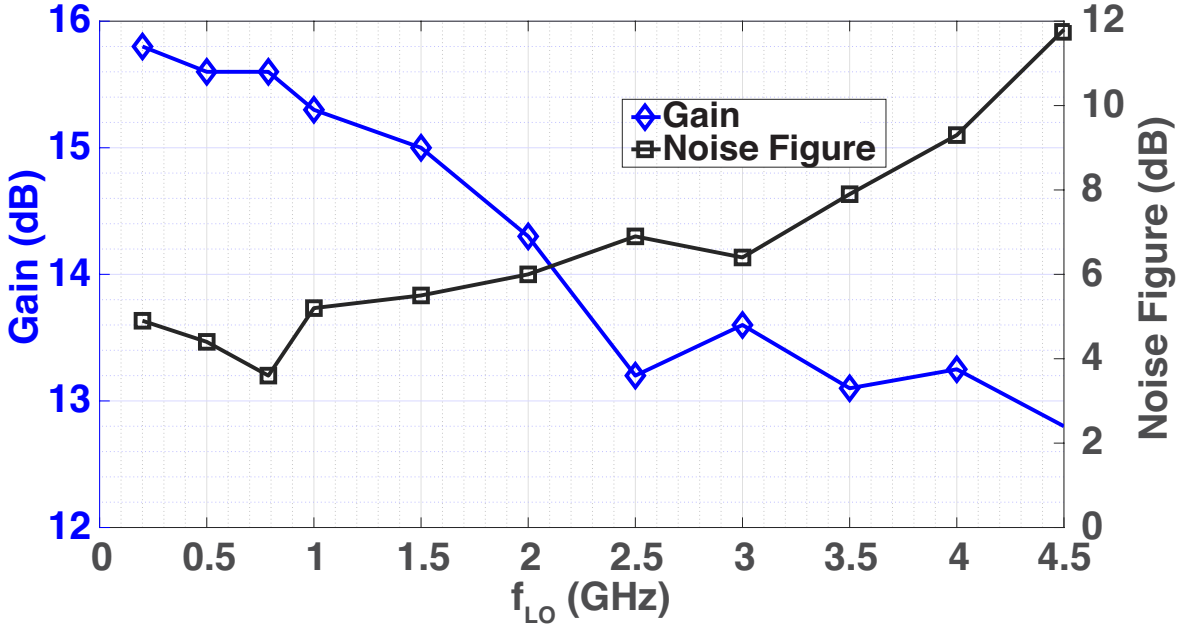


Figure 4.8: Measured gain, NF versus f_{LO}.

measured gain varies from 15.8dB to 12.8dB across the entire range of f_{LO} from 200MHz to 4.5GHz (see Fig. 4.8).

Fig. 4.9 shows the measured plots of IIP3 and blocker-induced 1-dB compression points versus tone offset frequency. IIP3 was measured using a 2-tone test where tones were placed at $f_{LO} + f_{OS} + 1$MHz and $f_{LO} + 2f_{OS} + 1$MHz, such that their IM3 product fell in-band at $f_{LO} + 1$MHz. For the blocker P1dB, the desired signal was placed at 1.001GHz, and B1dB was found as a function of the blocker offset frequency. The far-out IIP3 and B1dB are limited by the mixer switch linearity. A B1dB of +6.3dBm and IIP3 of +20.6dBm at the alternate channel ($f_{OS}/f_{BW} = 2$) confirm the benefits of improved linearity for close-in blockers with an N-path filter driving a third order impedance. A small degradation in IIP3 was also observed as the IM3 frequency moves towards the band-edge (see Fig. 4.10). This effect is very similar to what was observed in [5], and arises due to the high-pass transfer function from the non-linearity generated by the negative RC impedance, to the output.

An in-band noise figure (NF) of 3.6dB − 9.3dB was measured for f_{LO} up to 4GHz (see Fig. 4.8), after de-embedding cable losses and the noise of the spectrum analyzer and off-chip buffers. The degradation at higher LO frequencies is due to the parasitic capacitance of the mixer switches, pads and ESD diodes. Similar to the IIP3, a degradation in NF was also observed towards the band-edge (Fig. 4.10), as described in Section 4.2 and [5]. $f_{LO} = 787.5$MHz was chosen for the blocker NF measurement due to availability of high-Q bandpass filters for the LO input at $2f_{LO}$ and the blocker at 881MHz. The NF degrades from 3.6dB to 6.8dB in the presence of a 0dBm blocker at offset $f_{OS}/f_{BW} = 2.6$ (see Fig.

4.11).

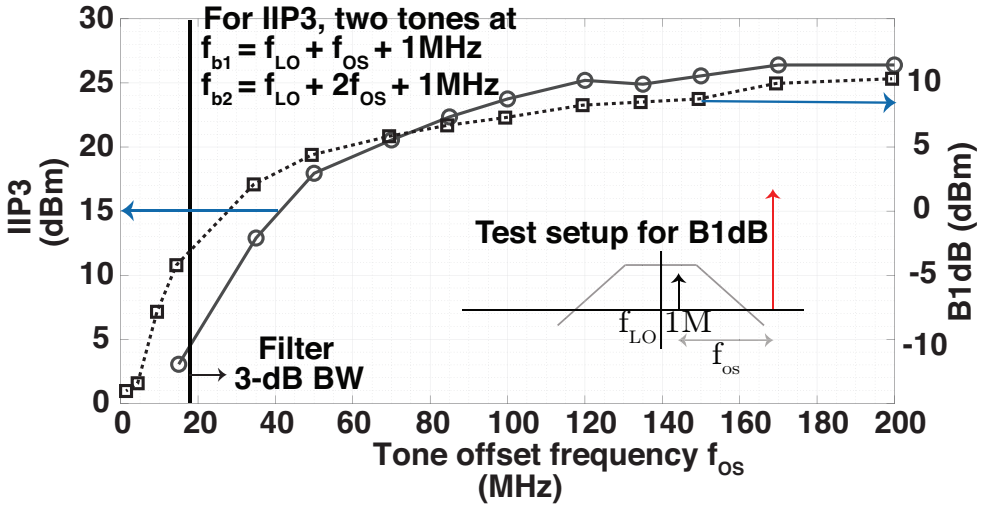


Figure 4.9: Measured IIP3 and B1dB v/s offset frequency for $f_{LO} = 1$GHz.

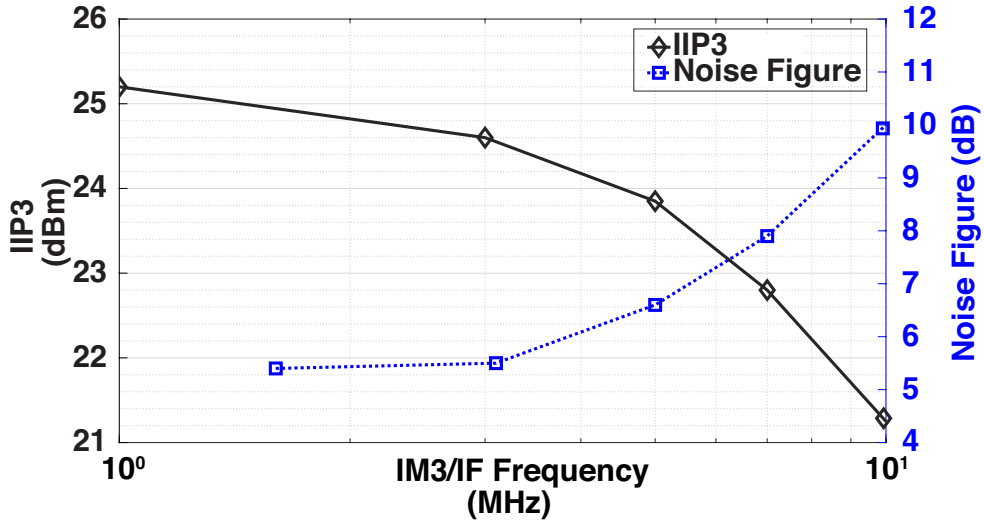


Figure 4.10: Measured out-of-band IIP3 at a tone offset of 120MHz as a function of the IM3 product frequency, and measured NF as a function of IF frequency for $f_{LO} = 1$GHz.

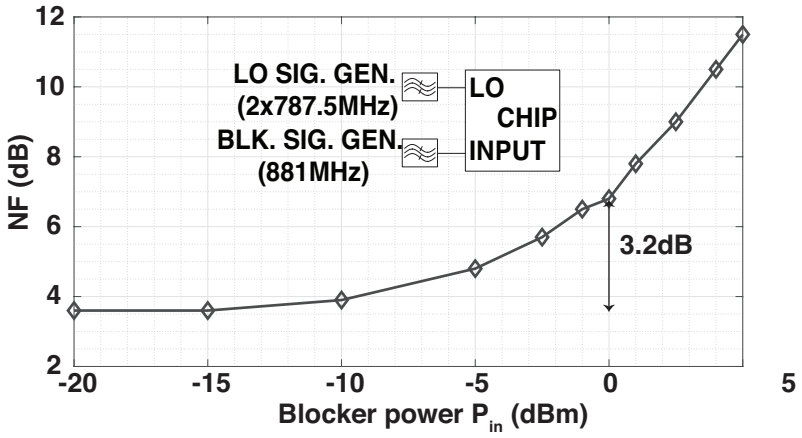


Figure 4.11: Measured in-band blocker noise figure for $f_{LO} = 787.5$MHz.

4.5 Conclusion

In summary, this chapter presents a higher order N-path filter driving an impedance which rolls off at 60dB/decade. It achieves sixth order band-pass filtering with highly competitive performance (Table 4.1) with respect to blocker resilience, particularly, B1dB and OOB IIP3 for close-in blockers. Also, this work provides the first known synthesis of a third order driving point impedance.

Table 4.1: Comparison with State-of-Art

	JSSC13 [48]	JSSC15 [49]	ISSCC17 [29]	JSSC18 [28]	RFIC18 [54]	RFIC 2019 [30]	JSSC 2020 [59]	**This work**
Architecture	Active N-Path Filter	LNTA + NPF + Baseband notches	Bot. Plate Mixing in N-Path Filter	N-Path Filter with positive cap. feedback	N-path filter with shunting notch	N-Path Filter driving Z w/ 40dB/dec. roll-off	N-Path Filter with third order current mode filtering	**N-Path Filter driving Z w/ 60dB/dec. roll-off**
Technology	65nm	65nm	28nm	45nm SOI	130nm SiGe	28nm	28nm	**28nm**
f_{RF} (GHz)	0.1-1.2	0.5-3	0.1-2	0.2-8	2-11	0.2-2	0.5-2	**0.2-4.5**
RF Input	Differential	Differential	Differential	Differential	Single Ended	Single Ended	Differential	**Single Ended**
Gain(dB)	25	50	16	21	10-24	13	32.4	**13-16**
Bandwidth	8MHz	2-60MHz	13MHz	20MHz	80-260MHz	18MHz	260MHz	**35MHz**
RF Selectivity (dB/dec.)	60†	20	40	40	40	40	<40‡	**60**
OOB-IIP3* f_{OS}/BW=2	18dBm	-4.8dBm	32dBm	28dBm	20dBm	22dBm	21dBm	**20.6dBm**
B1dB* f_{OS}/BW=2	-2dBm	-4dBm	5dBm	7.5dBm	2dBm	2/8dBm (I/Q)	-4dBm	**6.3dBm**
NF (dB)	2.8	3.8-4.7	6.3	2.3-5.4 ($0.2-4$GHz)	11 ± 1	4.3-7.6	3-5.5	**3.6-9.3** ($0.2-4$GHz)
Power (mW)	18-57.4	Rx:76-168 LO:54-194	38-96	50 + 30/GHz	Rx:656 LO:1466 - 1494	Active Z:100 TIA:43 LO:3.6-36	Rx:21.6 LO:3.9-15.6	**Active Z:130 TIA:40 LO:4.8-81.6**
Supply (V)	1.2	1.2/2.5	1.2/1	1.2	4.5/2.5	1.2	1.2/1.8	**1.2**
Area (mm^2)	0.27	7.8	0.49	0.8	3.4/5	0.48	0.16	**0.38**

* Alternate channel IIP3 and B1dB values for other works extrapolated from graphs.
† Active cascade of N-path filters.
‡ Third order current-mode baseband filtering, but lower order filtering at baseband input.

Chapter 5

N-Path Filters with Distortion Cancellation, Achieving 80dB/decade RF selectivity

5.1 Introduction

This chapter extends the work of the previous two chapters to address the growing requirements for highly linear front-ends that are resilient to interferers both in adjacent and far-out channels. Recent advances in N-path filter design have shown a pathway for SAW-less receiver front-ends, but have their limitations in terms of the channel selectivity and resilience to close-in blockers.

Recently, several attempts have been made to improve front-end channel selectivity [48, 60, 61]. The use of a transconductance to cascade N-path filters in [48] limits the linearity. While the filter in [61] shows higher order filtering, it has high insertion loss without any baseband circuits, and is not amenable for broadband SAW-less solutions due to the use of inductors. Some other examples of higher order N-path filters include [3], which uses a passive cascade of N-path filters and [28, 30] where N-path filters drive a second-order driving point impedance, achieving sharper selectivity and linearity. The N-path filter in [59] has third-order current mode filtering to achieve better baseband selectivity and tolerance to close-in blockers, but has lower RF selectivity. Recently, an N-path filter [6] driving the first-ever third-order driving point impedance was demonstrated. However, the amplifiers used to synthesize the higher-order impedances in [6, 30] exhibit distortion, which affects the linearity for close-in blockers.

The N-path filter based receiver front-end of [3] has a second order real-pole roll-off, thereby limiting the sharpness of achievable filtering. Bottom-plate mixing helps enhance the far-out out-of-band linearity but not for close-in blockers. However, [3] and [4] provide a pathway to building higher-order N-path filters, by replacing the capacitive loads (Z_A, Z_B) of the N-path filters (see Fig. 5.1) with higher order impedances. With recent innovations [5, 6]

in synthesizing driving point impedances with 40dB/decade and 60dB/decade roll-off, the passive cascade of N-path filters shows potential to synthesize N-path filter-based receivers with up to 120dB/decade RF selectivity.

5.2 Architecture

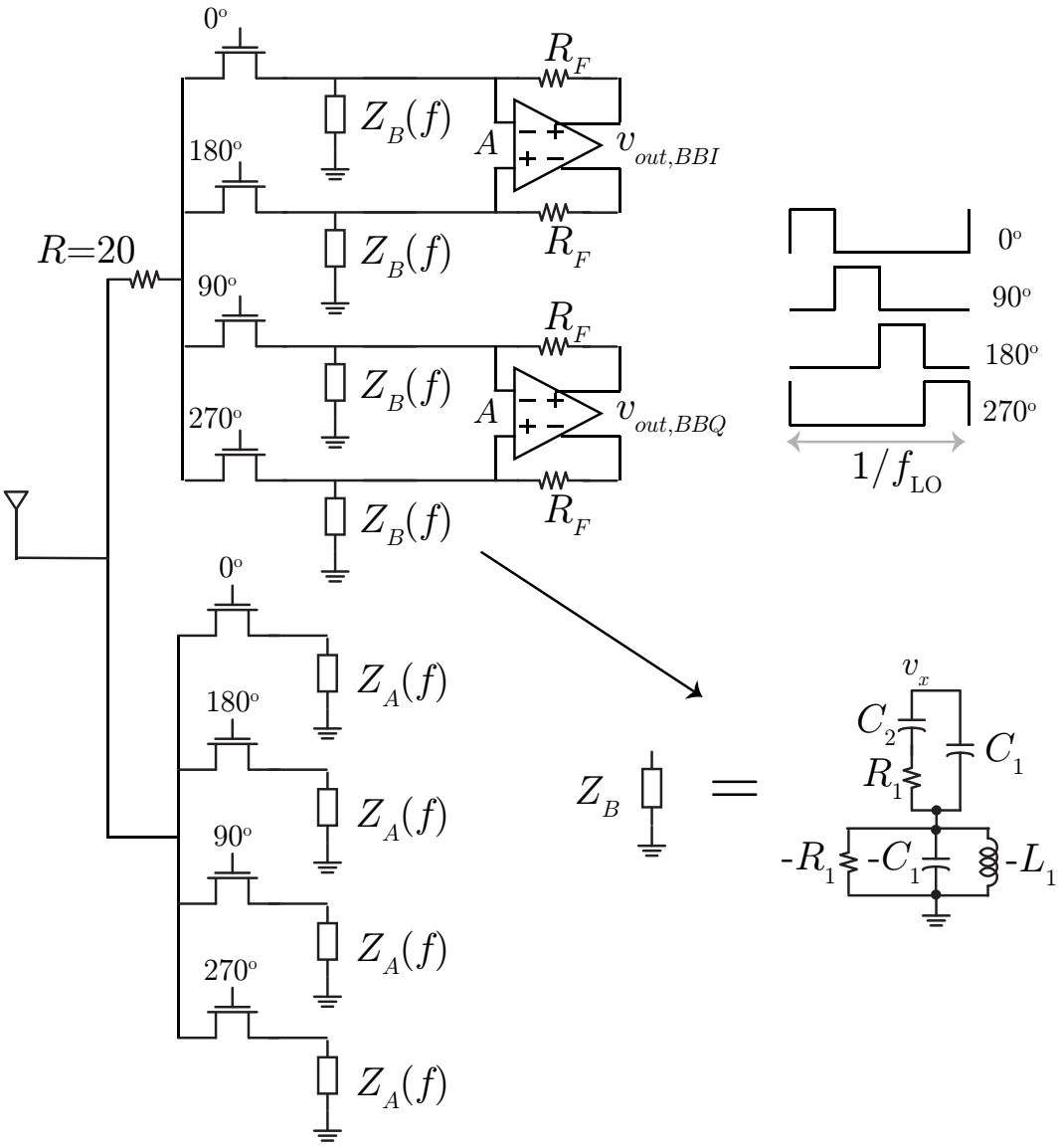


Figure 5.1: Passive cascade of N-path filters similar to [3, 4].

In this chapter, we propose an architecture for an N-path filter with 80dB/decade RF selectivity, through a passive cascade of a conventional N-path filter with an N-path filter loaded by a third order driving point impedance (see Fig. 5.1). The mechanism by which distortion is generated in the third-order impedance is studied, and a distortion cancellation mechanism is proposed. Detailed simulation plots verify the efficacy of this distortion cancellation mechanism. The driving point impedance with 60dB/dec. roll-off used in this work is shown in Fig. 5.1. It was shown in [6] that the impedance Z_B in Fig. 5.1 is capacitive, but with 60dB/dec. roll-off at higher frequencies instead of the 20dB/dec. roll-off exhibited by a capacitor. For the purpose of minimizing in-band noise, it is realized as a four-pole, one-zero impedance leading to a small in-band ripple in the transfer function. The design of the negative R_1, C_1 and L_1 required for synthesizing the desired impedance poses an interesting challenge.

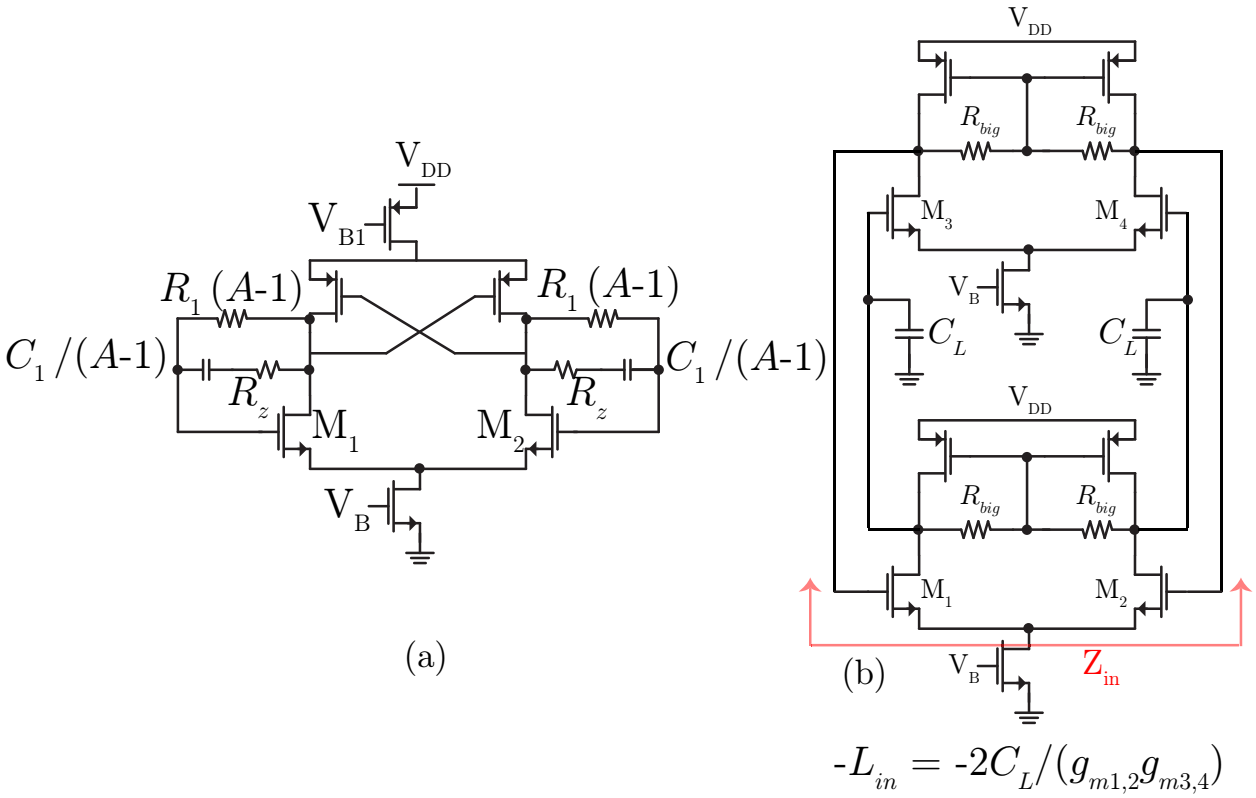


Figure 5.2: (a) Amplifier to realize negative RC. (b) "Negative gyrator" to realize negative inductance.

The negative inductance is synthesized using a "negative" gyrator with differential mode positive feedback [see Fig. 5.2(b)]. Just like in conventional gyrators, there exists common mode positive feedback, but with a loop gain much less than unity due to the tail current source degeneration. The negative shunt RC was synthesized in a similar fashion as in [5, 6]

by having a resistor and capacitor in positive feedback around an amplifier of gain A [see Fig. 5.2(a)]. The stability of this circuit was discussed in detail in [5]. The distortion generated by the amplifier in [5] limits its maximum achievable close-in IIP3. The distortion has a high-pass transfer function to the output, progressively worsening the IIP3 as the IM3 frequency approaches the edge of the band, an effect also observed in active filters.

5.3 Distortion Cancellation

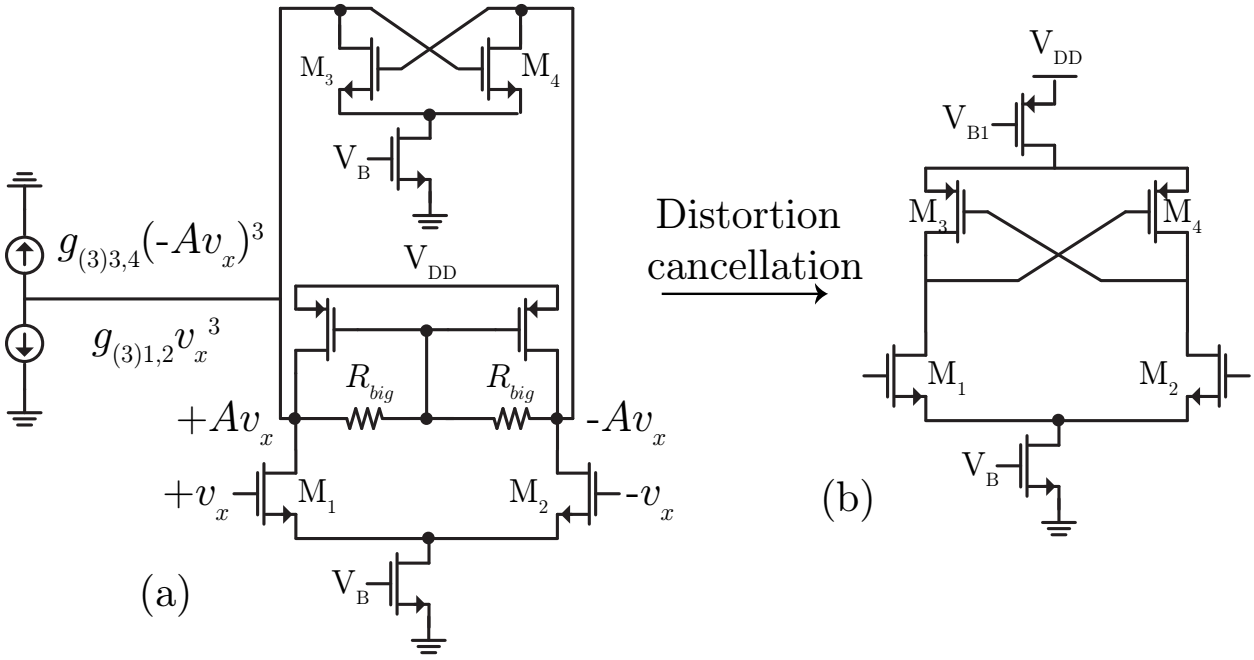


Figure 5.3: (a) Amplifier to realize negative RC in [5, 6]. (b) Proposed Amplifier used to realize negative RC, with distortion cancellation.

In [5, 6], the amplifier used to synthesize the negative RC impedance has an NMOS input transconductance with an NMOS cross-coupled pair as the load. A brief analysis of the weak third order non-linearity in this circuit gives us insights into cancelling this non-linearity. Weak non-linearity is analyzed by the method of distortion current injection. First, the linearized circuit is solved and the linear solution for the voltage v_x at the positive input of the negative RC amplifier is obtained [see Fig. 5.3(a)]. The node voltage at the corresponding output of the negative RC amplifier is given by Av_x, where $A = g_{m1,2}/g_{m3,4}$.

Now, the third order non-linearity injected by the NMOS input transconductance is given by $g_{(3)1,2}v_x^3$ and the third order non-linearity injected by the NMOS cross-coupled pair is given by $g_{(3)3,4}(-Av_x)^3$ [see Fig. 5.3(a)]. For M_{12} and M_{34} biased at the same g_m/I_D, $g_{(3)1,2} = Ag_{(3)3,4}$. Additionally, it may be noted that the third order non-linearity injected

by M_{12} is anti-phase to that injected by M_{34}. Therefore, the net third-order non-linearity injected at the output node of the amplifier used to synthesize the negative RC impedance is given by

$$i_{nl3} = g_{(3)1,2} v_x^3 (1 - A^2) \tag{5.1}$$

Clearly, this third order non-linearity i_{nl3} can be canceled when $A = 1$. However, this puts an unrealistic requirement of zero resistance and infinite capacitance in feedback in order to synthesize the desired negative RC shunt impedance. However, the realization that the two distortions are anti-phase may be used to cancel the net distortion. If M_{12} and M_{34} are biased at different g_m/I_D such that $g_{(3)1,2} = g_{(3)3,4} A^3$, then the net distortion current i_{nl3} injected at the output of this amplifier of gain A is zero. Additionally, using a PMOS cross-coupled pair, as shown in Fig. 5.3(b), also results in current reuse between the input transconductance and the cross-coupled pair, leading to power savings. However, it may be noted that this technique only cancels the distortion of the amplifier used to synthesize the negative RC impedance and not the distortion of the negative gyrator.

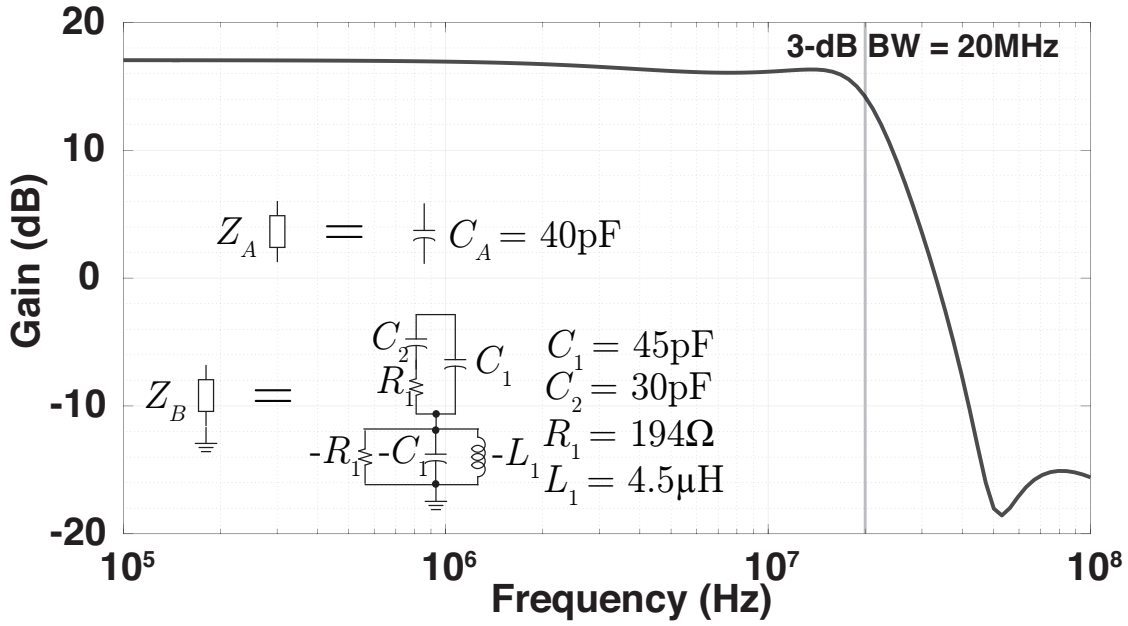


Figure 5.4: Representative simulation plots for the transfer function from the RF input to the baseband output (see Fig. 5.1) are shown for the component values indicated in the figure. For the amplifier used to synthesize the negative RC impedance, the value of $g_{m1,2} = 164$mS and $g_{m3,4} = 104$mS. The value of $A = 1.58$.

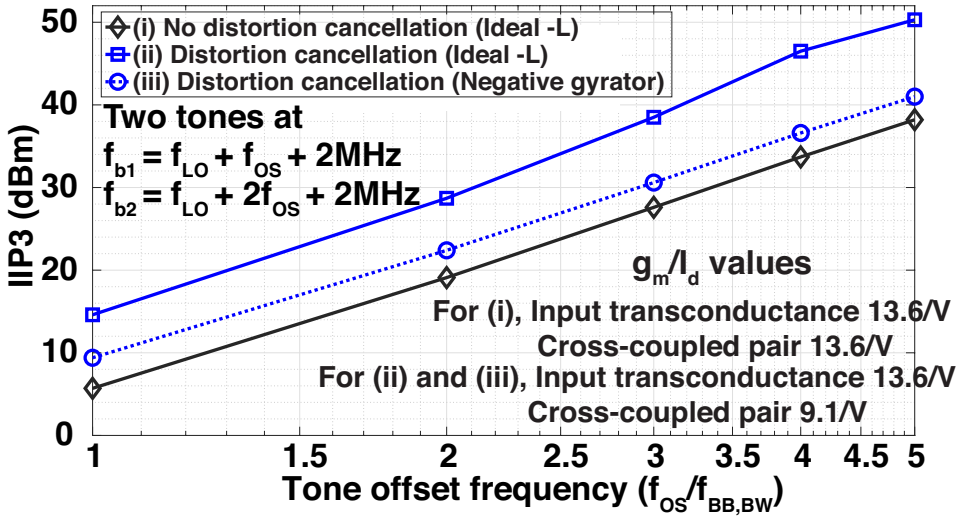


Figure 5.5: Plot showing simulated IIP3 as a function of tone offset frequency (represented as a fraction of the baseband bandwidth), for the following cases: (i) Without distortion cancellation and ideal negative inductance, (ii) With distortion cancellation in the negative RC amplifier and ideal negative inductance, (iii) With distortion cancellation in the negative RC amplifier, but not in the "negative" gyrator.

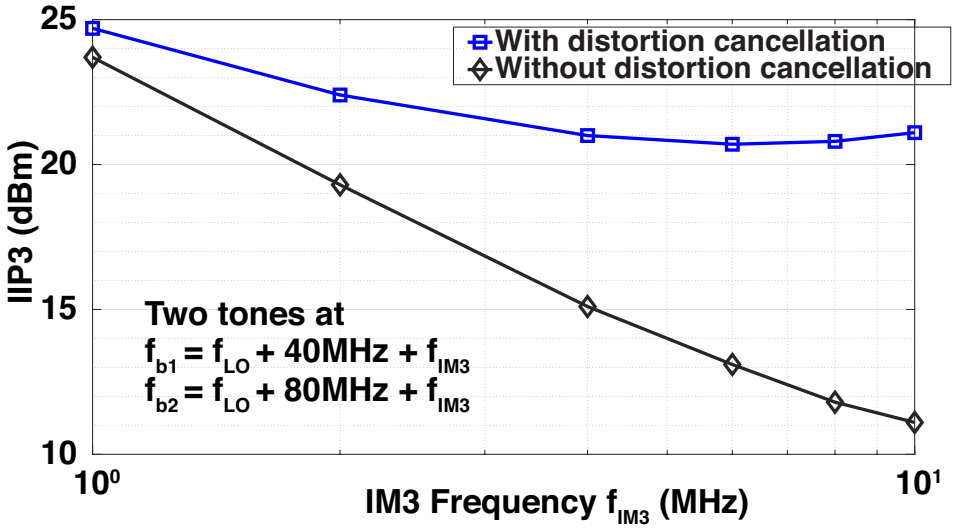


Figure 5.6: Plot showing simulated IIP3 as a function of in-band IM3 frequency (for a fixed tone-offset frequency of 40MHz), with and without distortion cancellation for the negative RC amplifier. In both cases, the simulation is with the actual "negative gyrator" circuit.

The distortion cancellation is illustrated with simulation plots from a representative example for the circuit in Fig. 5.1. The small signal gain and the component values are shown in the plot in Fig. 5.4. The IIP3 is simulated using a two-tone test such that the IM3 product falls in-band at 2MHz. In order to quantify the effect of the higher-order impedances and the baseband amplifiers alone on non-linearity, ideal mixer switches are assumed for this simulation. Consider the following two cases where the amplifier used to synthesize the negative RC impedance is implemented without [Fig. 5.3(a)] and with distortion cancellation [Fig. 5.3(b)]. In both cases, an ideal negative inductance is used so that only the effect of distortion cancellation of the negative RC amplifier may be studied. A significantly improved IIP3 is observed (9-12dB improvement) by using the circuit in Fig. 5.3(b) compared to the circuit in Fig. 5.3(a) [see Fig. 5.5]. However, when the distortion of the actual gyrator [see Fig. 5.5] is also taken into account, the benefits are reduced, as the distortion cancellation is not optimized to cancel the gyrator's distortion as well.

To provide a more complete comparison, the IIP3 is compared with and without distortion cancellation for the negative RC amplifier, but with the actual gyrator circuit in both cases. Additionally, since the distortion of the negative RC amplifier and the gyrator have different transfer functions to the output, a comparison of IIP3 is shown as a function of the in-band IM3 frequency for a fixed tone-offset frequency of 40MHz. Clearly, the circuit with the distortion cancellation for the negative RC amplifier only has a small degradation in IIP3 with the IM3 frequency, and outperforms the circuit without distortion cancellation [see Fig. 5.6].

5.4 Measurement

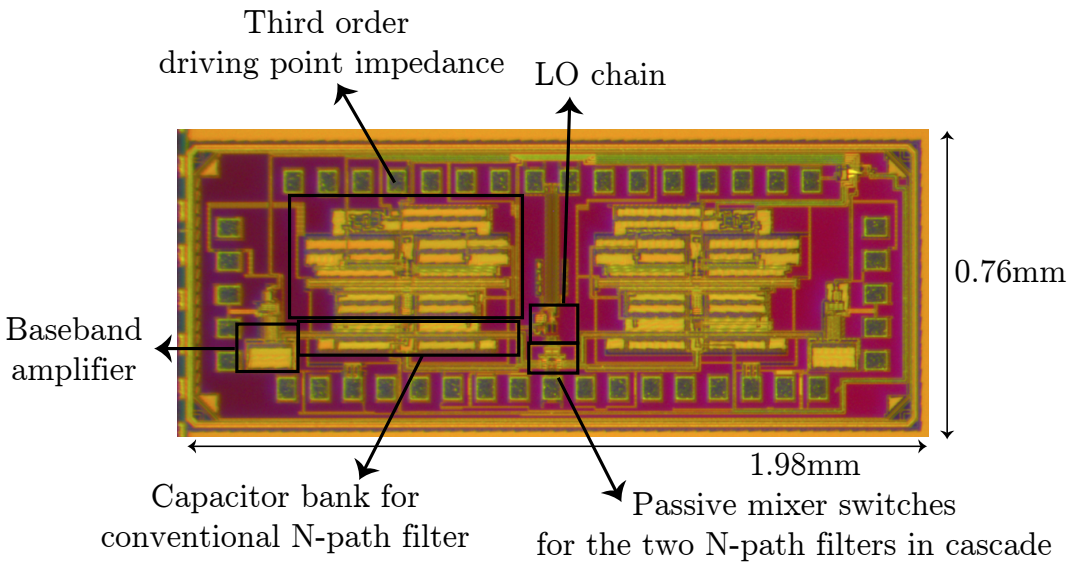


Figure 5.7: Die micrograph. The chip occupies an area of 1.5mm^2.

As proof-of-concept, a test chip (see Fig. 5.7) was fabricated in 28nm bulk CMOS, and directly bonded to a PCB. The measured conversion gain and s_{11} are shown in Fig. 5.8 for five different LO frequencies. A zoomed in plot of the conversion gain [Fig. 5.9] at f_{LO} = 1GHz shows a gain of 16.3dB and an RF bandwidth of 30MHz. The close-in sharp 23dB/octave roll-off verifies the fourth order front-end filtering. The subsequent flat region comes from the zeros in the implementation of the amplifier used to synthesize the negative RC impedance [5]. The measured conversion gain varies from 13.6dB to 16.8dB with f_{LO} [see Fig. 5.10].

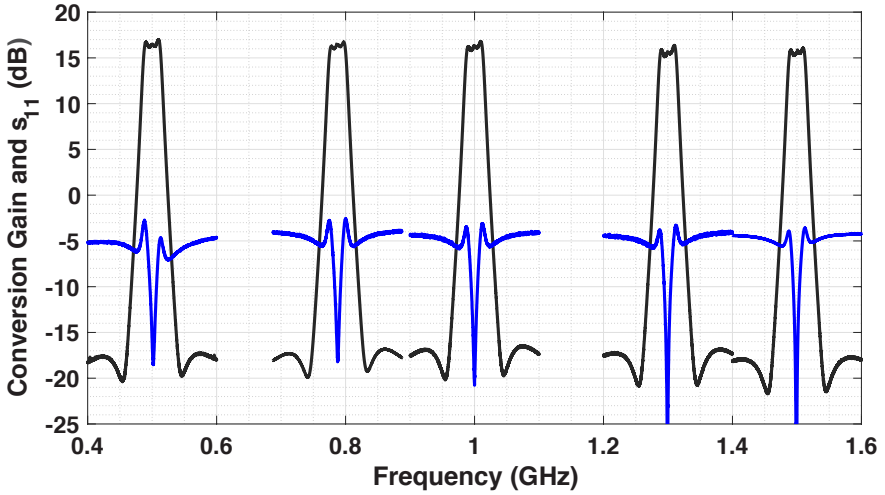


Figure 5.8: Measured s_{11}, gain for three different LO frequencies.

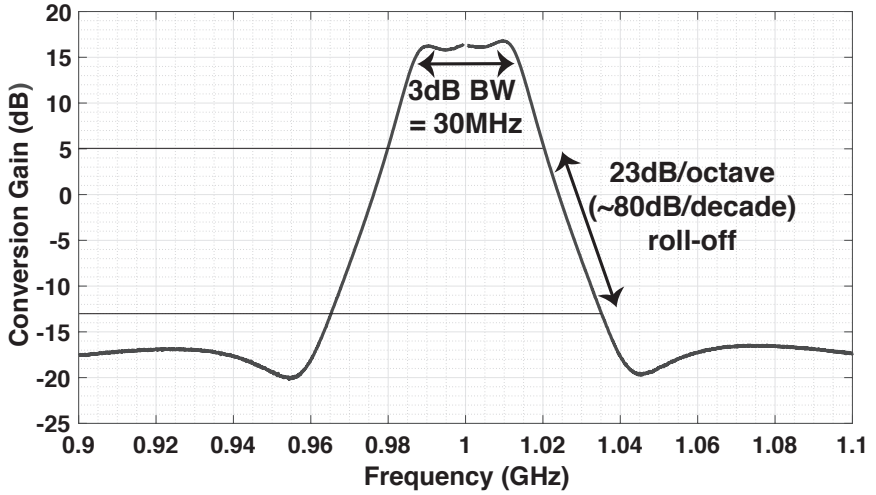


Figure 5.9: Zoomed-in gain for f_{LO} = 1GHz.

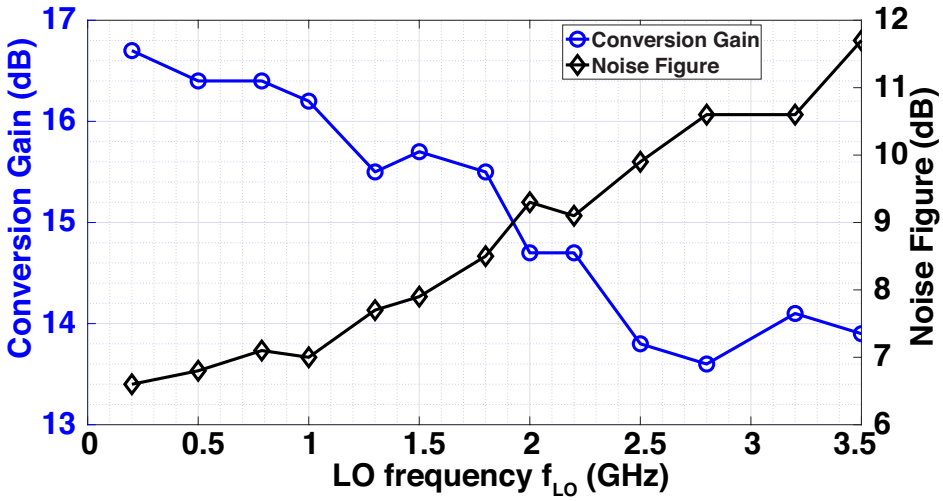


Figure 5.10: Measured gain, NF versus f_{LO}.

IIP3 was measured using a two-tone test, with the IM3 product falling in-band at 1MHz. Fig. 5.11 plots the IIP3 as a function of tone-offset frequency at $f_{LO} = 1.3$GHz. An adjacent channel ($f_{OS}/f_{RF,BW} = 1$) IIP3 of +22.5dBm was observed. The far-out IIP3 is limited by the size of the switches used. An adjacent channel B1dB of +7.5dBm and an alternate channel ($f_{OS}/f_{RF,BW} = 2$) B1dB of +10dBm illustrate the benefit of the fourth order RF filtering achieved in this work. Fig. 5.12 shows the measured adjacent and alternate channel B1dB and IIP3 versus f_{LO}, illustrating high linearity for a wide range of LO frequencies.

The measured in-band noise figure [see Fig. 5.10] varies from around 6.6dB at 200MHz to 11.7dB at 3.5GHz. The blocker-induced noise figure degradation was measured for f_{LO} = 787.5MHz and a blocker at 881MHz. The measured noise figure is around 7dB without a blocker and degrades by around 2dB in the presence of a 0dBm blocker and by 4.5dB in the presence of a 5dBm blocker [see Fig. 5.13], mainly due to reciprocal mixing.

5.5 Conclusion

To summarize, this chapter demonstrates an N-path filter based receiver with sharp 80dB per decade close-in roll-off, by using a passive cascade of a first order N-path filter and a third order N-path filter. A distortion cancellation scheme was proposed to mitigate the distortion caused by the amplifiers used in synthesizing the negative RC impedance. Table 5.1 compares this work against the state-of-the-art N-path filter based receivers with higher order roll-off. This work achieves a record adjacent channel B1dB of 8dBm and alternate channel B1dB of 10dBm, and state-of-the-art adjacent channel IIP3 of 23dBm.

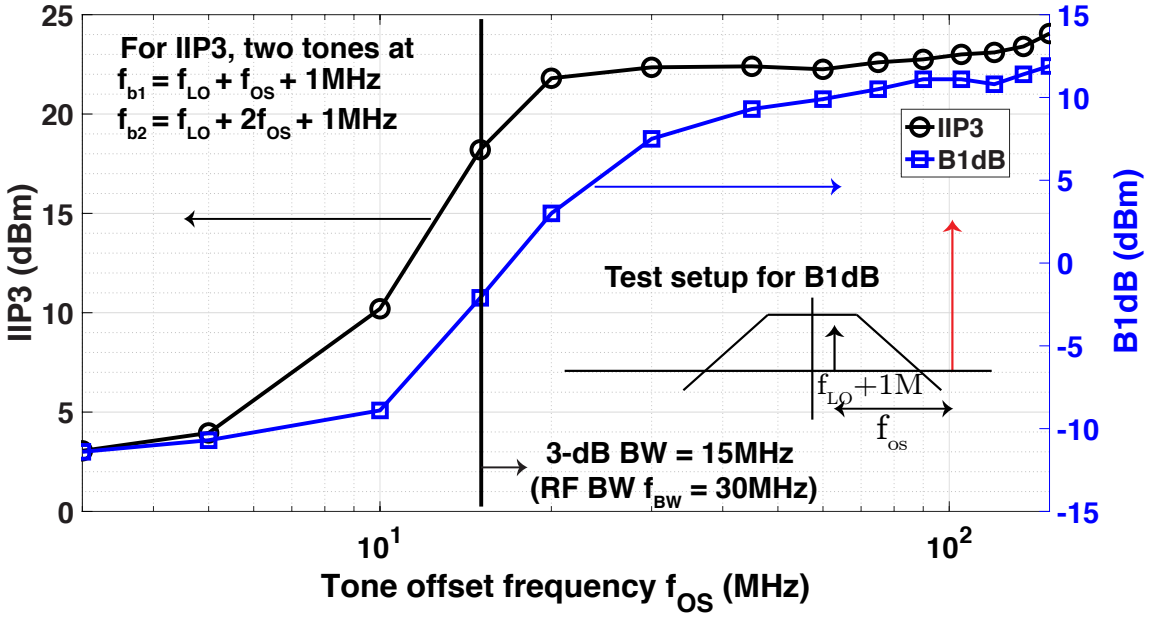


Figure 5.11: Measured IIP3 and B1dB versus offset frequency for $f_{LO} = 1$GHz.

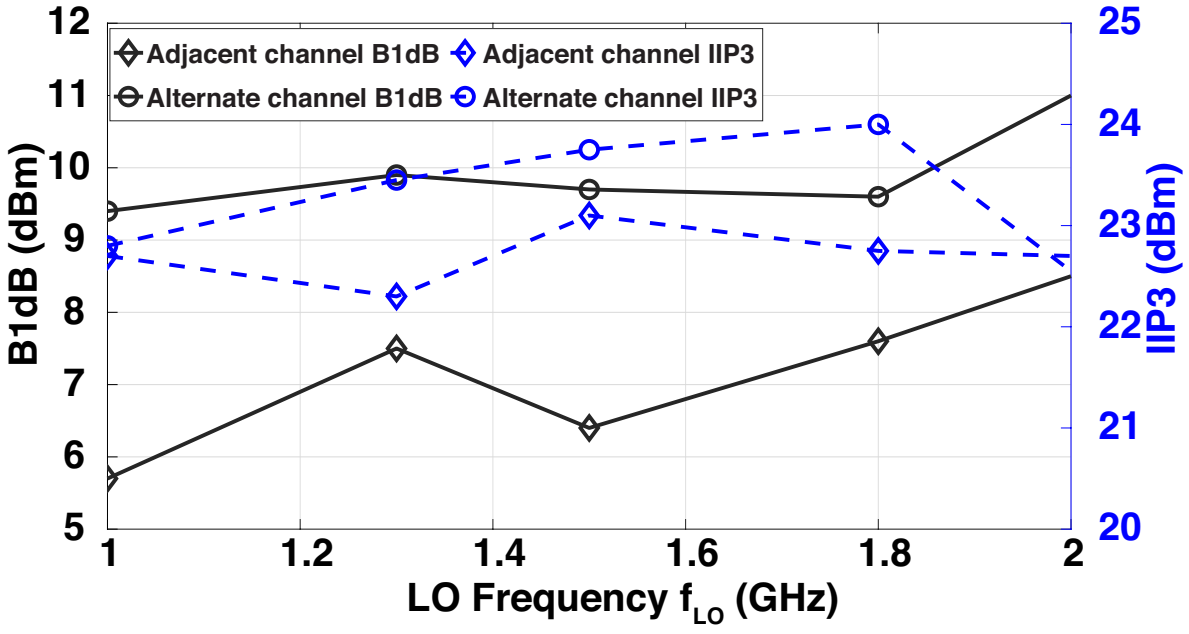


Figure 5.12: Measured adjacent and alternate channel B1dB and IIP3 versus f_{LO}.

Table 5.1: Comparison with State-of-the-Art N-Path Filter-Based Receivers with Higher Order Roll-Off

	JSSC13 [48]	ISSCC17 [60]	ISSCC17 [3]	JSSC18 [28]	JSSC20 [5]	SSCL20 [6]	**This work**
Architecture	Active N-Path Filter	Filtering by Aliasing	Bot. Plate Mixing in N-Path Filter	N-Path Filter with positive cap. feedback	N-Path Filter driving Z w/ 40dB/dec. roll-off	N-Path Filter driving Z w/ 60dB/dec. roll-off	**N-Path Filter w/ 80dB/dec. RF Selectivity**
Technology	65nm	65nm	28nm	45nm SOI	28nm	28nm	**28nm**
f_{RF} (GHz)	0.1-1.2	0.1-1	0.1-2	0.2-8	0.2-2	0.2-4.5	**0.2-3.5**
RF Input	Differential	Differential	Differential	Differential	Single Ended	Single Ended	**Single Ended**
Gain (dB)	25	23	16	21	13	15.3	**16.3**
RF Bandwidth	8MHz	2.5-40MHz	13MHz	20MHz	18MHz	35MHz	**30MHz**
Adjacent channel IIP3* f_{OS}/f_{BW}=1	12dBm	20dBm	24dBm	17dBm	15dBm	13dBm	**+23dBm**
Adjacent channel B1dB* f_{OS}/f_{BW}=1	-14dBm	2dBm	-3dBm	0dBm	-3/3dBm (I/Q)	2dBm	**+8dBm**
Alternate channel B1dB* f_{OS}/f_{BW}=2	-1dBm	10dBm	5dBm	7dBm	2/8dBm (I/Q)	6.3dBm	**+10dBm**
NF at 1GHz ‡	3.0dB	7dB	6.3dB	2.5dB	4.8dB	5dB	**7dB**
Power at 1GHz ♯	57.4mW	84 mA	66mW	80mW	160mW	190mW	**100mW**
Supply (V)	1.2	1.2/1	1.2/1	1.2	1.2	1.2	**1.2/1.4**

* Adjacent and alternate channel B1dB and IIP3 values for other works extrapolated from graphs.
‡ Noise figure at 1GHz for other works extrapolated from graphs.
♯ Power includes LO power and power consumption of all the core baseband circuits.

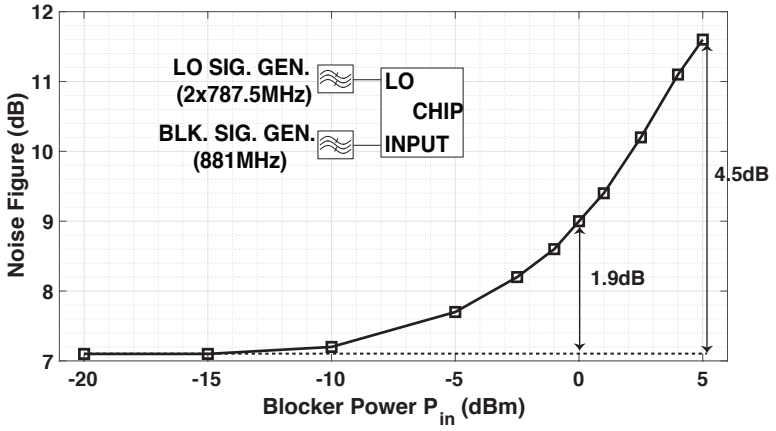


Figure 5.13: Measured in-band blocker noise figure for $f_{LO} = 787.5$MHz.

Chapter 6

Design of High Linearity Mixer-First Receivers for mm-wave Digital MIMO Arrays

6.1 Introduction

As described in Chapter 1, multi-user support for a large number of users can be achieved through massive digital beam-forming arrays with high spatial flexibility. Since the noise of the receiver front-ends is mostly uncorrelated across the array, the beamforming operation results in a $\sim 10\log(M)$ boost of the signal-to-noise ratio (SNR) due to noise averaging, where M is the number of antennas in the array. As a result, in massive arrays, the noise figure requirement of each individual receiver can be relaxed [62]. On the other hand, digital beamforming architectures require high linearity RF front-ends, since the spatial filtering of out-of-beam, in-band interferers is performed at the baseband.

The mm-wave 5G spectrum covers a wide range of bands, including bands ranging from 24–40GHz. Traditional circuit techniques, using tuned front-ends [23–25], cannot support the entire band with a single transceiver. It is desirable to have a single integrated circuit solution to support operation across the entire mm-wave 5G band. This mandates the need for wideband highly linear receiver front-ends.

Passive mixer-first receivers or N-path-filter-based receivers (see Fig. 6.1) have been used at lower RF frequencies for high linearity across a wide band of operation. A lot of focus of the research at lower RF frequencies has been to improve the resilience to out-of-band interferers. The impedance translational property of N-path filters has been used to synthesize tunable high-Q band-pass filters. While passive mixer-first receivers and their enhancements [13, 14, 30] have made strides towards improving out-of-band IIP3, the in-band linearity of such receivers is still limited by the linearity of the baseband amplifiers.

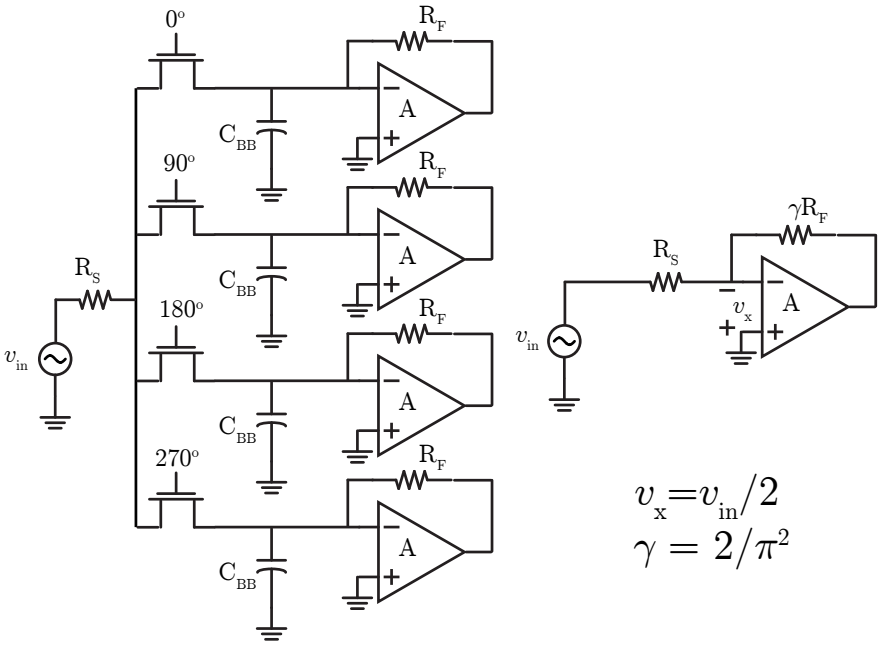


Figure 6.1: Conventional N-path filter and its LTI equivalent.

N-path filters at RF frequencies use N non-overlapping square-wave LO phases (usually $N = 4$) to drive the mixer switches. Today, such an LO waveform cannot be synthesized at mm-wave frequencies even in the most advanced process nodes. A common solution in mm-wave mixer-first receivers like [42] is to use pseudo non-overlapping sine-wave LO drive, at the cost of reduced mixer switch linearity. In [27], we proposed a broadband highly linear mixer-first receiver front-end exploiting feedback linearization, which addresses the aforementioned issues.

Compared to [27], this chapter provides greater detail on the benefits and limitations of feedback linearization. It also delves into great detail about enhancing linearity of mixer switches and provides simulation results supporting the superior mixer IIP3 of our architecture compared to others. It also describes the challenges associated with LO waveform generation for N-path filters at mm-wave frequencies, and provides solutions. Additionally, it provides more extensive measurement results compared to [27]. Finally, it also shows why this architecture is a good candidate for an LNA-based receiver front-end driving a passive mixer.

The content of this chapter is organized as follows. Section 6.2 describes the architecture and circuit design details. It provides simulation results to highlight the various salient features of this work. Section 6.3 presents the measurement results, and Section 6.4 compares this work against the state-of-the-art and provides the key takeaways of the work.

6.2 Architecture and Circuit Design

6.2.1 Feedback Linearization

Fig. 6.1 shows the architecture for a conventional passive mixer-first receiver driven by a 4-phase non-overlapping square wave LO drive, and its LTI equivalent, where the baseband impedance is scaled by a factor $\gamma = 2/\pi^2$ [19].[1] As detailed in [19], the impedance translational property of these N-path filters is used for input matching. An explicit shunt termination resistance at baseband would yield a 3dB noise figure penalty. Therefore, input matching is performed in these receiver front-ends through a resistor R_F in feedback around an amplifier of gain A. In addition to reducing the noise figure, increasing the gain A and R_F of the amplifier also helps in achieving higher closed loop gain, given by

$$\begin{aligned} A_{CL} &\approx 1 - \frac{\gamma R_F}{R_S} \\ &\approx -\frac{\gamma R_F}{R_S} \end{aligned} \tag{6.1}$$

The input impedance looking into the amplifier input is $R_F/(1+A)$. Therefore, to maintain input match, as the amplifier gain A is increased, the feedback resistance R_F also needs to be increased. This implies that the amplifier input always processes a signal equal to $v_{in}/2$. We analyze the non-linearity arising from both the input transconductance g_m of the amplifier and the output conductance ($g_o = 1/r_o$) of the amplifier.

First, let us consider the V_{GS}-limited linearity due to the input transconductance. The drain-source current is given by $i_{ds} = g_m v_{gs} + g_{m3} v_{gs}^3$. The output voltage v_o is given by $v_o = g_m r_o v_{gs} + g_{m3} r_o v_{gs}^3$. Therefore, the characteristic of the open-loop amplifier of Fig. 6.1 can be described as $v_o = A v_{gs} + a_3 v_{gs}^3$. If r_o is increased, while maintaining the same g_m, both $A = g_m r_o$ and $a_3 = g_{m3} r_o$ of the amplifier characteristic are scaled up by the same factor. In other words, third order distortion a_3 scales proportionally to the open-loop gain A.[2] For the architecture of Fig. 6.1, where input matching is performed using a resistor R_F in feedback around an amplifier of gain A, it is easy to show that under the constraint for input match, the in-band IIP3 and OIP3 due to the non-linearity of the input transconductance are given by

$$\begin{aligned} V_{IIP3} &\approx \sqrt{\frac{8A}{3a_3}} \\ V_{OIP3} &\approx A\sqrt{\frac{8A}{3a_3}} \end{aligned} \tag{6.2}$$

[1] Note that the shunt re-radiation resistance has been neglected in the LTI equivalent for simplicity. It will be considered while analyzing the noise figure.

[2] If r_o is increased by increasing channel length, while maintaining same g_m, g_{m3} may not scale proportionally. However, such an assumption serves to illustrate the benefits of higher A for feedback linearization.

This assumes that the mixer switches are perfectly linear. The linearity of the mixer switches will be dealt with in a subsequent section. It is clear from equation (6.2) that the in-band IIP3 (due to input transconductance non-linearity) of a conventional mixer-first front-end of Fig. 6.1 does not benefit from feedback linearization under the constraint of input match, and is purely a function of the V_{GS} bias. As A is changed, both the closed loop gain A_{CL} and the OIP3 increase proportionally to the open loop gain.

Now, let us consider the V_{DS}-limited linearity due to the output conductance. The drain-source current is given by $i_{ds} = g_o v_{ds} + g_{o3} v_{ds}^3$. It can be shown that the in-band IIP3 and OIP3 due to the non-linearity of the output conductance are given by

$$\begin{aligned} V_{IIP3} &\approx \frac{1}{A}\sqrt{\frac{8g_o}{3g_{o3}}} \\ V_{OIP3} &\approx \sqrt{\frac{8g_o}{3g_{o3}}} \end{aligned} \tag{6.3}$$

Consider the term g_o/g_{o3} in equation (6.3). In order to enhance open loop gain A, if g_o is reduced, while maintaining the same g_m, g_{o3} is assumed to scale down by the same amount using arguments used previously. Now, this means that, as g_o is changed, the term g_o/g_{o3} remains constant and is a function of the bias. From the equation for in-band IIP3 and OIP3, it is seen that the in-band IIP3 degrades with increasing loop gain A and the in-band OIP3 remains a constant. Clearly, that the in-band IIP3 and OIP3 (due to output conductance non-linearity) of a conventional mixer-first front-end of Fig. 6.1 do not benefit from feedback linearization under the constraint of input match. Extraction of the parameters g_{o3} and g_{m3} of the actual inverter-based amplifier used in this work show that the non-linearity due to the output conductance is a much more dominant source of non-linearity than the input transconductance. However for sake of completeness, both sources of non-linearity have been analyzed.

Now consider the architecture proposed in Fig. 6.2. Here, the input match is performed using an explicit series termination resistance R'_S. Compatibly with the digital massive MIMO requirements discussed in Section 6.1, this topology targets enhanced linearity at the cost of higher noise figure, by using an explicit series termination resistance R'_S for input match. The R_F and gain A are chosen such that $\gamma R_F/(1+A)$ is considerably smaller than R'_S. The closed loop gain, under input-match constraint, is now given by,

$$A_{CL} \approx -\frac{\gamma R_F}{R_S} \tag{6.4}$$

Node v_x is a virtual ground whose magnitude is given by

$$\begin{aligned} \frac{v_x}{v_{in}} &= \frac{\gamma R_F}{(1+A)(R_S + R'_S) + \gamma R_F} \\ &= \frac{\gamma R_F}{2(1+A)R_S} \end{aligned} \tag{6.5}$$

For the circuit in Fig. 6.2, where input match is performed through an explicit series resistor, the feedback resistance R_F need not be changed with A to maintain input match (under the previously stated assumption $\gamma R_F/(1+A) \ll R'_S$). However, as A is increased, the virtual ground voltage v_x becomes smaller. To analyze the non-linearity of the circuit due to the input transconductance, we inject a third order voltage non-linearity (equal to $g_{m3} r_o v_x^3$) at the output node of the LTI equivalent circuit shown in Fig. 6.2, and compute the amount by which the negative feedback loop attenuates it. The third order non-linearity injected $v_{nl3,gm}$, and the resultant output third order non-linearity $v_{o3,gm}$ are given by,

$$\begin{aligned} v_{nl3,gm} &= a_3 \left(\frac{\gamma R_F}{2(1+A)R_S} v_{in} \right)^3 \\ v_{o3,gm} &= \frac{v_{nl3}}{1 + \frac{(R_S+R'_S)A}{(R_S+R'_S)+\gamma R_F}} \approx \frac{v_{nl3}}{1 + \frac{2R_S A}{2R_S+\gamma R_F}} \end{aligned} \tag{6.6}$$

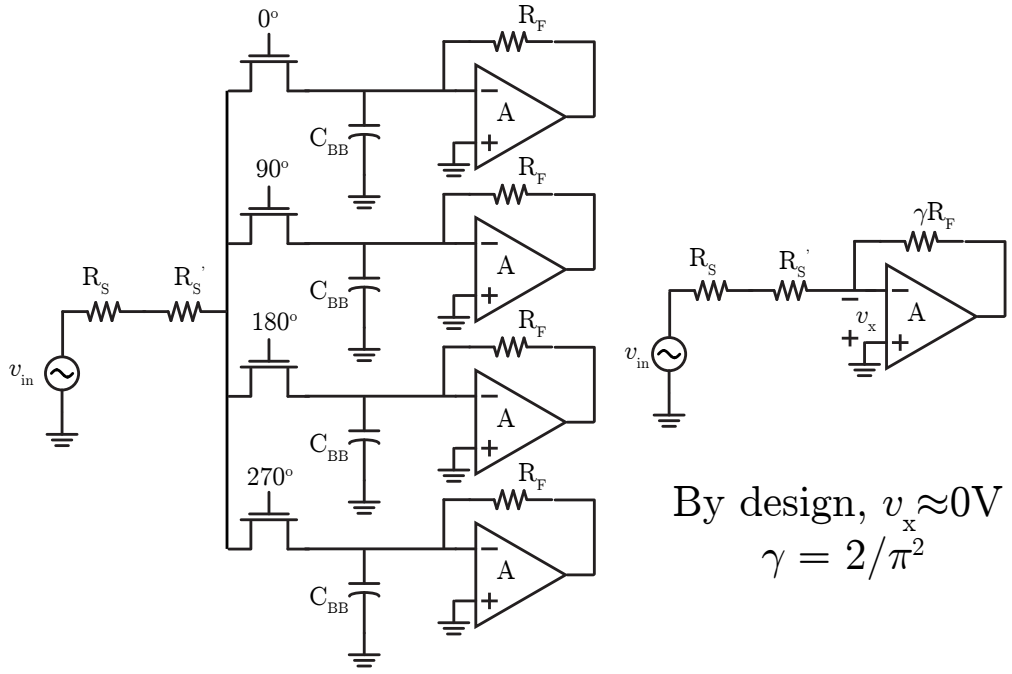


Figure 6.2: N-path filter exploiting feedback linearization and its LTI equivalent.

Consequently, the in-band IIP3 and OIP3 are given by

$$\begin{aligned} V_{IIP3} &\approx \sqrt{\frac{4A}{3a_3}\left(\frac{(1+A)R_S}{\gamma R_F}\right)^2\left(1+\frac{2R_SA}{2R_S+\gamma R_F}\right)} \\ &\approx \sqrt{\frac{8A}{3a_3}}\left(\frac{AR_S}{\gamma R_F}\right)^{\frac{3}{2}} \\ &\approx \sqrt{\frac{8A}{3a_3}}\left(\frac{A}{A_{CL}}\right)^{\frac{3}{2}} \\ V_{OIP3} &= A_{CL}V_{IIP3} \\ &\approx \sqrt{\frac{8A}{3a_3}}\sqrt{\frac{A^3}{A_{CL}}} \end{aligned} \tag{6.7}$$

The assumptions made in the approximation in equation (6.7) are $A \gg 1$ and $\gamma R_F \gg 2R_S$. The first term $\sqrt{8A/3a_3}$ in equation (6.7) is purely a function of the V_{GS} bias. If the closed loop gain $A_{CL} = \gamma R_F/R_S$ is kept constant, and the open loop gain of the amplifier A is increased, the OIP3 and IIP3 increase as $A^{3/2}$.

Now, we repeat this analysis for the V_{DS} limited non-linearity due to the output conductance. As stated earlier, for the amplifier used in this work, the output conductance is the more dominant source of non-linearity. To analyze the non-linearity of the circuit due to the output conductance, we inject a third order voltage non-linearity (equal to $g_{o3}r_oA^3v_x^3$) at the output node of the LTI equivalent circuit shown in Fig. 6.2, and compute the amount by which the negative feedback loop attenuates it. The third order non-linearity injected $v_{nl3,go}$, and the resultant output third order non-linearity $v_{o3,go}$ are given by,

$$\begin{aligned} v_{nl3,go} &= g_{o3}r_o\left(\frac{A\gamma R_F}{2(1+A)R_S}v_{in}\right)^3 \\ v_{o3,go} &= \frac{v_{nl3,go}}{1+\frac{(R_S+R'_S)A}{(R_S+R'_S)+\gamma R_F}} \approx \frac{v_{nl3,go}}{1+\frac{2R_SA}{2R_S+\gamma R_F}} \end{aligned} \tag{6.8}$$

Consequently, the in-band IIP3 and OIP3 are given by

$$\begin{aligned} V_{IIP3} &\approx \sqrt{\frac{8g_o}{3g_{o3}}}\sqrt{\frac{A}{A_{CL}^3}} \\ V_{OIP3} &= A_{CL}V_{IIP3} \\ &\approx \sqrt{\frac{8g_o}{3g_{o3}}}\sqrt{\frac{A}{A_{CL}}} \end{aligned} \tag{6.9}$$

As discussed previously, the first term $\sqrt{8g_o/3g_{o3}}$ in equation (6.9) does not vary with increasing open loop gain A and is purely a function of the bias. If the closed loop gain

$A_{CL} = \gamma R_F/R_S$ is kept constant, and the open loop gain of the amplifier A is increased, the OIP3 and IIP3 increase as $\sqrt{A}$, illustrating the benefit of higher linearity with increased open loop gain A. This is verified by simulation results shown in Fig. 6.3. The open loop gain A of the amplifier is swept, but the feedback resistance R_F is kept constant as the matching is performed through the explicit series resistor R'_S. Therefore, the closed loop gain A_{CL} remains constant as the open-loop gain A is swept. However, the in-band IIP3 and the OIP3 increase as $A^{1/2}$, as seen from the slope of 0.5 in the log scale plot in Fig. 6.3.

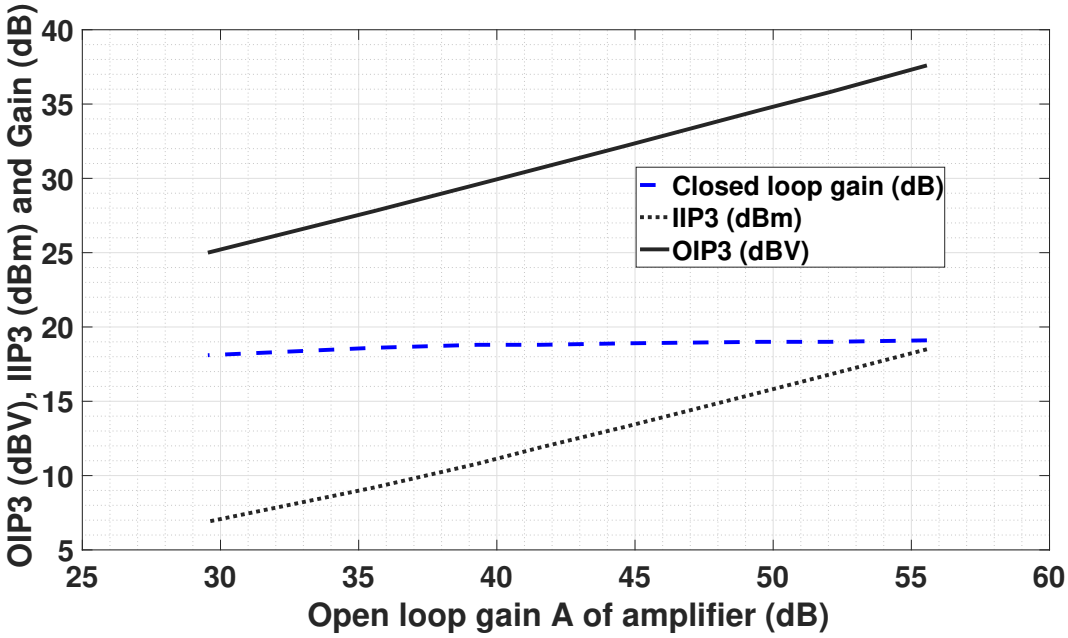


Figure 6.3: Simulated in-band IIP3, differential OIP3 and closed loop differential gain of proposed architecture versus amplifier open loop gain A.

For the plot in Fig. 6.4, we consider the actual implementation of our circuit, where the open loop gain A of the amplifier is fixed. The feedback resistance R_F is programmable to trade-off gain for linearity. It can be seen from equation (6.7) that for a fixed open loop gain A of the amplifier, the closed loop gain A_{CL} is proportional to R_F. The IIP3 is proportional to $A_{CL}^{-3/2}$ and the OIP3 is proportional to $A_{CL}^{-1/2}$. This well-studied effect of feedback linearization is verified by the simulation plot in Fig. 6.4.

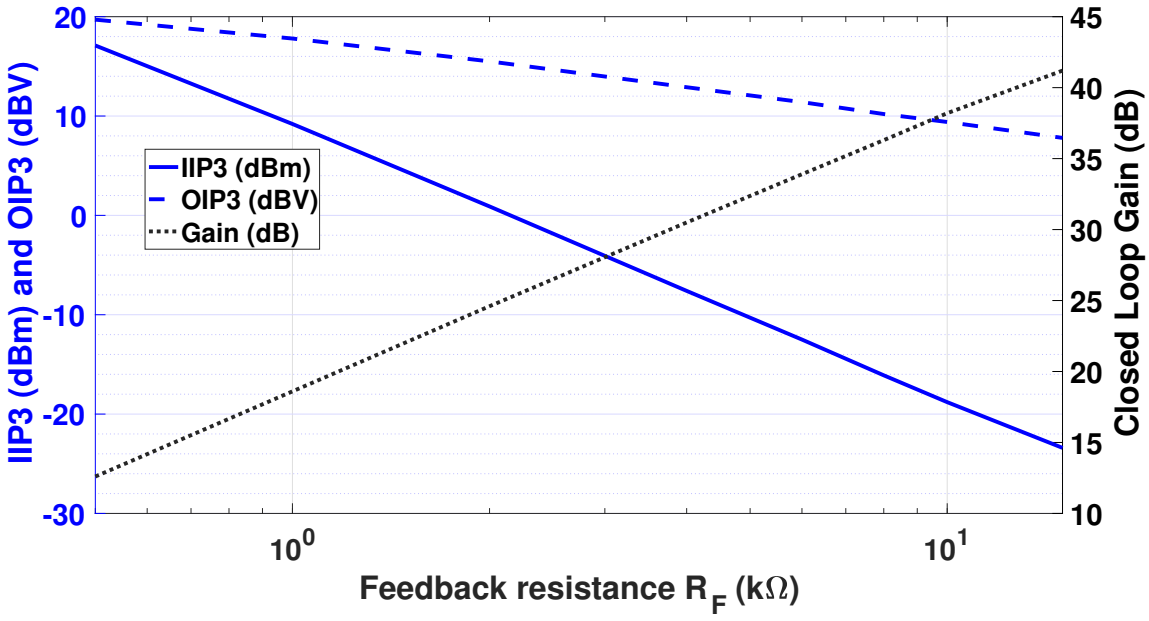


Figure 6.4: Simulated in-band IIP3, differential OIP3 and closed loop differential gain of proposed architecture versus R_F, for amplifier open loop gain A equal to 60.

Importantly, the use of shunt feedback also increases the instantaneous bandwidth of the receiver front-ends, an important requirement to support the high data rates of next generation wireless devices. To ensure high open-loop gain A for the amplifier and good common mode rejection, a current starved differential inverter-based amplifier was used. Devices with a channel length of 200nm were used to obtain a higher $g_m r_o$. However, the parasitics limit the achievable RF bandwidth to around 600MHz, for the choice of transistor widths. A higher bandwidth may be obtained with a lower channel length with a lower $g_m r_o$ at the cost of reduced IIP3.

6.2.2 Mixer Switch Linearity

It was seen in Fig. 6.4 that for a gain of $\sim$ 18dB and $\sim$ 12dB, an IIP3 of 9dBm and 17dBm respectively, may be achieved. However, this holds true only if the mixer switches are perfectly linear. Considering the non-linearity of the mixer switches as well, the overall IIP3 is given by the well-known cascade IIP3 formula[3],

$$\frac{1}{V_{IIP3}^2} = \frac{1}{V_{IIP3,mix}^2} + \frac{a_{mix}^2}{V_{IIP3,BB}^2} \tag{6.10}$$

The conversion gain of a 4-phase passive mixer is approximately unity. Therefore, to achieve the desired IIP3 of Fig. 6.4, $\text{IIP3}_{\text{mix}} \gg \text{IIP3}_{\text{BB}}$. That is, we need to build highly linear

[3]neglecting second order interaction.

passive mixers with IIP3 much higher than $9 - 17$dBm. This is quite challenging at mm-wave frequencies. In this section, we look at various techniques to achieve high in-band linearity for passive mixers at mm-wave frequencies.

Consider the proposed architecture of Fig. 6.2 with an explicit series resistor R'_S for matching. Now, there are three possible locations for the placement of R'_S. One is shown in Fig. 6.2, where there is a series resistor common to all four paths of the N-path mixer. For a 4-phase non-overlapping LO, this is equivalent to placing one series resistor R'_S in each of the four paths, as shown in Fig. 6.5(a). The distinction between these two cases will be made subsequently. However, for now, we compare the two circuits shown in Figs. 6.5(a) and (b), where there is an explicit R'_S in each path. In Fig. 6.5(a), R'_S is placed before the mixer switch towards the RF input. In Fig. 6.5(b), R'_S is placed after the mixer switch towards the baseband amplifier.

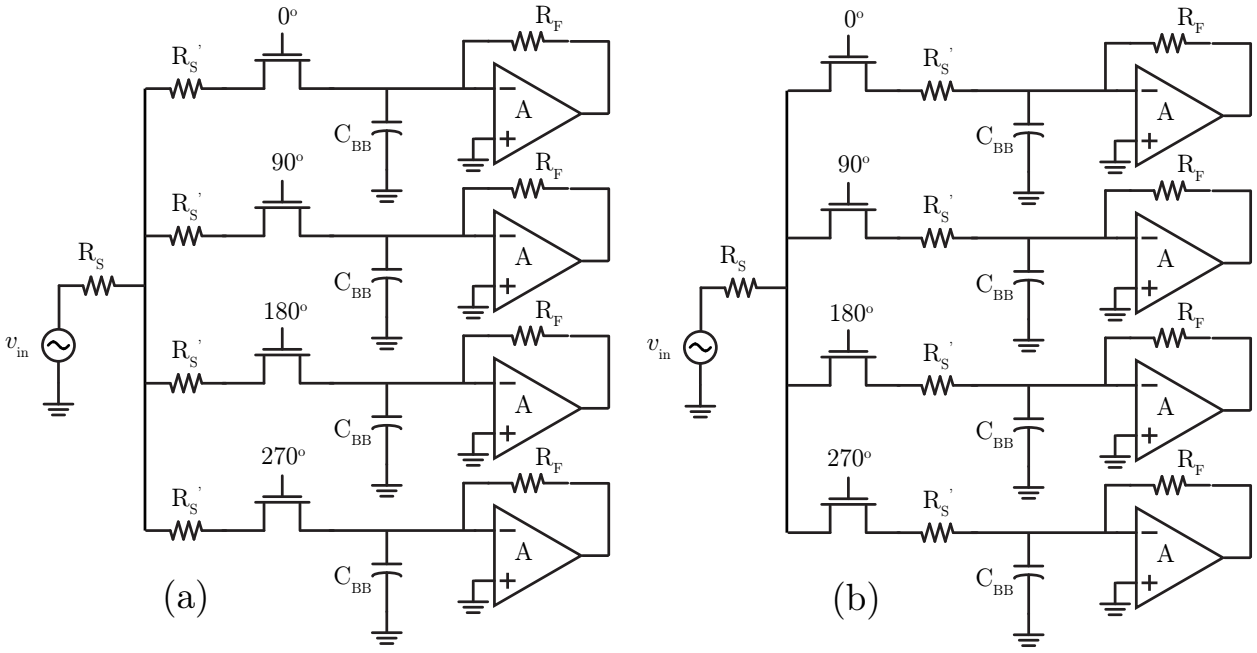


Figure 6.5: Two variants of proposed N-path filter architecture with series resistor R'_S (a) before the mixer switches (b) after the mixer switches.

To compare the linearity of the mixer switches in the two cases, the mixer is simulated without the baseband amplifier by terminating the mixer baseband output with a resistance equal to the input impedance ($\gamma R_F/(1 + A)$) looking into the amplifier. Additionally, this resistance is terminated with a DC voltage equal to the bias point of the inverter in the desired mode of operation. The gates of the mixer switches are driven at $f_{LO} = 20$GHz, with a 4-phase non-overlapping square wave LO swinging from 0 to $V_{DD} = 1.2$V. The size of the mixer switches is swept such that R_{SW}, the mixer switch ON resistance, varies from

7.2Ω to 36Ω.[4] IIP3 of the mixer switches is plotted versus R_{SW} for the two placements of R'_S in Fig. 6.6. Clearly, the IIP3 of mixer switches is significantly higher (more than 10dB higher for ON resistance equal to 7.2Ω) if the series resistor R'_S is placed before the mixer switch as compared to placing it after the mixer switch.

Analytical expressions to compare the linearity performance of the circuits in Fig. 6.5 are cumbersome. Hence, we resort to explaining the simulation results through approximate calculations which are more insightful. Consider the source node of the NMOS mixer switch shown in Fig. 6.5(a). The voltage swing at this virtual ground node is approximately given by equation (6.5). However for the circuit in Fig. 6.5(b), the source node swings by an amount approximately equal to

$$\begin{aligned} v_{\text{mix,source}} &= v_{in}\frac{R'_S + \frac{\gamma R_F}{A+1}}{2R_S} \\ &\approx \frac{v_{in}}{2} \end{aligned} \tag{6.11}$$

The approximation in the second line is valid when the mixer switch resistance $R_{SW} \ll R_S$. Equation (6.11) tells us that the source node swings by an amount equal to $v_{in}/2$ for the circuit in Fig. 6.5(b). During the ON phase of the LO, the gate voltage V_G of the mixer switches is constant, equal to V_{DD}, except during the finite rise and fall times of the LO waveform. However, the source voltage swing is significantly lesser in case of the circuit in Fig. 6.5(a) than for the circuit in Fig. 6.5(b). Therefore, there is significantly smaller V_{GS} modulation of ON resistance of the mixer switches in Fig. 6.5(a). This reduction of V_{GS} modulation of ON resistance of mixer switches is very similar to the effect of bottom plate mixing demonstrated in [29]. If the source of the mixer switch were a perfect ground, the in-band IIP3 of the mixer switches may be derived similar to the derivation of out-of-band IIP3 in [36], and it can be shown that the IIP3 is proportional to

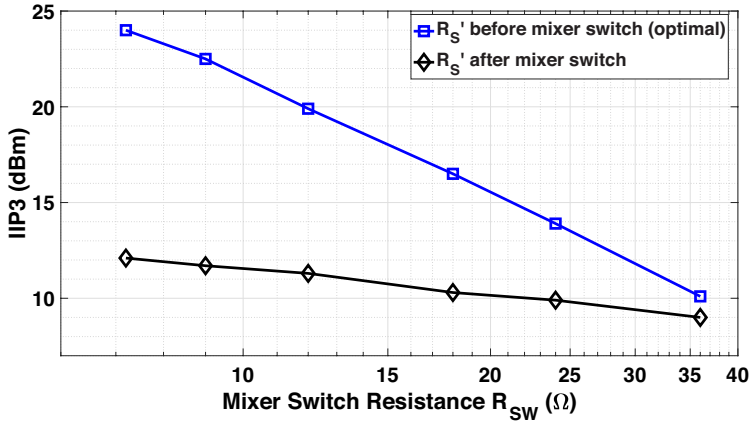
$$\begin{aligned} V_{IIP3,mix} &\propto \rho^{-\frac{3}{2}} \\ \rho &= \frac{R_{SW}}{R_S + R'_S + R_{SW}} \end{aligned} \tag{6.12}$$

However, as seen from the log scale plot of IIP3 versus R_{SW} in Fig. 6.6 (in case of optimal R'_S placement), the slope of IIP3 versus R_{SW} is less than 1.5. This could be because, while our architecture reduces the V_{GS} modulation to a large extent due to the virtual ground, it does not completely eliminate it.

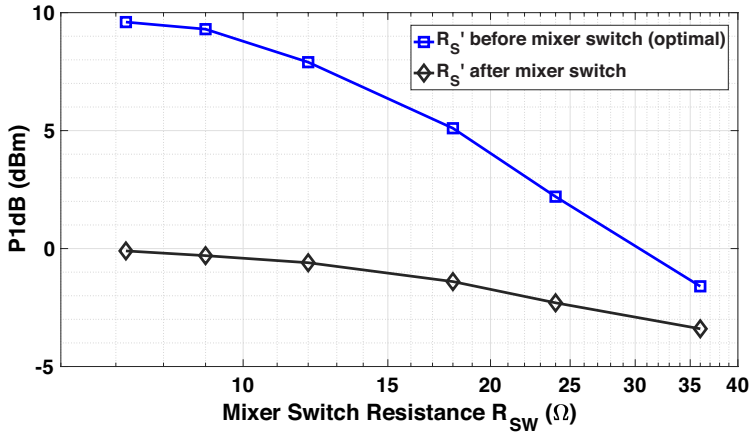
Thus far, we have shown simulation results using a 25% duty-cycled non-overlapping square wave LO to illustrate the benefits of reduced V_{GS} modulation of ON resistance of mixer switches. However, it is extremely challenging to synthesize such a waveform at the desired frequency of operation ($10 - 35$GHz). A commonly used technique to drive the gate

[4] R'_S is also swept to ensure that input match happens with the series combination of R'_S and R_{SW}, that is $R'_S + R_{SW}$ is maintained constant.

of the mixer switches at mm-wave frequencies is to use pseudo non-overlapping sinusoidal LO drive. However, with such a drive, while the source voltage of the mixer switch is held approximately a constant due to the virtual ground at the input of the baseband amplifier, the gate voltage varies throughout the ON phase of the LO. Therefore, there still exists V_{GS} modulation of ON resistance of mixer switches. Fig. 6.7 illustrates that the IIP3 and P1dB of the mixer switches drop significantly when driven by a sine wave LO (with same rail-rail swing), with a reduced slope for IIP3 versus R_{SW} as compared to the 25% non-overlapping square wave LO drive.



(a) Mixer Switch IIP3 v/s R_{SW}



(b) Mixer Switch P1dB v/s R_{SW}

Figure 6.6: Simulated IIP3 and P1dB ($f_{LO} = 20$GHz) of mixer switches for the two circuits shown in Figs. 6.5(a) and (b). The series resistor is placed before and after the mixer switch, in the two cases. The baseband is assumed to be perfectly linear for this simulation.

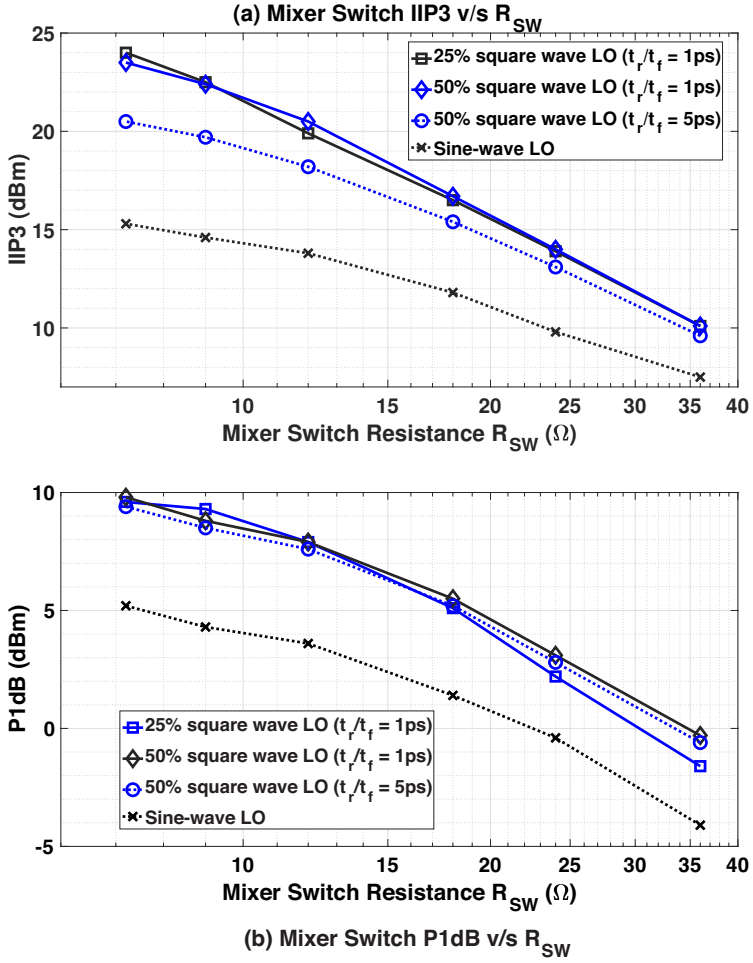


Figure 6.7: Simulated IIP3 and P1dB (f_{LO} = 20GHz) of mixer switches for the circuit shown in Fig. 6.5(a), for different LO drives. The different cases are 25% non-overlapping LO, 50% overlapping LO and pseudo non-overlapping sine wave drive. The LO swings from 0 to V_{DD} = 1.2V in each case. The baseband is assumed to be perfectly linear for this simulation.

While it may not be possible to synthesize a 25% duty-cycled non-overlapping LO waveform at mm-wave frequencies, it is definitely possible to synthesize 50% duty-cycled overlapping LO waveforms in the desired $10-35$GHz band, in the 28nm bulk CMOS node used in this work. The charge sharing issues associated with an overlapping LO [63] are dealt with subsequently. Fig. 6.7 shows the IIP3 and P1dB of the mixer switch versus mixer switch ON resistance for different LO drives: 25% duty-cycled non-overlapping LO with 1ps rise and fall times, 50% duty-cycled overlapping LO with 1ps rise and fall times, 50% duty-cycled overlapping LO with 5ps rise and fall times, and finally a pseudo-non-overlapping sine-wave LO with the same peak swing. The IIP3 is approximately the same for 25% and 50% duty-cycled LO drive, with the same rise and fall times (1ps). Therefore, there is no linearity

penalty for using a 50% duty-cycled LO compared to a more conventional 25% duty-cycled LO, which cannot be synthesized at these frequencies. As the rise and fall times of the LO waveform increase, the IIP3 starts reducing, as the V_{GS} modulation of ON resistance occurs for a larger fraction of the ON period. Therefore, it is desirable to make the transitions as sharp as possible, while designing the LO chain, to maximize IIP3.

Due to issues encountered with respect to convergence and the well-known BSIM4 model discontinuities [44], the IIP3 was simulated using transient simulations with relatively high input powers (> -10dBm) as the discontinuity would form a smaller fraction of the waveform at higher power levels [28, 44]. For completeness, P1dB simulation results are also provided. The P1dB simulation results exhibit similar trends as the IIP3 simulations, re-affirming the various concepts discussed in this section.

6.2.3 Noise and Charge Sharing

To analyze the noise figure of the traditional and proposed circuit and understand the various trade-offs, consider the LTI equivalent circuit shown of [36] in Fig. 6.8, which shows both the shunt re-radiation resistance R_{sh} and the overlap resistance R_{OL}. R_{OL} is used to capture the effects of charge-sharing due to LO waveform overlap. While deriving this LTI model, [36] makes some assumptions on the leakage current during the overlap, which do not hold for this work. However, the model suffices to gain some design insights. The noise figure (without considering amplifier noise) is given by

$$\begin{aligned} F &= 1 + \frac{R_{SW}}{R_S} + \frac{R'_S}{R_S} + \frac{R_{sh}}{R_S}\left(\frac{R_S + R'_S + R_{SW}}{R_{sh}}\right)^2 + \\ &\frac{R_{OL}}{R_S}\left(\frac{R_S + R'_S + R_{SW}}{R_{OL}}\right)^2 \\ R_{sh} &= \frac{8}{\pi^2 - 8}\left(R_S + R'_S + R_{SW}\right) \end{aligned} \tag{6.13}$$

The overlap resistance R_{OL} [36] is given by,

$$R_{OL} \propto \frac{R_{path}}{\tau_{overlap}\omega_{LO}} \tag{6.14}$$

where R_{path} is the resistance per path of the N-path mixer and $\tau_{overlap}$ is the overlap time of the LO [36].

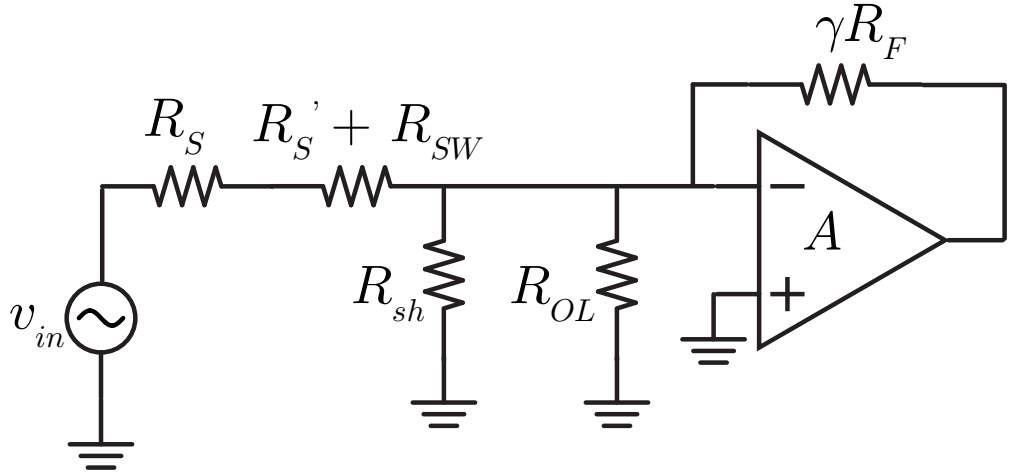


Figure 6.8: LTI equivalent circuit of the circuits in Figs. 6.1 and 6.10, showing shunt re-radiation resistance R_{sh} and overlap resistance R_{OL}. The values of R_{OL} are different for each of the circuits, depending on the nature of the LO driving the mixers.

Equations (6.13) and (6.14), in conjunction with the simulated noise figure plots in Fig. 6.9, may be used to explain the noise of different architectures for different LO drives. First consider the noise figure of the traditional N-path filter based architecture of Fig. 6.1 with $R_{SW} = 12\Omega$ (using transistors of dimension 27μm/30nm), driven by a 25% duty-cycled non-overlapping square wave LO ($R'_S = 0\Omega$ for the circuit in Fig. 6.1). The overlap resistance $R_{OL} = \infty\Omega$ for mixers driven by non-overlapping LO waveforms. A simulated DSB (double side-band) noise figure of $\sim$ 6.7dB is observed. The simulated noise figure includes contributions from the switch parasitics and the baseband noise which are not included in equation (6.13). Now, consider the circuits of Figs. 6.10(a) and (b), where an explicit series resistor R'_S is added for input matching. First, let us consider the scenario where the circuits in Fig. 6.10 are driven by a 25% duty-cycled non-overlapping LO, as opposed to the 50% duty-cycled LO shown in the figure. The circuit in Fig. 6.10(a) has one common R'_S for all the four paths, whereas the circuit in Fig. 6.10(b) has one R'_S in each path. Simulations show an increase in NF of 3.1dB for the circuit in Fig. 6.10(a) compared to the circuit in Fig. 6.1. This increase is due to the noise contribution of resistor R'_S, as well as additional losses that arise at high frequency from the RC network created by R'_S and the switch parasitic capacitance. Neglecting switch parasitics, an equal increase in noise figure is expected for both circuits when driven by a non-overlapping 25% duty-cycled LO. However, simulations show a further 0.3dB increase for the circuit in Fig. 6.10(b). This is due to the difference in the network formed by the series resistor R'_S and the parasitics in the two cases.

As discussed previously, it is extremely challenging to generate a 4-phase 25% duty-cycled non-overlapping square wave LO, but it is possible to generate a 4-phase 50% duty-cycled overlapping square wave LO for the desired 10–35GHz frequency of operation. When the mixers are driven by the LO waveform thus generated, there is I/Q charge sharing, which

degrades the noise figure [63].

The two circuits shown in Fig. 6.10(a) and (b) are indistinguishable when driven by a 25% duty-cycled non-overlapping LO, if the parasitics are neglected. However, when driven by a 50% duty-cycled overlapping LO, the noise figure of the circuit in Fig. 6.10(a) degrades by as much as 4.7dB (see Fig. 6.9) compared to 25% duty-cycled non-overlapping drive. By judiciously placing the explicit series termination resistance R'_S (see Fig. 6.10(b)), the degradation may be improved from 4.7dB to just 0.9dB. This mitigation is due to the reduced overlap leakage current, which in turn leads to a reduction of the charge sharing effect. For the circuit in Fig. 6.10(a), the overlap leakage current is proportional to $1/R_{SW}$, whereas for the circuit in Fig. 6.10(b), it is proportional to $1/(R_{SW} + R'_S)$.

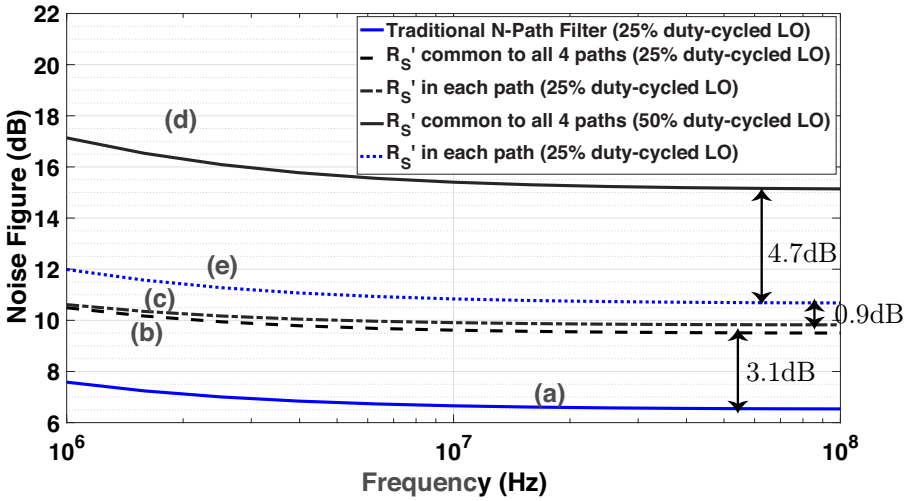


Figure 6.9: Simulated noise figure (f_{LO} = 20GHz) for the following cases (a) The circuit in Fig. 6.1 driven by non-overlapping 25% duty-cycled LO. (b) The circuit in Fig. 6.10(a) driven by non-overlapping 25% duty-cycled LO. (c) The circuit in Fig. 6.10(b) driven by non-overlapping 25% duty-cycled LO. (d) The circuit in Fig. 6.10(a) driven by overlapping 50% duty-cycled LO. (e) The circuit in Fig. 6.10(b) driven by overlapping 50% duty-cycled LO.

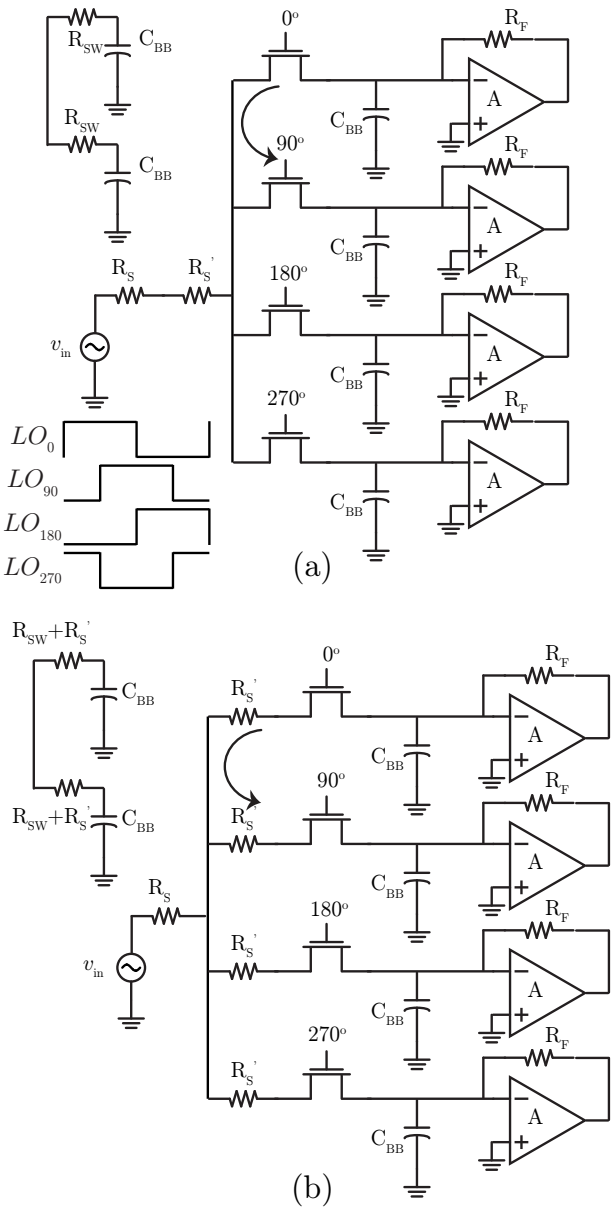


Figure 6.10: (a) Charge sharing problem due to LO overlap when driven by a 50% duty-cycled LO. (b) Mitigating charge-sharing.

Another way of looking at it based on equation (6.13) and the results of [36] is by using overlap resistance R_{OL} to denote the charge-sharing losses. The expression for R_{OL} is given by equation (6.14). R_{path} increases from R_{SW} in Fig. 6.10(a) to $R_{SW} + R'_S$ in Fig. 6.10(b). From equation (6.13), it is seen that higher R_{OL} lowers the noise figure. Fig. 6.11 illustrates the effect of $\tau_{overlap}$ and R'_S on the noise figure contribution of the mixer switch and the series resistance, for the circuit in Fig. 6.10(b). When driven by a 25% duty-cycled non-

overlapping LO, $R_{OL} = \infty\Omega$. Therefore, the noise figure increases with increasing R'_S as given by equation (6.13) and the results of [19]. However, with overlapping LO drive, there exists an optimum value of $R'_S + R_{SW}$ in terms of noise figure. Increasing series resistance increases the noise contribution from R'_S, but also increases R_{OL}, thereby decreasing the noise contribution due to the overlap.

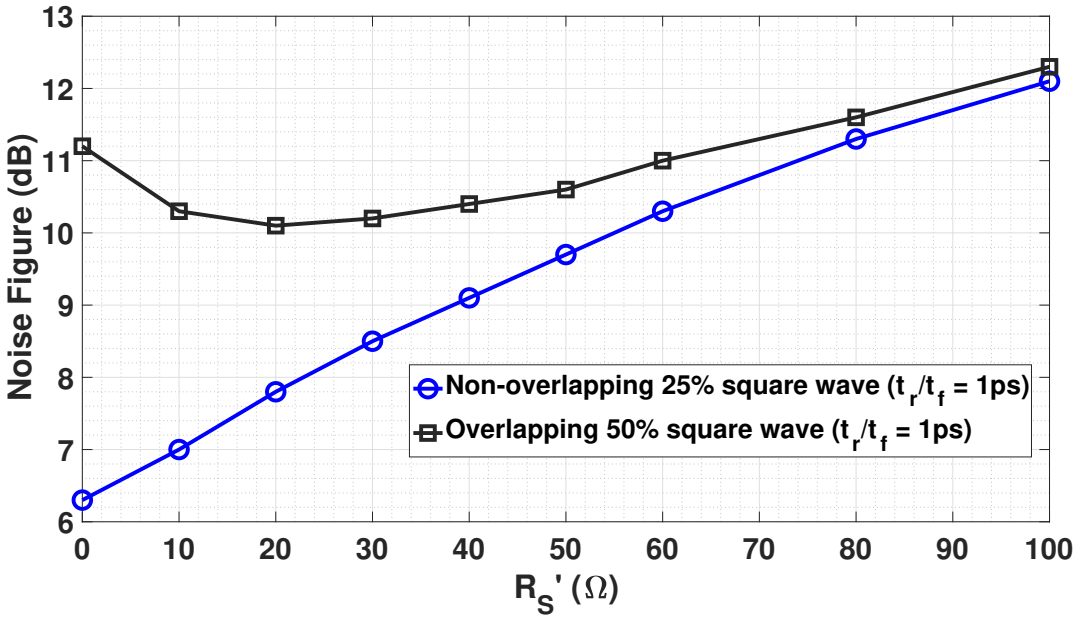


Figure 6.11: Simulated noise figure ($f_{LO} = 20$GHz) of the circuit in Fig. 6.10(b) versus series termination resistance R'_S for different cases of LO drive. For these simulations, the switch ON resistance (equal to 12Ω) is constant and corresponds to the actual switch used in the circuit.

The existence of an optimum $R'_S + R_{SW}$ for noise is similar to the existence of an optimal switch resistance in conventional N-path mixers with narrow-band input matching networks [19]. This reduction of charge sharing due to LO overlap is quite similar to the technique with series inductors proposed in [63]. However, the technique proposed in this work has a frequency invariant R'_S and occupies lesser area due to the use of an explicit resistance rather than an inductor as in [63].

6.2.4 Effects of LO Overlap on Baseband Non-Linearity

In the previous section, we discussed the issue of gain and noise figure degradation due to charge sharing arising out of LO overlap, and solutions to mitigate the same. In a similar vein, LO overlap also degrades the baseband non-linearity due to leakage between the I and Q channels [64]. Fig. 6.12 plots the simulated OIP3 of the two circuits in Figs. 6.10 (a) and

(b) versus the duty-cycle of the LO drive, for a value of feedback resistance $R_F = 1\text{k}\Omega$.[5] 25% duty-cycle implies zero LO overlap. The extent of LO overlap becomes higher with larger duty-cycle. To illustrate the effect of LO overlap on baseband non-linearity alone, ideal mixer switches are used in the simulation. Clearly, the LO overlap leads to a significant degradation in baseband non-linearity (more than 8dB degradation from 25% duty-cycle to 50% duty-cycle) for the circuit in Fig. 6.10(a), where R'_S is common to all four paths. The technique used for mitigation of charge-sharing also mitigates the baseband non-linearity degradation. For the circuit in Fig. 6.10(b), where R'_S is placed in each of the four paths, the degradation in baseband non-linearity is reduced significantly (see Fig. 6.12).

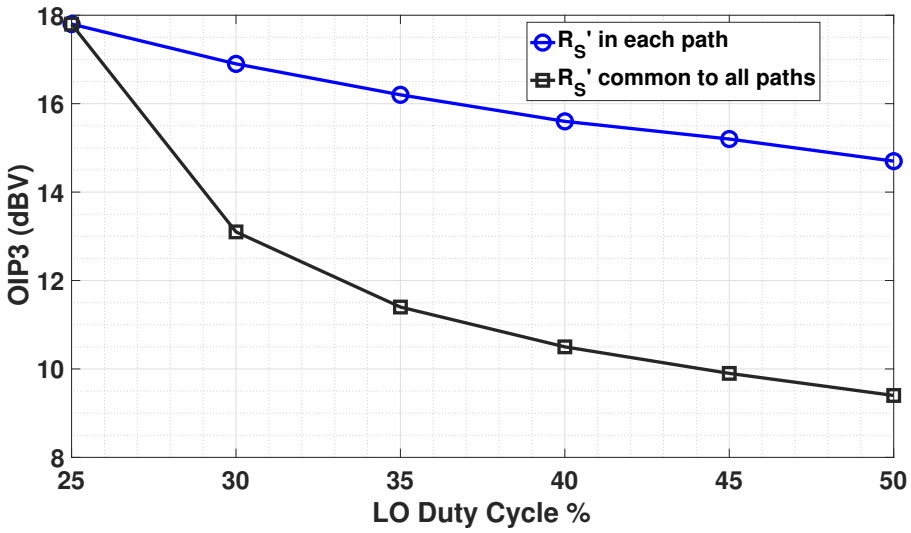


Figure 6.12: Degradation of baseband non-linearity due to LO overlap for the circuits in Figs. 6.10(a) and (b). The model used for the baseband amplifiers is the same as the one used for the simulation plot in Fig. 6.4, and is derived from the actual transistor implementation of the amplifier used in this work. The OIP3 is shown for $R_F = 1\text{k}\Omega$. In each case, an ideal mixer of switch ON resistance equal to 5Ω is placed in each of the four paths.

6.2.5 Input Matching Network

The parasitic capacitance of the mixer switches, bonding pad and ESD diodes degrade the noise figure [65], with greater degradation at higher frequencies. In this section, we discuss the input matching network to mitigate this degradation. Assuming that the mixer switch resistance R_{SW}, series resistance R'_S and the baseband resistance have been chosen appropriately to match to the input resistance R_S, Fig. 6.13 gives an approximate representation of the input matching network. The noise figure simulations thus far have included the effect

[5]Note the OIP3 is plotted instead of the IIP3 to normalize for the front-end losses which arise due to charge sharing.

of C_{par}, the parasitic capacitance ($\sim$ 110fF) of the mixer switches. Fig. 6.14 shows the insertion loss of the input matching network with C_{par} alone, and also with the capacitance of the probe pad (C_{PAD}) and the ESD diodes (C_{ESD}), in addition to C_{par}. C_{PAD} = 40fF and C_{ESD} = 120fF cause a further degradation in the insertion losses, which are reflected in the 1.7dB degradation in noise figure at f_{LO}=20GHz (see Fig. 6.15). To mitigate the losses due to C_{PAD} and C_{ESD}, a matching network using an artificial 50Ω transmission line may be created by inserting L_{match} between the pad and mixer. Obviously, this is a second order transfer function with a steep roll-off beyond the 3-dB bandwidth. Therefore, while it minimizes the insertion losses up to $\sim$ 38GHz compared to not having L_{match}, the losses are worse at higher frequencies (see Fig. 6.14). This improvement is also reflected in the improved noise figure at f_{LO}=20GHz (see Fig. 6.15).

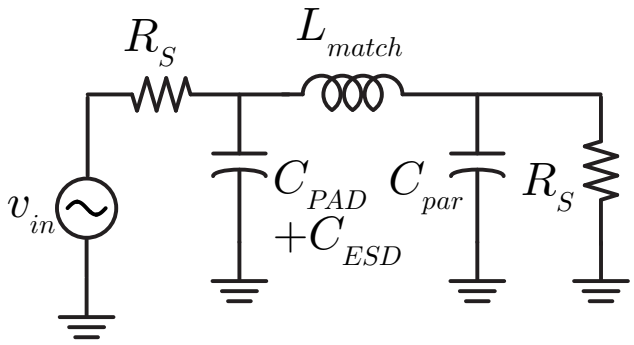


Figure 6.13: Schematic of the input matching network. The matching network includes pad and ESD capacitance and an additional inductor L-match added to reduce front-end loss, by forming a π-section T-line.

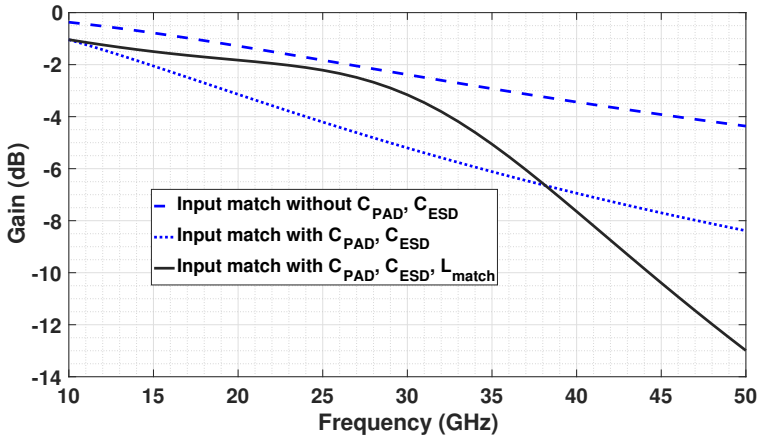


Figure 6.14: Input matching network losses.

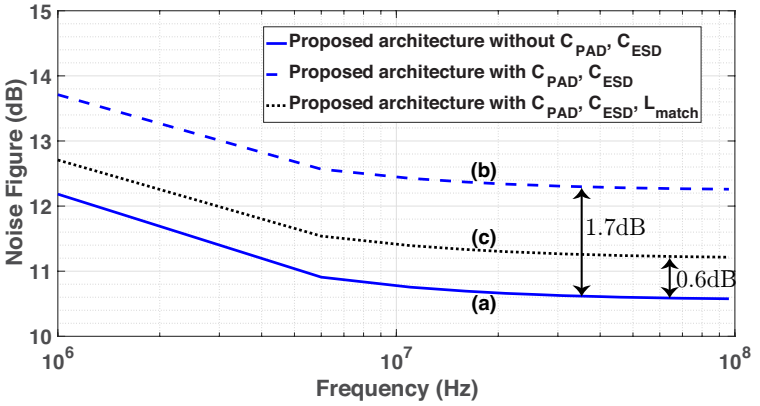


Figure 6.15: Simulated noise figure at f_{LO} = 20GHz (a) with only C_{par} (b) with C_{par}, C_{PAD}, C_{ESD} (c) with entire input matching network including L_{match}.

6.2.6 LO generation

The LO chain shown in Fig. 6.16 is used to generate the four-phase 50% duty-cycled overlapping LO required to drive the mixer switches. A single-ended off-chip LO input (nominally 0dBm) is converted to a differential signal using an on-chip balun. To compensate for the losses of the balun and the transmission line routing, an inverter based buffer is used.[6] A lumped implementation of a differential quadrature hybrid [42, 66] is used to generate the I/Q signals. In the differential quadrature hybrid implementation shown in Fig. 6.16, most of the capacitance comes from the parasitic capacitance of the inductors and the buffers before and after the quadrature hybrid. The quadrature hybrid is followed by an inverter chain to ensure rail-to-rail LO swing at the mixer gate input. To ensure low quadrature phase error across the entire bandwidth of interest, a small tunable capacitor bank is implemented. While this helps correct for phase error at different frequencies, there exists an amplitude mismatch between the four differential I/Q signals as seen from the small signal gain from the input to the four different LO outputs (see Fig. 6.17). However, our target is to have square wave LO drive for the mixer switches. The gain of the entire LO chain to all four I/Q mixer gates is high enough in the 10–35GHz frequency range to ensure that the LO swing "rails out" for a 0dBm input LO power, ensuring square wave drive. Fig. 6.18 shows the simulated amplitude imbalance and phase difference between the differential I and Q outputs for the small signal conversion gain from the RF input to the baseband output. For each f_{LO}, the capacitor bank of the quadrature hybrid was suitably adjusted to ensure phase difference as close to 90° as possible. With suitable settings, it is observed that the simulated I/Q phase error is less than ±1° across 10–35GHz and the amplitude imbalance is less than 0.15dB.

[6]Note that this buffer may not be necessary if the LO input power is higher or if a differential on-chip local oscillator with sufficient output swing is used to synthesize the LO.

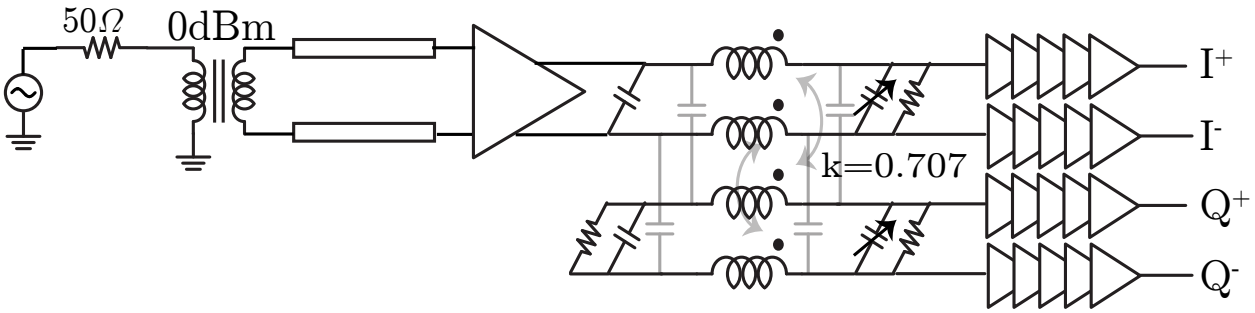


Figure 6.16: Schematic of LO chain.

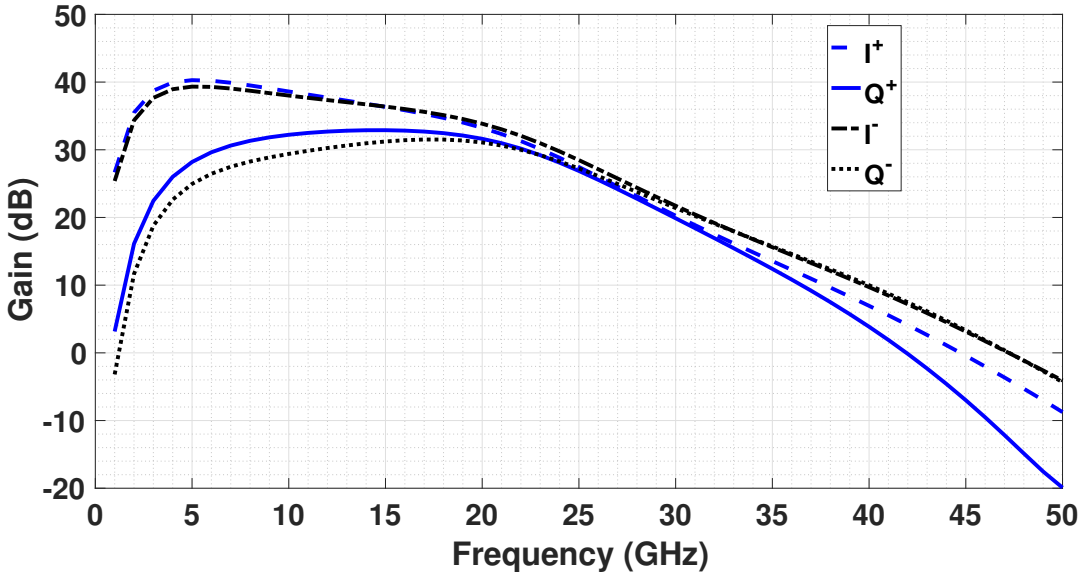


Figure 6.17: Small signal gain of the LO chain from LO input to the four gates of the I/Q mixer switches.

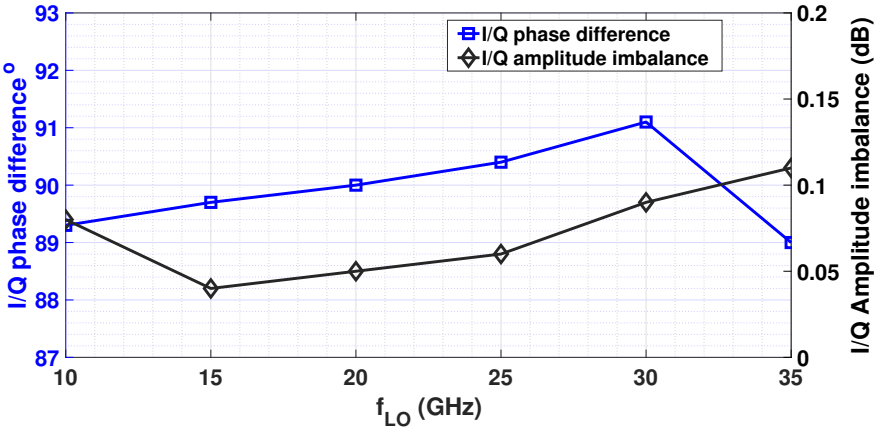


Figure 6.18: Simulated I/Q amplitude and phase imbalance for differential baseband outputs.

6.3 Measurement Results

A test chip was fabricated in a 28nm bulk CMOS process and wire-bonded directly onto PCB (see Fig. 6.19). The RF and LO inputs were probed using GSG probes.

The feedback resistance R_F in Fig. 6.10 is programmable, so that the chip may be used over a wide range of gain and linearity settings. Fig. 6.20 shows the measured voltage conversion gain and input matching for f_{LO} varying from 15GHz to 30GHz in steps of 5GHz, for a setting of $R_F = 1\text{k}\Omega$. An RF bandwidth of 400MHz was achieved for this gain setting. The s_{11} is less than -10dB across f_{LO}, and is largely flat across frequency due to the use of an explicit series resistor R'_S for matching.

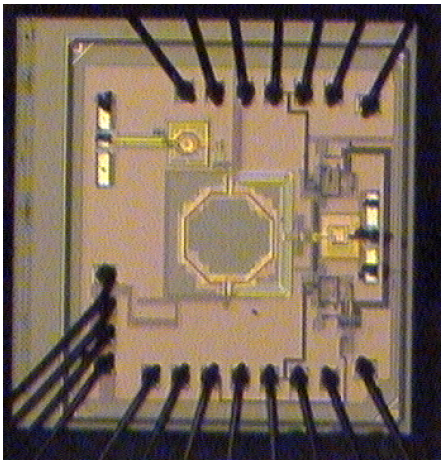


Figure 6.19: Die micrograph of 28nm bulk CMOS prototype of receiver front-end.

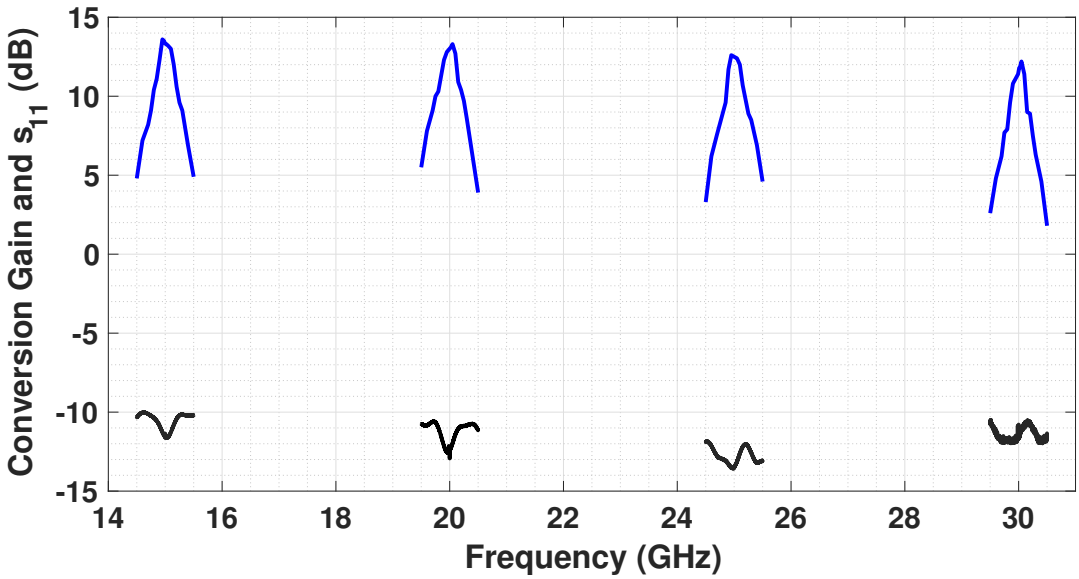


Figure 6.20: Measured conversion gain and input match for $R_F = 1\text{k}\Omega$ versus frequency for four different f_{LO}.

Fig. 6.21 and Fig. 6.22 show the measured conversion gain and noise figure for f_{LO} varying from 10–35GHz, for two different settings of feedback resistance R_F, 1kΩ and 2kΩ. As expected, conversion gain for $R_F = 2\text{k}\Omega$ is around 5dB higher than that for $R_F = 1\text{k}\Omega$, and drops with f_{LO}. The increased conversion gain at $R_F = 2\text{k}\Omega$ comes at the cost of RF bandwidth reducing from 400MHz to 240MHz. Also, there is a discrepancy of >1.5dB between the simulated and measured conversion gain, which may be explained by probe losses and underestimation of input parasitic capacitance. For the higher linearity setting of R_F equal to 1kΩ, a NF of 12.5 to 15.7dB was measured for f_{LO} varying from 10–30GHz. The noise figure is lower by about 0.4dB for $R_F = 2\text{k}\Omega$. The simulated NF for $R_F = 1\text{k}\Omega$ varies from 10.8 to 14.3dB for f_{LO} varying from 10–35GHz. The discrepancy of >1.5dB may be explained by probe losses and inaccurate noise models. The steep jump in measured noise figure from 30 to 35GHz may be attributed to higher parasitic capacitance. Fig. 6.14 shows the input matching network loss as a function of frequency, and the higher order transfer function of the input matching network leads to a steeper roll-off with frequency. For higher parasitics than simulation, the roll-off starts at a lower frequency, explaining the bigger discrepancy between simulated and measured noise figure at $f_{LO} = 35\text{GHz}$.

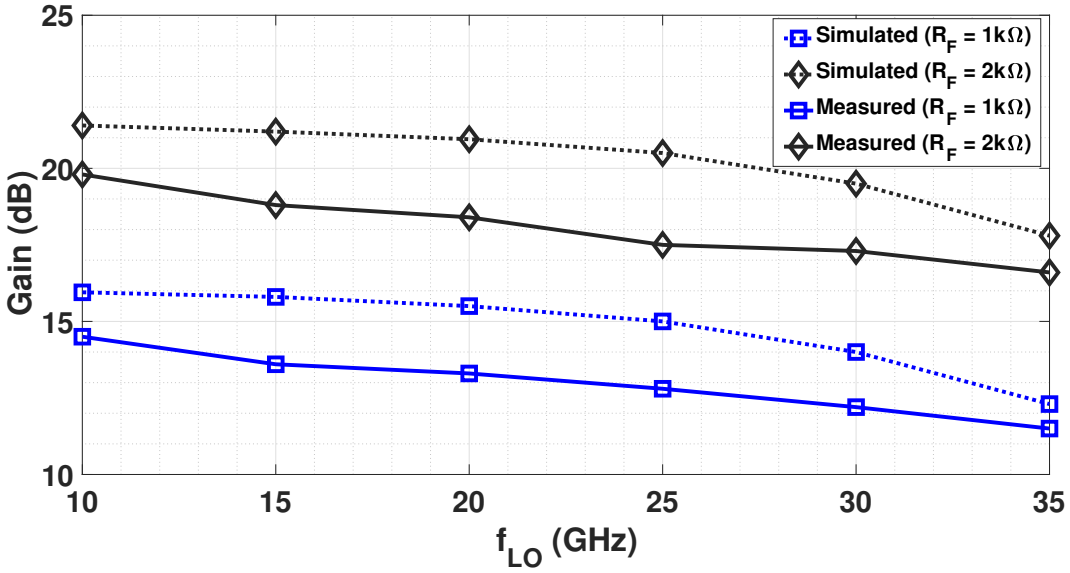


Figure 6.21: Measured and simulated gain versus f_{LO} for $R_F = 1\text{k}\Omega$ and $R_F = 2\text{k}\Omega$.

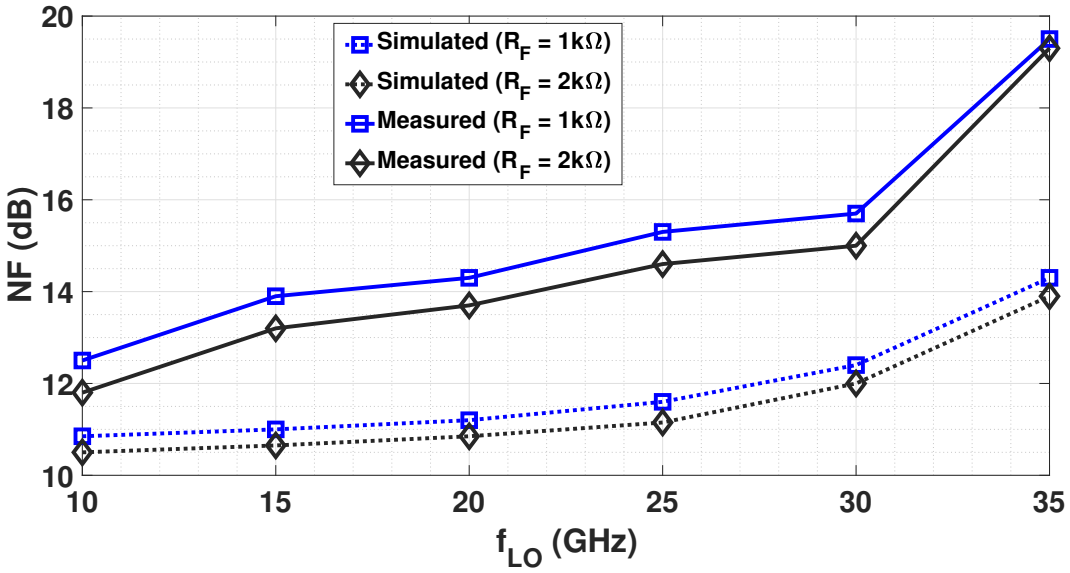


Figure 6.22: Measured and simulated noise figure versus f_{LO} for $R_F = 1\text{k}\Omega$ and $R_F = 2\text{k}\Omega$.

A 2-tone test was performed to characterize the IIP3 of the receiver front-end (for $R_F = 1\text{k}\Omega$), with one tone at $f_{LO} + f_{OS} + 40\text{MHz}$ and another tone at $f_{LO} + 2f_{OS} + 40\text{MHz}$, with the IM3 tone falling at $f_{LO} + 40\text{MHz}$. Fig. 6.23 plots the IIP3 as a function of tone offset. In

traditional mixer-first receivers, which are used to enhance out-of-band RF selectivity, the IIP3 increases considerably for tones at higher offset from f_{LO} [30]. However, in this case, the IIP3 is almost constant for f_{OS} within the baseband bandwidth (that is, for in-band blockers), due to the use of an explicit resistor for matching. There is a slight drop for f_{OS} outside the band, which may be explained by the reduction of loop gain in the baseband amplifier, and hence reduced benefits of feedback linearization. IIP3 numbers as high as +14dBm show that we have indeed derived benefit both from feedback linearization and the improved mixer switch linearity.

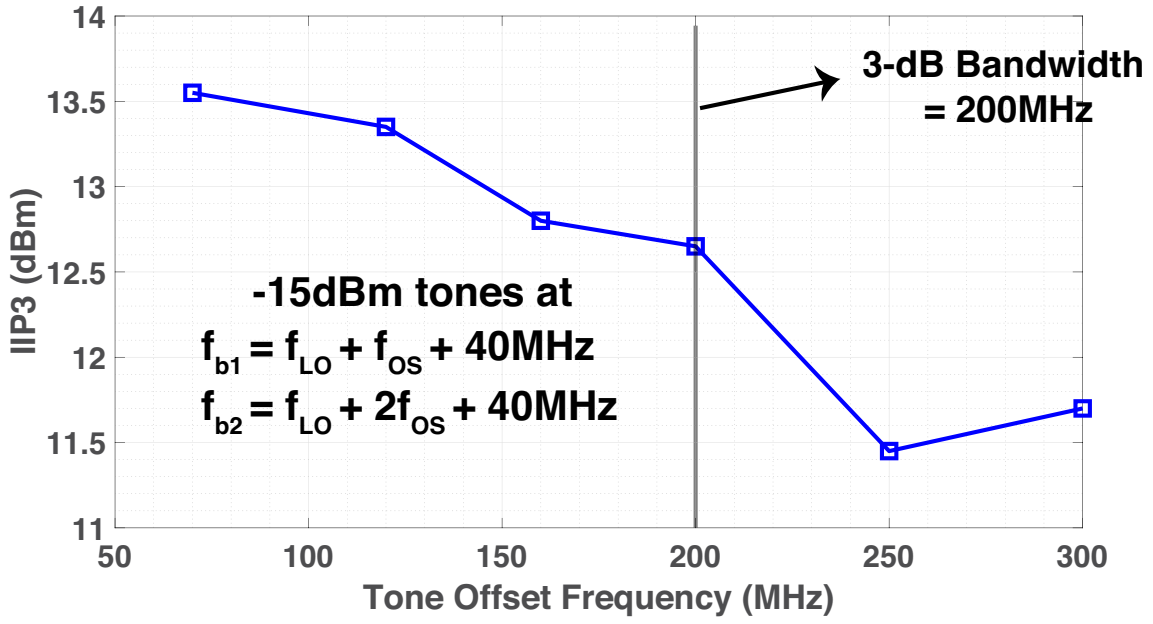


Figure 6.23: Measured IIP3 as a function of tone offset for $f_{LO} = 20$GHz for $R_F = 1$kΩ.

Fig. 6.24 shows the conversion gain and in-band IIP3 across f_{LO} for $R_F = 1$kΩ. The in-band IIP3 is largely flat up to $f_{LO} = 30$GHz, varying between +12dBm and +14dBm. The drop to +10dBm at 35GHz is likely due to less "square" LO drive, and hence reduce mixer linearity. Figs. 6.25 and 6.26 show P1dB measurements. Measured input P1dB and output OP1dBV are plotted versus f_{LO} for R_F equal to 1kΩ and 2kΩ in Fig. 6.25. The higher OP1dBV for R_F equal to 1kΩ (lower closed loop gain) illustrates the benefit of feedback linearization and shows that we are not just giving up closed loop gain for P1dB dB for dB.

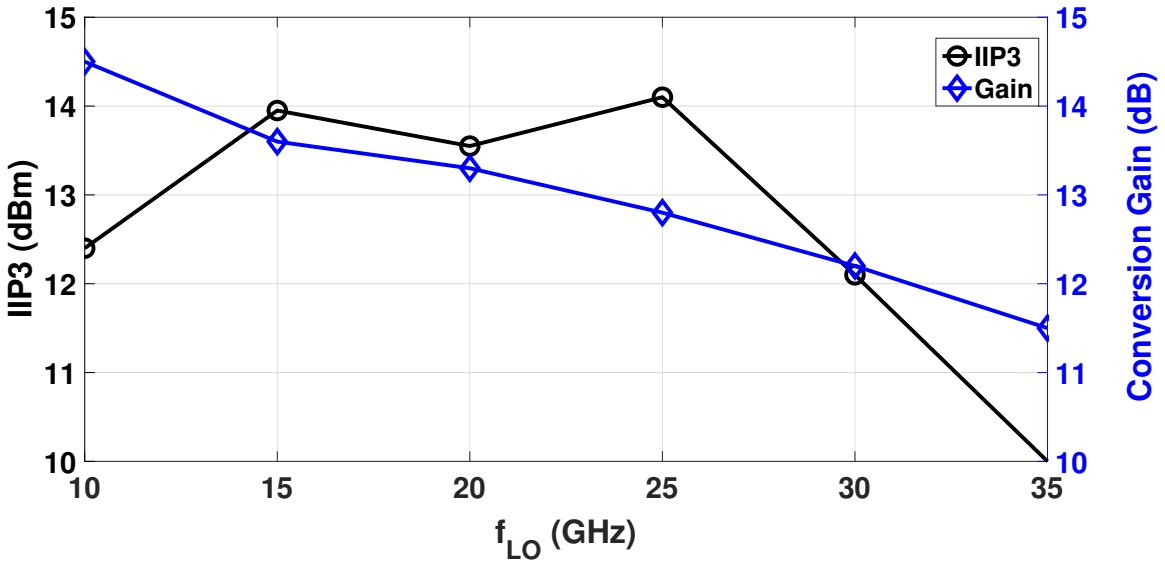


Figure 6.24: Measured conversion gain and in-band IIP3 versus f_{LO} for $R_F = 1\text{k}\Omega$.

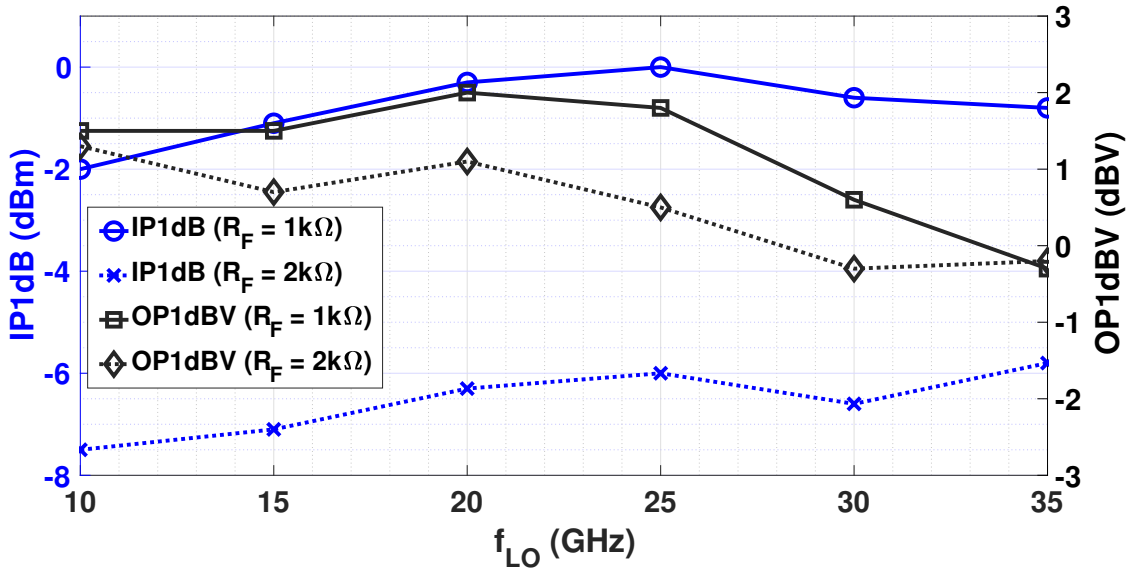


Figure 6.25: Measured IP1dB and OP1dBV versus f_{LO} for $R_F = 1\text{k}\Omega$ and $R_F = 2\text{k}\Omega$.

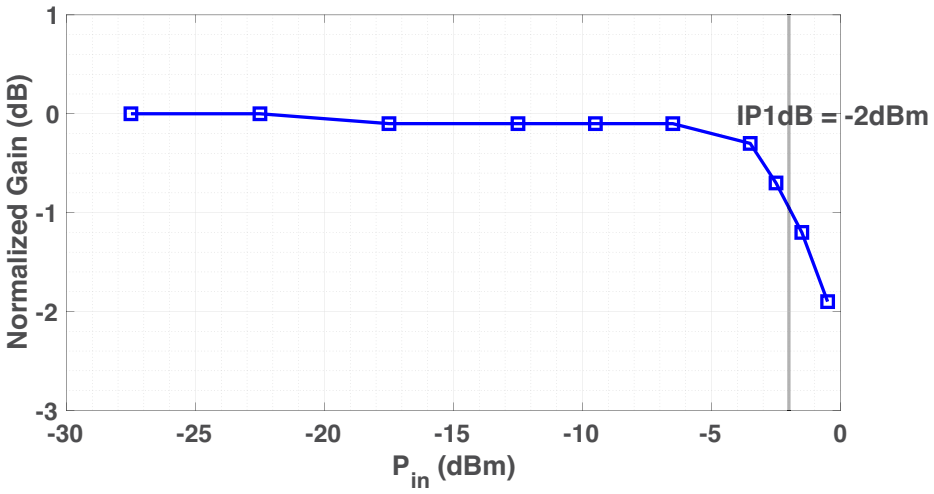


Figure 6.26: Normalized measured gain versus input power P_{in} for $R_F = 1k\Omega$ at $f_{LO} = 10GHz$.

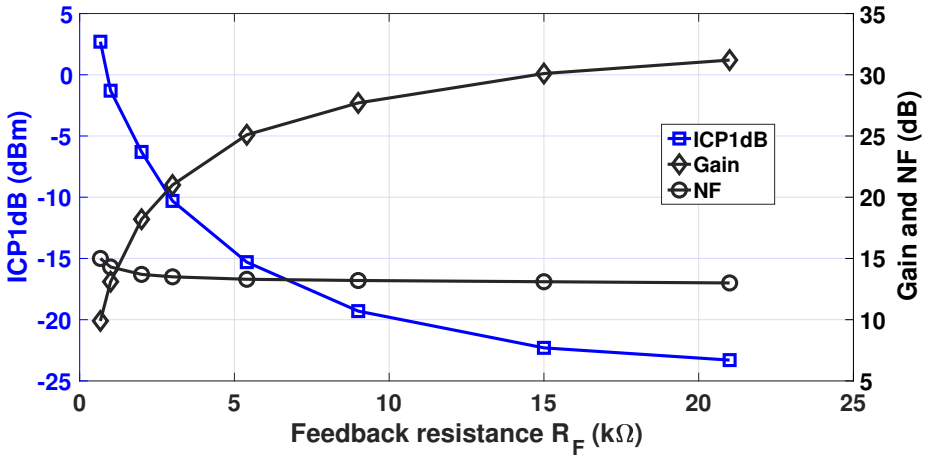


Figure 6.27: Trade-off between P1dB, Gain and NF versus feedback resistance R_F. (Measured)

Fig. 6.27 illustrates the trade-offs between P1dB, gain and NF as the feedback resistance R_F is changed. The benefit of feedback linearization may be inferred from the following observations. In Fig. 6.27, when R_F is reduced from 9kΩ to 5.4kΩ, the gain drops by less than 3dB, but the P1dB increases by more than 4dB. The increase in P1dB by a factor approximately 1.5× the gain shows that we are benefitting from feedback linearization. Additionally, while R_F is reduced from 15kΩ to 667Ω, the gain drops by around 20dB, while the P1dB increases by 26dB. It may be noted from the plot that for R_F as low as 667Ω,

the P1dB (+3dBm) continues to increase without trailing off. This shows that the mixer P1dB is higher than +3dBm, validating our techniques to increase mixer switch linearity. Of course, the noise figure does increase with reducing R_F, but the penalty is quite low up to values of R_F equal to 1kΩ, as R_F is not the dominant noise source.

6.4 Conclusion

Table 6.1 compares this work against the state-of-the-art mixer-first receivers operating at greater than 10GHz. While the modest noise figure of our receiver was a choice based on utilization in massive digital MIMO arrays, it may be seen that the IP1dB of 0dBm is an order of magnitude better than the next best receiver. While most previously publications do not directly report IIP3, +14dBm of in-band IIP3 is achieved in this work and is 16dB higher than the state-of-the-art. Also, the OP1dBV is significantly better than the state-of-the-art mixer-first receivers operating at greater than 10GHz. Finally, the broadband operation from 10–35GHz is among the highest fractional bandwidth reported in mm-wave mixer-first receivers.

Table 6.2 compares this work against other works intended for the 28GHz band. Most of the work in Table 6.2 have LNA front-ends, and are RF-phase-shifter-based systems. Therefore, while they do achieve considerably lower noise figure, they are not capable of broadband operation. Also, [23, 24, 67] have significantly lower linearity due to the use of vector interpolator based active phase shifters. [25], which uses transmission line based passive phase shifters, also shows lower linearity. The receiver front-end presented in this work could also be re-purposed for use in smaller sized phase arrays, in which case an LNA-based front-end is required. To illustrate this point, we consider the LNA from [23] driving the passive-mixer front-end described in this work. The LNA in [23] had a post-layout simulated gain of 25dB, noise figure of 3.6dB and ICP1dB of -3.2dBm at 28GHz. The last column of Table 6.2 shows the calculated performance specifications of the aforementioned LNA driving the front-end proposed in this work. The competitive performance metrics of such a front-end indicate that our work is suitable for use in an LNA-based front-end for arrays with lower number of elements.

To summarize, this work demonstrates a wideband highly linear mixer-first receiver front-end for massive digital arrays. As the array relaxes the noise requirement, feedback linearizaton at baseband was proposed to enhance linearity at the cost of noise. The limitations of feedback linearization were also highlighted. Techniques were proposed to enhance the linearity of mixer switches at mm-wave frequencies using overlapping square wave drive, and solutions were proposed to address the issue of charge sharing arising from the use of the same.

Table 6.1: Comparison with mixer-first receivers greater than 10GHz

	Moroni [68] RFIC 2012	**Wilson** [69] RFIC 2016	**Ying** [70] ESSCIRC 2017	**Iotti** [42] JSSC2020	**Boynton** [71] RFIC2020	**Ahmed** [72] CICC2020	**This work**
Technology	65nm CMOS	45nm SOI	130nm HBT	28nm CMOS	65nm CMOS	22nm FD-SOI	**28nm CMOS**
f_{RF} (GHz)	49 – 67	20–30	0.3 – 12	70 – 100	9 – 31	43 – 97	**10 – 35**
Voltage gain (dB)	13	8 – 20.6	3 – 5	19.5 – 25.3	45	12 – 15	**10 – 31** (20GHz) [*]; **11.5 – 14.5** [†]
IP1dB (dBm)	-12	-9.3 – -13	-20 – -40	-16.8 – -24	-45	-5.6 – -8	**-2 – 0** [†]
Best case OP1dBV	-10	-3.4	-26	-8.3	-11	-4	**1.5**
In-band IIP3 (dBm)	-	-2.3 – -9.7	-	-	-	0 – +4	**+10 – +14.1** [†]
NF (dB)	11–14	8	10	8 – 12.7	12.5 – 17.5	12.5 – 16.5	**12.5 – 19.2** [♯]
DC power (mW)	14	41 (at 24GHz)	1200 – 1300	12	72	36	**22.8** (Baseband); **19 – 37** (LO)
Supply (V)	1.2	0.9/1.8	-	1	-	-	**1.2**

[*] Measured gain at 20GHz across different gain settings.
[†] Measurements reported at nominal setting ($R_F = 1\text{k}\Omega$), across f_{LO}.
[♯] NF varies from 12.5 – 15.7 dB for $f_{LO} = 10 - 30$GHz.

Table 6.2: Comparison with recently published 28GHz receiver front-ends

	Yeh [67] RFIC 2016	**Kibaroglu** [24] RFIC 2017	**Mondal** [23] JSSC2019	**Sadhu** [25] JSSC2017	**This work**	**This work with LNA front-end (calculated)**
Technology	120nm SiGe	180nm SiGe	65nm CMOS	130nm SiGe	**28nm CMOS**	**28nm CMOS**
f_{RF} (GHz)	28-32	28-32	28/37	28	**10 – 35**	**28**
Voltage gain (dB)	9.4	20	33/26.5	34	**11.5 – 14.5**	**37.5**
IP1dB (dBm)	-16 – -13	-22	-30/-24	-22.5	**-2 – 0**	**-25.5**
Best case OP1dBV (dBV)	-14.6	-13	-8	-1.3	**1.5**	**-3**
NF (dB)	5.1	4.6	7.3	6	**12.5 – 19.2**[♯]	**3.8**
DC power (mW)	136.5	130	52.5	103.1	**22.8** (Baseband); **19 – 37** (LO)	**66**

[♯] NF varies from 12.5 – 15.7 dB for $f_{LO} = 10 - 30$GHz.

Chapter 7

Conclusions and Future Work

In this dissertation, we have provided circuit-level solutions to address the increasing interference that comes with the advent of the IoT and 5G revolution. Specifically, we have demonstrated several interference-resilient receiver front-ends for three separate application thrusts: sub-mW IoT, sub-6GHz 5G and mm-wave digital beam-forming applications. In this chapter, we provide the key takeaways from each of these works and describe future avenues for extending this research.

7.1 sub-mW IoT applications

In this dissertation, we have shown the pathway to building sub-mW interference resilient radio receivers for internet-of-things (IoT) applications, by having an N-path filter in shunt with a power-efficient LNA front-end. The consequent trade-off between input matching, noise figure and out-of-band filtering was solved in a power-efficient manner using N-path filter based translational positive feedback. We have demonstrated record out-of-band IIP3 compared to the state-of-the-art sub-mW 2.4GHz receiver front-ends. However, the noise figure and sensitivity are quite modest compared to the state-of-art sub-mW receivers.

One potential direction of future research would be to enhance the noise performance of this receiver front-end without compromising on interference resilience. Recently, noise cancellation at sub-mW powers was demonstrated in [35]. The mutual noise cancellation technique could be integrated with shunt N-path filters to enhance the noise figure while maintaining similar out-of-band IIP3. Another potential research direction could be to enhance the out-of-band IIP3 by leveraging the technique of implicit capacitive stacking in N-path filters demonstrated by [38].

7.2 sub-6GHz 5G applications

In this dissertation, we have provided a pathway to the SAW-less CMOS receiver by building enhanced N-path filters with higher order RF selectivity. We have shown N-path filters

with 40dB/decade and 60dB/decade RF selectivity using N-path filters loaded by driving point impedances with 40dB/decade and 60dB/decade roll-off respectively. Through the course of this dissertation, we have also shown the first-ever synthesis of a driving point impedance with 60dB/decade roll-off. Through passive cascade of N-path filters, we have also demonstrated N-path filters with up to 80dB/decade RF selectivity. We have demonstrated partial distortion cancellation in the amplifiers used in the synthesis of these higher order impedances. Putting all these together, we were able to demonstrate SAW-like channel selectivity and record large-signal blocker resilience for close-in blockers.

There are several promising avenues of future research to build on the work done in this dissertation. One "low hanging fruit" would be to leverage the benefits of using better technology than the 28nm-bulk CMOS used in this dissertation. FinFETs have significantly lower body-effect [73]. Therefore, the variation of threshold voltage (and consequently switch ON resistance) due to the bulk-source voltage is significantly lower, promising higher switch IIP3. Bottom-plate mixing demonstrated in [29] showed some of these benefits regarding switch IIP3, however the large parasitic capacitance at the RF node makes the front-end losses prohibitively high for frequencies greater than a few GHz. Use of FinFETs has the potential to yield similar benefits as bottom-plate mixing for switch IIP3 without the penalty of the large parasitic capacitance in bottom-plate mixing. Use of fully depleted silicon-on-insulator (FDSOI) technology with higher transit frequency f_T [74, 75] can help extend some of the techniques described in this work to higher frequencies. The back-gate biasing in FDSOI could help lower threshold voltages, and consequently switch ON resistances for the same switch size. Therefore, higher switch IIP3 could be obtained without the penalty of higher switch parasitics and losses from larger switches.

One major problem inhibiting wider acceptance of passive-mixer first receivers as a replacement for SAW filters is the reciprocal mixing due to LO phase noise. In the receivers in this dissertation, the on-chip LO chain was designed to have a simulated phase noise of -170dBc/Hz at 100MHz offset for f_{LO} of 1GHz. The challenges of designing an LO chain with such strict specifications are detailed in [76]. In all the works in this dissertation, the LO and blocker signals were filtered using sharp SAW filters to ensure that only the phase noise of the on-chip LO chain dominates. However, in an actual receiver system, the on-chip VCO must have a phase noise much lower than -170dBc/Hz at 100MHz offset for f_{LO} of 1GHz. Assume that a VCO phase noise of -180dBc/Hz at 100MHz (f_{LO} = 1GHz) is required in order not to degrade the total phase noise significantly when cascaded with the rest of the LO chain. This translates to a challenging LC-VCO design with a FoM of 190dB at a power consumption of 10mW. However, LC-VCOs have a limited tuning range and multiple VCOs are required to support the entire range of sub-6GHz bands. Ring-oscillators with much wider tuning ranges are more amenable for broadband receivers. However, it was shown in [77], that the maximum achievable FoM in ring-oscillators is around 165dB. To meet a similar phase noise specification as the LC-VCO with 190dB FoM, the ring-oscillator must consume prohibitively high power, approximately 300× more than the 10mW LC-VCO. [76] provides some direction towards phase noise cancellation but a lot remains to be done in order to solve the problem of reciprocal mixing.

There are several other avenues of research to build on the work presented in this dissertation. Yet another "low-hanging" fruit would be to build N-path filters with 100dB/decade and 120dB/decade RF selectivity through the passive cascade of two higher order N-path filters. The distortion cancellation scheme presented in this dissertation canceled only the distortion generated by the amplifier used to synthesize the negative RC impedance. Optimizing this distortion cancellation to cancel the distortion of the gyrator would be another natural extension of this work. However, the distortions from the "negative gyrator" and the negative RC amplifier have different transfer functions to the output. So, a more thorough analysis is required in order to simultaneously cancel the distortion of the "negative gyrator" as well. It was shown in [55] that the synthesis of driving point impedances with 40dB/decade and 60dB/decade roll-off, like the ones presented in this dissertation, is not possible with passive elements alone. From an electrical network theory standpoint, it would be interesting to investigate if driving point impedances with 80dB/decade and higher roll-off can be synthesized, and if it is possible to come up with a generic procedure to synthesize higher order driving point impedances with active elements. Another problem worth investigating is the use of N-path filters in transmitters. N-path filters at the output of power amplifiers are promising for filtering but contribute to insertion loss. While [78] has demonstrated a transmitter with a second order N-path filter (followed by a power amplifier), a lot remains to be done in terms of investigating the trade-offs between N-path filter based transmitters versus baseband filters followed by transmit mixers.

7.3 Mm-wave digital MIMO applications

The last part of this dissertation demonstrated a highly linear receiver front-end for mm-wave digital MIMO applications. The in-band linearity was enhanced at baseband using feedback linearization. Techniques were proposed to enhance mixer switch linearity at mm-wave frequencies using series resistors and overlapping square wave LO waveforms to drive the mixer switches. Techniques were also proposed to mitigate charge sharing resulting from overlapping LO waveforms. While this dissertation focused on implementing these techniques for frequencies up to 35GHz, the frequency range of this work may easily be extended by using technology like 22nm FD-SOI with higher f_T (and lower switch $R_{on}C_{off}$ products). Use of FD-SOI would not only help mitigate losses in the signal path at frequencies higher than what was shown in this dissertation, but also aid in the generation of square wave LO waveforms for higher frequencies.

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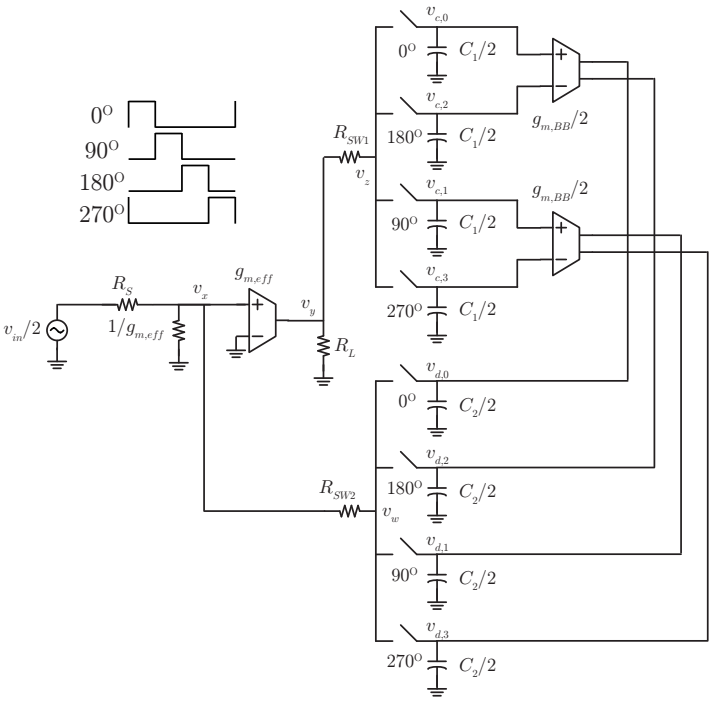
Appendix A

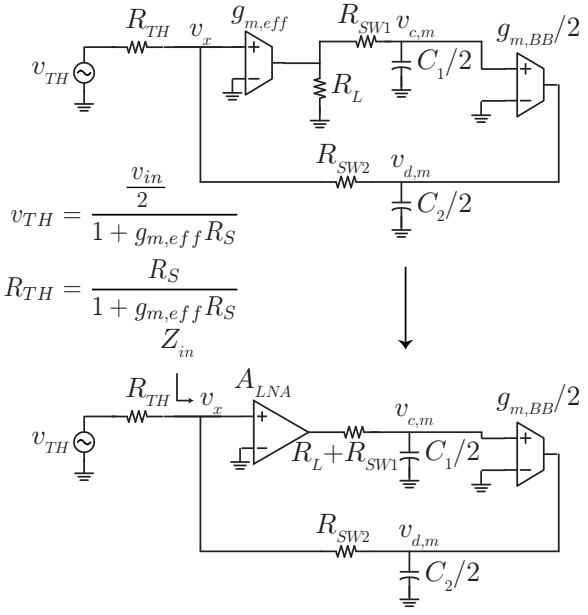
Analysis of Impedance Matching in Receivers with Translational Feedback

The LTI equivalent circuit of the receiver front-end described in Chapter 2 is derived in detail, for two cases – broadband and narrowband input matching network. The circuit, shown in Fig. A.1, has two 4-phase switched RC kernels. Both of them operate in the "mixing region" defined in [15], [17] and [16]. Therefore, we may analyze this circuit in a manner similar to [19], by assuming that for the entire T_{LO}, both $v_{c,m}$ and $v_{d,m}$ (See Fig. A.1(a)) are approximately constant, where m indicates which phase of the LO is on, and the charge dissipated through any resistive load at $v_{c,m}$ and $v_{d,m}$ is replenished when the m^{th} phase of the LO is on. It may be noted that the common-gate LNA in Fig. A.1 is replaced by its equivalent input resistance $1/g_{m,eff}$ and a common-source LNA with the same transconductance. This simplifies the subsequent derivations. Also, the input source, transformed source resistance and the input resistance of the CGLNA, are replaced by their Thevenin equivalent.[1]

[1]The Thevenin equivalent splits the circuit into two parts, one containing only a signal at the fundamental and the other containing signals at both the fundamental and harmonics, allowing this circuit to be analyzed in a similar fashion to the one in [19], even in the case of $R_{SW2} = 0\Omega$.



(a) Half-Circuit



(b) Half-Circuit during LO phase m

Figure A.1: Equivalent half-circuit of the schematic in Fig. 2.3(b), and the representation of the circuit during phase m of the LO. The CC-CGLNA is replaced by its input impedance $1/g_{m,eff}$ and a high input-Z transconductance $g_{m,eff}$ with load R_L.

Consider the RF input at $\omega_{RF} = \omega_{LO} + \omega_{IF}$, given by

$$v_{in}(kT_{LO} + \tau) = A\cos((\omega_{LO} + \omega_{IF})(kT_{LO} + \tau)) \tag{A.1}$$

where A is amplitude of the input RF signal. Without repeating much detail, we try to arrive at expressions for $v_{d,m}$ and $v_{c,m}$ similar to the expressions in equations (4) and (26) of [19]. When the m^{th} switch is closed, we perform a charge balance at the two nodes $v_{c,m}$ and $v_{d,m}$, of the schematic shown in Fig. A.1(b). Consider the charge balance at node $v_{d,m}$, over a quarter LO period,

$$\begin{aligned}\left(-\frac{g_{m,BB}}{2}v_{c,m} + \frac{v_{d,m}}{2Z_{C_2}}\right)T_{LO} = \\ \int_{mT_{LO}/4 - T_{LO}/8}^{(m+1)T_{LO}/4 - T_{LO}/8} \frac{v_{TH} - v_{d,m}}{R_{TH} + R_{SW2}}dt\end{aligned} \tag{A.2}$$

Now, from charge balance at $v_{c,m}$, we have

$$\frac{v_{c,m}}{2Z_{C_1}}T_{LO} = \int_{mT_{LO}/4 - T_{LO}/8}^{(m+1)T_{LO}/4 - T_{LO}/8} \frac{A_{LNA}v_x - v_{c,m}}{R_L + R_{SW1}}dt \tag{A.3}$$

Here, it is important to note that v_x is a linear combination of $v_{d,m}$, which is approximately constant for T_{LO}, and v_{TH} which is the scaled RF input at the antenna. That is,

$$v_x = \frac{R_{TH}\ v_{d,m} + R_{SW2}\ v_{TH}}{R_{TH} + R_{SW2}} \tag{A.4}$$

When $R_{SW2} \approx 0\Omega$, v_x is now

$$v_x = v_{d,m} \tag{A.5}$$

Jointly solving the charge balance equations in (A.3) and (A.2), using (A.5), we have the following expressions for $v_{c,m}$ and $v_{d,m}$.

$$\begin{aligned}v_{d,m} &= \frac{2\sqrt{2}}{\pi}\frac{2Z_{C2}||\frac{-2}{A_{LNA}g_{m,BB}k_1}}{2Z_{C2}||\frac{-2}{A_{LNA}g_{m,BB}k_1} + 4R_{TH}} \times \\ &\frac{A}{1 + g_{m,LNA}R_S}\cos\left(\omega_{IF}T_{LO}\left(k + \frac{m}{4}\right) + \frac{m\pi}{2}\right) \\ v_{c,m} &= A_{LNA}k_1 v_{d,m}\end{aligned} \tag{A.6}$$

where k_1 is given by

$$k_1 = \frac{Z_{C1}}{Z_{C1} + 2\left(R_L + R_{SW1}\right)} \tag{A.7}$$

Now, by reconstructing v_x, which is equal to $v_{d,m}$ for $m = 1$ to 4, and computing the Fourier coefficient of the fundamental component of v_x at ω_{RF}, we have

$$v_x(\omega_{RF}) = v_{TH}(\omega_{RF}) \frac{8}{\pi^2} \frac{2Z_{C2}||\frac{-2}{A_{LNA}g_{m,BB}k_1}}{2Z_{C2}||\frac{-2}{A_{LNA}g_{m,BB}k_1} + 4R_{TH}} \tag{A.8}$$

Now, proceeding to find the RF current as in [19], and consequently the LTI small-signal equivalent, we find that impedance looking into node v_x, Z_{in}, as shown in Fig. A.1, is given by

$$\begin{aligned} Z_{in} &= \frac{2}{\pi^2}\left(2Z_{C2}||\frac{-2}{A_{LNA}k_1 g_{m,BB}}\right)||R_{sh} \\ R_{sh} &= \frac{8}{\pi^2 - 8}R_{TH} \end{aligned} \tag{A.9}$$

where k_1 is given by equation (A.7). It is not hard to see that the equation (A.9) can be represented by the equivalent circuit shown in Fig. A.2. Now, on including the feedback mixer switch resistance R_{SW2} and re-deriving the input impedance, after a few transformations, the approximate equivalent circuit shown in Fig. 2.5(a) may be obtained. The preceding analysis and LTI model are validated by the simulation results for a representative example, shown in Fig. A.3.

An interesting observation in the LTI equivalent circuit of Fig. A.2 is the shunt re-radiation resistance R_{sh} in the feedback path, but its absence in the feedforward path. To understand this, we delve into the source of R_{sh}. The node v_x is a sampled version (at f_{LO}) of the input $v_{RF,in}$, and contains components at odd harmonics of f_{LO}. However, the input $v_{RF,in}$ contains only a component at the fundamental f_{LO}. This leads to shunting of the higher harmonic components. However, the broadband LNA amplifies all harmonics of node voltage v_x. Now, both the output node of the LNA v_y and the node v_z (see Fig. A.1(a)) contain all components at the fundamental and all harmonics of f_{LO}. Moreover, the two node voltages are equal at all harmonics under the "mixing-region" assumption for the feedforward switch-RC kernel. Therefore, there is no harmonic shunting in the feedforward path.

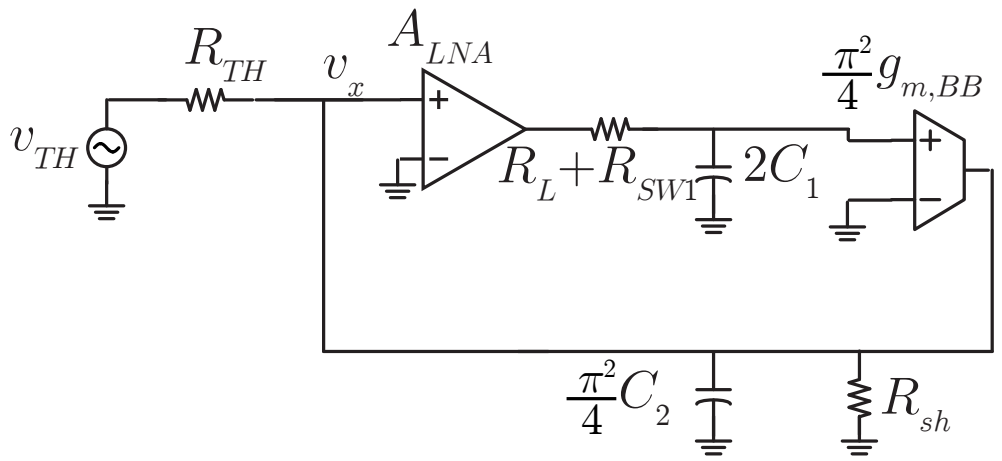


Figure A.2: LTI equivalent representation of the circuit in Fig. A.1 for $R_{SW2} = 0\Omega$ and broadband input match.

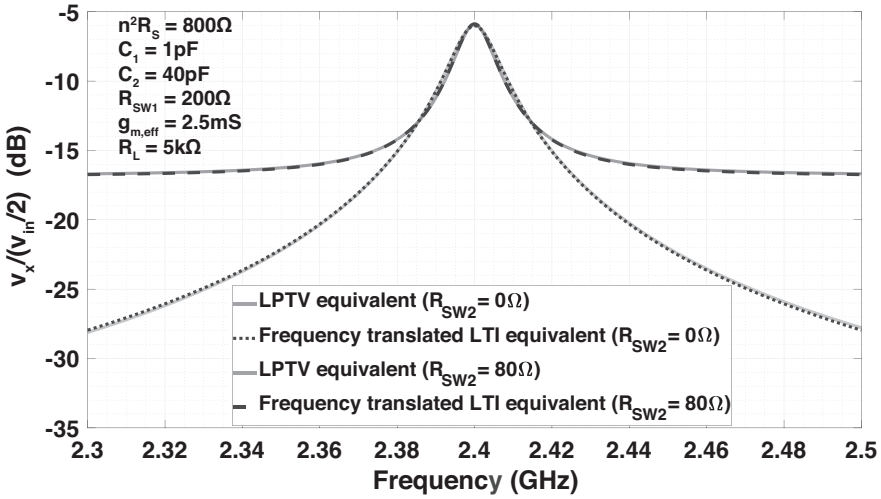


Figure A.3: SpectreRF PAC simulation of the LPTV half-circuit of Fig. A.1(a) and the frequency translated transfer function of the derived LTI equivalent shown in Fig. 2.5(a), for a broadband source impedance R_S. Simulation results are shown for two different values of R_{SW}.

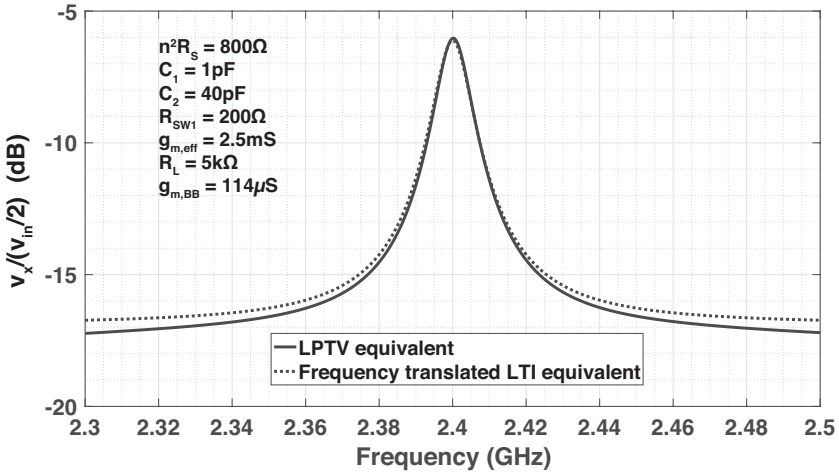


Figure A.4: SpectreRF PAC simulation of the LPTV half-circuit of Fig. A.1(a) and the frequency translated transfer function of the derived LTI equivalent shown in Fig. 2.5(b), for a narrowband source impedance R_S.

Finally, we analyze the equivalent circuit in case of an infinitesimally narrowband input match. In case of a narrowband input match, the node v_x in Fig. A.1 only has a component at the fundamental. Therefore, the equivalent circuit looking to the left of node v_x (voltage v_{TH} in series with R_{TH}) may be analyzed independently of the circuit looking to the right of the node v_x. In other words, the effects of sampling and harmonic re-upconversion become independent of R_{TH}. Applying charge balance equations at nodes $v_{c,m}$ and $v_{d,m}$, we have

$$\frac{v_{c,m}}{2Z_{C_1}}T_{LO} = \int_{mT_{LO}/4-T_{LO}/8}^{(m+1)T_{LO}/4-T_{LO}/8} \frac{A_{LNA}v_x - v_{c,m}}{R_L + R_{SW1}}dt \tag{A.10}$$

$$\left(-\frac{g_{m,BB}}{2}v_{c,m} + \frac{v_{d,m}}{2Z_{C_2}}\right)T_{LO} = \int_{mT_{LO}/4-T_{LO}/8}^{(m+1)T_{LO}/4-T_{LO}/8} \frac{v_x - v_{d,m}}{R_{SW2}}dt \tag{A.11}$$

After jointly solving these and a few circuit transformations, the circuit in Fig. 2.5(b) may be obtained. To contrast with the broadband input match case, now we observe that both the N-path filters have shunt re-radiation losses. This is not surprising because the node v_x and the output node v_y of the LNA, which amplifies the node v_x, contain only a component at the fundamental. On the other hand, the nodes v_z and v_w (see Fig. A.1(a)) contain harmonic components as well. Simulation results for a representative example with a narrowband source impedance, shown in Fig. A.4, validate the theory.

Appendix B

Harmonic Folding of the Common-Gate LNA's Noise

This section provides a detailed discussion of the harmonic noise folding of the transistor noise in the CG-LNA discussed in Section 2.4A (see Fig. 2.5). The amount of noise figure degradation due to harmonic noise folding is given by β. Clearly, the degradation is worse when the input matching network is narrowband, as the harmonic noise folding is worse [19]. In a broad-band (not tuned at drain) CC-CGLNA, the current noise source of the transistor in the LNA is also broadband. Therefore, noise current at the harmonics of ω_{LO} is also downconverted and appears at baseband. It was shown in [19] that the effect of harmonic noise folding of the source resistance R_S and the switch resistance R_{SW2} is captured by treating the shunt re-radiation resistance as a physical resistance. However, the noise folding of the transistor in the LNA needs to be analyzed separately.

Consider the broadband current noise source $i_{n,gm}$ with power spectral density equal to $4kTg_{m,LNA}\gamma/\alpha$ (at all harmonics), in shunt with the $g_{m,eff}$ in Fig. 2.5. To compute the total output noise, first we compute the transfer function from the current source $i_{n,gm}$ to the output at all harmonics. Based on a result from equation (25) in [16], if the transfer function from $i_{n,gm}(f_{LO}+f)$ to the differential output is $|H(f_{LO}+f)|$, then the transfer function from $i_{n,gm}(f_{LO}+kf)$ to the differential output is $|H(f_{LO}+f)/k|$ for all odd harmonics, and 0 for all even harmonics. This harmonic folding gives an additional factor of $\pi^2/8$ in the expression for β in equation (2.6) in case of the broad-band R_S. For a narrowband R_S, the node v_x is approximately shorted to ground at the harmonics of f_{LO}. Therefore, while the noise source $i_{n,gm}$ is degenerated by R_S at the fundamental f_{LO}, it is not degenerated at the harmonics of f_{LO}. This leads to a dependence of harmonic folding on the value of $g_{m,LNA}$. As seen from the expression for β in equation (2.6) and the solid plot in Fig. 2.7, it is apparent that increasing $g_{m,LNA}$ beyond a certain value yields diminishing returns, and eventual degradation in noise figure, for the case of narrowband input match. This effect is very similar to the existence of an optimal switch resistance (from a noise perspective) if the input match is narrow-band [19].