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A High-Efficiency Charge-Pump Gate Drive Power Delivery Technique for Flying Capacitor Multi-Level Converters with Wide Operating Range

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***Abstract*—In this work, we present a robust gate drive power delivery approach well-suited for converter topologies, such as the flying-capacitor multi-level (FCML) converter, that contain several series-connected switching elements. The proposed power delivery network leverages internal voltages inherent to the FCML topology in combination with a charge-pump mechanism to provide gate drive power with high efficiency. The charge-pump design operates independently of the primary switching devices, allowing the converter to operate at very low duty ratios without suffering from significant degradation of the floating supplies. The concept is validated in a hardware prototype, demonstrating an estimated 38 % reduction in gate drive power delivery losses compared to competing techniques. Moreover, the robustness of the technique is validated through incorporation into a 400 V, 2 kW 6-level FCML DC-DC converter, achieving a 99.07 % peak conversion efficiency and 2.05 kW/in^3 power density.**

I. Introduction

In recent work, flying-capacitor multi-level (FCML) converter implementations have demonstrated greatly increased power densities and efficiencies compared to more conventional 2-level topologies [1], [2]. This improved performance is enabled by both a multiplication of the effective switching frequency observed by the inductor, and by reduced volt-seconds applied to it – effects described in detail in [1], [3], and [4].

FCML converters with high level-count contain many power switches connected in series. The large number of power switches referenced to different voltage potentials presents a challenge for providing power to the associated floating gate drivers. An example of a 6-level buck-type FCML converter containing 10 power switches is shown in Fig. 1. Physical implementations of such a converter would require 10 gate drive supplies capable of enhancing their respective power devices with a sufficiently large gate-to-source voltage. In Fig. 1, these 10 supplies are shown as independent voltage sources, each referenced to the source terminal of the power device it drives. One verified method for generating these floating supplies utilizes isolated DC-DC converters [1], [5], [6]. Converters incorporating such supplies are not only expensive, but also typically report volumes greatly exceeding that of their powertrain. For an N-level flying-capacitor converter, where N refers to the number of discrete voltage levels the converter is capable of generating at its switched node (denoted V_{SW} in Fig. 1), the number of floating power supplies scales as

$$\#_{supplies} = 2N - 3\ . \tag{1}$$

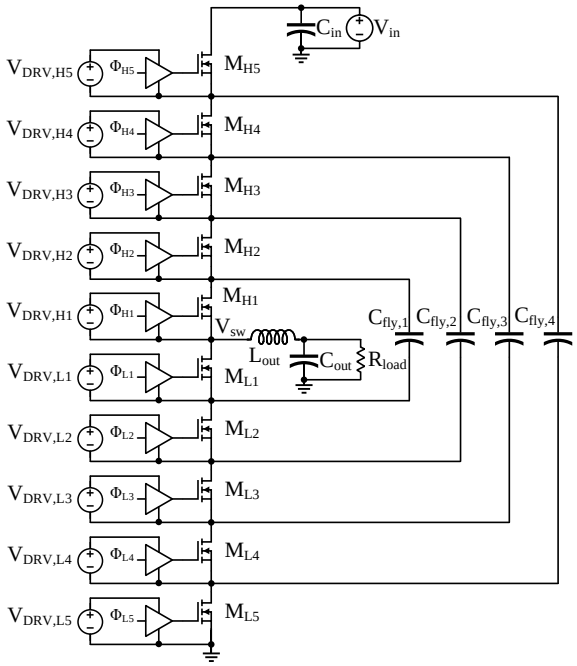

Fig. 1. A 6-level buck-type FCML converter with gate drive supplies generated from floating isolated voltage sources. In practice, this approach consumes significant volume, often greater than the power stage itself in modern designs [1], [6].

II. Background

To generate the required floating supply voltages without sacrificing significant converter volume, recent works on gate drive power delivery techniques for FCML converters have proposed the "cascaded bootstrap" approach for generating the required floating gate driver supplies [7]. Low-dropout linear regulators (LDOs) are included in this approach to regulate the bootstrap capacitor voltage to a fixed and reliable value that can be used to drive the FETs. An example 6-level FCML with a cascaded bootstrap gate drive supply is shown in Fig. 2.

Each bootstrap capacitor only charges when the power switch whose drain is connected to its negative plate conducts. If this charging interval is very short, the bootstrapping network operates in the fast switching limit (FSL) [8] and complete charge transfer does not occur between the bootstrap capacitors. As a practical example, the converter of [7] reports that for switching frequencies above 100 kHz, the charging current into the bootstrapped supply is roughly constant. Given that there is an incentive to switch at higher frequencies for reduced converter passive component volume

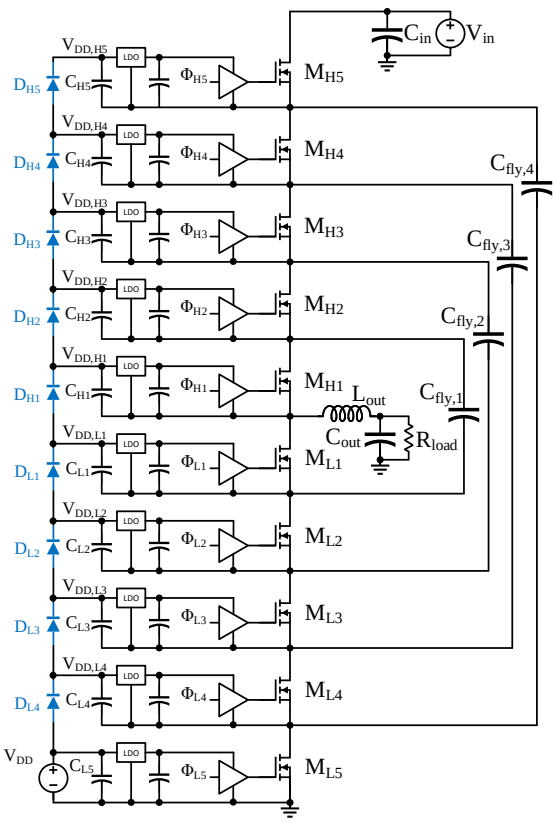

Fig. 2. A practical 6-level FCML with the cascaded bootstrap technique of [7] providing gate drive power.

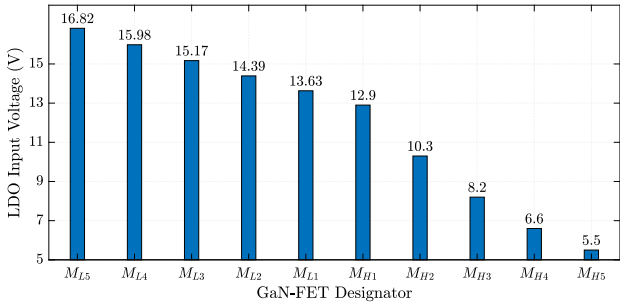

Fig. 3. Estimated minimum LDO voltages for converter operation at D = 5 % for a 6-level converter utilizing the cascaded bootstrap power delivery technique. A piecewise-linear diode model is used with $V_{D,on} = 0.6\,\text{V}$ and $R_{D,on} = 5\,\Omega$. To achieve 5 V gate drive on all power switches, we estimate the ground-referenced supply voltage $V_{DD,L5}$ must be significantly oversized above 16 V, which matches the findings in [7].

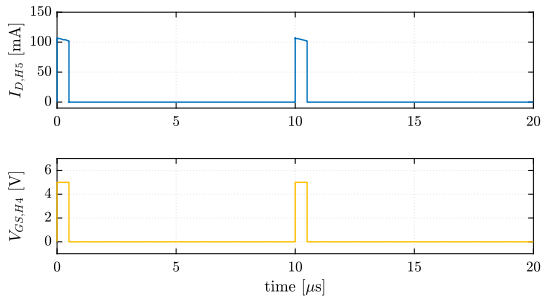

Fig. 4. SPICE simulation of bootstrap diode current at D = 5 % with a piecewise-linear diode model for D_{H5} and a 5 mA current source load modeling average gating current of M_{H5}. $f_{sw} = 100\,\text{kHz}$, $V_{D,on} = 0.6\,\text{V}$, $R_{D,on} = 5\,\Omega$. The bootstrap network operates in the fast-switching limit when the power switches conduct for short durations.

[9], operation in the FSL region is often encountered in practical implementations of FCML converters.

As the number of switches in the FCML increases, the gate drive supply voltage feeding the bootstrap chain must also increase, which corresponds to additional power loss across the LDO circuitry. Starting from the ground-referenced LDO connected to V_{DD} in Fig. 2, the loss in the k^{th} LDO cascaded from it scales approximately as

$$P_{loss_{LDO,k}} \approx \left(V_{DD} - \sum_{n=1}^{k} V_{f,n} - V_{GS,on} \right) I_g \qquad (2)$$

where $V_{f,n}$ represents the voltage drop across the n^{th} bootstrap diode during conduction.

Assuming that each gate drive supply consumes an average gating current I_g, we can use a piecewise-linear conduction model for the bootstrap diodes to estimate the minimum voltage V_{DD} required to generate at least 5.5V on $V_{DD,H5}$. This a typical lower limit suitable for driving gallium nitride (GaN) power semiconductor switches with a well-regulated 5 V gate-to-source voltage. With a target value for the top-most gate drive supply in the converter ($V_{DD,H5}$), and assuming a piecewise-linear diode conduction model, the required average high-side supply voltages $V_{DD,Hk}$ for this 6-level FCML can be expressed as

$$V_{DD,Hk} = V_{DD,H5} + (5-k)V_{D,on} + \sum_{n=0}^{5-k} \frac{n}{D} I_g R_{D,on} \qquad (3)$$

where D represents the converter duty ratio and $R_{D,on}$ is the conduction resistance of the bootstrap diode. Similarly, the required low-side supplies can be expressed as

$$V_{DD,Lk} = V_{DD,H1} + kV_{D,on} + \sum_{n=1}^{k} \frac{n+4}{1-D} I_g R_{D,on} \qquad (4)$$

where we assume the high-side switches $M_{H,x}$ of the FCML are driven with on-time equal to DT_s where T_s is the switching period, and the low-side switches $M_{L,x}$ are driven with the complementary switching signals. The switching signals $\Phi_{L5}, \Phi_{L4}, ..., \Phi_{H5}$ are commonly generated via Phase-Shifted Pulse-Width Modulation (PSPWM) [1], [4], [7], [10]. With cascaded bootstrapping, we can expect charge to be less effectively distributed through the high-side supplies at low duty ratios [7]. Our averaged model in (3) and (4) shows that to accommodate converter operation at very low duty ratios, the ground-referenced supply voltage V_{DD} must become very large.

An estimation of the gate drive supply voltage needed for operation at $D = 5\,\%$ is shown in Fig. 3, using (3) and (4). Diode parameters $V_{D,on} = 0.6$ V and $R_{D,on} = 5\ \Omega$ are used to match the simulation parameters reported in [7]. The gate drive power supply has to be sized at nearly 16 V to ensure the LDO at the end of the bootstrap chain receives adequate input voltage to turn on M_{H5}, which matches the simulation results in [7]. We verify the FSL operation of the bootstrapping network at $D = 5\,\%$ and $f_{sw} = 100\,\text{kHz}$ through a SPICE simulation, with results plotted in Fig. 4.

III. Oscillator-Driven Charge-Pump

In this work, we propose generating the floating gate drive supplies for the high-side switches via oscillator-driven charge-pumps that are connected as shown in Fig. 5. This approach is derived from the gate driven charge-pump proposed in [7], with the low-side pumping source replaced by an independent gate driver oscillating with a 50 % duty irrespective of the FCML converter duty. The oscillator derives its power from its associated unregulated low-side supply. Here we will demonstrate that in high level-count FCMLs, despite the two diode forward-voltage drops

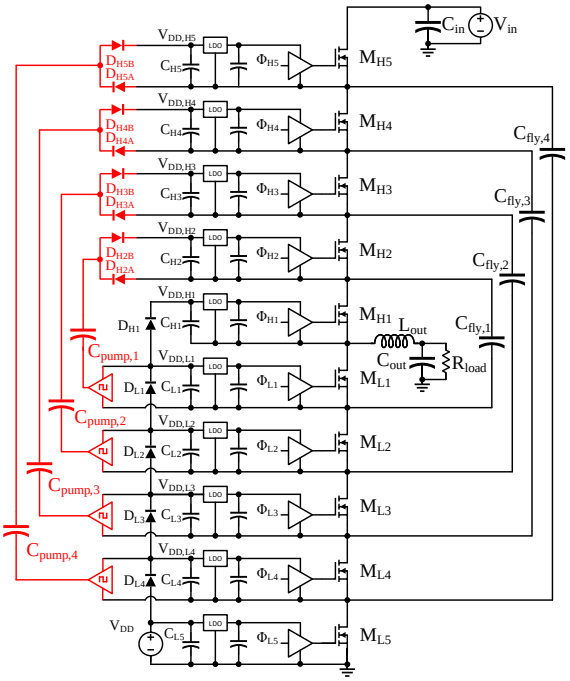

Fig. 5. Proposed gate drive power delivery network. Oscillator-driven charge-pumps (red) supply the high-side devices and operate at 50% duty independent of converter switching activity, allowing effective high side power delivery independent of converter duty cycle.

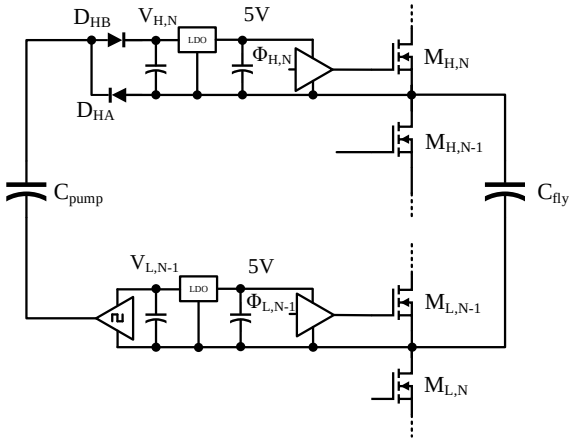

Fig. 6. Proposed oscillator-driven charge-pump structure shown between a general pair of switches.

introduced in the charge-pump, this approach greatly reduces the number of diodes through which charge must conduct to reach the large majority of high-side supplies. A detailed schematic diagram of the charge-pump structure within an N-level FCML is shown in Fig. 6.

The oscillator connected to the low-side floating supply charges C_{pump} using its corresponding C_{fly} and delivers charge onto the LDO input capacitor of the high-side driver. This operation is performed at an optimal 50% duty cycle, irrespective of the duty cycle of the converter itself, allowing maximum charge to propagate through C_{pump}. Note that as charge flows through two diodes, the high-side supply voltage lies below the low-side supply voltage that feeds it by two diode voltage drops. We assume that C_{pump}, C_{fly}, $C_{L,N-1}$, and $C_{H,N}$ are large enough such that they do not experience significant voltage ripple as they transfer charge. This allows us to assume that the charge-pump also operates in the FSL region.

When the oscillator output is driven low, the pump capacitor voltage can be solved from the following voltage loop equation

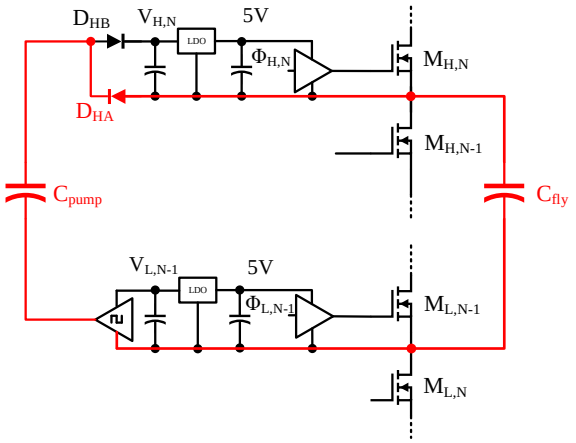

Fig. 7. Oscillator-driven charge-pump conduction path in State A. C_{pump} is charged up to the same voltage as flying capacitor C_{fly} minus one diode forward-voltage drop.

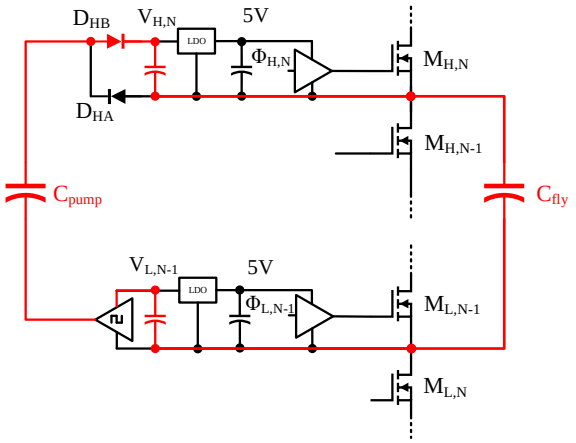

Fig. 8. Oscillator-driven charge-pump conduction path in State B. Energy from C_{pump} is transferred to the high-side supply $V_{H,N}$.

$$V_{C,fly} - V_{D,on} - \frac{I_g}{0.5} R_{D,on} - V_{C,pump} = 0 \tag{5}$$

and when oscillator output is driven high, the pump capacitor voltage can be found from

$$V_{L,N-1} + V_{C,pump} - V_{D,on} - \frac{I_g}{0.5} R_{D,on} - V_{H,N} - V_{C,fly} = 0 \tag{6}$$

We assume that the charge-pump duty cycle is 50 %, and that each diode conducts an average current I_g. We can combine (5) and (6) to obtain $V_{H,N}$ as a function of $V_{L,N-1}$.

$$V_{H,N} = V_{L,N-1} - 2V_{D,on} - 4I_g R_{D,on} \tag{7}$$

Similar to (4), we can form the following expressions for the low-side supplies in the 6-level converter employing our proposed gate drive power delivery technique:

$$V_{DD,L1} = max\left(V_{DD,H1} + V_{D,on} + \frac{I_g R_{D,on}}{1-D}, \right.$$
$$\left. V_{DD,H2} + 2V_{D,on,pump} + 4I_g R_{D,on,pump}\right) \tag{8}$$

As the diodes in the charge-pump are rated for significantly lower voltages than the bootstrap diodes, we can expect that the charge-pump diodes are higher conductivity devices, especially if the devices have similar die areas. Thus, we assume that in the proposed approach, the minimum value for V_{DD} is set by the floating supply referenced to the switched node (M_{H1} in our 6-level example). This is especially true

at low duty ratios where large pulsed currents flow through the bootstrap diodes. We thereby simplify (8) into

$$V_{DD,L1} = V_{DD,H1} + V_{D,on} + \frac{I_g R_{D,on}}{1-D} \ . \tag{9}$$

The required low-side supply voltages can therefore be expressed as

$$V_{DD,Lk} = V_{DD,H1} + kV_{D,on} + \frac{I_g R_{D,on}}{(1-D)} \sum_{n=1}^{k} (2n-1) \ . \tag{10}$$

To compare the gate drive power consumption of our proposed approach to that of the prior best approach, the cascaded bootstrap (Section II), we can analyze the minimum gate drive supply voltage required to feed the chain of floating-switch drivers and the power consumption of the two competing networks. The gate drive supply V_{DD} must be chosen such that the unregulated voltage at the LDO inputs for all floating supplies meets the LDO dropout voltage specification, V_{DO}. For a general N-level FCML, the minimum V_{DD} with cascaded bootstrapping is given by

$$V_{DD} \geq V_{GS,on} + V_{DO} + (2N-3)\, V_{D,on} + f_1\,(N, I_g, D) \tag{11}$$

whereas, with the proposed oscillator-driven charge-pump approach, the minimum V_{DD} expression is given by

$$V_{DD} \geq V_{GS,on} + V_{DO} + (N-1) V_{D,on} + f_2\,(N, I_g, D) \tag{12}$$

where f_1 and f_2 capture the dependence of the diodes' voltage drops on the current flowing through them. The following expressions for f_1 and f_2 can be derived from (3), (4), (9), and (10).

$$\begin{aligned} f_1(N, I_g, D) &= \frac{I_g R_{D,on}}{D} \sum_{n=1}^{N-2} n + \frac{I_g R_{D,on}}{1-D} \sum_{m=1}^{N-1} (m+4) \\ &= I_g R_{D,on} \left(\frac{(N-1)^2}{(1-D)} + \frac{(N-1)(N-2)}{2D(1-D)} \right) \end{aligned} \tag{13}$$

$$\begin{aligned} f_2(N, I_g, D) &= \frac{I_g R_{D,on}}{1-D} \sum_{n=1}^{N-1} (2n-1) \\ &= I_g R_{D,on} \frac{(N-1)^2}{(1-D)} \end{aligned} \tag{14}$$

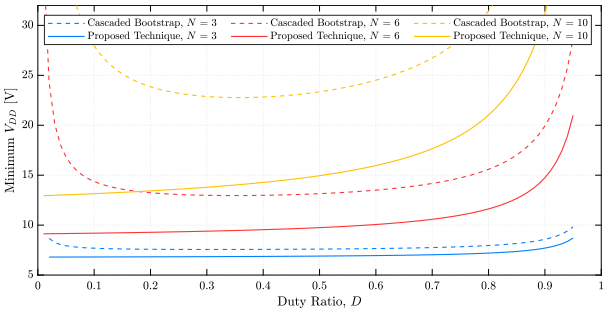

Fig. 9. Plot of minimum V_{DD} as a function of converter duty ratio D under the two competing gate drive power delivery techniques. We illustrate the minimum V_{DD} required for different level-counts N, with I_g = 5 mA and $R_{D,on}$ = 5 Ω. f_1 is significantly greater than f_2 at low duty ratios and contributes to a majority of the increase in required V_{DD}. This verifies the need to increase V_{DD} in cascaded bootstrap at low duty ratios.

Figure 9 illustrates the expressions in (11) - (14) for several different level-counts N with I_g = 5 mA and $R_{D,on}$ = 5 Ω. From (11) and (13) it is clear that with cascaded bootstrapping, as the duty ratio D approaches 0 %, the supply voltage V_{DD} must be increased without bound. By contrast, with the proposed technique, (12) and (14) show that the supply voltage required converges to a finite value as D approaches 0 %. Given that the average current provided by V_{DD} at the input to the gate drive network is $N \cdot I_g$ for both approaches, in considering (11) and (12) it becomes apparent that the oscillator-driven charge-pump technique demonstrates lower average gate drive power consumption by enabling use of a lower voltage V_{DD}. The ability of the proposed method to operate near 0 % duty while maintaining efficient power delivery to all gate drivers is a highly desirable trait for FCML-unfolder inverter topologies (e.g. [1]) in which the FCML is instructed to drive to zero-voltage output at twice the line frequency as the inverter output voltage changes polarity.

IV. Hardware Prototype and Experimental Results

A hardware prototype of a bi-directional 6-level FCML converter incorporating the oscillator-driven charge-pump scheme has been constructed, with annotated photographs shown in Fig. 10. A breakdown of the converter's specifications is provided in Table I. The converter is designed for high power density and was tested up to 2.03 kW at 400 V DC input, 200 V DC output, and at a device switching frequency of 120 kHz (corresponding to 600 kHz effective frequency seen by the inductor). The converter achieves a peak efficiency of 99.10 % (99.07 % when including a measured 380 mW of gate drive power) at 1.52 kW output power. Figure 11 depicts conversion efficiency over a range of output power levels. A Keysight PA2201A power analyzer

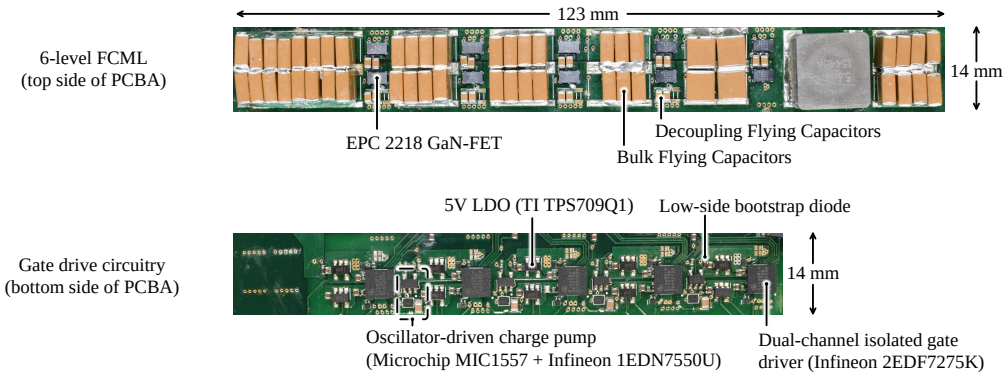

Fig. 10. Photograph of the constructed 6-level FCML prototype with key components annotated. The converter volume is approximately 0.987 in^3.

TABLE I
CONVERTER SPECIFICATIONS

Converter Parameter	Value
Input Voltage	400 V
Output Voltage	200 V
Switching Frequency	120 kHz
Nominal Flying Capacitance (C_{fly})	4 μF
Charge-Pump Frequency	620 kHz
Charge-Pump Capacitance (C_{pump})	47 nF
Effective Switched Node Frequency	600 kHz
Output Filter Inductance	5.6 μH
Maximum Output Power	2.03 kW
Measured Gate Drive Power	380 mW
Gate Drive Efficiency	$\sim$ 49.95 %
Peak Efficiency at 1.52 kW (including gate drive power)	99.07 %
Efficiency at 2.03 kW (including gate drive power)	99.04 %

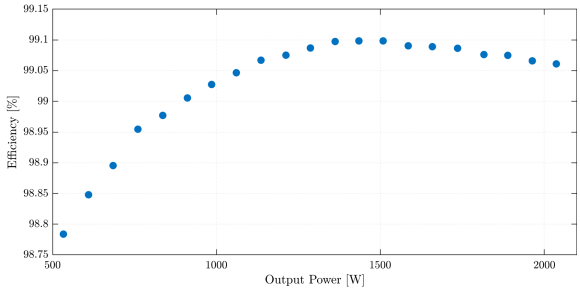

Fig. 11. Measured output power vs efficiency at 400 V input, 200 V output, 50 % duty, and 120 kHz switching frequency.

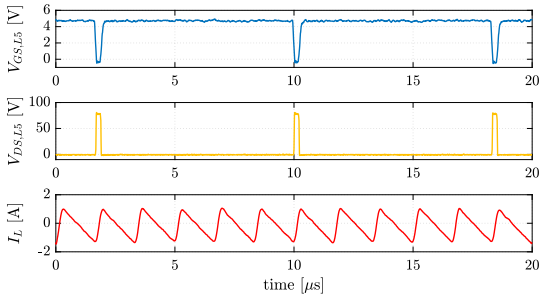

Fig. 12. Measured switch voltage and inductor current waveforms at D = 2.5 %. The converter demonstrates stable and balanced operation at extremely low duty-ratios. V_{in} = 400 V, V_{out} = 10 V, V_{DD} = 10.01 V, f_{sw} = 120 kHz, R_{load} = 100 Ω.

was employed to take high-precision measurements of input and output power.

With our proposed power delivery technique, the high-side supply voltages are maintained well above the LDO dropout levels, as they are fed directly from low-side counterparts independent of the converter's duty ratio. Conversely, the floating supplies for the low-side devices in our hardware prototype (M_{L1} - M_{L5}) exhibit higher values at lower duty ratios, as they are powered through a cascaded bootstrap arrangement in which charge delivery is a strong function of converter duty ratio [7]. Figure 12 illustrates measured steady-state converter waveforms at a very low duty cycle of D = 2.5 %, verifying correct operation with PSPWM under extreme step-down conditions. Figures 13-15 illustrate measured floating supply voltages at duty ratios of 2.5 %, 50 %, and 70 % respectively and demonstrate effective gate drive power delivery over a wide range of duty ratios.

The overall efficiency of the proposed power delivery

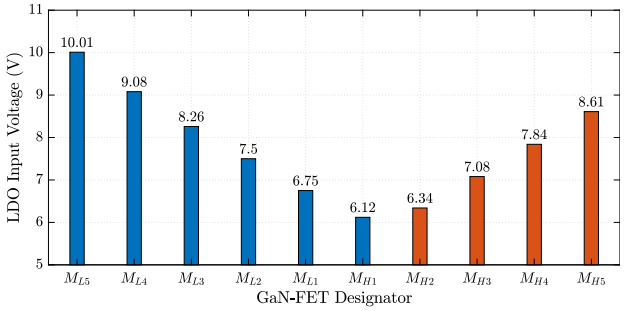

Fig. 13. Measured floating supply voltages at D = 2.5 %. V_{in} = 400 V, V_{out} = 10 V, V_{DD} = 10.01 V, f_{sw} = 120 kHz, R_{load} = 100 Ω.

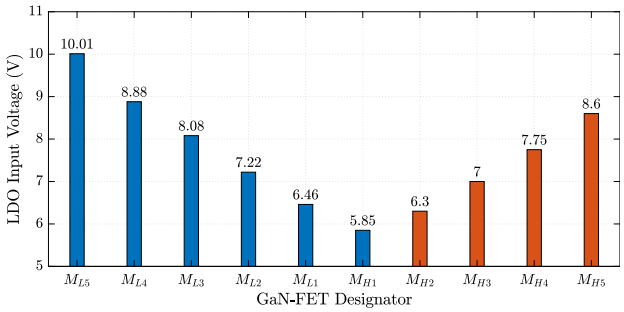

Fig. 14. Measured floating supply voltages at D = 50 %. V_{in} = 400 V, V_{out} = 200 V, V_{DD} = 10.01 V, f_{sw} = 120 kHz, R_{load} = 100 Ω.

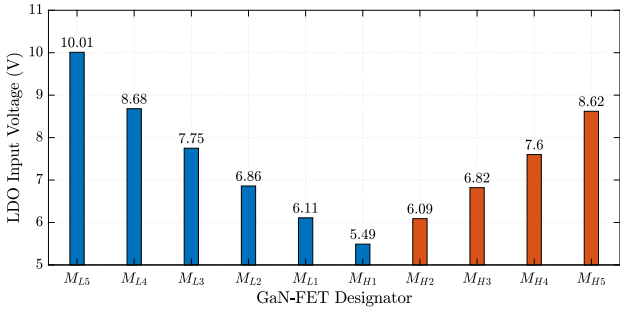

Fig. 15. Measured floating supply voltages at D = 70 %. V_{in} = 400 V, V_{out} = 280 V, V_{DD} = 10.01 V, f_{sw} = 120 kHz, R_{load} = 100 Ω.

technique is equal to the voltage conversion ratio $\frac{V_{GS,on}}{V_{DD}}$, similar to that of a single linear regulator. As power delivery to the high-side supplies is independent of converter duty ratio, we are able to achieve FCML conversion ratios as low as 2.5 % with a reduced supply voltage V_{DD} of 10.01 V and a measured gate drive efficiency of 49.95 %. In contrast, the cascaded bootstrap approach requires a supply voltage of 16 V or greater to maintain sufficient high-side gate drive voltage at a relaxed duty of 5 %. As such, the proposed technique achieves at least a 38 % improvement in gate drive power consumption at 5 % duty, with larger gains observed as duty decreases further.

V. CONCLUSION

In this work, we have demonstrated a gate drive power delivery scheme with reduced gate drive power consumption that enables FCML converter operation at extremely low duty ratios. The proposed oscillator-driven charge-pump power delivery technique was implemented in a 6-level FCML converter prototype that achieved 2.05 kW/in^3 power density and 99.07 % peak conversion efficiency.

TABLE II
HARDWARE PROTOTYPE COMPONENTS

Component	Part Number	Parameters
GaN FETs	EPC 2218	100 V, 3.2 mΩ
Gate Driver	Infineon 2EDF7275K	2-channel, isolated
Gate Resistor	20 Ω	SMD 0201
Linear Regulator (LDO)	TPS709Q1	5 V, 150 mA max
Cascaded Bootstrap Diodes	Central Semiconductor CMAD4448	120 V, 250 mA avg.
Gate Drive Bulk Capacitor	Murata GRM155R61E225ME11	2.2 μF, 25 V
Charge-Pump Oscillator	Microchip MIC1557	astable oscillator, RC configured
Charge-Pump Driver	Infineon 1EDN7550U	1-channel, differential
Charge-Pump Diodes	Nexperia PMEG4002AESF	40 V, 200 mA avg.
Charge-Pump Capacitor	TDK C2012X7T2W473K125AE	47 nF, 450 V
Bulk Flying Capacitor	TDK C5750X6S2W225K250KA	2.2 μF, 450 V
Decoupling Flying Capacitor	TDK C2012X7T2W473K125AE	47 nF, 450 V
Inductor	Vishay IHLP5050FDER5R6M01	5.6 μH, 32 A sat.

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