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Al-doped $HfO_2/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors

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Hafnium oxide gate dielectrics doped with a one to two percent of aluminum are grown on $In_{0.53}Ga_{0.47}As$ channels by codeposition of trimethylaluminum (TMA) and hafnium tertbutoxide (HTB). It is shown that the addition of TMA during growth allows for smooth, amorphous films that can be scaled to ~5 nm physical thickness. Metal-oxide-semiconductor capacitors (MOSCAPs) with this dielectric have an equivalent oxide thickness of 1 nm, show an unpinned, efficient Fermi level movement and lower interface trap densities than MOSCAPs with HfO_2 dielectrics grown by sequential TMA/HTB deposition. © *2011 American Institute of Physics*. [doi:10.1063/1.3575569]

The development of metal-oxide-semiconductor field effect transistor (MOSFET) technology with high-mobility III–V semiconductor channels faces serious challenges because of the inherently large interface trap densities (D_{it}) of dielectric/III–V interfaces. For III–V n-channel MOSFETs, $In_{0.53}Ga_{0.47}As$ is the leading candidate because it has a low electron effective mass, high saturation velocity, low intervalley scattering and is lattice-matched to InP.[1] Most studies of dielectric/$In_{0.53}Ga_{0.47}As$ interfaces have focused on Al_2O_3, HfO_2, or ZrO_2 dielectrics. Progress has been made in reducing the D_{it} of $Al_2O_3/In_{0.53}Ga_{0.47}As$ and $HfO_2/In_{0.53}Ga_{0.47}As$ interfaces to allow for Fermi level movement across the entire upper half of the band gap and into the lower half.[2,3] In contrast, dielectric/$In_{0.53}Ga_{0.47}As$ interfaces with large D_{it} show limited Fermi level movement in the upper band gap and are effectively pinned near midgap for practical gate biases. Even the best interfaces, however, still exhibit significant midgap D_{it}, which causes a pronounced frequency dispersion at negative gate biases in capacitance-voltage (CV) measurements.[4] Because of the small band gap of $In_{0.53}Ga_{0.47}As$ this frequency dispersion is detected even in room temperature measurements.[5] Furthermore, scaling of these gate stacks has been extremely limited, in particular for Al_2O_3, which has a low dielectric constant ($k \sim 9$). Typical accumulation capacitances of well-behaved metal-oxide-semiconductor capacitors (MOSCAPs) on $In_{0.53}Ga_{0.47}As$ are around 1 $\mu F/cm^2$, corresponding to an equivalent oxide thickness (EOT) of ~3 nm (the accumulation capacitance of MOSCAPs with $In_{0.53}Ga_{0.47}As$ is lower than the oxide capacitance, C_{ox}, because of the low density of conduction band states). Although EOTs of less than 1 nm have been reported for ZrO_2 and HfO_2 dielectrics,[6,7] these have been accompanied by large D_{it} and Fermi level pinning, as evidenced by a very large frequency dispersion at negative gate biases and failure to reach the depletion capacitance under negative bias.[4,8] Recently, TaSiO gate dielectrics on $In_{0.53}Ga_{0.47}As$ have been reported with high accumulation capacitance (1.7 $\mu F/cm^2$) and low frequency dispersion.[9] Because the dielectric constant of TaSiO ($k \sim 20$) is not significantly higher than that of HfO_2, and the D_{it} is most likely determined by the III–V surface, rather than the specific dielectric, the goal of the study presented in this letter was to investigate if a process could be developed for hafnium-based dielectrics with both low EOT and D_{it}.

Substrates were commercial, As-capped, 300 nm thick n-$In_{0.53}Ga_{0.47}As$ layers (Si: 1×10^{17} cm^{-3}) grown by molecular beam epitaxy (MBE) on (001) n^+-InP (IntelliEpi, Richardson, Texas). Before gate dielectric deposition, the As cap was removed *in-situ* by heating and monitoring the surface using reflection high-energy electron diffraction to obtain (2×4)-reconstructed $In_{0.53}Ga_{0.47}As$ surfaces [a mixture of β and γ-type (2×4)]. The dielectric was deposited in an ultrahigh vacuum MBE chamber by coevaporation of trimethylaluminum (TMA) and hafnium tertbutoxide (HTB) at a substrate temperature of 400 °C. The flux of TMA (p_{TMA}) was varied between 20 and 180 mtorr (gas inlet baratron pressure), while the HTB flux (p_{HTB}) was fixed at 330 mtorr. No carrier gas or additional oxygen was supplied. Samples were annealed *ex situ* at 400 °C for 5 min in ultrahigh purity nitrogen in a rapid thermal annealing system. 50-nm-thick Pt top electrodes were deposited by electron beam deposition through a shadow mask. A postmetal deposition anneal was carried out at 400 °C for 50 min in forming gas (95% of N_2 and 5% of H_2) to anneal out the damage in the $In_{0.53}Ga_{0.47}As$ caused by the metal gate deposition, which otherwise results in large D_{it}.[2,10] Back contacts were Ti (20 nm)/Pt (20 nm)/Au (250 nm). Frequency-dependent CV and conductance-voltage measurements were carried out in the dark from 1 kHz to 1 MHz at room temperature using an impedance analyzer (Agilent 4294). Capacitance and conductance values were corrected for series resistance (Eqs. 5.88, 5.90, and 5.91 in Ref. 11). CV and conductance-based methods were adapted for III–V MOSCAPs to correctly analyze the interface characteristics, as described in detail elsewhere.[8,12,13] Calculated, ideal (no D_{it}), high-frequency CV curves take the low conduction band density of states of $In_{0.53}Ga_{0.47}As$ and the nonparabolicity of the Γ valley into account.[8]

Figure 1 shows scanning electron microscopy (SEM) images of film surfaces grown with different TMA/HTB flux

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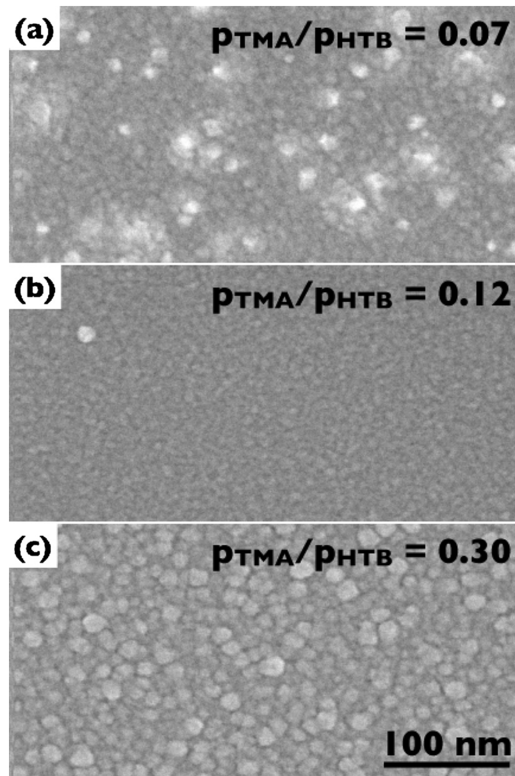

FIG. 1. Plan-view SEM images of dielectric films grown with different TMA/HTB flux ratios on (2×4) reconstructed $In_{0.53}Ga_{0.47}As$ surfaces. Flux ratios are given as baratron pressure ratios (p_{TMA}/p_{HTB}).

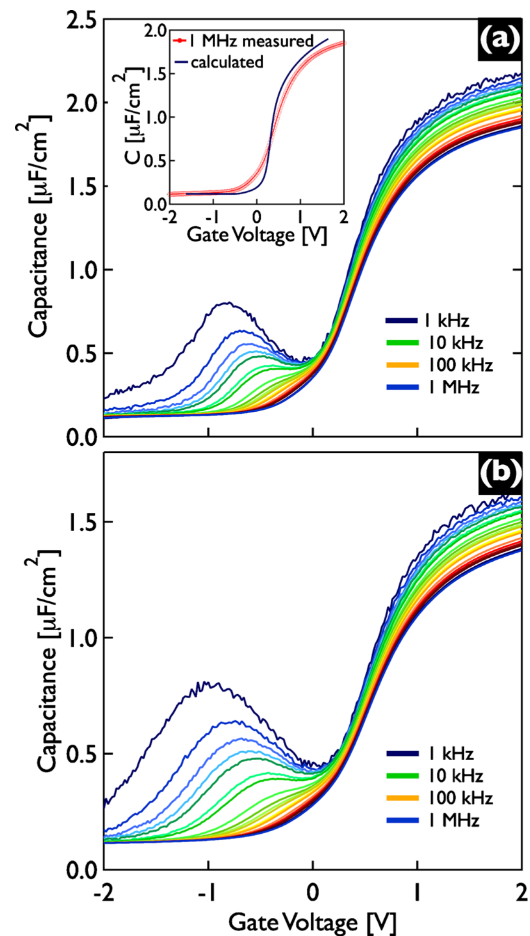

FIG. 2. (Color online) Capacitance-voltage curves measured as a function of frequency (from 1 kHz to 1 MHz) at room temperature for the $In_{0.53}Ga_{0.47}As$ MOSCAP with (a) a dielectric grown by TMA/HTB codeposition and (b) HfO_2 grown on TMA exposed $In_{0.53}Ga_{0.47}As$. The inset in (a) shows a comparison of the experimental 1 MHz CV of the MOSCAP with an ideal, calculated high-frequency CV.

ratios. For small TMA/HTB flux ratios [Fig. 1(a)] the films grow in island mode similar to HfO_2 (Ref. 12) and are not fully coalesced. Even larger grains are observed for too large TMA/HTB flux ratios [Fig. 1(c)]. In the intermediate flux ratio regime [Fig. 1(b)], however, smooth, coalesced films are obtained that can be scaled to thicknesses below 5 nm without pinholes. Transmission electron microscopy (TEM) showed that the as-deposited films are amorphous. Unlike crystallized HfO_2 films, the films can be wet-etched using diluted hydrofluoric acid. X-ray photoemission spectroscopy showed that the films contained about 1.5% of Al. The role of TMA in acting as a surfactant for HfO_2 growth has been documented recently[14] and it is likely that TMA also benefits the growth of smooth films during the codeposition of TMA and HTB. The suppression of crystallization is typical for mixtures in which structurally complex crystalline phases require extensive atomic rearrangement and are kinetically inhibited.[15]

Figure 2(a) shows the CV characteristics of a MOSCAP with a ~5 nm thick Al-doped HfO_2 dielectric that was grown under optimized conditions ($p_{TMA}/p_{HTB}=0.12$). The accumulation capacitance at 1 MHz is 1.85 $\mu F/cm^2$ at a gate voltage of 2 V, slightly higher than that for TaSiO.[9] The inset shows the comparison with the ideal calculated CV. Filling of higher lying valleys was not included in the calculated CV, as no evidence for this (such as a step in the capacitance) was seen in the experiments. From comparison with the calculated CV, C_{ox} is estimated to be 3.1 $\mu F/cm^2$, corresponding to an EOT of ~1 nm, in excellent agreement with the dielectric constant estimated from a thickness series (18 ± 3) and the physical thickness measured in TEM. The dielectric constant is similar to that reported in the literature for hafnium aluminate dielectrics with a few percent of Al.[16] The depletion capacitance density is close to its ideal value (0.119 $\mu F/cm^2$) for the dopant concentration of 10^{17} cm^{-3} (see inset), which indicates that negative biases fully deplete the channel and that the Fermi level moves past midgap. In addition, the midgap D_{it} response, apparent in the CV as a frequency-dependent "hump" at negative gate bias, is relatively small. For comparison, Fig. 2(b) shows the CV of a MOSCAP with a HfO_2 dielectric grown after short exposure of the $In_{0.53}Ga_{0.47}As$ surface to TMA but without TMA added during growth.[14] In this process HfO_2 could only be scaled to ~1.4 $\mu F/cm^2$ accumulation capacitance density (physical film thickness: 8–9 nm) without dramatically increasing the D_{it}.[14] Note the relatively larger and wider hump at negative biases, which shows that the HfO_2 MOSCAP has a larger midgap D_{it} than the MOSCAP with the dielectric grown by TMA/HTB codeposition. We note that the amount of Al in the film in Fig. 2(a) is too small to result in a detectable flat band voltage shift as may be expected due to the negative charge caused by large amounts of Al.[17]

Figure 3 shows a map of normalized parallel conductance, $[(G_p/\omega)/Aq]$, as a function of frequency and gate bias for the MOSCAPs with Al-doped HfO_2 and HfO_2 dielectrics shown in Fig. 2. Here, G_p is the parallel conductance, ω the angular frequency, A the MOSCAP area, and q the elemen-

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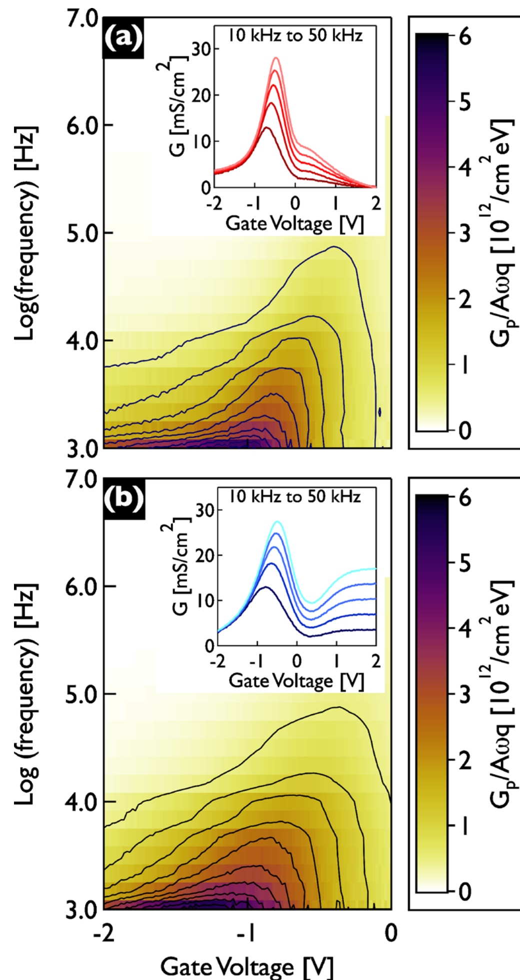

FIG. 3. (Color online) Normalized parallel conductance, $(G_p/\omega)/Aq$, as a function of gate voltage and frequency f for the $In_{0.53}Ga_{0.47}As$ MOSCAP with (a) the dielectric grown by TMA/HTB codeposition and (b) HfO_2 dielectric grown on TMA-exposed $In_{0.53}Ga_{0.47}As$. The insets show the measured conductance (G) as a function of gate voltage and frequency between 10 and 50 kHz.

tary charge. For both MOSCAPs, the normalized conductance peaks (maxima) move efficiently with gate bias, which shows that the Fermi level is not pinned at midgap.[13] For the MOSCAP with the dielectric grown by TMA/HTB codeposition [Fig. 3(a)] the movement is steeper and the trace width is narrower than for the HfO_2 MOSCAP [Fig. 3(b)], indicating a larger band bending in response to a change in gate bias.[13] The improvement in Fermi level response for the MOSCAP in Fig. 3(a) is due to a combination of larger oxide capacitance and lower D_{it}. The latter can be estimated by multiplying $[(G_p/\omega)/Aq]_{\max}$ with a factor of 2.5.[11] The conductance of the MOSCAPs also differs in the accumulation region (positive gate bias, see insets in Fig. 3). For the MOSCAP with the dielectric grown by TMA/HTB codeposition, the conductance is decreasing with increasing positive bias. In contrast, the conductance is higher for the pure HfO_2 dielectric. The lower conductance for the hafnium aluminate indicates smaller contribution from gate leakage,[18] despite its smaller physical thickness. From comparison with the ideal CV the band bending and the D_{it} of the hafnium aluminate MOSCAP can be estimated (see Ref. 8). At a gate bias of -1.5 V, the band bending of the $In_{0.53}Ga_{0.47}As$ channel was more than 0.6 eV from the flat band condition and the D_{it} is 6×10^{12} eV cm^{-2} near midgap (0.3 eV below the conduction band edge), which is similar to the value obtained from the conductance map.

In summary, we have shown that by codepositing small amounts of TMA, HfO_2 gate dielectrics can be scaled to a 1 nm EOT value, while at the same time avoiding the large midgap D_{it} and effective Fermi level pinning that are commonly observed for highly-scaled HfO_2-based dielectrics on $In_{0.53}Ga_{0.47}As$. The results demonstrate that careful optimization of dielectric deposition processes, in particular obtaining a thin, dense dielectric, can lead to improvements in the electrical quality of the dielectric/III–V interface.

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