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Zhu, Yicheng

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High-Performance Hybrid Switched-Capacitor Power Converters: Circuit Topologies,
Control Techniques, and Analytical Models

By

Yicheng Zhu

A dissertation submitted in partial satisfaction of the

requirements for the degree of

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in

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in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Robert Pilawa-Podgurski, Chair

Assistant Professor Jessica Boles

Professor David Perreault

Professor Kristofer Pister

Spring 2024

High-Performance Hybrid Switched-Capacitor Power Converters: Circuit Topologies,
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Abstract

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Yicheng Zhu

Doctor of Philosophy in Engineering – Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Robert Pilawa-Podgurski, Chair

Hybrid switched-capacitor (SC) converters have attracted increased attention due to their potential to provide improved solutions with higher efficiency and higher power density compared to conventional designs. As an emerging class of power converters, hybrid SC converters can leverage the greatly superior energy density of capacitors compared to inductors, while simultaneously benefiting from the improved figure-of-merit of low-voltage switching devices over their high-voltage counterparts. This dissertation explores the circuit topologies, control techniques, and analytical models for hybrid SC converters to enable higher performance.

First, this dissertation models and analyzes the effect of finite terminal capacitances on the performance of pure and resonant SC converters. By establishing a general output impedance model for each type of converter, the first part of this dissertation reveals that insufficient terminal capacitances can lead to a dramatic increase in output impedance and cause a considerable efficiency drop. Based on this analysis, a multi-resonant control technique is proposed to reduce terminal capacitances without sacrificing efficiency.

Second, this dissertation explores high-performance hybrid SC converters for direct 48 V to point-of-load (PoL) power conversion in data centers. High-performance processors (e.g., graphics processing units [GPUs], central processing units [CPUs], application-specific integrated circuits [ASICs], etc.) serve as the engine of data center computing platforms and the foundation for technical progress in areas such as artificial intelligence and autonomous vehicles. Due to the fast-growing demand for greater computational power, the electric power consumption of processors has increased dramatically in recent years and is approaching 1000 W, with core logic voltages below 1 V and peak current demand beyond 1000 A. At such high current levels, the large power distribution network (PDN) of the existing two-stage lateral power delivery architecture can lead to a dramatic voltage drop and unacceptable

conduction losses, which significantly limits processor performance, reduces system energy efficiency, and hinders data center decarbonization and densification.

In pursuit of a more efficient and compact alternative to the existing solution, the second part of this dissertation introduces a family of high-performance 48-V-to-PoL hybrid SC voltage regulators, named the switching bus converter. Based on a single-stage vertical power delivery (VPD) architecture, the switching bus converter significantly reduces the PDN size and power conversion losses. Moreover, the proposed switching bus converter family strategically merges two or multiple conversion stages through switching buses, a type of intermediate bus with a switching voltage. Compared to the existing dc-bus-based architecture, the proposed switching-bus-based architecture does not require dc bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. In addition, this dissertation conducts a comparative performance analysis of different regulated hybrid SC topologies, which reveals that a larger SC conversion ratio is advantageous for achieving higher performance. Through the two-phase operation of the series-capacitor buck modules, the proposed switching bus converter extends the maximum duty ratio and enables a larger SC conversion ratio. Various circuit topologies from the switching bus converter family and their hardware prototypes are presented in this dissertation, including a 1500-A high-efficiency prototype and a high-density prototype with a practical form factor for VPD, which push the performance boundary for 48-V-to-PoL power conversion.

*To my family
for your unconditional love and support*

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Chapter 1

Introduction

1.1 Background and Motivation

From the chip edge in data centers to the grid edge in solar farms, and from small smartphone chargers to the large superchargers of electric vehicles, power electronics serve as the enabling technology for electrical energy conversion and the driving force behind technical innovations in numerous applications.

A typical power electronic system consists of active switching devices and passive energy storage components, including capacitors and magnetics, and can be conceptually depicted in the block diagram shown in Fig. 1.1. In each switching cycle, the power electronic system first momentarily stores electrical energy from the source in the passive components and then releases it to the load. By repeating this process cyclically, the system converts electricity from one form at the input to another form at the output, as required by the load. The objectives of designing a high-performance power electronic system include high efficiency, small volume, light weight, fast response, low cost, high reliability, etc.

Since the field's inception, active semiconductor devices have played a key role in improving the performance of power electronics. From the development of the power bipolar junction transistor (BJT) through the power metal-oxide-semiconductor field-effect transistor (MOSFET) to silicon carbide (SiC) and gallium nitride (GaN) switching devices, advances in switching frequency and reductions in on-state resistance have enabled consistent efficiency and power density improvements. However, the selection of passive components in power converter design is often overlooked. To create the most compact power converter, it is essential to use the most energy-dense passive components available.

Traditional designs of power converters primarily utilize inductors and transformers for energy storage and transfer. However, as will be introduced in Section 1.2.1, recent studies have shown that capacitors generally have significantly higher energy densities compared to inductors. In addition, through a device loss analysis, Section 1.2.2 will show that low-voltage switching devices typically have better figures-of-merit (FOM) than high-voltage switching devices. Based on these two observations, this dissertation explores a hybrid

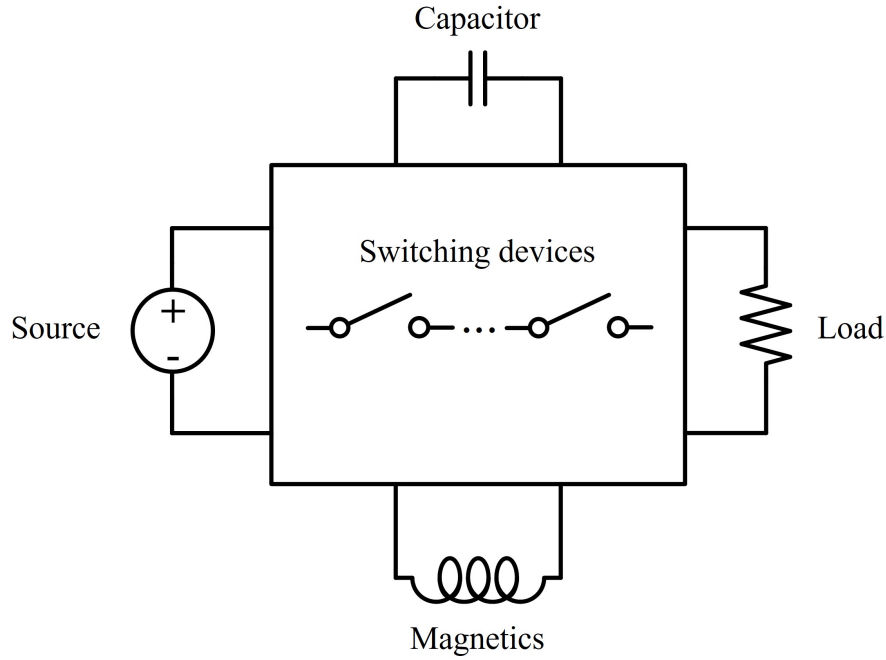


Figure 1.1: Conceptual representation of a power electronic system.

switched-capacitor (SC) approach to power electronic system design, which leverages the superior energy storage capabilities of capacitors compared to inductors while simultaneously benefiting from the improved FOM of low-voltage switching devices over their high-voltage counterparts.

1.2 Hybrid Switched-Capacitor Approach

1.2.1 Energy Storage Capabilities of Passive Components

Fig. 1.2 shows a comprehensive survey [1] of over 606,000 commercial capacitors and 88,000 commercial inductors from Digikey Electronics, a large electronic component distributor. As can be observed, the highest volumetric energy density (γ_v) of commercial capacitors is nearly $1,000\times$ greater than that of the densest commercial inductors, meaning that the best capacitor component available on the market can store nearly $1,000\times$ more energy than the best inductor component for a given volume. This marked difference in energy storage capabilities suggests that a topology designed to utilize capacitors more effectively as energy transfer elements has the potential to achieve higher power density.

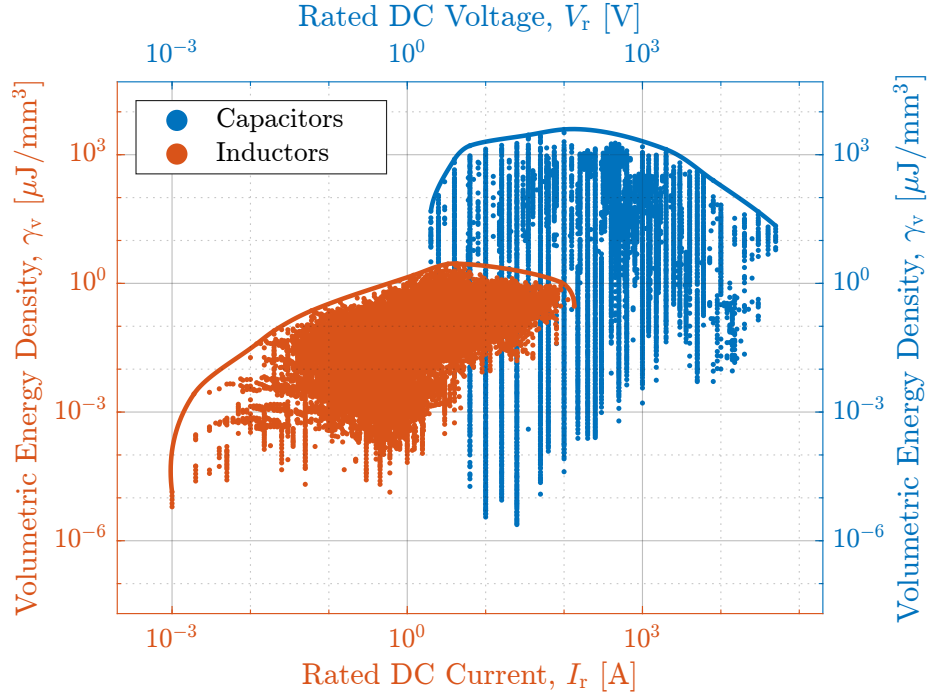


Figure 1.2: Commercial capacitor versus inductor volumetric energy densities (γ_v) across rated dc voltage (V_r) or current (I_r). From the highlighted Pareto fronts, commercial capacitors have a roughly 1,000 $\times$ better maximum volumetric energy density capability compared to commercial inductors. [1]

1.2.2 Scaling Trends of Power Semiconductor Devices

When assuming negligible V – I overlap loss and gate drive loss, the theoretical minimum power loss of a semiconductor switching device in a half-bridge is given by

$$P_{\text{semi}(\min)} = V_{\text{dc}} I_{\text{d}(\text{rms})} \sqrt{\frac{1}{2} f_{\text{sw}} R_{\text{ds,on}} C_{\text{oss,Q}}} \propto \sqrt{R_{\text{ds,on}} C_{\text{oss,Q}}}, \quad (1.1)$$

where V_{dc} is the dc-link voltage; $I_{\text{d}(\text{rms})}$ is the RMS value of the current flowing through the device; f_{sw} is the switching frequency; $R_{\text{ds,on}}$ is the on-state resistance of the device; and $C_{\text{oss,Q}}$ is the charge-equivalent output capacitance [2, 3] of the device. Since the theoretical minimum power loss ($P_{\text{semi}(\min)}$) is proportional to $\sqrt{R_{\text{ds,on}} C_{\text{oss,Q}}}$, a device figure-of-merit (FOM) can be defined as follows to investigate the scaling law of power semiconductor devices:

$$\text{Switching device FOM} = \sqrt{R_{\text{ds,on}} C_{\text{oss,Q}}} \quad (1.2)$$

A lower device FOM implies lower conduction and switching losses, and is thereby more desirable. A detailed derivation for the theoretical minimum power loss ($P_{\text{semi}(\min)}$) and the device FOM is provided in Appendix A.

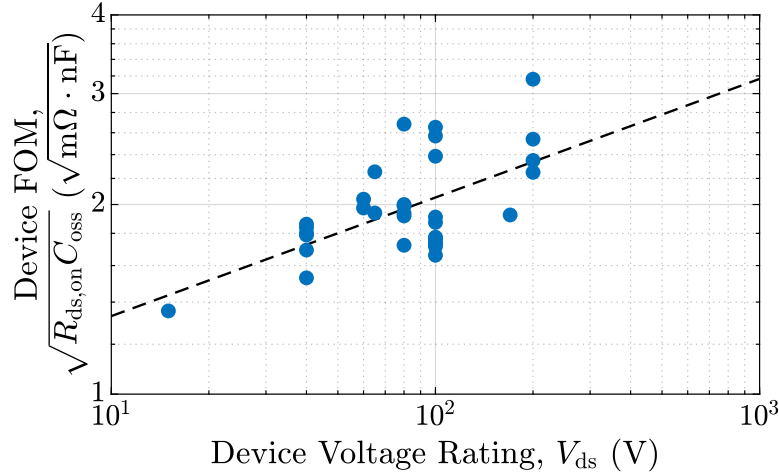


Figure 1.3: Device FOM ($\sqrt{R_{ds,on}C_{oss}}$) across rated voltage (V_{ds}) of EPC GaN transistors.

Figure 1.3 shows a survey of EPC GaN transistors. Each dot represents the FOM and voltage rating of each device. The dashed curve shows the fitted trend line predicted by semiconductor physics that is in the form of

$$\sqrt{R_{ds,on}C_{oss,Q}} = kV_{ds}^{\alpha}, \quad (1.3)$$

where k and α are voltage-scaling factors. The α factor values for Si, SiC, and GaN devices are typically 0.5, 0.3, and 0.2, respectively, according to [4]. In general, lower voltage switching devices have better FOM compared to higher voltage devices. This means that it is advantageous to replace a single large, high-voltage switch with multiple small, low-voltage switches that have improved device FOM.

1.2.3 Hybrid Switched-Capacitor Approach

Based on the above two observations regarding passive components and active switches, this thesis explores a new approach to power electronic circuit design: the hybrid switched-capacitor (SC) approach, which is built on the following two key motivations.

- Given that capacitors have much higher energy densities than inductors, energy transfer should be primarily based on capacitive energy storage instead of inductive energy storage to reduce overall passive component volume.
- To leverage the improved FOM of low-voltage devices compared to their high-voltage counterparts, multiple low-voltage switches should be used in place of a lumped high-voltage switch for device loss reduction.

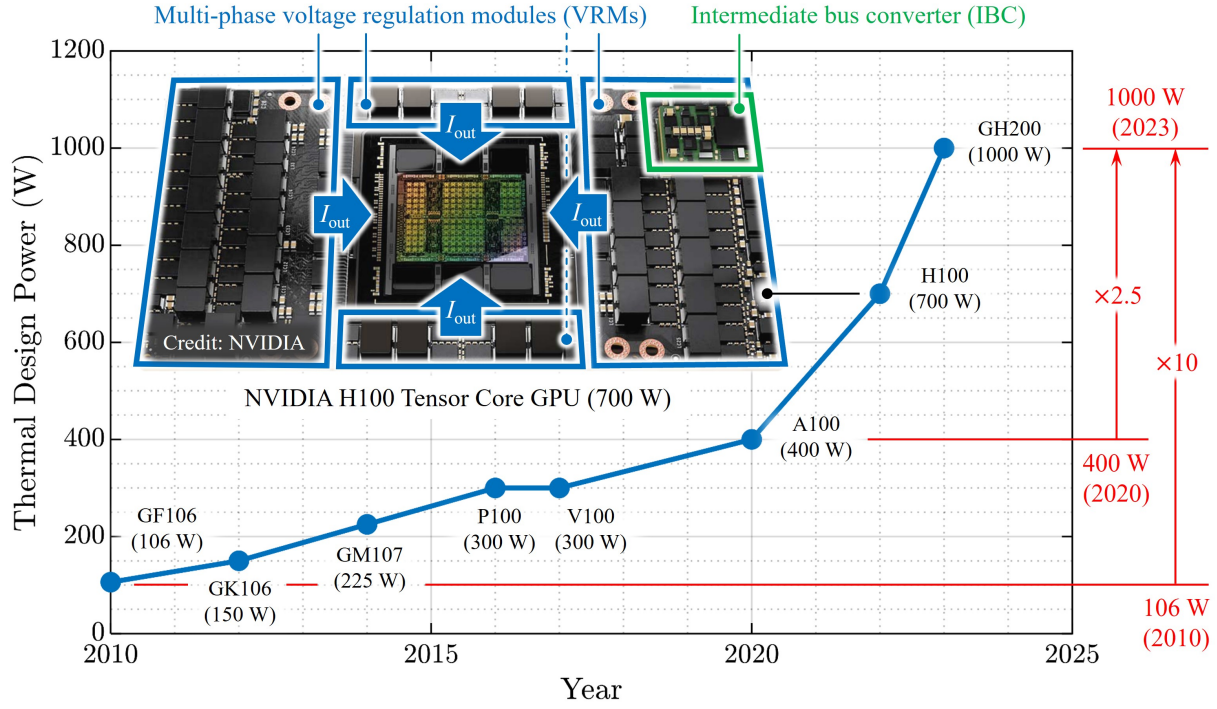


Figure 1.4: The past decade has witnessed rapid growth in the thermal design power (TDP) of NVIDIA data center GPUs [5]. The picture of NVIDIA H100 tensor core GPU [6] shows the existing two-stage lateral power delivery (LPD) architecture where the current flowing out of the voltage regulation modules (VRMs) needs to travel a long distance to the processor pins, leading to a large power distribution network (PDN) and high PDN losses.

1.3 Background and Challenges of 48 V to Point-of-Load Power Delivery in Data Centers

High-performance processors (e.g., GPUs, CPUs, ASICs, etc.) serve as the engine of data center computing platforms and the foundation for technical progress in areas such as artificial intelligence, deep learning, autonomous vehicles, and numerous other applications. In recent years, the electric power consumption of processors has increased dramatically and is approaching 1000 W due to the fast-growing demand for greater computational power. For example, as shown in Fig. 1.4, the thermal design power (TDP) of NVIDIA data center GPUs has grown by 10 times in the past decade, from 106 W to 1000 W. And just in the past three years alone, the TDP has more than doubled.

As power levels increase, the 48-V bus architecture is gradually replacing the legacy 12-V dc bus in modern data centers since the power distribution losses (i^2R losses) decrease by sixteen-fold with the quadrupling of the bus voltage. This makes the design of the voltage regulation modules (VRMs) responsible for the 48 V to point-of-load (PoL) power

conversion more challenging with a quadrupled voltage conversion burden. In addition to a large conversion ratio of 48-to-1 or higher, the VRMs for next-generation ultra-high power processors should be capable of sourcing ultra-high current (≥ 1000 A) at low supply voltage (≤ 1.0 V) and achieving high power density, high efficiency, and fast dynamic response.

The picture of the NVIDIA H100 tensor core GPU [6] in Fig. 1.4 shows the existing two-stage lateral power delivery (LPD) architecture where the current flowing out of the VRMs needs to travel a long distance to the processor pins, leading to a large power distribution network (PDN). With a load current beyond 1000 A, the high PDN resistance can lead to a dramatic voltage drop and unacceptable conduction losses, which significantly limits processor performance, reduces system energy efficiency, and hinders data center decarbonization. Moreover, the resulting low efficiency necessitates a larger size of the thermal management solution, which is presently a bottleneck of system densification.

In addition, in this two-stage architecture, as illustrated in Fig. 1.5(a), the 48-V input voltage needs to be first stepped down to the intermediate dc bus voltage (12/8/6 V) and then regulated down to the 1 V (or even lower voltage) at the PoL. This thesis explores the single-stage architecture shown in Fig. 1.5(b) for direct 48-V-to-PoL power conversion. By combining the two conversion stages into one single stage, this architecture can effectively reduce the power conversion losses and the PDN losses on the intermediate dc bus, thereby promising to achieve higher efficiency.

1.4 Organization of Dissertation

Part I: Modeling, Analysis, and Control of Pure and Resonant Switched-Capacitor Converters With Finite Terminal Capacitances

In pre-existing analytical models of pure switched-capacitor (SC) converters and resonant switched-capacitor (ReSC) converters, the input and output capacitances (C_{in} and C_{out}) have long been assumed to be infinitely large so that the input and output can be modeled as ideal voltage sources. However, in practice, the terminal capacitances can be insufficient to ensure ideal input and output behaviors due to space and cost constraints. This part models and analyzes the effect of finite terminal capacitances on the performance of pure SC and ReSC converters. By establishing the general output impedance models for pure SC and ReSC converters, Chapters 2 and 3 reveal that finite terminal capacitances can have considerable effects on the output impedance (R_{out}) and the overall efficiency of SC and ReSC converters. In addition, in ReSC converters with the conventional two-phase control, input and output capacitors need to be sufficiently large to ensure ideal input and output behaviors. However, the bulky terminal capacitors dramatically increase the overall converter volume and significantly limit the potential of ReSC converters for achieving higher power density. Chapter 4 proposes a control technique for ReSC converters to achieve terminal capacitance reduction without harming the overall efficiency.

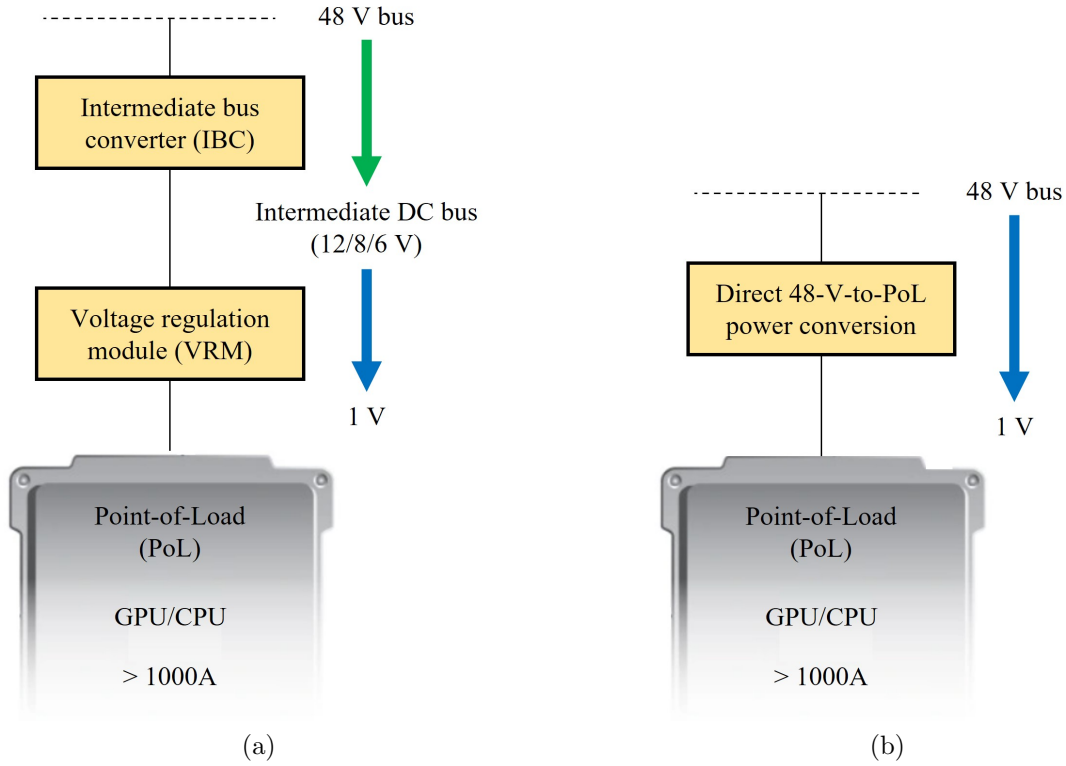


Figure 1.5: 48-V-to-PoL power delivery architectures. (a) Existing two-stage power delivery architecture. (b) Single-stage power delivery architecture for direct 48-V-to-PoL conversion.

Chapter 2: Modeling and Analysis of Pure Switched-Capacitor Converters with Finite Terminal Capacitances

This chapter proposes a general modeling and analysis methodology for SC converters to characterize the effects of finite terminal capacitances quantitatively. It is revealed that the insufficiency in C_{in} can lead to a considerably higher R_{out} and harm the overall efficiency. On the contrary, decreasing C_{out} can counter-intuitively help reduce R_{out} , which contributes to both higher efficiency and higher power density, although this benefit comes at the cost of a larger output voltage ripple. In addition, C_{out} has a stronger effect on R_{out} in the slow switching region, while C_{in} is more influential in the fast switching region, especially around the knee of the output impedance curve, which is the typical operating point of SC converters. Several design guidelines are provided based on these findings. Further discussions are provided to explain how to apply the proposed general output impedance model to arbitrary SC topologies.

Chapter 3: Modeling and Analysis of Resonant SC Converters with Finite Terminal Capacitances

This chapter proposes a general modeling and analysis methodology that can characterize the effects of finite terminal capacitances on the output impedance of ReSC converters. The proposed model is verified by circuit simulations and experimental measurements from a 2-to-1 ReSC converter prototype. It is revealed that the insufficiency in terminal capacitances can result in higher critical switching frequency, and C_{in} has a stronger influence on the critical switching frequency than C_{out} . Several design guidelines are provided based on these findings. Further explanations are also given for the applicability of this work to more complex ReSC topologies.

Chapter 4: Multi-Resonant Compensation Control for Terminal Capacitance Reduction in Resonant SC Converters

This chapter proposes a multi-resonant compensation control (MRCC) technique for ReSC converters that can adaptively compensate for the negative effects of finite terminal capacitances by ensuring multi-resonant and full zero current switching (ZCS) operation with adjusted duty ratio and switching frequency. The proposed technique is verified experimentally in a 2-to-1 ReSC converter prototype, demonstrating a more than 5 times terminal capacitance reduction without harming the overall efficiency compared to the conventional control technique.

Part II: Circuit Topologies, Comparative Analysis, and High-Performance Hardware Implementation For Direct 48 V to Point-of-Load Power Delivery in Data Centers

In pursuit of a more efficient and compact alternative to the existing two-stage LDP solution shown in Fig. 1.4, this part presents a family of high-performance regulated hybrid SC converters for 48-V-to-PoL power conversion in data centers. In the proposed family of topologies, two or multiple SC stages are merged through switching buses, a type of intermediate bus that allows switching voltages. Compared to the existing dc-bus-based architecture, the proposed switching-bus-based architecture does not require dc bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. Based on this switching bus concept, Chapters 5–9 present several different switching-bus-based topologies and their high-performance implementation for direct 48-V-to-PoL applications. These topologies are synthesized in Chapter 10 as a generalized switching-bus-based architecture, which yields a family of switching-bus-based converters. In addition, Chapter 11 introduces an analytical framework for characterizing and comparing regulated hybrid SC topologies for direct 48-V-to-PoL conversion, which reveals the theoretical benefits of a larger SC stage conversion ratio.

Chapter 5: Multi-Phase Cascaded Series-Parallel Hybrid Converter

This chapter proposes a multi-phase hybrid switched-capacitor (SC) converter that can be viewed as a 6-to-1 cascaded series-parallel (CaSP) converter merged with a three-phase interleaved buck converter with automatic current balancing. Due to multi-phase operation, the CaSP stage is able to achieve a higher conversion ratio compared to two-phase SC converters with the same number of components as well as lower turn-on voltage for switching devices. Moreover, the proposed CaSP-PoL topology benefits from the frequency multiplication effect similar to that in flying capacitor multilevel converters, which allows for lower frequency operation of higher voltage rated switches and doubled frequency operation of buck inductors, contributing to a further reduction in switching loss and inductor size.

Chapter 6: Dickson-Squared Hybrid Switched-Capacitor Converter

This chapter proposes a Dickson-squared hybrid switched-capacitor (SC) converter that comprises a 9-to-1 SC stage that can be viewed as two 3-to-1 Dickson SC converters combined together and a nine-phase interleaved buck stage. The proposed topology can achieve complete soft-charging operation with a simple control scheme, ensure naturally balanced interleaved inductor currents, enable reduced conversion burden on the buck stage, and eliminate the need for large bus capacitors with a switching bus architecture.

Chapter 7: The Switching Bus Converter: A High-Performance 48-V-to-1-V Architecture with Increased SC Conversion Ratio

This chapter proposes a switching bus converter that merges a 2-to-1 SC front-end with two 8-branch series-capacitor-buck (SCB) modules through two switching buses. Through the two-phase operation of the SCB modules, the proposed topology extends the maximum duty ratio and enables a larger SC conversion ratio. A hardware prototype was designed and built with custom two-phase coupled inductors and synchronous bootstrap daughterboards to validate the theoretical potential of the proposed topology. The theoretical benefits of a larger SC conversion ratio were experimentally verified with measured performance at different SC conversion ratios.

Chapter 8: A 1500-A/48-V-to-1-V Switching Bus Converter for Next-Generation Ultra-High-Power Processors

This chapter proposes an ultra-high-current 48-V-to-1-V hybrid switched-capacitor (SC) voltage regulator consisting of two 2-to-1 SC front-ends and four 10-branch series-capacitor-buck modules, merged through four switching buses. A hardware prototype was designed and built with custom four-phase coupled inductors and gate drive daughterboards to validate the functionality and performance of the proposed converter. It was tested up to 1500-A output current and pushes the performance limit of the state-of-the-art 48-V-to-1-V solutions towards higher efficiency and higher power density.

Chapter 9: A Compact 48-V-to-Sub-1-V Switching Bus Converter with 4.7-mm Height for Processor Vertical Power Delivery

To deliver high current at low processor core voltages with low power distribution network losses, this chapter proposes a compact 48-V-to-sub-1-V switching bus converter; a hybrid switched-capacitor (SC) voltage regulator for single-stage vertical power delivery (VPD). In the proposed switching bus converter, a 2-to-1 SC front-end and two 10-branch series-capacitor-buck modules are merged through two switching buses. A hardware prototype was designed and built with two-phase coupled inductors customized for VPD, meeting a stringent maximum height limit of less than 5 mm. It was tested up to 600-A output current and achieved excellent performance compared to the state-of-the-art 48-V-to-1-V academic works.

Chapter 10: Generalized Switching-Bus-Based Architecture for Regulated Hybrid Switched-Capacitor Converters

This chapter synthesizes the topologies proposed in Chapters 5–9 and extends the switching bus concept proposed in Chapter 7 as a generalized switching-bus-based architecture for regulated hybrid switched-capacitor converters. Based on this generalized architecture, a family of regulated switching-bus-based topologies can be constructed, including two-stage topologies and multi-stage topologies. Several concrete examples are provided.

Chapter 11: Comparative Performance Analysis of Regulated Hybrid SC Topologies for Direct 48-V-to-PoL Conversion

This chapter introduces an analytical framework for characterizing and comparing regulated hybrid SC topologies for direct 48-V-to-PoL conversion. In the proposed framework, a regulated hybrid SC topology is generally represented as a fixed-ratio SC stage merged with a subsequent regulated buck-type stage, with the total conversion ratio allocated between them. Three metrics are used for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. This framework reveals that increasing the SC stage conversion ratio reduces switch stress and passive component volume while accelerating the downward slew rate of inductor current, thereby improving efficiency, power density, and load step-down transient performance concurrently. Although a larger SC step-down ratio typically decreases the upward slew rate of inductor current, potentially impairing the load step-up transient performance, proper designs can achieve balanced load step-up and step-down transient performance.

Part I

Modeling, Analysis, and Control of Pure and Resonant Switched-Capacitor Converters With Finite Terminal Capacitances

Chapter 2

Modeling and Analysis of Pure Switched-Capacitor Converters with Finite Terminal Capacitances

2.1 Background and Motivation

Compared with traditional magnetic-based power converters, switched-capacitor (SC) converters have been demonstrated to have great potential of achieving higher power density and more effective switch utilization [7, 8]. Therefore, they are widely used in various applications, including CMOS integrated power conversion [9–12], consumer electronics [13], power amplifier [14], data center power delivery [15], and automotive systems [16–18], ranging from dc-dc [19] to dc/ac-ac [20–23] conversions.

Although pre-existing models [24–29], analyses [30–36], and control [37, 38] of SC converters assume input and/or output to be ideal voltage sources, as illustrated in Fig. 2.1(a), practical implementations of SC converters involve input and output capacitors (C_{in} and C_{out}) to stabilize the terminal voltages, as shown in Fig. 2.1(b). Theoretically, if C_{in} and C_{out} are much larger than the flying capacitor (C_{fly}) (i.e. $C_{\text{in}}, C_{\text{out}} \geq 10C_{\text{fly}}$) the input and output can be regarded as ideal voltage sources. However, in practical applications, the sizes of C_{in} and C_{out} are usually constrained by space and cost and thus can be insufficient to ensure ideal input and output behaviors. Fig. 2.2 illustrates the schematic drawing of a 2-to-1 SC converter with finite terminal capacitances, with the simulated output impedance curves with different terminal capacitances presented in Fig. 2.2(b). As shown in Fig. 2.2(b), the output impedance curve can significantly deviate from the ideal scenario when the terminal capacitances are insufficient.

Although terminal capacitances can have considerable effects on the output impedance, there is currently no analytical tool that is able to characterize their effects quantitatively. The selection of C_{in} and C_{out} in the design of SC converters is mainly based on engineering experiences and trial and error. However, since the die area is typically limited and valu-

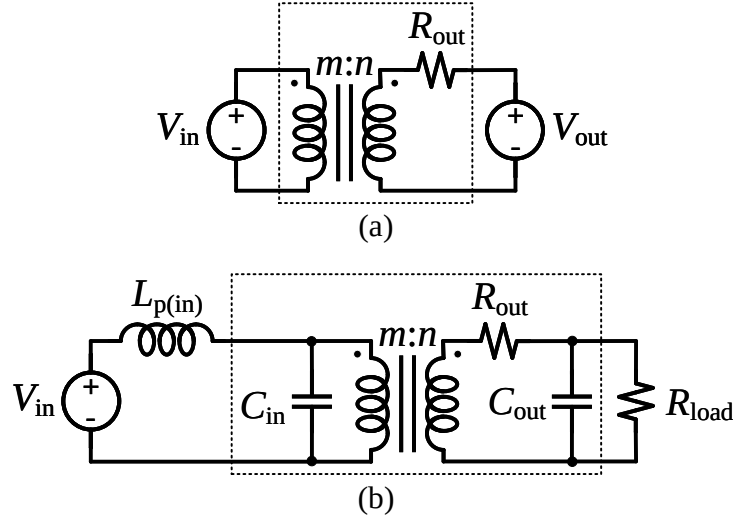


Figure 2.1: General steady-state model of an SC converter. (a) Idealized input and output. (b) Practical input and output. ($L_{p(in)}$: the parasitic source inductance)

able in integrated circuits such as CMOS converters, quantitative optimizations should be performed to find out the best combination of flying capacitances and terminal capacitances to achieve the lowest output impedance within the limited area. This indicates a need for a general analytical tool to characterize the effects of terminal capacitances in SC converters, which can help practicing engineers and researchers achieve the optimum converter size and performance.

In this chapter, a general modeling and analysis methodology for SC converters is proposed to characterize the effects of finite C_{in} and C_{out} . Section 2.2 explains the derivation of the proposed general output impedance model in detail. In Section 2.3, a 2-to-1 SC converter prototype is specially designed for model verification, and the modeling results agree well with experimental measurements with less than 8% relative error. To facilitate analysis, the proposed model is approximated by using Taylor expansion in Section 2.4.1 to obtain a simpler mathematical form. Based on the proposed model, it is revealed in Section 2.4.2 that the insufficiency of C_{in} can lead to a significant increase in output impedance, while smaller C_{out} can counter-intuitively help reduce the output impedance and achieve higher efficiency, although this benefit comes at the cost of a larger output voltage ripple. It is also revealed in Section 2.4.3 that the parasitic source inductance and the deadtime can have a nontrivial impact on the output impedance in the slow and fast switching regions, respectively. Based on the above findings, Section 2.4.4 provides several design guidelines. Further explanations for the applicability of the proposed model to arbitrary SC topologies are given in Section 2.5.

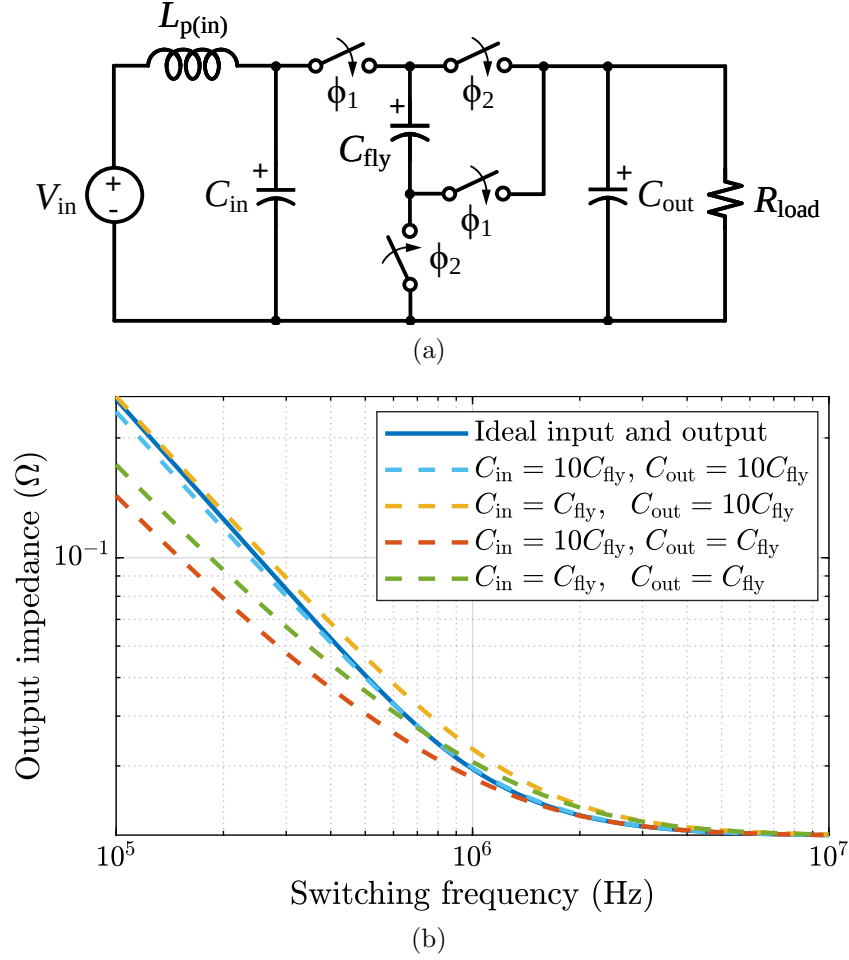


Figure 2.2: Output impedance of a 2-to-1 SC converter with different terminal capacitances. (a) Schematic drawing of the 2-to-1 SC converter. (b) Output impedance curves with different C_{in} and C_{out} . ($C_{fly} = 10 \mu\text{F}$, $R_{on} = 10 \text{ m}\Omega$)

2.2 General Output Impedance Model of Switched-Capacitor Converters With Finite Terminal Capacitances

2.2.1 Circuit Model

In a general circuit state (or phase) k , an SC topology can be viewed as an RC network and represented as the circuit model shown in Fig. 2.3. It consists of an equivalent resistance R_k and an equivalent capacitance C_k connected in series. With suitable (topology-dependent) R_k and C_k parameters, this general expression can capture any arbitrary SC topologies. The

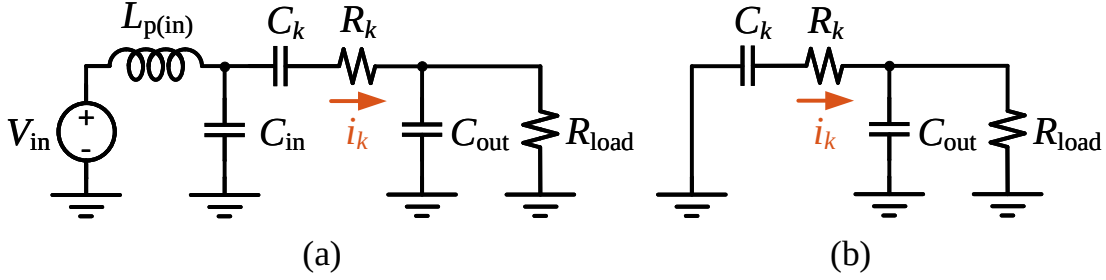


Figure 2.3: Complete circuit model of an SC converter with finite C_{in} and C_{out} . (a) Case 1: the input terminal is connected to the source. (b) Case 2: the input terminal is grounded.

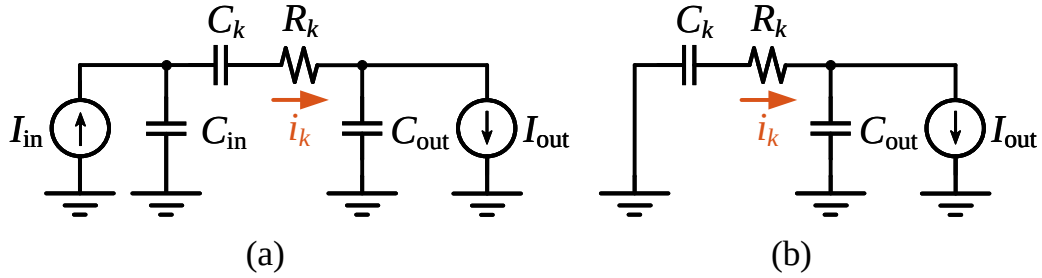


Figure 2.4: Simplified circuit model of an SC converter with finite C_{in} and C_{out} . (a) Case 1: the input terminal is connected to the source. (b) Case 2: the input terminal is grounded.

method of calculating the model parameters R_k and C_k for arbitrary SC topologies will be provided in Section 2.5.1.

As illustrated in Fig. 2.3, two cases should be considered due to the finite input capacitance. The SC converter can be represented as Fig. 2.3(a) when the input terminal is connected to the source and as Fig. 2.3(b) when the input terminal is grounded. As conventionally done in topology analysis, the second-order circuit model shown in Fig. 2.3 can be further simplified as the first-order model illustrated in Fig. 2.4. First, due to the existence of the parasitic source inductance $L_{p(in)}$ and the high-frequency operation of SC converters (SC converters typically operate above the critical switching frequency to reach the fast switching limit (FSL) [24]), it can be assumed that the input current ripple is sufficiently small so that V_{in} and $L_{p(in)}$ together can be regarded as a constant current source I_{in} . Second, since the output voltage ripple is typically designed to be small compared to the average dc output voltage, the ripple on the output current through the resistive load can also be ignored. In addition, some loads are inherently inductive and behave like current sources. Thus, the load can be modeled as a constant current source I_{out} .

2.2.2 Calculation of Output Impedance

By definition, the resistive output impedance R_{out} accounts for all conduction losses and charge-sharing losses in an SC converter. Therefore, R_{out} can be calculated with the average conduction loss P_{loss} as

$$R_{\text{out}} = \frac{P_{\text{loss}}}{I_{\text{out}}^2}. \quad (2.1)$$

Note that P_{loss} is the power loss averaged in one switching cycle and thus can be expressed with the summation of the energy losses over all phases as

$$P_{\text{loss}} = f_{\text{sw}} \sum_k E_k \quad (2.2)$$

where f_{sw} is the switching frequency. E_k represents the energy loss in phase k and can be calculated as

$$E_k = \int_0^{T_{k(\text{eff})}} R_k i_k^2(t) dt \quad (2.3)$$

in which i_k is the current through R_k in phase k and $T_{k(\text{eff})}$ is the effective duration of the phase k . Since there is no forced freewheeling operation in SC converters during the deadtime, the effective duration of phase k is

$$T_{k(\text{eff})} = T_k - t_d \quad (2.4)$$

where T_k is the duration of phase k and t_d is the deadtime.

2.2.3 Model Derivation

As indicated by (2.1)-(2.3), to calculate the output impedance, we need to find the explicit expression of i_k in all phases based on the first-order simplified model shown in Fig. 2.4 as

$$i_k(t) = (I_{0k} - I_{fk}) e^{-\frac{t}{\tau_k}} + I_{fk} \quad (2.5)$$

where I_{0k} and I_{fk} are the initial value and forced component of i_k in phase k , and τ_k represents the time constant of the equivalent circuit. τ_k and I_{fk} can be expressed as

$$\begin{cases} \tau_k = R_k C_{k(\text{eff})} \\ I_{fk} = p_k I_{\text{out}} \end{cases} \quad (2.6)$$

in which $C_{k(\text{eff})}$ is the effective capacitance and p_k is a dimensionless ratio. In the two cases illustrated in Fig. 2.4, for an m -to- n SC converter, $C_{k(\text{eff})}$ and p_k can be given as

$$\begin{aligned} \text{Case 1 : } & \begin{cases} C_{k(\text{eff})} = 1 / \left(\frac{1}{C_k} + \frac{1}{C_{\text{in}}} + \frac{1}{C_{\text{out}}} \right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{in}} C_{\text{out}}} \left(C_{\text{in}} + \frac{n}{m} C_{\text{out}} \right) \end{cases} \\ \text{Case 2 : } & \begin{cases} C_{k(\text{eff})} = 1 / \left(\frac{1}{C_k} + \frac{1}{C_{\text{out}}} \right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{out}}} \end{cases} \end{aligned} \quad (2.7)$$

Substituting (2.2)-(2.7) into (2.1) yields

$$R_{\text{out}} = \hat{R}_{\text{out}} + \sum_k R_k p_k (2a_k - p_k f_{\text{sw}} T_{k(\text{eff})}) \quad (2.8)$$

where

$$\begin{cases} \hat{R}_{\text{out}} = \frac{1}{2f_{\text{sw}}} \sum_k \frac{\hat{a}_k^2}{C_{k(\text{eff})}} \coth \left(\frac{T_{k(\text{eff})}}{2\tau_k} \right) \\ \hat{a}_k = a_k - p_k f_{\text{sw}} T_{k(\text{eff})} \end{cases} \quad (2.9)$$

in which a_k is the ratio of the transferred charged in phase k to the total delivered charge in a switching cycle. A detailed derivation of (2.8) is provided in Appendix B.1. The definition and calculation of a_k can be found in [24].

With ideal input and output, $C_{k(\text{eff})}$ and p_k become $C_{k(\text{eff})} = C_k$ and $p_k = 0$, so that

$$R_{\text{out}} = \hat{R}_{\text{out}} = \frac{1}{2f_{\text{sw}}} \sum_k \frac{a_k^2}{C_k} \coth \left(\frac{T_{k(\text{eff})}}{2\tau_k} \right) \quad (2.10)$$

which is the same as has been derived in [28].

2.3 Model Verification

In this section, a 2-to-1 SC converter prototype is designed to investigate the influence of terminal capacitances on the output impedance quantitatively. The accuracy of the proposed general model is verified by comparing the modeling results with circuit simulations and experimental measurements from 2-to-1 SC converter prototype.

2.3.1 Experimental Setup

Figures 2.5 and 2.6 present the schematic drawing and photograph of the 2-to-1 SC converter prototype for model verification, with the main components listed in Table 2.1. The test

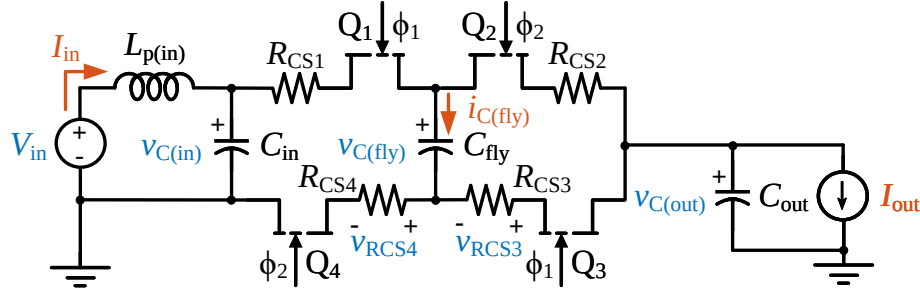


Figure 2.5: Schematic drawing of the 2-to-1 SC converter prototype.

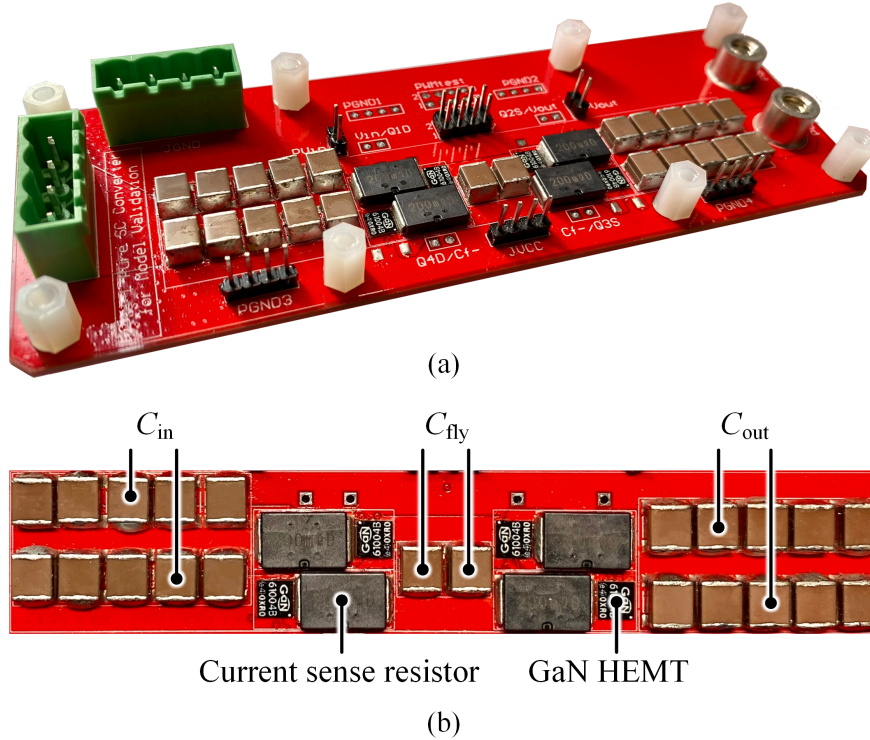


Figure 2.6: Photograph of the 2-to-1 SC converter prototype. (a) Overall view. (b) Top view with key components annotated.

condition is $V_{in} = 24$ V and $I_{out} = 1$ A. The input and output voltages are measured with digital multimeters Keysight 34405A and 34401A, respectively, and the output current I_{out} is measured by the E-load Rigol DL3031.

For the 2-to-1 SC converter shown in Fig. 2.6, the topology-dependent parameters in the output impedance model are $C_k = C_{fly}$, $R_k = 2(R_{on} + R_{CS}) + \text{ESR}_{C(fly)}$, $a_k = \frac{1}{2}$, and $T_k = \frac{1}{2f_{sw}}$ ($k = 1, 2$), where C_{fly} is the flying capacitance, R_{on} is the on-state resistance of

Table 2.1: Component list of the 2-to-1 SC converter prototype

Component	Part number	Parameters
GaN HEMT Q_1 - Q_4	GaN Systems GS61004B	100 V, 16 m Ω (@ 25 °C)
Current sense resistor R_{CS1} - R_{CS4}	KOA Speer SLN5TTEDR200D	200 m Ω , 7 W, 75 PPM/°C
Flying capacitor C_{fly}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μ F $\times 8$
Input and output capacitors C_{in} and C_{out}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μ F $\times 2 \times 40^*$
Gate driver	Analog Devices LTC4440	80 V, high-side
LDO voltage regulator	Texas Instruments LP2985AIM5-6.1/NOPB	2.5-16 V input, 6.1 V output
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky diode

* Measurements are performed with various terminal capacitances.

the GaN HEMT Q₁-Q₄, R_{CS} is the value of current sense resistors R_{CS1} - R_{CS4} , and $ESR_{C(fly)}$ is the ESR of C_{fly} . The reason why R_{CS1} - R_{CS4} are added in series with the GaN switches will be explained in the following section.

2.3.2 Experiment Design Considerations

There are two key considerations to achieve effective model verification:

1) *Ensure accurate parameter acquisition.* Since the precision of the predicted results is dependent on not only the correctness of the model itself but also the accuracy of the circuit parameters, we should ensure that the circuit parameters will not deviate from the nominal values provided in the manufacturers' datasheets during the measurement due to temperature variation, voltage bias, etc. There are two categories of variation-prone circuit parameters in the model: a) capacitances: C_{fly} , C_{in} , and C_{out} , and b) resistance: R_{on} and $ESR_{C(fly)}$.

KEMET C2220C474J5GACTU is a Class 1 capacitor with C0G dielectric that can maintain high capacitance stability over a wide range of operating temperature and voltage bias and has extremely low ESR and ESL. Therefore, we select it for C_{fly} , C_{in} , and C_{out} , so that the variation in the capacitances can be minimized and $ESR_{C(fly)}$ can be ignored (i.e. $ESR_{C(fly)} \approx 0$).

The on-state resistance of switching devices can vary significantly due to the changes in operating conditions (e.g. junction temperature, drain-to-source current, gate-to-source voltage, etc.). The on-state resistance of GaN HEMTs is particularly hard to accurately capture due to the dynamic on-state resistance phenomenon [39, 40].

To tackle this challenge, we add a high-precision current sense resistor (KOA Speer SLN5TTEDR200D) in series with each GaN switch to dominate the branch resistance. The current sense resistor can maintain high thermal stability (75 PPM/°C) and has a much higher resistance ($R_{CS} = 200 \text{ m}\Omega$) than the GaN switch ($R_{on} = 16 \text{ m}\Omega @ 25 \text{ }^\circ\text{C}$). As a result, the branch resistance can be stabilized by the current sense resistor against the variation in R_{on} . In addition, the cascaded bootstrap circuit with LDOs [41] is selected to drive the GaN switches since it can ensure stable gate drive voltage V_{drive} and minimize the variation in R_{on} resulting from the change in V_{drive} .

2) *Minimize the proportion of switching loss.* The proposed output impedance model can only capture the conduction losses and charge sharing losses in the SC converter. Therefore, to achieve effective model verification, we need to ensure that the converter operates in the conduction-loss-dominant condition, and the switching loss takes up only a small proportion of the total loss. Meanwhile, the converter needs to operate above 1 MHz to reach FSL. Therefore, we use GaN switches with small output capacitance and low gate charge and set the external gate resistance as $0 \text{ }\Omega$ to minimize the overlap loss.

2.3.3 Experimental Results

Figs. 2.7 and 2.8 show the comparison between the output impedances predicted by the proposed model (Model), simulated by PLECS (Sim.), and measured from the converter prototype (Expt.). Figs. 2.7(c) and 2.8(c) present the relative error of the modeling results with respect to the experimental measurements that is calculated by

$$\text{Relative error} = \frac{R_{\text{out(} \text{Model)}} - R_{\text{out(} \text{Expt.)}}}{R_{\text{out(} \text{Expt.)}}} \times 100\% \quad (2.11)$$

where $R_{\text{out(} \text{Model)}}$ and $R_{\text{out(} \text{Expt.)}}$ are the output impedance predicted by the model and measured from the prototype, respectively.

As can be seen in Figs. 2.7 and 2.8, the modeling results are in excellent agreement with the circuit simulations and the experimental measurements. The relative error of the modeling results with respect to the experimental measurements is less than 8% for various C_{in} and C_{out} within 100 kHz-2 MHz switching frequency range, covering the slow switching limit (SSL) and FSL. This indicates the excellent accuracy of the proposed general output impedance model and its applicability in a wide range of switching frequencies.

It should be noted that the relative error grows higher when the switching frequency increases. This is mainly due to the increase in the switching loss resulting from higher switching frequency. In addition, the relative error rises dramatically as the switching frequency decreases when C_{in} is small. This results from the undesired oscillation between $L_{\text{p(in)}}$ and C_{in} , which will be further explored in Section 2.4.3.

2.4 Effect Analysis of Terminal Capacitances

With the general model derived and verified in Sections 2.2 and 2.3, we will use it to explore the effect of finite terminal capacitances on the output impedance of SC converters in this section.

2.4.1 Model Approximation by Taylor Expansion

Although the general output impedance model is accurate within a wide range of switching frequency, it can be too complex to provide intuitive engineering insight. The existence of the hyperbolic function $\coth(x)$ makes it hard to handle mathematically. Therefore, to facilitate analysis, we approximate (2.8) with Taylor expansion to obtain a simplified mathematical form. Inspired by the concepts of SSL and FSL [24], we perform model approximation in the slow and fast switching regions separately, and name the obtained models as *slow switching model (SSM)* and *fast switching model (FSM)*, respectively.

For simplicity, here we perform the approximation to the model of the 2-to-1 SC converter prototype presented in Section 2.3 as an example. Note that this approximation technique is applicable to arbitrary SC topologies. To simplify calculation, we set $R_{\text{CS}} = 0 \Omega$ and

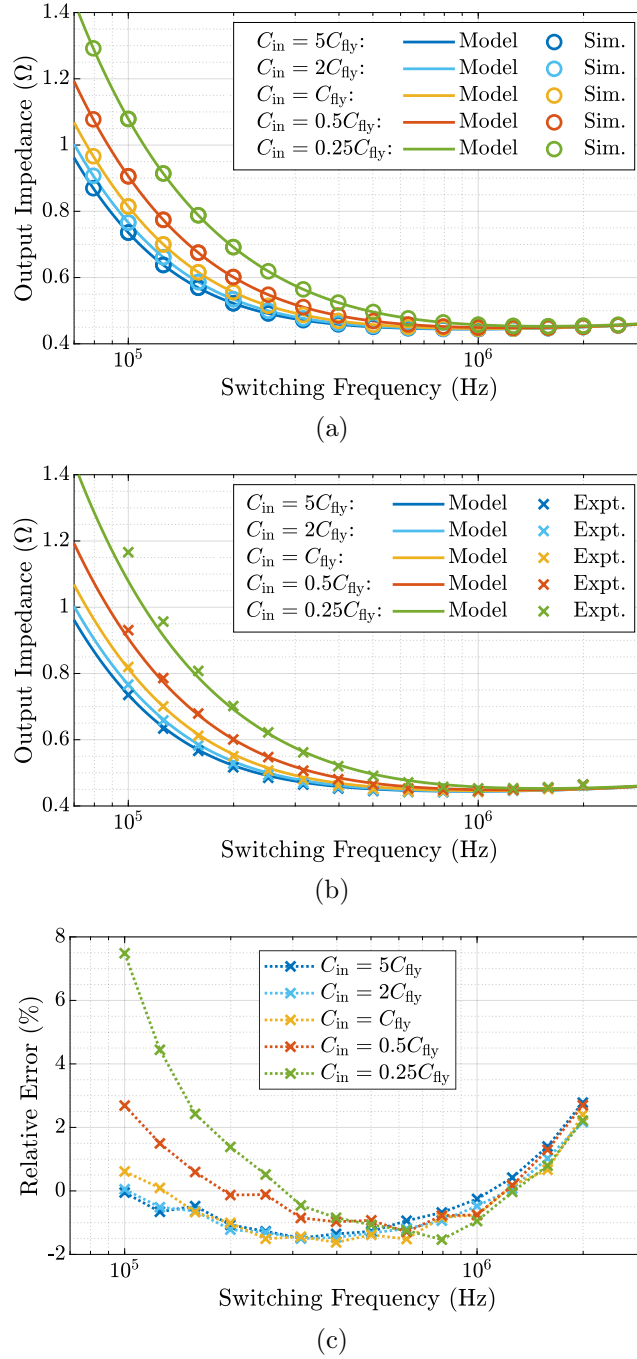


Figure 2.7: Output impedance of the SC converter with various C_{in} . ($C_{out} = 5C_{fly}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated by PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.). (c) Relative error of modeling results with respect to experimental measurements calculated with (2.11).

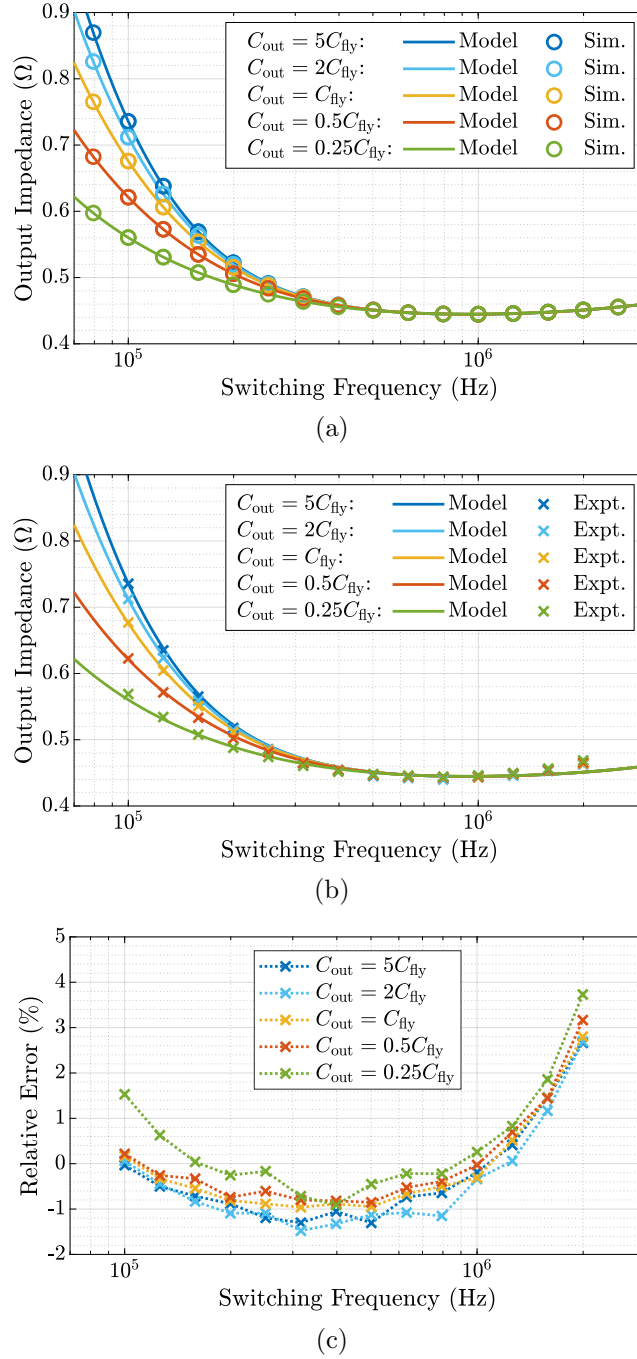


Figure 2.8: Output impedance of the SC converter with various C_{out} . ($C_{in} = 5C_{fly}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated by PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.). (c) Relative error of modeling results with respect to experimental measurements calculated with (2.11).

Table 2.2: Maximum relative errors of the approximated SSM and FSM in (2.12) with various C_{in} and C_{out}

k_{in}^{-1} or k_{out}^{-1}	10	7	5	4	3	2	1	0.5	0.25
$C_{\text{in}} = k_{\text{in}}^{-1} C_{\text{fly}},$ $C_{\text{out}} = 10 C_{\text{fly}}$	7.40%	7.27%	7.25%	7.18%	6.91%	7.32%	7.44%	10.6%	15.1%
$C_{\text{out}} = k_{\text{out}}^{-1} C_{\text{fly}},$ $C_{\text{in}} = 10 C_{\text{fly}}$	7.40%	6.89%	6.51%	6.06%	5.84%	4.95%	3.00%	1.52%	0.58%

assume negligible capacitor ESR and deadtime t_d . In the following examples in this section, $C_{\text{fly}} = 10 \mu\text{F}$, $R_{\text{on}} = 10 \text{ m}\Omega$.

Using Taylor expansion, we can approximate the output impedance model given in (2.8) for a 2-to-1 SC converter as

$$\begin{cases} R_{\text{SSM}} = \left(b + \frac{c}{s}\right) R_{\text{on}}, & s < s_c \\ R_{\text{FSM}} = \left(2 + \frac{d}{s^2}\right) R_{\text{on}}, & s \geq s_c \end{cases} \quad (2.12)$$

where

$$\begin{cases} s = 8f_{\text{sw}} R_{\text{on}} C_{\text{fly}}, & s_c = \frac{1 + k_{\text{in}}/2 + k_{\text{out}}}{\sqrt{3}} \\ k_{\text{in}} = \frac{C_{\text{fly}}}{C_{\text{in}}}, & k_{\text{out}} = \frac{C_{\text{fly}}}{C_{\text{out}}} \\ b = 2 - \frac{(1 + k_{\text{in}}/2)^2}{(1 + k_{\text{in}} + k_{\text{out}})^2} - \frac{1}{(1 + k_{\text{out}})^2} \\ c = \frac{(1 + k_{\text{in}}/2)^2}{1 + k_{\text{in}} + k_{\text{out}}} + \frac{1}{1 + k_{\text{out}}} \\ d = \frac{(1 + k_{\text{in}}/2)^2 + 1}{3} \end{cases} \quad (2.13)$$

in which s is a dimensionless product of the switching frequency f_{sw} and the time constant $R_{\text{on}} C_{\text{fly}}$ and is defined as the normalized switching frequency. Parameter s_c is the critical normalized frequency that marks the boundary between SSM and FSM, and k_{in} and k_{out} are the ratios of C_{fly} to C_{in} and C_{out} , respectively. A detailed derivation of (2.12) is provided in Appendix B.1.1.

Fig. 2.9 shows the comparison between the precise model given in (2.8) and the approximated models (SSM and FSM) shown in (2.12). Table 2.2 lists the maximum relative errors of the approximated model with various C_{in} and C_{out} . From Fig. 2.9, we can see that the maximum relative error always appears at the critical frequency s_c . Table 2.2 shows that SSM and FSM can approximate the precise model within 8% relative error except for the cases with extremely small C_{in} .

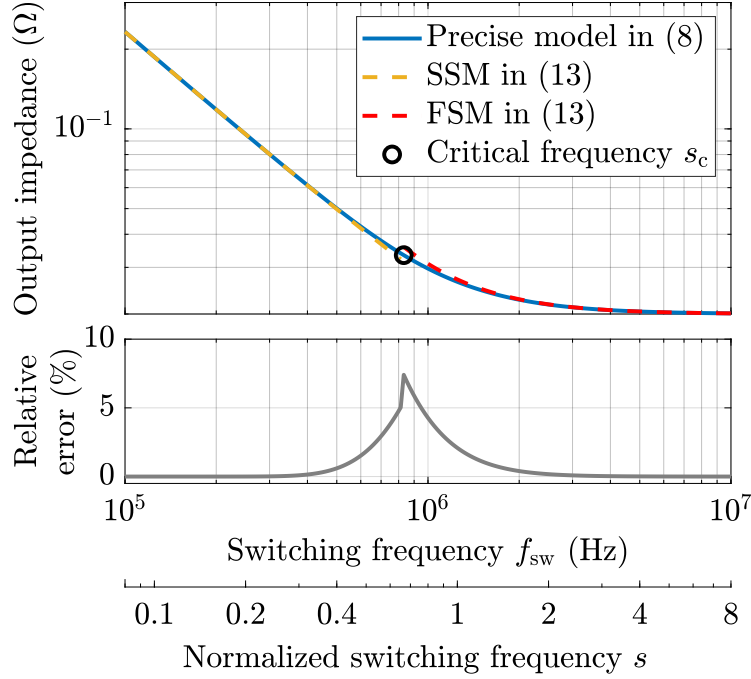


Figure 2.9: Comparison between the precise model in (2.8) and the approximated SSM and FSM in (2.12). ($C_{\text{in}} = C_{\text{out}} = 10C_{\text{fly}}$)

In the slow switching region that ensures complete charge transfer, we have $s \ll 1$ which yields the SSL in (2.14). When the switching frequency is sufficiently high so that the current through C_{fly} is almost constant in each phase, $s \gg 1$ and therefore yields the FSL in (2.14).

$$\begin{cases} R_{\text{SSM}} \approx R_{\text{SSL}} = \frac{c}{s} R_{\text{on}}, & s \ll 1 \\ R_{\text{FSM}} \approx R_{\text{FSL}} = 2R_{\text{on}}, & s \gg 1 \end{cases}. \quad (2.14)$$

When the terminal capacitances are sufficiently large so that the input and output can be regarded as constant voltage sources, k_{in} and k_{out} are approximately zero so that we get $R_{\text{SSL}} = \frac{1}{4C_{\text{fly}}f_{\text{sw}}}$ and $R_{\text{FSL}} = 2R_{\text{on}}$, which is expected and well-known.

2.4.2 Effect of Finite Terminal Capacitances

In this section, we first evaluate (2.12) to analyze the effect of terminal capacitances qualitatively, then perform quantitative analysis with numerical calculations, and finally explore the physical origins for these effects with circuit simulations.

1) *Qualitative analysis.* In the SSM of (2.12), when C_{in} becomes smaller, k_{in} increases so that c becomes greater, resulting in higher R_{SSM} . Conversely, with smaller C_{out} , k_{out} increases so that c becomes smaller, contributing to lower R_{SSM} . It is favorable, although

counter-intuitive, that decreasing C_{out} can help reduce the output impedance since this will contribute to both higher power density and higher efficiency. But note that this benefit comes at the cost of a larger output voltage ripple. C_{out} should still be sufficiently large to satisfy any ripple constraint.

In the FSM of (2.12), the coefficient d is only dependent on k_{in} while it is independent of k_{out} . This indicates that C_{out} has little effect on R_{FSM} . By inspection, we can predict that reducing C_{in} will lead to higher R_{FSM} .

2) *Quantitative analysis.* Figs. 2.10 and 2.11 show quantitative comparisons of the output impedance of 2-to-1 SC converters with different terminal capacitances. To generalize the analysis, Figs. 2.10 and 2.11 are plotted with the normalized switching frequency s in (2.13) ($s = 8f_{\text{sw}}R_{\text{on}}C_{\text{fly}}$), with the output impedance normalized to the FSL impedance as $R_{\text{out}}/R_{\text{FSL}}$ ($R_{\text{FSL}} = 2R_{\text{on}}$). It can be observed that smaller C_{in} leads to higher output impedance, while the output impedance becomes lower when C_{out} is smaller.

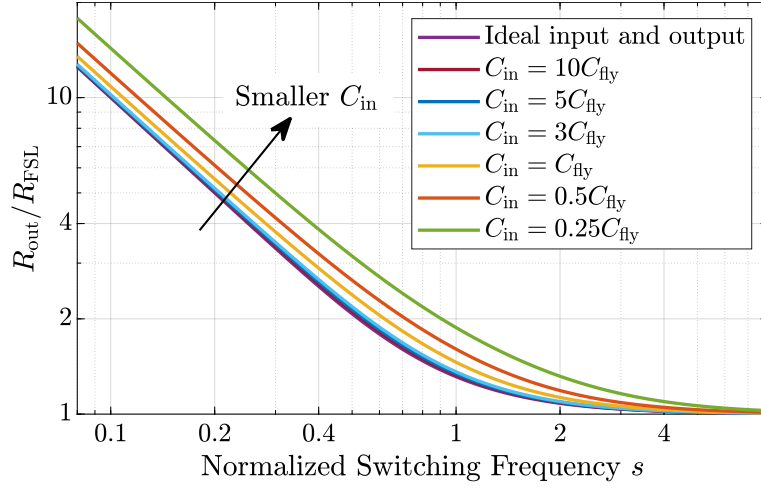
As has been predicted in the qualitative analysis, C_{out} has no influence on the output impedance in the fast switching region. Instead, C_{in} exhibits a greater effect in this region, especially around the knee of the output impedance curve. Since SC converters typically operate around the knee point, C_{in} should be carefully designed to avoid the undesired increase in the output impedance due to insufficient C_{in} . These findings are consistent with those from the qualitative analysis and the experimental results presented in Figs. 2.7 and 2.8.

In addition, it can be observed in Fig. 2.7 that $C_{\text{in}} = 3C_{\text{fly}}$ is sufficient to approximate an ideal input. However, further reduction in C_{in} can cause a significant increase in the output impedance, which harms efficiency. On the contrary, smaller C_{out} can always help reduce the output impedance. Moreover, in the slow switching region, C_{out} exhibits a stronger influence on the output impedance than C_{in} . For example, Fig. 2.10(b) shows that reducing C_{in} to $0.25C_{\text{fly}}$ can increase R_{out} by a factor of 1.5, while it is presented in Fig. 2.11(b) that reducing C_{out} to $0.25C_{\text{fly}}$ can decrease R_{out} by a factor of 0.3.

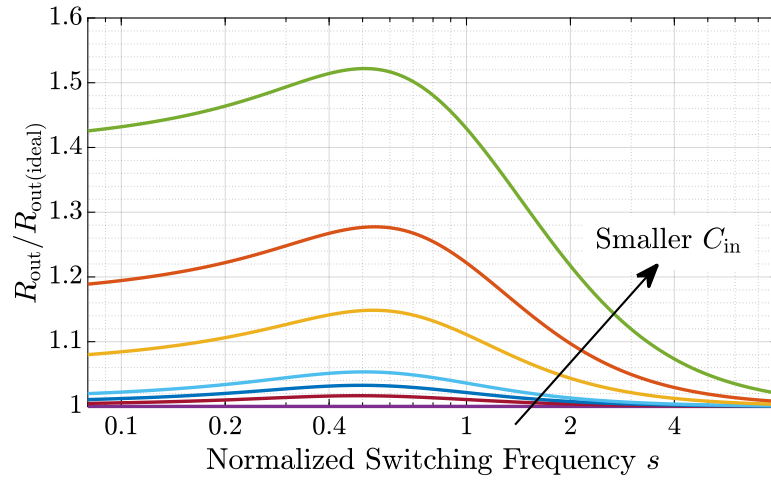
3) *Physical origins.* Fig. 2.12 compares the simulated waveforms of the 2-to-1 SC converter with large and small input capacitances, assuming ideal output. Fig. 2.12 shows that with smaller C_{in} , the voltage difference seen by C_{fly} ($V_{C(\text{in})} - V_{C(\text{out})} - V_{C(\text{fly})}$) becomes much larger. This results in a higher peak value of $i_{C(\text{fly})}$ in the case 1 shown in Fig. 2.4. Consequently, as listed in Table 2.3, the RMS value of $i_{C(\text{fly})}$ becomes higher when C_{in} is smaller, which leads to greater loss and higher output impedance.

Fig. 2.13 presents a similar comparison of output impedance between the 2-to-1 SC converter with large and small output capacitances, assuming ideal input. As listed in Table 2.4, the RMS value of $i_{C(\text{fly})}$ becomes lower with smaller C_{out} . This is because the output voltage ($V_{C(\text{out})}$) is able to follow $V_{C(\text{fly})}$ more rapidly when C_{out} is smaller. Consequently, $i_{C(\text{fly})}$ drops faster and thus has a lower RMS value, which contributes to less loss and lower output impedance.

In summary, reducing C_{in} exacerbates the imbalance of capacitor voltages between the two cases of Fig. 2.4, which increases the RMS value of $i_{C(\text{fly})}$. On the contrary, decreasing C_{out} accelerates the charge sharing processes, thus resulting in a lower RMS value of

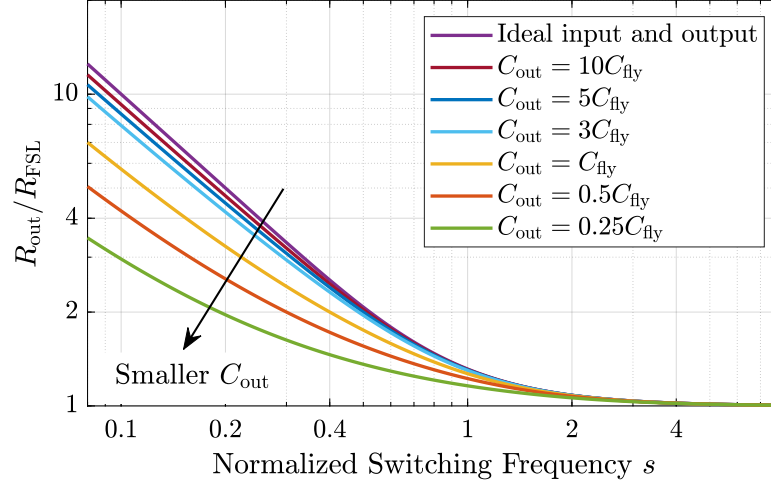


(a)

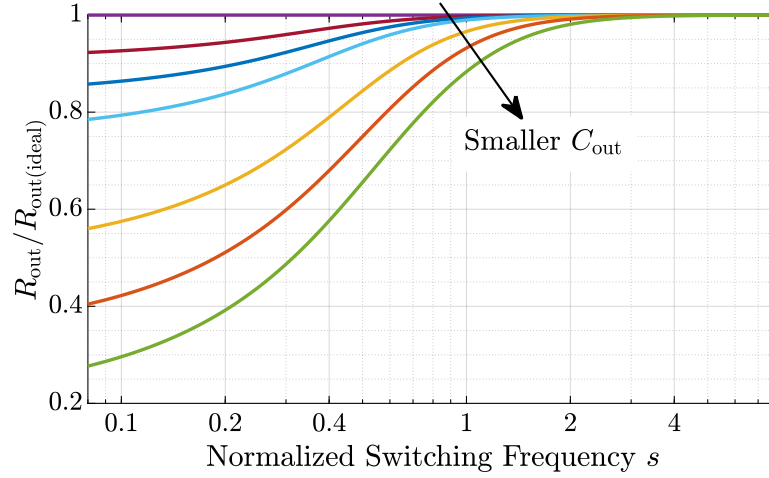


(b)

Figure 2.10: Effect of C_{in} on output impedance. (Assuming ideal output) (a) Normalized output impedance $R_{\text{out}}/R_{\text{FSL}}$ with various C_{in} . (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{\text{out(ideal)}}$.



(a)



(b)

Figure 2.11: Effect of C_{out} on input impedance. (Assuming ideal output) (a) Normalized output impedance $R_{\text{out}}/R_{\text{FSL}}$ with various C_{out} . (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{\text{out(ideal)}}$.

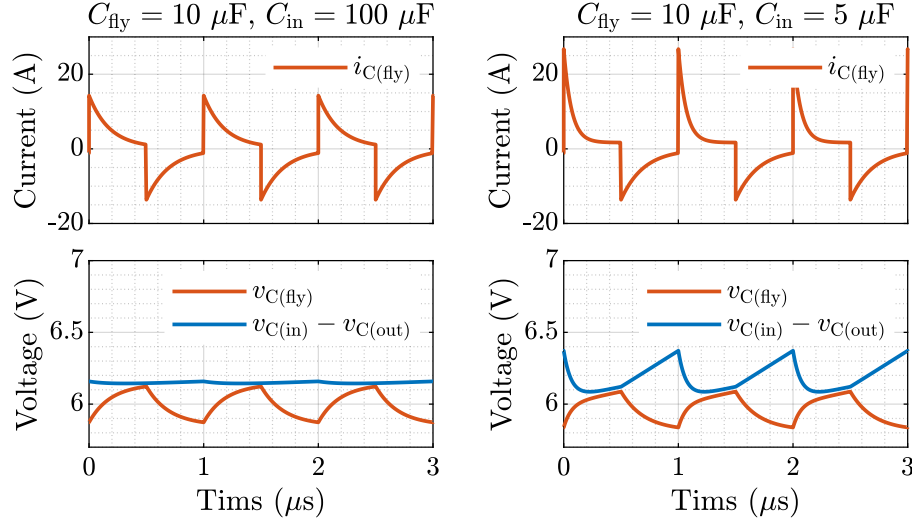


Figure 2.12: Comparison of simulated waveforms between large and small C_{in} cases. (Assuming ideal output, $C_{fly} = 10 \mu\text{F}$, $f_{sw} = 1 \text{ MHz}$, $I_{out} = 5 \text{ A}$)

Table 2.3: Comparison between the RMS and peak-to-peak values of the simulated $i_{C(fly)}$ waveforms between large and small C_{in} cases (Assuming ideal output, $C_{fly} = 10 \mu\text{F}$, $f_{sw} = 1 \text{ MHz}$, $I_{out} = 5 \text{ A}$)

$i_{C(fly)}$ \ C_{in}	100 μF	10 μF	5 μF
RMS value	6.18 A	6.49 A	6.84 A
Peak-to-peak value	28.6 A	34.0 A	40.6 A

$i_{C(fly)}$. This accounts for the opposite effects of C_{in} and C_{out} on the output impedance of SC converters. Experimental corroboration of the above simulation analyses and theoretical findings is provided below.

2.4.2.1 Experimental Corroboration for the Effect Analysis of Finite Terminal Capacitances

To corroborate the theoretical findings in Section 2.4.2, this Section presents and compares three sets of simulated and experimental waveforms shown in Figs. 2.14–2.16 with different C_{in} and C_{out} values. The experimental waveforms were measured from the hardware prototype presented in Figs. 2.5 and 2.6. Current sense resistor voltages v_{RCS3} and v_{RCS4} were measured to obtain the current through the flying capacitor $i_{C(fly)}$ as

$$i_{C(fly)} = \frac{-v_{RCS3} + v_{RCS4}}{R_{CS}}. \quad (2.15)$$

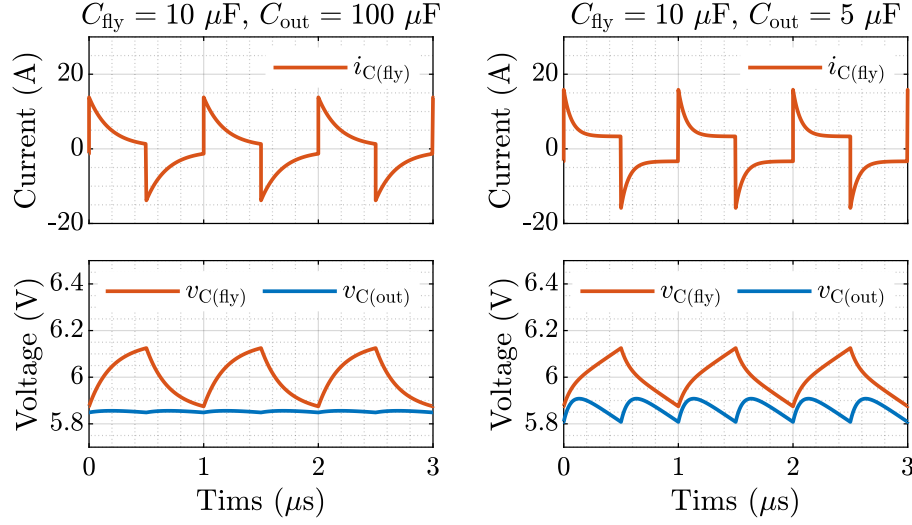


Figure 2.13: Comparison of simulated waveforms between large and small C_{out} cases. (Assuming ideal input, $C_{fly} = 10 \mu\text{F}$, $f_{sw} = 1 \text{ MHz}$, $I_{out} = 5 \text{ A}$)

Table 2.4: Comparison between the RMS and peak-to-peak values of the simulated $i_{C(fly)}$ waveforms between large and small C_{out} cases (Assuming ideal input, $C_{fly} = 10 \mu\text{F}$, $f_{sw} = 1 \text{ MHz}$, $I_{out} = 5 \text{ A}$)

$i_{C(fly)}$ \ C_{out}	100 μF	10 μF	5 μF
RMS value	6.07 A	5.95 A	5.81 A
Peak-to-peak value	28.2 A	30.7 A	32.7 A

As can be seen in Figs. 2.14–2.16, the simulated and experimental waveforms are in excellent agreement. In addition, the waveforms presented in Figs. 2.14–2.16 qualitatively match those in Figs. 2.12 and 2.13. The comparison between Fig. 2.14 and Fig. 2.15 shows that a smaller C_{in} leads to a larger voltage difference seen by C_{fly} ($V_{C(in)} - V_{C(out)} - V_{C(fly)}$), which results in higher RMS and peak-to-peak values of $i_{C(fly)}$ as listed in Table 2.5 and thus higher output impedance. Similarly, the comparison between Fig. 2.14 and Fig. 2.16 shows that the output voltage ($V_{C(out)}$) is able to follow $V_{C(fly)}$ when C_{out} is smaller. As a results, $i_{C(fly)}$ drops faster and thus has a lower RMS value as listed in Table 2.5, which contributes to less power loss and lower output impedance.

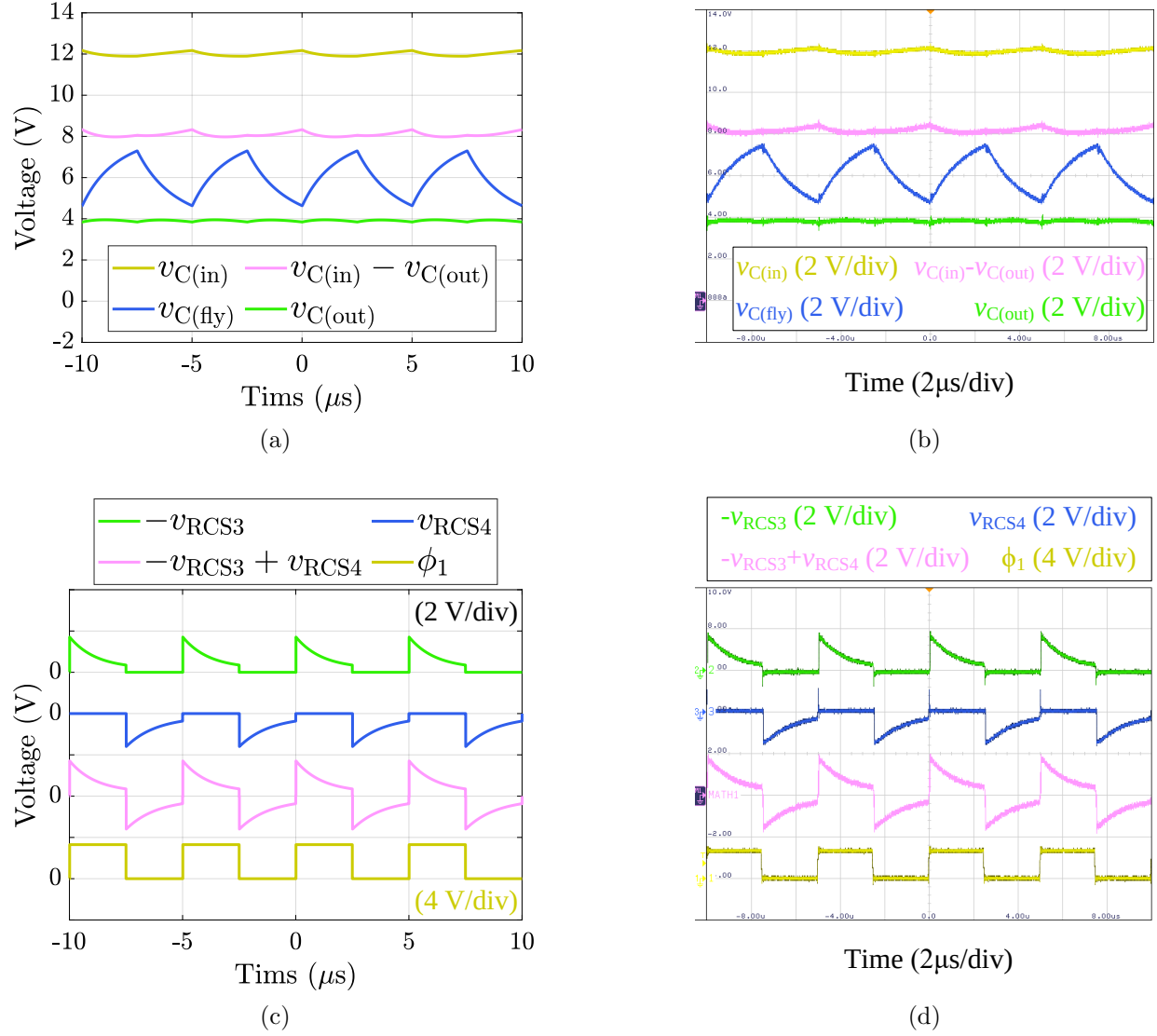


Figure 2.14: Comparison between simulated and experimental waveforms when $C_{\text{in}} = C_{\text{out}} = 5C_{\text{fly}}$. (a) Simulated capacitor voltage waveforms. (b) Experimental capacitor voltage waveforms. (c) Simulated voltage waveforms across current sense resistors. (d) Experimental voltage waveforms across current sense resistors.

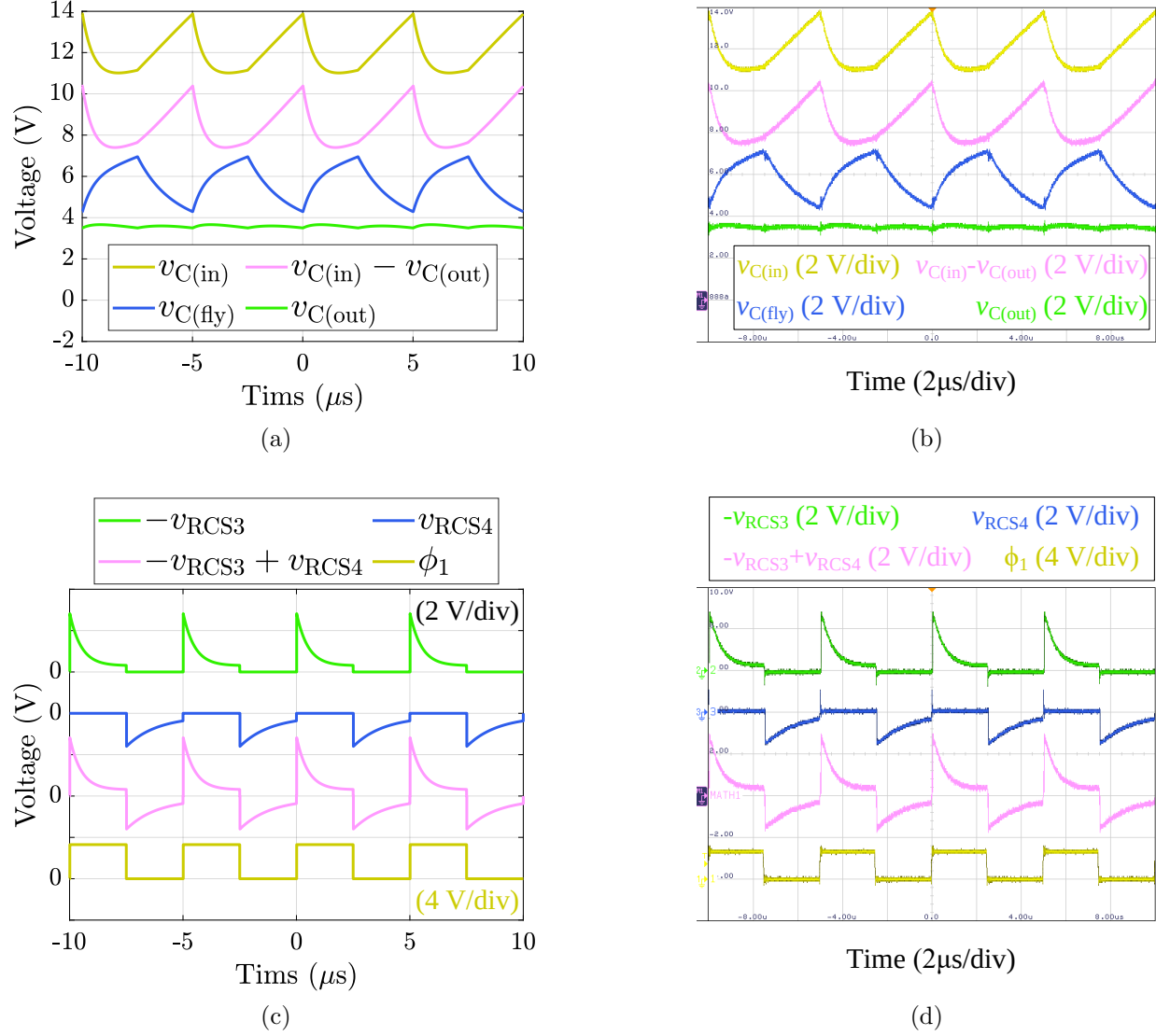


Figure 2.15: Comparison between simulated and experimental waveforms when $C_{in} = 0.5C_{fly}$, $C_{out} = 5C_{fly}$. (a) Simulated capacitor voltage waveforms. (b) Experimental capacitor voltage waveforms. (c) Simulated voltage waveforms across current sense resistors. (d) Experimental voltage waveforms across current sense resistors.

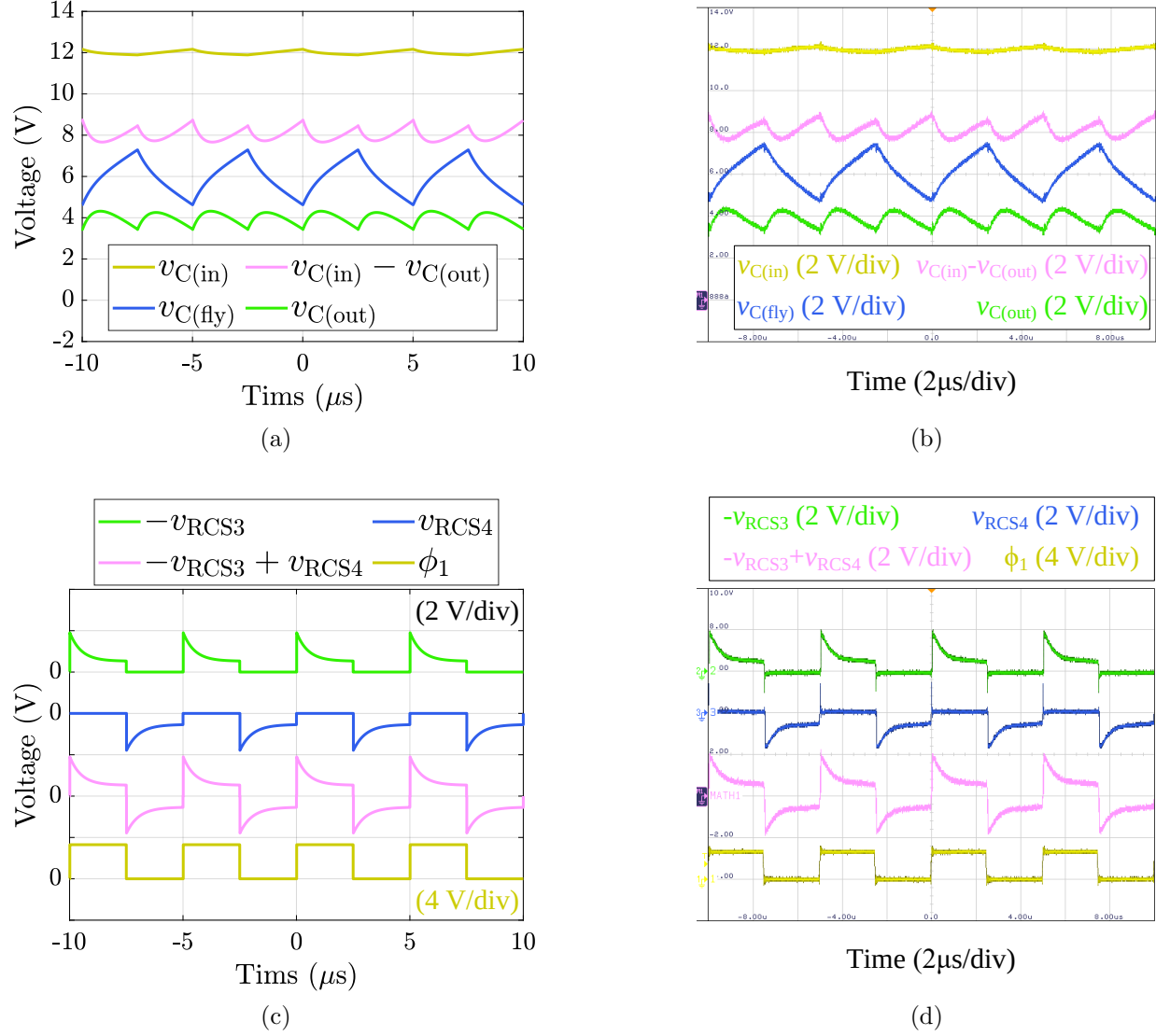
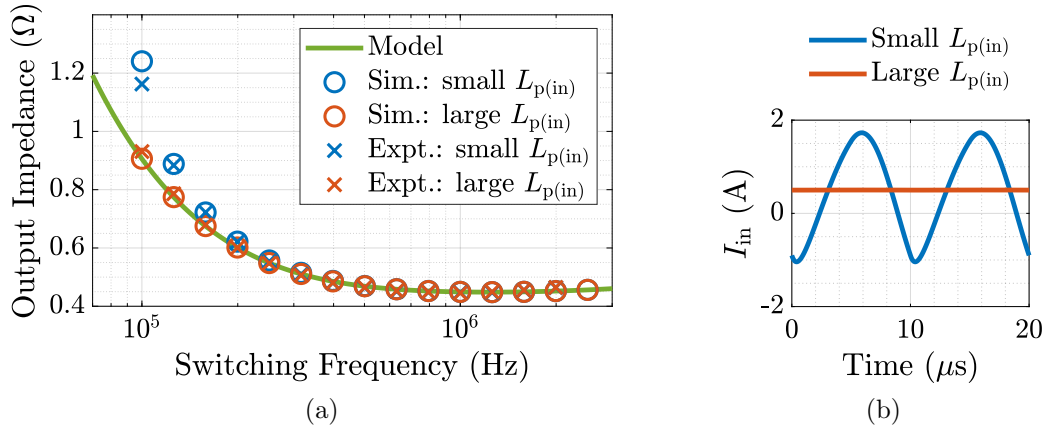


Figure 2.16: Comparison between simulated and experimental waveforms when $C_{\text{in}} = 5C_{\text{fly}}$, $C_{\text{out}} = 0.5C_{\text{fly}}$. (a) Simulated capacitor voltage waveforms. (b) Experimental capacitor voltage waveforms. (c) Simulated voltage waveforms across current sense resistors. (d) Experimental voltage waveforms across current sense resistors.

Table 2.5: Comparison between the RMS and peak-to-peak values of the simulated (Sim.) and experimental (Expt.) $i_{C(\text{fly})}$ waveforms with different C_{in} and C_{out} values

$C_{\text{in}}/C_{\text{fly}}$ $C_{\text{out}}/C_{\text{fly}}$		5 5 (Fig. 2.14)	0.5 5 (Fig. 2.15)	5 0.5 (Fig. 2.16)
RMS value of $i_{C(\text{fly})}$	Sim.	4.40 A	4.73 A	4.33 A
	Expt.	4.48 A	4.82 A	4.39 A
Peak-to-peak value of $i_{C(\text{fly})}$	Sim.	16.5 A	22.1 A	18.4 A
	Expt.	19.1 A	23.8 A	20.7 A


 Figure 2.17: Effect of $L_{p(\text{in})}$ on the output impedance of the 2-to-1 SC converter prototype. ($C_{\text{in}} = 0.5C_{\text{fly}}$, $C_{\text{out}} = 5C_{\text{fly}}$) (a) Output impedance with small and large L_{in} . (b) Simulated waveforms of I_{in} with small and large L_{in} . ($f_{\text{sw}} = 100$ kHz)

2.4.3 Other Practical Considerations

1) *Resonance between $L_{p(\text{in})}$ and C_{in} .* As shown in Fig. 2.17(a), it is observed both in simulation (Sim.) and experiment (Expt.) that, with low C_{in} , there will be an undesired increase in the output impedance in the slow switching region when $L_{p(\text{in})}$ is small. This phenomenon is due to the resonance between $L_{p(\text{in})}$ and C_{in} , and can be explained as follows.

As C_{in} becomes smaller and smaller, the resonant frequency of $L_{p(\text{in})}$ and C_{in} , which can be given as $f_{r(\text{in})} = \frac{1}{2\pi\sqrt{L_{p(\text{in})}C_{\text{in}}}}$, gradually increases. When the switching frequency approaches $f_{r(\text{in})}$, the input current I_{in} will start to oscillate largely between positive and negative values, as illustrated in Fig. 2.17(b). Such oscillation can dramatically increase the input voltage ripple and therefore augment the voltage difference seen by C_{fly} , thus leading to higher RMS value of $i_{C(\text{fly})}$ and higher output impedance.

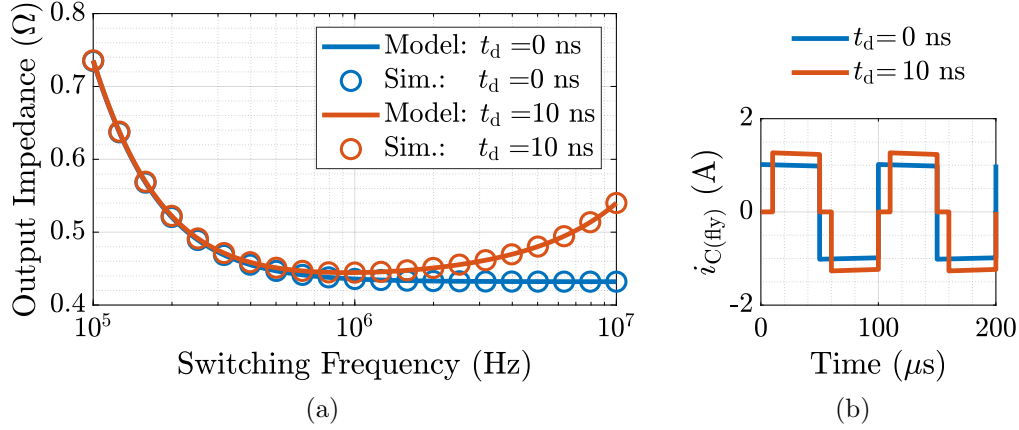


Figure 2.18: Effect of deadtime on the output impedance of the 2-to-1 SC converter prototype. ($C_{in} = C_{out} = 5C_{fly}$) (a) Output impedance with and without deadtime. (b) Simulated waveforms of $i_{C(fly)}$ with and without deadtime. ($f_{sw} = 10$ MHz)

It is worth noting that the above analysis is only an example of how the $L_{p(in)}-C_{in}$ resonance can affect the input voltage ripple and output impedance of SC converters. Realistic input impedance networks can be more complex and can affect not only the performance but also the stability of power converters. Detailed effect analysis of the resonance between the source impedance and C_{in} is out of the scope of this chapter and can be a good research topic for future works.

2) *Effect of deadtime.* As shown in Fig. 2.18(a), at very high switching frequency (i.e. beyond several MHz), a practical deadtime t_d of several ns can lead to an unexpected increase in output impedance. This effect can be accurately captured by the proposed model by introducing the effective duration of conduction given in (2.7).

As illustrated in Fig. 2.18(b), the average value of $i_{C(fly)}$ in each phase should be the same no matter how long the deadtime is. However, with longer deadtime, the conduction duration of $i_{C(fly)}$ will become shorter, which leads to a higher RMS value and thus higher conduction loss. This indicates that deadtime is also a factor that impedes increasing f_{sw} in practice, apart from higher switching loss.

3) *Multiphase interleaving.* As discussed in [27, 33], for integrated SC converters, there is usually no penalty for multiphase interleaving. In multiphase interleaved SC converters, the flying capacitor(s) of one SC converter unit can serve as the terminal capacitor(s) for other units. Therefore, with sufficient interleaved phases, no explicit terminal capacitors are needed so that the majority of die area can be used to implement the flying capacitance.

The application of the proposed output impedance model to multiphase interleaved SC converters is out of the scope of this chapter and can be a worthwhile topic for future studies. Discussions on how to capture the effect of interleaving can be found in [27].

2.4.4 Design Guidelines

- Size of the input capacitance: Since an insufficient input capacitance can increase the output impedance and harm overall efficiency, C_{in} should be sufficiently large to ensure an approximately ideal input behavior. In particular, when Class 2 capacitors are used as the input capacitor, special attention should be paid to ensure that C_{in} is sufficient, since Class 2 capacitors suffer from dc derating with applied input voltage.
- Size of the output capacitance: The output capacitance can be appropriately reduced to achieve both smaller physical size and lower output impedance (i.e. both higher power density and higher efficiency). However, C_{out} should still be sufficiently large to satisfy the ripple constraint on the output voltage.
- Other practical considerations: 1) In the slow switching region, the resonance between $L_{\text{p(in)}}$ and C_{in} can cause an undesired increase in the output impedance. This can be avoided by ensuring sufficient C_{in} or operating at a higher switching frequency. 2) At very high switching frequency (i.e. beyond several MHz), a practical deadtime t_d of several nano-seconds can lead to a considerable increase in the output impedance and therefore can no longer be neglected in the analysis and design of SC converters.

Further quantitative optimizations can be performed to find the best combination of C_{fly} , C_{in} , and C_{out} to achieve the lowest output impedance within the given physical space limits and voltage ripple constraints.

2.5 Application to Arbitrary Switched-Capacitor Topologies

In this section, we apply the proposed modeling and analysis methodology to four commonly-used SC topologies: series-parallel, Fibonacci, doubler, and Dickson topologies, as shown in Fig. 2.19. These four examples are provided here to demonstrate the applicability of this model to arbitrary SC topologies. The set of converters considered in this section is limited to two-phase SC converters operating at 50% duty cycle. In the following examples, for simplicity, all flying capacitors have the same capacitance $C_{\text{fly}} = 10 \mu\text{F}$, and all switching devices have the same on-state resistance $R_{\text{on}} = 10 \text{ m}\Omega$.

2.5.1 Model Application to Arbitrary SC Topologies

As has been mentioned in Section 2.2.1, the circuit model shown in Fig. 2.4 can capture arbitrary SC topologies with suitable topology-dependent parameters. Therefore, the key step of applying the proposed model to an arbitrary SC topology is to obtain the equivalent capacitance C_k and equivalent resistance R_k in each phase.

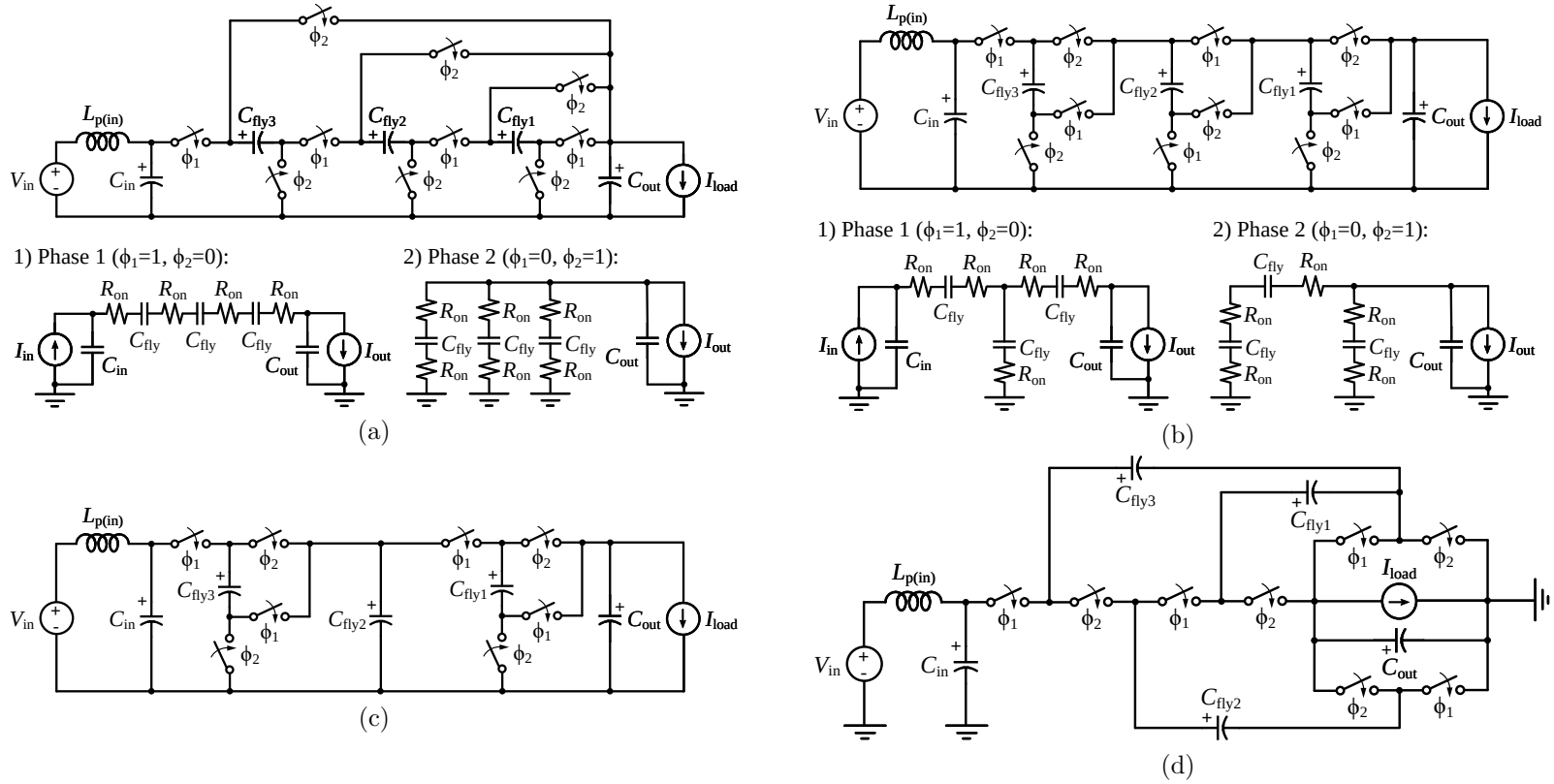


Figure 2.19: Common SC topologies. (a) 4-to-1 series-parallel topology and its equivalent circuit in each phase. (b) 5-to-1 Fibonacci topology and its equivalent circuit in each phase. (c) 4-to-1 doubler topology. (d) 4-to-1 Dickson topology.

There are two cases: a) the simple case where C_k and R_k can be directly acquired by inspection, and b) the general case where the model parameters have to be carefully derived.

1) *Simple case.* Apart from the 2-to-1 SC topology, the series-parallel topology is also an example of the simple case. Take the 4-to-1 series-parallel topology illustrated in Fig. 2.19(a) as an example—the model parameters of the series phase (i.e. phase 1) are $C_1 = \frac{1}{3}C_{\text{fly}}$ and $R_1 = 4R_{\text{on}}$, and those of the parallel phase (i.e. phase 2) are $C_2 = 3C_{\text{fly}}$ and $R_2 = \frac{2}{3}R_{\text{on}}$, which can be obtained from the equivalent circuits shown in Fig. 2.19(a) by inspection.

2) *General case.* In more general cases, C_k and R_k cannot be directly obtained by inspection from the equivalent circuits but have to be carefully derived according to the invariance of the SSL and FSL output impedance.

On the one hand, with ideal input and output, the asymptotic SSL and FSL output impedances of two-phase SC converters have been given in [24] as

$$\begin{cases} R_{\text{SSL}} = \frac{1}{f_{\text{sw}}} \sum_{i \in \text{caps}} \frac{(a_{\text{c},i})^2}{C_{\text{fly},i}} \\ R_{\text{FSL}} = 2 \sum_{i \in \text{switches}} R_{\text{on},i} (a_{\text{r},i})^2 \end{cases} \quad (2.16)$$

in which $C_{\text{fly},i}$ is the value of flying capacitor i , $R_{\text{on},i}$ is the on-state resistance of switch i , and $a_{\text{c},i}$ and $a_{\text{r},i}$ are the charge multipliers of capacitor i and switch i , respectively.

On the other hand, according to the proposed model, the output impedance of a SC converter with ideal input and output is given by (2.10). By performing the model approximation introduced in Section 2.4.1, the asymptotic SSL and FSL output impedances of (2.10) can be obtained as

$$\begin{cases} R_{\text{SSL}} = \frac{1}{2f_{\text{sw}}} \sum_k \frac{a_k^2}{C_k} \\ R_{\text{FSL}} = 2 \sum_k R_k a_k^2 \end{cases} \quad (2.17)$$

The SSL and FSL output impedances in (2.16) and (2.17) should be the same, and therefore we get

$$\begin{cases} \sum_k \frac{a_k^2}{C_k} = 2 \sum_{i \in \text{caps}} \frac{(a_{\text{c},i})^2}{C_{\text{fly},i}} \\ \sum_k R_k a_k^2 = \sum_{i \in \text{switches}} R_{\text{on},i} (a_{\text{r},i})^2 \end{cases} \quad (2.18)$$

Splitting (2.18) into each phase yields

$$\begin{cases} C_k = a_k^2 / \left(\sum_{i \in \text{caps}} \frac{(a_{\text{c},i})^2}{C_{\text{fly},i}} \right) \\ R_k = \frac{1}{a_k^2} \sum_{i \in \text{switches}} \delta_{i,k} R_{\text{on},i} (a_{\text{r},i})^2 \end{cases} \quad (2.19)$$

where $\delta_{i,k}$ equals 1 when switch i is ON in phase k and equals 0 when it is OFF in phase k .

Here, take the 5-to-1 Fibonacci converter illustrated in Fig. 2.19(b) as an example—we can obtain the model parameters as $C_1 = \frac{2}{3}C_{\text{fly}}$, $C_2 = \frac{3}{2}C_{\text{fly}}$, $R_1 = \frac{11}{4}R_{\text{on}}$, and $R_2 = \frac{16}{9}R_{\text{on}}$. With the C_k and R_k values, we can calculate the output impedance of SC converters with ideal input and output by substituting (2.19) into (2.10).

To take the effect of finite C_{in} into consideration, we need to make further modification to C_1 (i.e. the C_k value in case 1 of Fig. 2.4). Denote the charge multiplier of C_{in} as $a_{\text{c,in}}$, which is defined as the ratio of the charge transferred in C_{in} in one phase to the total charge delivered to the output during a full switching period. For two-phase SC converters operating at 50% duty cycle, the charge transferred in C_{in} in one phase is

$$q_{\text{c,in}} = \frac{T}{2}I_{\text{in}} = \frac{T}{2} \left(\frac{n}{m}I_{\text{out}} \right) = \frac{n}{2m}q_{\text{out}}. \quad (2.20)$$

Thus, $a_{\text{c,in}}$ can be obtained by inspection as

$$a_{\text{c,in}} = \frac{n}{2m}. \quad (2.21)$$

Similar to the flying capacitors, the contribution of the input capacitor to the SSL output impedance is proportional to $a_{\text{c,in}}^2/C_{\text{in}}$ which has the same mathematical form of R_{SSL} in (2.16). Therefore, compared to the situation with ideal input, due to the existence of finite C_{in} , the contribution of phase 1 (case 1 in Fig. 2.4) to R_{SSL} is increased by

$$f_1 = 1 + \left(\frac{a_{\text{c,in}}^2}{C_{\text{in}}} \right) / \left(\sum_{i \in \text{caps}} \frac{(a_{\text{c},i})^2}{C_{\text{fly},i}} \right). \quad (2.22)$$

This means that we can incorporate the effect of C_{in} in the model by modifying the C_1 in (2.19) with the factor f_1 as

$$C'_1 = \frac{C_1}{f_1} \quad (2.23)$$

while still mathematically assuming ideal input in the calculation. Note that here we do not assume C_{in} to be physically infinite but only introduce a mathematical simplification. Additionally, note that since C_{in} is hard-charged in phase 1 and soft-charged by $L_{\text{p(in)}}$ in phase 2, it only leads to a greater contribution of phase 1 to R_{SSL} but has no influence on the contribution of phase 2 to R_{SSL} , which means only C_1 needs to be modified while C_2 does not.

To sum up, there are four steps to apply the proposed model to arbitrary SC topologies:

- i) calculate the model parameters C_k and R_k with (2.19),
- ii) modify C_1 with the factor f_1 given in (2.22) as (2.23),
- iii) substitute C'_1 and C_2 into the case 2 of (2.3) to calculate $C_{k(\text{eff})}$ and p_k for each phase,
- iv) substitute $C_{k(\text{eff})}$, p_k and R_k into (2.8), and calculate R_{out} .

Fig. 2.20 presents the output impedance of the four SC topologies shown in Fig. 2.19 with various terminal capacitances. The comparison between modeling and simulation results in

Fig. 2.20 demonstrates the accuracy of the proposed output impedance model in different SC topologies with various terminal capacitances. Note that the proposed output impedance model is widely applicable to arbitrary SC topologies with practical C_{in} and C_{out} values but can be inaccurate in extreme scenarios that are not usual in practical applications, such as when C_{out} is less than C_{fly} .

2.5.2 Effect of Terminal Capacitances

As can be observed in Fig. 2.20, qualitatively speaking, the terminal capacitances exhibit the same effects on output impedance in these common SC topologies as in the 2-to-1 SC converter analyzed in Section 2.4—the insufficiency of C_{in} leads to higher output impedance while smaller C_{out} helps reduce output impedance. Quantitatively speaking, we can notice that C_{out} is more influential in the slow switching region while C_{in} has a stronger effect at higher frequency around the knee of the output impedance curve.

It can also be observed that the effect of C_{in} is weaker in these four SC topologies in comparison with the 2-to-1 SC converter. In the four SC topologies shown in Fig. 2.20, the output impedance with $C_{\text{in}} = C_{\text{fly}}$ is very close to that with $C_{\text{in}} = 10C_{\text{fly}}$. SC topologies with higher conversion ratio generally have smaller equivalent capacitance (C_k) in the phase where the input terminal is connected to the source (i.e. case 1 in Fig. 2.4). Given that the output impedance is dependent on the series capacitance of C_{in} and C_k , C_{in} needs to be smaller to make the same impact on the output impedance of SC topologies with higher conversion ratio. This is a favorable feature, which means smaller C_{in} can be sufficient to ensure an approximately ideal input behavior in SC converters with a higher conversion ratio.

2.6 Chapter Summary

This chapter proposes a general modeling and analysis methodology that is able to characterize the effect of finite terminal capacitances on the output impedance of SC converters. A general output impedance model is derived and verified by circuit simulations and experimental measurements from a 2-to-1 SC converter prototype with less than 8% relative error. It is revealed that larger C_{in} is favorable for efficiency improvement. On the contrary, smaller C_{out} can help reduce output impedance, which contributes to both higher efficiency and higher power density, although C_{out} should still be sufficiently large to satisfy the ripple constraint on the output voltage. In addition, C_{out} is quantitatively more influential in the slow switching region while C_{in} has a stronger effect on output impedance in the fast switching region, especially around the knee of the output impedance curve where SC converters typically operate. Finally, we demonstrate the applicability of the proposed modeling and analysis methodology to arbitrary SC topologies with four examples of commonly-used SC converters.

This chapter provides an analytical tool for future investigations, such as design optimizations of SC converters with physical space limits and voltage ripple constraints.

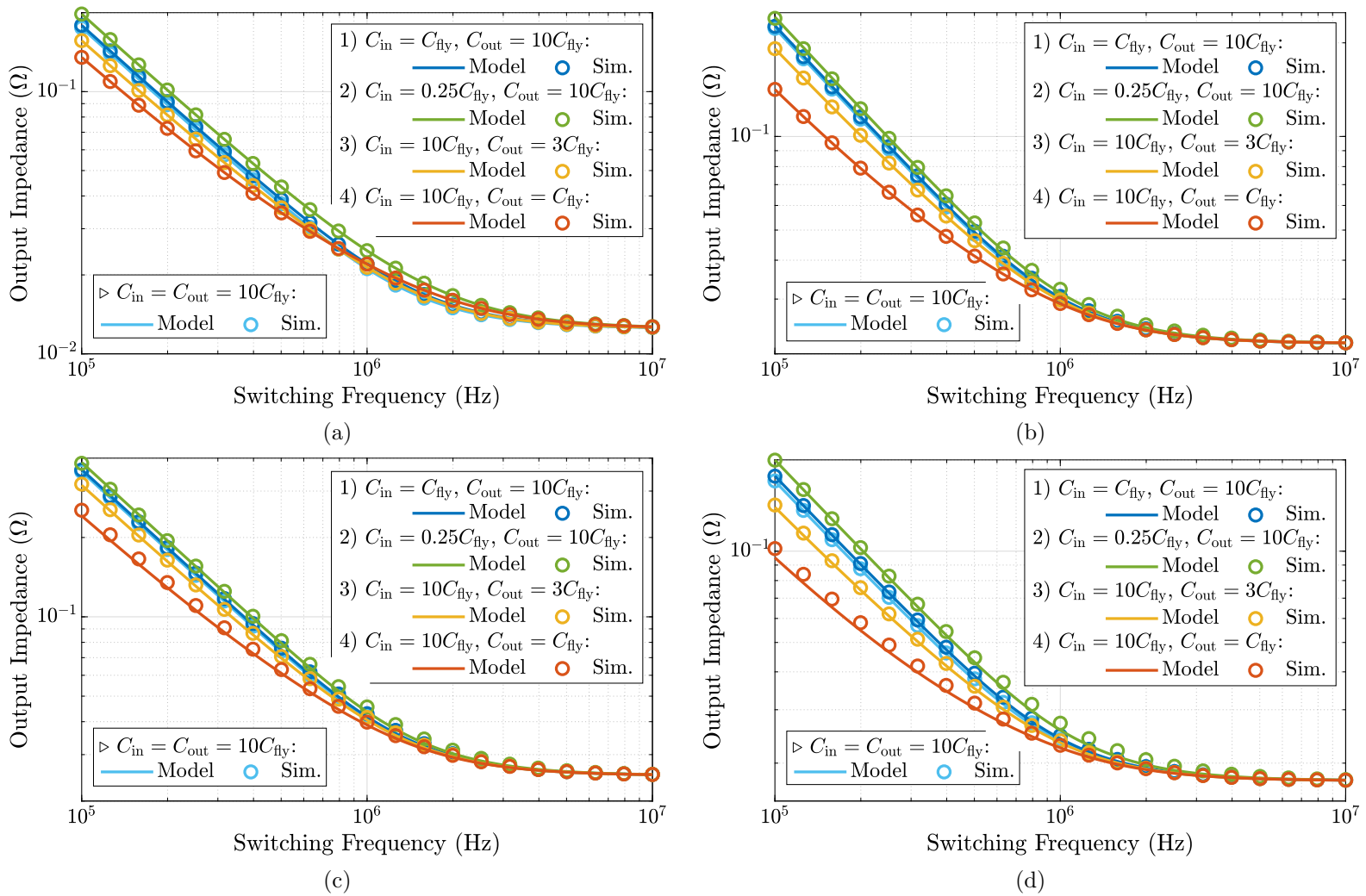


Figure 2.20: Output impedance of common SC topologies with various terminal capacitances and comparison between modeling (Model) and simulation (Sim.) results. (a) 4-to-1 series-parallel topology. (b) 5-to-1 Fibonacci topology. (c) 4-to-1 doubler topology. (d) 4-to-1 Dickson topology.

Chapter 3

Modeling and Analysis of Resonant SC Converters with Finite Terminal Capacitances

3.1 Background and Motivation

Originating from the conventional pure switched-capacitor (SC) converters [7, 24], resonant switched-capacitor (ReSC) converters can not only leverage the greatly superior energy densities of capacitors compared to inductors and transformers but also significantly reduce the inherent capacitor charge sharing loss with soft-charging operation enabled by the augmenting inductor(s) [42–44]. Therefore, ReSC converters open up new opportunities for achieving record-breaking high efficiency and high power density, and have recently received increasing attention in various applications [45–52].

Although pre-existing models [53–55] and analyses [43, 56, 57] of ReSC converters assume input and/or output to be ideal voltage sources as illustrated in Fig. 3.1(a), practical implementations of ReSC converters involve input and output capacitors (C_{in} and C_{out}) to stabilize the terminal voltages, as illustrated in Fig. 3.1(b). If the terminal capacitances are much larger than the flying capacitance (i.e. $C_{\text{in}}, C_{\text{out}} \geq 10C_{\text{fly}}$), the input and output can be regarded as ideal voltage sources. However, in practical applications, the sizes of C_{in} and C_{out} are constrained by space and cost, and thus usually not large enough to ensure ideal input and output behaviors. Fig. 3.2 illustrates the simulated output impedance of a 2-to-1 ReSC converter with different C_{in} and C_{out} , which shows that the actual output impedance curve can significantly deviate from the ideal scenario when the terminal capacitances are insufficient.

Despite the significant effects of finite terminal capacitances, currently there exists no model that can quantitatively characterize their effects on the performance of ReSC converters. In practice, the sizes of C_{in} and C_{out} are selected mainly based on engineering experiences and through trial and error, indicating the great need for a general method to model and

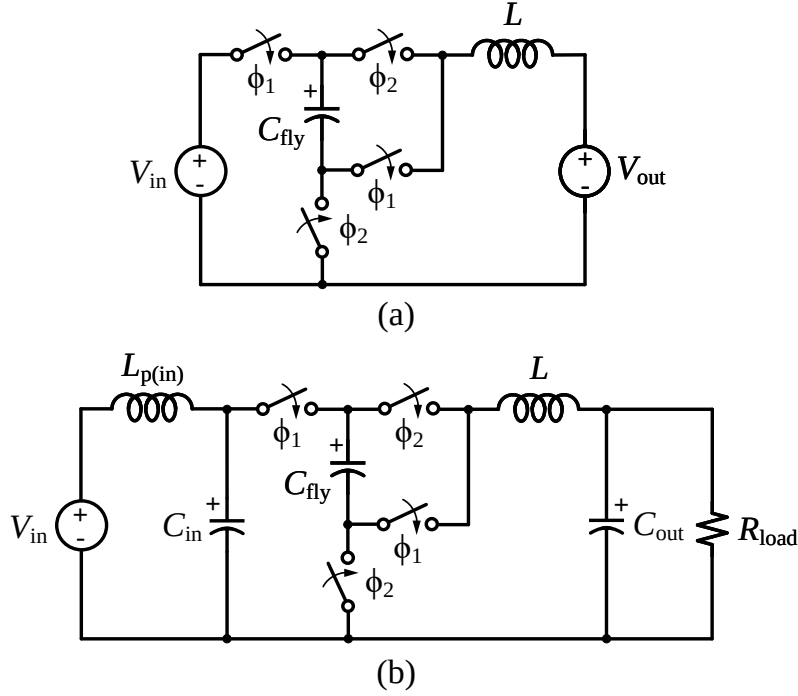


Figure 3.1: Schematic of a 2-to-1 resonant switched-capacitor (ReSC) converter. (a) With idealized input and output. (b) With practical input and output. ($L_{p(in)}$: the parasitic source inductance)

analyze the effects of terminal capacitances.

This chapter proposes a general modeling and analysis methodology that can capture the effects of finite terminal capacitances on the output impedance of ReSC converters. With the proposed model derived and verified in Sections 3.2 and 3.3, respectively, Section 3.4 reveals the effects of C_{in} and C_{out} based on simulation and experimental results. It is revealed that the insufficiency in terminal capacitances will result in higher critical switching frequency, and C_{in} has stronger influence on critical switching frequency than C_{out} . The set of converters discussed in this chapter is limited to two-phase ReSC converters with a single augmenting inductor at the output that can achieve full soft-charging operation.

3.2 General Output Impedance Model of ReSC Converters With Finite Terminal Capacitances

3.2.1 Circuit Model

In a general circuit state (or phase) k , a two-phase ReSC converter can be modeled as the equivalent circuit shown in Fig. 3.3 consisting of an equivalent resistance R_k , an equivalent

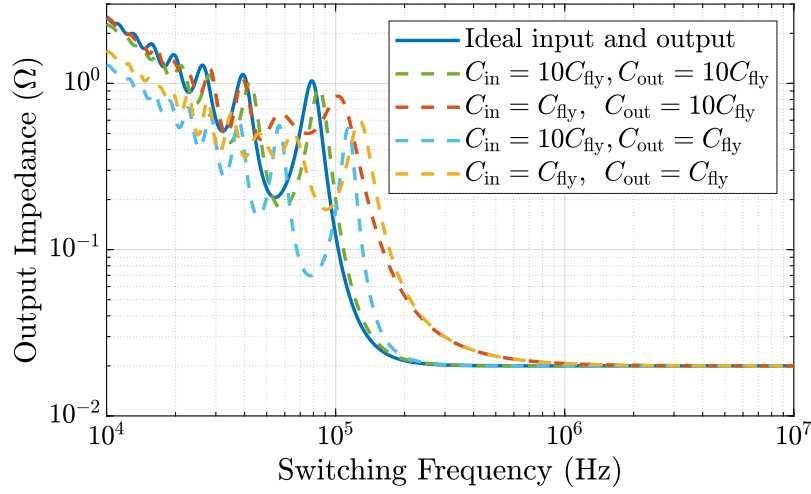


Figure 3.2: Output impedance of a 2-to-1 ReSC converter with different C_{in} and C_{out} . ($C_{fly} = 10 \mu\text{F}$, $L = 0.1 \mu\text{H}$, $R_{on} = 10 \text{ m}\Omega$)

lent capacitance C_k and an augmenting inductor L at the output. Note that this general expression is able to capture any arbitrary ReSC topologies with a single inductor at the output that can achieve full soft-charging operation with (topology-dependent) equivalent R_k and C_k values. With nonideal input, two cases should be considered. Figs. 3.3(a) and (b) illustrate the equivalent circuits for the cases when the input terminal is connected to the source and when it is grounded, respectively.

Since the complete model shown in Fig. 3.3 is a third-order circuit that is difficult to handle, it has to be simplified to be practically useful. Due to the existence of the parasitic source inductance $L_{p(in)}$ (e.g. the parasitic inductance on the source cable) and the high switching frequency of ReSC converters, the input current ripple is typically sufficiently small so that we can regard the source as an ideal constant current source I_{in} . Similarly, since the output voltage ripple of ReSC converters are typically designed to be small compared to the average dc output voltage, the current through the resistive load can also be viewed as an ideal constant current source I_{out} . In fact, some loads are intrinsically inductive and behave like a constant current source. Therefore, for simplicity (and as conventionally done in topology analysis), the third-order complete circuit model shown in Fig. 3.3 can be simplified as the second-order model illustrated in Fig. 3.4.

3.2.2 Calculation of Output Impedance

Since the resistive output impedance R_{out} accounts for all conduction losses in the ReSC converter, it can be calculated with the average conduction power loss P_{loss} as

$$R_{out} = \frac{P_{loss}}{I_{out}^2}. \quad (3.1)$$

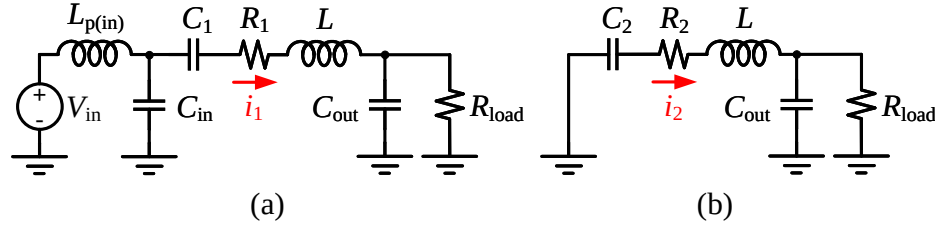


Figure 3.3: Complete circuit model of a two-phase ReSC converter with finite terminal capacitances. (a) In phase 1, the input terminal is connected to the source. (b) In phase 2, the input terminal is grounded.

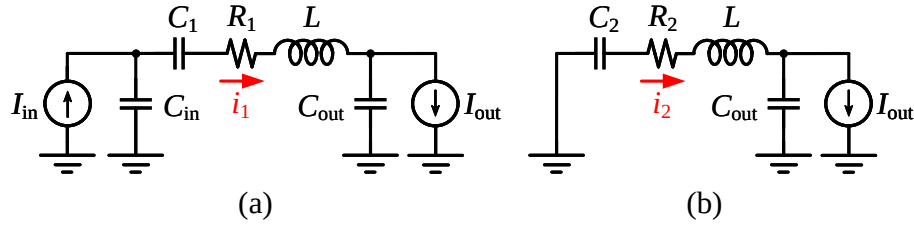


Figure 3.4: Simplified circuit model of a two-phase ReSC converter with finite terminal capacitances. (a) In phase 1, the input terminal is connected to the source. (b) In phase 2, the input terminal is grounded.

Note that P_{loss} is the power loss averaged in one switching cycle and thus can be expressed as the summation of the energy losses over all phases:

$$P_{loss} = f_{sw} \sum_{k=1,2} E_k \quad (3.2)$$

where f_{sw} is the switching frequency and E_k represents the conduction energy loss in phase k which can be expressed as

$$E_k = \int_0^{D_k T} R_k i_k^2(t) dt. \quad (3.3)$$

3.2.3 Model Derivation

As explained in [43], ReSC converters are typically designed to be highly underdamped ($\frac{R}{2} \sqrt{\frac{C}{L}} \ll 1$, i.e. with high quality factor Q) so that they can reach the fast switching limit (FSL) impedance at much lower switching frequency compared to pure SC converters with the same R and C parameters. Therefore, in the following analysis, we assume that the ReSC converter is underdamped in both phases. Thus, in phase k of the simplified circuit

model shown in Fig. 3.4, the inductor current i_k can be expressed as

$$i_k(t) = A_k e^{-\alpha_k t} \cos(\omega_k t + \varphi_k) + I_{fk} \quad (3.4)$$

where A_k is the amplitude, α_k is the decay rate, ω_k is the angular frequency, φ_k is the initial phase angle, and I_{fk} is the forced dc component of i_k in phase k , which can be expressed as

$$\begin{aligned} \alpha_k &= \frac{R_k}{2L} & \omega_{0k} &= \frac{1}{\sqrt{LC_{k(\text{eff})}}} \\ \omega_k &= \sqrt{\omega_{0k}^2 - \alpha_k^2} & I_{fk} &= p_k I_{\text{out}} \end{aligned} \quad (3.5)$$

in which $C_{k(\text{eff})}$ is the effective capacitance and p_k is a dimensionless ratio. In the two cases illustrated in Fig. 3.4, for an m -to- n ReSC converter, $C_{k(\text{eff})}$ and p_k can be given as

$$\begin{aligned} \text{Phase 1 : } & \begin{cases} C_{k(\text{eff})} = 1 / \left(\frac{1}{C_k} + \frac{1}{C_{\text{in}}} + \frac{1}{C_{\text{out}}} \right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{in}} C_{\text{out}}} \left(C_{\text{in}} + \frac{n}{m} C_{\text{out}} \right) \end{cases} \\ \text{Phase 2 : } & \begin{cases} C_{k(\text{eff})} = 1 / \left(\frac{1}{C_k} + \frac{1}{C_{\text{out}}} \right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{out}}} \end{cases} \end{aligned} \quad (3.6)$$

To find out the unknowns A_k and φ_k in (3.4), we need two additional conditions. First, since the inductor current i_k must be continuous at every switching instant, the following condition should be satisfied:

$$i_k(0) = i_{\bar{k}}(D_{\bar{k}}T) \quad (3.7)$$

where T is switching period, D_k is the duty ratio of phase k , and the label $\bar{k}$ is defined as

$$\bar{k} = \begin{cases} 1, & k = 2 \\ 2, & k = 1 \end{cases} \quad (3.8)$$

Second, according to the charge balance of the flying capacitor(s) in the periodic steady state, the charge delivered to the output in phase k can be expressed as

$$q_k = a_k q_{\text{out}} \quad (3.9)$$

where

$$q_k = \int_0^{D_k T} i_k(t) dt \quad q_{\text{out}} = I_{\text{out}} T \quad (3.10)$$

in which a_k is the ratio of the transferred charged in phase k to the total delivered charge in a switching cycle. The definition and calculation of a_k can be found in [24].

By substituting (3.4) into (3.7) and (3.9), we can find the unknowns A_k and φ_k and thus the explicit expression of i_k . Then, substituting i_k into (3.1)-(3.3) yields

$$R_{\text{out}} = \sum_{k=1,2} \left[\hat{R}_k + R_k p_k (2a_k - D_k p_k) \right] \quad (3.11)$$

where

$$\hat{R}_k = R_k \cdot \frac{[(a_k - D_k p_k) \omega_{0k}]^2}{4f_{\text{sw}}} \cdot \frac{(G_k - H_{k,2}) T_k^2 + 2H_{k,1} T_k + (G_k + H_{k,2})}{(M_{k,1} T_k + M_{k,2})^2} \quad (3.12)$$

and

$$\begin{aligned} \beta_k &= \frac{D_k \alpha_k}{f_{\text{sw}}} \quad \gamma_k = \frac{D_k \omega_k}{f_{\text{sw}}} \quad G_k = \frac{\omega_{0k}^2}{\alpha_k} (e^{2\beta_k} - 1) \\ \begin{cases} M_{k,1} = \omega_k [\cos(\gamma_k) - e^{\beta_k}] + \alpha_k \sin(\gamma_k) \\ M_{k,2} = \omega_k \sin(\gamma_k) - \alpha_k [\cos(\gamma_k) - e^{\beta_k}] \\ H_{k,1} = \omega_k [\cos(2\gamma_k) - e^{2\beta_k}] + \alpha_k \sin(2\gamma_k) \\ H_{k,2} = \omega_k \sin(2\gamma_k) - \alpha_k [\cos(2\gamma_k) - e^{2\beta_k}] \end{cases} \\ \begin{cases} P_{k,1} = e^{-\beta_k} + \left[\frac{\alpha_{\bar{k}}}{\omega_{\bar{k}}} \sin(\gamma_{\bar{k}}) - \cos(\gamma_{\bar{k}}) \right] \\ P_{k,2} = e^{\beta_k} - \left[\frac{\alpha_{\bar{k}}}{\omega_{\bar{k}}} \sin(\gamma_{\bar{k}}) + \cos(\gamma_{\bar{k}}) \right] \\ P_{k,3} = \frac{2(p_k - p_{\bar{k}}) f_{\text{sw}} [\cosh(\beta_{\bar{k}}) - \cos(\gamma_{\bar{k}})]}{(a_k - D_k p_k) \omega_{0k}^2} - \\ \quad \frac{(a_{\bar{k}} - D_{\bar{k}} p_{\bar{k}}) \omega_{0\bar{k}}^2}{(a_k - D_k p_k) \omega_{0k}^2} \cdot \frac{\sin(\gamma_{\bar{k}})}{\omega_{\bar{k}}} \end{cases} \\ T_k &= \frac{P_{k,1} \cos(\gamma_k) + e^{\beta_k} P_{k,2} + P_{k,3} M_{k,2}}{P_{k,1} \sin(\gamma_k) - P_{k,3} M_{k,1}} \end{aligned} \quad (3.13)$$

A detailed derivation of (3.11) is provided in Appendix B.2.

Due to the simplicity of the 2-to-1 ReSC converter, its output impedance model can be further simplified. Assume all switches have the same on-state resistance R_{on} . Then with ideal input and output, its output impedance can be given as

$$\hat{R}_{\text{out}} = \frac{1}{4f_{\text{sw}} C_{\text{fly}}} \cdot \frac{\sinh\left(\frac{\alpha}{2f_{\text{sw}}}\right) + \frac{\alpha}{\omega} \sin\left(\frac{\omega}{2f_{\text{sw}}}\right)}{\cosh\left(\frac{\alpha}{2f_{\text{sw}}}\right) - \cos\left(\frac{\omega}{2f_{\text{sw}}}\right)} \quad (3.14)$$

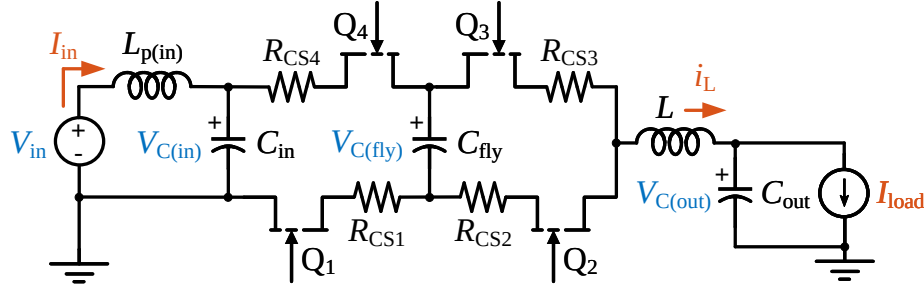


Figure 3.5: Schematic drawing of the 2-to-1 ReSC converter prototype.

where $\alpha = R_{\text{on}}/L$, $\omega_0 = 1/\sqrt{LC_{\text{fly}}}$ and $\omega = \sqrt{\omega_0^2 - \alpha^2}$, which is the same as the model derived in [58].

In addition, the output impedance model of the 2-to-1 ReSC converter with ideal input but finite output capacitance can be given as

$$R_{\text{out}} = \left(\frac{1}{k_{\text{out}} + 1} \right)^2 \left[\hat{R}_{\text{out}} + k_{\text{out}} (2 + k_{\text{out}}) R_{\text{on}} \right] \quad (3.15)$$

where $k_{\text{out}} = C_{\text{fly}}/C_{\text{out}}$ and $\hat{R}_{\text{out}}$ is the output impedance when assuming ideal input and output which has been given in (3.14).

3.3 Model Verification

To verify the accuracy of the proposed output impedance model, we compare the modeling results with circuit simulations and experimental measurements from a 2-to-1 ReSC converter prototype.

3.3.1 Experimental Setup

Figures 3.5 and 3.6 present the schematic drawing and photograph of the 2-to-1 ReSC converter prototype for model verification, with the main components listed in Table 3.1. The key circuit parameters of the prototype include the flying capacitance $C_{\text{fly}} = 3.76 \mu\text{F}$, effective output inductance $L = 388.9 \text{ nH}$ (including parasitic inductance), GaN HEMT on-state resistance $R_{\text{on}} = 16 \text{ m}\Omega$, and current sense resistance $R_{\text{CS}} = 50 \text{ m}\Omega$.

As can be seen in 3.9, the parameters α_k and ω_k are required to calculate the optimum duty ratio and switching frequency, meaning that the equivalent parameters R_k and C_k in Fig. 3.4 need to be accurately obtained. However, the R_{on} of GaN HEMTs is prone to large variation under different operating conditions (e.g. junction temperature, drain-to-source current, gate-to-source voltage, etc.) and can be hard to capture due to the dynamic R_{on} phenomenon [59]. Therefore, to ensure that we can accurately obtain the equivalent

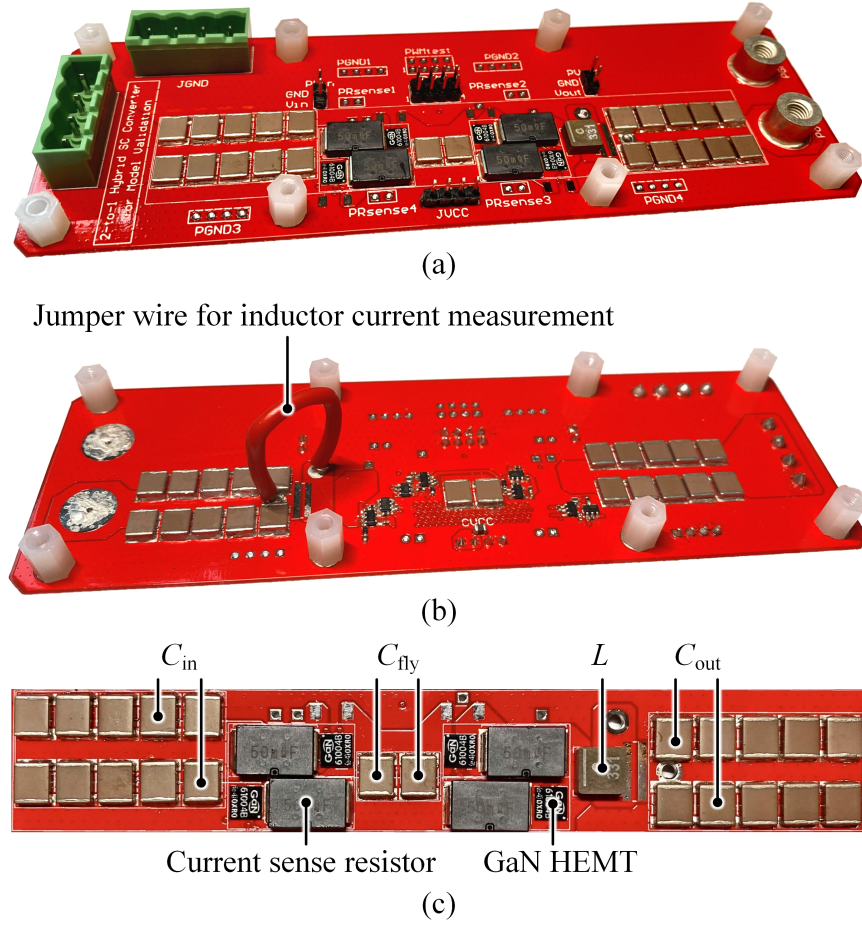


Figure 3.6: Photograph of the 2-to-1 ReSC converter prototype. (a) Overall view. (b) Top view with key components annotated.

resistance R_k , we add a high-precision current sense resistor KOA Speer SLN5TTED50L0F with high thermal stability (75 PPM/°C) in series with each GaN switch to dominate R_k and stabilize it against the variation in R_{on} . In addition, to minimize the variation in capacitances, we choose the Class 1 capacitor KEMET C2220C474J5GACTU which features high capacitance stability over wide range of operating temperature and voltage bias, and extremely low ESR and ESL.

In the experiment, the output impedance is calculated as

$$R_{out} = \frac{V_{C(in)}I_{in} - V_{C(out)}I_{load}}{I_{load}^2}, \quad (3.16)$$

in which the input voltage $V_{C(in)}$ and input current I_{in} are measured with digital multimeters Keysight 34405A and 34401A, respectively, and the output voltage $V_{C(out)}$ and load current

Table 3.1: Component List of the 2-to-1 ReSC converter prototype

Component	Part number	Parameters
GaN HEMT Q_1 - Q_4	GaN Systems GS61004B	100 V, 16 m Ω (@ 25 °C)
Current sense resistor R_{CS1} - R_{CS4}	KOA Speer SLN5TTED50L0F	50 m Ω , 7 W, 75 PPM/°C
Flying capacitor C_{fly}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μ F $\times 8$
Input and output capacitors C_{in} and C_{out}	KEMET C2220C474J5GACTU	C0G, 50 V, 0.47 μ F $\times 8$, $\times 40$ *
Resonant inductor L	Coilcraft XAL6030-331MEC	330 nH, 2.3 m Ω , 30 A
Gate driver	Analog Devices LTC4440-5	80 V, high-side
LDO voltage regulator	Texas Instruments LP2985AIM5-6.1/NOPB	2.5-16 V input, 6.1 V output
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky diode

* Measurements are performed with various terminal capacitances.

I_{load} are measured by the electronic load Rigol DL3031.

3.3.2 Experimental Results

Figs. 3.7 and 3.8 present the comparison between the output impedances predicted by the proposed model (Model), simulated with PLECS (Sim.), and measured from the prototype (Expt.) with various C_{in} and C_{out} . As can be seen in Figs. 3.7 and 3.8, the modeling results match well with the simulated and experimental results within a wide range of switching frequency, including the oscillating R_{out} curves at low switching frequency. This demonstrates that the proposed model is able to accurately capture the effects of finite terminal capacitances. As the switching frequency increases, the switching loss in the prototype becomes higher and higher. Since the proposed model can capture only conduction loss but no switching loss in the converter, the modeling results will deviate from the experimental results in the high frequency region.

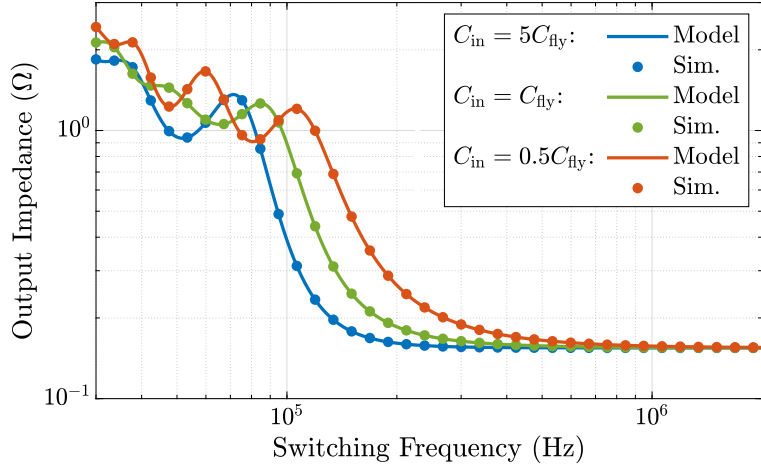
3.4 Effect Analysis of Finite Terminal Capacitances

With the general output impedance model derived and verified in Sections 3.2 and 3.3, we can now use it to explore the effects of finite terminal capacitances on the output impedance of ReSC converters. In this section, the 2-to-1 ReSC converter mentioned in Section 3.3 is used as an example to investigate the effects of C_{in} and C_{out} .

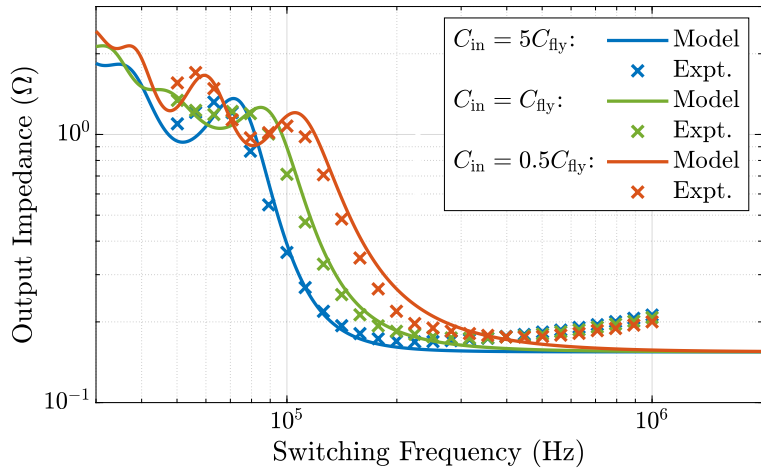
Figs. 3.9 and 3.10 show the effects of C_{in} and C_{out} on the output impedance of the 2-to-1 ReSC converter, where Figs. 3.9(a) and 3.10(a) present the output impedance curves with various C_{in} and C_{out} , and Figs. 3.9(b) and 3.10(b) show how much R_{out} is changed with respect to the output impedance with ideal input and output $R_{\text{out}(\text{ideal})}$.

1) *Effect of C_{in} .* As can be seen in Fig. 3.9(a), with smaller C_{in} , the knee of the output impedance curve will shift to the right, meaning that the critical switching frequency becomes higher. This indicates that higher switching frequency is required to reach the FSL impedance due to the insufficiency of C_{in} . Since higher switching frequency typically leads to higher switching loss and lower overall efficiency, this effect is undesired and should be avoided in converter design by using sufficient C_{in} to ensure nearly ideal input behavior.

Additionally, we can see that C_{in} has stronger influence on the critical switching frequency than C_{out} . Table 3.2 presents a quantitative comparison of the output impedance at the intrinsic critical frequency with different terminal capacitances. Here, we define the intrinsic critical frequency of the 2-to-1 ReSC converter as $f_{\text{crit}(\text{int})} = \frac{1}{2\pi\sqrt{LC_{\text{fly}}}} = 132 \text{ kHz}$. It is called *intrinsic* because it is not related to the terminal capacitances and determined only by the primary passive components (i.e. L and C_{fly}). As can be seen in Table 3.2, R_{out} will increase by roughly a factor of 3 when C_{in} is reduced from $5C_{\text{fly}}$ to C_{fly} , while R_{out} will increase by only a factor of 1.5 when C_{out} is reduced from $5C_{\text{fly}}$ to C_{fly} .

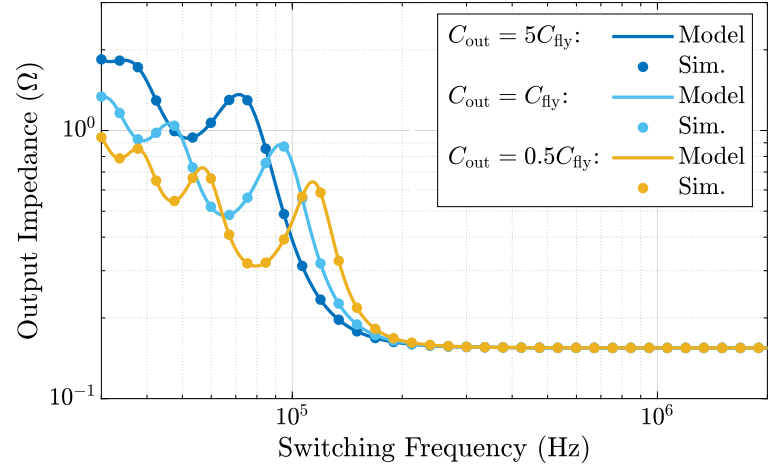


(a)

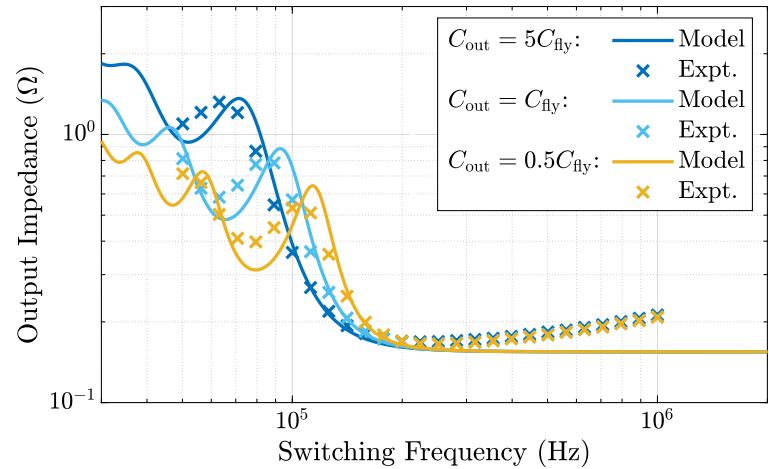


(b)

Figure 3.7: Output impedance of the converter with various C_{in} . ($C_{out} = 5C_{fly}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated with PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.).

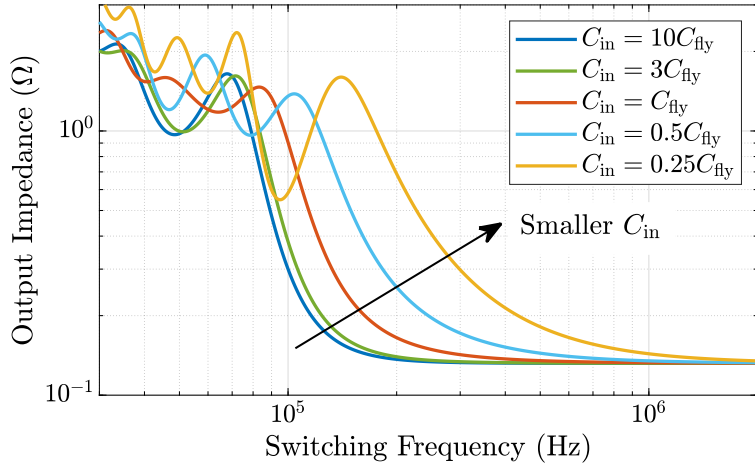


(a)

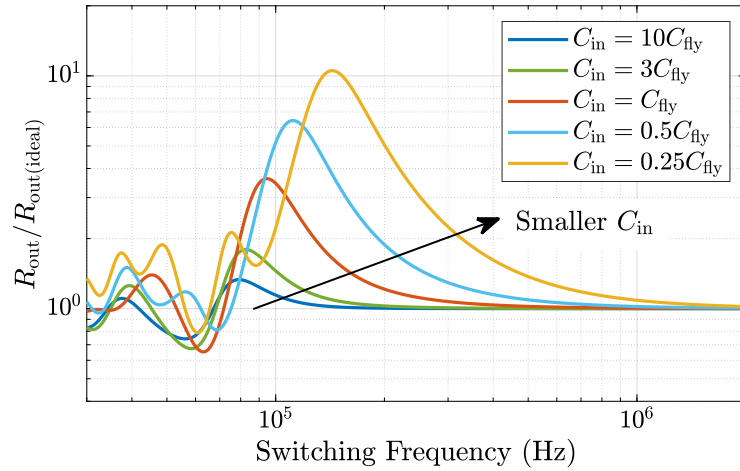


(b)

Figure 3.8: Output impedance of the converter with various C_{out} . ($C_{in} = 5C_{fly}$) (a) Comparison between the output impedances predicted by the proposed model (Model) and simulated with PLECS (Sim.). (b) Comparison between the output impedances predicted by the proposed model (Model) and measured from the prototype (Expt.).

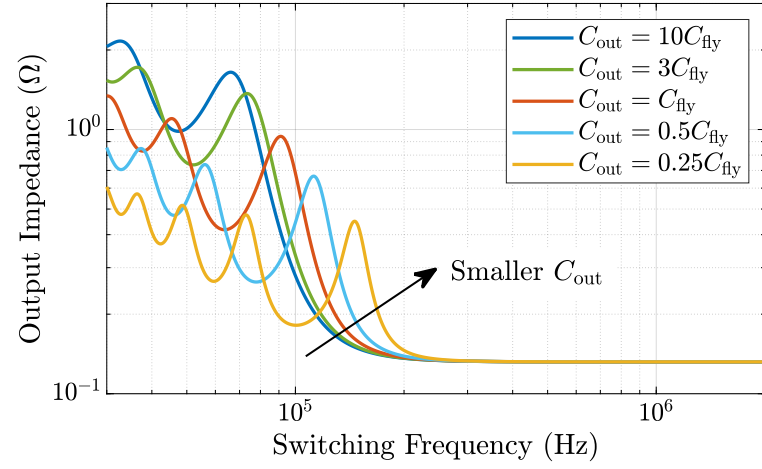


(a)

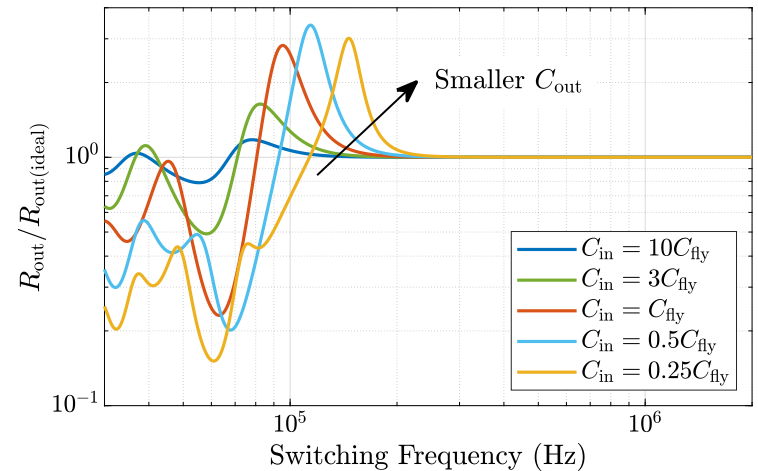


(b)

Figure 3.9: Effect of C_{in} on output impedance. ($C_{out} = 10C_{fly}$) (a) R_{out} with various C_{in} . (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{out(ideal)}$.



(a)



(b)

Figure 3.10: Effect of C_{out} on input impedance. ($C_{in} = 10C_{fly}$) (a) R_{out} with various C_{out} . (b) Ratio of R_{out} to the output impedance with ideal input and output $R_{out(ideal)}$.

Table 3.2: Comparison of the output impedance at the intrinsic critical frequency ($f_{\text{crit(int)}} = 132$ kHz) with different terminal capacitances

No.	$C_{\text{in}}/C_{\text{fly}}$	$C_{\text{out}}/C_{\text{fly}}$	Calculated R_{out} (m Ω)	Measured R_{out} (m Ω)
1)	5	5	201.3	209.5
2)	1	5	326.3	300.3
3)	0.5	5	732.9	621.5
4)	5	1	235.9	238.7
5)	5	0.5	358.9	316.0

2) *Effect of C_{out} .* As we can see in Fig. 3.10(a), in contrast to C_{in} , C_{out} shows a greater influence on the output impedance in the low-frequency region, where smaller C_{out} helps reduce output impedance. This should be a favorable feature since decreasing C_{out} will contribute to both higher efficiency and higher power density. However, since the ReSC converters typically operate above resonance, this phenomenon is hard to utilize in practice for performance improvement.

It can also be seen that smaller C_{out} will lead to higher critical switching frequency, meaning that higher switching frequency will be required to reach the FSL impedance if C_{out} becomes smaller, although C_{out} 's effect on the critical switching frequency is quantitatively weaker than that of C_{in} .

To reduce the sizes of terminal capacitors without sacrificing the efficiency of ReSC converters, we can adjust the duty ratio and switching frequency to compensate for the negative effects of finite terminal capacitances, as will be presented in Chapter 4.

3.5 Application to Arbitrary ReSC Topologies

In this section, the proposed modeling and analysis methodology is applied to other two commonly-used ReSC topologies: series-parallel and Fibonacci topologies, with their schematic drawings shown in Fig. 3.11. These examples are provided here to demonstrate the applicability of this model to more complex ReSC topologies. The set of converters considered in this section is limited to two-phase ReSC converters with the augmenting inductor placed at the output that is able to achieve full soft-charging operation. For simplicity, it is assumed in the following examples that all flying capacitors have the same value $C_{\text{fly}} = 10$ μF , all switches have the same on-state resistance $R_{\text{on}} = 10$ m Ω , and the value of the output inductor is $L = 0.1$ μH .

The key step of applying the proposed model to an arbitrary SC topology is to obtain the equivalent capacitance C_k and equivalent resistance R_k in each phase as illustrated in Fig. 3.4. In simple cases, C_k and R_k can be directly acquired by inspection, while they have to be carefully calculated in other more general cases. The method of calculating C_k and R_k

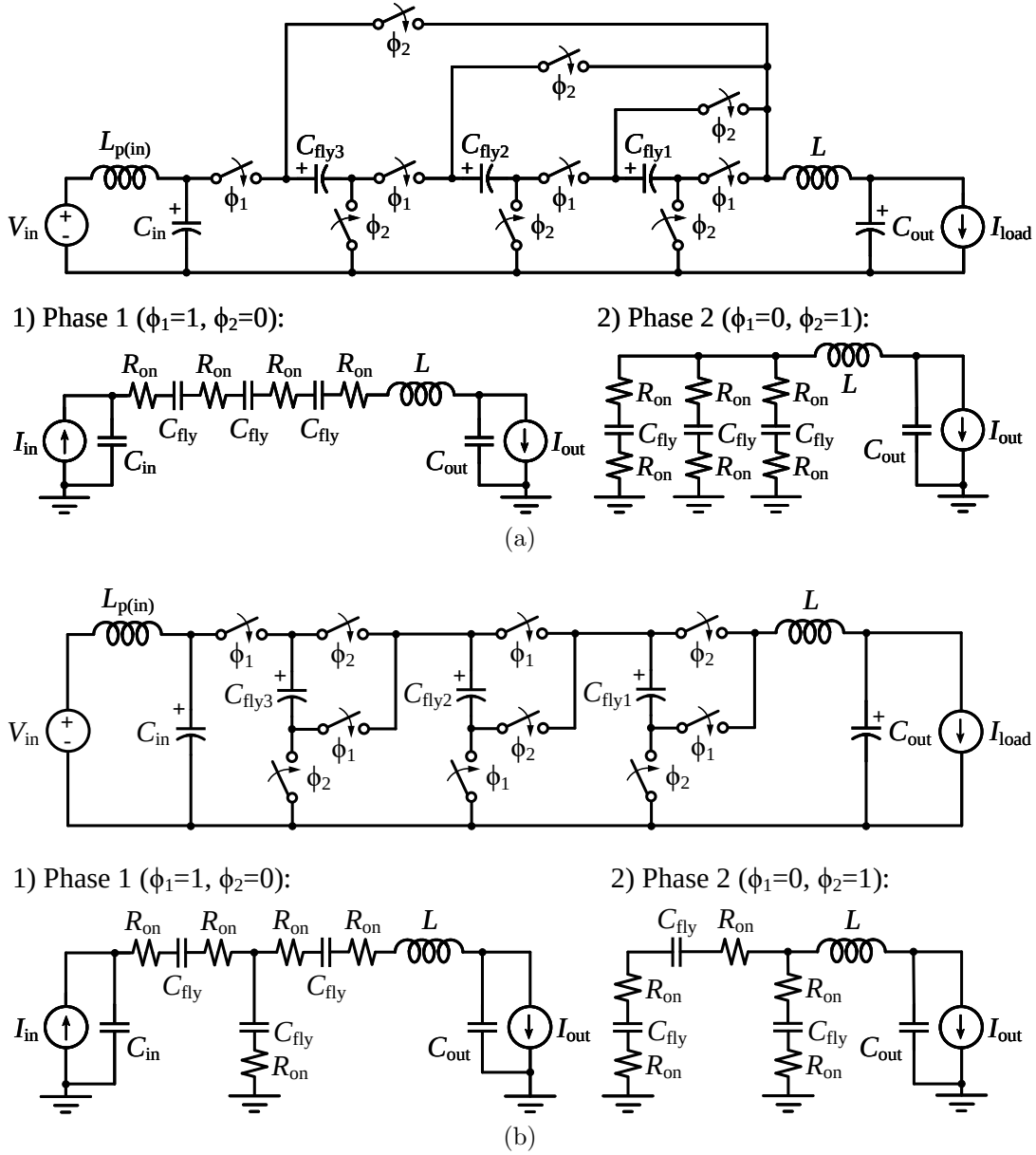


Figure 3.11: Commonly-used ReSC topologies and their equivalent circuits. (a) 4-to-1 series-parallel topology. (b) 5-to-1 Fibonacci topology.

can be found in Section 2.5.1.

Fig. 3.12 presents the output impedance of the two commonly-used ReSC topologies shown in Fig. 3.11 with various terminal capacitances. The comparison between modeling and simulation results in Fig. 3.12 demonstrates the accuracy of the proposed output impedance model in different ReSC topologies with various terminal capacitances.

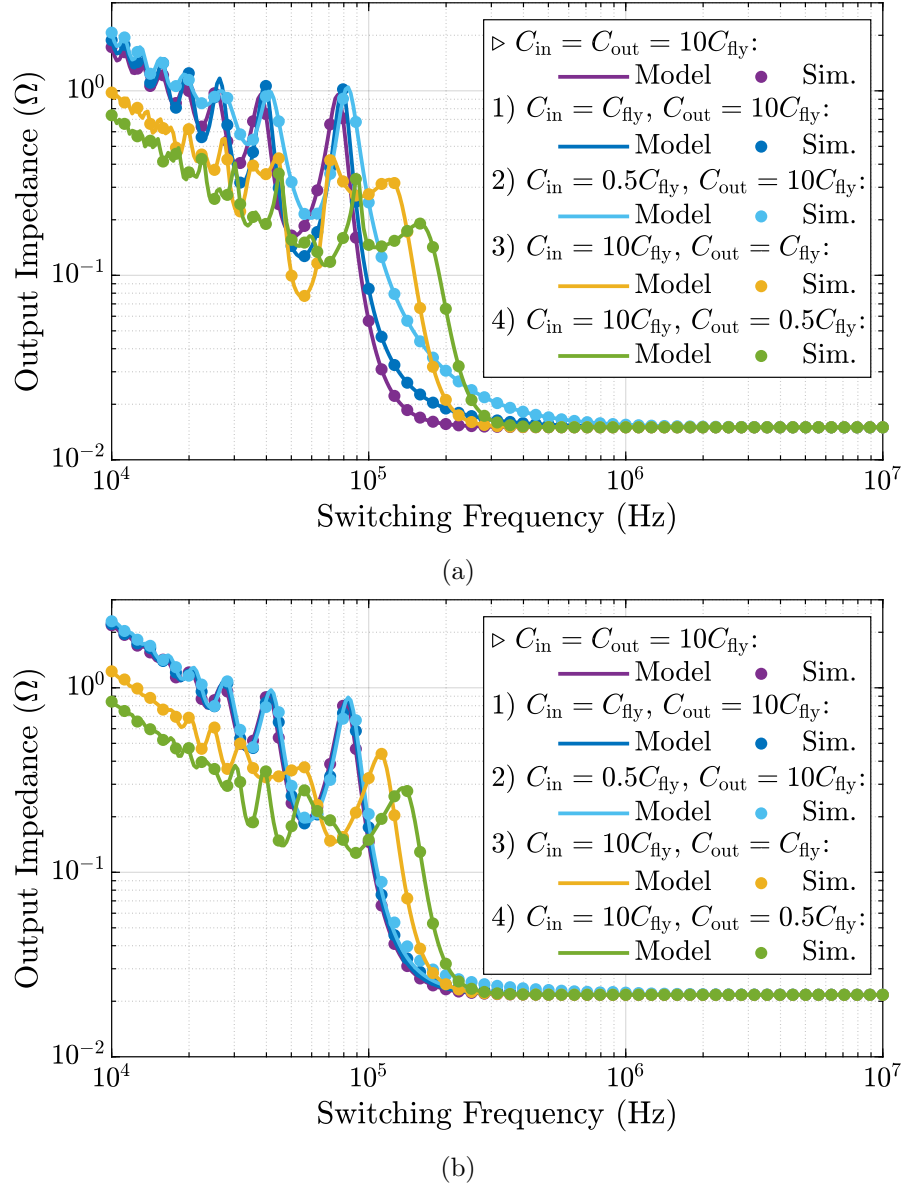


Figure 3.12: Output impedance of commonly-used ReSC topologies with various terminal capacitances and comparison between modeling (Model) and simulation (Sim.) results. (a) 4-to-1 series-parallel topology. (b) 5-to-1 Fibonacci topology.

3.6 Chapter Summary

This chapter proposes a general modeling and analysis methodology to capture the effect of finite terminal capacitances on the output impedance of ReSC converters. A general output impedance model is derived and verified by circuit simulations and experimental

measurements from a 2-to-1 ReSC converter prototype. It is revealed that the insufficiency in terminal capacitances will result in higher critical switching frequency, and C_{in} is quantitatively more influential on the critical switching frequency than C_{out} .

This work provides an analytical tool for future investigations such as design optimizations of ReSC converters with voltage ripple and physical volume constraints.

Chapter 4

Multi-Resonant Compensation Control for Terminal Capacitance Reduction in Resonant SC Converters

4.1 Background and Motivation

Stemming from the conventional pure switched-capacitor (SC) converters [7, 24], resonant switched-capacitor (ReSC) converters utilize high-energy-density capacitors to perform voltage conversion and can achieve both soft-charging and soft-switching operation by the augmenting inductor(s), enabling higher power density and higher efficiency compared to conventional pure SC and magnetics-based converters [42–44].

As illustrated in Fig. 4.1, practical ReSC converters require sufficiently large input and output capacitors (typically $C_{\text{in}}, C_{\text{out}} \geq 10C_{\text{fly}}$) to stabilize the terminal voltages and ensure ideal input and output behaviors. In practice, such bulky terminal capacitors can be even physically larger than the primary passive components in ReSC converters, which significantly limits the potential of the ReSC topology for higher power density and becomes the bottleneck for converter miniaturization in practice.

Although it is desirable to reduce the size of terminal capacitors in ReSC converters, insufficient terminal capacitances will incur dc bias and asymmetry in the inductor current (i_L) if the conventional two-phase control with a fixed duty ratio is used, which not only leads to higher output impedance but also prohibits zero current switching (ZCS), resulting in both higher conduction loss and higher switching loss. Since pre-existing models [53–55] and analyses [43, 56, 57] of ReSC converters all assume ideal input and/or output behaviors and thus cannot be used to characterize the effects of finite terminal capacitances, Chapter 3 proposed a general method for modeling and analyzing ReSC converters with finite terminal capacitances.

To adaptively compensate for the negative effects of insufficient terminal capacitances on the performance of ReSC converters, this chapter proposes a multi-resonant compensation

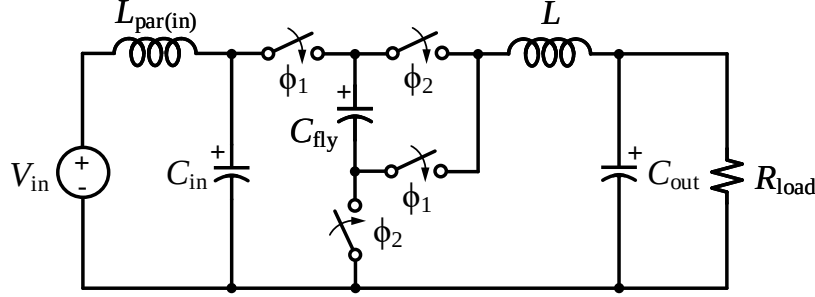


Figure 4.1: Schematic of a 2-to-1 ReSC converter with practical input and output. ($L_{\text{par(in)}}$: parasitic source inductance)

control (MRCC) technique that can maintain low output impedance and full ZCS capability even when the terminal capacitors are extremely small. In the proposed MRCC technique, the duty ratio and switching frequency are adjusted to ensure multi-resonant operation. With the effects of finite terminal capacitances analyzed in Section 4.2, Section 4.3 explains the basic ideas and operating principles of the proposed MRCC technique. In Section 4.4, the proposed control technique is verified experimentally in a 2-to-1 ReSC converter prototype, demonstrating a more than 5 times terminal capacitance reduction without harming the overall efficiency compared to the conventional control technique.

4.2 Effect of Finite Terminal Capacitances

According to Section 2.2, in a general circuit state (or phase) k , a ReSC converter with finite terminal capacitances can be modeled as the second-order circuit illustrated in Fig. 4.2. Note that this general expression is applicable to any arbitrary ReSC topologies with a single inductor at output that can achieve full soft-charging operation as long as suitable (topology-dependent) R_k and C_k values are used. For example, for the 2-to-1 ReSC converter shown in Fig. 4.1, $R_k = 2R_{\text{ds(on)}}$ and $C_k = C_{\text{fly}}$. As illustrated in Fig. 4.2, with nonideal input, two cases should be considered according to whether the input terminal is connected to the source or ground.

Based on the second-order circuit model provided in Fig. 4.2, the inductor current in phase k can be expressed as

$$i_k(t) = A_k e^{-\alpha_k t} \cos(\omega_k t + \varphi_k) + I_{fk} \quad (4.1)$$

where I_{0k} and I_{fk} are the initial value and forced component of i_k in phase k , and τ_k represents the time constant of the equivalent circuit. τ_k and I_{fk} can be expressed as

$$\begin{aligned} \alpha_k &= \frac{R_k}{2L} & \omega_{0k} &= \frac{1}{\sqrt{LC_{k(\text{eff})}}} \\ \omega_k &= \sqrt{\omega_{0k}^2 - \alpha_k^2} & I_{fk} &= p_k I_{\text{out}} \end{aligned} \quad (4.2)$$

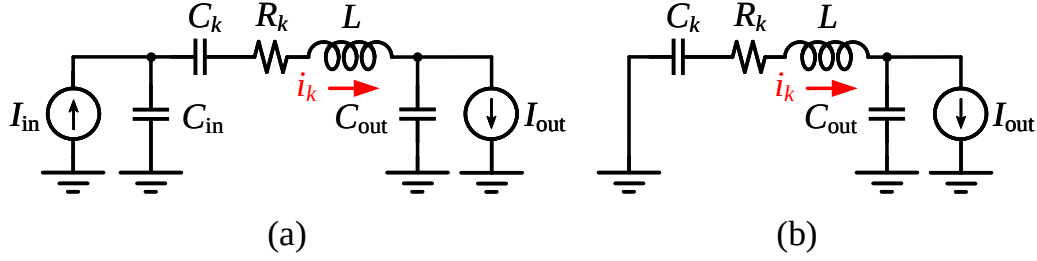


Figure 4.2: Second-order circuit model of a two-phase ReSC converter with finite terminal capacitances proposed in Section 2.2. (a) Case 1 (Phase 1): the input terminal is connected to the source. (b) Case 2 (Phase 2): the input terminal is grounded.

in which α_k , ω_{0k} and ω_k are the decay rate, natural angular frequency and angular frequency of the inductor current in phase k , respectively. $C_{k(\text{eff})}$ is the effective capacitance and p_k is a dimensionless ratio. In the two cases illustrated in Fig. 4.2, for an m -to- n ReSC converter, $C_{k(\text{eff})}$ and p_k can be given as

$$\begin{aligned} \text{Case 1 :} & \begin{cases} C_{k(\text{eff})} = 1 / \left(\frac{1}{C_k} + \frac{1}{C_{\text{in}}} + \frac{1}{C_{\text{out}}} \right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{in}} C_{\text{out}}} \left(C_{\text{in}} + \frac{n}{m} C_{\text{out}} \right) \end{cases} \\ \text{(Phase 1)} & \\ \text{Case 2 :} & \begin{cases} C_{k(\text{eff})} = 1 / \left(\frac{1}{C_k} + \frac{1}{C_{\text{out}}} \right) \\ p_k = \frac{C_{k(\text{eff})}}{C_{\text{out}}} \end{cases} \\ \text{(Phase 2)} & \end{aligned} \quad (4.3)$$

With the above circuit model derived, we can now analyze the effects of finite terminal capacitances. First, from (4.1)-(4.3), we can see that insufficient C_{in} and C_{out} will incur dc bias in the inductor current, since I_{fk} will be nonzero when C_{in} and C_{out} are comparable to C_k . Second, (4.3) indicates that the effective capacitance $C_{k(\text{eff})}$ will be different in the two phases if C_{in} is not sufficiently large. This means that the angular frequency ω_k of the inductor current in the two phases will no longer be the same, resulting in asymmetric inductor current waveform. In summary, both insufficient C_{in} and C_{out} can incur dc bias in the inductor current while low C_{in} will further induce an asymmetric inductor current waveform, which will lead to higher RMS inductor current and thus higher output impedance.

Fig. 4.3 shows the simulated output impedance curves and inductor current waveforms in a 2-to-1 ReSC converter with various terminal capacitances ($C_{\text{fly}} = 10 \mu\text{F}$, $L = 0.1 \mu\text{H}$, $R_{\text{ds(on)}} = 10 \text{ m}\Omega$). Here, we define the intrinsic critical frequency of the 2-to-1 ReSC converter as $f_{\text{crit(int)}} = \frac{1}{2\pi\sqrt{LC_{\text{fly}}}} = 159 \text{ kHz}$. It can be seen in Fig. 4.3(a) that if we reduce C_{in} or C_{out} to C_{fly} and still operate the converter at $f_{\text{crit(int)}}$, the output impedance will significantly rise due to the insufficiency in terminal capacitances. Meanwhile, the influence

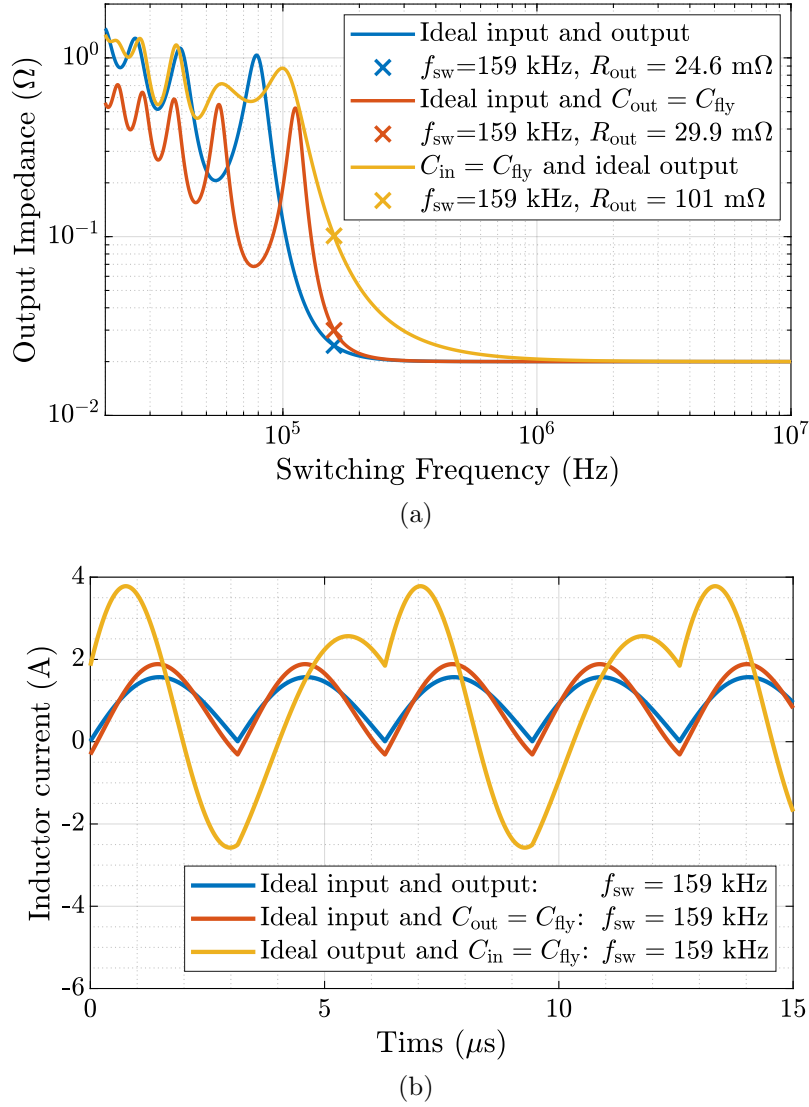


Figure 4.3: Effect of terminal capacitances on output impedance and inductor current waveform in the 2-to-1 ReSC converter at the intrinsic critical frequency $f_{crit(int)} = \frac{1}{2\pi\sqrt{LC_{fly}}} = 159$ kHz and $D = 0.5$. ($C_{fly} = 10$ μ F, $L = 0.1$ μ H, $R_{ds(on)} = 10$ m Ω) (a) Comparison of output impedance. (b) Comparison of inductor current waveform.

of C_{in} is quantitatively much stronger than C_{out} , since C_{in} will incur not only dc bias but also asymmetry in the inductor current which can be clearly seen in Fig. 4.3(b).

To facilitate analysis, we define the critical frequency f_{crit} as the switching frequency at which the minimal value of the inductor current i_L is 0 A. The parameter f_{crit} is typically around the knee of the output impedance curve near the fast switching limit (FSL)

impedance and thus usually chosen as the operating point of the converter. Note that f_{crit} differs from $f_{\text{crit}(\text{int})}$ since the former can reflect the influence of C_{in} and C_{out} while the latter is independent of the terminal capacitances and determined by only the primary passive components.

Under conventional control, the output impedance of the 2-to-1 ReSC converter can be reduced by increasing the switching frequency. As shown in Fig. 4.4(a), we can maintain low output impedance when $C_{\text{in}} = C_{\text{fly}}$ by increasing the switching frequency from $f_{\text{crit}(\text{int})} = 159$ kHz to $f_{\text{crit}} = 390$ kHz. However, as can be seen in the time-domain plot of Fig. 4.4(b), the inductor current waveform at $D = 0.5$ and $f_{\text{crit}} = 390$ kHz is no longer half-wave resonant but nearly triangular, prohibiting ZCS at the transition from phase 2 to phase 1. This will result in greatly higher switching loss, especially since the converter now operates at even higher switching frequency, indicating that the terminal capacitances cannot be reduced without harming the overall efficiency when the conventional 0.5-duty-ratio control is used.

4.3 Multi-Resonant Compensation Control

To reduce the terminal capacitances without sacrificing efficiency, this section proposes a multi-resonant compensation control (MRCC) technique. As explained in Section 4.2, insufficient terminal capacitances will incur dc bias and asymmetry in the inductor current when the conventional control is used. To maintain low output impedance and full ZCS capability when the terminal capacitors are small, the duty ratio should be adjusted to ensure a multi-resonant inductor current waveform as shown in Fig. 4.4(c). Since the effective capacitance in phase 1 is lower than that in phase 2 (i.e. $C_{1(\text{eff})} < C_{2(\text{eff})}$), the angular frequency of the inductor current is higher in phase 1 (i.e. $\omega_1 > \omega_2$). Since ReSC converters are typically designed to be highly underdamped ($\frac{R}{2}\sqrt{\frac{C}{L}} \ll 1$) [43], the decay rate α_k in (4.2) is usually much smaller than ω_{0k} , which implies $\omega_k \approx \omega_{0k}$. This means that if we let the inductor current start to oscillate from zero at the beginning of a phase, it will take longer time in phase 2 than in phase 1 for the inductor current to oscillate back to zero again. Therefore, the duty ratio of phase 1 D_1 should be decreased from 0.5 and the duty ratio of phase 2 D_2 should be increased from 0.5 (i.e. $D_1 + D_2 = 1$ and $D_1 < D_2$). At the optimum duty ratio and switching frequency, we will be able to achieve the multi-resonant inductor current waveform as illustrated in Fig. 4.4(c).

Next, we need to calculate this optimum duty ratio and switching frequency that ensures multi-resonant operation. First, to achieve full ZCS, the inductor current i_k should be zero at the starting and ending points of each phase:

$$i_k(0) = i_k(D_k T) = 0 \quad (k = 1, 2) \quad (4.4)$$

in which D_k is the duty ratio of phase k and T is the switching period. Moreover, we know that $D_1 + D_2 = 1$. Second, the charge balance in the flying capacitor(s) should be satisfied,

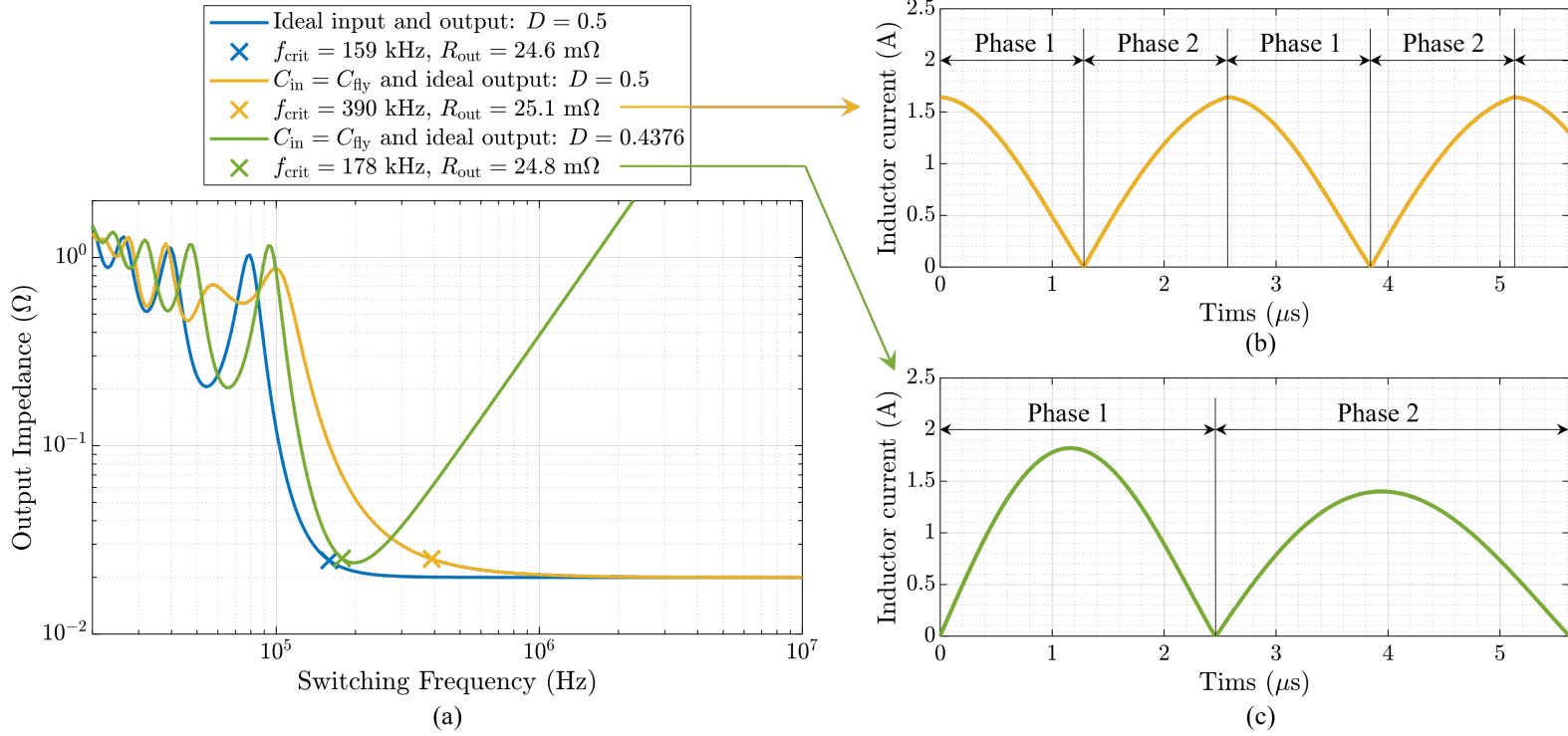


Figure 4.4: Comparison between the conventional two-phase control with a duty ratio of 0.5 and the proposed MRCC with the optimum duty ratio and switching frequency. ($C_{fly} = 10 \mu F$, $L = 0.1 \mu H$, $R_{ds(on)} = 10 m\Omega$) (a) Comparison of output impedance. (b) Inductor current waveform of the conventional control ($D = 0.5$ and $f_{crit} = 390$ kHz). (c) Inductor current waveform of MRCC ($D = 0.4376$ and $f_{crit} = 178$ kHz).

which implies

$$\int_0^{D_k T} i_k(t) dt = a_k I_{\text{out}} T \quad (k = 1, 2) \quad (4.5)$$

in which I_{out} is the output current and a_k is the ratio of the transferred charge in phase k to the total delivered charge in a switching cycle. The definition and calculation of a_k can be found in [24].

Based on (4.2)-(4.5), we find that the optimum duty ratio and switching frequency for MRCC is the solution to the following set of equations:

$$\frac{\cosh(\alpha_k D_k T) - \cos(\omega_k D_k T)}{\sin(\omega_k D_k T)} = \frac{\omega_{0k}^2}{2\omega_k} \left(D_k T - \frac{T}{2p_k} \right) \quad (k = 1, 2). \quad (4.6)$$

Since $D_1 + D_2 = 1$, there are two unknowns in (4.6): the duty ratio D_1 (which is defined as the duty ratio of the converter D) and the switching period T (the reciprocal of the switching frequency f_{sw}). Although (4.6) is a set of transcendental equations that does not have a closed-form analytical solution, it can be conveniently solved with the nonlinear system solver *fsolve* in MATLAB.

4.4 Experimental Verification

In this section, a 2-to-1 ReSC converter prototype is specially designed to verify the proposed MRCC technique.

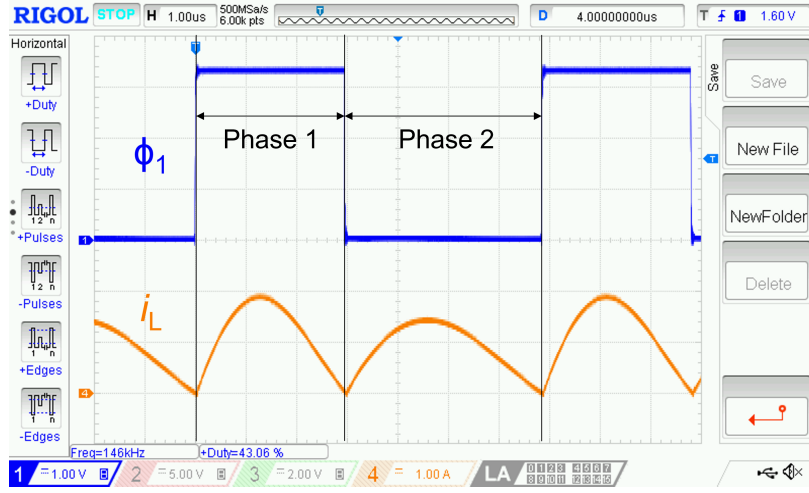
4.4.1 Experimental Setup

Figures 3.5 and 3.6 present the schematic drawing and photograph of the 2-to-1 ReSC converter prototype for model verification, with the main components listed in Table 3.1. The key circuit parameters of the prototype include the flying capacitance $C_{\text{fly}} = 3.76 \mu\text{F}$, effective output inductance $L = 388.9 \text{ nH}$ (including parasitic inductance), GaN HEMT on-state resistance $R_{\text{on}} = 16 \text{ m}\Omega$, and current sense resistance $R_{\text{CS}} = 50 \text{ m}\Omega$.

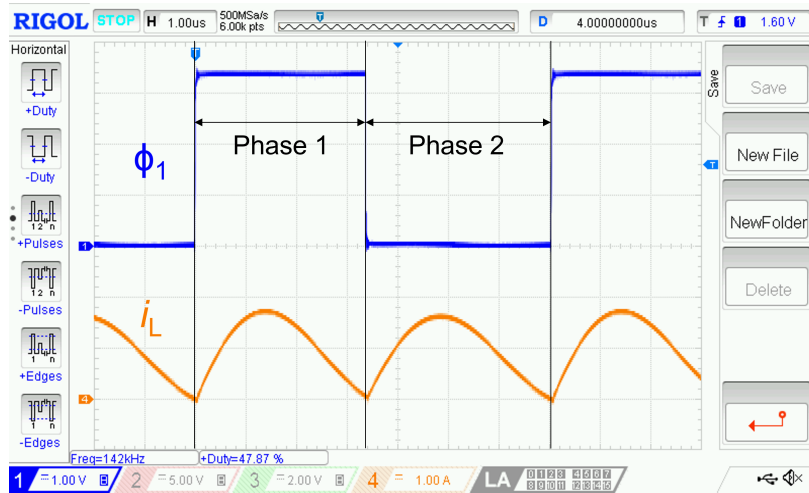
In the experiment, the output impedance is calculated as

$$R_{\text{out}} = \frac{V_{\text{in}} I_{\text{in}} - V_{\text{out}} I_{\text{load}}}{I_{\text{load}}^2}, \quad (4.7)$$

in which the input voltage V_{in} and input current I_{in} are measured with digital multimeters Keysight 34405A and 34401A, respectively, and the output voltage V_{out} and load current I_{load} are measured by the electronic load Rigol DL3031.



(a)



(b)

Figure 4.5: Measured waveforms of MRCC at the optimum duty ratio and switching frequency. (ϕ_1 : control signal of Q_2 and Q_4 , i_L : inductor current) (a) $C_{in} = C_{fly}$, $C_{out} = 5C_{fly}$, $D = 0.4322$, $f_{crit} = 146$ kHz. (b) $C_{in} = 5C_{fly}$, $C_{out} = C_{fly}$, $D = 0.4795$, $f_{crit} = 142$ kHz.

4.4.2 Experimental Results

Fig. 4.5 shows the measured waveforms of MRCC at the optimum D and f_{crit} calculated from (4.6), in which we can see that MRCC achieves excellent multi-resonant inductor current waveforms and full ZCS even when the input and output capacitors are small. Fig. 4.6 presents the measured output impedance curves of the 2-to-1 ReSC converter with various C_{in} and C_{out} under the conventional control and MRCC, with the key performance at the critical frequency summarized in Table 4.1.

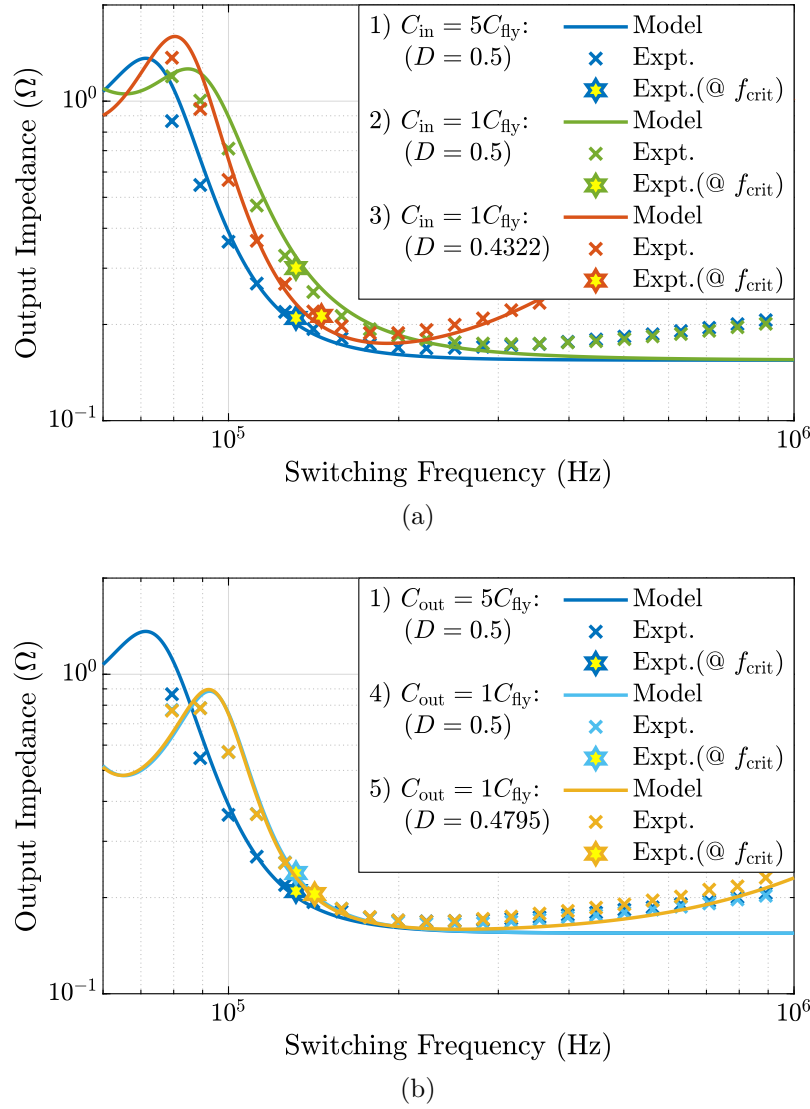


Figure 4.6: Measured output impedance curves with the conventional control and MRCC. (a) Output impedances with various C_{in} . ($C_{out} = 5C_{fly}$) (b) Output impedances with various C_{out} . ($C_{in} = 5C_{fly}$)

In Table 4.1, we can see that under the conventional control, the reduction in C_{in} and C_{out} will result in a dramatic increase in output impedance at the critical frequency, meaning that it is impossible to shrink the size of terminal capacitors without harming the overall efficiency. By contrast, MRCC is able to maintain low output impedance even when the terminal capacitors are small, which verifies its capability of reducing the terminal capacitances without harming the overall efficiency.

Table 4.1: Comparison between the conventional control and MRCC at the critical frequency

No.	$\frac{C_{in}}{C_{fly}}$	$\frac{C_{out}}{C_{fly}}$	Control method	D	f_{crit}^* (kHz)	Calculated R_{out} (m Ω)	Measured R_{out} (m Ω)
1)	5	5	Conventional control	0.5	132	201.3	209.5
2)	1	5	Conventional control	0.5	132	326.3	300.3
3)	1	5	MRCC	0.4322	146	198.1	212.8
4)	5	1	Conventional control	0.5	132	235.9	238.7
5)	5	1	MRCC	0.4795	142	201.0	205.1

* The critical frequency of the conventional control is defined as its intrinsic critical frequency $f_{crit(int)} = \frac{1}{2\pi\sqrt{LC_{fly}}} = 132$ kHz, while the D and f_{crit} of MRCC is calculated with (4.6).

4.5 Chapter Summary

In ReSC converters with the conventional two-phase control, the terminal capacitors need to be sufficiently large to ensure ideal input and output behaviors, which dramatically increases the overall physical volume of the converter and significantly limits the potential of ReSC topologies for achieving higher power density. This chapter proposes a multi-resonant compensation control (MRCC) technique for ReSC converters that can adaptively compensate for the negative effects of insufficient terminal capacitances. At the optimum duty ratio and switching frequency, MRCC can ensure multi-resonant inductor current and full ZCS capability even with extremely small terminal capacitors. The proposed control technique is implemented in a 2-to-1 ReSC converter prototype for experimental verification. It is shown that the proposed MRCC technique is able to reduce the terminal capacitances by at least a factor of 5 without harming the overall efficiency.

Part II

Circuit Topologies, Comparative Analysis, and High-Performance Hardware Implementation For Direct 48 V to Point-of-Load Power Delivery in Data Centers

Chapter 5

Multi-Phase Cascaded Series-Parallel Hybrid Converter

This chapter proposes a multi-phase hybrid SC converter that can achieve direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 6-to-1 *cascaded series-parallel* (CaSP) stage and a three-phase interleaved buck stage with automatic current balancing. Due to multi-phase operation, the CaSP stage is able to achieve a higher conversion ratio compared to two-phase SC converters with the same number of capacitors and switches and enable lower turn-on voltage for the switching devices. The proposed CaSP topology also benefits from the frequency multiplication effect similar to that in flying capacitor multilevel (FCML) converters, which allows for lower frequency operation of higher voltage rated switches and doubled frequency operation of the buck inductors, further contributing to a reduction in switching loss and inductor size. A 48 V-to-PoL hardware prototype was built in vertical assembly structure to achieve compact packaging and tested up to 90 A output current. At 48-to-2.0 V conversion, the prototype achieved 94.1% peak efficiency (93.2% including gate drive loss) and 702 W/in³ power density (by box volume).

5.1 Proposed Topology and Operating Principles

Fig. 5.1 shows the schematic of the proposed CaSP converter, with the voltage rating and operating frequency of the main active and passive components listed in Table 5.1. Fig. 5.2 illustrates the key current waveforms and control signals, with the equivalent circuit model for each phase shown on the right. The proposed topology can be viewed as a 6-to-1 CaSP converter merged with a three-phase interleaved buck converter. The CaSP structure, on the one hand, can be regarded as a 2-to-1 front-end stage followed by a 3-to-1 series-parallel stage. On the other hand, it can also be derived from the classic 4-to-1 series-parallel topology, by moving the source terminals of Q_2 , Q_5 and Q_6 from the left-side of L_3 to the positive-side of C_2 and the left-sides of L_1 and L_2 , respectively, and removing the switch between the

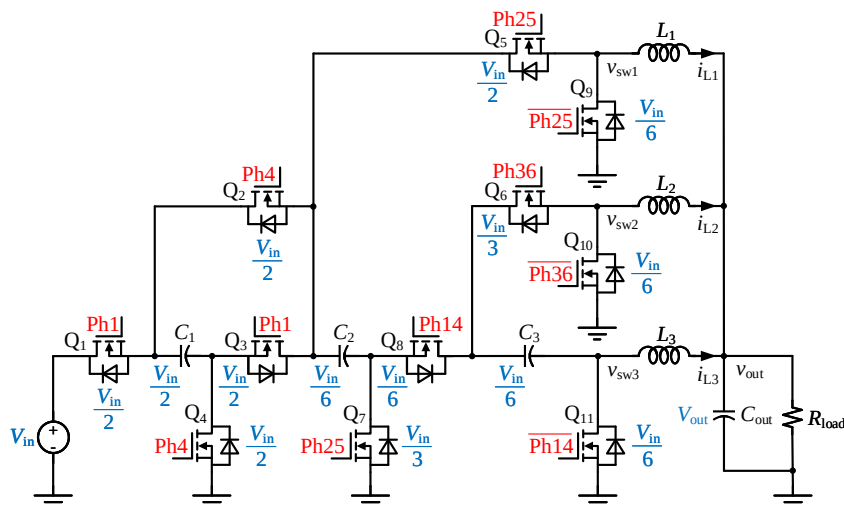


Table 5.1: Voltage rating and operating frequency of the main components

	V_{blocking}	f_{sw}
Q_1 - Q_4	$\frac{V_{\text{in}}}{2}$	f_0
Q_5	$\frac{V_{\text{in}}}{2}$	$2f_0$
Q_6 - Q_7	$\frac{V_{\text{in}}}{3}$	$2f_0$
Q_8	$\frac{V_{\text{in}}}{6}$	$2f_0$
Q_9 - Q_{11}	$\frac{V_{\text{in}}}{6}$	$2f_0$ (ZVS)
C_1	$\frac{V_{\text{in}}}{2}$	f_0
C_2 - C_3	$\frac{V_{\text{in}}}{6}$	$2f_0$
L_1 - L_3	$\frac{V_{\text{in}}}{6} - V_{\text{out}}$	$2f_0$

Figure 5.1: Schematic of the proposed CaSP converter with device ratings labeled in blue and control signals labeled in red.

negative-side of C_3 and the left-side of L_3 .

As illustrated in Fig. 5.2, each switching cycle of the proposed converter is divided into multiple phases. The charge and discharge of C_2 and C_3 each takes two phases. C_1 is charged in phase 1 and discharged in phase 4, whereas C_2 and C_3 are charged in phases 1 and 4. C_2 is discharged in phases 2 and 5, and C_3 is discharged in phases 3 and 6. Due to the high conversion ratio of the CaSP stage, the conversion burden on the buck stage is reduced. Another advantage of multi-phase operation is lower turn-on voltage of switching devices. As can be seen in Fig. 5.2, although Q_7 's peak blocking voltage is $\frac{V_{in}}{3}$, its drain-to-source voltage $V_{ds,Q7}$ naturally drops to a lower level before it turns on, contributing to reduced switching loss.

In the proposed CaSP topology, the CaSP stage and the three-phase buck stage are merged together without additional switches or flying capacitors. This helps not only minimize the number of components but also reduce the conduction loss compared to a two-stage approach, contributing to both higher power density and higher efficiency. The operation of the CaSP and buck stages is merged seamlessly to ensure interleaved inductor currents. Each inductor is energized twice in a switching cycle in two different phases by the source or flying capacitors and de-energized twice in the freewheeling phase 7.

The three-phase buck stage has an automatic current balancing capability that is similar to that of the series capacitor buck converter [60, 61]. There is a negative feedback mechanism that keeps the average currents through L_1 and L_2 the same as that through L_3 , so that the

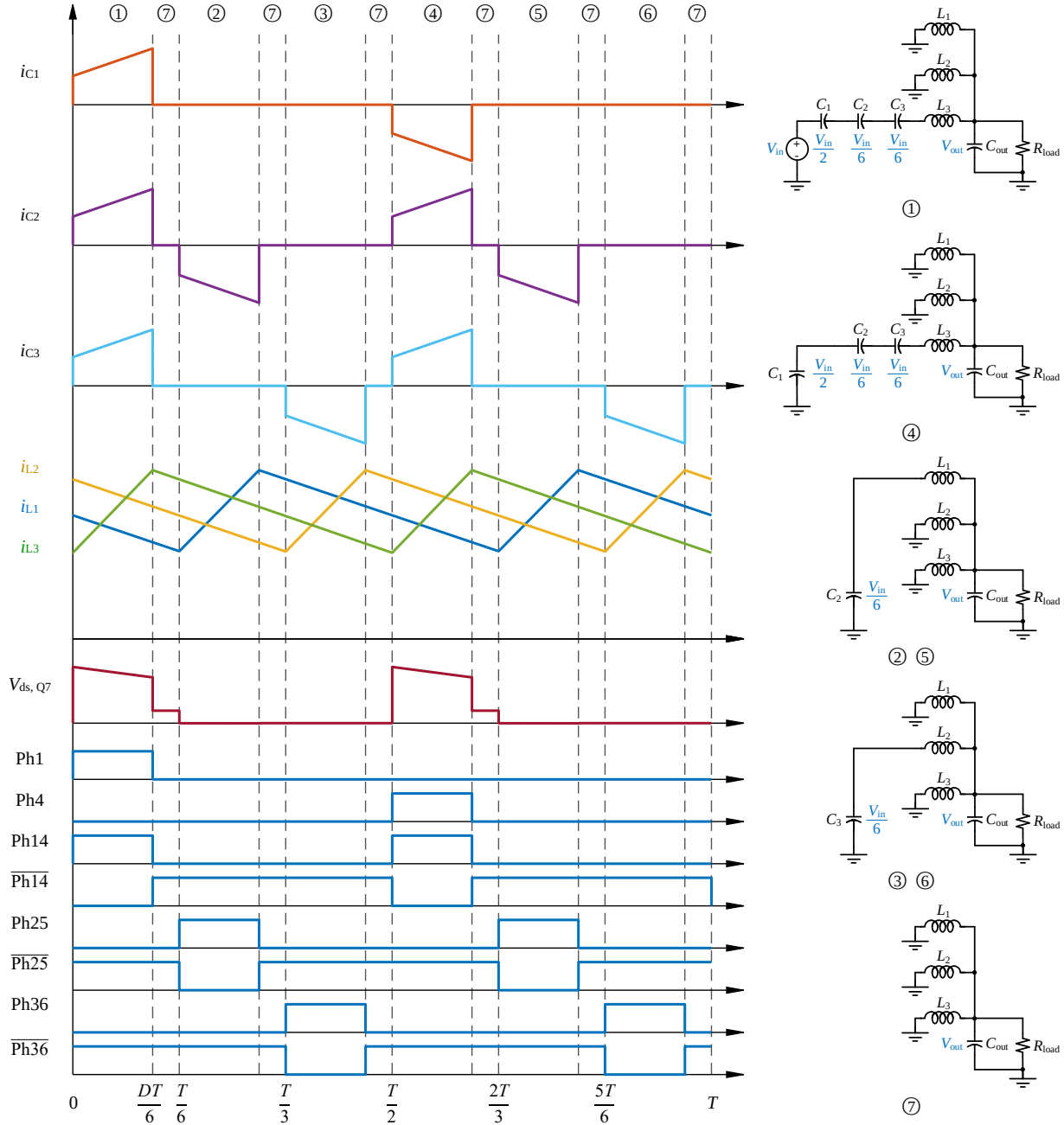


Figure 5.2: Key current waveforms and control signals of the proposed hybrid SC converter. The equivalent circuit model for each phase is shown on the right.

three inductor currents are naturally balanced. For example, if the average current through L_1 is higher than that through L_3 (i.e. $\langle i_{L1} \rangle > \langle i_{L3} \rangle$), then the net charge flowing into C_2 in phases 1, 2, 4 and 5 will be negative, meaning C_2 will be discharged. Therefore, the voltage across L_1 in phases 2 and 5 in which L_1 is energized will decrease while the voltage across L_3 in phases 1 and 4 will increase, so that i_{L1} will decrease and i_{L3} will increase correspondingly until $\langle i_{L1} \rangle = \langle i_{L3} \rangle$. A similar analysis can be applied to i_{L2} and i_{L3} . If $\langle i_{L2} \rangle < \langle i_{L3} \rangle$, then the net charge flowing into C_3 in phases 1, 2, 3 and 6 will be positive, meaning C_3 will be charged. Therefore, the voltage across L_2 in phases 3 and 6 in which L_2 is energized will increase while the voltage across L_3 in phases 1 and 4 will decrease, so that i_{L2} will increase and i_{L3} will decrease until $\langle i_{L2} \rangle = \langle i_{L3} \rangle$. In summary, such a negative feedback mechanism naturally ensures $\langle i_{L1} \rangle = \langle i_{L3} \rangle$ and $\langle i_{L2} \rangle = \langle i_{L3} \rangle$ so that the three-phase interleaved inductor currents can be naturally balanced.

In addition, the abovementioned automatic current balancing capability can also be explained with a more quantitative analysis. Due to the triangular shape of the inductor currents, the average inductor current in the rising and falling stages will be the same as the average current over one switching cycle in the periodic steady state (PSS). Therefore, in PSS, the average currents through the flying capacitors can be given as

$$\begin{cases} \langle i_{C1} \rangle = \frac{D}{6} \langle i_{L3} \rangle - \frac{D}{6} \langle i_{L3} \rangle \\ \langle i_{C2} \rangle = \frac{D}{3} \langle i_{L3} \rangle - \frac{D}{3} \langle i_{L1} \rangle \\ \langle i_{C3} \rangle = \frac{D}{3} \langle i_{L3} \rangle - \frac{D}{3} \langle i_{L2} \rangle \end{cases} \quad (5.1)$$

In PSS, the average currents through the flying capacitors should be zero, i.e.

$$\langle i_{C1} \rangle = \langle i_{C2} \rangle = \langle i_{C3} \rangle = 0. \quad (5.2)$$

Substituting (5.2) into (5.1) yields $\langle i_{L1} \rangle = \langle i_{L3} \rangle$ and $\langle i_{L2} \rangle = \langle i_{L3} \rangle$, which means well-balanced inductor currents can be automatically achieved in PSS.

Moreover, the proposed CaSP converter benefits from the frequency multiplication effect similar to that in FCML converters. If C_1 and Q_1 - Q_4 operate at a frequency f_0 , then the other main components operate at a frequency $2f_0$. As listed in Table 5.1, the switches with higher voltage ratings (Q_1 - Q_4) operate at lower switching frequency than those with lower voltage ratings, which is favorable to switching loss reduction. Since the operating frequency of the inductors is doubled due to multi-phase operation, lower inductance can be chosen while maintaining the same inductor current ripple. Also, due to the reduced switch voltage stress in the CaSP stage, low-voltage MOSFETs with lower $R_{ds(on)}$ and lower switching loss can be used. In addition, Q_9 - Q_{11} operate with zero-voltage switching (ZVS) turn-ON.

The conversion ratio of the proposed converter can be derived based on the volt-second balance of the buck inductors:

$$\left(\frac{V_{in}}{6} - V_{out} \right) \cdot \frac{DT}{6} + (-V_{out}) \cdot \left(\frac{T}{2} - \frac{DT}{6} \right) = 0 \quad \Rightarrow \quad V_{out} = \frac{D}{18} V_{in} \quad (5.3)$$

where D is the duty ratio of phases 1 – 6 with respect to $\frac{T}{6}$, as illustrated in Fig. 5.2. Therefore, the output voltage can be regulated by adjusting the duty cycle.

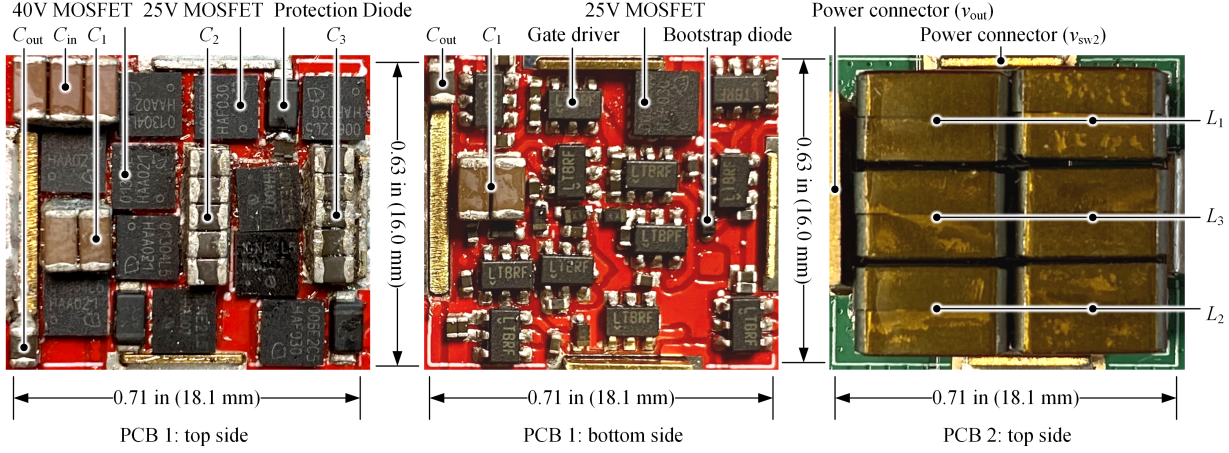


Figure 5.3: Photograph of the hardware prototype. Dimensions: PCB 1: $0.71 \times 0.63 \times 0.24$ inch ($18.1 \times 16.0 \times 6.2$ mm); PCB 2: $0.71 \times 0.63 \times 0.33$ inch ($18.1 \times 16.0 \times 8.3$ mm).

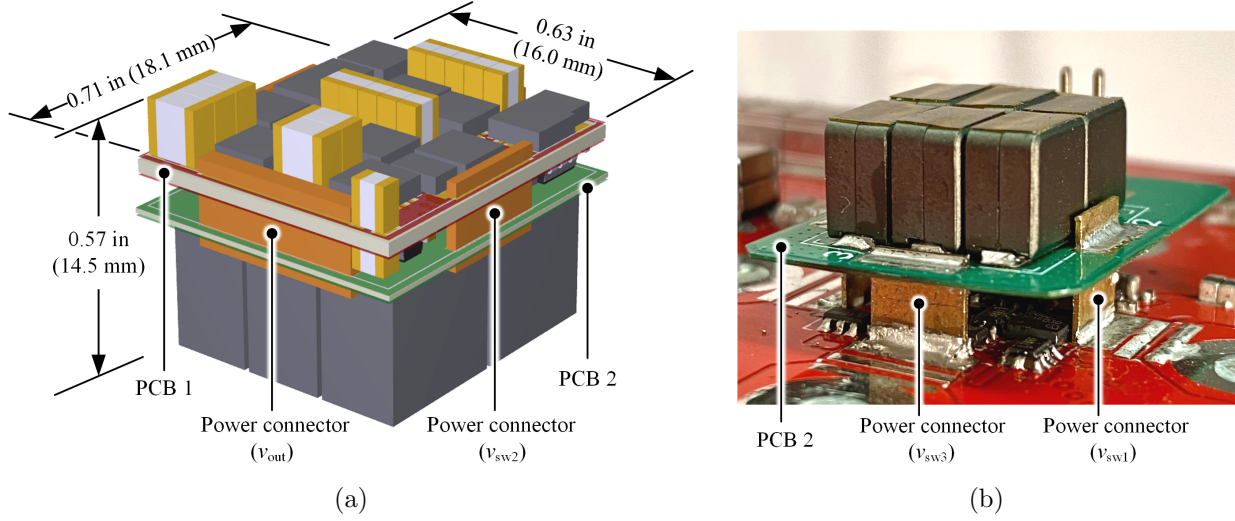


Figure 5.4: Vertical assembly of the prototype. (a) 3D assembly drawing. Dimensions: $0.71 \times 0.63 \times 0.57$ inch ($18.1 \times 16.0 \times 14.5$ mm). (b) Photograph of the power connectors in the prototype.

5.2 Hardware Implementation and Experimental Results

Figures 5.3 and 5.4 show the annotated photograph and 3D assembly drawing of the converter prototype, with the key parameters and component list tabulated in Tables 5.2 and 5.3, respectively.

Table 5.2: Key parameters of the prototype

Parameter	Value
Input voltage	48 V
Output voltage	1.2-2.0 V*
Output current	90 A
Switching frequency f_0	160 kHz
Inductor operating frequency $2f_0$	320 kHz
Prototype box volume	0.256 in ³
Power component volume ⁺	0.136 in ³
Current density	351 A/in ³

* The converter prototype is able to operate at 1.0 V and lower output voltages but was only tested to 1.2 V due to the limited capability of the electronic load.

⁺ The power components included in the volume calculation are switching devices, capacitors, and inductors.

Table 5.3: Component list of the prototype

Component	Part number	Parameters
MOSFET Q_1 - Q_5	Infineon IQE013N04LM6	40 V, 1.35 m Ω
MOSFET Q_6 - Q_8	Infineon BSZ010NE2LS5	25 V, 1.0 m Ω
MOSFET Q_9 - Q_{10}	Infineon IQE006NE2LM5CG	25 V, 0.65 m Ω
MOSFET Q_{11}	Infineon IQE006NE2LM5CG	25 V, 0.65 m Ω $\times 2$ (in parallel)
Flying capacitor C_1	TDK C3216X5R1V226M160AC	X5R, 35 V, 22 μ F* $\times 6$ (in parallel)
Flying capacitor C_2 - C_3	TDK C2012X6S1C226M125AC	X6S, 16 V, 22 μ F* $\times 10$ (in parallel)
Inductors L_1 - L_3	TDK VLB0805080T-R18L	180 nH, 0.2 m Ω $\times 2$ (in series)
Input capacitor C_{in}	TDK C3216X7S2A335K160AB	X7S, 100 V, 3.3 μ F* $\times 6$ (in parallel)
Output capacitor C_{out}	TDK C2012X5R1A476M125AC	X5R, 10 V, 47 μ F* $\times 3$ (in parallel)
Gate driver	Analog Devices LTC4440-5	80 V, high-side
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky diode

* The capacitance listed in this table is the nominal value before dc derating.

As illustrated in Fig. 5.4, the prototype consists of two vertically stacked PCBs connected via nodes v_{sw1} , v_{sw2} , v_{sw3} and v_{out} (labeled in Fig. 5.1) with thick copper sheets (0.5 mm thick for v_{sw1} , v_{sw2} and v_{sw3} , and 1.0 mm thick for v_{out}). PCB 1 contains the switches, flying capacitors and gate drive circuitry while the inductors are placed on PCB 2.

This vertical structure can not only ease the layout design since it offers an additional dimension for component placement but also facilitate full utilization of the box volume of the converter. Commercial inductors with the desired parameters and the small footprint required in this design are typically high-profile with a height of more than 7 mm and are

significantly taller than the other components (e.g. MOSFETs and capacitors) that are lower than 2 mm. If the inductors are placed on the same board with the other components, it would be difficult to achieve the smallest possible box volume since the large space above the low-profile components could not be utilized. Instead, by stacking the high-profile inductors and the other low-profile components in the way illustrated in Fig. 5.4, all main components are tightly packaged within a $0.71 \times 0.63 \times 0.57$ inch box with most space inside the box effectively utilized.

In this prototype, efficiency is slightly traded for higher power density. Therefore, the selection of inductor is first based on the suitable footprint size that can be packaged with the other components in a rectangular box. Additionally, to achieve high efficiency, inductors with high inductance and low DCR should be selected. Finally, the TDK VLBU805080T-R18L with 5×8 mm footprint, 180 nH inductance and $0.2 \text{ m}\Omega$ DCR was selected. For each inductor (L_1 - L_3 in Fig. 5.1), two TDK VLBU805080T-R18Ls are connected in series. As for the selection of flying capacitors, the capacitance design in this regulated converter is largely relaxed compared to the resonant converters [62] in which the L and C values have to be precisely tuned. Relatively small flying capacitors can be employed as long as they can ensure sufficiently small capacitor voltage ripples that will not cause overvoltage breakdown of switching devices and imbalanced inductor currents. Choosing larger flying capacitors can help reduce total capacitor ESR and hysteresis loss [63] and ensure well-balanced inductor currents.

As listed in Table 5.1, due to the reduced switch voltage stress in the CaSP stage, low-voltage MOSFETs with lower $R_{ds(on)}$ and lower switching loss can be used (40 V for Q_1 - Q_5 and 25 V for Q_6 - Q_{11}). An additional switch is added in parallel to Q_{11} to reduce the conduction loss since it carries two-times higher peak current than Q_9 and Q_{10} . The floating switches are driven by high-side gate drivers with internal level-shifters that are powered by a cascaded bootstrap circuit [41]. The gate drive voltage is 7.0 V in this prototype. The output voltage is regulated with a hysteretic control on the duty cycle D in which D will be increased by a step ΔD if the measured output voltage is lower than the reference value and will be reduced by ΔD if the measured output voltage is higher than the reference value. More advanced control techniques can be employed for desired transient response and control bandwidth, but are not the focus of this work (CaSP). PCB 1 has 6 layers and is fabricated with 3 oz copper on the outer layers and 2 oz in the inner layers. PCB 2 has 2 layers and is fabricated with 3 oz copper. Thicker outer copper can be used to help further reduce the PCB trace loss.

Figs. 5.5(a) and (b) show the measured waveforms of the inductor currents and switch node voltages, respectively. As can be seen in Fig. 5.5(a), the three-phase interleaved inductor currents are naturally well-balanced which verifies the automatic current balancing capability explained in Section 5.1. Fig. 5.6 presents the measured ZVS turn-ON waveforms of Q_{11} . These waveforms are also representative of Q_9 and Q_{10} .

Figs. 5.7(a) and (b) show the measured power stage efficiency and system efficiency (including gate drive loss) of the prototype at various output voltages, with the peak and full-load efficiency and power density (by box volume) summarized in Table 5.4. The efficiency

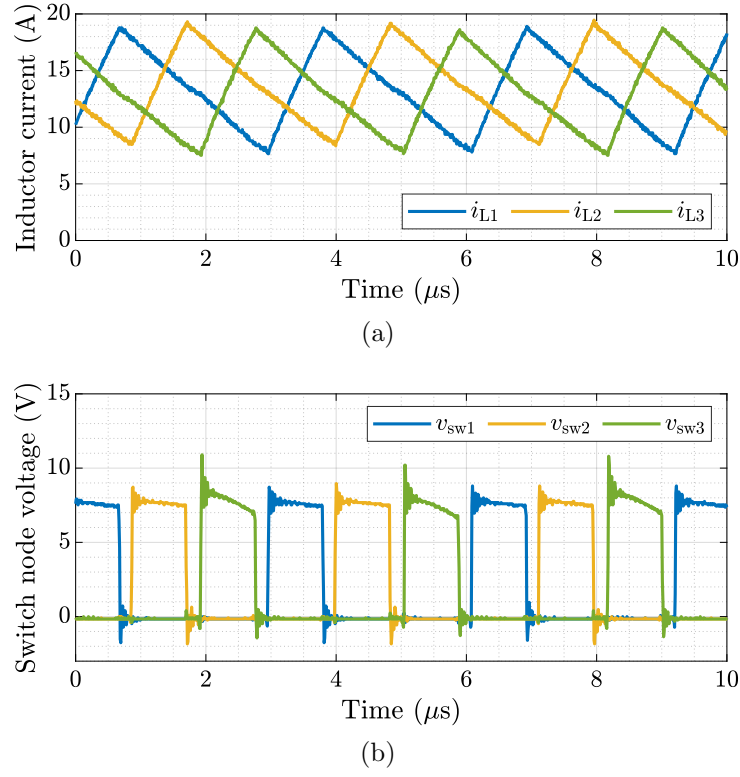


Figure 5.5: Experimental waveforms of the proposed CaSP converter ($V_{out} = 2.0$ V, $I_{out} = 40$ A). (a) Balanced interleaved inductor currents. (b) Switch-node voltages. (v_{sw1} , v_{sw2} , and v_{sw3} are labeled in Fig. 5.1.)

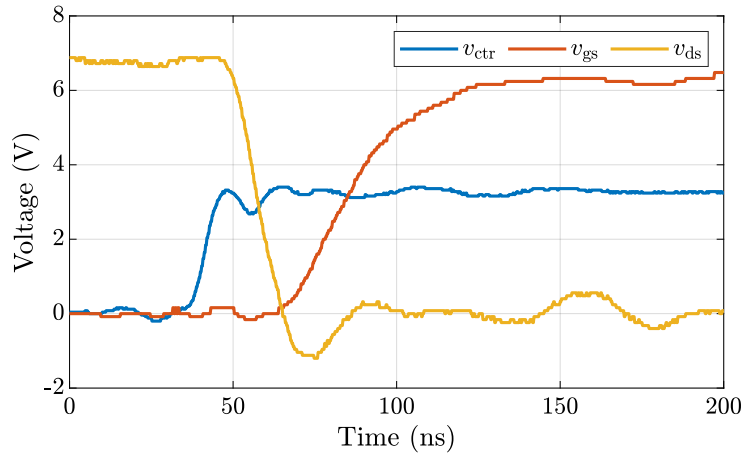


Figure 5.6: ZVS turn-ON of Q_{11} . v_{ctr} : PWM control signal, v_{gs} : gate-to-source voltage, v_{ds} : drain-to-source voltage.

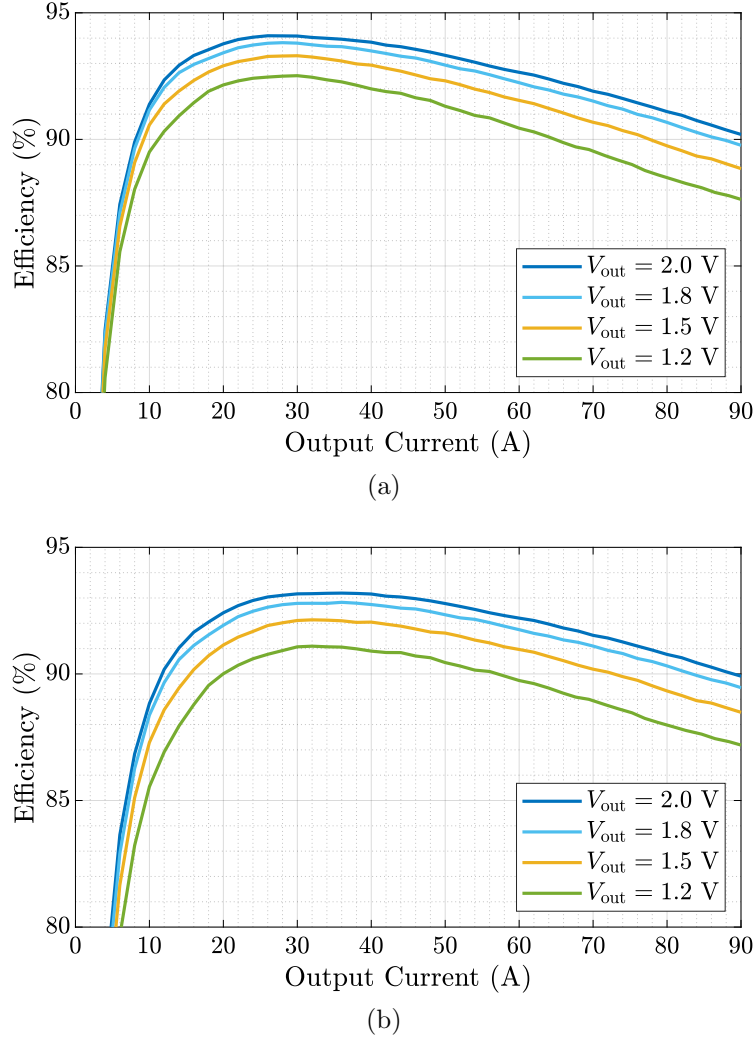


Figure 5.7: Measured efficiency of the prototype at various output voltages. (a) Power stage efficiency. (b) System efficiency (including gate drive loss).

of the prototype was measured with the following equipment: the input voltage and current were measured with digital multimeters Keysight 34401A and 34405A, respectively, and the output voltage and current were measured with electronic loads Rigol DL3021 and DL3031. Note that although Table 5.4 only lists the measured efficiency at 1.2-2.0 V output voltages, the converter prototype is able to operate at 1.0 V and lower output voltages but was only tested to 1.2 V due to the limited capability of the electronic load Rigol DL3031 whose minimum operating voltage is 1.3 V at 60 A. The prototype was tested up to 90 A output current and achieved a current density of 351 A/in³. At 48-to-2.0 V conversion and $f_0 = 160$ kHz switching frequency (320 kHz seen by the inductors), the prototype achieved 94.1% peak efficiency (93.2% including gate drive loss) and 90.2% full load (89.9% including gate

Table 5.4: Measured efficiency and power density of the prototype at various output voltages

Output voltage	Power stage efficiency	System efficiency (including gate drive loss)	Power density*
2.0 V	Peak: 94.1% Full load: 90.2%	Peak: 93.2% Full load: 89.9%	702 W/in ³ 401 W/in ²
1.8 V	Peak: 93.8% Full load: 89.8%	Peak: 92.8% Full load: 89.5%	632 W/in ³ 361 W/in ²
1.5 V	Peak: 93.3% Full load: 88.8%	Peak: 92.1% Full load: 88.5%	527 W/in ³ 301 W/in ²
1.2 V	Peak: 92.5% Full load: 87.6%	Peak: 91.1% Full load: 87.2%	421 W/in ³ 241 W/in ²

* The volumetric power density listed here is calculated based on the prototype box volume in Table 5.2. The areal power density listed here is calculated based on the prototype box area 0.71×0.63 inch (18.1×16.0 mm) shown in Fig. 5.3.

drive loss), and 702 W/in³ power density (by box volume).

Fig. 5.8 shows the thermal image of the prototype at equilibrium with fan cooling only at $V_{\text{out}} = 1.2$ V, $I_{\text{out}} = 90$ A, and 27.8 °C ambient temperature. As shown in Fig. 5.8, the maximum temperature on the board is 91.8 °C. Note that better thermal performance can be achieved by adding heat sinks on the MOSFETs without increasing the box volume since there is still room above the MOSFETs as illustrated in Fig. 5.4(a).

Table 5.5 compares the performance of this work (CaSP), with that of several hybrid SC works published before 2021, when the CaSP converter was first proposed. It can be seen that the proposed CaSP converter achieves a very high power density, while maintaining excellent peak and full-load efficiency. Note that some power density numbers in Table 5.5 are calculated by box volume, while others are by power component volume which can be much smaller than the real box volume of the converter. For reference, the power density by power component volume of our design is also provided in Table 5.5. As explained above, the vertical assembly structure is adopted in this prototype to help package all main components in a rectangular box, which necessitates the use of power connectors to join the two PCBs. Since the power connectors at switch nodes v_{sw1} , v_{sw2} and v_{sw3} conduct inductor currents i_{L1} , i_{L2} and i_{L3} that ripple at 320 kHz, the addition of the power connectors incurs not only additional dc conduction loss but also ac conduction loss that cannot be easily reduced by increasing the thickness of the copper sheets due to the skin effect. Therefore, this prototype is designed to trade efficiency for relatively better power density. This can be seen in Table 5.5 as this prototype achieved 1.8 times higher power density at the cost of around 1% lower efficiency compared to the MLB converter proposed in [65]. For further

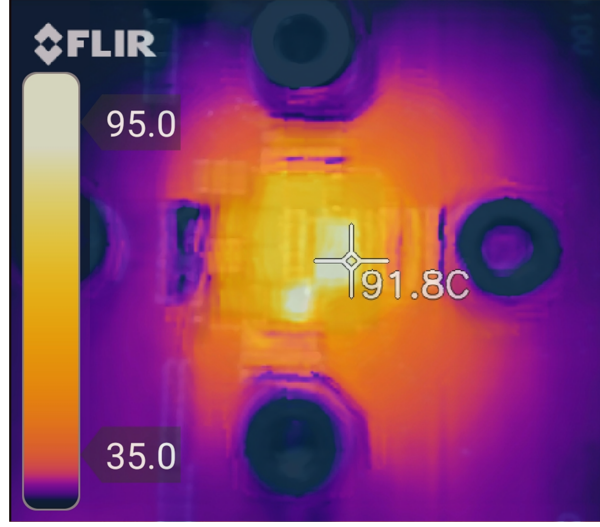


Figure 5.8: Thermal image at equilibrium with fan cooling only ($V_{\text{out}} = 1.2 \text{ V}$, $I_{\text{out}} = 90 \text{ A}$, ambient temperature: $27.8 \text{ }^{\circ}\text{C}$).

optimization, low-profile customized inductors and board cutouts for recessing inductors can be used so that the inductors in this converter can be placed on the same board with the rest of the components without increasing the overall height of the converter, which could remove the need for power connectors and help achieve higher efficiency.

5.3 Chapter Summary

This chapter presents a multi-phase hybrid SC converter for direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 6-to-1 cascaded series-parallel (CaSP) stage and a three-phase interleaved buck stage with automatic current balancing. It benefits from the multi-phase operation and frequency multiplication effect which help decrease the number of components, reduce the switching loss, and shrink the inductor size. A 48 V to 2.0-1.2 V hardware prototype was built and assembled vertically to facilitate compact packaging and achieve high power density. The prototype was tested up to 90 A output current, achieving 94.1% peak efficiency (93.2% including gate drive loss) and 702 W/in^3 power density (by box volume) at 2.0 V output voltage.

Table 5.5: Comparison between this work (CaSP) and previous hybrid SC works

Reference	Conversion Ratio	Output Current	Power Density	Power Stage Efficiency
This work (CaSP [64])	48-to-2.0 V	90 A (30 A/phase)	702 W/in ³ (by box volume) 1328 W/in ³ (by power component volume [†])	Peak efficiency: 94.1% Full load efficiency: 90.2%
	48-to-1.5 V	90 A (30 A/phase)	527 W/in ³ (by box volume) 996 W/in ³ (by power component volume [†])	Peak efficiency: 93.3% Full load efficiency: 88.8%
MLB [65]	48-to-2.0 V	65 A (32.5 A/phase)	395 W/in ³ (by box volume)	Peak efficiency: 95.1% Full load efficiency: 91.3%
	48-to-1.5 V	65 A (32.5 A/phase)	296 W/in ³ (by box volume)	Peak efficiency: 94.4% Full load efficiency: 89.9%
MIH [66]	48-to-2.0 V	40 A (13.3 A/phase)	426 W/in ³ * (by power component volume [†])	Peak efficiency: 94.6%* Full load efficiency: 87.2%* (including calculated gate charge loss)
DP-MIH [67]	48-to-2.0 V	100 A (25 A/phase)	304 W/in ³ (by estimated box volume)	Peak efficiency: 93.6% Full load efficiency: 87.1% (including gate drive loss)
7-level FCML [68]	48-to-2.0 V	10 A (10 A/phase)	N/A	Peak efficiency: 85.0% Full load efficiency: 81.5%
LEGO [69]	48-to-1.5 V	300 A (25 A/phase)	171 W/in ³ * (by box volume)	Peak efficiency: 96.0%* Full load efficiency: 87.7%*
Crossed-coupled QSD buck [70]	48-to-1.5 V	40 A (20 A/phase)	150 W/in ³ (by power component volume [†])	Peak efficiency: 95.1%* Full load efficiency: 92.7%*

* According to direct correspondence with the author.

[†] The power components included in the volume calculation are switching devices, capacitors, and inductors.

Chapter 6

Dickson-Squared Hybrid Switched-Capacitor Converter

This chapter proposes a Dickson² hybrid SC converter that can achieve direct 48 V-to-PoL conversion with high efficiency and high power density. The proposed topology comprises a 9-to-1 SC stage and a nine-phase interleaved buck stage, in which the SC stage can be viewed as two 3-to-1 Dickson converters directly combined together without an intermediate dc bus. The proposed topology can achieve complete soft-charging operation with a simple control and ensures naturally balanced interleaved inductor currents. Compared with the existing 48 V-to-PoL hybrid SC converters, the proposed topology achieves the highest conversion ratio at the SC stage, thus reducing the conversion burden on the buck stage. Moreover, the proposed topology requires no large bus capacitors by using a switching bus architecture. A 48 V-to-PoL hardware prototype is built to verify the performance of the proposed converter. At 1.0 V output voltage, the prototype achieves 93.8% peak efficiency, 88.4% full-load efficiency, and 360 W/in³ power density (by box volume).

6.1 Proposed Topology and Operating Principles

Fig. 6.1 shows the schematic drawing of the proposed Dickson² converter, with the key waveforms and control signals illustrated in Fig. 6.2. As illustrated in Fig. 6.1(a), the proposed topology consists of two stages. The first stage is a 3-to-1 Dickson SC topology with three separated output terminals. The second stage is composed of three modules with the same circuit structure and cyclic control signals as shown in Fig. 6.1(b). Inside each module is a three-phase series-capacitor buck converter, which can also be viewed as a 3-to-1 Dickson converter with the top switch moving to the bottom and the three output branches replaced by three inductors. Since this SC topology can be viewed as two Dickson converters merged together with redundant components removed, it is given the name *Dickson*².

The proposed Dickson² converter has the following features.

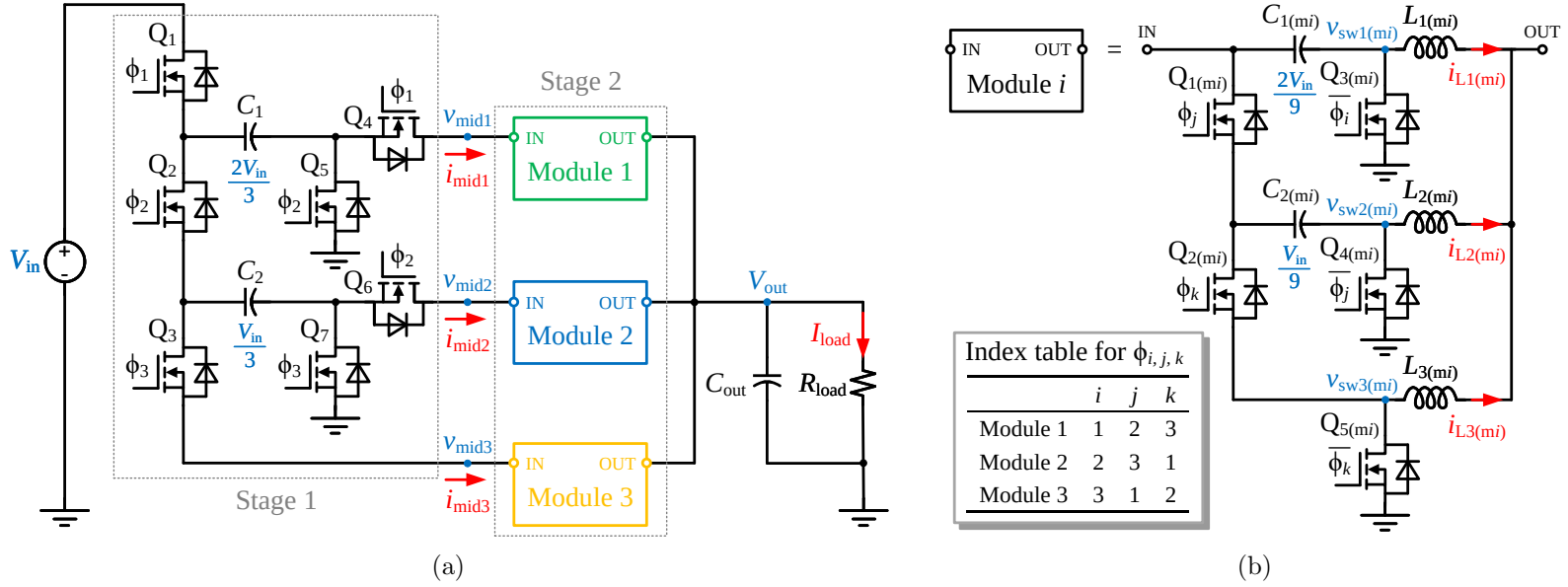
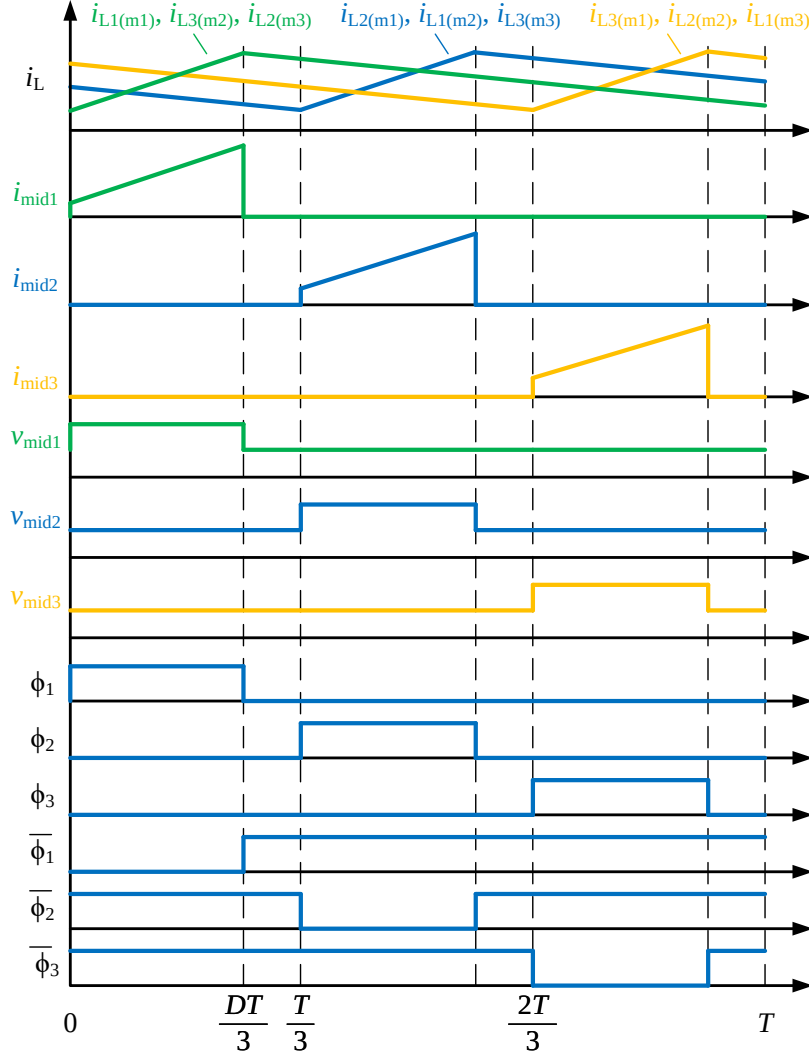


Figure 6.1: Schematic drawing of the proposed Dickson² converter. (a) Overall architecture. (b) Structure of Module i in Stage 2. The components labeled with the subscript (mi) are in Module i . The values of the label indexes (i, j and k) for circuit components and control signals (ϕ_i, ϕ_j and ϕ_k) in each module are listed in the index table.


 Figure 6.2: Key waveforms and control signals of the proposed Dickson² converter.

6.1.0.1 Complete Soft-Charging Operation With Simple Control

As explained in [71], to achieve complete soft-charging operation in resonant Dickson SC converters, a more complex control technique such as the split-phase control [72] has to be employed. However, despite the simple three-phase control of the proposed topology shown in Fig. 6.2, the capacitor charge-sharing loss can be completely eliminated with the three modules in the second stage inserted into the 3-to-1 Dickson SC topology in the first stage at the three output terminals. This can help improve efficiency without compromising on control complexity.

Table 6.1: Comparison of the conversion ratio division over the SC and buck stages among different 48 V-to-PoL hybrid SC works (assuming 48 V to 1.0 V conversion)

Topology	SC stage ratio	buck stage ratio
Crossed-coupled QSD buck [70]	4:1	12:1
CaSP [64]	6:1	8:1
LEGO [73]	6:1	8:1
VIB [74]	8:1	6:1
MLB [65]	8:1	6:1
This work (Dickson ²)	9:1	5.33:1

6.1.0.2 Naturally Balanced Interleaved Inductor Currents

With the cyclic control shown in Figs. 6.1(b) and 6.2, the operation of the SC and buck stages is merged seamlessly so that the three-phase inductor currents in each model are interleaved with each other, which can reduce the net output current ripple. Moreover, the interleaved inductor currents are naturally balanced due to an inherent negative feedback mechanism between the inductor currents and flying capacitor voltages as explained in [64]. In addition, the bottom switches in the buck stage $Q_{3-5(m1)-(m3)}$ can operate with zero-voltage switching (ZVS).

6.1.0.3 Reduced Conversion Burden on the Buck Stage

As listed in Table 6.1, compared to the existing 48 V-to-PoL hybrid SC works, the proposed topology achieves the highest conversion ratio at the SC stage, resulting in less conversion burden on the following buck stage. Since the efficiency and power density of the buck stage will increase with a lower conversion ratio, the overall performance can be improved with the SC stage carrying more conversion burden without much extra loss or many additional components.

6.1.0.4 Switching Bus Architecture Without Large Bus Capacitors

In most two-stage conversion architectures, an intermediate dc bus is needed to connect the two stages, which requires large bus capacitors to stabilize the dc bus voltage that hinders converter miniaturization. By contrast, in the proposed Dickson² topology, the two Dickson stages are merged directly and seamlessly without an intermediate dc bus. As illustrated in Fig. 6.2, the middle points between the two stages see switching voltages $v_{mid1-mid3}$. This *switching bus architecture* not only eliminates the need for large bus capacitors but also enables further topology simplification by removing the redundant switches.

Table 6.2: Key parameters of the hardware prototype

Parameter	Value
Input voltage	48 V
Tested output voltage	1.0-1.5 V
Maximum output current	270 A
Switching frequency	280 kHz
Gate drive voltage	6.5 V
Prototype box volume [*]	0.750 in ³
Power component volume ⁺	0.381 in ³
Current density	360 A/in ³

^{*} The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.

⁺ The power component volume is calculated as the total volume of all switching devices, capacitors and inductors in the power stage, excluding the gate drive circuitry.

The output voltage of the proposed converter can be derived by multiplying the conversion ratios of the fixed-ratio SC stage and the regulated buck stage as

$$V_{\text{out}} = \text{Ratio}_{\text{SC}} \times \text{Ratio}_{\text{buck}} = \frac{V_{\text{in}}}{9} \times \frac{D}{3} = \frac{D}{27} V_{\text{in}} \quad (6.1)$$

where D is the duty ratio with respect to $\frac{T}{3}$, as illustrated in Fig. 6.2. Thus, V_{out} can be regulated by adjusting D .

6.2 Hardware Implementation

A 48 V-to-PoL hardware prototype is designed and tested up to 270 A load current to verify the functionality and performance of the proposed topology. The key parameters of the hardware prototype are listed in Table 6.2. Fig. 6.3 shows the annotated photograph of the hardware prototype, with the 3D view of its assembly drawing and the side view presented in Fig. 6.4. As shown in Figs. 6.3 and 6.4, the modular structure of the proposed topology eases the PCB layout design. The inductors are recessed in the board cut-out to reduce the overall height. As can be seen in Fig. 6.4, S-shape copper sheets are placed between the inductors for ground connection with tight packaging.

Table 6.3 tabulates the components used in the hardware prototype. Two paralleled MOSFETs are used for the bottom switches in the buck stage $Q_{3-5(\text{m1})-(\text{m3})}$ to reduce the ON-resistance and achieve higher heavy-load efficiency. Low-profile capacitors (thickness: 0.85 mm) are selected for the bottom side so that the overall component height on the bottom side (i.e., h_{bottom} in Fig. 6.4(b)) will not be increased. The shielded power inductor Coilcraft SLR1065-301KEC with low DCR is chosen for higher heavy-load efficiency. The

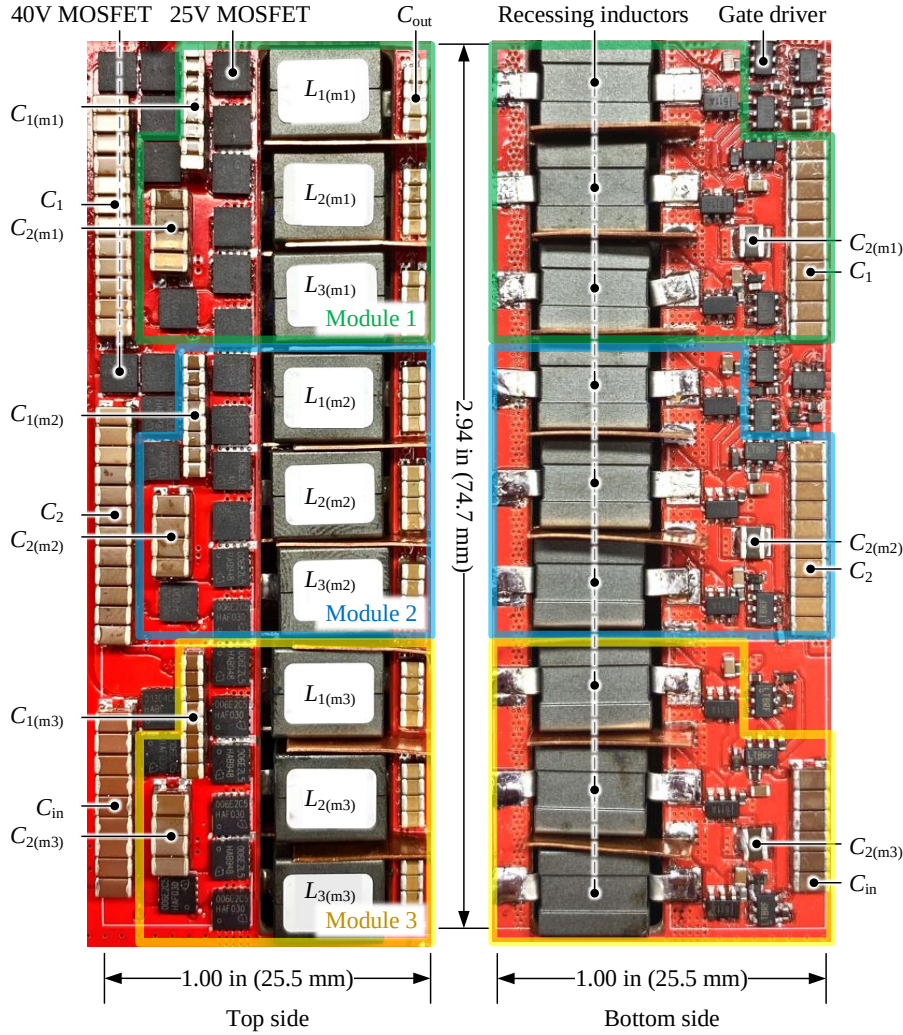


Figure 6.3: Photograph of the hardware prototype. Dimensions: $2.94 \times 1.00 \times 0.25$ in ($74.7 \times 25.5 \times 6.45$ mm). (6 layers, 4 oz copper on outer layers, 2 oz copper on inner layers)

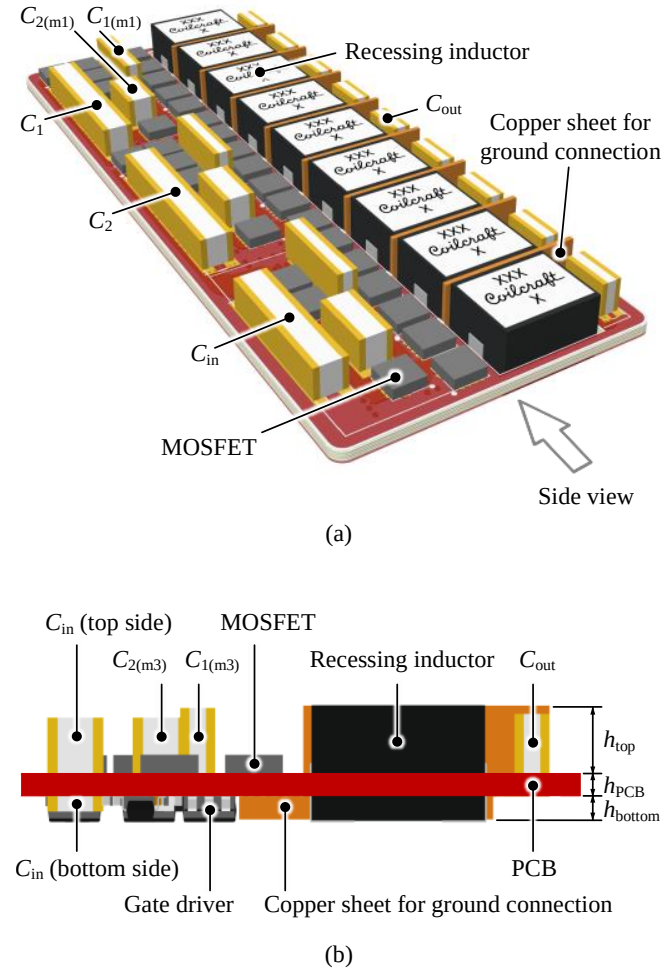


Figure 6.4: 3D view of the hardware prototype. (a) Assembly drawing. (b) Side view. ($h_{top} = 3.75$ mm, $h_{PCB} = 1.6$ mm, $h_{bottom} = 1.1$ mm)

Table 6.3: Component list of the hardware prototype

Component	Part number	Parameters
MOSFET $Q_{1,4,6}$	Infineon IQE006NE2LM5	25 V, 0.65 m Ω
MOSFET $Q_{2,3}$	Infineon IQE013N04LM6CG	40 V, 1.35 m Ω
MOSFET $Q_{5,7}, Q_{1,2(m1)-(m3)}$	Infineon IQE006NE2LM5CG	25 V, 0.65 m Ω
MOSFET $Q_{3-5(m1)-(m3)}$	Infineon IQE006NE2LM5CG, IQE006NE2LM5	25 V, 0.65 m Ω (in parallel)
Flying capacitor C_1	TDK CGA5L3X5R1H106M160AB (top side)	X5R, 50 V, 10 $\mu\text{F}^* \times 24$ (in parallel)
	TDK C3216X5R1H475K085AB (bottom side)	X5R, 50 V, 4.7 $\mu\text{F}^* \times 12$ (in parallel)
Flying capacitor C_2	TDK C3216X5R1E476M160AC (top side)	X5R, 25 V, 47 $\mu\text{F}^* \times 24$ (in parallel)
	TDK C3216X5R1E106M085AC (bottom side)	X5R, 25 V, 10 $\mu\text{F}^* \times 12$ (in parallel)
Flying capacitor $C_{1(m1)-(m3)}$	TDK C2012X5R1C226M125AC	X5R, 16 V, 22 $\mu\text{F}^* \times 24$ (in parallel)
Flying capacitor $C_{2(m1)-(m3)}$	TDK C3216X5R1A686M160AC (top side)	X5R, 10 V, 22 $\mu\text{F}^* \times 8$ (in parallel)
	TDK C2012X5R1A226M085AC (bottom side)	X5R, 25 V, 10 $\mu\text{F}^* \times 2$ (in parallel)
Inductors $L_{1(m1)}-L_{3(m3)}$	Coilcraft SLR1065-301KEC	300 nH, 0.48 m Ω , 32 A
Input capacitor C_{in}	TDK CGA5L3X7S2A335M160AB (top side)	X7S, 100 V, 3.3 $\mu\text{F}^* \times 18$ (in parallel)
	Kyocera AVX 12061C225KAT2A (bottom side)	X7R, 100 V, 2.2 $\mu\text{F}^* \times 9$ (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 $\mu\text{F}^* \times 108$ (in parallel)
Gate driver	Analog Devices LTC4440-5	High-side gate driver, 80 V
	Texas Instruments UCC27511ADBVT	Low-side gate driver
Bootstrap diode	Infineon BAT6402VH6327XTSA1	Schottky diode, 40 V

* The capacitance listed in this table is the nominal value before dc derating.

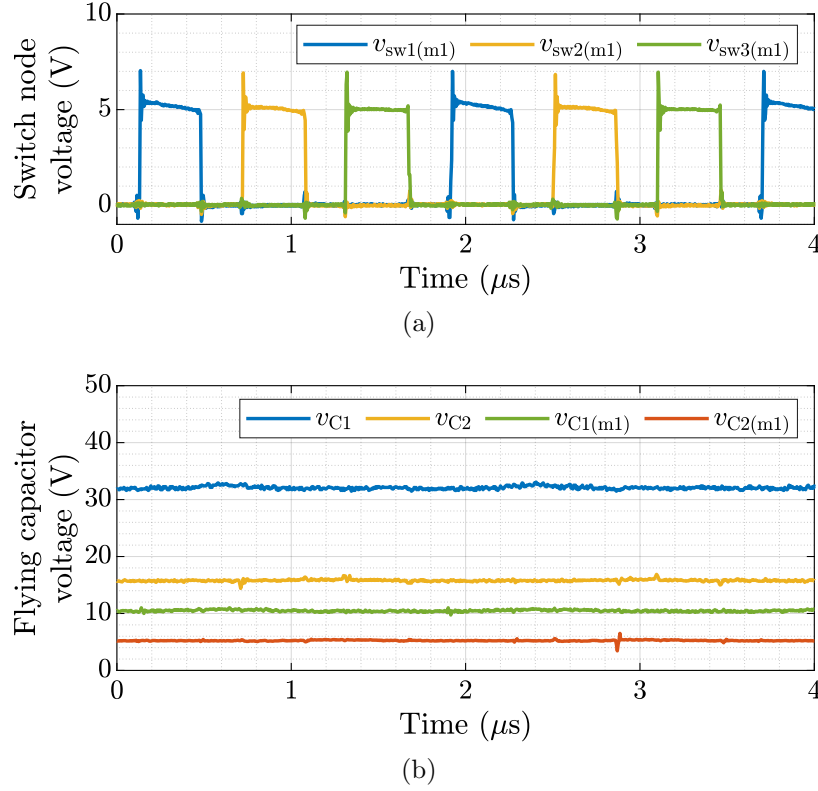


Figure 6.5: Measured waveforms at $V_{out} = 1.0$ V, $I_{out} = 200$ A. (a) Switch node voltages in Module 1. (b) Flying capacitor voltages.

cascaded bootstrap and gate-driven charge pump circuits introduced in [41] are adopted to power the floating switches.

6.3 Experimental Results and Performance Comparison

Fig. 6.5 shows the measured waveforms of the switch node voltages in Module 1 (i.e., $v_{sw1-3(m1)}$ in Fig. 6.1(b)) and the flying capacitor voltages, which verifies the functionality of the hardware prototype. The output voltage is regulated with a hysteretic control on the duty ratio D . Figs. 6.6(a) and (b) show the measured power stage efficiency and overall system efficiency (including gate drive loss) of the hardware prototype at various output voltages, with the measured efficiency and power density summarized in Table 6.4. The input voltage, input current, and output voltage are measured with a high-precision Yokogawa WT3000E power meter, and the load current is measured with an electronic load Chroma 63203. The prototype is tested up to 270 A. At 1.0 V output voltage, the prototype achieves

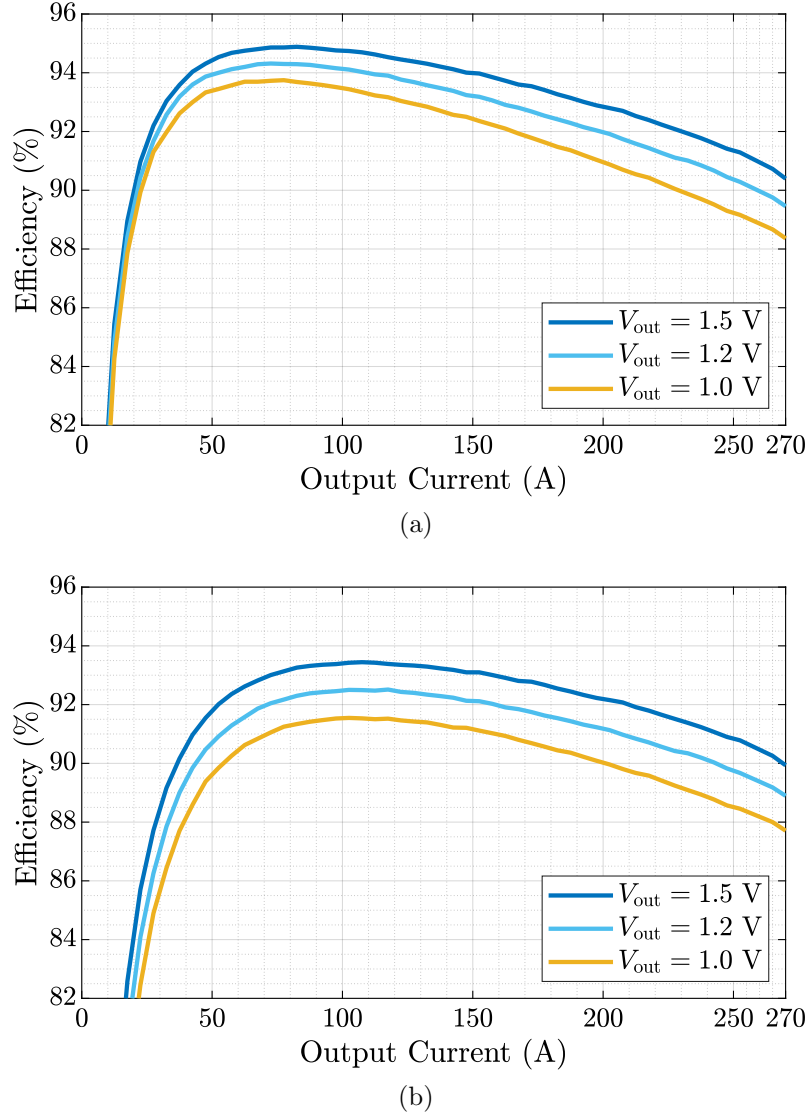


Figure 6.6: Measured efficiency of the hardware prototype at various output voltages. (a) Power stage efficiency. (b) Overall system efficiency (including gate drive loss).

93.8% peak efficiency (91.6% including gate drive loss) and 88.4% full-load efficiency (87.7% including gate drive loss), and 360 W/in³ power density (by box volume).

Fig. 6.7 shows the thermal image of the hardware prototype at equilibrium with fan cooling only at $V_{out} = 1.0$ V and $I_{out} = 270$ A. As can be seen in Fig. 6.7, the hot spots are the floating switches in the middle of the converter. This is because they are neither connected to large pieces of copper in the PCB nor close to the ground plane that can serve as a good heat extractor. Since there is still space left above the MOSFETs, as illustrated in Fig. 6.4(b), heat sinks can be added to the top of the switches for more effective cooling

Table 6.4: Measured efficiency and power density of the prototype at various output voltages

Output voltage	Power stage efficiency	System efficiency (including gate drive loss)	Power density*
1.5 V	Peak: 94.9% Full load: 90.4%	Peak: 93.5% Full load: 89.9%	540 W/in ³ 137 W/in ²
1.2 V	Peak: 94.3% Full load: 89.5%	Peak: 92.5% Full load: 88.9%	432 W/in ³ 110 W/in ²
1.0 V	Peak: 93.8% Full load: 88.4%	Peak: 91.6% Full load: 87.7%	360 W/in ³ 91 W/in ²

* The volumetric power density listed here is calculated based on the prototype box volume in Table 6.2. The areal power density listed here is calculated based on the prototype area 2.94×1.00 inch (74.7×25.5 mm) shown in Fig. 6.3.

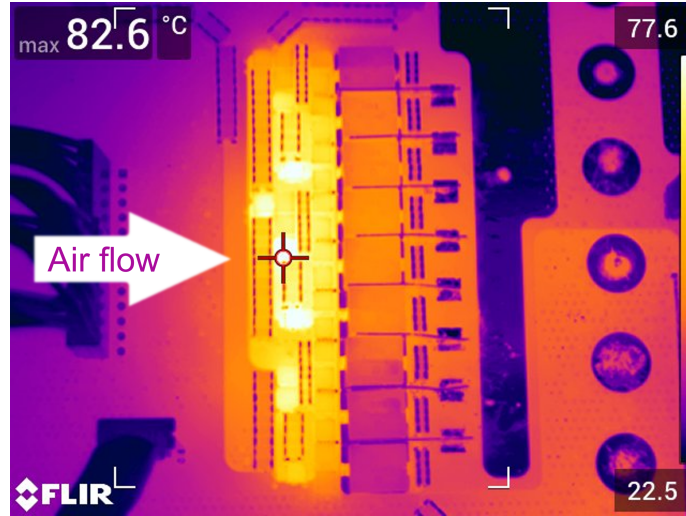


Figure 6.7: Thermal image of the hardware prototype at equilibrium with fan cooling only. ($V_{\text{out}} = 1.0$ V, $I_{\text{out}} = 270$ A)

if better thermal performance is desired.

Table 6.5 compares the performance of this work (Dickson²), with that of several hybrid SC works published before 2022, when the Dickson² converter was first proposed. It can be seen that the proposed Dickson² converter not only achieves a high power density but also maintains excellent peak and full-load efficiency, demonstrating great potential for both high efficiency and high power density. Further optimization can be achieved with advanced

Table 6.5: Comparison between this work (Dickson²) and previous 48 V-to-PoL hybrid SC works

Year	Reference	Output Voltage	Output Current	Power Density ⁺	Power Stage Efficiency
2022	This work (Dickson ² [75])	1.5 V	270 A (30 A/phase)	540 W/in ³ (by box volume) 1062 W/in ³ (by power component volume)	Peak efficiency: 94.9% Full load efficiency: 90.4%
		1.0 V	270 A (30 A/phase)	360 W/in ³ (by box volume) 708 W/in ³ (by power component volume)	Peak efficiency: 93.8% Full load efficiency: 88.4%
2022	MLB [76]	1.0 V	60 A (30 A/phase)	263 W/in ³ (by box volume)	Peak efficiency: 92.7% Full load efficiency: 88.6%
2021	CaSP [64]	1.5 V	90 A (30 A/phase)	527 W/in ³ (by box volume)	Peak efficiency: 93.3% Full load efficiency: 88.8%
2021	VIB [77]	1.0 V	450 A (28.1 A/phase)	232 W/in ³ (by box volume)	Peak efficiency: 95.2% Full load efficiency: 89.1%
2021	On-chip series capacitor buck [78]	1.0 V	8 A (4 A/phase)	198 W/in ³ (by box volume)	Peak efficiency: 90.2% Full load efficiency: ~76%
2020	LEGO [69]	1.5 V	300 A (25 A/phase)	171 W/in ^{3*} (by box volume)	Peak efficiency: 96.0%* Full load efficiency: 87.7%*
2020	Crossed-coupled QSD buck [70]	1.5 V	40 A (20 A/phase)	150 W/in ³ (by power component volume)	Peak efficiency: 95.1%* Full load efficiency: 92.7%*

⁺ The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry. The power component volume is calculated as the total volume of all switching devices, capacitors, and inductors in the power stage, excluding the gate drive circuitry.

* According to direct correspondence with the author.

magnetic components (e.g., customized coupled inductors [76]) and better thermal design (e.g., 3D printed heat sink and immersion cooling).

6.4 Chapter Summary

This chapter presents a Dickson² hybrid SC converter for direct 48 V-to-PoL conversion with high efficiency and high power density. The SC stage in the proposed topology can be viewed as two 3-to-1 Dickson SC converters directly merged together without an intermediate dc bus, and thus given the name *Dickson²*. The proposed converter achieves complete soft-charging operation with a simple control, ensures naturally balanced interleaved inductor currents, has a high SC stage conversion ratio and reduced conversion burden on the buck stage, and requires no large bus capacitors due to the switching bus architecture. A 48 V-to-PoL hardware prototype is built and tested up to 270 A load current (30 A/phase), achieving 93.8% peak efficiency, 88.4% full-load efficiency, and 360 W/in³ power density (by box volume) at 1.0 V output voltage.

Chapter 7

The Switching Bus Converter: A High-Performance 48-V-to-1-V Architecture with Increased SC Conversion Ratio

This chapter proposes a high-performance hybrid SC converter based on a switching bus architecture for direct 48-to-1-V power conversion in data centers. The proposed topology merges a 2-to-1 SC front-end and two 8-branch series-capacitor-buck (SCB) modules through two switching buses. In order to theoretically compare the performance of different regulated hybrid SC topologies, this chapter conducts a comparative analysis that reveals that a larger SC stage conversion ratio is favorable for achieving both higher efficiency and higher power density. Through the two-phase operation of the SCB modules, the proposed topology extends the limit on duty ratio and enables a very large SC stage conversion ratio of 16-to-1. A 500-A hardware prototype was designed and built with custom two-phase coupled inductors and synchronous bootstrap daughterboards to validate the functionality and performance of the proposed topology, achieving 93.4% peak system efficiency, 86.1% full-load system efficiency (including gate drive loss), and 464-W/in³ power density (by box volume). Moreover, the theoretical benefits of a larger SC stage conversion ratio were experimentally verified with measured performance at different SC stage conversion ratios.

The remainder of this chapter is organized as follows. First, Section 7.1 details the topology and operating principles of the proposed switching bus converter, discusses the advantages of the switching-bus-based architecture, reveals the benefits of a larger SC stage conversion ratio for regulated hybrid SC topologies, and explains how this works achieves a large SC stage conversion ratio through the two-phase operation of the SCB modules. Then, Section 7.2 presents a hardware prototype with custom two-phase coupled inductors and synchronous bootstrap daughterboards and discusses its design considerations and practical implementation challenges. Finally, Section 7.3 shows the experimental waveforms, measured performance at different SC stage conversion ratios, loss analysis, and performance

comparison with state-of-the-art academic works and commercial products.

7.1 Proposed Topology and Operating Principles

7.1.1 Proposed Topology

Fig. 7.1 shows the schematic drawing of the proposed switching bus converter. In the proposed topology, a 2-to-1 SC front-end (i.e., Stage 1) is merged with two 8-branch series-capacitor-buck (SCB) modules (i.e., Modules A and B in Stage 2) through two switching buses (i.e., Switching buses A and B). As the key waveforms in Fig. 7.2 shows, the bus voltages v_{swA} and v_{swB} always switch between two different levels, rather than being dc. Therefore, this type of intermediate bus between conversion stages is referred to as a *switching bus*. The concept of a switching bus was first introduced in [75]. The advantages of the proposed switching-bus-based architecture over the existing dc-bus-based architecture will be explained in Section 7.1.4.

7.1.2 Operating Principles

Fig. 7.2 illustrates the key waveforms, control signals, and equivalent circuits of the proposed switching bus converter. Each SCB module operates in a two-phase fashion, with a 180° phase shift between neighboring branches. Each SCB module consists of four submodules, within which each pair of inductors is negatively coupled. The analysis and design of the two-phase coupled inductor will be detailed in Section 7.2.1. The control signals in the two modules are staggered to achieve inter-module interleaving at the output.

In periodic steady state, the average voltage across flying capacitor C_1 is $\frac{1}{2}V_{in}$ and the average voltages across flying capacitors $C_{kA/B}$ are $\frac{8-k}{16}V_{in}$ ($k = 1, 2, \dots, 7$). C_1 is softly charged by L_{1A} through Switching bus A in operating modes ① and ②, and softly discharged by L_{1B} through Switching bus B in operating modes ⑤ and ⑥. All other flying capacitors in Stage 2 $C_{kA/B}$ ($k = 1, 2, \dots, 7$) operate with complete soft-charging as well. All inductor currents and capacitor voltages are naturally balanced as a result of the negative feedback mechanism of the series-capacitor-buck converter, as explained in [79] and [64]. A detailed explanation about the automatic current sharing and natural voltage balancing mechanisms of the proposed topology is provided in Section 7.1.3. The low-side switches $S_{1LA/B-8LA/B}$ can operate with zero-voltage switching (ZVS) turn-ON, provided continuous forward inductor current and sufficient deadtime. The output voltage V_{out} can be regulated by duty cycle control:

$$V_{out} = \frac{D}{16}V_{in}, \quad (7.1)$$

where V_{in} is the input voltage and D is the buck stage duty ratio as annotated in the clocking scheme in Fig. 7.2.

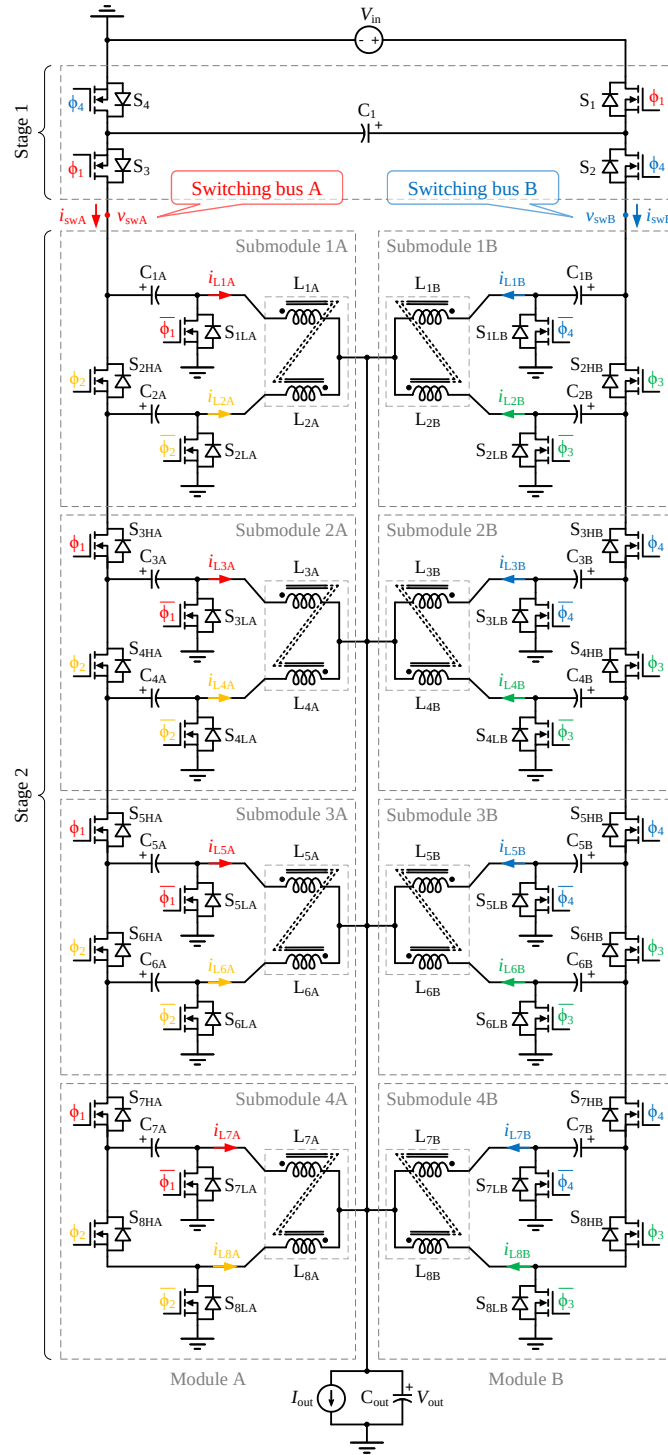


Figure 7.1: Schematic drawing of the proposed switching bus converter.



Figure 7.2: Key waveforms and control signals of the proposed switching bus converter. The equivalent circuits for the six operating modes are shown on the right-hand side. The sequence of operating modes: ① $\rightarrow$ ② $\rightarrow$ ③ $\rightarrow$ ④ $\rightarrow$ ⑤ $\rightarrow$ ⑥ $\rightarrow$ ① $\rightarrow$ ② $\rightarrow$ ③ $\rightarrow$ $\dots$.

7.1.3 Automatic Current Sharing and Natural Voltage Balancing Mechanisms

This Section explains the automatic current sharing and natural voltage balancing mechanisms of the proposed switching bus converter. First, a quantitative analysis is performed to show that the balanced state is the natural equilibrium of the converter in periodic steady state (PSS). Second, a qualitative analysis is provided to intuitively explain how the converter counteracts any temporary imbalance in inductor currents and capacitor voltages and restores them to their balanced states after disturbance.

7.1.3.1 Quantitative Analysis

• Automatic Current Sharing Mechanism

Denote the average currents of the inductors and capacitors in the switching bus converter as $\langle i_{LjA/B} \rangle$ ($j = 1, 2, \dots, 8$), $\langle i_{C1} \rangle$, $\langle i_{CkA/B} \rangle$ ($k = 1, 2, \dots, 7$), and $\langle i_{Cout} \rangle$. According to Kirchhoff's current law (KCL), the average current flowing through the capacitors in Fig. 7.1 can be expressed as

$$\langle i_{C1} \rangle = D (\langle i_{L1A} \rangle - \langle i_{L1B} \rangle) \quad (7.2)$$

$$\langle i_{CkA/B} \rangle = D (\langle i_{LkA/B} \rangle - \langle i_{L(k+1)A/B} \rangle) \quad (k = 1, 2, \dots, 7) \quad (7.3)$$

$$\langle i_{Cout} \rangle = \sum_{j=1}^8 \langle i_{LjA} \rangle + \sum_{j=1}^8 \langle i_{LjB} \rangle - I_{out} \quad (7.4)$$

where D is the duty ratio, and I_{out} is the output current.

In PSS, the average capacitor currents must be zero, i.e.,

$$\langle i_{C1} \rangle = 0 \quad (7.5)$$

$$\langle i_{CkA/B} \rangle = 0 \quad (k = 1, 2, \dots, 7) \quad (7.6)$$

$$\langle i_{Cout} \rangle = 0 \quad (7.7)$$

Substituting (7.5)–(7.7) into (7.2)–(7.4) yields

$$\langle i_{L1A} \rangle = \langle i_{L2A} \rangle = \dots = \langle i_{L8A} \rangle = \langle i_{L1B} \rangle = \langle i_{L2B} \rangle = \dots = \langle i_{L8B} \rangle = \frac{1}{16} I_{out} \quad (7.8)$$

This implies the output current can be evenly shared among all inductors in the natural equilibrium.

• Natural Voltage Balancing Mechanism

Denote the average voltages of the inductors and capacitors in the switching bus converter as $\langle v_{LjA/B} \rangle$ ($j = 1, 2, \dots, 8$), $\langle v_{C1} \rangle$, $\langle v_{CkA/B} \rangle$ ($k = 1, 2, \dots, 7$), and $\langle v_{Cout} \rangle$. According to

Kirchhoff's voltage law (KVL), the average voltage applied across the inductors in Fig. 7.1 can be expressed as

$$\langle v_{L1A} \rangle = D(V_{in} - \langle v_{C1} \rangle - \langle v_{C1A} \rangle) - \langle v_{Cout} \rangle \quad (7.9)$$

$$\langle v_{L1B} \rangle = D(\langle v_{C1} \rangle - \langle v_{C1B} \rangle) - \langle v_{Cout} \rangle \quad (7.10)$$

$$\langle v_{LjA/B} \rangle = D(\langle v_{C(j-1)A/B} \rangle - \langle v_{CjA/B} \rangle) - \langle v_{Cout} \rangle \quad (j = 2, 3, \dots, 7) \quad (7.11)$$

$$\langle v_{L8A/B} \rangle = D\langle v_{C7A/B} \rangle - \langle v_{Cout} \rangle \quad (7.12)$$

where V_{in} is the input voltage.

In PSS, the average inductor voltages must be zero, i.e.,

$$\langle v_{L1A} \rangle = 0 \quad (7.13)$$

$$\langle v_{L1B} \rangle = 0 \quad (7.14)$$

$$\langle v_{LjA/B} \rangle = 0 \quad (j = 2, 3, \dots, 7) \quad (7.15)$$

$$\langle v_{L8A/B} \rangle = 0 \quad (7.16)$$

Substituting (7.13)–(7.16) into (7.9)–(7.12) yields

$$\langle v_{C1} \rangle = \frac{1}{2}V_{in}, \quad \langle v_{Cout} \rangle = \frac{D}{16}V_{in}, \quad \langle v_{CkA/B} \rangle = \frac{8-k}{16}V_{in} \quad (k = 1, 2, \dots, 7) \quad (7.17)$$

which means the capacitor voltages can naturally balance themselves in the equilibrium.

Equations (7.8) and (7.17) show that the balanced state is the natural equilibrium of the switching bus converter in PSS. It is worth noting that this quantitative analysis is independent of the values of inductors and capacitors. Therefore, the automatic current sharing and natural voltage balancing mechanisms do not rely on component accuracy and can tolerate passive component tolerance, variations, and derating.

7.1.3.2 Qualitative Analysis

Due to a negative feedback mechanism, the switching bus converter can counteract any temporary imbalance in inductor currents and capacitor voltages and restore them to their balanced states. This subsection qualitatively explains the automatic current sharing of inductor L_{1A} and the natural voltage balancing of capacitor C_{1A} as examples.

• Automatic Current Sharing Mechanism

Consider the case where $\langle i_{L1A} \rangle > \frac{1}{16}I_{out}$ (the average current through L_{1A} in the balanced state) and all other inductor currents and capacitor voltages are in their balanced states.

Due to this deviation of $\langle i_{L1A} \rangle$ from the equilibrium, the average current flowing into C_1 and C_{1A} in operating modes ① and ② in Fig. 7.2 will be higher than that flowing out of them in operating modes ④–⑥. As a result, the net charge flowing into C_1 and C_{1A} in each switching cycle is positive, leading to an increase in $\langle v_{C1} \rangle$ and $\langle v_{C1A} \rangle$, which makes

$\langle v_{C1} \rangle > \frac{1}{2}V_{in}$ and $\langle v_{C1} \rangle > \frac{7}{16}V_{in}$. Consequently, the switch-node voltage applied to the left-hand side of L_{1A} in operating modes ① and ② will be lower than $\frac{1}{16}V_{in}$ (the voltage applied to the left-hand side of L_{1A} in the balanced state). This means that $\langle i_{L1A} \rangle$ will then start to decrease until $\langle i_{L1A} \rangle = \frac{1}{16}I_{out}$.

Similarly, if $\langle i_{L1A} \rangle < \frac{1}{16}I_{out}$, the net charge flowing into C_1 and C_{1A} in each switching cycle will be negative, forcing $\langle v_{C1} \rangle$ and $\langle v_{C1A} \rangle$ to decrease, which makes $\langle v_{C1} \rangle < \frac{1}{2}V_{in}$ and $\langle v_{C1} \rangle < \frac{7}{16}V_{in}$. As a result, $\langle i_{L1A} \rangle$ will increase until $\langle i_{L1A} \rangle = \frac{1}{16}I_{out}$.

This negative feedback mechanism applies to other inductor currents as well. In addition, the inductor currents can be evenly shared between the two SCB modules due to this current-voltage interaction through capacitor C_1 .

• Natural Voltage Balancing Mechanism

Consider the case where $\langle v_{C1A} \rangle > \frac{7}{16}V_{in}$ (the average voltage across C_{1A} in the balanced state) and all other inductor currents and capacitor voltages are in their balanced states.

Due to this deviation of $\langle v_{C1A} \rangle$ from the equilibrium, the switch-node voltage applied to the left-hand side of L_{1A} in operating modes ① and ② is lower than $\frac{1}{16}V_{in}$ (the voltage applied to the left-hand side of L_{1A} in the balanced state). As a result, $\langle i_{L1A} \rangle$ will decrease below $\frac{1}{16}I_{out}$. Therefore, the average current flowing into C_{1A} in operating modes ① and ② will be higher than that flowing out of it in operating modes ④–⑥. Consequently, the net charge flowing into C_{1A} in each switching cycle will be positive, which forces $\langle v_{C1A} \rangle$ to increase until $\langle v_{C1A} \rangle = \frac{7}{16}V_{in}$.

Similarly, if $\langle v_{C1A} \rangle < \frac{7}{16}V_{in}$, $\langle i_{L1A} \rangle$ will increase beyond $\frac{1}{16}I_{out}$, causing the net charge flowing into C_{1A} in each switching cycle to be negative. As a result, $\langle v_{C1A} \rangle$ will increase until $\langle v_{C1A} \rangle = \frac{7}{16}V_{in}$. This negative feedback mechanism applies to other capacitor voltages as well.

In summary, the quantitative analysis proves that the balanced state is the natural equilibrium of the converter in PSS, while the qualitative analysis shows that the converter can counteract any temporary imbalance in inductor currents and capacitor voltages due to the negative feedback mechanism explained above, thereby restoring them to their balanced states. This means that the balanced state is naturally a stable equilibrium of the converter in PSS. Therefore, the inductor currents and capacitor voltages can be naturally balanced in PSS without any active balancing control.

It is worth noting that the above analyses are based on the assumption that the converter operates in the continuous capacitor voltage mode (CCVM). With very large voltage ripples on the flying capacitors, capacitor voltage clamping can occur through the reverse conduction of the switching devices, driving the converter into a discontinuous capacitor voltage mode (DCVM) [80]. In DCVM, inductor currents can no longer be automatically balanced. Instead, a modified duty cycle scheme can be used to recover the inductor current balancing. The discussion of the DCVM operation of the switching bus converter is beyond the scope of this chapter.

7.1.4 Advantages of the Switching-Bus-Based Architecture

The most straightforward approach to combining two (or multiple) conversion stages is to link them with an intermediate dc bus, as illustrated in Fig. 7.3(a). This dc-bus-based architecture typically requires a large and bulky bus capacitor (C_{bus}) to maintain a stiff dc bus voltage (V_{DC}), which hinders converter miniaturization.

Compared to the existing dc-bus-based architecture, the proposed switching-bus-based architecture shown in Fig. 7.3(b) has three advantages that promise higher performance:

- It does not require bus capacitors to maintain a stiff dc bus voltage.
- One redundant switch can be removed on each switching bus while two stages are merged.
- It ensures complete soft-charging operation.

Fig. 7.4 illustrates the two-stage merging process of a 2-to-1 SC front-end followed by two SCB modules, resulting in a switching bus architecture. First, open the output node of the 2-to-1 SC converter in Stage 1 as shown in Fig. 7.4(a), leaving two floating nodes v_{swA} and v_{swB} . Second, as illustrated in Fig. 7.4(b), connect a series-capacitor buck (SCB) module to each of these floating nodes through a switching bus. After this combination, we can see that the highest high-side switch $S_{1\text{HA}}$ in Module A is connected in series with S_3 and $S_{1\text{HB}}$ in Module B is in series with S_2 . Since none of the switching buses need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, compared to the dc-bus-based architecture, the switching-bus-based architecture enables a reduction in the number of switches.

In addition, the switching-bus-based architecture ensures complete soft-charging operation for all flying capacitors with a simple clocking scheme, whereas complete soft-charging operation is only achievable with split-phase control [72] in some topologies [81, 82] or even unachievable in other topologies [77, 83], leading to higher power loss and greater controller complexity.

Fig. 7.5 shows the general representation of a dc bus and a switching bus. The switching bus concept can be generalized to construct a family of regulated hybrid SC topologies through the combination of different SC topologies. For example, the concept of a switching bus was first introduced in [75], where a Dickson² topology was constructed by merging a 3-to-1 Dickson front-end and three 3-branch SCB modules through three switching buses. Other switching-bus-based regulated hybrid SC topologies include the MLB converter [65] and the CaSP converter [64], with all benefiting from a similar reduction in switch count due to the strategic merging of adjacent stages. In addition, the switching bus concept can also be employed to construct fixed-ratio multi-resonant SC topologies [84] for intermediate bus converters (IBCs) in data center applications.

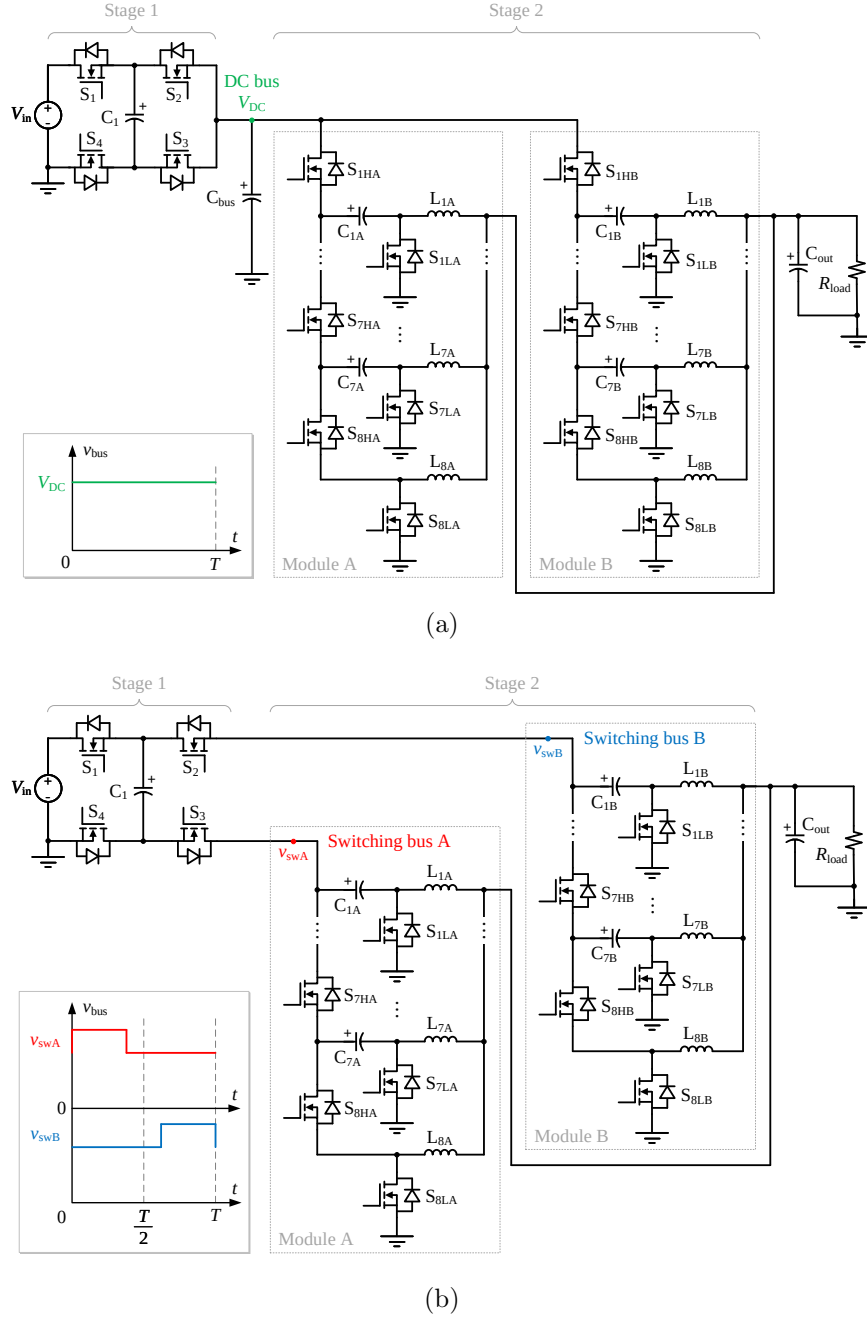


Figure 7.3: Comparison between the existing dc-bus-based architecture and the proposed switching-bus-based architecture. (a) dc-bus-based architecture. (b) Switching-bus-based architecture. Compared to the dc-bus-based architecture, the switching-bus-based architecture does not require bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

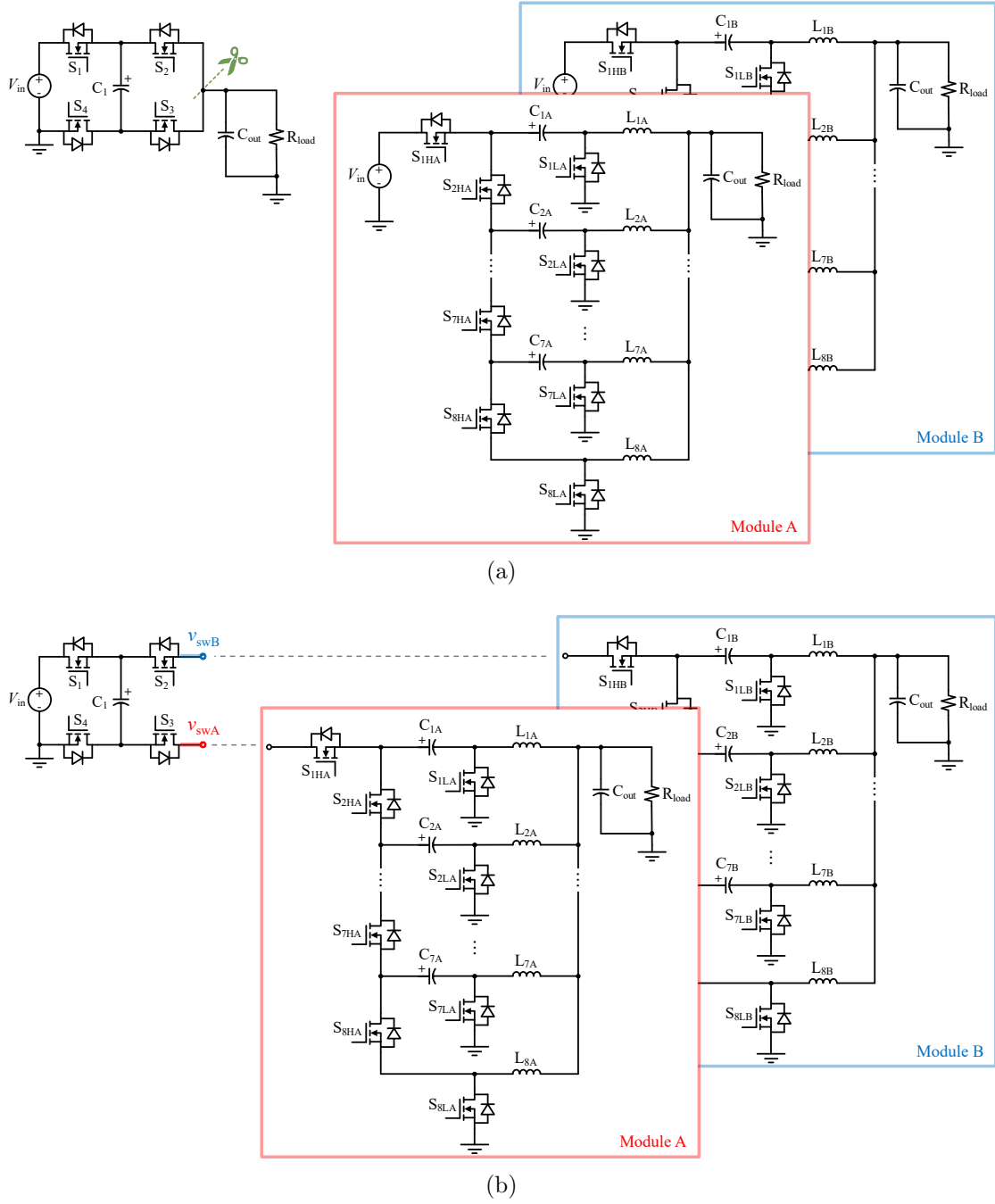
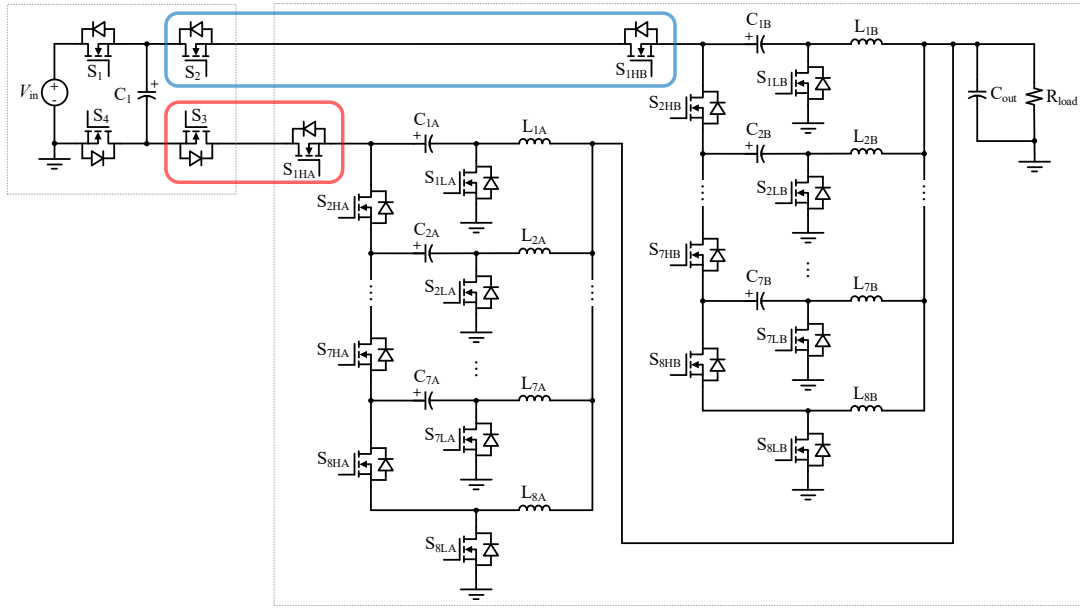
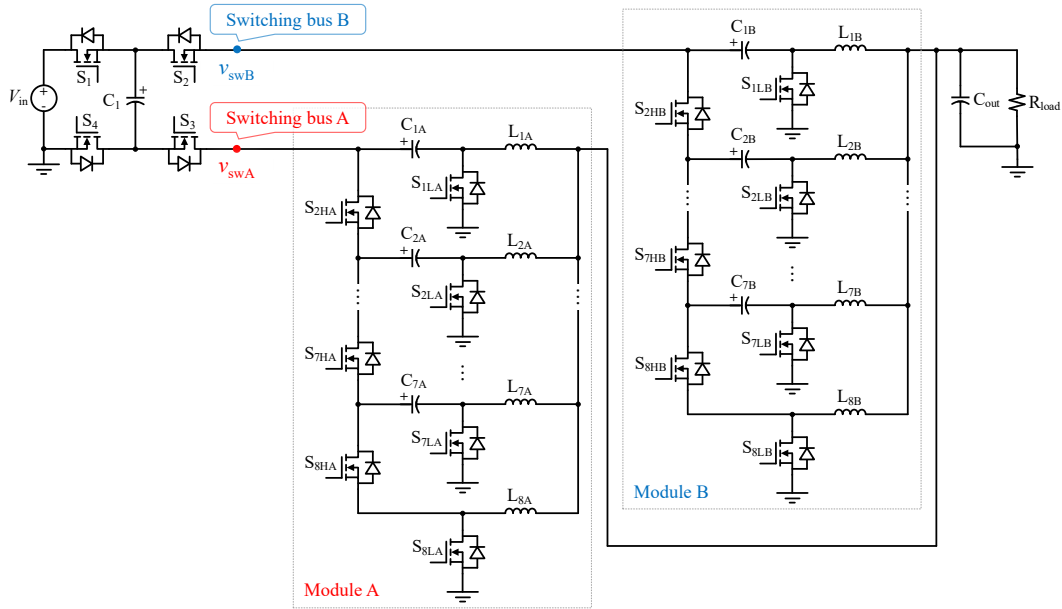


Figure 7.4: Illustration of the two-stage merging process of a 2-to-1 SC front-end followed by two SCB modules, resulting in a switching bus architecture. (a) First, open the output node of the 2-to-1 SC converter in Stage 1, leaving two floating nodes v_{swA} and v_{swB} . (b) Second, connect a series-capacitor buck (SCB) module to each of the floating nodes through a switching bus.



(c)



(d)

Figure 7.4 (continued): Illustration of the two-stage merging process of a 2-to-1 SC front-end followed by two SCB modules, resulting in a switching bus architecture. (c) Third, since none of the switching buses need to support bidirectional voltage blocking, only one switch is needed on each bus, and the other redundant one can be removed. Therefore, switches S_{1HA} and S_{1HB} are removed. (d) Finally, obtain the topology of one switching bus converter.

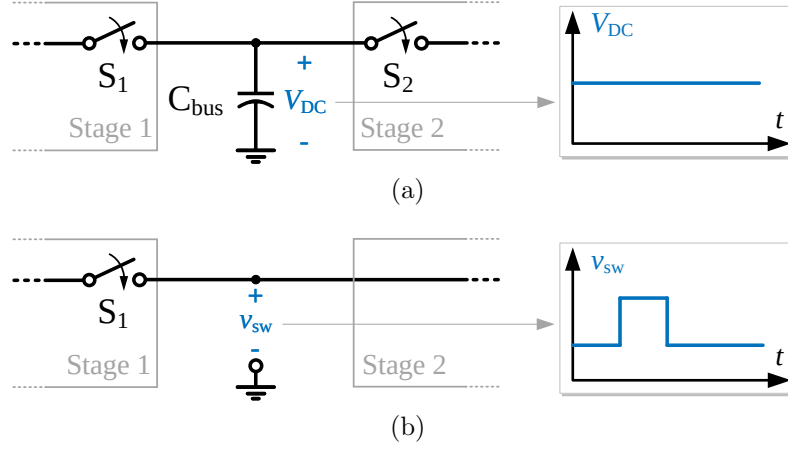


Figure 7.5: General representation of (a) a dc bus and (b) a switching bus.

7.1.5 Theoretical Analysis and Topological Comparison

To compare the theoretical potential of the proposed topology to that of existing 48-V-to-1-V hybrid SC topologies, this chapter uses two metrics for topological comparison [85].

The first metric is the normalized switch stress M_S , defined as the total switch volt-ampere (VA) stress normalized to the output power

$$M_S = \frac{\sum_{\text{switches}} V_{ds,i} I_{d(rms),i}}{V_{out} I_{out}}, \quad (7.18)$$

where $V_{ds,i}$ is the peak blocking voltage across switch i when assuming no capacitor voltage ripple, and $I_{d(rms),i}$ is the RMS value of the current through switch i when assuming no inductor current ripple. The normalized switch stress M_S indicates how much VA stress the switches in a topology experience when transferring one per-unit watt of power from the input to the output. A lower M_S is desirable, as it indicates lower switching losses and lower conduction losses and thus higher efficiency. A lower M_S also indicates a smaller switch size, which is favorable for higher power density. Fig. 7.6 shows the normalized switch stress M_S of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion.

The second metric is the normalized passive component volume M_P , which can be assessed with an energy-based approach by analyzing the peak energy stored in each passive component [86, 87]. The normalized passive component volume M_P indicates the total passive component volume needed to meet given ripple requirements on the inductor currents and flying capacitor voltages when transferring one per-unit watt of power from the input to the output. A smaller normalized passive component volume is desirable, as it indicates higher power density. More details of the definition of the normalized passive component volume M_P can be found in [85]. Fig. 7.7 shows the normalized passive component volume M_P of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion.

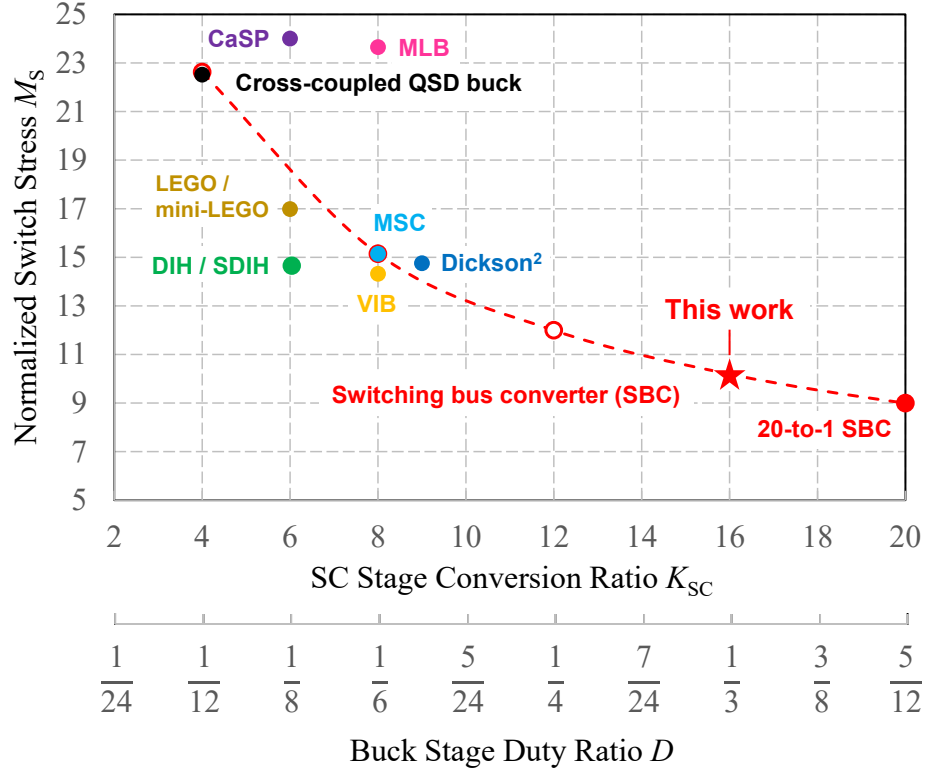


Figure 7.6: Normalized switch stress M_S of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. In the analysis of normalized switch stress, capacitor voltage ripples and inductor current ripples are assumed to be negligible. A lower normalized switch stress M_S is more desirable. With a larger SC stage conversion ratio K_{SC} , the buck stage duty ratio D can be extended.

In general, a regulated hybrid SC topology consists of two stages: 1) a fixed-ratio SC stage for efficient and compact voltage conversion, and 2) a multi-phase buck-type stage for the remainder of the voltage conversion task, output voltage regulation, and soft-charging operation. With a larger SC stage conversion ratio, the conversion burden on the following buck-type stage can be alleviated, enabling buck-type stage efficiency improvement and inductor size reduction. Given that magnetic components are much less energy dense compared to capacitors [88] and typically dominate the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden so that the inductor volume of the buck-type stage can be reduced.

In the proposed switching bus converter, the SC stage conversion ratio can be changed by varying the number of submodules in Stage 2. The more submodules, the larger the SC stage conversion ratio. As shown in Figs. 7.6 and 7.7, as the SC stage conversion ratio increases, both the normalized switch stress M_S and the normalized passive component volume M_P decrease, meaning that a larger SC stage conversion ratio is advantageous to both higher

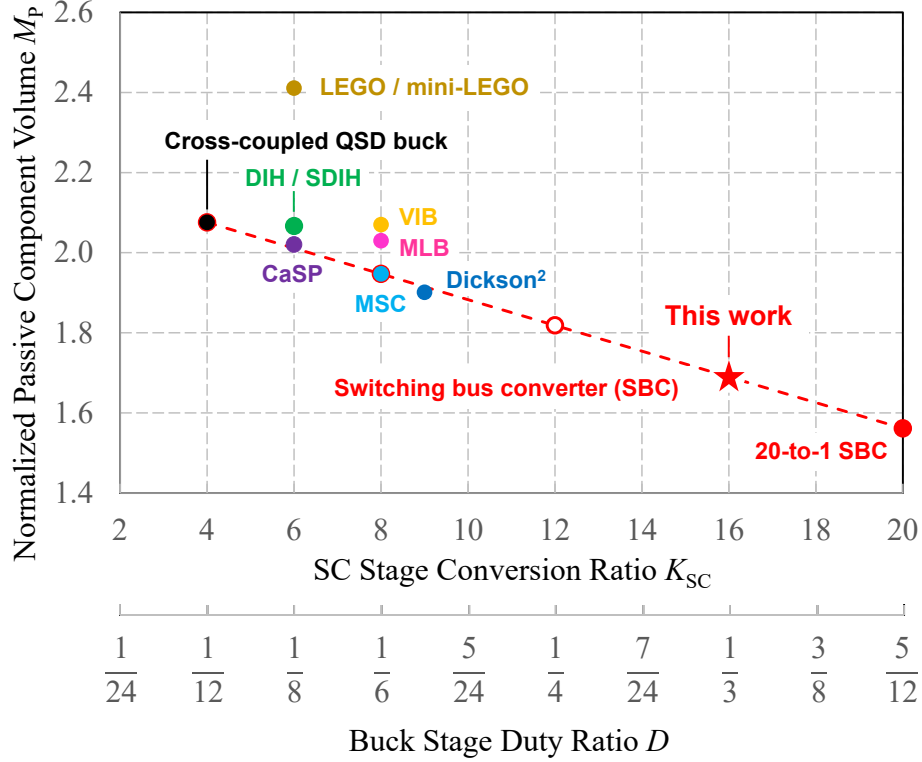


Figure 7.7: Normalized passive component volume M_P of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion (assuming 30% peak-to-peak inductor current ripple and 10% peak-to-peak capacitor voltage ripple at full load, and the volumetric energy density of capacitors is 100 times higher than inductors). A smaller normalized passive component volume M_P is more desirable.

efficiency and higher power density. This conclusion will be experimentally verified with the measured performance at different SC stage conversion ratios in Section 7.3.3. Compared with existing 48-V-to-1-V hybrid SC demonstrations, this work achieves a lower normalized switch stress and a smaller normalized passive component volume with a much larger SC stage conversion ratio, showing great potential for both higher efficiency and higher power density than prior solutions.

7.1.6 Two-Phase Operation of SCB Modules: Enabling A Larger SC Stage Conversion Ratio and Higher Performance

Figs. 7.6 and 7.7 show that a larger SC stage conversion ratio is desirable to achieve higher performance. In order to achieve a larger SC stage conversion ratio, this work modifies the control scheme of the SCB modules in Stage 2, from multi-phase operation to two-phase operation.

The series-capacitor-buck (SCB) topology was first proposed in [60] with multi-phase operation and then extended in [89] with two-phase operation. Fig. 7.8 shows a four-phase SCB converter as an example. In the multi-phase operation illustrated in Fig. 7.8(b), each inductor operates in an individual phase, whereas in the two-phase operation illustrated in Fig. 7.8(c), the inductors are grouped together into two phases with a 180° phase shift.

Compared to the two-phase operation, the multi-phase operation can achieve a smaller net output current ripple through multi-phase interleaving. However, the two-phase operation can extend the maximum duty ratio from $\frac{1}{N}$ to $\frac{1}{2}$, where N is the number of branches in a SCB converter. As a result, the upper limit on the number of branches ($N_{\text{m-ph}}$ and $N_{2\text{-ph}}$) can be increased:

$$\text{Multi-phase operation: } N_{\text{m-ph}} < \sqrt{\frac{V_{\text{in(SCB)}}}{V_{\text{out(SCB)}}}} \quad (7.19)$$

$$\text{Two-phase operation: } N_{2\text{-ph}} < \frac{V_{\text{in(SCB)}}}{2V_{\text{out(SCB)}}}, \quad (7.20)$$

where $V_{\text{in(SCB)}}$ and $V_{\text{out(SCB)}}$ are the input and output voltages of the SCB converter, respectively. For the proposed switching bus converter, the input and output voltages of the SCB modules in Stage 2 are $V_{\text{in(SCB)}} = 24$ V and $V_{\text{out(SCB)}} = 1$ V, respectively. Therefore, the maximum allowable numbers of branches in the SCB modules for multi-phase operation and two-phase operation are $N_{\text{m-ph(max)}} = 4$ and $N_{2\text{-ph(max)}} = 10$, respectively. Compared to the multi-phase operation, the two-phase operation can extend the upper limit on the number of branches and thus better leverage the benefit of a larger SC stage conversion ratio. In addition, the two-phase operation enables a faster transient response with an extended maximum duty ratio.

One possible concern about the two-phase operation is that it sacrifices the net output current ripple reduction compared to the multi-phase operation. However, this does not generally mean that the two-phase operation necessitates the need for a larger output capacitor. In PoL applications, the size of the output capacitor is typically determined by the requirements for transient performance (i.e., maximum overshoot and undershoot on output voltage). With a sufficiently large output capacitor to satisfy the transient performance requirements, the steady-state output voltage ripple is typically much smaller than the maximum tolerable value allowed by microprocessors. In other words, the output capacitor is usually oversized in terms of steady-state output voltage ripple suppression. Therefore, the output capacitance does not need to be increased when using the two-phase operation. In fact, since the two-phase operation enables a faster transient response compared to the multi-phase operation, the output capacitance can be reduced.

A major contribution of this work is to reveal that a larger SC stage conversion ratio enables higher performance of regulated hybrid SC topologies, which can be achieved through the two-phase operation of SCB modules.

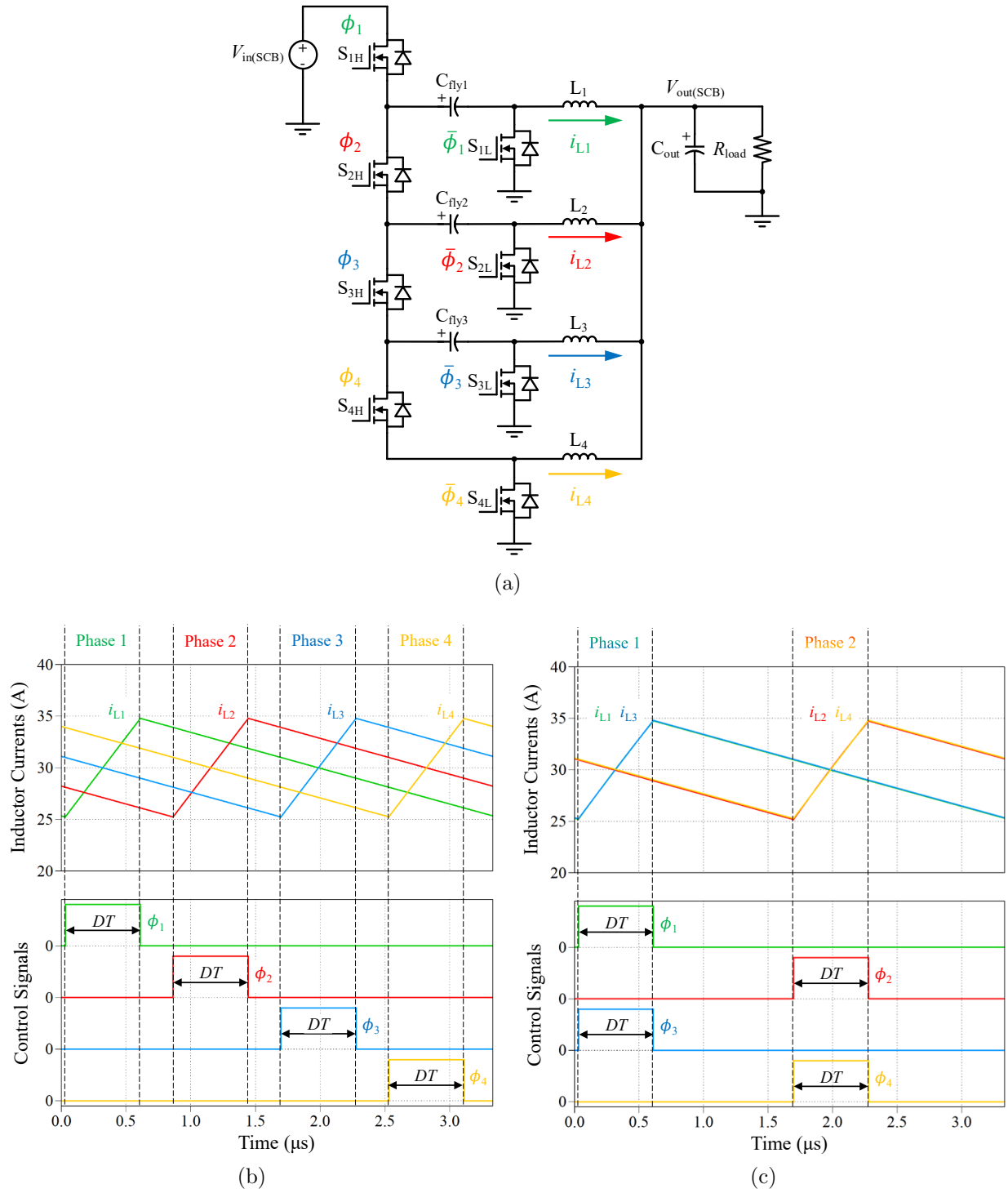


Figure 7.8: Four-branch series-capacitor-buck (SCB) converter. (a) Schematic drawing. (b) Multi-phase operation. (c) Two-phase operation.

7.2 Hardware Prototype and Practical Implementation Challenges

A 48-V-to-1-V hardware prototype was designed and built to verify the functionality and performance of the proposed switching bus converter. Fig. 7.9 shows an annotated photograph of the prototype, with the main circuit components listed in Table 7.1. Fig. 7.10 presents the side view of the hardware prototype and a zoomed-in photograph of the gate drive circuitry, including the custom synchronous bootstrap daughterboards used to power the high-side switches.

All flying capacitors are stacked up to 3 layers to match the height of the coupled inductors so that the box volume of the prototype can be fully utilized. The stacked flying capacitors serve as natural heat sinks due to their connection with power MOSFETs through thermally conductive PCB traces. In addition, the distributed switch and capacitor network provides an inherent heat spreading. The switching frequency of this prototype is 150 kHz. The 1.3-mm thick PCB has 8 layers, with 2 oz copper on each layer.

7.2.1 Analysis and Design of the Two-Phase Coupled Inductor

As demonstrated in [76], compared with discrete inductors, two-phase coupled inductors can reduce the core volume by approximately half while preserving the same equivalent per-phase steady-state inductance. To improve power density, the two-phase coupled inductor shown in Fig. 7.11 was customized and assembled for this prototype. The two phases are negatively coupled through the magnetic core combined from an E core and an I core. The magnetic cores were fabricated with DMEGC DMR96A Mn-Zn ferrite material. Each winding has two turns, and each turn is made from a piece of 0.5 mm thick and 2 mm wide copper. To reduce the total height of the coupled inductor, the two turns are connected with a PCB trace beneath the E core.

The key parameters and operating conditions of this two-phase coupled inductor are listed in Table 7.2. Operating at a duty ratio of 0.333, the equivalent per-phase steady-state inductance of this coupled inductor is 606.5 nH, leading to a peak-to-peak inductor current ripple of 7.33 A at 150-kHz switching frequency and 1.0-V output voltage. More details about the analysis and design of the two-phase coupled inductor are provided below.

As a rule of thumb, the peak-to-peak inductor current ripple ($\Delta i_{L,pp}$) of a buck converter is typically designed to be 20% to 40% of the full-load output current [90]. For the hardware prototype presented in this chapter, the inductor current ripple ratio was selected as 25%. Given a per-phase full-load current of 31.3 A, the maximum allowable peak-to-peak inductor current ripple is $\Delta i_{L,pp(max)} = 25\% \times 31.3 = 7.8$ A. In order to meet this current ripple requirement, the per-phase steady-state inductance should not be lower than

$$L_{ss(min)} = \frac{(1 - D)V_{out}}{f_{sw}\Delta i_{L,pp(max)}}, \quad (7.21)$$

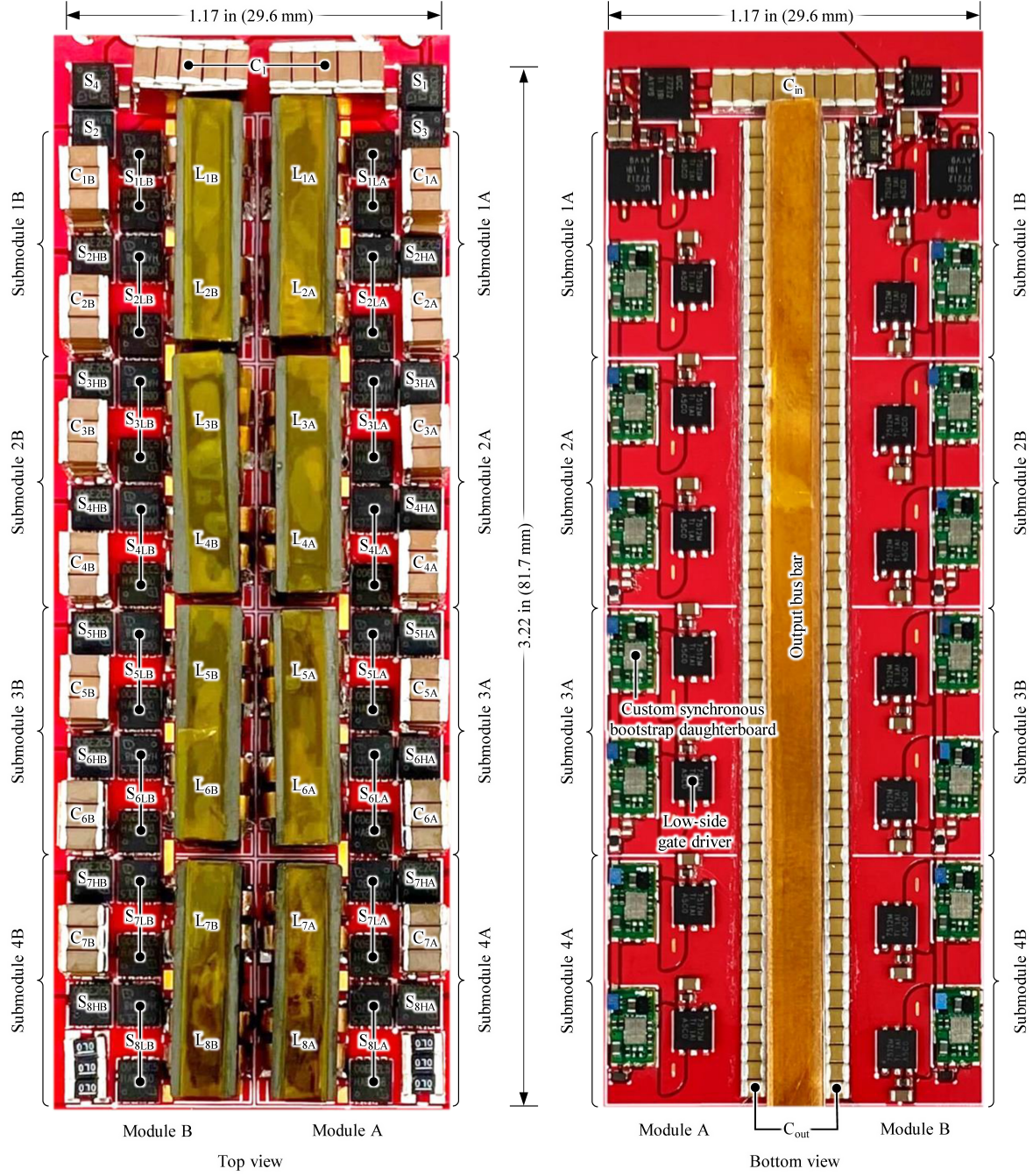


Figure 7.9: Photograph of the hardware prototype. Dimensions: $3.22 \times 1.17 \times 0.29 \text{ in}^3$ ($81.7 \times 29.6 \times 7.3 \text{ mm}^3$).

Table 7.1: Component list of the hardware prototype

Component	Part number	Parameters
MOSFET S_{1-4}	Infineon IQE013N04LM6CG	40 V, 1.35 m Ω
MOSFET $S_{2HA/B-8HA/B}$	Infineon IQE006NE2LM5CG	25 V, 0.65 m Ω
MOSFET $S_{1LA/B-8LA/B}$	Infineon IQE006NE2LM5CG, IQE006NE2LM5	25 V, 0.65 m Ω (in parallel)
Flying capacitor C_1	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 μ F* $\times$ 30 (in parallel)
Flying capacitor $C_{1A/B-5A/B}$	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 μ F* $\times$ 9 (in parallel)
Flying capacitor $C_{6A/B, 7A/B}$	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μ F* $\times$ 9 (in parallel)
Coupled inductor $L_{1A/B-8A/B}$	Custom two-phase coupled inductor	See Table 7.2 for details
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 μ F* $\times$ 8 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μ F* $\times$ 108 (in parallel)
Low-side gate driver	Texas Instruments UCC27512	4-A peak source, 8-A peak sink
High-side gate driver in Stage 1	Texas Instruments UCC27212	4-A peak source, 4-A peak sink
High-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source, 5-A peak sink

* The capacitance listed in this table is the nominal value before dc derating.



Figure 7.10: (a) Side view of the hardware prototype. (b) Photograph of the gate drive circuitry, including the custom synchronous bootstrap daughterboards (dimensions: $5.8 \times 3.5 \times 1.0$ mm³) used to power the high-side switches.

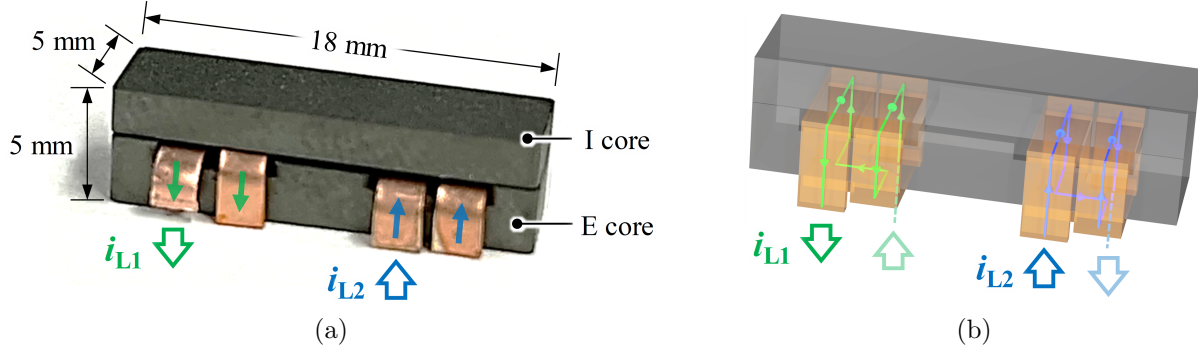


Figure 7.11: Custom two-phase coupled inductor. The two phases are negatively coupled. Each winding has two turns that are connected with a PCB trace beneath the E core. (a) Photograph with dimensions annotated. (b) 3D rendering with current paths annotated.

Table 7.2: Key parameters and operating conditions of the two-phase coupled inductor

Parameter	Value
Coupling coefficient	-0.8
Per-Phase steady-state inductance	606.5 nH
Per-Phase transient inductance	200 nH
Overall transient inductance	12.5 nH
Per-Phase dc resistance	0.48 m Ω
Per-Phase saturation current	40 A
Output voltage	1.0 V
Switching frequency	150 kHz
Nominal duty ratio	0.333
Per-Phase current ripple	7.33 A

where D is the duty ratio, V_{out} is the output voltage, and f_{sw} is the switching frequency. In this design, the nominal duty ratio is $D = \frac{1}{3}$, $V_{\text{out}} = 1.0$ V, $f_{\text{sw}} = 150$ kHz, and $\Delta i_{L,\text{pp}(\text{max})} = 7.8$ A. Therefore, $L_{\text{ss}(\text{min})} = 570$ nH. In addition, the height of the coupled inductor was constrained to 5 mm to align with the thickness of the three-layer stacked flying capacitors.

Considering the ripple requirement and height constraint, the two-phase coupled inductor presented in Fig. 7.11 was designed. It consists of an E core, an I core, and two windings. Each winding has two turns. The selection of the number of turns can be approached as an integer programming problem. The objective is to minimize the core volume while satisfying the requirements on steady-state inductance, dc resistance of the windings, and saturation current. A lower number of turns contributes to a reduction in the dc resistance and an increase in saturation current. However, it diminishes the steady-state inductance at the same time. Conversely, increasing the number of turns can facilitate achieving the target

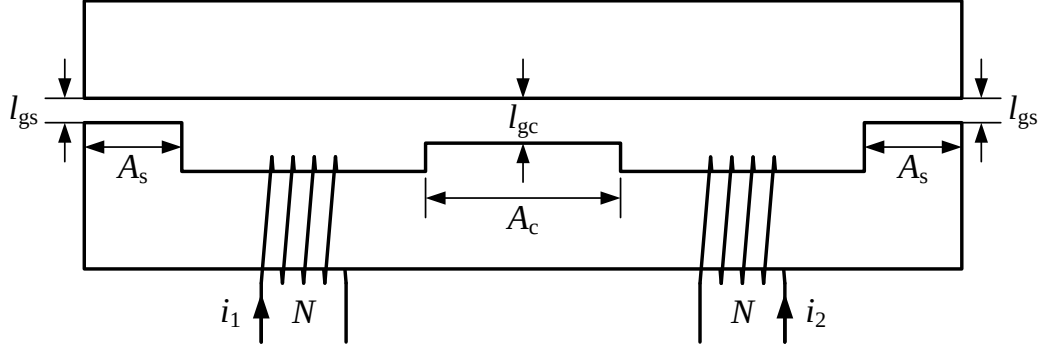


Figure 7.12: Core geometry of the two-phase coupled inductor. l_{gs} and l_{gc} are the lengths of the air gap in the side legs and the center leg, respectively. A_s and A_c are the cross-sectional areas of the side legs and the center leg, respectively. The currents in the two windings are i_1 and i_2 , respectively. Each winding has N turns. In this design, $N = 2$.

saturation current but at the cost of increased dc resistance and reduced saturation current. Two turns per winding provided the optimal solution for this prototype, as it achieved a good trade-off among the steady-state inductance, the dc resistance of the windings, and the saturation current.

7.2.1.1 Magnetic Circuit Model

Fig. 7.12 illustrates the core geometry of the two-phase coupled inductor, with its magnetic circuit model shown in Fig. 7.13. Since the initial relative permeability of the core material (DMR96A [91]) is $\mu_r = 3300$ which is much greater than 1, it is assumed that the magnetic reluctances of the air gap are much higher than those of the cores. Therefore, the reluctances of the side legs and the center leg are dominated by the air-gap reluctances and can be approximated as

$$\mathcal{R}_s = \frac{l_{gs}}{\mu_0 A_s} \quad (7.22)$$

$$\mathcal{R}_c = \frac{l_{gc}}{\mu_0 A_c} \quad (7.23)$$

where μ_0 is the permeability of vacuum, l_{gs} and l_{gc} are the lengths of the air gap in the side legs and the center leg, respectively, and A_s and A_c are the cross-sectional areas of the side legs and the center leg, respectively. In this design, $l_{gs} = 0.0254$ mm (1 mil), $l_{gc} = 0.3054$ mm, $A_s = 10$ mm², and $A_c = 20$ mm². Therefore, the side-leg and center-leg reluctances are $\mathcal{R}_s = 2.02 \times 10^6$ H⁻¹ and $\mathcal{R}_c = 1.22 \times 10^7$ H⁻¹, respectively.

Based on this magnetic circuit model, the self and mutual inductances of the coupled

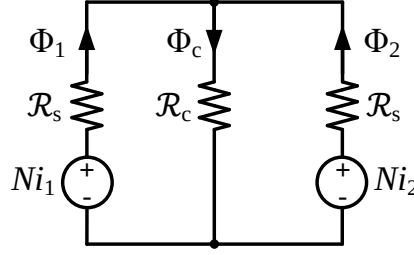


Figure 7.13: Magnetic circuit model of the two-phase coupled inductor. $\mathcal{R}_s$ and $\mathcal{R}_c$ are the magnetic reluctances of the side legs and the center leg, respectively. Ni_1 and Ni_2 are the magnetomotive forces (MMFs) applied by the two windings around the cores. Φ_1 , Φ_2 , and Φ_c are the magnetic fluxes in the side legs and the center leg.

inductor can be obtained as

$$L = \frac{N^2 (\mathcal{R}_s + \mathcal{R}_c)}{\mathcal{R}_s (\mathcal{R}_s + 2\mathcal{R}_c)} \quad (7.24)$$

$$M = -\frac{N^2 \mathcal{R}_c}{\mathcal{R}_s (\mathcal{R}_s + 2\mathcal{R}_c)} \quad (7.25)$$

which yields $L = 1066$ nH and $M = -914$ nH.

7.2.1.2 Simulation Results

Fig. 7.14 shows the self and mutual inductances of the two-phase coupled inductor obtained from Ansys FEM simulation. It can be seen that the self and mutual inductances at 0-A per-phase average current are $L = 1040$ nH and $M = -840$ nH, which align well with the values calculated from the magnetic circuit model. It is reasonable that the calculated values are slightly higher than the simulated values since the core reluctances are ignored in the model. The steady-state inductance can be calculated as

$$L_{ss} = \frac{L^2 - M^2}{L + \frac{D}{D'} M} \quad (7.26)$$

which yields $L_{ss} = 606$ nH. Since $L_{ss} > L_{ss(\min)} = 570$ nH, this design can satisfy the current ripple requirement. In addition, it can also be observed from Fig. 7.14 that the inductances drop sharply when the per-phase average current is above 40 A which is the designed saturation current of this coupled inductor.

Fig. 7.15 illustrates the current waveforms of the coupled inductor at a per-phase average current of 40 A (the designed saturation current). The magnetic cores are most prone to saturation when the current in one phase reaches its peak value. At this moment, the sum of and the difference between the two currents simultaneously reach their peaks, thereby maximizing the magnitude of flux density in the cores. Fig. 7.16 shows the magnitude of

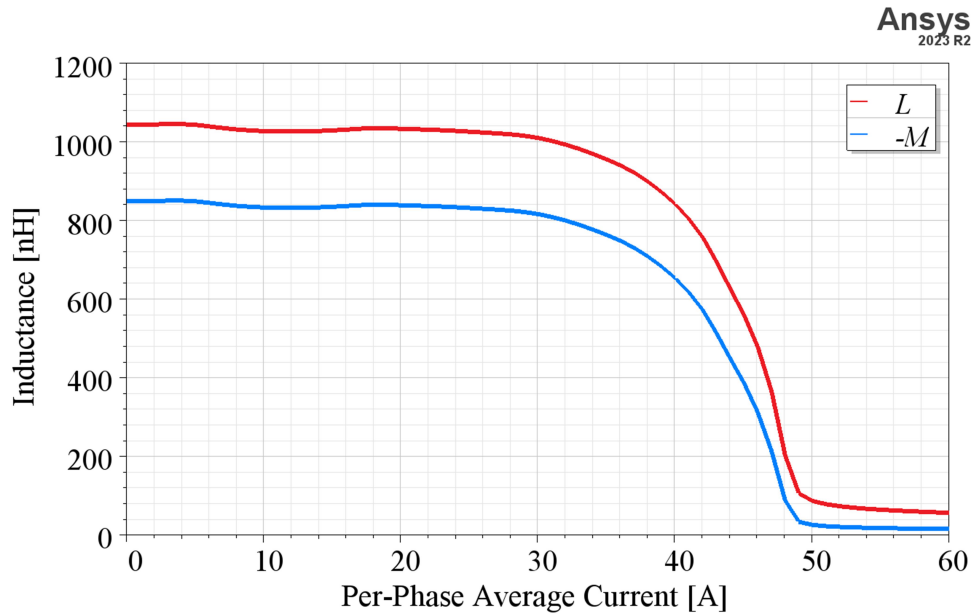


Figure 7.14: Self and mutual inductances of the two-phase coupled inductor obtained from Ansys FEM simulation.

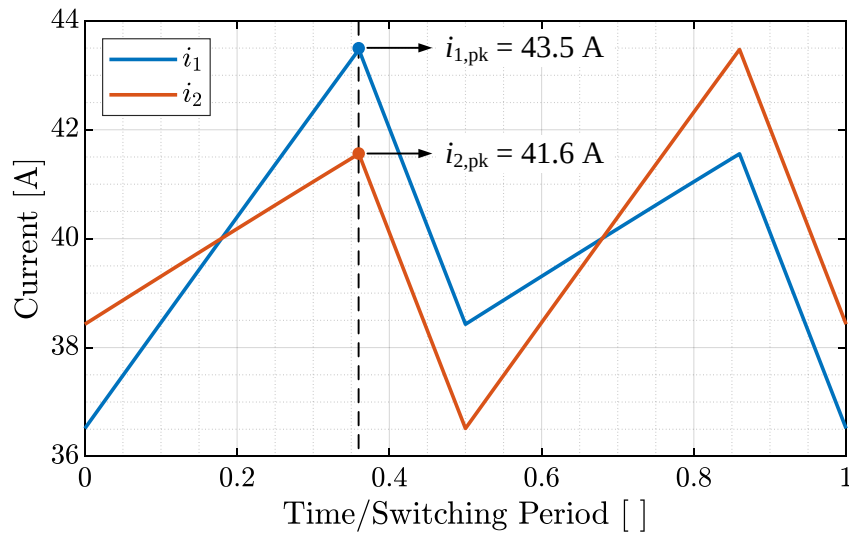


Figure 7.15: Current waveforms of the coupled inductor at a per-phase average current of 40 A (the designed saturation current). The waveforms were obtained from circuit simulation with $L = 1040$ nH and $M = -840$ nH. The magnetic cores are most prone to saturation when the current in one phase reaches its peak value, as annotated with the dashed line. The corresponding winding currents are $i_{1,pk} = 43.5$ A and $i_{2,pk} = 41.6$ A.

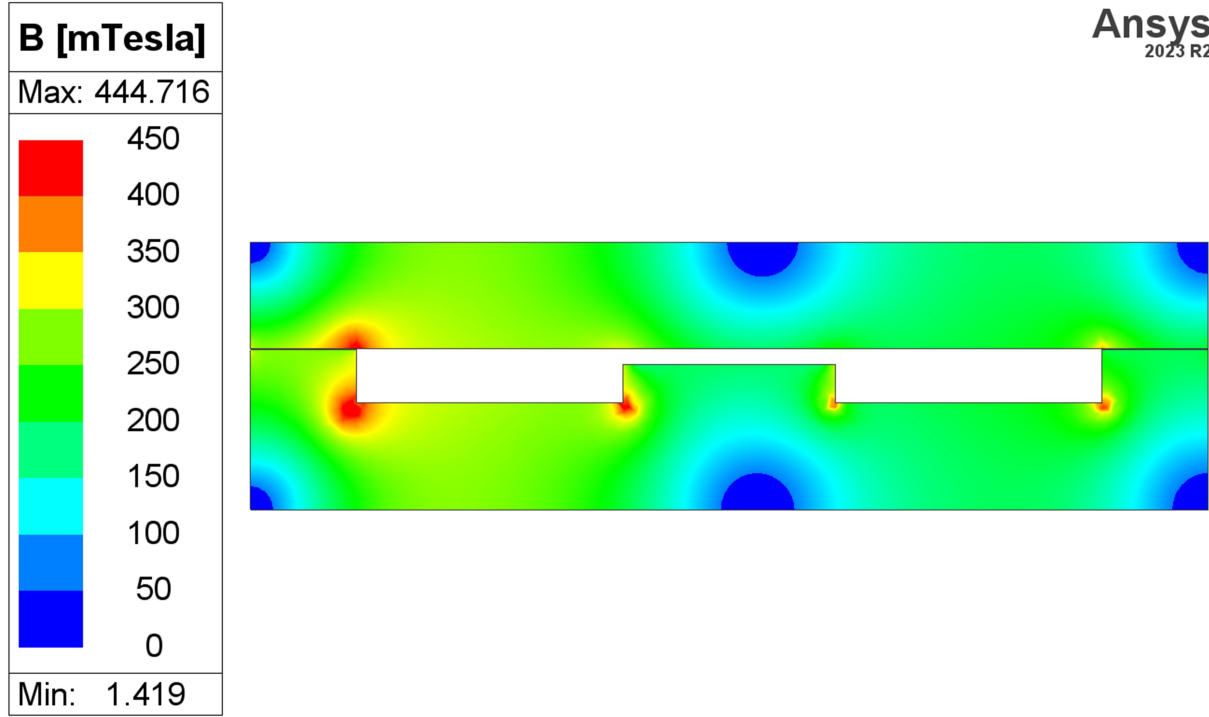


Figure 7.16: Magnitude of flux density on the cross-section of the cores at a per-phase average current of 40 A (the designed saturation current). In this FEM simulation, the current in the left-hand side winding is 43.5 A and the current in the right-hand side winding is 41.6 A.

flux density on the cross-section of the cores at this moment, where $i_{1,\text{pk}} = 43.5$ A and $i_{2,\text{pk}} = 41.6$ A. The saturation magnetic flux density of the core material (DMR96A) at 100 °C is 430 mT. As can be observed in Fig. 7.16, only a small portion of the magnetic cores saturate. This demonstrates that the coupled inductor is able to handle the target saturation current of 40 A.

7.2.2 Gate Drive Circuitry Design for High-Side Switches

One practical challenge of the hardware implementation is the gate drive circuitry for the high-side switches in Stage 2 (i.e., $S_{2\text{HA/B-8HA/B}}$). Due to the large number of high-side switches, conventional cascaded bootstrapping [41] illustrated in Fig. 7.17(a) suffers from accumulative voltage drops across bootstrap diodes, leading to considerable gate drive loss.

To address this challenge, this work adopts the synchronous bootstrap technique [92] illustrated in Fig. 7.17(b), with a synchronous bootstrap daughterboard customized for this demonstration, as shown in Fig. 7.10(b). By replacing bootstrap diodes with active FETs, the voltage drops in the bootstrap circuit can be greatly reduced, thus improving the gate

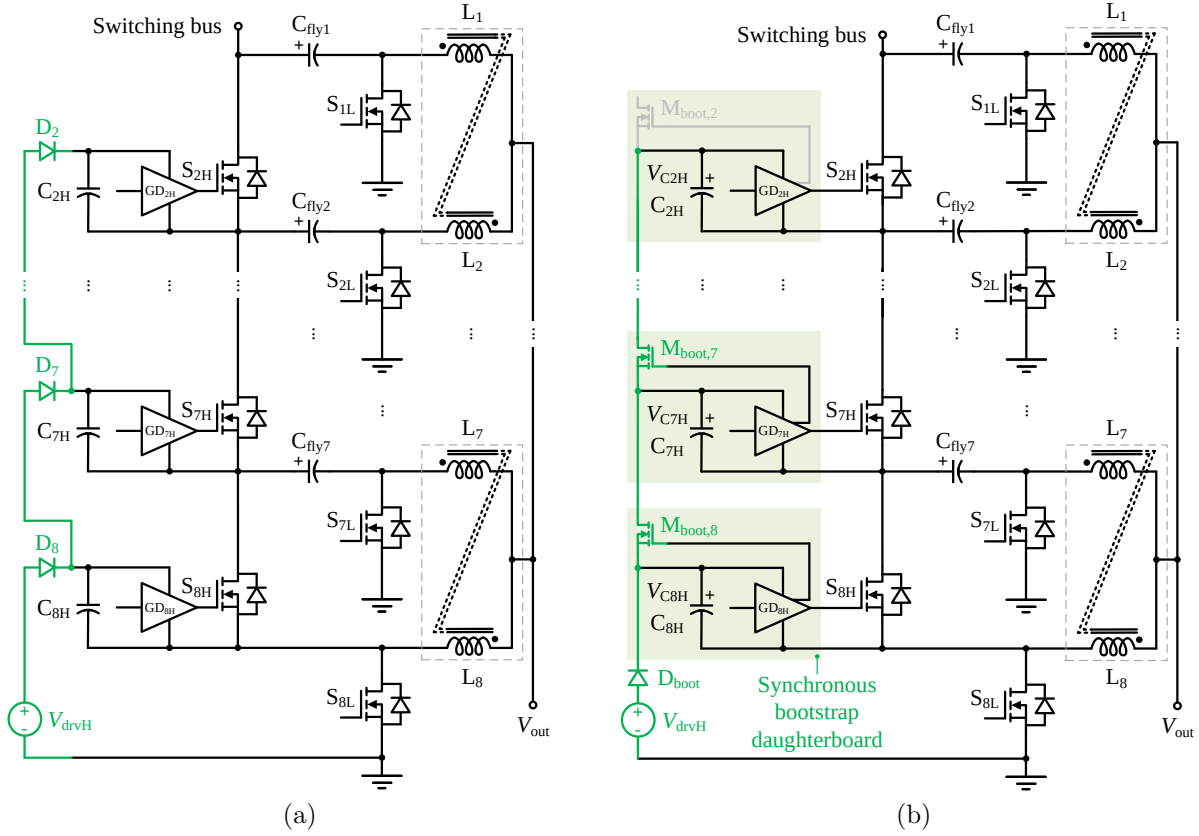


Figure 7.17: Comparison between two gate drive techniques for the high-side switches in Modules A and B. (a) Conventional cascaded bootstrapping that suffers from accumulative voltage drops across bootstrap diodes. (b) Synchronous bootstrapping that replaces bootstrap diodes with active FETs [92].

drive efficiency. Experimental results in Fig. 7.18 show that the total voltage drop in the bootstrap circuit across seven daughterboards is only 0.7 V, which is typically the voltage drop across one bootstrap diode in the conventional cascaded bootstrap circuit.

In Stage 1, the gate-driven charge pump circuit [41] is used to power high-side switches S_1 and S_2 . S_3 is powered by cascaded bootstrapping through a single diode.

7.2.3 Commutation Loop Optimization

Another implementation challenge is the commutation loop optimization. Large commutation loop inductance can be detrimental in multiple ways, including large voltage spikes during switching transitions that can cause device over-voltage, increased overlap loss if the switching transition has to be slowed (e.g., with larger the gate resistance) to mitigate the

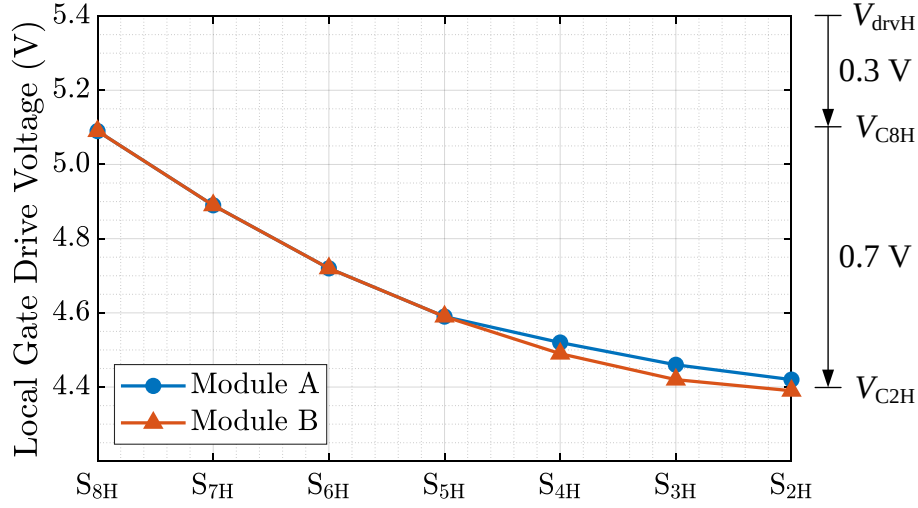


Figure 7.18: Measured local gate drive voltages of Modules A and B in the hardware prototype. The high-side gate drive supply voltage (V_{drvH} in Fig. 7.17(b)) is 5.4 V. The voltage drop across the bootstrap diode (D_{boot} in Fig. 7.17(b)) is roughly 0.3 V. The total voltage drop across the seven daughterboards is only 0.7 V.

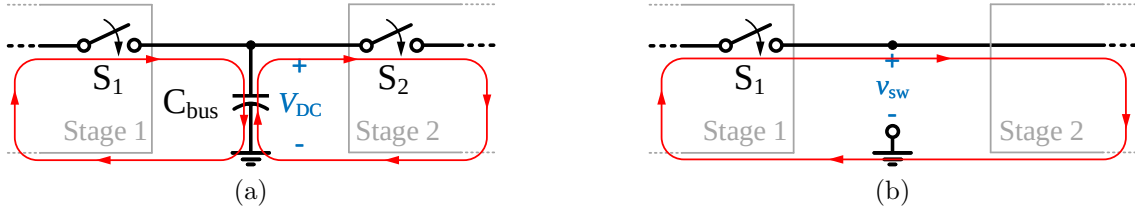


Figure 7.19: Illustration of the commutation loops in (a) the dc-bus-based architecture and (b) the switching-bus-based architecture.

voltage spike, increased parasitic inductance loss, and high-frequency ringing which leads to electromagnetic interference (EMI) [93–95].

As illustrated in Fig. 7.19(a), in the dc-bus-based architecture, the commutation loops in the two stages can be decoupled through the bus capacitor C_{bus} . However, in the switching-bus-based architecture, the two small commutation loops in Fig. 7.19(a) merge into one large loop through the switching bus, as illustrated in Fig. 7.19(b).

Fig. 7.20(a) shows the original PCB layout of Stage 1 and Submodules 1A and 1B that directly follows the schematic drawing in Fig. 7.1, which leads to a large commutation loop (highlighted in blue) with a parasitic inductance of 2.75 nH (obtained through Ansys FEM simulation). To reduce the size of the commutation loop, we swapped the positions of Submodule 1A plus S_3 and Submodule 1B plus S_2 , split the flying capacitor bank C_1 into

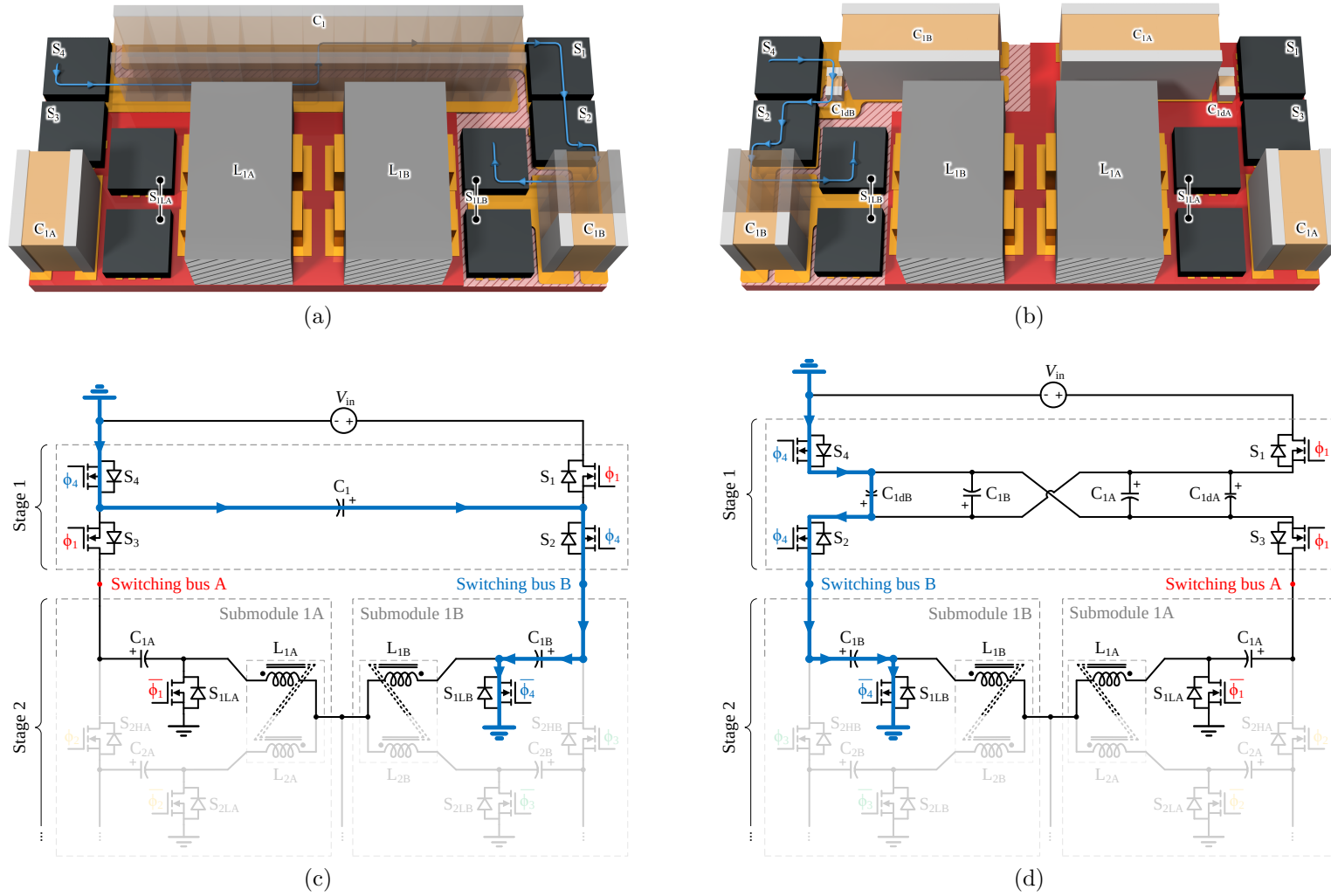


Figure 7.20: (a) Original PCB layout of Stage 1 and Submodules 1A and 1B that directly follows the schematic drawing in Fig. 7.1, leading to a large commutation loop (highlighted in blue) with a parasitic inductance of 2.75 nH (obtained through Ansys FEM simulation). (b) Improved PCB layout with Submodule 1A plus S_3 and Submodule 1B plus S_2 swapped, the flying capacitor bank C_1 split, and two small decoupling capacitors C_{1dB} and C_{1dA} added that dramatically reduces the size of the commutation loop (highlighted in blue) with a parasitic inductance of 1.76 nH (obtained through Ansys FEM simulation), demonstrating a reduction in parasitic inductance approximately by half. (c) Schematic drawing of the original PCB layout with the commutation loop highlighted in blue. (d) Schematic drawing of the improved PCB layout with the commutation loop highlighted in blue.

Table 7.3: Key parameters and test conditions

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	1.0 V
Full-load output current	500 A
Per-phase average inductor current at full load	31.25 A
Switching frequency	150 kHz
Gate drive voltage of Stage 1	8.0 V
High-side gate drive voltage of Stage 2	5.4 V
Low-side gate drive voltage of Stage 2	5.0 V
Prototype box volume*	1.08 in ³
Power component volume [†]	0.331 in ³

* The box volume is defined as the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry.

[†] The power components included in the volume calculation are switching devices, flying capacitors, and buck inductors.

C_{1A} and C_{1B} , and added two small decoupling capacitors C_{1dA} and C_{1dB} , as demonstrated in Fig. 7.20(b). It can be seen that this improvement dramatically shrinks the commutation loop, reducing its parasitic inductance by one-third from 2.75 nH to 1.76 nH. The schematic drawings of the original and improved PCB layout are shown in Figs. 7.20(c) and (d), with the commutation loop highlighted in blue.

7.3 Experimental Results and Analysis

Table 7.3 lists the key parameters and test conditions of the hardware prototype presented in Section 7.2. A TDK-Lambda GEN 60-85-3P480 60-V dc power supply was used to provide the 48-V input voltage, and a Chroma 63203 600-A dc electronic load was used to sink the output current. A Yokogawa WT3000E precision power analyzer was used to measure the input voltage, input current, and output voltage, and the dc electronic load measured the output current.

7.3.1 Experimental Waveforms

Fig. 7.21 shows the simulation and experimental waveforms of the switching bus voltages v_{swA} and v_{swB} . As shown in Figs. 7.21(a) and (b), at no load, the bus voltages switch between two different levels (21 V and 24 V), as has been explained in Section 7.1 and illustrated in Fig. 7.2. At full load, the flying capacitor voltage ripples are superimposed on the switching bus voltage waveforms. As shown in Figs. 7.21(c) and (d), the experimental waveforms are in good agreement with the simulation waveforms. Fig. 7.22 presents the simulation

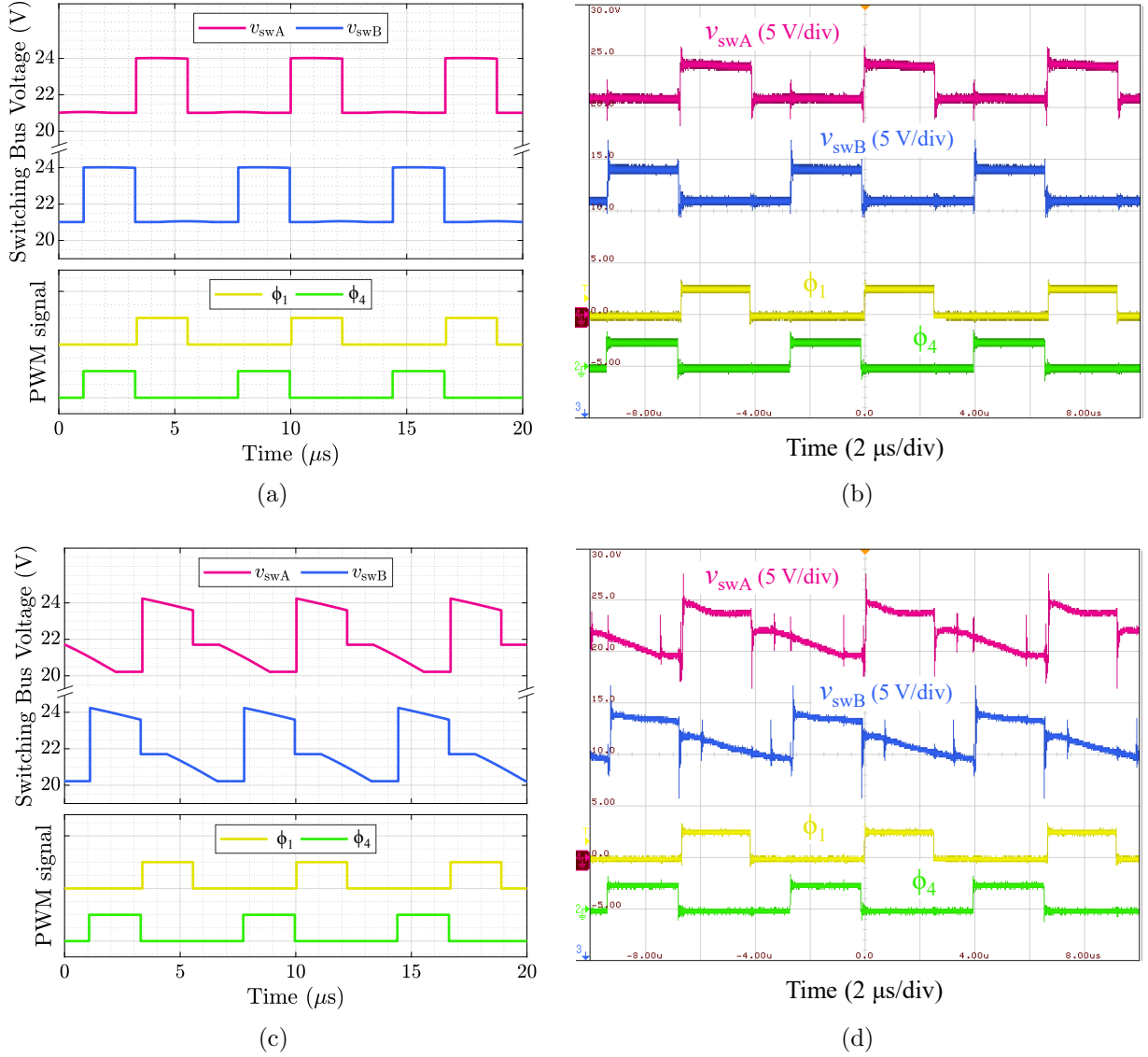


Figure 7.21: Waveforms of switching bus voltages v_{swA} and v_{swB} . (a) Simulation waveforms at no load. (b) Experimental waveforms at no load. (c) Simulation waveforms at full load. (d) Experimental waveforms at full load.

and experimental waveforms of flying capacitor voltages C_1 and C_{1B} - C_{7B} . As can be seen, the measured flying capacitor voltages are naturally balanced and in excellent agreement with the simulation waveforms. Moreover, the smooth and continuous capacitor voltage waveforms confirm the complete soft-charging operation of all flying capacitors.

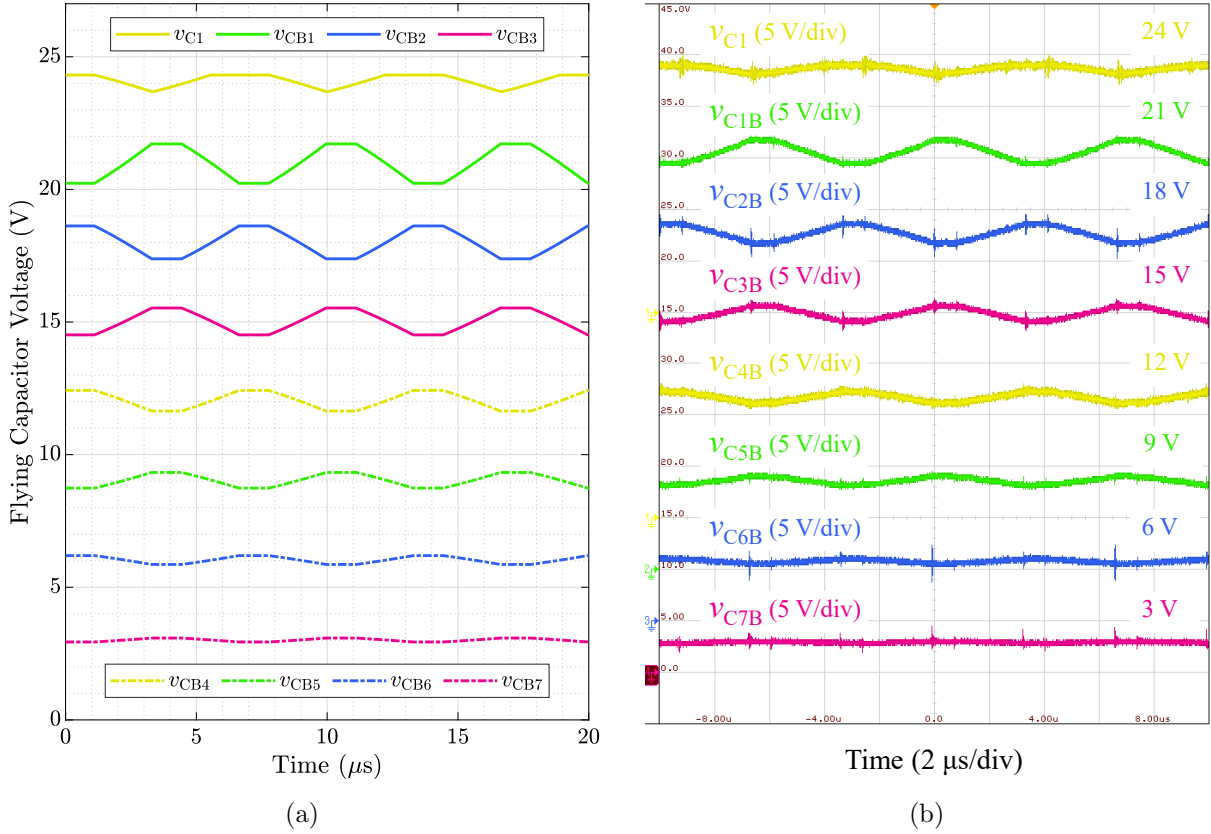


Figure 7.22: Waveforms of flying capacitor voltages v_{C1} and v_{CB1} – v_{CB7} . (a) Simulation waveforms at full load. (b) Experimental waveforms at full load.

7.3.2 Measured Performance and Loss Analysis

The proposed converter was tested up to 500-A output current at 1.0-V output voltage, achieving a power density of 464 W/in³ by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry). Fig. 7.23 shows the thermal image of the prototype running continuously at full load with fan cooling only. As can be observed in the thermal image, the distributed switch and capacitor network inherently facilitates heat dissipation, and the vertically-stacked flying capacitors function as natural heat sinks, which mitigates the hot-spot cooling challenges and enables easier thermal management. It should be noted that custom heat sinks can be added to the MOSFETs for better thermal performance without increasing the box volume since there is currently 4 mm of unused space above the MOSFETs.

Fig. 7.24 presents the measured efficiency of the hardware prototype. It achieved 94.7% peak power stage efficiency at 104-A output current and 86.4% full-load power stage efficiency at 500-A output current. With the gate drive loss included, it achieved 93.4% peak system

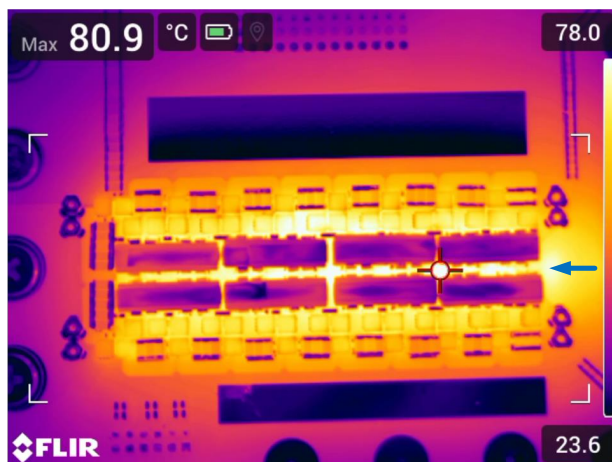


Figure 7.23: Full-load thermal image at thermal equilibrium with fan cooling only ($V_{in} = 48$ V, $V_{out} = 1.0$ V, $I_{out} = 500$ A). The blue arrow on the right-hand side indicates the direction of airflow.

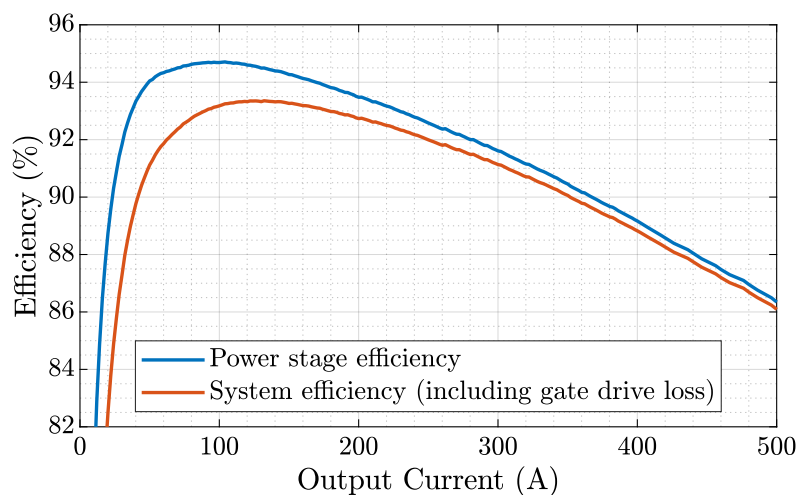


Figure 7.24: Measured 48-to-1-V efficiency. Peak efficiency: 94.7% at $I_{out} = 104$ A (93.4% at $I_{out} = 132$ A including gate drive loss). Full-load efficiency: 86.4% (86.1% including gate drive loss) at $I_{out} = 500$ A.

efficiency at 132-A output current and 86.1% full-load system efficiency at 500-A output current.

In order to gain deeper insights into the origins of power loss in the prototype and to identify potential avenues for performance improvement, a comprehensive loss breakdown was conducted at both the peak system efficiency point and full-load point, as shown in Fig. 7.25. The frequency-dependent losses (i.e., MOSFET switching loss, body-diode con-

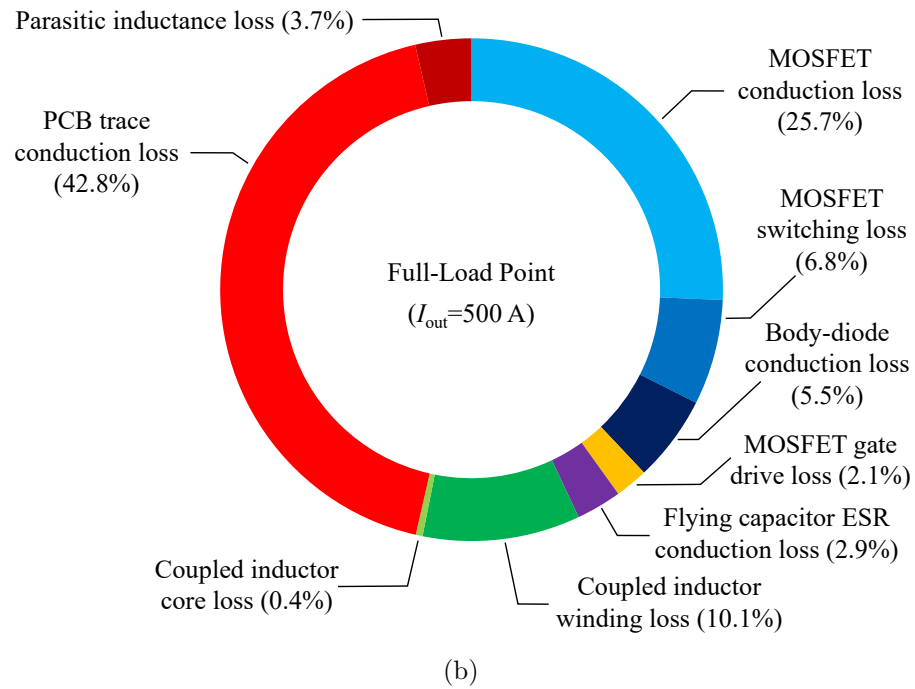
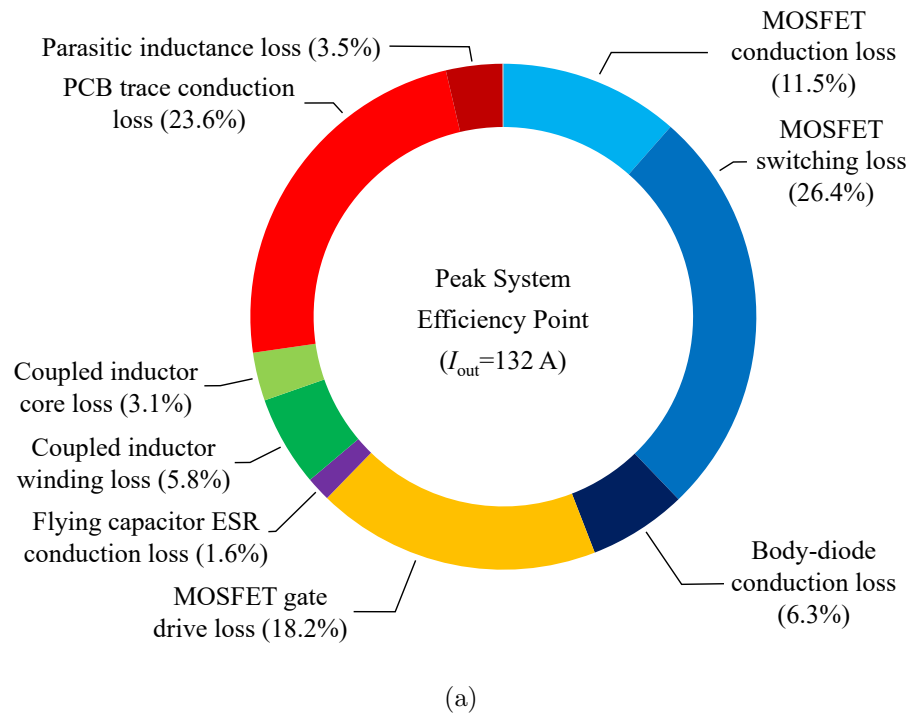


Figure 7.25: Loss breakdown of the hardware prototype. (a) Loss breakdown at the peak system efficiency point. (b) Loss breakdown at the full-load point.

duction loss, MOSFET gate drive loss, coupled inductor core loss, and parasitic inductance loss) represent a large portion of the total loss at the peak system efficiency point, while the conduction losses (i.e., MOSFET conduction loss, flying capacitor ESR conduction loss, coupled inductor winding loss, and PCB trace conduction loss) are dominant at the full-load point. The PCB trace conduction loss accounts for roughly a quarter of the total loss at the peak system efficiency point and nearly half of the total loss at the full-load point. In future work, the PCB trace conduction loss can be reduced with thicker copper layers or a more compact PCB layout enabled by higher switching frequency.

7.3.3 Comparison of Measured Performance at Different SC Stage Conversion Ratios

As revealed in the comparative analysis in Section 7.1.5, for regulated hybrid SC topologies, a larger SC stage conversion ratio is favorable for achieving higher performance. To experimentally verify this conclusion, this subsection compares and analyzes the performance of the hardware prototype measured at different SC stage conversion ratios.

Due to the good modularity of the hardware prototype presented in Section 7.2, the converter can be easily reconfigured for different SC stage conversion ratios. The SC stage conversion ratio of the configuration shown in Figs. 7.1 and 7.9 is 16-to-1, which comes from the multiplication of the 2-to-1 SC conversion ratio of Stage 1 and the 8-to-1 SC conversion ratio of Stage 2. By removing Submodules 4A and 4B and short-circuiting flying capacitors C_{6A} and C_{6B} , Stage 2 can be reconfigured to have a 6-to-1 SC conversion ratio, making the SC stage conversion ratio of the prototype 12-to-1. Similarly, an 8-to-1 SC stage conversion ratio can be achieved with Submodules 3A, 3B, 4A and 4B removed and flying capacitors C_{4A} and C_{4B} short-circuited. The gate drive circuitry is designed to be reconfigurable as well.

Fig. 7.26 shows the measured efficiency at different SC stage conversion ratios (K_{SC}), with the operating conditions and key performance listed in Table 7.4. In all configurations, the switching frequency was adjusted to maintain the same per-phase inductor current ripple ratio, defined as the ratio of the peak ripple amplitude to the average value of the inductor current. To facilitate a fair full-load efficiency comparison, all three configurations were designed to achieve the same power density.

As can be observed in Fig. 7.26 and Table 7.4, with a larger SC stage conversion ratio, the hardware prototype achieved both higher peak efficiency and higher full-load efficiency, which experimentally verifies the theoretical benefits revealed in the comparative analysis in Section 7.1.5. In theory, as shown in Figs. 7.6 and 7.7, the performance of the converter can be improved by further increasing the SC stage conversion ratio from 16-to-1 to 20-to-1 (maximum allowable SC stage conversion ratio for 48-V-to-1-V conversion as explained in Section 7.1.6), with one additional submodule added to each of the SCB modules. One major benefit of a larger SC stage conversion ratio is the switch voltage stress reduction. In practice, however, although the peak blocking voltages of the high-side switches $S_{1HA/B-8HA/B}$

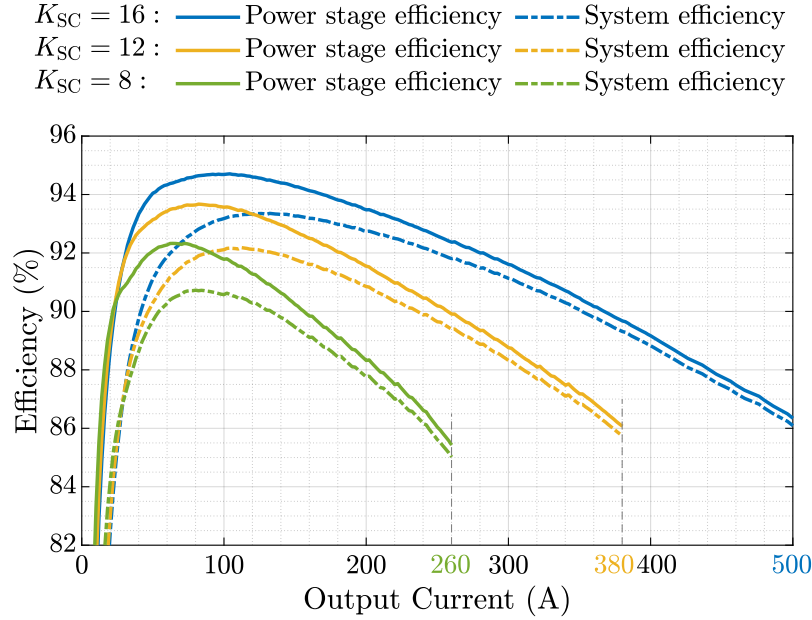


Figure 7.26: Measured 48-to-1-V efficiency at different SC stage conversion ratios (K_{SC}).

and the low-side switches $S_{1LA/B}$ – $S_{8LA/B}$ are 6 V and 3 V, respectively, with a 16-to-1 SC stage conversion ratio and 48-V input voltage, the best-performance switching devices (Infineon IQE006NE2LM5CG and IQE006NE2LM5) available on the market for this application are rated at 25 V. Given that the switching devices are overrated, the theoretical potential of the 20-to-1 configuration cannot be fully realized. This is why the hardware prototype presented in this chapter adopts a SC stage conversion ratio of 16-to-1. To fully realized the theoretical potential of the proposed switching bus topology, lower voltage devices with better figure-of-merit are needed.

7.3.4 Performance Comparison with the State of the Art

Table 7.5 compares the performance of this work (16-to-1 SBC) to that of the state-of-the-art 48-V-to-1-V academic works in previous literature, demonstrating the high efficiency and high power density of this work. It is worth noting that the 20-to-1 switching bus converter (SBC) is an extension of this work with a larger SC stage conversion ratio that achieves excellent performance.

Table 7.6 shows a performance comparison between this work (16-to-1 SBC) and existing 48-V-to-1-V commercial products. It can be seen that this preliminary laboratory prototype achieves outstanding efficiency and power density, even when compared to highly optimized commercial power modules with advanced packaging.

In the switching bus converter, the conversion burden on the buck stage can be alleviated

Table 7.4: Comparison of measured performance at different SC stage conversion ratios (K_{SC})

K_{SC}	16	12	8
Nominal duty ratio	0.333	0.25	0.167
Switching frequency*	150 kHz	200 kHz	250 kHz
Per-phase inductor current ripple ratio*	12%	12%	12%
Overall output current at full load	500 A	380 A	260 A
Power density [†]	464 W/in ³	464 W/in ³	464 W/in ³
Peak power stage efficiency	94.7% (at 104 A)	93.7% (at 82 A)	92.3% (at 64 A)
Full-load power stage efficiency	86.3%	86.1%	85.4%
Peak system efficiency	93.4% (at 132 A)	92.2% (at 112 A)	90.7% (at 80 A)
Full-load system efficiency	86.1%	85.7%	85.0%

* In all configurations, the switching frequency was adjusted to maintain the same per-phase inductor current ripple ratio, defined as the ratio of the peak ripple amplitude to the average value of the inductor current.

[†] To facilitate a fair full-load efficiency comparison, all three configurations were designed to achieve the same power density.

by increasing the SC stage conversion ratio, which enables inductor volume reduction. This means that the target power density can be achieved with a lower switching frequency, contributing to lower switching losses and higher efficiency.

7.4 Chapter Summary

This chapter presents a switching bus converter for direct 48-V-to-PoL power conversion in data centers. In the proposed topology, a 2-to-1 SC front-end is merged with two 8-branch SCB modules through two switching buses, achieving a SC stage conversion ratio of 16-to-1. Compared to the existing dc-bus-based architecture, the proposed switching-bus-based architecture does not require dc bus capacitors, reduces the number of switches, and ensures complete soft-charging operation.

Through a comparative analysis based on the normalized switch stress and the normalized passive component volume, this chapter reveals that a regulated hybrid SC topology with a larger SC stage conversion ratio has the potential to achieve both higher efficiency and higher power density, which is experimentally verified with measured performance at different SC stage conversion ratios. In order to achieve a larger SC stage conversion ratio, this work (16-to-1 SBC) modifies the control scheme of the SCB modules from multi-phase to two-phase operation, which extends the maximum duty ratio and allows for more SCB branches.

Table 7.5: Performance comparison between this work (16-to-1 SBC) and the state-of-the-art 48-V-to-1-V academic works

Year	Reference	Output Current	Operating Frequency*	Power Density**	Power Stage Efficiency	System Efficiency†
2023	This work (16-to-1 SBC)	500 A (31.3 A/phase)	150 kHz	464 W/in ³ (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2023	20-to-1 SBC [96] (extension of this work)	1200 A (30 A/phase)	200 kHz	607 W/in ³ (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 87.9%	92.4% 87.5%
2023	MSC [97]	450 A (28.1 A/phase)	400 kHz	621 W/in ³ (by box volume)	Peak efficiency: 93.1% Full-load efficiency: 86.2%	91.7% 85.8%
2023	Mini-LEGO [98]	240 A (20 A/phase)	1.5 MHz	1390 W/in ³ (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2022	SDIH [82]	105 A (52.5 A/phase)	750 kHz	598 W/in ³ (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2022	Dickson ² [75]	270 A (30 A/phase)	280 kHz	360 W/in ³ (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [77]	450 A (28.1 A/phase)	417 kHz	232 W/in ³ (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [76]	60 A (30 A/phase)	250 kHz	263 W/in ³ (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	LEGO [83]	450 A (37.5 A/phase)	1 MHz	294 W/in ³ (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [70]	40 A (20 A/phase)	125 kHz	150 W/in ³ (by power component volume)	Peak efficiency: 95.1% [‡] Full-load efficiency: 92.7% [‡]	N/A N/A
2020	Sigma [99]	80 A	1 MHz	420 W/in ³ (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

* Switching frequency of the voltage regulation stage.

** The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.

† Gate drive loss is included in the calculation of system efficiency.

[‡]According to direct correspondence with the author.

Table 7.6: Performance comparison between this work (16-to-1 SBC) and existing 48-V-to-1-V commercial products

Release Year	Reference	Output Current	Operating frequency*	Power Density**	System Efficiency [†]
2023	This work (16-to-1 SBC)	500 A	150 kHz	464 W/in ³	Peak: 93.4%, Full-load: 86.1%
2021	ADI LTM4664 [100]	50 A	350 kHz	415 W/in ³	Peak: 90.8%, Full-load: 88.0%
2018	Bel Power Solutions ST4-1V0M07G [101]	70 A	450 kHz	167 W/in ³	Peak: 91.5%, Full-load: 90.5%
2016	TI LMG5200POLEVM-10 [102]	50 A	600 kHz	N/A	Peak: 90.7%, Full-load: 87.6%
2012 2015	Vicor PRM48AF480T400A00 [103] +2×VTM48EF012T130C01 [104] [‡]	200 A	1.03 MHz 1.20 MHz	236 W/in ³	Total efficiency: 89.7% [‡]

* Switching frequency of the voltage regulation stage.

**Power density calculated by the box volume.

[†] Gate drive loss is included in the calculation of system efficiency.
System Designer.

[‡]Recommended and provided by Vicor's online Power System Designer.

In order to validate the theoretical potential of the proposed topology, we designed and built a modular hardware prototype with custom two-phase coupled inductors. The synchronous bootstrap technique, implemented on custom daughterboards, was used to overcome the accumulative voltage drops seen when using conventional cascaded bootstrapping diodes. Additionally, the PCB layout was optimized for smaller commutation loops along the switching buses.

The hardware prototype was tested up to 500-A output current at 1-V output voltage, achieving 93.4% peak system efficiency, 86.1% full-load system efficiency (including gate drive loss), and 464-W/in³ power density (by box volume). Compared to state-of-the-art 48-V-to-1-V academic works and commercial products, this switching bus converter prototype achieved both excellent efficiency and power density. The performance of this hardware prototype demonstrates the great potential of the switching-bus-based architecture and underscores the benefits of a larger SC stage conversion ratio.

Chapter 8

A 1500-A/48-V-to-1-V Switching Bus Converter for Next-Generation Ultra-High-Power Processors

8.1 Motivation for Vertical Power Delivery

To address the challenges of 48 V to point-of-load (PoL) power conversion mentioned in Section 1.3, multiple solutions have been proposed in previous literature for 48-V-to-PoL power conversion in data centers, including transformer-based solutions [99, 105–109] and hybrid switched-capacitor (SC) solutions [64, 65, 70, 75–77, 81–83, 97, 110–115]. Relying on highly optimized LLC converters [116], transformer-based solutions can achieve high performance with integrated magnetics and planar matrix transformers which leverages flux cancellation [117]. Although galvanic isolation is achievable in transformer-based topologies, it is typically not necessary for 48-V-to-PoL applications [118]. As an emerging family of topologies, hybrid SC converters can leverage both the greatly superior energy density of capacitors compared to magnetic components [86, 88] and the better figure-of-merit (FOM) of low-voltage switching devices compared to high-voltage devices [4].

Both transformer-based and hybrid SC solutions can be developed with either a two-stage architecture [77, 83, 106, 107, 111, 112, 114] or a single-stage architecture [64, 65, 70, 75, 76, 81, 82, 97, 99, 108–110, 113, 115, 119]. In the two-stage architecture, the 48-V bus voltage needs to be first stepped down to a lower dc bus voltage (e.g., 12/8/6 V) with a fixed-ratio intermediate bus converter (IBC) such as LLC converters [106, 107, 117] and resonant SC converters [62, 120–122], and then regulated down to 1 V at the point-of-load (PoL) with multi-phase VRMs. In the single-stage architecture, as its name suggests, the 48-V bus voltage is directly regulated down to 1 V within one conversion stage without an intermediate dc bus.

In pursuit of a more efficient and compact alternative to the existing two-stage lateral power delivery (LPD) solution shown in Fig. 1.4, this chapter proposes an ultra-high-current

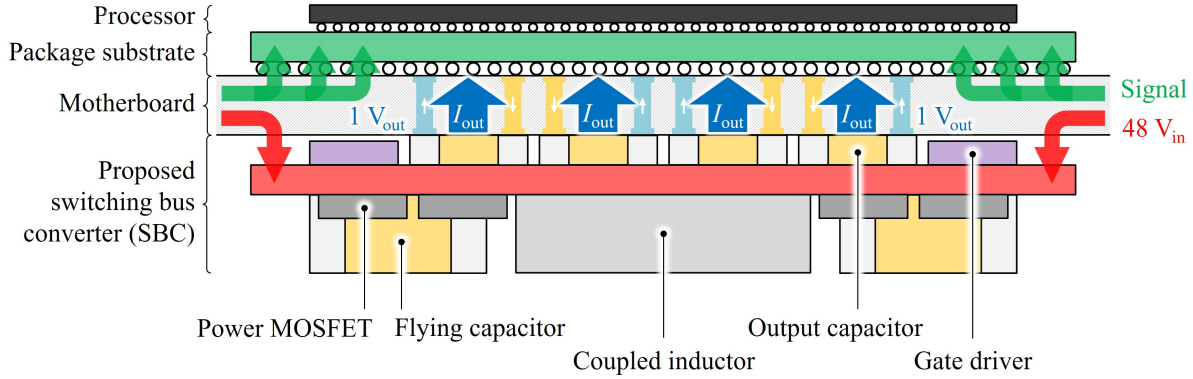


Figure 8.1: Single-stage vertical power delivery (VPD) architecture for next-generation ultra-high-power processors with the proposed 48-V-to-1-V switching bus converter (SBC). In this VPD solution, the SBC on the bottom side of the motherboard can vertically deliver an ultra-high current to the processor on the top side through vias, which can greatly reduce the PDN size and PDN losses.

48-V-to-1-V hybrid SC voltage regulator, named the switching bus converter (SBC), to address the aforementioned challenges through single-stage vertical power delivery (VPD), as illustrated in Fig. 8.1. In this single-stage VPD solution, the proposed SBC is placed on the bottom side of the motherboard directly underneath the processor so that it can deliver the ultra-high current vertically to the top side through vias, which greatly reduces the PDN size and PDN losses and saves the valuable topside area on the motherboard for high-speed communication and memories. Moreover, merging two conversion stages into one single stage reduces power conversion losses and eliminates the need for dc bus capacitors, which effectively improves overall system efficiency and power density.

More specifically, the proposed topology merges two 2-to-1 SC front-ends and four 10-branch series-capacitor-buck (SCB) modules through four switching buses. Revealed by a topological comparison, the proposed topology exhibits the theoretical potential of achieving both higher efficiency and higher power density than existing 48-V-to-1-V hybrid SC demonstrations. To validate its theoretical potential, a hardware prototype was built with custom four-phase coupled inductors and gate drive daughterboards and tested up to 1500 A of output current. The prototype achieved a peak system efficiency of 92.7%, a full-load system efficiency of 85.7%, and a power density of 759 W/in³ at 1500-A output current and 1-V output voltage. This article expands upon our earlier conference publications [96, 123] with additional explanations for the design and optimization of the four-phase coupled inductor, an in-depth loss analysis of the hardware prototype, as well as a more comprehensive performance comparison with the state-of-the-art academic and industry solutions.

The remainder of this chapter is organized as follows: First, Section 8.2 introduces the topology and operating principles of the proposed switching bus converter, explains the ad-

advantages of the proposed switching-bus-based architecture over the existing dc-bus-based architecture, and demonstrates the theoretical potential of the proposed topology through a topological comparison. Section 8.3 presents the 1500-A hardware prototype and discusses the key design considerations for the four-phase coupled inductor and the gate drive circuitry. Section 8.4 demonstrates measured performance, loss analysis, and performance comparison with state-of-the-art academic works and commercial products. Finally, Section 8.5 summarizes the contribution of this chapter.

8.2 Switching Bus Converter

8.2.1 Proposed Topology and Operating Principles

Fig. 8.2 shows the schematic drawing of the proposed switching bus converter, which merges two 2-to-1 SC front-ends (i.e., Stage 1) with four 10-branch series-capacitor-buck (SCB) modules (i.e., Modules A-D in Stage 2) through four intermediate buses (i.e., Switching buses A-D). As illustrated in the key waveforms and control signals in Fig. 8.3, the intermediate bus voltages v_{swA} - v_{swD} always switch between two voltage levels rather than being dc. Therefore, this type of intermediate bus interfacing two conversion stages is referred to as a *switching bus*, the concept of which was first introduced in [75]. It should be noted that although the SC front-ends and SCB modules are referred to as Stage 1 and Stage 2 in the schematic drawing to facilitate understanding, the proposed topology is still considered a single-stage architecture since there is no intermediate dc bus.

Each SCB module consists of five submodules and operates in a two-phase fashion with a 180° phase shift between neighboring branches. The control signals of Modules C and D are 90° phase shifted with respect to those of Modules A and B to ensure the four-phase symmetric interleaving of ϕ_{1A} , ϕ_{1C} , ϕ_{2A} , and ϕ_{2C} , and of ϕ_{1B} , ϕ_{1D} , ϕ_{2B} , and ϕ_{2D} , which enables the use of four-phase coupled inductors illustrated with the grey boxes. All flying capacitor voltages and inductor currents in the proposed topology are naturally balanced because of the negative feedback mechanism of the series-capacitor-buck (SCB) converter, as explained in [79] and [124]. The low-side switches $S_{1LX-10LX}$ ($X = A, B, C, D$) can operate with zero-voltage switching (ZVS) turn-ON, provided continuous forward inductor current and sufficient deadtime.

In existing dc-bus-based two-stage architectures [106, 107, 111, 112], a large dc bus capacitor is typically required to maintain a stiff dc bus voltage, which hinders converter miniaturization. In [77], the intermediate bus capacitance was reduced by allowing a significant ripple on the bus voltage. However, this led to the hard charging between the intermediate bus capacitor and flying capacitors, which induced additional charge-sharing losses. Similarly, in [83, 114], filter capacitors were required on the intermediate buses to filter the high-frequency pulsating current from the buck stage, which led to undesired hard-charging operation and additional charge-sharing losses. In contrast, the proposed switching-bus-based architecture allows the intermediate buses to switch between two voltage levels,

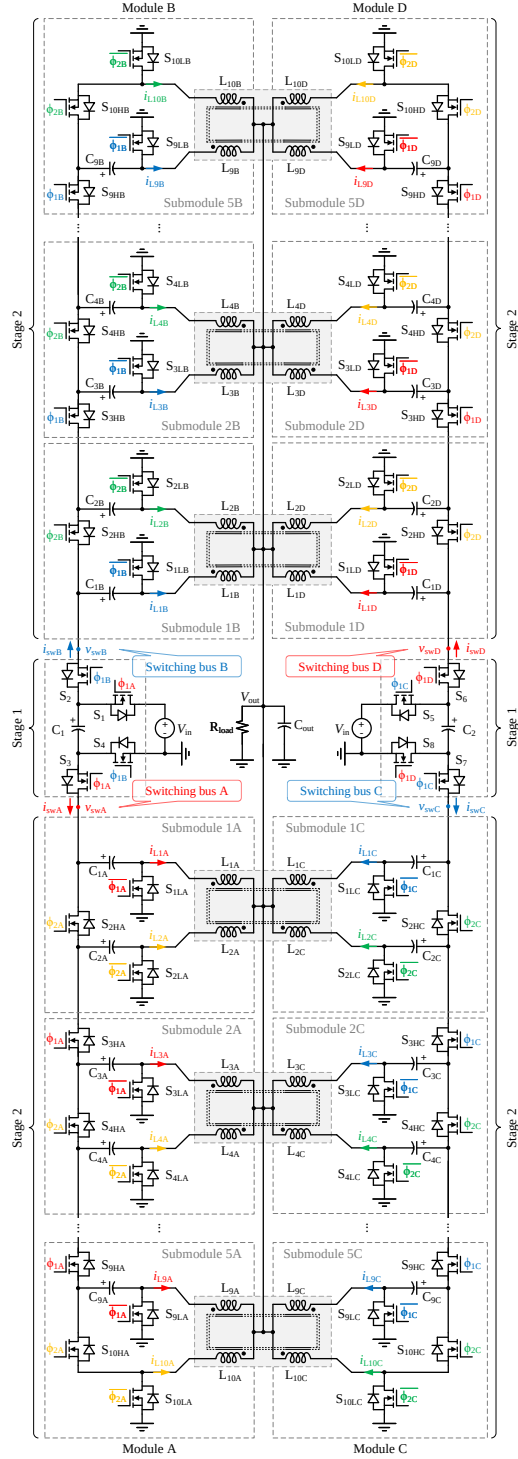


Figure 8.2: Schematic drawing of the proposed switching bus converter (SBC).

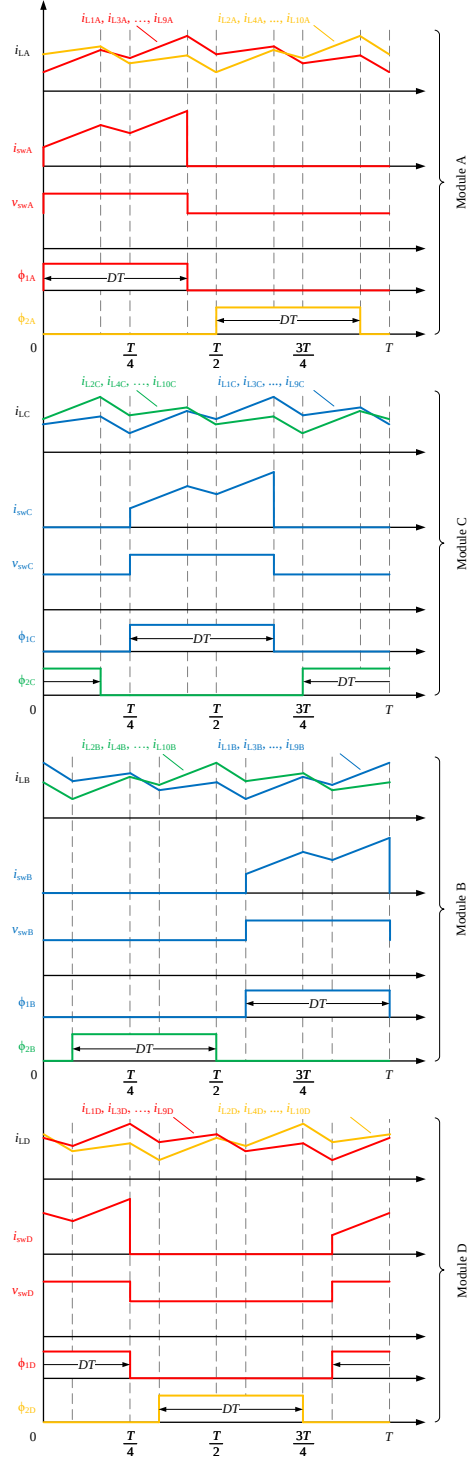


Figure 8.3: Key waveforms and control signals.

thus eliminating the need for intermediate bus capacitors, while guaranteeing complete soft-charging operation for all flying capacitors as well. In addition, the switching-bus-based architecture enables a reduction in the number of switches, since one redundant switch is removed on each switching bus while the two stages are merged.

It is worth noting that the switching bus concept can be generalized to enable the combination of different SC topologies. As a result, a family of regulated hybrid SC topologies can be generated. For example, the Dickson² converter [75], where the concept of a switching bus was first introduced, merges a 3-to-1 Dickson front-end and three 3-branch SCB modules through three switching buses. Other examples include the MLB converter [65] and the CaSP converter [64]. In addition to regulated hybrid SC topologies, the switching bus concept has also been adopted in fixed-ratio multi-resonant SC converters [84] for 48-V-to-12-V data center applications.

8.2.2 Topological Comparison

In this section, a topological comparison is performed to show the theoretical potential of the proposed topology compared to existing 48-V-to-1-V hybrid SC demonstrations. The topological comparison is based on two metrics: a) normalized switch stress as an indicator of efficiency and b) normalized passive component volume as an indicator of power density.

The normalized switch stress, denoted as M_S , is defined as the total switch volt-ampere (VA) stress normalized to the output power, expressed by the following equation:

$$M_S = \frac{\sum_{\text{switches}} V_{ds,i} I_{d(rms),i}}{V_{out} I_{out}}, \quad (8.1)$$

where $V_{ds,i}$ represents the peak blocking voltage across switch i assuming no capacitor voltage ripple, and $I_{d(rms),i}$ is the RMS value of the current through switch i assuming no inductor current ripple. The M_S value serves as an indicator of the VA stress experienced by the switches in a given topology when transferring one per-unit watt of power from input to output. A lower normalized switch stress is preferable because it indicates lower switching losses, lower conduction losses, and smaller switch sizes, which contribute to higher efficiency and higher power density.

The normalized passive component volume, denoted as M_P , can be assessed with an energy-based approach by analyzing the peak energy stored in each passive component [86, 87]. The M_P value reflects the overall volume of passive components required to meet given ripple requirements on inductor currents and flying capacitor voltages while transferring one per-unit watt of power from input to output. A smaller normalized passive component volume is preferred, as it indicates higher power density. Detailed derivations and analyses of the normalized passive component volume can be found in [85].

A topological comparison between this work and existing 48-V-to-1-V hybrid SC demonstrations is presented in Table 8.1 and visualized in Fig. 8.4. A regulated hybrid SC topology typically consists of a SC stage for fixed-ratio voltage step-down and a multi-phase buck-type

stage for the remainder of the voltage conversion task, output voltage regulation, and soft-charging operation [85]. A larger SC stage conversion ratio (K_{SC}) alleviates the conversion burden on the following buck-type stage and enables buck-type stage efficiency improvement and inductor size reduction. Due to the fact that inductors are much less energy dense compared to capacitors [1] and typically dominate the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden, which contributes to overall converter volume reduction and efficiency improvement. The proposed switching bus converter topology can be extended to different SC stage conversion ratios by changing the number of submodules in Stage 2. For 48-V-to-1-V conversion, the allowed SC stage conversion ratios are $K_{SC} = 4, 8, 12, 16, 20$. Given that a larger SC stage conversion ratio enables higher performance, this work adopts the maximum allowable SC stage conversion ratio $K_{SC(max)} = 20$. It is worth noting that such a large SC stage conversion ratio is enabled by the two-phase operation of the SCB modules and is not achievable with the conventional multi-phase operation [85].

As shown in Table 8.1 and Fig. 8.4, the proposed topology stands out as it achieves the lowest normalized switch stress and the smallest normalized passive component volume with the largest SC stage conversion ratio, indicating its great potential for both higher efficiency and higher power density compared to prior hybrid SC solutions.

8.3 Hardware Implementation and Design Considerations

This section introduces a 48-V-to-1-V hardware prototype designed and constructed to validate the functionality and performance of the proposed topology. Fig. 8.5 presents the photograph of the prototype, with the top view showing the power stage and the bottom view showing the gate drive circuitry. Fig. 8.6 annotates the submodules and main circuit components of the prototype, which shows its good modularity and extendibility. Table 8.2 lists the main circuit components.

To optimize the use of the prototype's box volume, all flying capacitors are stacked in two layers, aligning with the height of the coupled inductors. The stacked flying capacitors also function as effective natural heat sinks, as they are connected to power MOSFETs through thermally conductive PCB traces. Moreover, the distributed switch and capacitor network contribute to an inherent heat-spreading mechanism. The 2-mm thick PCB has 6 layers, with 6-oz copper on the two outer layers and 2-oz copper on the four inner layers.

8.3.1 Four-Phase Coupled Inductor

As introduced in Section 8.2.1, each group of the four inductors highlighted with grey boxes in Fig. 8.2 can be implemented as a four-phase coupled inductor. Compared to discrete inductors, coupled inductors can achieve faster transient response without sacrificing steady-state current ripple [125] and can achieve core volume reduction through dc flux cancellation [76].

Table 8.1: Topological comparison between this work and existing 48-V-to-1-V hybrid SC demonstrations

Year	Reference	SC Stage Conversion Ratio (K_{SC})	Buck Stage Conversion Ratio (K_{buck})	Buck Stage Duty Ratio (D)	Normalized Switch Stress (M_S)	Normalized Passive Component Volume (M_P)
2020	Crossed-coupled QSD buck [70]	4:1	12:1	0.083	24.2	2.08
2020	DIH [81]	6:1	8:1	0.125	14.7	2.40
2021	CaSP [64]	6:1	8:1	0.125	23.5	2.02
2022	LEGO [83]	6:1	8:1	0.125	17.6	2.41
2023	Mini-LEGO [114]					
2023	SDIH [82]	6:1	8:1	0.125	14.7	2.40
2022	MLB [76]	8:1	6:1	0.167	23.7	2.03
2022	VIB [77]	8:1	6:1	0.167	14.3	2.07
2023	MSC [97]	8:1	6:1	0.167	15.1	1.95
2022	Dickson ² [75]	9:1	5.33:1	0.188	14.8	1.90
2023	16-to-1 SBC [115]	16:1	3:1	0.333	10.2	1.69
2023	This work	20:1	2.4:1	0.417	8.99	1.56

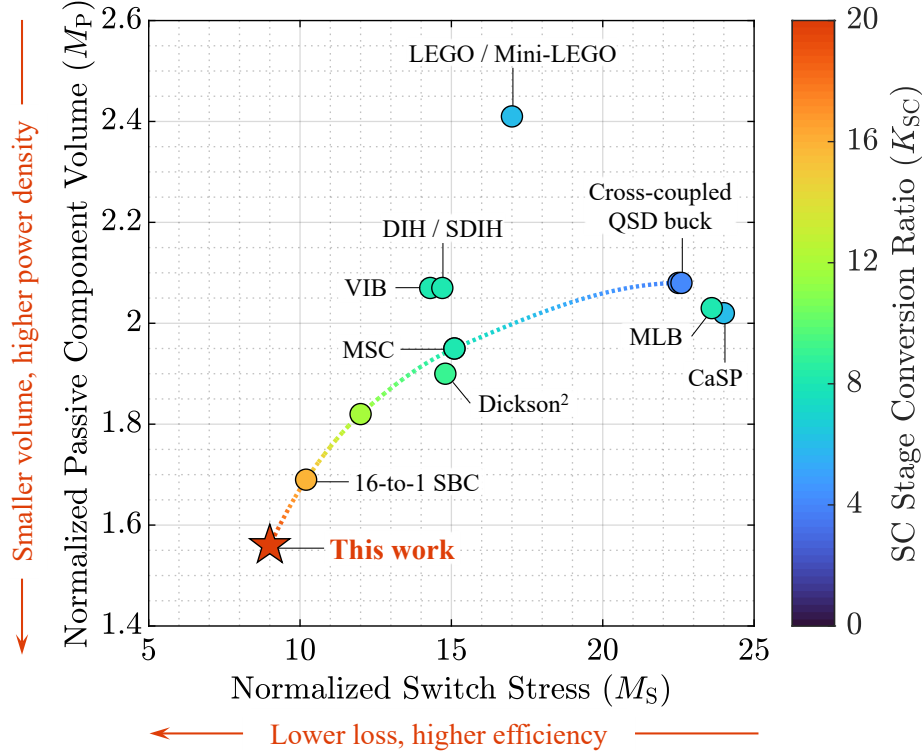


Figure 8.4: Normalized switch stress (M_S), normalized passive component volume (M_P) and SC stage conversion ratio (K_{SC}) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. A lower normalized switch stress is more desirable since it indicates lower losses and higher efficiency. A smaller normalized passive component volume is preferable, as it implies a smaller converter volume and higher power density. The proposed switching bus converter topology can be extended to different SC stage conversion ratios by changing the number of submodules in Stage 2, as illustrated with the dashed curve. Each dot on the dashed curve represents an implementation of the switching bus converter at a SC stage conversion ratio corresponding to its color.

In pursuit of high performance, a four-phase coupled inductor presented in Fig. 8.7 comprising two pieces of magnetic cores and four pieces of one-turn copper windings was customized for this hardware prototype. The magnetic cores were fabricated with DMEGC DMR96A Mn-Zn ferrite material [91]. To minimize conduction losses on the vertical output current path, each winding is connected to the output bus bar on the back of the PCB through plated through holes.

The subsequent part of this subsection details the key design considerations and optimizations of the four-phase coupled inductor. The per-phase steady-state inductance (L_{ss}) and transient inductance (L_{tr}) [126, 127] of a symmetric four-phase coupled inductor operating

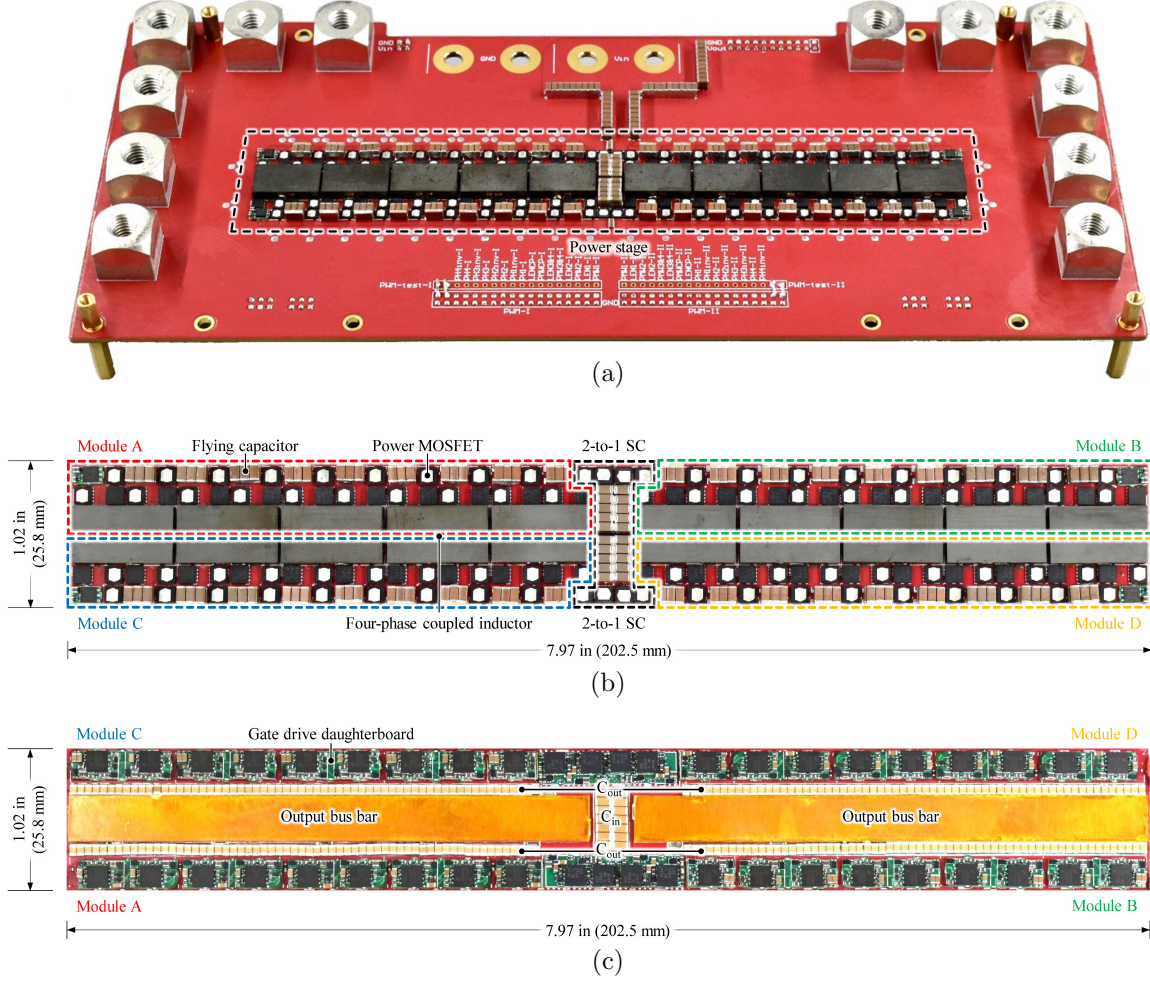


Figure 8.5: Photograph of the hardware prototype. Converter dimensions: $7.97 \times 1.02 \times 0.244$ in³ ($202.5 \times 25.8 \times 6.2$ mm³). (a) Complete view. (b) Top view showing the power stage. (c) Bottom view showing the gate drive circuitry.

at a duty ratio between 0.25 and 0.5 can be expressed as

$$L_{ss} = \frac{\left(1 - \frac{\alpha}{3}\right) (1 + \alpha)}{1 + \left(\frac{1}{D} + \frac{3}{D'} - 2\right) \frac{\alpha}{6}} L \quad (8.2)$$

$$L_{tr} = (1 + \alpha) L, \quad (8.3)$$

where D is the duty ratio, $D' = 1 - D$, L and M are the self and mutual inductances of the coupled inductor, and α is the coupling coefficient defined as

$$\alpha = \frac{3M}{L}. \quad (8.4)$$

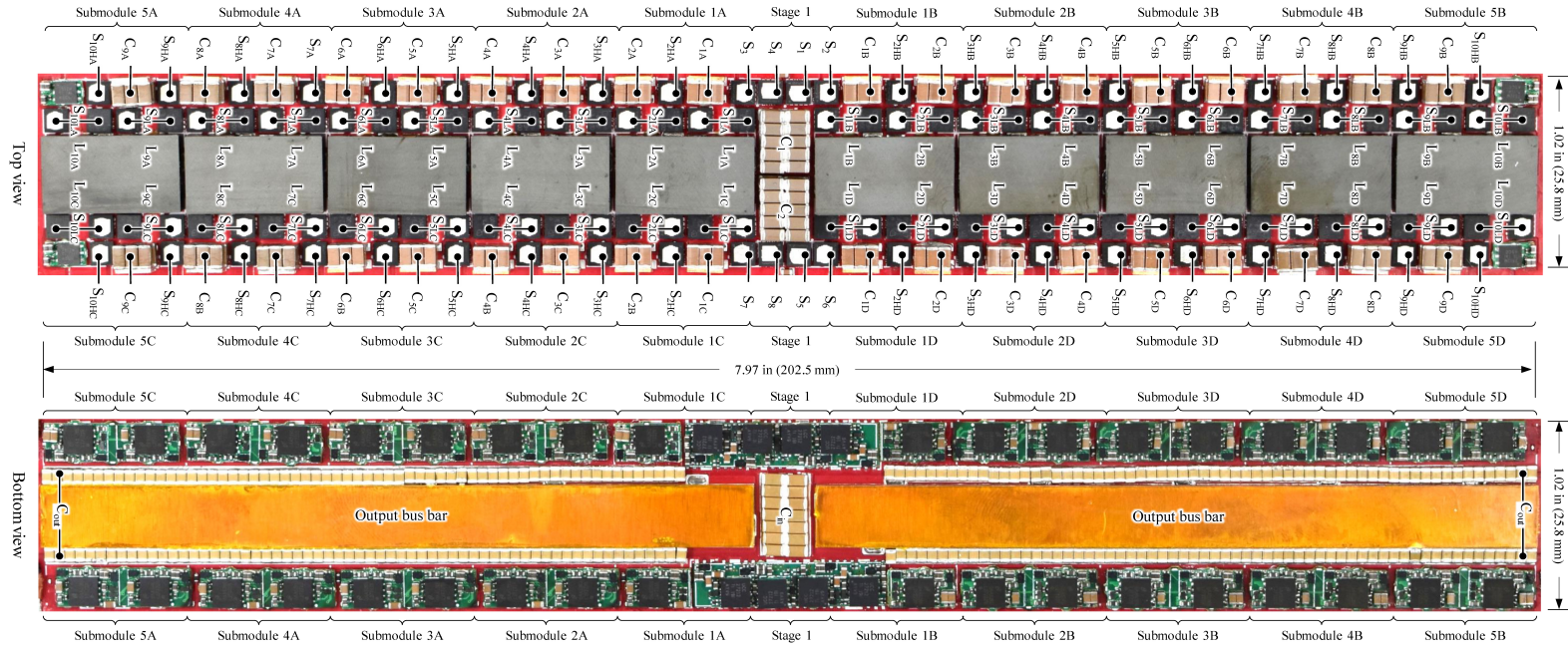


Figure 8.6: Submodules and key circuit components of the hardware prototype.

Table 8.2: Component list of the hardware prototype

Component (X = A, B, C, D)	Part number	Parameters
MOSFET S_{1-8}	Infineon IQE013N04LM6CGSC	40 V, 1.35 m Ω , dual-side cooling
MOSFET $S_{2HX-10HX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 m Ω , dual-side cooling
MOSFET $S_{1LX-10LX}$	Infineon IQE006NE2LM5CGSC	25 V, 0.58 m Ω , dual-side cooling
	Infineon IQE004NE1LM6	15 V, 0.45 m Ω
Flying capacitor $C_{1,2}$	TDK C3216X7R1H106K160AE	X7R, 50 V, 10 μ F* $\times$ 20 (in parallel)
Flying capacitor C_{1X-6X}	TDK C3216X6S1E226M160AC	X6S, 25 V, 22 μ F* $\times$ 6 (in parallel)
Flying capacitor C_{7X-9X}	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μ F* $\times$ 6 (in parallel)
Input capacitor C_{in}	KEMET C1206C224K1RECAUTO	X7R, 100 V, 0.22 μ F* $\times$ 14 (in parallel)
Output capacitor C_{out}	Murata GRM219R60J476ME44D	X5R, 6.3 V, 47 μ F* $\times$ 248 (in parallel)
Gate driver in Stage 1	Texas Instruments UCC27212	4-A peak source, 4-A peak sink
Low-side gate driver in Stage 2	Texas Instruments LMG1020	7-A peak source, 5-A peak sink
High-side gate driver in Stage 2	Texas Instruments LM27222	3-A peak source, 4.5-A peak sink

* The capacitance listed in this table is the nominal value before dc derating.

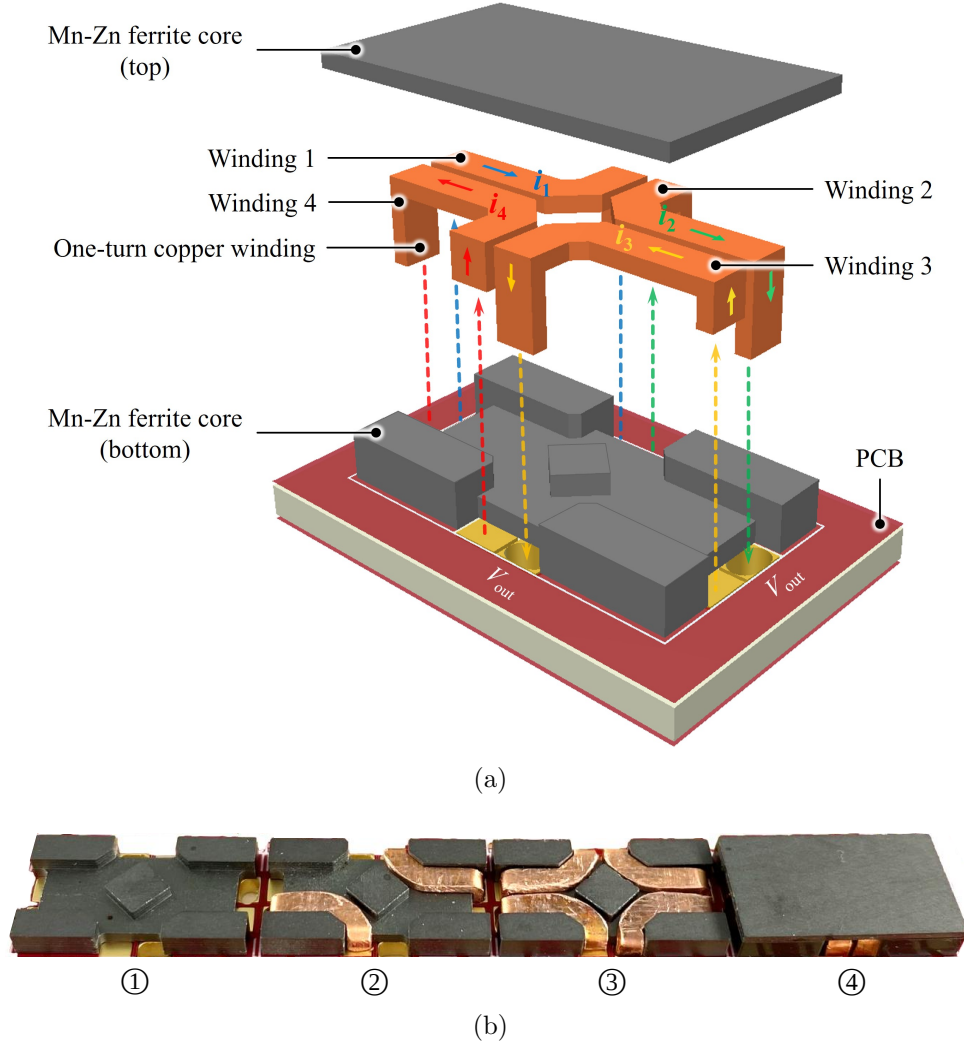


Figure 8.7: Custom four-phase coupled inductor. Dimensions: $18.5 \times 10.5 \times 3.2 \text{ mm}^3$. (a) 3D rendering of the coupled inductor with current paths annotated. Each winding is connected to the output bus bar on the back of the PCB through plated through holes in order to minimize conduction losses on the output current path for VPD. (b) Coupled inductor assembly with two pieces of Mn-Zn ferrite cores and four pieces of one-turn copper windings: ① → ② → ③ → ④ .

In this design, the four phases of the coupled inductor are negatively coupled to achieve dc flux cancellation, meaning that the mutual inductance (M) is negative, resulting in a negative coupling coefficient. In (8.4), the coupling coefficient (α) has been normalized and is a design variable that can vary between 0 and -1. A coupling coefficient closer to -1 indicates stronger magnetic coupling.

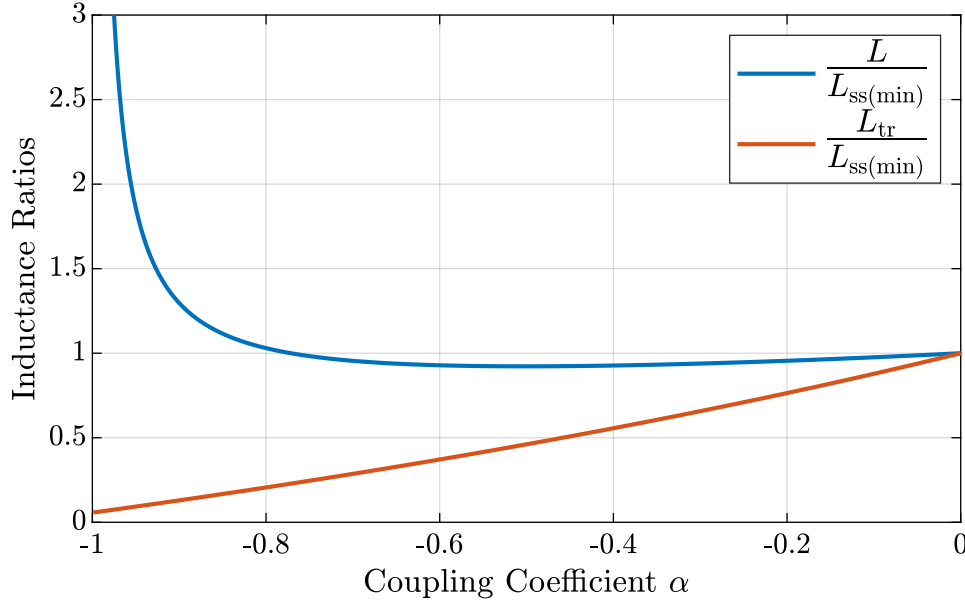


Figure 8.8: Ratios of the self and transient inductances to the steady-state inductance ($\frac{L}{L_{ss}}$ and $\frac{L_{tr}}{L_{ss}}$) as functions of the coupling coefficient (α) when the duty ratio (D) is 0.417. Magnetic coupling becomes stronger as α varies from 0 towards -1.

In practical design problems, the per-phase steady-state inductance (L_{ss}) of a coupled inductor needs to be greater than or equal to a minimum value ($L_{ss(\min)}$) in order to meet given current ripple requirements, i.e., to ensure the per-phase peak-to-peak current ripple does not exceed the specified upper limit $\Delta i_{L,pp(\max)}$. This minimum steady-state inductance value can be calculated as

$$L_{ss(\min)} = \frac{D'V_{out}}{f_{sw}\Delta i_{L,pp(\max)}}, \quad (8.5)$$

where f_{sw} is the switching frequency and V_{out} is the output voltage. Since $L_{ss(\min)}$ is a design target that needs to be satisfied, it is fixed in the following optimization procedure.

Fig. 8.8 shows the ratios of the self and transient inductances to the minimum steady-state inductance ($\frac{L}{L_{ss(\min)}}$ and $\frac{L_{tr}}{L_{ss(\min)}}$) when $D = 0.417$, which can be obtained from (8.2) and (8.3) as

$$\frac{L}{L_{ss(\min)}} = \frac{1 + \left(\frac{1}{D} + \frac{3}{D'} - 2\right) \frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3}\right) (1 + \alpha)} \quad (8.6)$$

$$\frac{L_{\text{tr}}}{L_{\text{ss}(\min)}} = \frac{1 + \left(\frac{1}{D} + \frac{3}{D'} - 2 \right) \frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3} \right)}. \quad (8.7)$$

As can be seen, the transient inductance (L_{tr}) always decreases with stronger coupling (i.e., with a coupling coefficient α closer to -1), which contributes to a faster transient response. However, with a coupling coefficient beyond -0.8, the self-inductance (L) required to maintain the minimum steady-state inductance ($L_{\text{ss}(\min)}$) increases dramatically. For a coupled inductor with a fixed length of air gap, a higher self-inductance typically requires a larger core volume. This implies that the self-inductance can serve as a proxy for the core volume in the optimization of gapped coupled inductors. Given $L_{\text{ss}(\min)}$, a coupled inductor design that requires a smaller self-inductance (L) is preferable, as it indicates a smaller core volume.

For a smaller core volume and a faster transient response, the self-inductance (L) and the transient inductance (L_{tr}) both need to be minimized. To strike a trade-off between these two conflicting objectives, a cost function is defined for this optimization problem as the geometric mean of L and L_{tr} :

$$f(\alpha, D) = \sqrt{LL_{\text{tr}}}, \quad (8.8)$$

which needs to be minimized. With (8.5)-(8.7) inserted, equation (8.8) can be rearranged as

$$f(\alpha, D) = \frac{D' + \left(\frac{D'}{D} + 3 - 2D' \right) \frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3} \right) \sqrt{1 + \alpha}} \cdot \frac{V_{\text{out}}}{f_{\text{sw}} \Delta i_{\text{L,pp}(\max)}}. \quad (8.9)$$

Since V_{out} , f_{sw} and $\Delta i_{\text{L,pp}(\max)}$ are fixed in each design, $f(\alpha, D)$ can be normalized by $\frac{V_{\text{out}}}{f_{\text{sw}} \Delta i_{\text{L,pp}(\max)}}$ as

$$\hat{f}(\alpha, D) = \frac{f(\alpha, D)}{\frac{V_{\text{out}}}{f_{\text{sw}} \Delta i_{\text{L,pp}(\max)}}} = \frac{D' + \left(\frac{D'}{D} + 3 - 2D' \right) \frac{\alpha}{6}}{\left(1 - \frac{\alpha}{3} \right) \sqrt{1 + \alpha}}. \quad (8.10)$$

It is worth noting that this normalized cost function ($\hat{f}(\alpha, D)$) is dimensionless and design-independent, which makes it widely applicable for the optimization of gapped coupled inductors. Apparently, minimizing $f(\alpha, D)$ is equivalent to minimizing $\hat{f}(\alpha, D)$.

The nominal duty ratio of the proposed topology for 48-V-to-1-V conversion is 0.417, and the maximum allowable duty ratio during transients is 0.5. To minimize the normalized cost function ($\hat{f}(\alpha, D)$) while ensuring that the peak-to-peak current ripple never exceeds

$\Delta i_{L,pp(max)}$ when the duty ratio (D) varies between 0.417 and 0.5, the optimum coupling coefficient (α_{opt}) can be obtained as

$$\alpha_{opt} = \underset{\alpha \in [-1,0]}{\operatorname{argmin}} \left(\underbrace{\max_{D \in [0.417, 0.5]} \hat{f}(\alpha, D)}_{\text{worst-case scenario for each } \alpha} \right). \quad (8.11)$$

Fig. 8.9 illustrates this optimization process by sweeping α and D within the range of interest, with the color and contour lines showing the value of $\hat{f}(\alpha, D)$. According to Fig. 8.9, the optimum coupling coefficient (α_{opt}) for this design is -0.92 , which minimizes $\hat{f}(\alpha, D)$ and thus minimizes $f(\alpha, D)$.

The four-phase coupled inductor illustrated in Fig. 8.7 was designed around this optimum coupling coefficient $\alpha_{opt} = -0.92$, with manufacturing tolerances taken into consideration. Table 8.3 summarizes key parameters and operating conditions of this four-phase coupled inductor.

The current handling capability of the designed four-phase coupled inductor is verified by circuit and finite element method (FEM) simulations using PLECS and Ansys, respectively. Fig. 8.10 shows the simulation waveforms of the four-phase interleaved winding currents at the full-load conditions listed in Table 8.3, with the directions of the winding currents illustrated in Fig. 8.7(a). As annotated in Fig. 8.10, the magnetic cores are most prone to saturation at Moments I–IV when the current in one phase reaches its peak value. Fig. 8.11 shows the Ansys FEM simulation results of the magnetic flux density distributions in the bottom core. Figs. 8.11(a) and (b) depict the surface and cross-sectional magnetic flux density distributions in the bottom core at Moment I. Since current i_1 reaches its peak at Moment I and is the highest among the four winding currents, the magnitude of the magnetic flux density around Winding 1, as annotated in Fig. 8.7(a), is the highest. The saturation magnetic flux density of the core material (DMR96A [91]) is 540 mT at 25 °C and 430 mT at 100 °C. As Figs. 8.11(a) and (b) show, only a small portion of the bottom core around Winding 1 saturates at Moment I. Similarly, Figs. 8.11(c) and (d) depict the magnetic flux density distributions at Moment II when i_2 reaches its peak, showing marginal saturation around Winding 2. Because of the symmetry of the core geometry, the magnetic flux density distributions at Moments III and IV, after being rotated by 180° around the center of the bottom core, are identical to those at Moments I and II. Therefore, the magnetic flux density distributions at Moments III and IV are omitted in Fig. 8.11. In summary, the FEM simulation results presented in Fig. 8.11 demonstrate that the four-phase coupled inductor is capable of handling the 37.5-A per-phase average current at the full-load conditions listed in Table 8.3.

8.3.2 Gate Drive Circuitry

One practical implementation challenge of the proposed topology is the gate drive circuitry for the high-side switches in the SCB modules in Stage 2 (i.e., $S_{2HX-10HX}$, $X = A, B, C, D$).

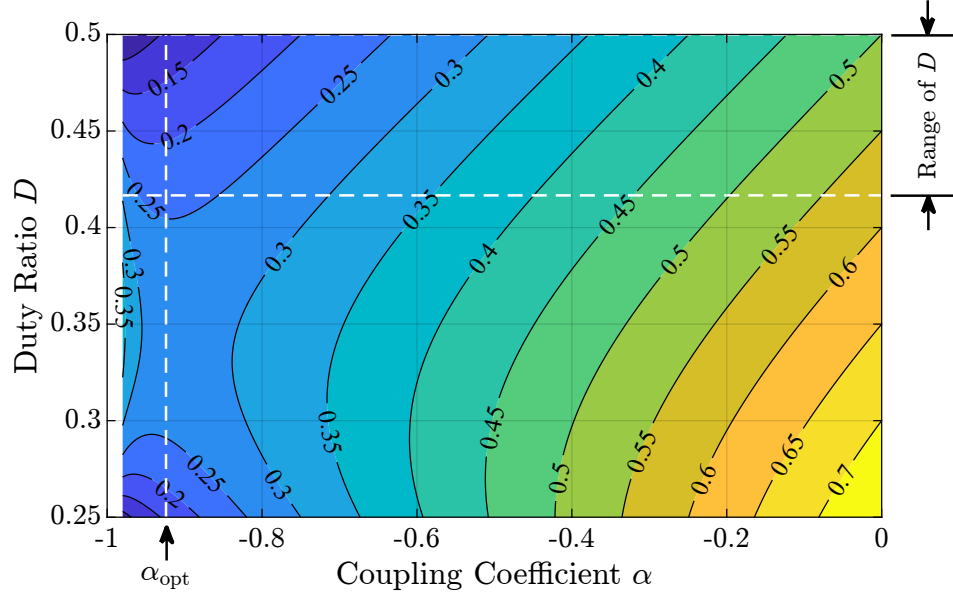


Figure 8.9: Optimization of the coupling coefficient (α) with a duty ratio (D) varying between 0.417 and 0.5. The color and contour lines of this figure show the value of the normalized cost function ($\hat{f}(\alpha, D)$) defined in (8.8).

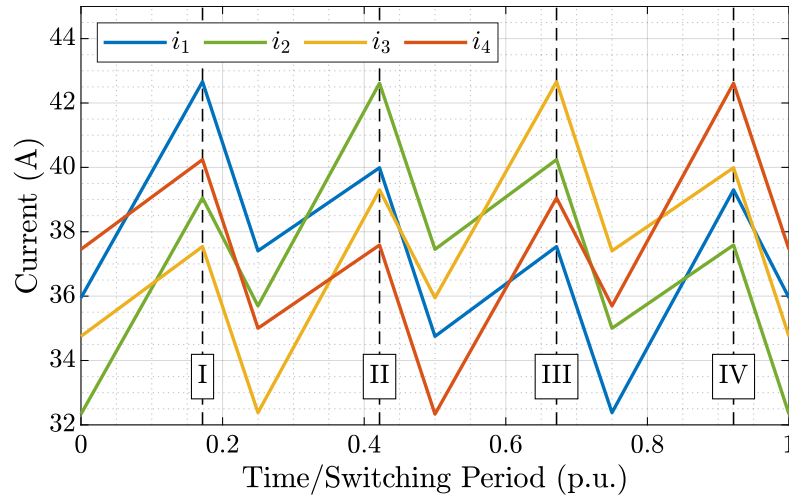


Figure 8.10: Simulation waveforms of winding currents for the four-phase coupled inductor at full load, with a per-phase average current of 37.5 A and other operating conditions listed in Table 8.3. The directions of the winding currents are illustrated in Fig. 8.7(a). The magnetic cores are most prone to saturation at Moments I–IV when the current in one phase reaches its peak value, as annotated with the dashed line. The magnetic flux density distributions in the bottom core at Moments I and II are shown in Fig. 8.11.

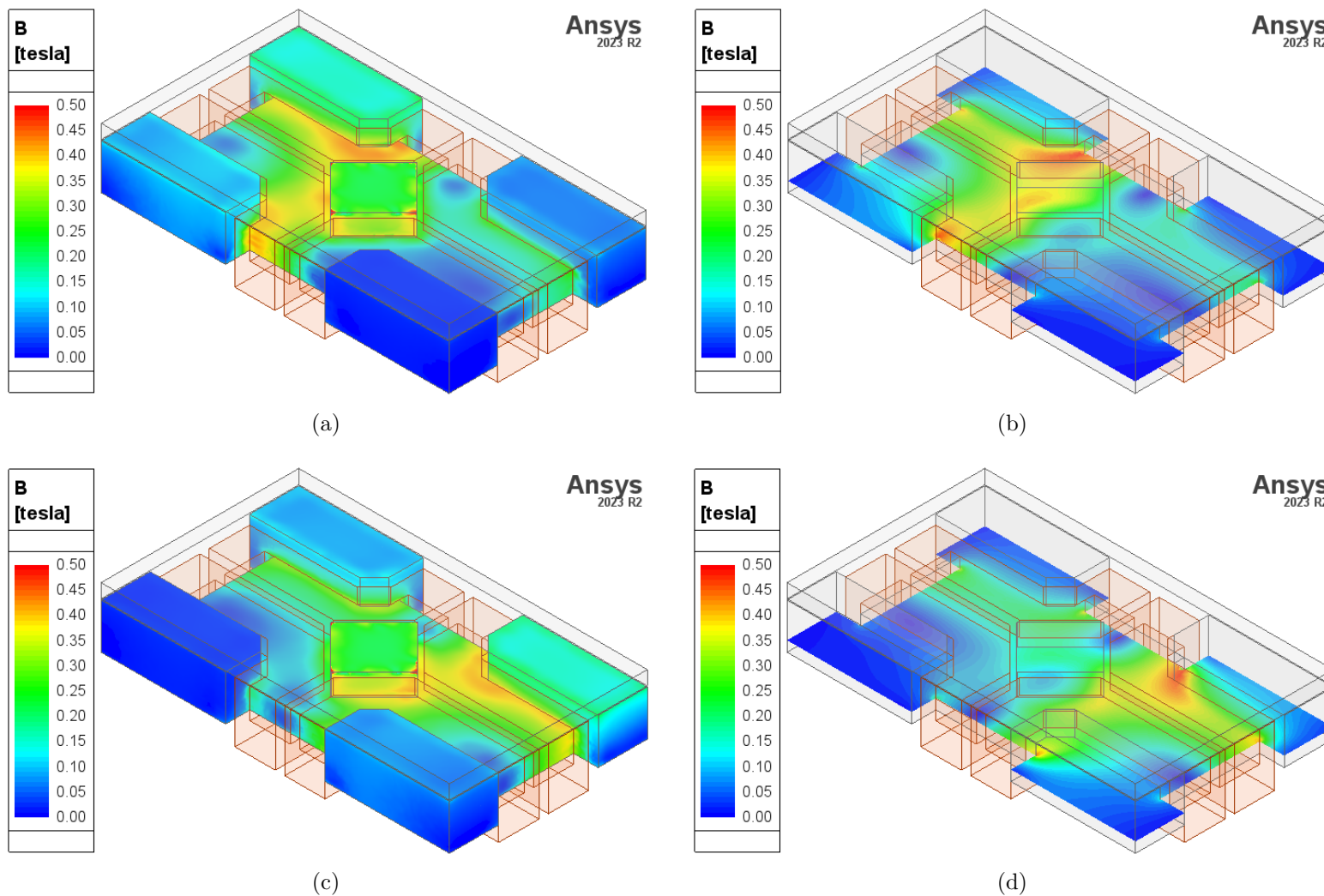


Figure 8.11: Magnetic flux density distributions in the bottom core at Moments I and II, as annotated in Fig. 8.10, when the magnetic cores are most prone to saturation. The magnetic flux density distributions at Moments III and IV are omitted since they are identical to those at Moments I and II after being rotated by 180° around the center of the bottom core. (a) Surface flux density distribution at Moment I. (b) Cross-sectional flux density distribution at Moment I. (c) Surface flux density distribution at Moment II. (d) Cross-sectional flux density distribution at Moment II.

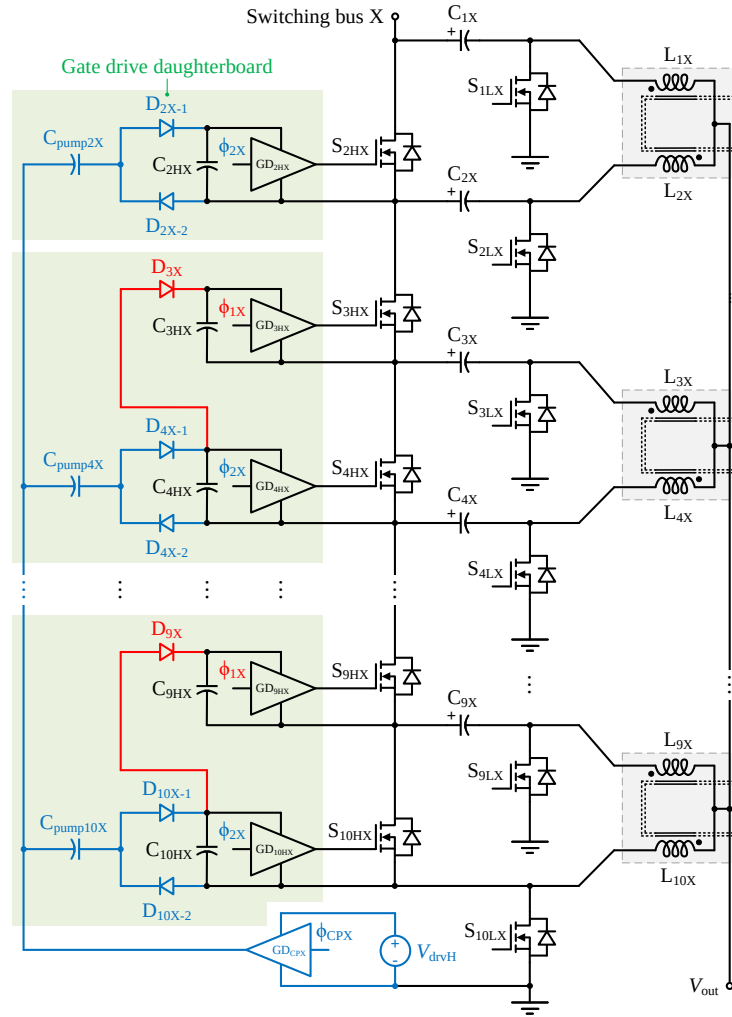
Table 8.3: Key parameters and operating conditions of the four-phase coupled inductor

Parameter	Value
Coupling coefficient	-0.91
Per-phase steady-state inductance*	260 nH
Per-phase transient inductance	31.8 nH
Overall transient inductance (40 phases)	0.80 nH
Per-phase dc resistance	0.16 m Ω
Output voltage	1.0 V
Switching frequency	220 kHz
Nominal duty ratio	0.417
Per-phase peak-to-peak current ripple*	10.2 A
Per-phase average current at full load	37.5 A
Height	3.2 mm

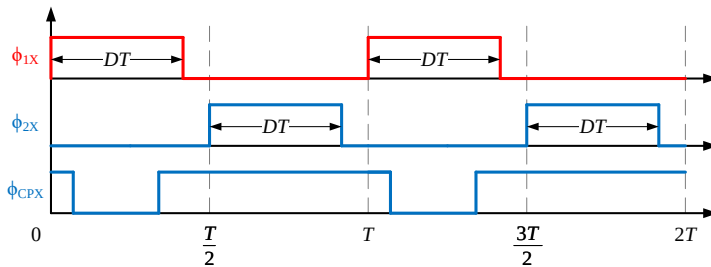
* Four-phase average value at $D = 0.417$.

Due to a large number of high-side switches in the SCB modules, conventional cascaded bootstrapping suffers from accumulative voltage drops across bootstrap diodes, leading to higher gate drive losses and gate drive voltage mismatch along the cascaded bootstrap chain [41]. To ensure that all high-side switches can be fully enhanced, the ground-referenced power supply V_{drvH} needs to be higher than the required gate drive voltage for full enhancement, such that there remains sufficient voltage at each switch after the diode voltage drop. For switching devices that only allow a narrow range of gate drive voltage, such as GaN transistors, low-dropout (LDO) regulators are typically required to tightly regulate the local gate drive voltage at the required level, which further increases gate drive losses and circuit complexity.

To address this challenge, this chapter customized a new gate drive circuit for the proposed topology by hybridizing gate-driven charge pumps [41] and cascaded bootstrapping, as shown in Fig. 8.12(a). In this hybrid gate drive circuit, switches $S_{2\text{HX},4\text{HX},\dots,10\text{HX}}$ are powered with gate-driven charge pump circuits, and switches $S_{3\text{HX},5\text{HX},\dots,9\text{HX}}$ are powered with cascaded bootstrap circuits. Fig. 8.12(b) illustrates the control signals of the hybrid gate drive circuit. Charge-pump capacitors $C_{\text{pump}2\text{X},\text{pump}4\text{X},\dots,\text{pump}10\text{X}}$ are charged by flying capacitors $C_{2\text{X},4\text{X},\dots,10\text{X}}$ when $\phi_{\text{CPX}} = 0$, and local decoupling capacitors $C_{2\text{HX},4\text{HX},\dots,10\text{HX}}$ are charged by the additional gate driver GD_{CPX} when $\phi_{\text{CPX}} = 1$. To ensure proper operation, ϕ_{CPX} must be high when $\phi_{2\text{X}} = 1$. Otherwise, charge-pump capacitors $C_{\text{pump}2\text{X},\text{pump}4\text{X},\dots,\text{pump}10\text{X}}$ will be overcharged by flying capacitors $C_{1\text{X},3\text{X},\dots,9\text{X}}$ through high-side switches $S_{2\text{HX},4\text{HX},\dots,10\text{HX}}$ when $\phi_{2\text{X}} = 1$. Therefore, as can be seen in Fig. 8.12(b), the pulse width of ϕ_{CPX} is greater than that of $\phi_{2\text{X}}$ to ensure ϕ_{CPX} always encompasses $\phi_{2\text{X}}$. This hybrid gate drive circuit was implemented as the green daughterboard presented in Fig. 8.13 with good modularity. In the hardware prototype presented in Figs. 8.5 and 8.6, the gate drive daughterboards were mounted on the bottom side of the red power board underneath the power MOSFETs.



(a)



(b)

Figure 8.12: Hybrid gate drive circuit customized for the high-side switches in Module X ($X = A, B, C, D$), where switches $S_{2HX}, S_{4HX}, \dots, S_{10HX}$ are powered with gate-driven charge pump circuits, and switches $S_{3HX}, S_{5HX}, \dots, S_{9HX}$ are powered with cascaded bootstrap circuits. (a) Schematic drawing. (b) Control signals.

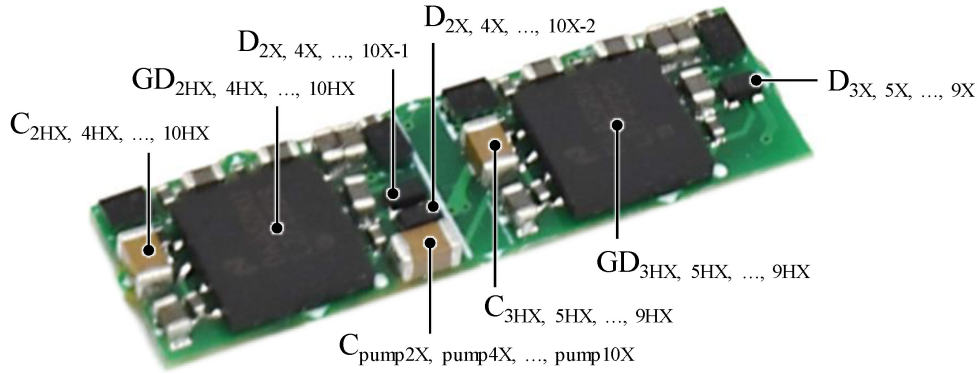


Figure 8.13: Photograph of the custom gate drive daughterboard for powering the switches in Module X ($X = A, B, C, D$), including high-side and low-side switches. Dimensions: $18.5 \times 5.5 \times 1.0 \text{ mm}^3$.

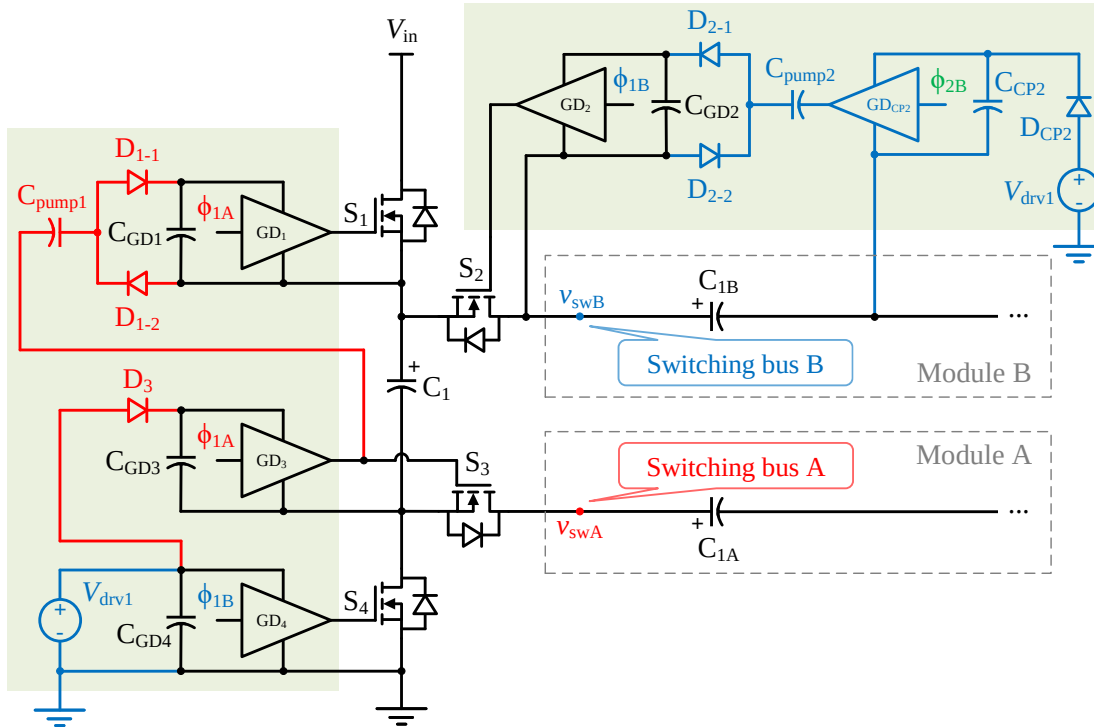


Figure 8.14: Gate drive circuitry for switches S_{1-4} in Stage 1. S_1 and S_2 are powered with gate-driven charge pump circuits. S_3 is powered with cascaded bootstrapping through a low voltage-drop diode D_3 . Control signals ϕ_{1A} , ϕ_{1B} and ϕ_{2B} are illustrated in Fig. 8.3. The gate drive circuitry for switches S_{5-8} is the same.

Table 8.4: Key parameters and test conditions of the hardware prototype

Parameter	Value
Nominal input voltage	48 V
Nominal output voltage	1.0 V
Maximum tested output current	1500 A (37.5 A/phase)
Switching frequency	220 kHz
Gate drive voltage of Stage 1	8.0 V
High-side gate drive voltage of Stage 2	6.5 V
Low-side gate drive voltage of Stage 2	5.3 V
Prototype box volume*	1.98 in ³
Power density by box volume	759 W/in ³

* The box volume is defined as the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry.

Another solution to powering the high-side switches in the SCB modules is the synchronous bootstrap technique [92], which was adopted in an earlier version of the proposed topology [115]. The idea of synchronous bootstrapping is to reduce the voltage drops in the bootstrap circuit by replacing bootstrap diodes with active FETs. Though effective and widely applicable, the synchronous bootstrap circuit has a high component count when implemented with discrete components, which complicates hardware implementation and reduces overall reliability. In contrast, the proposed hybrid gate drive circuit is simpler and more robust.

Fig. 8.14 illustrates the gate drive circuitry for Stage 1. The high-side switches S_1 , S_2 , S_5 and S_6 are powered with the gate-driven charge pump circuit proposed in [41]. S_3 and S_7 are powered with cascaded bootstrapping through a low voltage-drop diode.

8.4 Experimental Results and Performance Comparison

To validate the functionality and performance of the proposed switching bus converter, the hardware prototype was tested with an output current of up to 1500 A for 48-V-to-1-V conversion. Table 8.4 lists the key parameters and test conditions of the hardware prototype, with the experimental setup for automated efficiency measurement shown in Fig. 8.15. A 1000-A Chroma 63206A-60-1000 dc electronic load and two 600-A Chroma 63203 dc electronic loads were used to sink the ultra-high output current of the converter. The input voltage, input current, and output voltage were measured with a high-precision Yokogawa WT3000E power analyzer. The output current was measured by the dc electronic loads. A FLIR thermal camera was used to monitor the surface temperature of the prototype.

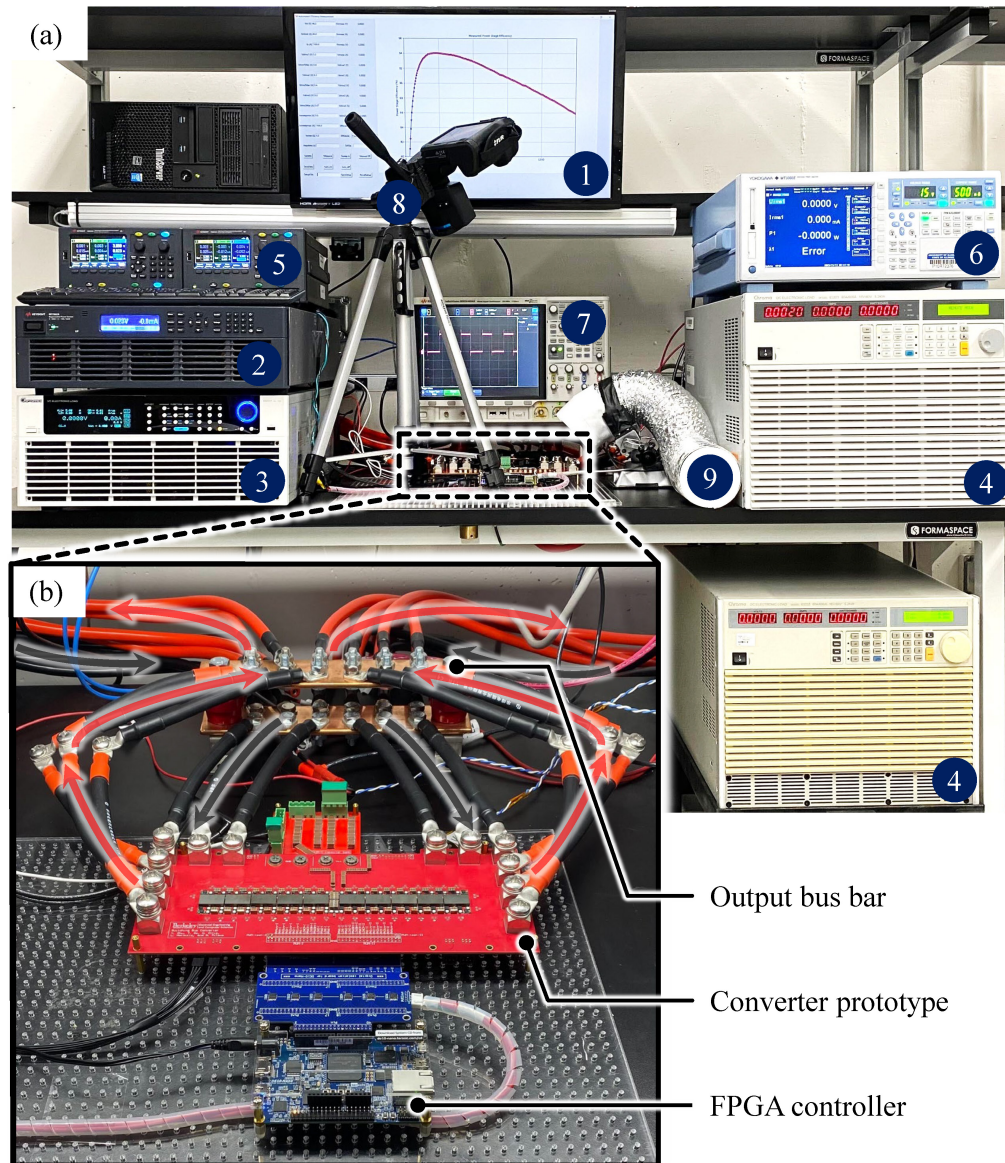


Figure 8.15: Experimental setup for automated efficiency measurement with remote control of equipment. (a) Bench setup. (b) Prototype under test. List of equipment: ① Monitor for displaying measurement results. ② Keysight RP7962A regenerative power system (500 V/ $\pm$ 40 A). ③ Chroma 63206A-60-1000 dc electronic load (60 V/1000 A). ④ Chroma 63203 dc electronic load (80 V/600 A) $\times$ 2. ⑤ Keysight E36312A triple output programmable dc power supply used to power the control and gate drive circuitry. ⑥ Yokogawa WT3000E precision power analyzer used to measure the input voltage, input current, and output voltage. ⑦ Keysight oscilloscope. ⑧ FLIR thermal camera. ⑨ Air inlet of the air cooling system.

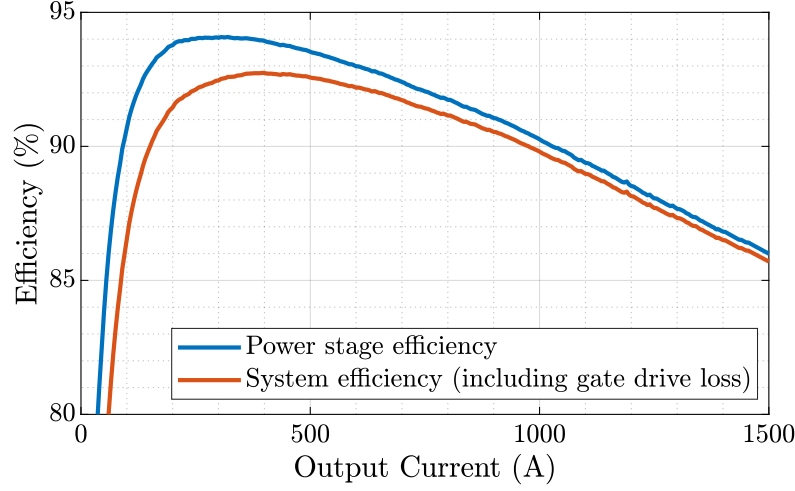


Figure 8.16: Measured 48-V-to-1-V efficiency. Peak efficiency: 94.1% at $I_{\text{out}} = 320$ A (92.7% at $I_{\text{out}} = 395$ A including gate drive loss). Heavy-load efficiency: 87.7% (87.3% including gate drive loss) at $I_{\text{out}} = 1300$ A. Full-load efficiency: 86.0% (85.7% including gate drive loss) at $I_{\text{out}} = 1500$ A.

8.4.1 Measured Performance

Fig. 8.16 presents the measured efficiency from the hardware prototype for 48-V-to-1-V conversion. It achieved a peak power stage efficiency of 94.1% at 320-A output current, a heavy-load power stage efficiency of 87.7% at 1300-A output current, and a full-load power stage efficiency of 86.0% at 1500-A output current. With gate drive loss included, it achieved 92.7% peak system efficiency at 395-A output current, 87.3% heavy-load system efficiency at 1300-A output current, and 85.7% full-load system efficiency. At 1500-A output current, the hardware prototype achieved a power density of 759 W/in³ by box volume (the volume of the best-fit cuboid encompassing the entire solution, including the gate drive circuitry).

Fig. 8.17 shows the thermal image of the prototype running continuously at an output current of 1300 A with air cooling only. It should be noted that the current hardware prototype does not incorporate any heat sink, heat spreader, or any other type of thermal management system. For continuous operation above 1300 A and converter temperature below 85 °C, either improved heat-sinking in air-cooled systems, or incorporation of liquid-cooling technology is needed. For example, a custom cold plate can be designed for the prototype utilizing the space above the switches between the flying capacitors and coupled inductors and leveraging the dual-side cooling package of the power MOSFETs.

It is worth noting that the theoretical high-performance potential of the proposed topology illustrated in Fig. 8.4 hasn't been fully realized in this hardware prototype. Although the voltage stresses on the high-side switches (i.e., $S_{2\text{HX}} - S_{10\text{HX}}$ [$X = A, B, C, D$]) and low-side switches (i.e., $S_{1\text{LX}} - S_{10\text{LX}}$ [$X = A, B, C, D$]) in Stage 2 are only 4.8 V and 2.4 V, respectively,

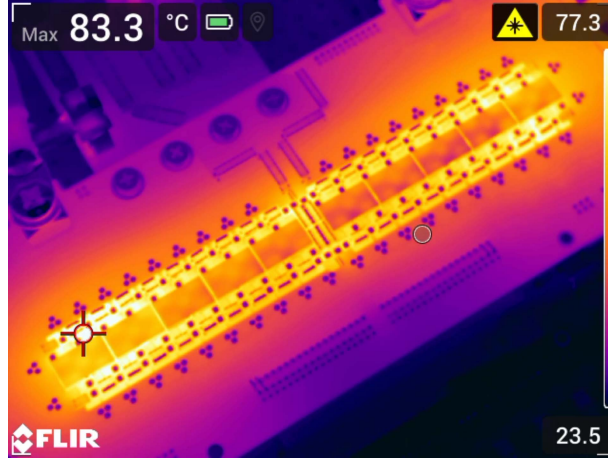


Figure 8.17: Thermal image at equilibrium with air cooling only ($V_{in} = 48$ V, $V_{out} = 1.0$ V, $I_{out} = 1300$ A). The air blew from the top-right corner of this thermal image to the bottom-left corner.

the best switching devices available on the market for this application when the prototype was built are rated at 25 V (Infineon IQE006NE2LM5 and IQE006NE2LM5CG). If implemented with lower voltage devices with lower $R_{ds(on)}$ and smaller C_{oss} , this prototype would be able to achieve better performance. Currently, there are already 15-V MOSFETs in dual-side cooling packages (Infineon IQE004NE1LM7SC and IQE004NE1LM7CGSC) with both better electrical characteristics and higher thermal performance. With the advancement of device technologies, the theoretical potential of the proposed topology can be further unleashed in the future.

8.4.2 Loss Analysis

Fig. 8.18 presents a comprehensive loss breakdown of the hardware prototype at both the peak system efficiency point and full-load point. This loss analysis was conducted to offer a deeper understanding of the sources of power losses in the prototype and to identify potential avenues for performance improvement. The MOSFET conduction loss was simulated with the measured duty ratio at the corresponding output current and with the ON-resistance ($R_{ds(on)}$) provided by the datasheets. The MOSFET switching loss incorporates the C_{oss} loss and the overlap loss, estimated with the datasheet parameters. The coupled inductor core loss was simulated with an electric-thermal co-simulation in ANSYS. The PCB trace resistance and parasitic commutation loop inductance were estimated with finite element analysis (FEA) using ANSYS.

At the peak system efficiency point, frequency-dependent losses—including MOSFET switching loss, body-diode conduction loss, MOSFET gate drive loss, coupled inductor core loss, and parasitic inductance loss—predominate the total loss. Conversely, conduction losses

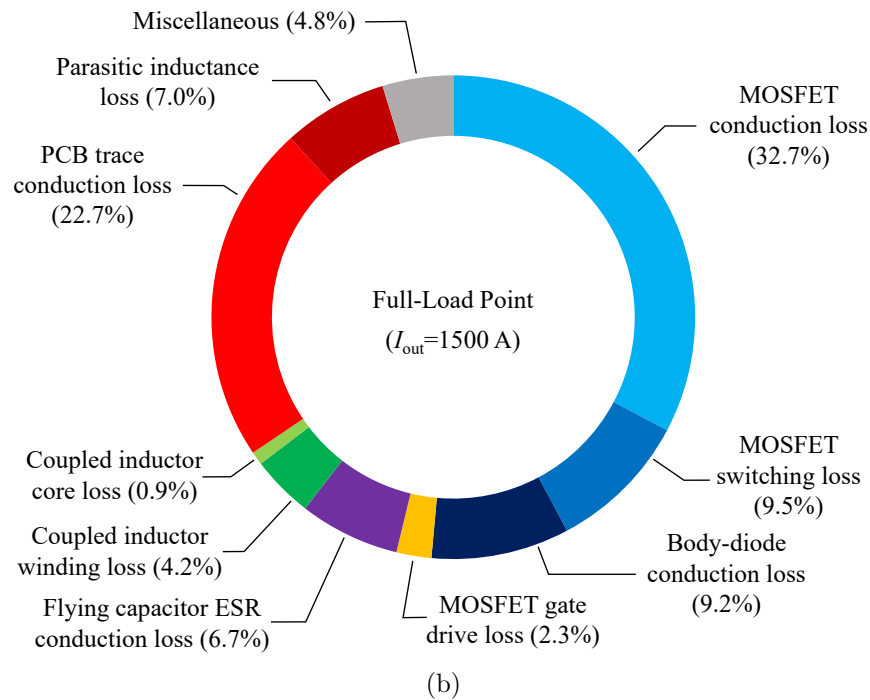
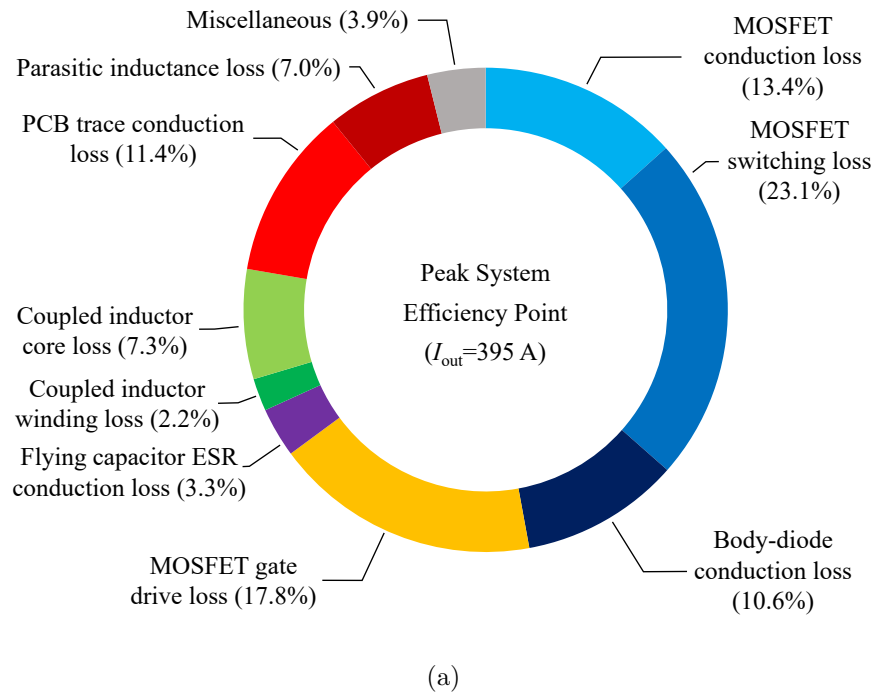


Figure 8.18: Loss breakdown of the hardware prototype. (a) Loss breakdown at the peak system efficiency point. (b) Loss breakdown at the full-load point.

such as MOSFET conduction loss, body-diode conduction loss, flying capacitor ESR conduction loss, coupled inductor winding loss, and PCB trace conduction loss become more dominant at the full-load point.

8.4.3 Performance Comparison with the State of the Art

Tables 8.5 and 8.6 compare the performance of this work to that of the state-of-the-art 48-V-to-1-V academic works and commercial products, respectively. Compared to existing solutions, this laboratory prototype achieved the highest output current with outstanding efficiency and power density, even when benchmarked against highly optimized commercial power modules with advanced packaging.

Fig. 8.19 visually illustrates the system performance of the state-of-the-art 48-V-to-1-V academic hybrid SC works and commercial products that report their measured system efficiencies (including gate drive loss). The performance of each solution is visually represented by two dots: the bottom-right dot denotes the performance at the peak system efficiency point, and the top-left dot denotes the performance at the full-load point. Solid dots represent the performance of academic works, while hollow dots correspond to the performance of commercial products. As can be seen in Fig. 8.19, this prototype pushes the performance limit toward the upper right corner, which represents higher efficiency and higher power density.

8.5 Chapter Summary

This chapter introduces an ultra-high-current 48-V-to-1-V switching bus converter with a single-stage VPD architecture for next-generation processors. The proposed topology merges two 2-to-1 SC front-ends with four 10-branch SCB modules through four switching buses, achieving a very large SC stage conversion ratio of 20-to-1. In contrast to the existing dc-bus-based architecture, the proposed switching-bus-based architecture eliminates the need for dc bus capacitors, reduces the switch count, and guarantees complete soft-charging operation. Furthermore, a topological comparison reveals that the proposed topology, when compared to existing 48-V-to-1-V hybrid SC demonstrations, achieves the lowest normalized switch stress and the smallest normalized passive component volume with the largest SC stage conversion ratio compared to existing 48-V-to-1-V hybrid SC demonstrations. This suggests that the proposed topology holds great promise for simultaneously achieving higher efficiency and power density than prior hybrid SC solutions.

To validate the theoretical potential of the proposed topology, a hardware prototype with good modularity and extendability was designed and constructed with customized coupled magnetics and gate drive circuitry. A four-phase coupled inductor was optimized for a good trade-off between size and transient performance, with the range of duty ratio taken into consideration. In addition, an efficient, simple, and robust hybrid gate drive circuit was designed to overcome the accumulative diode voltage drops of conventional cascaded

Table 8.5: Performance comparison between this work (20-to-1 SBC) and the state-of-the-art 48-V-to-1-V academic works

Year	Reference	Output Current	Operating Frequency*	Power Density**	Power Stage Efficiency	System Efficiency [†]
2024	This work (20-to-1 SBC)	1500 A (37.5 A/phase)	220 kHz	759 W/in ³ (by box volume)	Peak efficiency: 94.1% Full-load efficiency: 86.0%	92.7% 85.7%
2023	16-to-1 SBC [115]	500 A (31.3 A/phase)	150 kHz	464 W/in ³ (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2023	MSC [97]	450 A (28.1 A/phase)	400 kHz	621 W/in ³ (by box volume)	Peak efficiency: 93.1% Full-load efficiency: 86.2%	91.7% 85.8%
2023	Mini-LEGO [114]	240 A (20 A/phase)	1.5 MHz	1390 W/in ³ (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2022	SDIH [82]	105 A (52.5 A/phase)	750 kHz	598 W/in ³ (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2022	Dickson ² [75]	270 A (30 A/phase)	280 kHz	360 W/in ³ (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [77]	450 A (28.1 A/phase)	417 kHz	232 W/in ³ (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [76]	60 A (30 A/phase)	250 kHz	263 W/in ³ (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	LEGO [83]	450 A (37.5 A/phase)	1 MHz	294 W/in ³ (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [70]	40 A (20 A/phase)	125 kHz	150 W/in ³ (by power component volume)	Peak efficiency: 95.1% [‡] Full-load efficiency: 92.7% [‡]	N/A N/A
2020	Sigma [99]	80 A	1 MHz	420 W/in ³ (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

* Switching frequency of the voltage regulation stage.

** The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.

[†] Gate drive loss is included in the calculation of system efficiency.

[‡] According to direct correspondence with the author.

Table 8.6: Performance comparison between this work (20-to-1 SBC) and existing 48-V-to-1-V commercial products

Release Year	Reference	Output Current	Operating frequency*	Power Density**	System Efficiency [†]
2024	This work (20-to-1 SBC)	1500 A	220 kHz	759 W/in ³	Peak: 92.7%, Full-load: 85.7%
2021	Analog Devices LTM4664 [100]	50 A	350 kHz	415 W/in ³	Peak: 90.8%, Full-load: 88.0%
2019	Flex Power Modules BMR482 (satellite) [128]	110 A	600 kHz	306 W/in ³	Peak: 92.1%, Full-load: 87.4%
2018	Bel Power Solutions ST4-1V0M07G [101]	70 A	450 kHz	167 W/in ³	Peak: 91.5%, Full-load: 90.5%
2016	Texas Instruments LMG5200POLEV10 [102]	50 A	600 kHz	N/A	Peak: 90.7%, Full-load: 87.6%
2012 2015	Vicor PRM48AF480T400A00 [103] +2×VTM48EF012T130C01 [104] [‡]	200 A	1.03 MHz 1.20 MHz	236 W/in ³	Total efficiency: 89.7% [‡]

* Switching frequency of the voltage regulation stage.

**Power density calculated by the box volume.

[†] Gate drive loss is included in the calculation of system efficiency.
System Designer.

[‡]Recommended and provided by Vicor's online Power

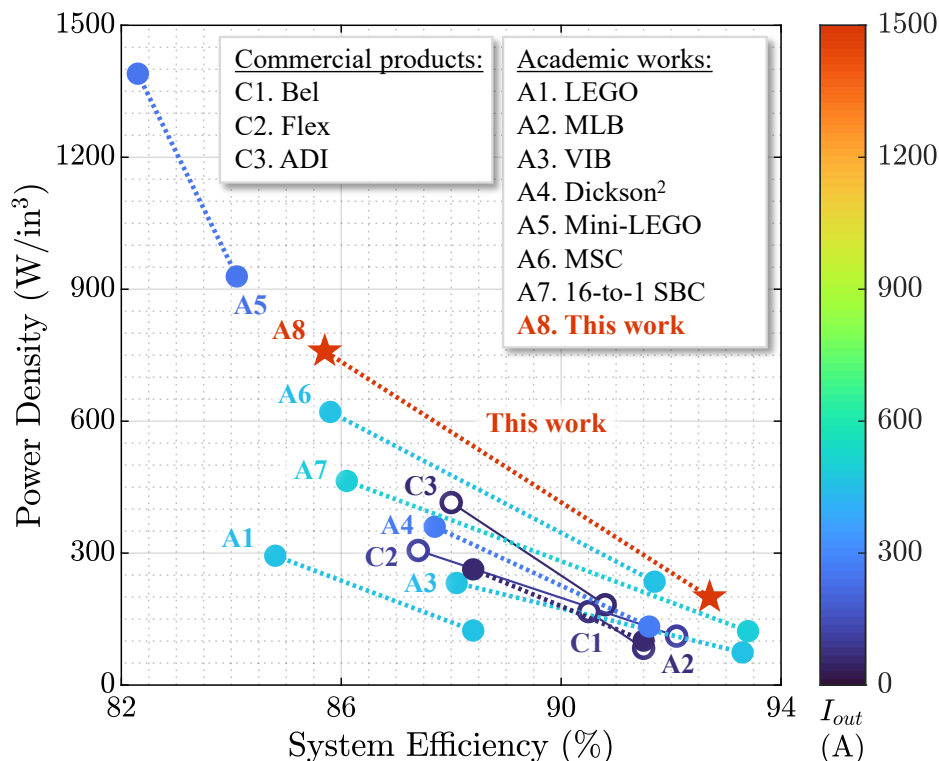


Figure 8.19: Performance comparison between this work (20-to-1 SBC) and the state-of-the-art 48-V-to-1-V academic hybrid SC works and commercial products. The performance of each solution is visually represented by two dots, with the bottom-right dot denoting the performance at the peak system efficiency point and the top-left dot denoting the performance at the full-load point. The system performances of academic works and commercial products are illustrated with solid and hollow dots, respectively.

bootstrapping. This hybrid gate drive circuit powered the high-side switches in the SCB modules and was implemented as modular gate drive daughterboards.

The hardware prototype was tested up to 1500-A output current for 48-V-to-1-V conversion and achieved 92.7% peak system efficiency, 85.7% full-load system efficiency (including gate drive loss), and 759 W/in³ power density (by box volume) without any heat sink and with air cooling only. The outstanding performance of this laboratory prototype pushes the performance limit of the state-of-the-art 48-V-to-1-V solutions, including academic works and commercial products, towards higher efficiency and higher power density.

Chapter 9

A Compact 48-V-to-Sub-1-V Switching Bus Converter with 4.7-mm Height for Processor Vertical Power Delivery

9.1 Background and Motivation

High-performance processors (e.g., GPUs, CPUs, ASICs, etc.) serve as the engine of data center computing platforms and the foundation for technical progress in areas such as artificial intelligence, machine learning, and autonomous vehicles. In recent years, processor power consumption has increased dramatically due to the fast-growing demand for greater computational power and is approaching 1000 W, with core logic voltages below 1 V and peak current demand beyond 1000 A.

With operating currents beyond 1000 A, the high power distribution network (PDN) resistance of existing two-stage lateral power delivery (LPD) solutions can lead to a dramatic voltage drop and unacceptable PDN losses, which significantly limits processor performance, reduces system energy efficiency, and hinders data center decarbonization. Moreover, the resulting low efficiency necessitates a larger thermal management size, which is presently a bottleneck of system densification.

This chapter presents a compact switching bus converter (SBC) to address the above challenges with single-stage vertical power delivery (VPD) as illustrated in Fig. 9.1. In this single-stage VPD solution, the proposed SBC is placed on the bottom side of the motherboard directly underneath the processor so that it can deliver high current vertically to the top side through vias, which greatly reduces the PDN size and PDN losses and saves the valuable topside area on the motherboard for high bandwidth memory (HBM) and high-speed communication. In addition to an overall small converter size, stringent height limitations (e.g., < 5 mm) are required of the solution in this application, owing to connec-

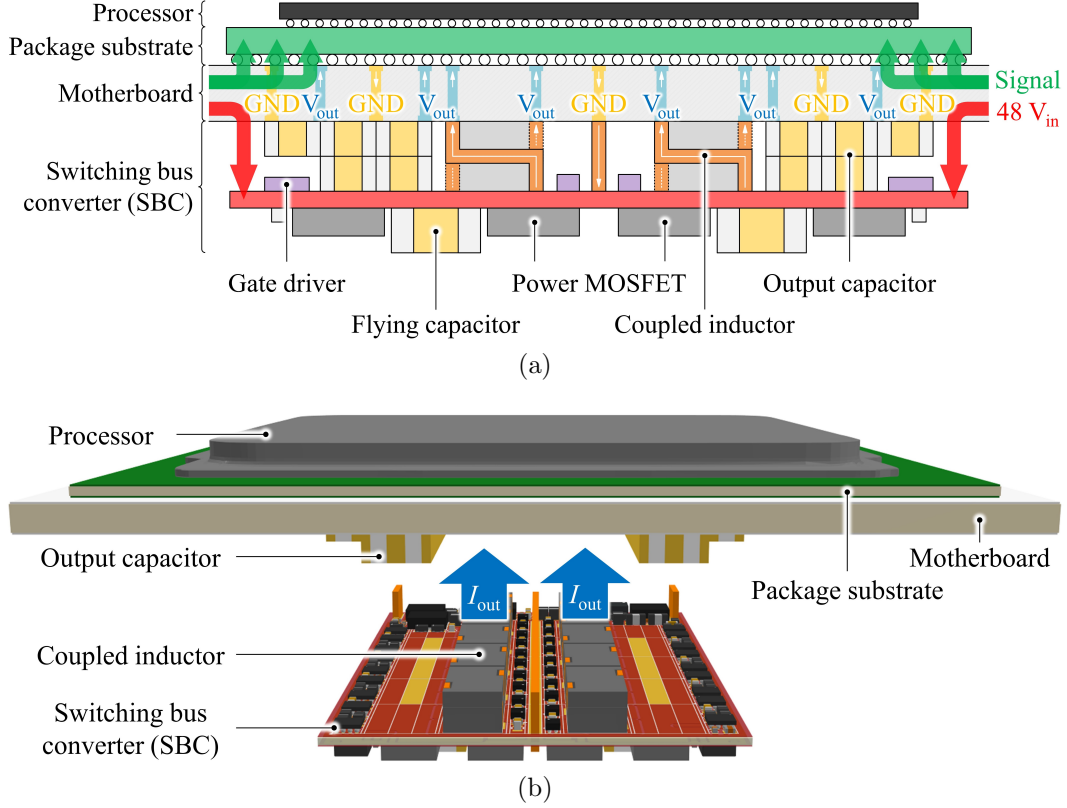


Figure 9.1: Single-stage vertical power delivery (VPD) with the proposed switching bus converter (SBC). (a) Side view. (b) 3D rendering.

tor heights. Moreover, merging two conversion stages into one single stage reduces power conversion losses and eliminates the need for dc bus capacitors, which effectively improves overall system efficiency and power density.

9.2 Proposed Topology and Operating Principles

Fig. 9.2 shows the schematic drawing of the proposed switching bus converter, with the control signals illustrated in Chapter 7. In the proposed topology, a 2-to-1 SC front-end (i.e., Stage 1) is merged with two 10-to-1 series-capacitor-buck (SCB) modules (i.e., Modules A and B in Stage 2) through two switching buses (i.e., Switching buses A and B). Each SCB module consists of five submodules and operates in a two-phase fashion with a phase shift of 180° between neighboring branches. As explained in Chapter 7, two-phase operation greatly increases the effective conversion ratio of the SC stage compared to conventional multi-phase control, which enables higher efficiency and higher power density. The two inductors in each submodule are coupled and implemented as a two-phase coupled inductor. Since

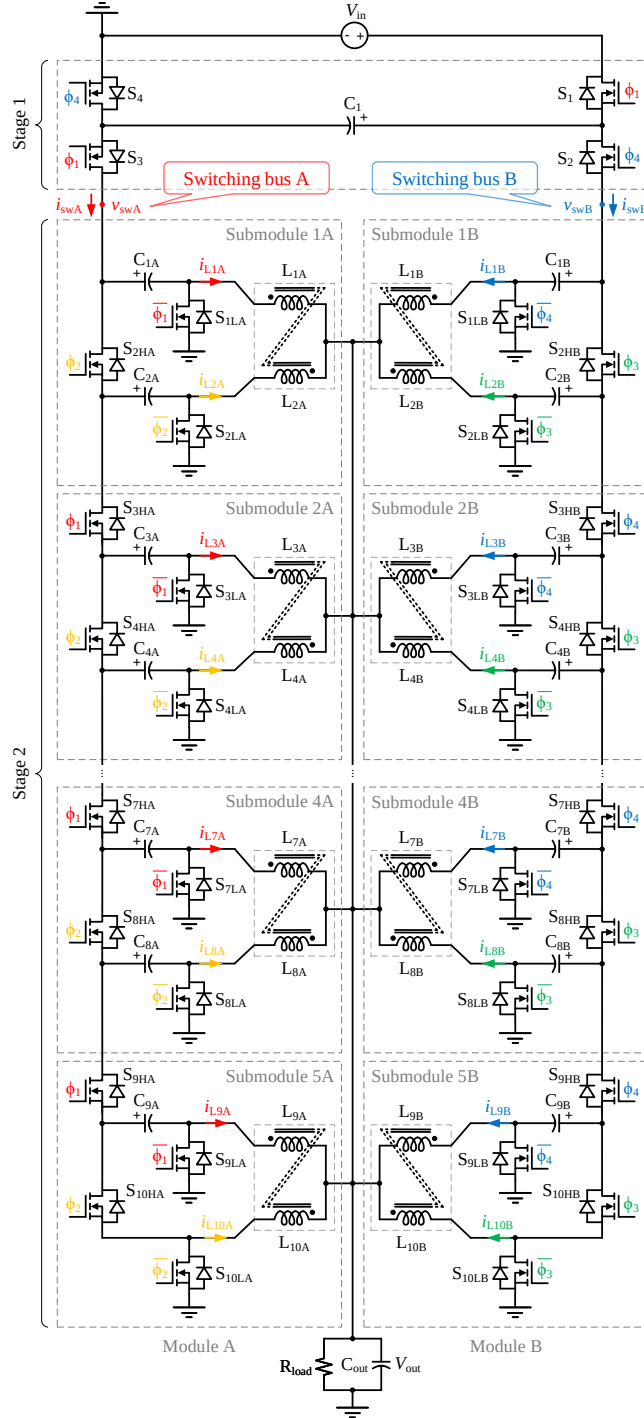


Figure 9.2: Schematic of the proposed switching bus converter.

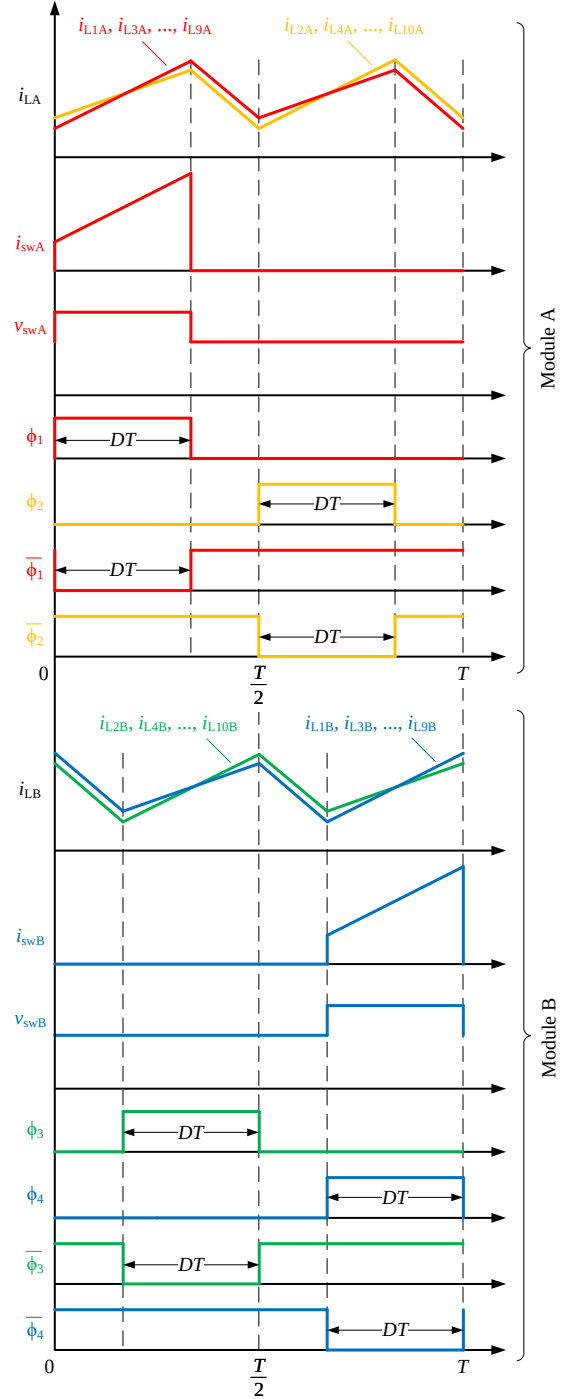


Figure 9.3: Control signals of the proposed switching bus converter.

the bus voltages v_{swA} and v_{swB} always switch between two voltage levels rather than being dc, this type of intermediate bus is referred to as a *switching bus* [75, 115]. Compared to the existing dc-bus-based architecture, the switching-bus-based architecture does not require intermediate dc bus capacitors, reduces the number of switches, and ensures complete soft-charging operation, as explained in Chapter 7.

9.3 Hardware Implementation and Experimental Results

A 48-V-to-sub-1-V hardware prototype was designed and built to verify the functionality and performance of the proposed converter. Fig. 9.4 shows the annotated photograph of the prototype, with an overview of the prototype mounted on a white motherboard provided in Fig. 9.5. The two inductors in each submodule illustrated in Fig. 9.2 were implemented as a custom two-phase coupled inductor. As shown in Figs. 9.1 and 9.5, the coupled inductors and output capacitors were packaged between the red converter board and the white motherboard for VPD. The coupled inductors serve as the connection between the two boards and deliver the high output current (I_{out}) vertically, which can help reduce the resistance on the output current path.

The hardware prototype was tested in two configurations. Figs. 9.2 and 9.4 show the 10-branch configuration where each SCB modules consist of 10 inductor branches. To investigate the impact of the number of branches on the converter performance, the hardware prototype was reconfigured into an 8-branch configuration by removing all switches and flying capacitors in Submodules 5A and 5B in Fig. 9.2 and short-circuiting flying capacitors C_{8A} and C_{8B} in Submodules 4A and 4B. Fig. 9.6 shows the steady-state thermal image of the prototype in the 8-branch configuration running continuously at 300-A output current with fan cooling only. Figs. 9.7 and 9.8 present the measured efficiency of the hardware prototype in the 10-branch and 8-branch configurations, respectively, at 48-V input voltage and sub-1-V output voltages. It was tested up to an output current of 600 A and 400 A in the 10-branch and 8-branch configurations, respectively. The switching frequency was 600 kHz in all cases.

Table 9.1 compares the performance of this work with that of the state-of-the-art 48-V-to-1-V academic works presented in previous literature, with the performance of each work at the peak system efficiency point and the full-load point plotted in Fig. 9.9. As can be seen in Table 9.1 and Fig. 9.9, this work achieved excellent power density while maintaining high efficiency, pushing the performance limit in Fig. 9.9 toward the top-right corner.

9.4 Chapter Summary

This chapter presents a compact switching bus converter with 4.7-mm height for single-stage VPD. In the proposed topology, a 2-to-1 SC front-end is merged with two 10-branch SCB

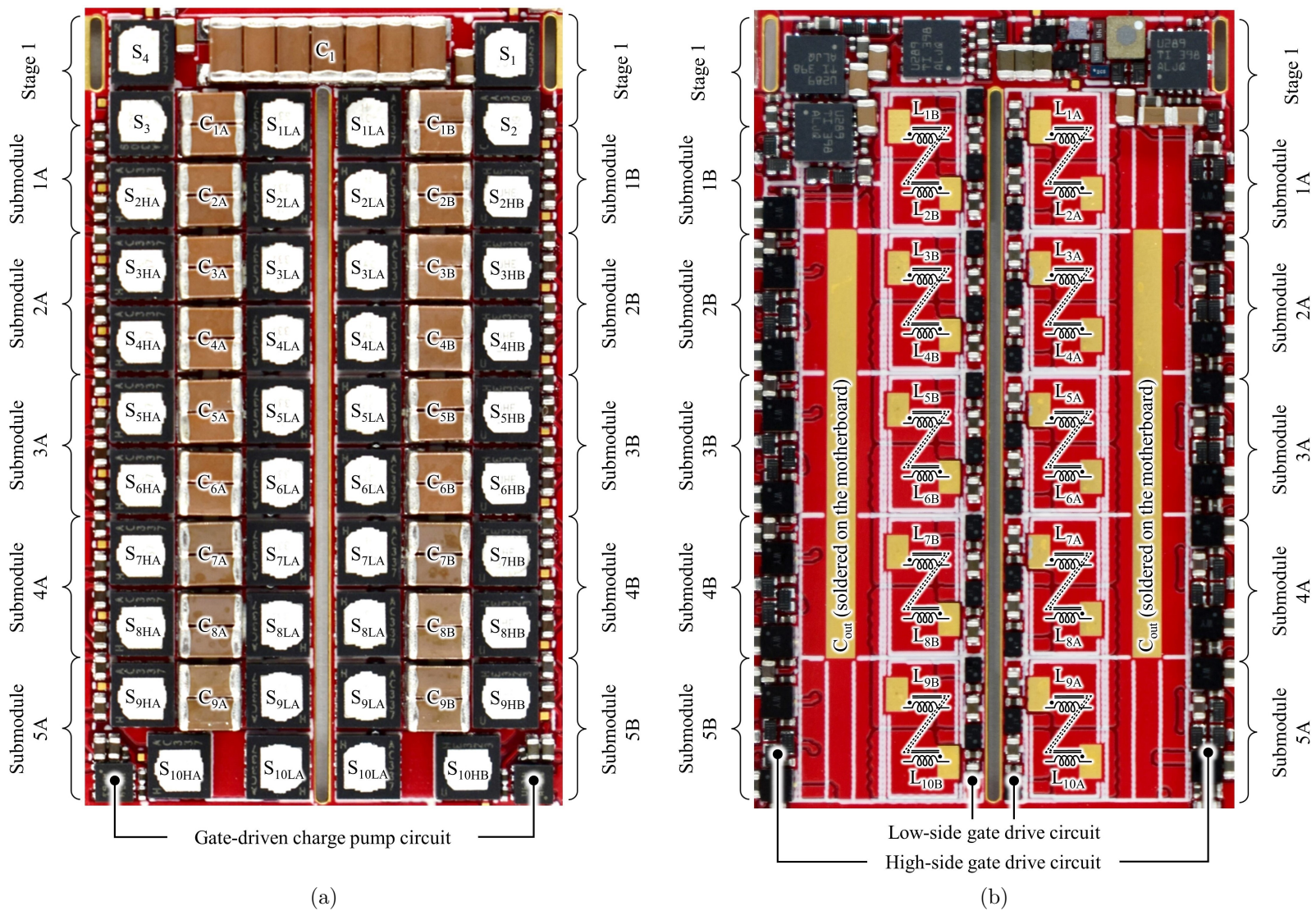
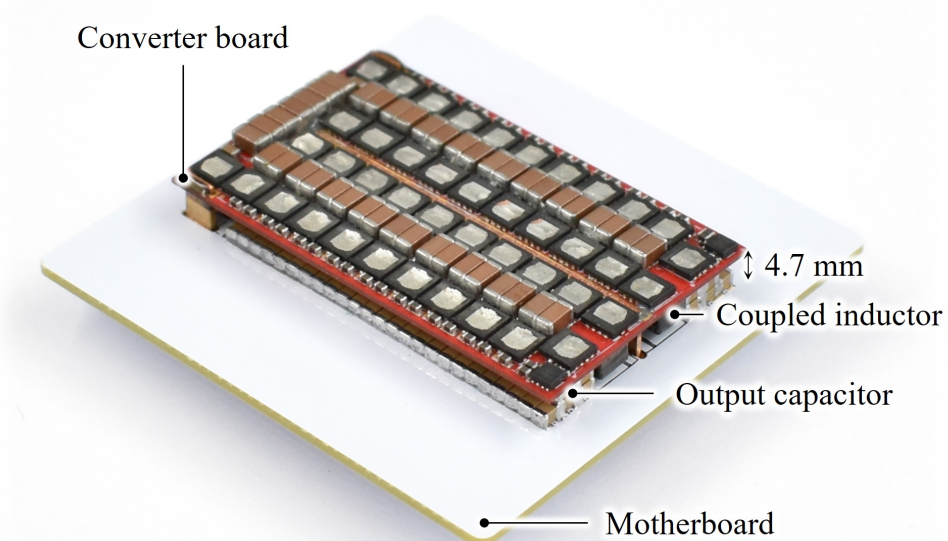
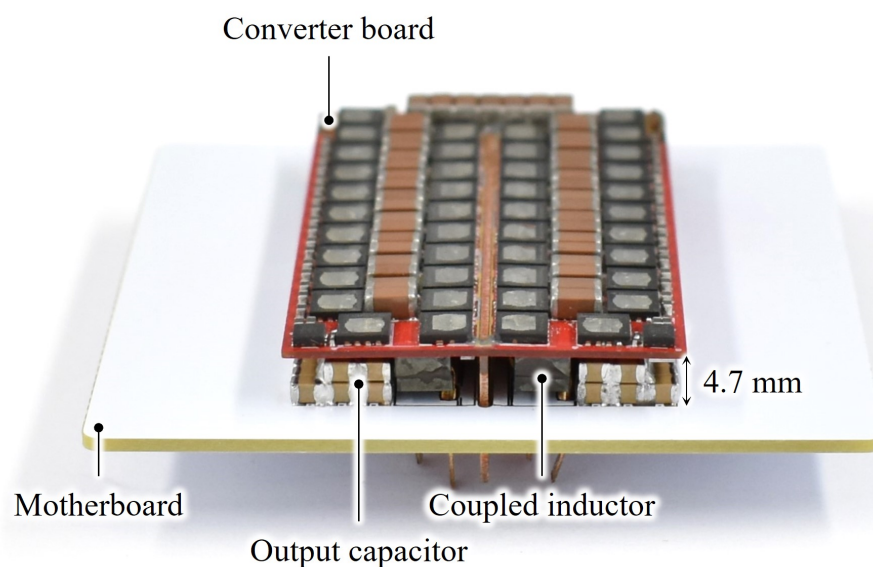


Figure 9.4: Photograph of the hardware prototype. Dimensions: $1.60 \times 0.945 \times 0.185 \text{ in}^3$ ($40.7 \times 24.0 \times 4.7 \text{ mm}^3$). (a) Top view. (b) Bottom view.



(a)



(b)

Figure 9.5: (a) Overview of the prototype mounted on a white motherboard. (b) Coupled inductors and output capacitors were packaged between the red converter board and the white motherboard.

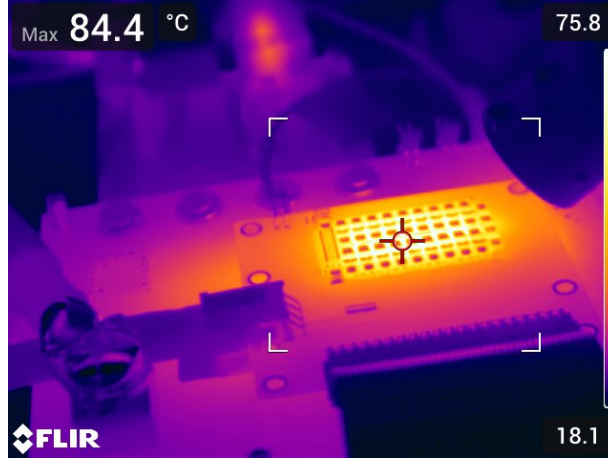


Figure 9.6: Steady-state thermal image of the prototype in the 8-branch configuration cooled by a 44.2 CFM fan only. ($V_{in} = 48$ V, $V_{out} = 1.0$ V, $I_{out} = 300$ A).

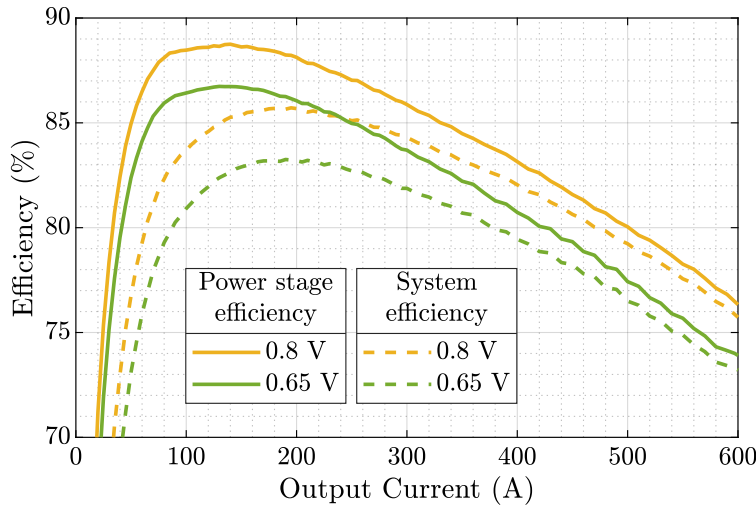


Figure 9.7: Measured power stage efficiency (excluding the gate drive loss) and system efficiency (including the gate drive loss) of the hardware prototype in the 10-branch configuration at 48-V input voltage and sub-1-V output voltages.

modules through two switching buses. Compared to the existing dc-bus-based architecture, the switching-bus-based architecture does not require dc bus capacitors, reduces the number of switches, and ensures complete soft-charging operation. A 48-V-to-sub-1-V hardware prototype was designed and built with custom two-phase coupled inductors for VPD. It was tested up to 600-A output current and achieved excellent performance compared to the state-of-the-art 48-V-to-1-V academic works presented in previous literature.

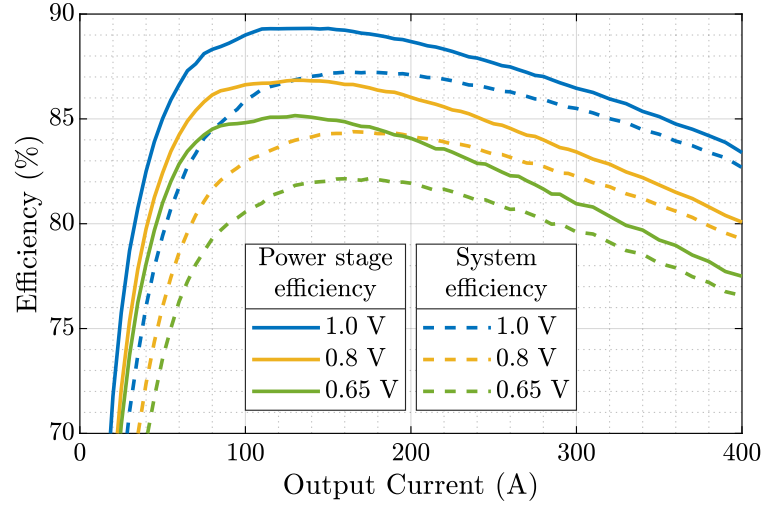


Figure 9.8: Measured power stage efficiency (excluding the gate drive loss) and system efficiency (including the gate drive loss) of the hardware prototype in the 8-branch configuration at 48-V input voltage and sub-1-V output voltages.

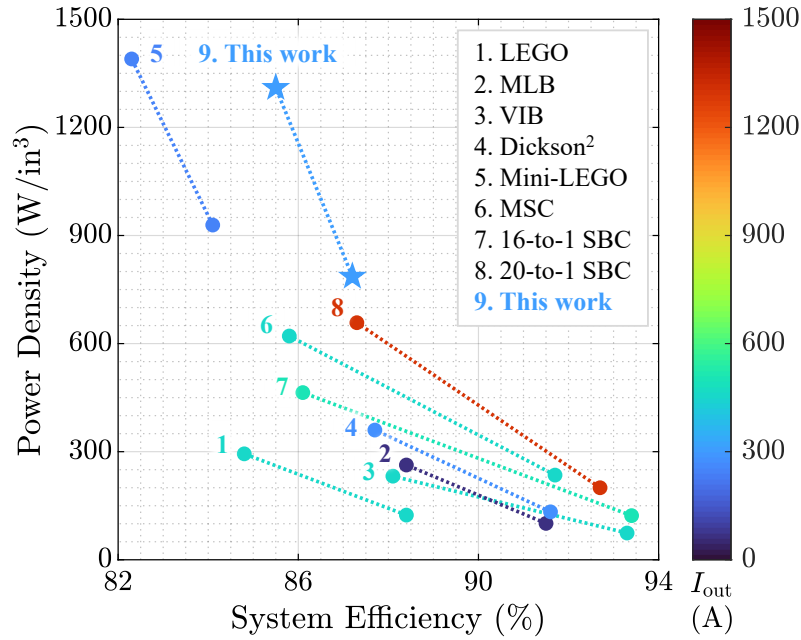


Figure 9.9: Performance comparison between this work (SBC-VPD) and the state-of-the-art 48-V-to-1-V hybrid SC works.

Table 9.1: Performance comparison between this work (SBC-VPD) and the state-of-the-art 48-V-to-1-V academic works

Year	Reference	Output Current	Power Density [†]	Power Stage Efficiency	System Efficiency [‡]
2024	This work (SBC-VPD)	300 A (18.8 A/phase)	1310 W/in ³ (by box volume)	Peak efficiency: 89.3% Full-load efficiency: 86.5%	87.2% 85.5%
2024	20-to-1 SBC [123]	1300 A (32.5 A/phase)	658 W/in ³ (by box volume)	Peak efficiency: 94.1% Full-load efficiency: 87.7%	92.7% 87.3%
2023	16-to-1 SBC [115]	500 A (31.3 A/phase)	464 W/in ³ (by box volume)	Peak efficiency: 94.7% Full-load efficiency: 86.4%	93.4% 86.1%
2023	MSC [97]	220 A (27.5 A/phase)	607 W/in ³ (by box volume)	Peak efficiency: 92.9% Full-load efficiency: 86.3%	91.1% 85.8%
2023	Mini-LEGO [98]	240 A (20 A/phase)	1390 W/in ³ (by box volume)	Peak efficiency: 87.1% Full-load efficiency: 84.1%	84.1% 82.3%
2023	SDIH [82]	105 A (52.5 A/phase)	598 W/in ³ (by box volume)	Peak efficiency: 83.5% Full-load efficiency: 71.5%	81.4% 70.9%
2022	Dickson ² [75]	270 A (30 A/phase)	360 W/in ³ (by box volume)	Peak efficiency: 93.8% Full-load efficiency: 88.4%	91.6% 87.7%
2022	VIB [77]	450 A (28.1 A/phase)	232 W/in ³ (by box volume)	Peak efficiency: 95.2% Full-load efficiency: 89.1%	93.3% 88.1%
2022	MLB [76]	60 A (30 A/phase)	263 W/in ³ (by box volume)	Peak efficiency: 92.7% Full-load efficiency: 88.6%	91.5% 88.4%
2022	LEGO [83]	450 A (37.5 A/phase)	294 W/in ³ (by box volume)	Peak efficiency: 91.1% Full-load efficiency: 85.7%	88.4% 84.8%
2020	Crossed-coupled QSD buck [70]	40 A (20 A/phase)	150 W/in ³ (by power component volume)	Peak efficiency: 95.1%* Full-load efficiency: 92.7%*	N/A N/A
2020	Sigma [99]	80 A	420 W/in ³ (by box volume)	Peak efficiency: 94.0% Full-load efficiency: 92.5%	N/A N/A

[†] The box volume is measured as the smallest rectangular box that can contain the converter, including the gate drive circuitry.

[‡] Gate drive loss is included in the calculation of system efficiency.
the author.

*According to direct correspondence with

Chapter 10

Generalized Switching-Bus-Based Architecture for Regulated Hybrid Switched-Capacitor Converters

10.1 Generalized Switching-Bus-Based Architecture

This chapter presents a switching-bus-based architecture for regulated hybrid switched-capacitor (SC) converters composed of multiple pure SC units and regulated hybrid SC units, as illustrated in Fig. 10.1. Each stage can have one or multiple SC units. The conversion ratio of Unit j in Stage i is denoted as $N_{i,j:1}$. The last stage consists of multiple regulated hybrid SC units. As shown in Figure 1, the intermediate bus voltages always switch between two different levels. Therefore, this type of intermediate bus is referred to as a switching bus. Power electronics converters constructed with switching buses are referred to as switching-bus-based converters.

Section 7.1.4 details the advantages of the proposed switching-bus-based architecture over the existing dc-bus-based architecture. Compared to the existing dc-bus-based architecture illustrated in Fig. 7.3(a), the proposed switching-bus-based architecture shown in Fig. 7.3(b) has three advantages that promise higher performance:

- It does not require bus capacitors to maintain a stiff dc bus voltage.
- One redundant switch can be removed on each switching bus while two stages are merged.
- It ensures complete soft-charging operation.

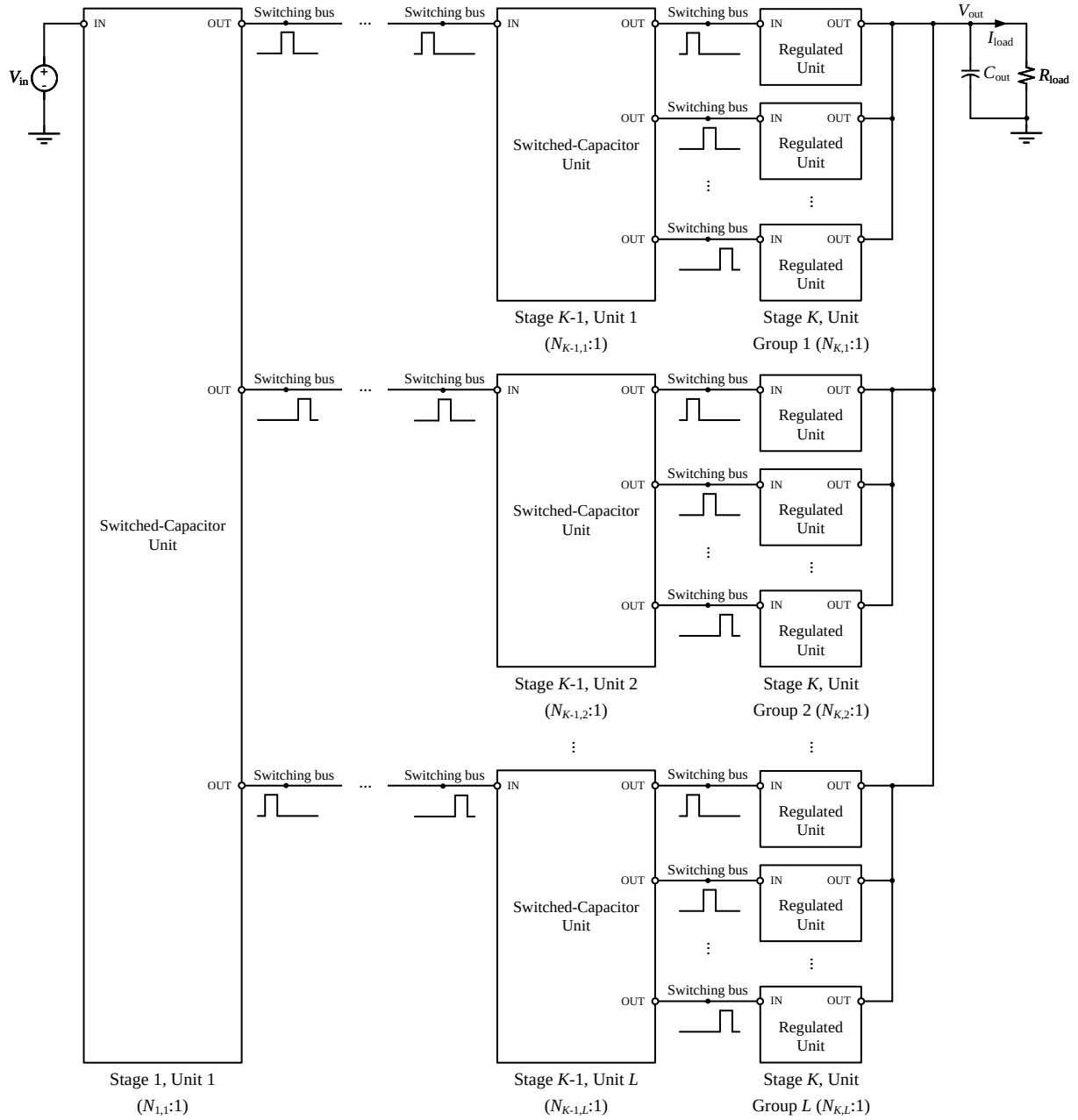


Figure 10.1: Generalized switching-bus-based architecture for regulated hybrid switched-capacitor converters.

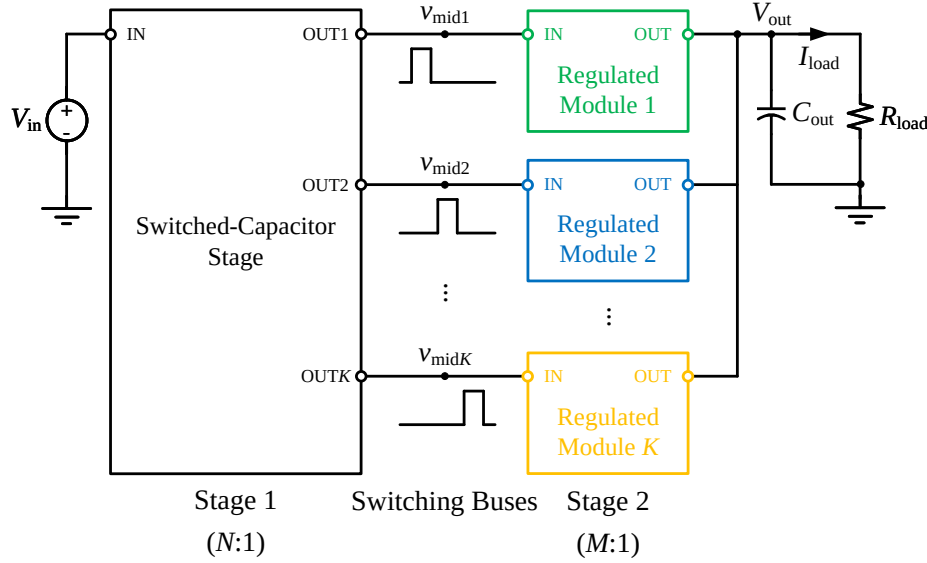


Figure 10.2: Generalized switching-bus-based architecture for regulated hybrid switched-capacitor converters.

10.2 Two-Stage Switching-Bus-Based Architecture

Fig. 10.2 illustrates the block diagram of a two-stage switching-bus-based architecture. It consists of two conversion stages: 1) a fixed-ratio SC stage, Stage 1, with a SC conversion ratio of $N : 1$, and 2) a regulated stage, Stage 2, with a SC conversion ratio of $M : 1$. The two conversion stages are merged through K switching buses. A two-stage switching-bus-based topology can be characterized by the above three parameters: Stage 1 SC conversion ratio ($N : 1$), the number of switching buses (K), and Stage 2 SC conversion ratio ($M : 1$). This section provides several concrete examples of topologies based on this architecture.

10.2.1 Switching Bus Converters

The 16-to-1 switching bus converter ($N = 2$, $K = 2$, and $M = 8$) presented in Chapter 7 and the 20-to-1 switching bus converter ($N = 2$, $K = 2$, and $M = 10$) presented in Chapter 8 are constructed based on the above two-stage switching-bus-based architecture. In the switching bus converters, the two stages are merged through two switching buses. The conversion ratio of the first stage is $2 : 1$, while the SC step-down ratio of the second stage can be $2 : 1$, $4 : 1$, $\dots$, $10 : 1$ for 48-V-to-1-V voltage conversion. The total SC stage conversion ratio is equal to the product of the two stages' SC step-down ratios. Therefore, the topology shown in Fig. 7.1 achieves a total SC stage conversion ratio of $(2 : 1) \times (8 : 1) = 16 : 1$; the topologies shown in Fig. 8.2 achieve a total SC stage conversion ratio of $(2 : 1) \times (10 : 1) = 20 : 1$.

10.2.2 Dickson-Squared (Dickson²) Converters

Another example is the Dickson-Squared (Dickson²) converter presented in Chapter 6. Fig. 10.3 shows the schematic drawing of a 9-to-1 Dickson² converter ($N = 3$, $K = 3$, and $M = 3$). Since the SC network in this converter can be viewed as two Dickson converters merged together with redundant components removed, it is given the name Dickson². In this converter, the two stages are merged through three switching buses $v_{\text{mid1}}-v_{\text{mid3}}$. The total SC stage conversion ratio is $(3 : 1) \times (3 : 1) = 9 : 1$.

It is worth noting that the Dickson² topology allows multiple choices for the two stages. For example, a 4-to-1 Dickson converter can be merged with four 2-to-1 series-capacitor buck modules (which can also be viewed as 2-to-1 Dickson converters), which yields the converter topology illustrated in Fig. 10.4 ($N = 4$, $K = 4$, and $M = 2$). The two stages are merged through four switching buses $v_{\text{mid1}}-v_{\text{mid4}}$. The total SC stage conversion ratio is $(4 : 1) \times (2 : 1) = 8 : 1$.

10.2.3 Series-Parallel-Dickson (SPD) Converter

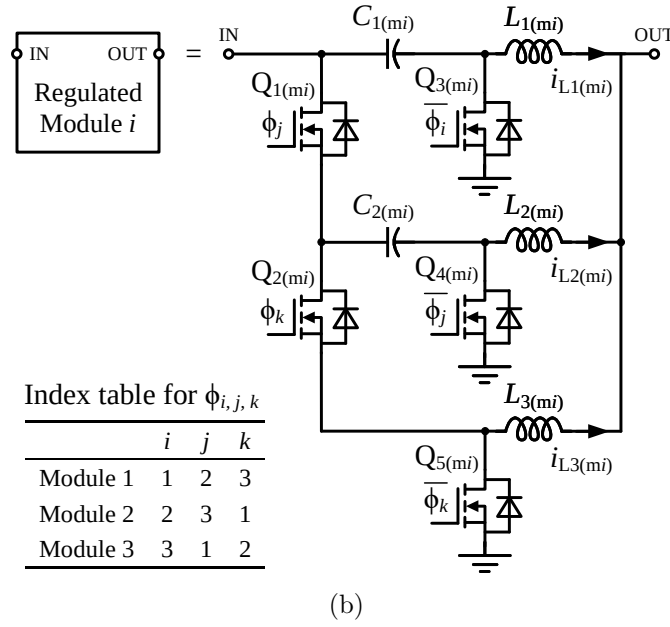
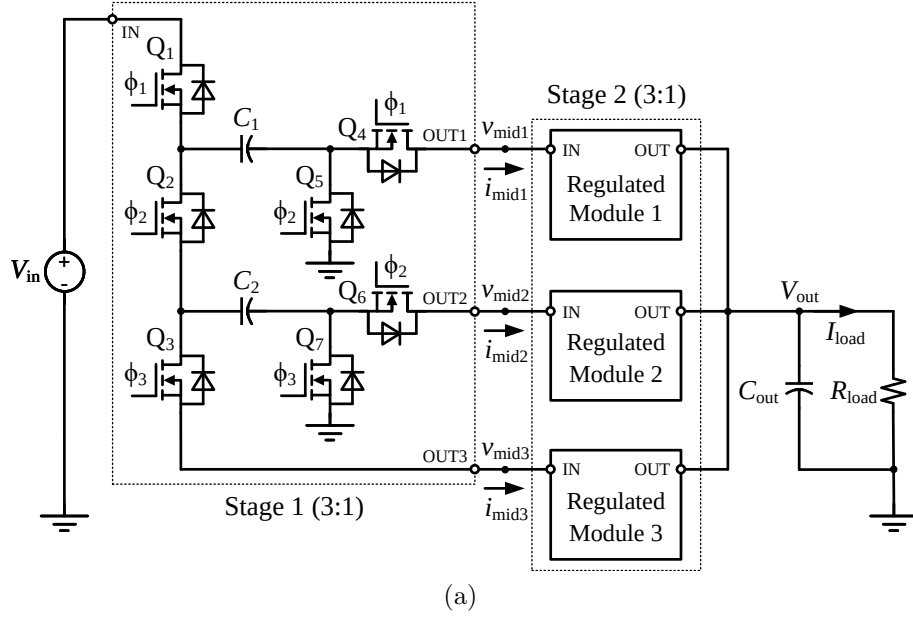
Fig. 10.5 shows the schematic drawing of a series-parallel-Dickson (SPD) converter ($N = 3$, $K = 3$, and $M = 3$). As illustrated in Fig. 10.5(a), the proposed topology consists of two stages. The first stage is a 3-to-1 series-parallel topology with three separate output terminals. The second stage is composed of three modules with the same circuit structure and cyclic control signals, as shown in Fig. 10.5(b). Inside each module is a three-phase series-capacitor buck converter, which can also be viewed as a 3-to-1 Dickson converter with the top switch moving to the bottom and the three output branches replaced by three inductors. The two stages are merged through three switching buses $v_{\text{mid1}}-v_{\text{mid3}}$. The total SC stage conversion ratio is $(3 : 1) \times (3 : 1) = 9 : 1$.

10.2.4 Cascaded Series-Parallel (CaSP) Converter

Fig. 10.6 shows the schematic drawing of the cascaded series-parallel (CaSP) converter presented in Chapter 5 ($N = 2$, $K = 1$, and $M = 3$). Its schematic drawing is the same as Fig. 5.1 but rearranged in the form of a two-stage switching-bus-based converter. It consists of two conversion stages. The first stage is a 2-to-1 SC front-end. The second stage is a 3-to-1 series-parallel converter. The two stages are merged through one switching bus v_{mid1} . The total SC stage conversion ratio is $(2 : 1) \times (3 : 1) = 6 : 1$.

10.2.5 Multi-Level-Binary (MLB) Converter

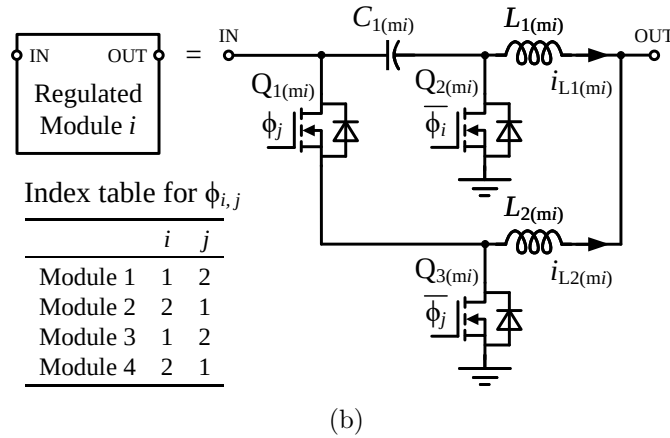
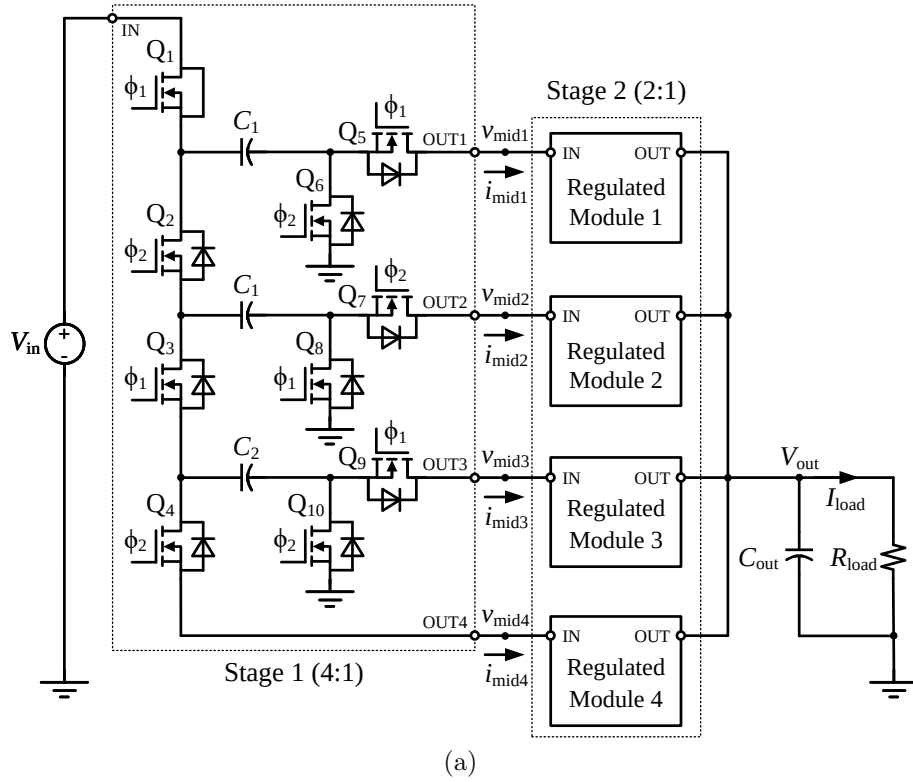
Fig. 10.7 shows the schematic drawing of the multi-level-binary (MLB) converter ($N = 4$, $K = 1$, and $M = 2$) proposed in [65]. It consists of two conversion stages. The first stage is a 4-to-1 series-parallel converter. The second stage is a 2-to-1 series-capacitor buck converter.



Index table for $\phi_{i,j,k}$

	i	j	k
Module 1	1	2	3
Module 2	2	3	1
Module 3	3	1	2

Figure 10.3: A Dickson² converter with $N = 3$, $K = 3$, and $M = 3$. (a) Overall schematic drawing. (b) Structure of Regulated Module i in Stage 2. The components labeled with the subscript (mi) are in Regulated Module i . The values of the label indexes (i , j , and k) for circuit components and control signals (ϕ_i , ϕ_j , and ϕ_k) in each module are listed in the index table.



Index table for $\phi_{i,j}$

	i	j
Module 1	1	2
Module 2	2	1
Module 3	1	2
Module 4	2	1

Figure 10.4: A Dickson² converter with $N = 4$, $K = 4$, and $M = 2$. (a) Overall schematic drawing. (b) Structure of Regulated Module i in Stage 2. The components labeled with the subscript (mi) are in Regulated Module i . The values of the label indexes (i , j , and k) for circuit components and control signals (ϕ_i , ϕ_j , and ϕ_k) in each module are listed in the index table.

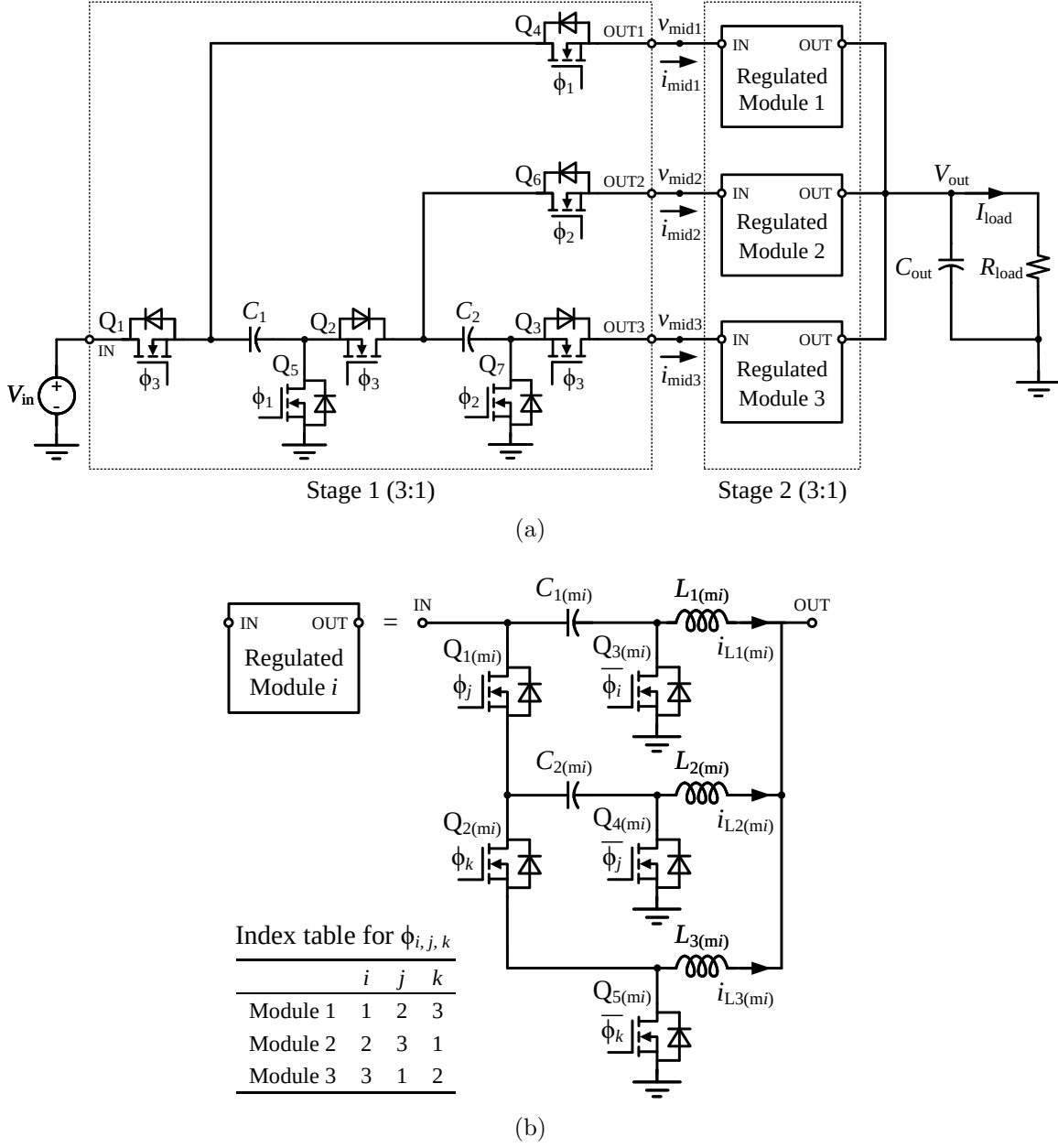


Figure 10.5: A series-parallel-Dickson (SPD) converter with $N = 3$, $K = 3$, and $M = 3$. (a) Overall schematic drawing. (b) Structure of Regulated Module i in Stage 2. The components labeled with the subscript (mi) are in Regulated Module i . The values of the label indexes (i , j , and k) for circuit components and control signals (ϕ_i , ϕ_j , and ϕ_k) in each module are listed in the index table.

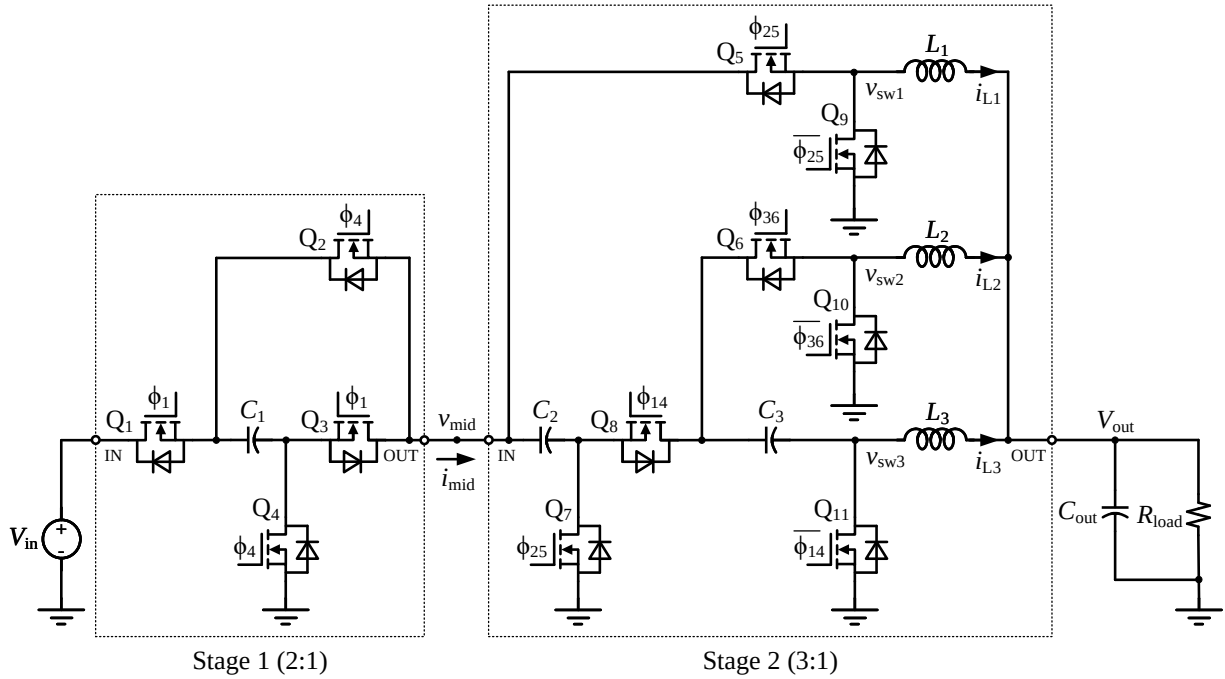


Figure 10.6: A cascaded series-parallel (CaSP) converter with $N = 2$, $K = 1$, and $M = 3$.

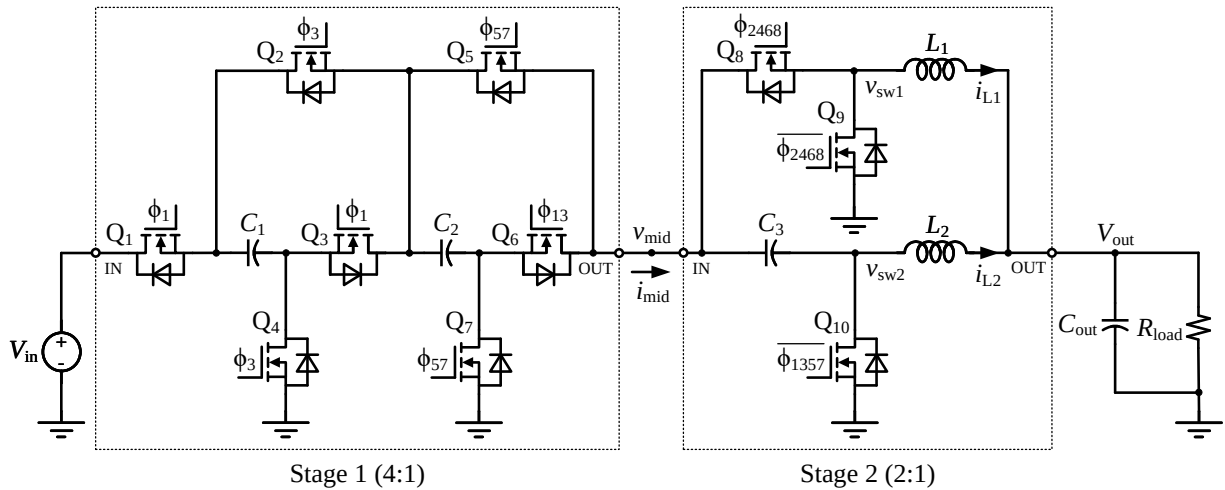


Figure 10.7: A multi-level-binary (MLB) converter with $N = 4$, $K = 1$, and $M = 2$.

The two stages are merged through one switching bus v_{mid1} . The total SC stage conversion ratio is $(4 : 1) \times (2 : 1) = 8 : 1$.

10.3 Multi-Stage Switching-Bus-Based Architecture

An example of this architecture is the switched-capacitor binary tree (SCBT) converter. Multiple different combinations of the SCBT converter can be implemented to achieve the same SC stage conversion ratio. For example, a 16-to-1 total SC stage conversion ratio can be factorized as

- Case 1: $16 : 1 = (2 : 1) \times (8 : 1)$
- Case 2: $16 : 1 = (2 : 1) \times (2 : 1) \times (4 : 1)$
- Case 3: $16 : 1 = (2 : 1) \times (2 : 1) \times (2 : 1) \times (2 : 1)$

Based on the switching bus concept, there are three different implementations of the SCBT converter to achieve a total SC stage conversion ratio of 16-to-1.

- Case 1: Fig. 10.8 illustrates a two-stage switched-capacitor binary tree (SCBT) converter. Stage 1 is a 2-to-1 SC converter. Stage 2 consists of two 8-to-1 series-capacitor buck (SCB) converters, as shown in Fig. 10.8(b). Stage 1 and Stage 2 are connected through two switching buses.
- Case 2: Fig. 10.9 illustrates a three-stage switched-capacitor binary tree (SCBT) converter. Stage 1 and Stage 2 consist of 2-to-1 SC converters. Stage 3 consists of four 4-to-1 series-capacitor buck (SCB) converters, as shown in Fig. 10.9. Stage 1 and Stage 2 are connected through two switching buses. Stage 2 and Stage 3 are connected through four switching buses.
- Case 3: Fig. 10.10 illustrates a four-stage switched-capacitor binary tree (SCBT) converter. Stage 1, Stage 2, and Stage 3 consist of 2-to-1 SC converters. Stage 4 consists of eight 2-to-1 series-capacitor buck (SCB) converters, as shown in Fig. 10.10. Stage 1 and Stage 2 are connected through two switching buses. Stage 2 and Stage 3 are connected through four switching buses. Stage 3 and Stage 4 are connected through eight switching buses.

10.4 Chapter Summary

This chapter synthesizes and extends the topologies and the switching bus concept proposed in previous chapters into a generalized switching-bus-based architecture for regulated hybrid switched-capacitor converters. Based on this generalized architecture, a family of regulated

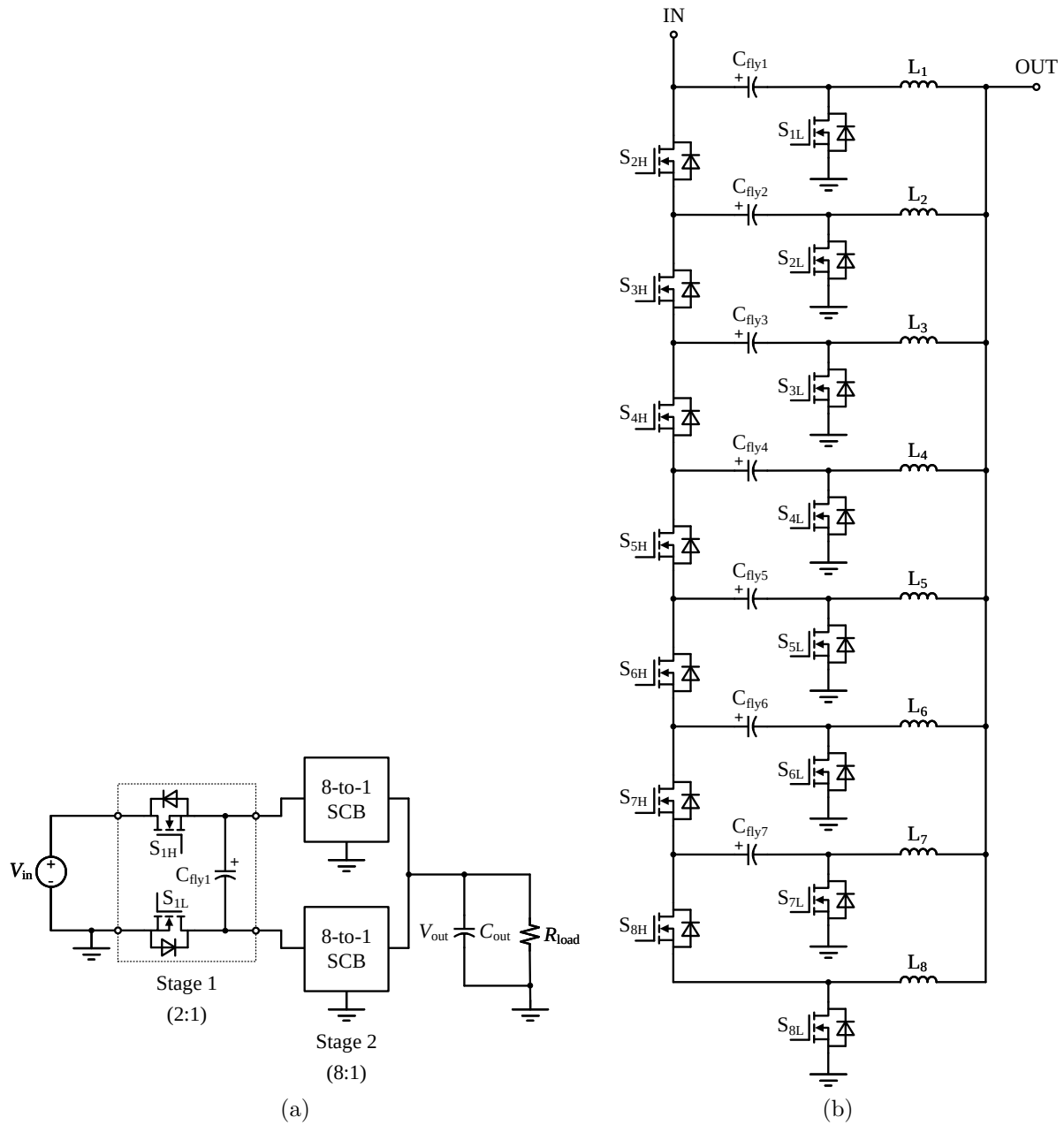


Figure 10.8: Example of a two-stage switched-capacitor binary tree (SCBT) converter. (a) Overall schematic drawing. (b) Structure of an 8-to-1 series-capacitor buck (SCB) module.

switching-bus-based topologies can be constructed by strategically merging two or multiple SC conversion stages.

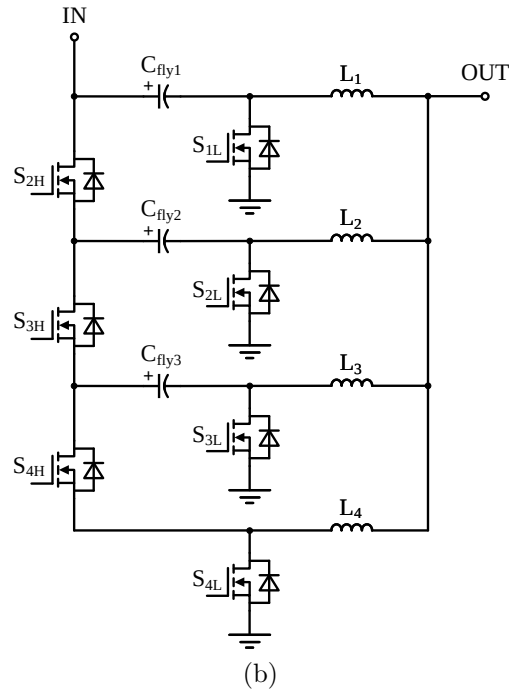
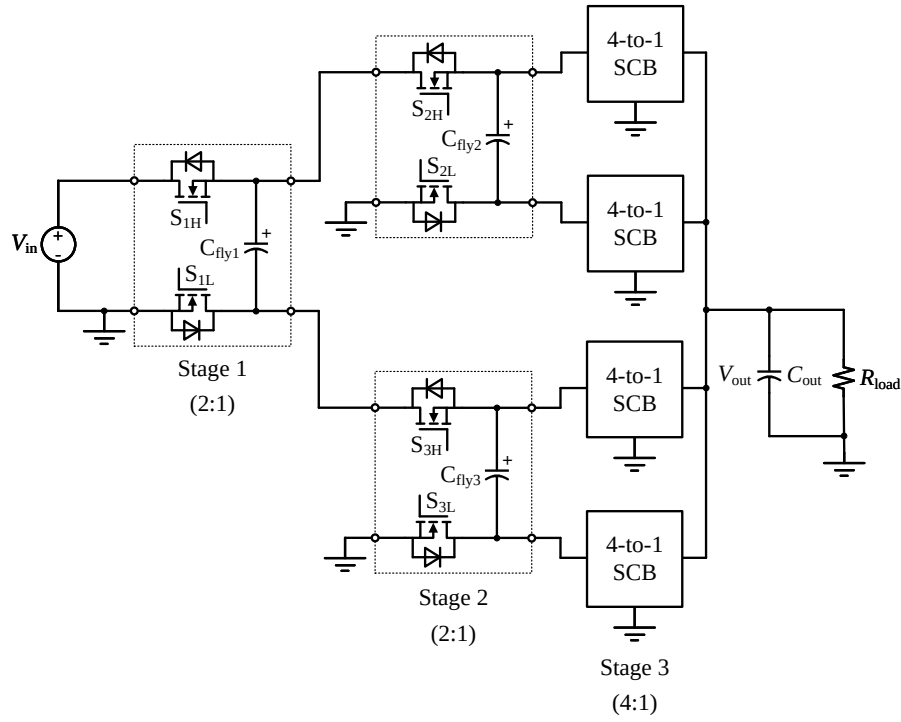


Figure 10.9: Example of a three-stage switched-capacitor binary tree (SCBT) converter. (a) Overall schematic drawing. (b) Structure of a 4-to-1 series-capacitor buck (SCB) module.

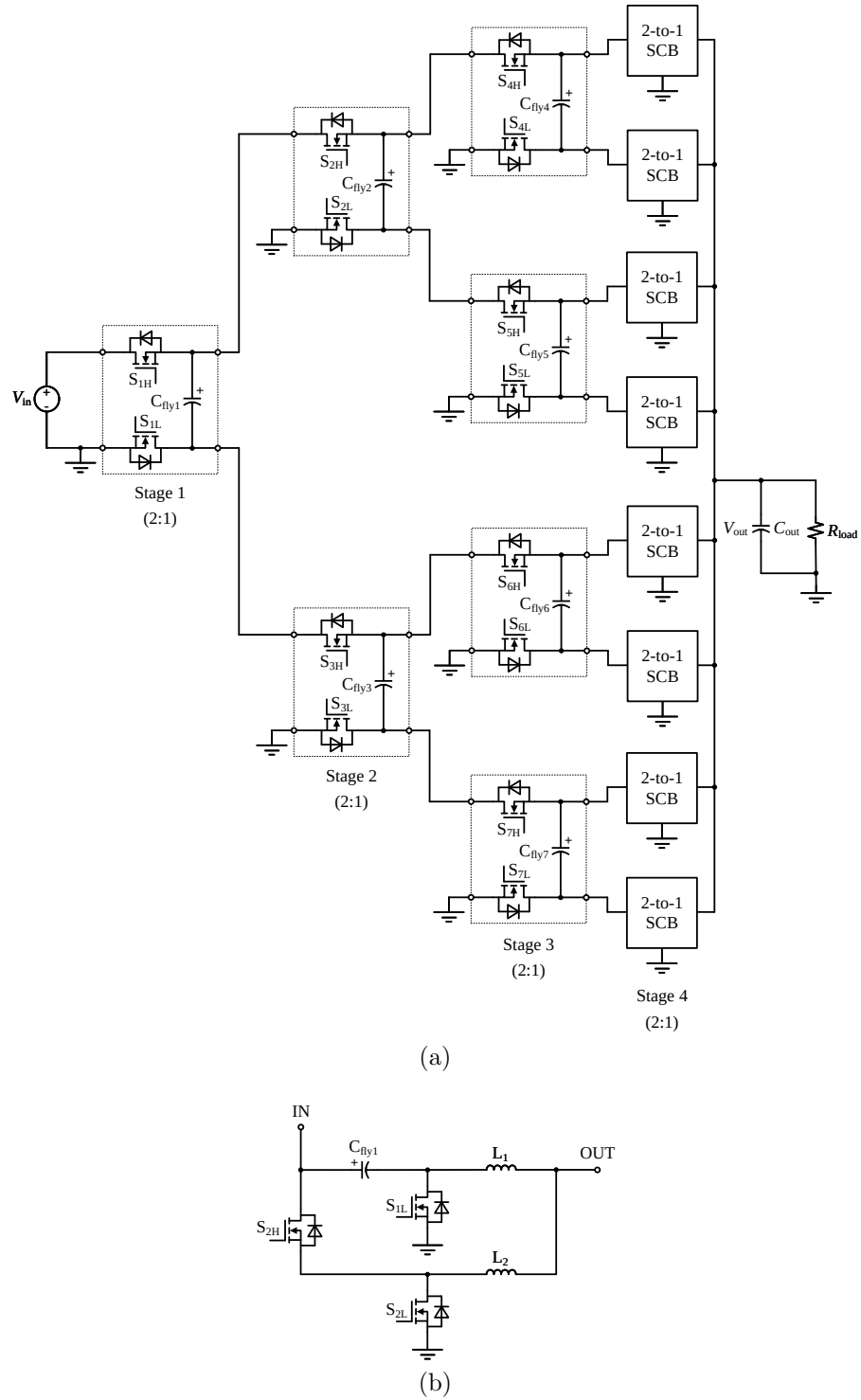


Figure 10.10: Example of a four-stage switched-capacitor binary tree (SCBT) converter. (a) Overall schematic drawing. (b) Structure of a 2-to-1 series-capacitor buck (SCB) module.

Chapter 11

Comparative Performance Analysis of Regulated Hybrid SC Topologies for Direct 48-V-to-PoL Conversion

11.1 Background and Motivation

Hybrid switched-capacitor (SC) converters have attracted increased attention for 48-V step-down conversion in data center [60, 62, 64–66, 70, 73–77, 81–84, 89, 96–98, 110–115, 119, 120, 123, 129–135] and automotive [136, 137] applications, due to their potential to provide improved solutions with higher efficiency and power density compared to conventional designs. As an emerging class of power converters, hybrid SC converters can leverage the greatly superior energy densities of capacitors compared to inductors [1], while simultaneously benefiting from the improved figures-of-merit (FOM) of low-voltage switching devices over high-voltage counterparts [4]. For unregulated, fixed-ratio voltage step-down applications (e.g., 48-V-to-12-V intermediate bus converters), various resonant switched-capacitor (ReSC) [62, 120, 132–134] and multi-resonant switched-capacitor (MRSC) [84, 135] converters operating at or above resonance have been proposed, demonstrating their advantages over existing dc-dc solutions, such as multi-phase buck converters [138] and LLC converters [139]. Previous studies [86, 140–142] have shown how to analyze and compare different ReSC topologies and strategically size the passive components in each topology to achieve optimal performance. Additionally, multiple regulated hybrid SC topologies [60, 64–66, 70, 73–77, 81–83, 89, 96–98, 110–115, 119, 123, 129–131] have been proposed for direct 48 V to point-of-load (PoL) conversion, particularly for 48-V voltage regulation modules (VRMs), where output voltage regulation is typically required. However, there is a lack of a method to theoretically compare the performance of regulated hybrid SC topologies, which could be useful for informing topology selection and converter design.

To fill this gap, this chapter aims to establish an analytical framework for the topological characterization and performance comparison of regulated hybrid SC topologies in

direct 48-V-to-PoL applications. In the proposed framework, each topology is captured with topology-dependent characteristic vectors, which are then utilized to calculate three metrics for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. Building on our previous conference paper [85], this chapter provides an additional comparative analysis of transient performance, as well as in-depth discussions on the comparison results. Based on this analytical framework, a comprehensive comparative analysis reveals that increasing the SC stage conversion ratio can reduce switch stress and passive component volume while speeding up the falling slew rate of the total inductor current, thereby improving efficiency, power density, and load step-down transient performance at the same time. Although a larger SC conversion ratio typically slows down the rising slew rate of the total inductor current, potentially impairing the load step-up transient performance, a converter with a larger SC conversion ratio can be properly designed to achieve balanced load step-up and step-down transient performance.

The remainder of this chapter is organized as follows: Section 11.2 provides a general representation of regulated hybrid SC topologies consisting of a fixed-ratio SC stage and a regulated buck-type stage. Section 11.3 introduces the analytical framework with the three metrics for performance comparison, including a formalized analysis procedure using topology-dependent characteristic vectors. Based on the proposed framework, Section 11.4 conducts a comparative analysis of the state-of-the-art 48-V-to-PoL regulated hybrid SC topologies and demonstrates the benefits of a larger SC stage conversion ratio. Finally, Section 11.5 concludes this chapter.

11.2 General Representation of Regulated Hybrid SC Topologies

A regulated hybrid SC topology can be captured by the general representation depicted in Fig. 11.1. It consists of two stages: 1) a fixed-ratio SC stage for efficient and compact voltage conversion and 2) a regulated buck-type stage for the remainder of the voltage conversion task and output voltage regulation. Moreover, when designed properly, the buck-type stage serves as an inductive load to the preceding SC stage, ensuring complete soft-charging operation. It should be noted that a distinctive feature of high-performance hybrid SC topologies is that the two stages are not independent; instead, their operations are merged to achieve improved performance [143]. Additionally, although the buck-type stage can regulate the output voltage with duty cycle control and achieve multi-phase interleaving similar to a buck converter, it does not necessarily require dedicated pull-up switches due to its strategic merging with the preceding SC stage.

As is consistent with all previously cited works, this analysis considers only topologies where all switch-node voltages in Fig. 11.1 ($v_{sw,1}, v_{sw,2}, \dots, v_{sw,N_L}$, where N_L denotes the

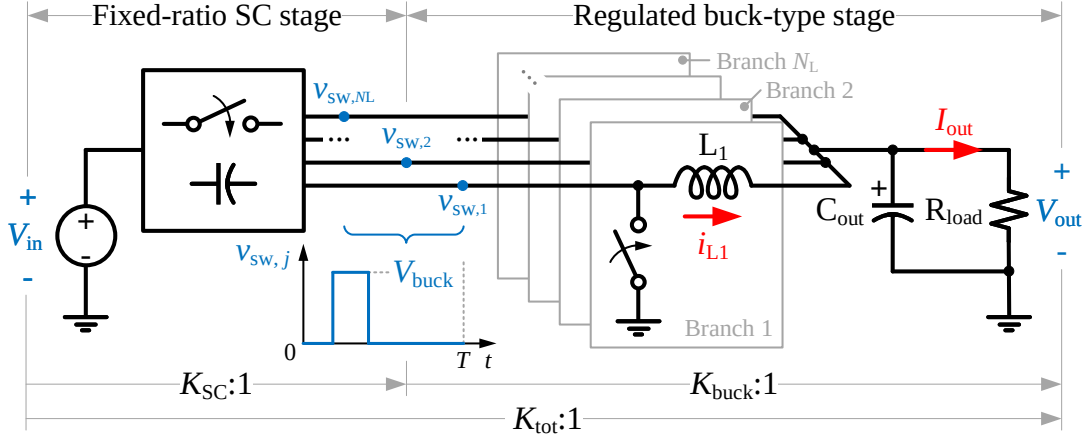


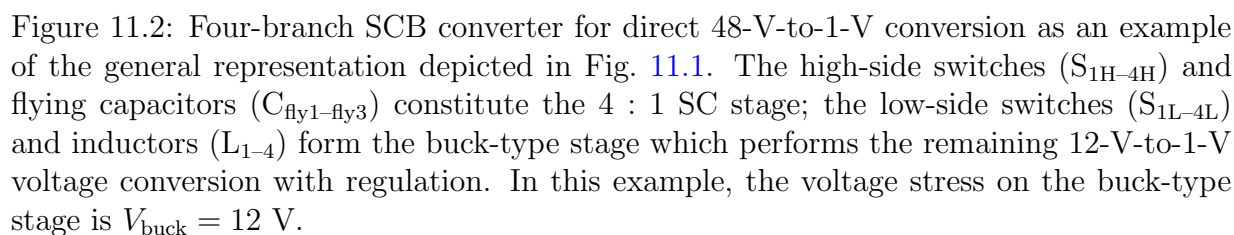
Figure 11.1: General representation of a regulated hybrid switched-capacitor (SC) topology consisting of a fixed-ratio SC stage and a regulated buck-type stage. The input voltage (V_{in}) is first stepped down to V_{buck} by the SC stage. The buck-type stage then performs the remaining voltage conversion from V_{buck} to the output voltage (V_{out}) with regulation. The total conversion ratio $K_{tot} : 1$ is allocated between the SC stage and the buck-type stage.

total number of inductors) switch between the same two voltage levels: V_{buck} and 0. V_{buck} is the highest voltage that the buck-type stage experiences (ignoring flying capacitor voltage ripples), thereby defined as the voltage stress on the buck-type stage. The input voltage (V_{in}) is first stepped down to V_{buck} by the SC stage, where V_{buck} can be calculated as

$$V_{buck} = \frac{V_{in}}{K_{SC}}, \quad (11.1)$$

and K_{SC} is the SC stage conversion ratio, also interchangeably referred to as the SC step-down ratio. The buck-type stage then performs the remaining voltage conversion from V_{buck} to the output voltage (V_{out}) with regulation. Fig. 11.2 illustrates a four-branch series-capacitor buck (SCB) converter as an example of the general representation depicted in Fig. 11.1, where $V_{in} = 48$ V and $V_{out} = 1$ V. The high-side switches (S_{1H-4H}) and flying capacitors ($C_{fly1-fly3}$) constitute the SC stage with a step-down ratio of 4:1 ($K_{SC} = 4$). According to (11.1), the voltage stress on the buck-type stage can be obtained as $V_{buck} = 12$ V. The buck-type stage, consisting of the low-side switches (S_{1L-4L}) and inductors (L_{1-4}), completes the remaining 12-V-to-1-V voltage conversion ($K_{buck} = 12$) with regulation.

Since the total conversion ratio (K_{tot}), defined as $K_{tot} = V_{in}/V_{out}$, is allocated between the SC stage and the buck-type stage, if the SC stage achieves a larger step-down ratio (K_{SC}), the voltage conversion burden on the buck-type stage (K_{buck}) can be reduced. At the same output voltage, buck converters with lower step-down ratios typically require smaller inductors and achieve higher efficiency. Given that magnetic components typically dominate



the volume of power converters, it is favorable to design the SC stage to take on more voltage conversion burden so that the inductor volume of the buck-type stage can be reduced.

Although it is clear that a larger SC stage conversion ratio (K_{SC}) benefits the buck-type stage, there is still a concern that increasing K_{SC} can impair overall efficiency. This is because achieving a larger SC step-down ratio generally requires more switching devices, which can lead to higher conduction and switching losses. Moreover, higher-order SC networks typically require more flying capacitors, potentially offsetting the inductor volume reduction seen in the buck-type stage. These concerns are addressed in the following sections.

11.3 Analytical Framework for Topological Characterization and Performance Comparison

The proposed analytical framework focuses on three metrics for performance comparison: a) normalized switch stress (M_S) as an indicator of efficiency, b) normalized passive component volume (M_P) as an indicator of power density, and c) normalized falling and rising slew rates ($\widehat{SR}_F$ and $\widehat{SR}_R$) of the total inductor current as indicators of transient performance. This section first discusses the key assumptions of the proposed framework, then provides the definitions and derivations of the three metrics, and finally introduces a formalized analytical procedure using topology-dependent characteristic vectors.

11.3.1 Key Assumptions

The proposed analytical framework is based on the following assumptions:

- *Small-ripple approximation:* It is selectively assumed that the magnitude of the switching ripple is much smaller than the dc component of capacitor voltages and inductor currents, which enables three subsequent assumptions:
 - In the analysis of normalized switch stress, inductor current ripples and capacitor voltage ripples are assumed to be negligible.
 - In the analysis of normalized passive component volume (where ripple cannot meaningfully be ignored), inductor current ripples and capacitor voltage ripples are assumed to be piecewise linear. In other words, capacitor voltage ripples are assumed to be negligible in inductor volume analysis, and inductor current ripples are assumed to be negligible in capacitor volume analysis.
 - In the analysis of normalized total inductor current slew rate, all capacitor voltage ripples (including the output voltage ripple) are again assumed to be negligible.
- *Uniform ripple ratios:* Ripple ratios of all inductor currents (α_I) are assumed to be the same. Ripple ratios of all capacitor voltages (α_V) are assumed to be the same.

- *Lossless energy transfer:* Duty ratio is calculated based on the assumption that the converter is lossless with no requirement for output voltage droop compensation.
- *Uniform energy density:* All inductors are assumed to have the same volumetric energy density ($\rho_{E,L}$). All capacitors are assumed to have the same volumetric energy density ($\rho_{E,C}$).

The symbols used in this framework are defined in Table 11.1. Later symbols with the hat notation ($\hat{\cdot}$) are normalized values with respect to their base values listed in Table 11.2.

11.3.2 Normalized Switch Stress

The normalized switch stress (M_S) is defined as the total switch stress normalized to the output power

$$M_S = \frac{\sum_{\text{switches}} V_{ds,i} I_{d(\text{rms}),i}}{V_{\text{out}} I_{\text{out}}} = \underbrace{\frac{V_{\text{in}}}{V_{\text{out}}}}_{K_{\text{tot}}} \cdot \sum_{i=1}^{N_S} \underbrace{\frac{V_{ds,i}}{V_{\text{in}}}}_{\hat{V}_{ds,i}} \cdot \underbrace{\frac{I_{d(\text{rms}),i}}{I_{\text{out}}}}_{\hat{I}_{d(\text{rms}),i}} = K_{\text{tot}} \sum_{i=1}^{N_S} \hat{V}_{ds,i} \hat{I}_{d(\text{rms}),i}, \quad (11.2)$$

where $V_{ds,i}$ is the peak blocking voltage across switch i when assuming no capacitor voltage ripple, and $I_{d(\text{rms}),i}$ is the root mean square (RMS) value of the current flowing through switch i when assuming no inductor current ripple.

The normalized switch stress M_S indicates how much volt-ampere (VA) stress the switches in a topology experience when transferring one per-unit watt of power from the input to the output. It commonly serves as a proxy for switching device losses or semiconductor areas in a topology [86, 140, 142, 144]. A lower M_S is desirable, as it indicates lower switching and conduction losses, thus contributing to higher efficiency. In addition, a lower M_S indicates smaller switching device areas, which is favorable to higher power density.

11.3.3 Normalized Passive Component Volume

The normalized passive component volume (M_P) is defined as the total passive component volume normalized to the base volume and is the sum of the normalized inductor volume and the normalized capacitor volume

$$M_P = \frac{\text{Vol}_{\text{tot}}}{\text{Vol}_{\text{base}}} = \frac{\sum_{\text{inductors}} \text{Vol}_{L,j} + \sum_{\text{capacitors}} \text{Vol}_{C,k}}{\text{Vol}_{\text{base}}} = \sum_{j=1}^{N_L} \hat{\text{Vol}}_{L,j} + \sum_{k=1}^{N_C} \hat{\text{Vol}}_{C,k}, \quad (11.3)$$

where the base value for volume is

$$\text{Vol}_{\text{base}} = \frac{V_{\text{out}} I_{\text{out}} T}{\rho_{E,L}}. \quad (11.4)$$

Table 11.1: Symbol definitions

Symbol	Definition
N_S	Total number of switching devices
N_L	Total number of inductors
N_C	Total number of flying capacitors
V_{in}	Input voltage (base value for voltage)
V_{buck}	Buck-type stage input voltage (illustrated in Fig. 11.1)
V_{out}	Output voltage
I_{out}	Total output current (base value for current)
K_{tot}	Total conversion ratio ($K_{tot} = V_{in}/V_{out}$)
K_{SC}	SC stage conversion ratio ($K_{SC} = V_{in}/V_{buck}$)
K_{buck}	Buck-type stage conversion ratio ($K_{buck} = V_{buck}/V_{out}$)
$V_{ds,i}$	Peak blocking voltage across switch i
$I_{d(rms),i}$	RMS value of the current through switch i
Vol_{tot}	Total passive component volume
$Vol_{L,j}$	Volume of inductor j
$Vol_{C,k}$	Volume of capacitor k
L_j	Value of inductor j
$I_{L,j}$	Average current of inductor j
$\Delta i_{L,j,pp}$	Peak-to-peak current ripple of inductor j
T	Switching period of the buck-type stage
D	Duty ratio of the buck-type stage
D_{max}	Maximum duty ratio of the buck-type stage
$E_{L,j,peak}$	Peak energy stored in inductor j
C_k	Value of capacitor k
$V_{C,k}$	Mid-range voltage of capacitor k
$\Delta v_{C,k,pp}$	Peak-to-peak voltage ripple of capacitor k
$q_{C,k}$	Total charge contained in the positive portion of capacitor k 's current waveform in one switching cycle
$E_{C,k,peak}$	Peak energy stored in capacitor k
α_I	Inductor current ripple ratio ($\alpha_I = \Delta i_{L,j,ap}/I_{L,j}$)
α_V	Capacitor voltage ripple ratio ($\alpha_V = \Delta v_{C,k,ap}/V_{C,k}$)
$\rho_{E,L}$	Volumetric energy density of inductors
$\rho_{E,C}$	Volumetric energy density of flying capacitors
β	Energy density ratio of capacitors to inductors ($\beta = \rho_{E,C}/\rho_{E,L}$)
$SR_{F,j}$	Maximum current falling rating of inductor j
SR_F	Maximum total inductor current falling rate
$SR_{R,j}$	Maximum current rising rating of inductor j
SR_R	Maximum total inductor rising rate

Table 11.2: Base values for normalization

Quantity	Voltage	Current	Charge	Volume	Current Slew Rate
Base value	V_{in}	I_{out}	$I_{\text{out}}T$	$\frac{V_{\text{out}}I_{\text{out}}T}{\rho_{\text{E,L}}}$	$\frac{2\alpha_I I_{\text{out}}}{T}$

Parameter $\rho_{\text{E,L}}$ is the volumetric energy density of inductors, and T is the converter switching period. The normalized passive component volume (M_{P}) indicates the total passive component volume needed to meet the given ripple requirements on the inductor currents and flying capacitor voltages when transferring one per-unit watt of power from the input to the output. A smaller normalized passive component volume is desirable, as it indicates higher power density.

This work adopts an energy-based approach to passive component volume assessment by analyzing the peak energy stored in each passive component [86, 142]. To determine the total passive component volume that a topology requires, this section first finds the minimum inductor and capacitor values that can meet chosen current and voltage ripple requirements and then calculates the peak energy stored in the passive components.

11.3.3.1 Normalized Inductor Volume

Define the current ripple ratio (α_I) for inductor j as the ratio of the peak current ripple amplitude to the average inductor current:

$$\alpha_I = \frac{\frac{1}{2}\Delta i_{\text{L},j,\text{pp}}}{I_{\text{L},j}}, \quad (11.5)$$

where $I_{\text{L},j}$ and $\Delta i_{\text{L},j,\text{pp}}$ are the average inductor current and peak-to-peak inductor current ripple, respectively, as annotated in Fig. 11.3. In this analysis, ripple ratios of all inductor currents are assumed to be the same.

By integrating the inductor's current-voltage relation over $t \in [DT, T]$, we can obtain the peak-to-peak inductor current ripple as

$$\Delta i_{\text{L},j,\text{pp}} = \frac{V_{\text{out}}}{L_j} (1 - D) T, \quad (11.6)$$

where D is the duty ratio of the buck-type stage. Based on the assumption of lossless energy transfer, D can be calculated as

$$D = \frac{1}{K_{\text{buck}}} = \frac{K_{\text{SC}}}{K_{\text{tot}}}. \quad (11.7)$$

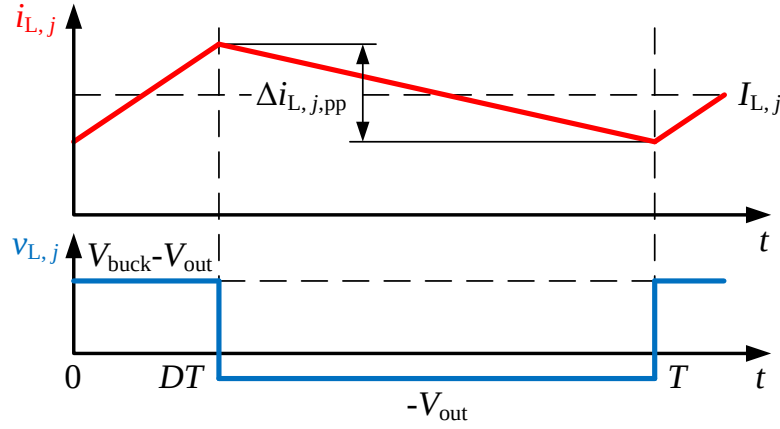


Figure 11.3: Current (top, red) and voltage (bottom, blue) waveforms of inductor j . $I_{L,j}$ and $\Delta i_{L,j,pp}$ are the average inductor current and peak-to-peak inductor current ripple, respectively. The voltage applied across the inductor jumps between $V_{\text{buck}} - V_{\text{out}}$ and $-V_{\text{out}}$.

We can obtain the minimum inductor value required to meet the chosen current ripple requirement (α_I) by substituting (11.5) and (11.7) into (11.6), which yields

$$L_j = \frac{V_{\text{out}} T}{2\alpha_I I_{L,j}} \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right). \quad (11.8)$$

Therefore, the peak energy stored in the inductor is

$$\begin{aligned} E_{L,j,\text{peak}} &= \frac{1}{2} L_j \left(I_{L,j} + \frac{1}{2} \Delta i_{L,j,pp} \right)^2 \\ &= \frac{1}{2} (1 + \alpha_I)^2 L_j I_{L,j}^2. \end{aligned} \quad (11.9)$$

Substituting (11.8) into (11.9) yields the required inductor volume

$$\text{Vol}_{L,j} = \frac{E_{L,j,\text{peak}}}{\rho_{E,L}} = \frac{(1 + \alpha_I)^2 V_{\text{out}} I_{L,j} T}{4\alpha_I \rho_{E,L}} \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right). \quad (11.10)$$

Using the base value for volume in (11.4), we can obtain the normalized inductor volume as

$$\widehat{\text{Vol}}_{L,j} = \frac{\text{Vol}_{L,j}}{\text{Vol}_{\text{base}}} = \frac{(1 + \alpha_I)^2}{4\alpha_I} \cdot \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right) \cdot \underbrace{\frac{I_{L,j}}{I_{\text{out}}}}_{\hat{I}_{L,j}} = \frac{(1 + \alpha_I)^2}{4\alpha_I} \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right) \hat{I}_{L,j}. \quad (11.11)$$

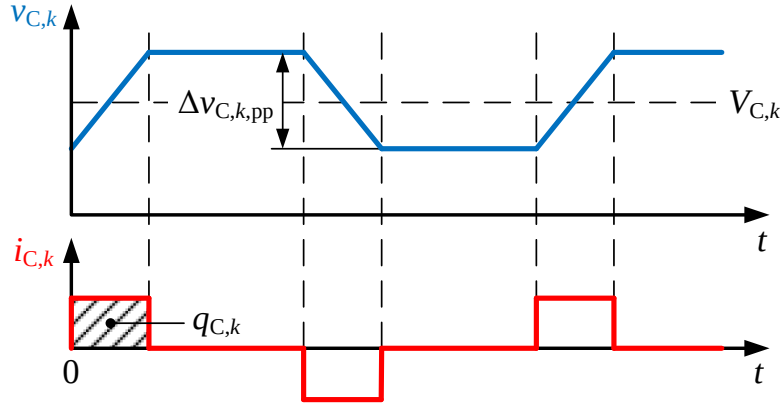


Figure 11.4: Voltage (top, blue) and current (bottom, red) waveforms of capacitor k (C_k). $V_{C,k}$ and $\Delta v_{C,k,pp}$ are the mid-range capacitor voltage and peak-to-peak capacitor voltage ripple, respectively. $q_{C,k}$ is the total charge contained in the positive portion of the capacitor current waveform per switching cycle and is illustrated as the shaded area. If a capacitor is charged multiple times before discharged, all charges flowing into the capacitor should be added up when calculating $q_{C,k}$.

11.3.3.2 Normalized Capacitor Volume

Define the voltage ripple ratio (α_V) for capacitor k as the ratio of the peak voltage ripple amplitude to the mid-range capacitor voltage:

$$\alpha_V = \frac{\frac{1}{2}\Delta v_{C,k,pp}}{V_{C,k}}, \quad (11.12)$$

where $V_{C,k}$ and $\Delta v_{C,k,pp}$ are the mid-range capacitor voltage and peak-to-peak capacitor voltage ripple, respectively, as annotated in Fig. 11.4. The *mid-range* voltage is the average of the maximum and minimum values of the capacitor voltage waveform and is distinct from the time-averaged or dc voltage of a capacitor whose voltage waveform does not have a 50% duty cycle [145]. In this analysis, ripple ratios of all capacitor voltages are assumed to be the same.

Illustrated as the shaded area on the capacitor current waveform in Fig. 11.4, $q_{C,k}$ represents the total charge contained in the positive portion of the capacitor current waveform per switching cycle. The peak-to-peak capacitor voltage ripple can be obtained as

$$\Delta v_{C,k,pp} = \frac{q_{C,k}}{C_k}. \quad (11.13)$$

We can obtain the minimum capacitor value required to meet the chosen voltage ripple requirement (α_V) by substituting (11.12) into (11.13), which yields

$$C_k = \frac{q_{C,k}}{2\alpha_V V_{C,k}}. \quad (11.14)$$

Thus, the peak energy stored in the capacitor is

$$E_{C,k,\text{peak}} = \frac{1}{2}C_k \left(V_{C,k} + \frac{1}{2}\Delta v_{C,k,\text{pp}} \right)^2 = \frac{1}{2}(1 + \alpha_V)^2 C_k V_{C,k}^2. \quad (11.15)$$

Substituting (11.14) into (11.15) yields the capacitor volume

$$\text{Vol}_{C,k} = \frac{E_{C,k,\text{peak}}}{\rho_{E,C}} = \frac{(1 + \alpha_V)^2 V_{C,k} q_{C,k}}{4\alpha_V \rho_{E,C}}, \quad (11.16)$$

where $\rho_{E,C}$ is the volumetric energy density of capacitors.

Using the base value for volume in (11.4), we can obtain the normalized capacitor volume as

$$\widehat{\text{Vol}}_{C,k} = \frac{\text{Vol}_{C,k}}{\text{Vol}_{\text{base}}} = \frac{(1 + \alpha_V)^2}{4\alpha_V} \cdot \underbrace{\frac{\rho_{E,L}}{\rho_{E,C}}}_{1/\beta} \cdot \underbrace{\frac{V_{\text{in}}}{V_{\text{out}}}}_{K_{\text{tot}}} \cdot \underbrace{\frac{V_{C,k}}{V_{\text{in}}}}_{\widehat{V}_{C,k}} \cdot \underbrace{\frac{q_{C,k}}{I_{\text{out}}T}}_{\widehat{q}_{C,k}} = \frac{(1 + \alpha_V)^2}{4\alpha_V \beta} K_{\text{tot}} \widehat{V}_{C,k} \widehat{q}_{C,k}, \quad (11.17)$$

where β is the ratio of the energy density of capacitors to that of inductors

$$\beta = \frac{\rho_{E,C}}{\rho_{E,L}}. \quad (11.18)$$

11.3.3.3 Normalized Passive Component Volume

Summing the normalized volumes over all inductors and capacitors by substituting (11.11) and (11.17) into (11.3) yields

$$M_P = \sum_{j=1}^{N_L} \frac{(1 + \alpha_I)^2}{4\alpha_I} \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right) \widehat{I}_{L,j} + \sum_{k=1}^{N_C} \frac{(1 + \alpha_V)^2}{4\alpha_V \beta} K_{\text{tot}} \widehat{V}_{C,k} \widehat{q}_{C,k}. \quad (11.19)$$

Applying Kirchhoff's current law (KCL), we can obtain

$$\sum_{j=1}^{N_L} \widehat{I}_{L,j} = \frac{1}{I_{\text{out}}} \sum_{j=1}^{N_L} I_{L,j} = 1, \quad (11.20)$$

which can be used to simplify (11.19) as

$$M_P = \frac{(1 + \alpha_I)^2}{4\alpha_I} \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right) + \frac{(1 + \alpha_V)^2}{4\alpha_V \beta} K_{\text{tot}} \sum_{k=1}^{N_C} \widehat{V}_{C,k} \widehat{q}_{C,k}. \quad (11.21)$$

Note that the derivation of M_P does not rely on balanced inductor currents (i.e., $I_{L,1} = I_{L,2} = \dots = I_{L,N_L}$). Instead, the final expression for M_P , as shown in (11.21), applies to topologies where inductor currents are not equal, since the KCL relationship in (11.20) always holds.

11.3.4 Normalized Total Inductor Current Slew Rate

Fast dynamic response to load transients is typically required for PoL power converters. When a step change in the load current occurs, the maximum inductor current slew rate determines the fastest response a converter can achieve to recover the output voltage, regardless of the control scheme. Therefore, it represents the physical limit of a converter's transient performance. In the proposed framework, the falling and rising slew rates of the total inductor current are chosen as indicators of transient performance for comparative analysis.

11.3.4.1 Normalized Total Inductor Current Falling Rate

Fig. 11.5 illustrates the key waveforms of a regulated hybrid SC converter, as shown in Fig. 11.1, during a load step-down transient. The load transient begins at t_0 when the load current (i_{out}) suddenly drops. The output voltage (v_{out}) reaches its peak at t_1 when the inductor current ($i_{L,j}$) crosses the load current flowing through branch j ($i_{\text{out},j}$); it recovers to the reference value (V_{out}) at t_2 . Note that although the output voltage overshoot ($V_{\text{out(max)}} - V_{\text{out}}$) is exaggerated in Fig. 11.5 for clear illustration, it is assumed to be much smaller than V_{out} .

The fastest way of recovering v_{out} during the load step-down transient is by grounding all switch nodes and allowing the inductor currents to fall at the maximum rate. The maximum total inductor current falling rate (SR_{F}) represents the physical limit of a topology's performance during load step-down transients. Therefore, SR_{F} is chosen as a metric to compare the transient performance of different topologies. To derive SR_{F} , we first need to obtain the maximum inductor current falling rate for each branch ($\text{SR}_{\text{F},j}$) and then sum them up. Assuming the output voltage overshoot is much smaller than the nominal output voltage (V_{out}) due to the existence of the large output capacitor (C_{out}), the maximum current falling rate of inductor j ($\text{SR}_{\text{F},j}$) can be approximated as

$$\text{SR}_{\text{F},j} = \frac{V_{\text{out}}}{L_j}, \quad (11.22)$$

which can be rewritten as

$$\text{SR}_{\text{F},j} = \frac{K_{\text{tot}}}{K_{\text{tot}} - K_{\text{SC}}} \cdot \frac{2\alpha_{\text{I}} I_{L,j}}{T} \quad (11.23)$$

with the expression for L_j in (11.8) substituted into (11.22). It can be normalized to the base value of current slew rates listed in Table 11.2 (i.e., $\text{SR}_{\text{base}} = 2\alpha_{\text{I}} I_{\text{out}}/T$) as

$$\widehat{\text{SR}}_{\text{F},j} = \frac{\text{SR}_{\text{F},j}}{\text{SR}_{\text{base}}} = \frac{\text{SR}_{\text{F},j}}{2\alpha_{\text{I}} I_{\text{out}}/T} = \frac{K_{\text{tot}}}{K_{\text{tot}} - K_{\text{SC}}} \widehat{I}_{L,j} \quad (11.24)$$

Therefore, the normalized total inductor current falling rate can be obtained using the KCL relationship in (11.20) as

$$\widehat{\text{SR}}_{\text{F}} = \sum_{j=1}^{N_{\text{L}}} \widehat{\text{SR}}_{\text{F},j} = \frac{K_{\text{tot}}}{K_{\text{tot}} - K_{\text{SC}}}. \quad (11.25)$$

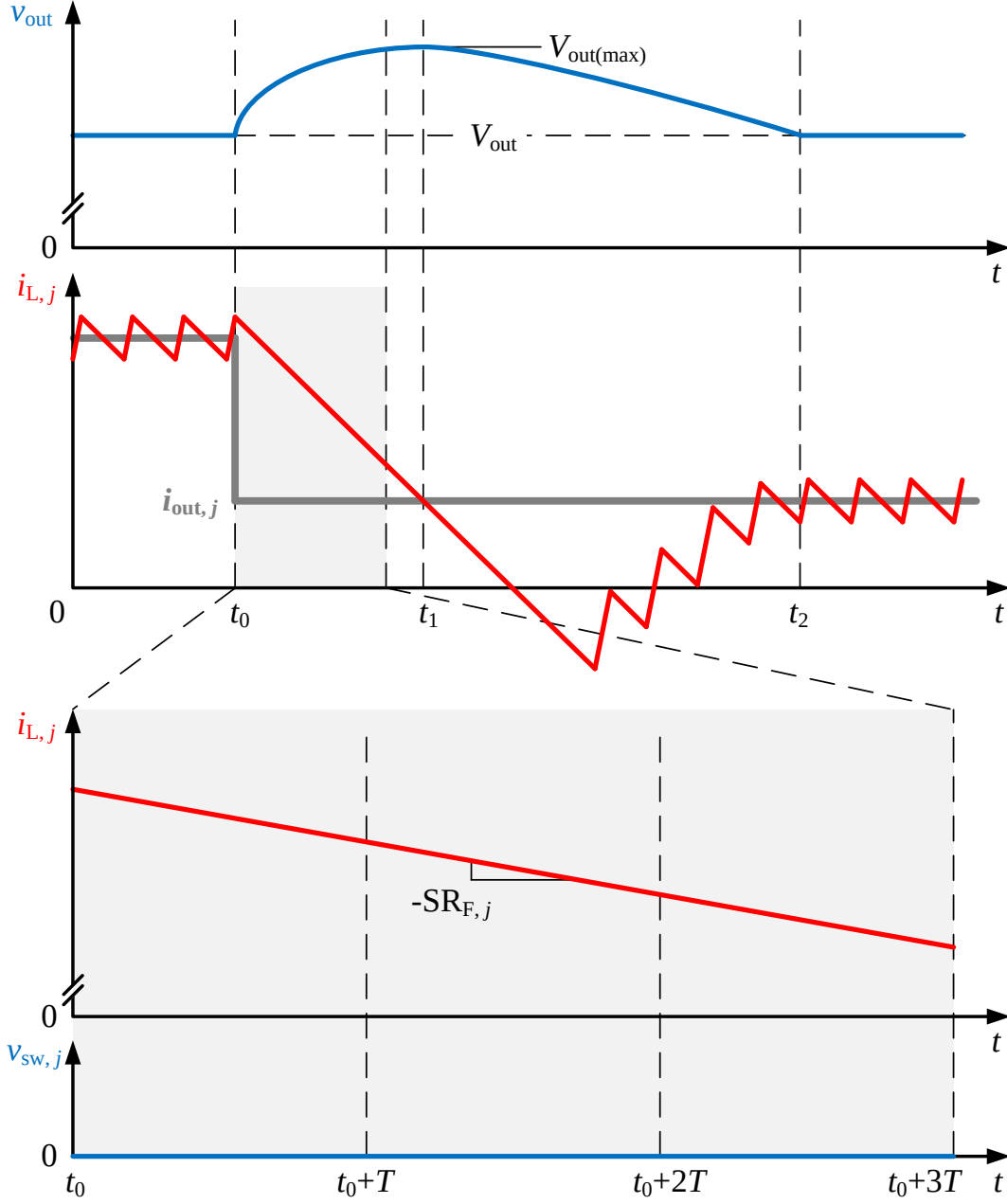


Figure 11.5: Load step-down transient waveforms of branch j . From top to bottom: the output voltage waveform (v_{out}), the waveforms of the current flowing through inductor j ($i_{L,j}$) and the load current flowing through branch j ($i_{out,j}$), the zoomed-in waveform of the inductor current over three switching cycles, and the switch-node voltage waveform seen by inductor j ($v_{sw,j}$). The fastest way of recovering v_{out} to the reference value (V_{out}) is by grounding all switch nodes and allowing the inductor currents to fall at the maximum rate.

Since K_{tot} is a constant determined by the application, $\widehat{\text{SR}}_{\text{F}}$ is a function of the SC stage conversion ratio (K_{SC}) only.

11.3.4.2 Normalized Total Inductor Current Rising Rate

Fig. 11.6 depicts the load step-up transient waveforms of a regulated hybrid SC converter. Similar to the load step-down transient illustrated in Fig. 11.5, this load step-up transient begins at t_0 when the load current (i_{out}) suddenly increases. The output voltage reaches its valley ($V_{\text{out}(\min)}$) at t_1 when the inductor current crosses the per-branch load current ($i_{\text{out}}/N_{\text{L}}$); it recovers to the reference value (V_{out}) at t_2 . The output voltage undershoot ($V_{\text{out}} - V_{\text{out}(\min)}$) is assumed to be much smaller than V_{out} , although it is exaggerated in Fig. 11.6 for clear illustration.

The fastest way of recovering v_{out} is by operating all branches at the maximum duty ratio (D_{max}) and forcing the inductor currents to rise at the maximum rate. Unlike the conventional multi-phase buck converter, many regulated hybrid SC topologies have an upper limit on the achievable duty ratio. For, example, the SCB converter with multi-phase operation shown in Fig. 11.2 has a maximum duty ratio of $1/N_{\text{L}}$. A discussion of how this upper limit on the duty ratio affects the load step-up transient performance of regulated hybrid SC topologies will be provided in Section 11.4.

The maximum total inductor current rising rate (SR_{R}) represents the physical limit of a topology's performance during load step-up transients. Therefore, SR_{R} is chosen as a metric for the performance comparison of load step-up transients. Based on the small-ripple approximation, the maximum current rising rate of inductor j ($\text{SR}_{\text{R},j}$) can be obtained as

$$\text{SR}_{\text{R},j} = \frac{\langle v_{\text{sw},j} \rangle - V_{\text{out}}}{L_j}, \quad (11.26)$$

where $\langle v_{\text{sw},j} \rangle$ denotes the average value of the switch-node voltage, $v_{\text{sw},j}$, over a switching period:

$$\langle v_{\text{sw},j} \rangle = D_{\text{max}} V_{\text{buck}}. \quad (11.27)$$

Substituting (11.27) and the expression for L_j in (11.8) into (11.26) and rearranging it with (11.23) yields

$$\text{SR}_{\text{R},j} = \left(D_{\text{max}} \frac{V_{\text{buck}}}{V_{\text{out}}} - 1 \right) \text{SR}_{\text{F},j} = \left(D_{\text{max}} \frac{K_{\text{tot}}}{K_{\text{SC}}} - 1 \right) \text{SR}_{\text{F},j}. \quad (11.28)$$

Similar to (11.24), $\text{SR}_{\text{R},j}$ can be normalized as

$$\widehat{\text{SR}}_{\text{R},j} = \frac{\text{SR}_{\text{R},j}}{\text{SR}_{\text{base}}} = \left(D_{\text{max}} \frac{K_{\text{tot}}}{K_{\text{SC}}} - 1 \right) \widehat{\text{SR}}_{\text{F},j}. \quad (11.29)$$

Therefore, the normalized total inductor current rising rate can be obtained as

$$\widehat{\text{SR}}_{\text{R}} = \sum_{j=1}^{N_{\text{L}}} \widehat{\text{SR}}_{\text{R},j} = \left(D_{\text{max}} \frac{K_{\text{tot}}}{K_{\text{SC}}} - 1 \right) \widehat{\text{SR}}_{\text{F}} = \left(D_{\text{max}} \frac{K_{\text{tot}}}{K_{\text{SC}}} - 1 \right) \frac{K_{\text{tot}}}{K_{\text{tot}} - K_{\text{SC}}}. \quad (11.30)$$

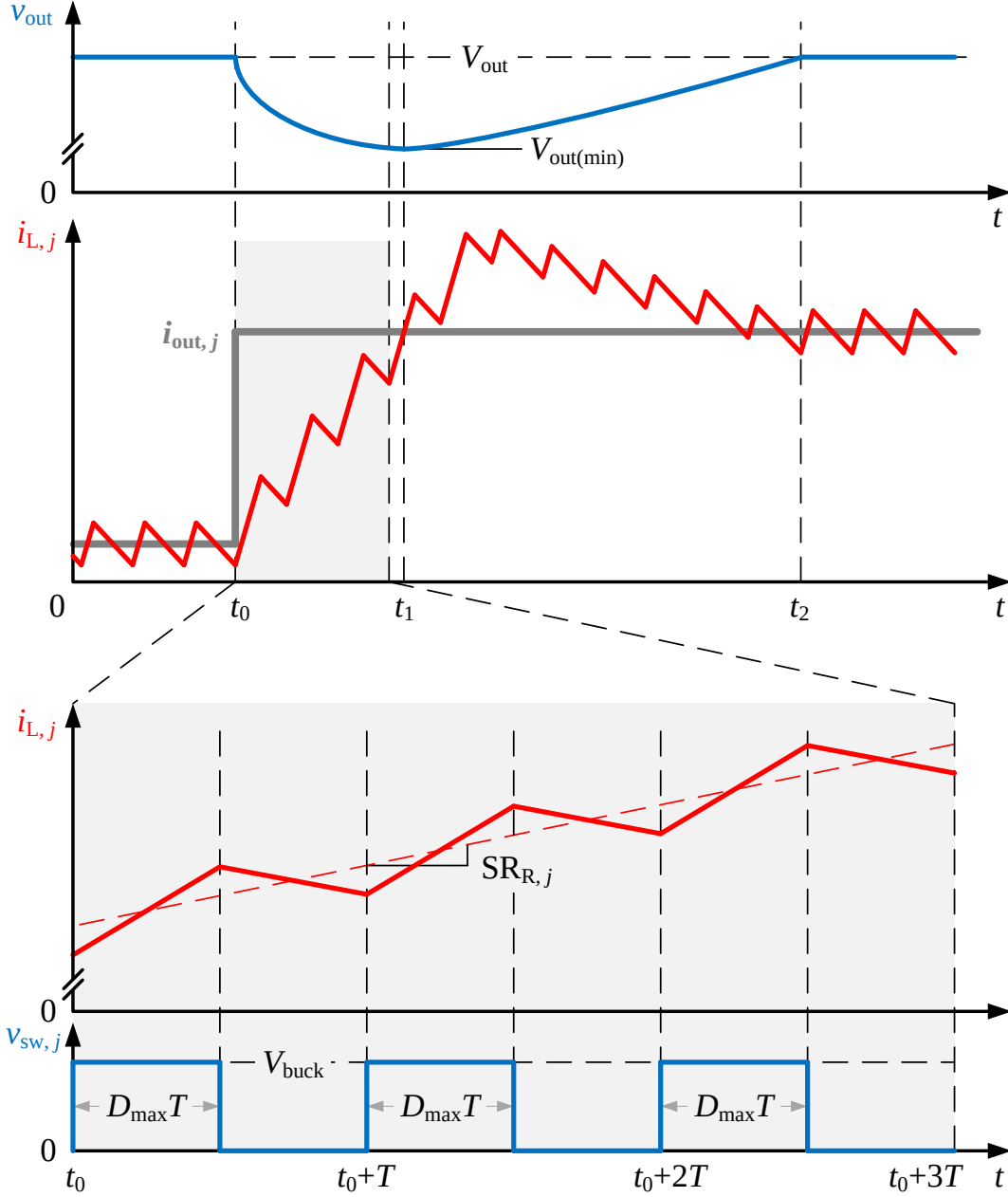


Figure 11.6: Load step-up transient waveforms of branch j . From top to bottom: the output voltage waveform (v_{out}), the waveforms of the current flowing through inductor j ($i_{L,j}$) and the load current flowing through branch j ($i_{out,j}$), the zoomed-in waveform of the inductor current over three switching cycles, and the switch-node voltage waveform seen by inductor j ($v_{sw,j}$). The fastest way of recovering v_{out} to the reference value (V_{out}) is by operating all branches at the maximum duty ratio (D_{max}) and forcing the inductor currents to rise at the maximum rate.

This means that $\widehat{\text{SR}}_{\text{R}}$ is a function of the SC stage conversion ratio (K_{SC}) and the maximum duty ratio (D_{max}).

11.3.5 Formalized Analysis Procedure

According to (11.2) and (11.21), the following topology-dependent characteristic parameters are needed to calculate the normalized metrics M_{S} and M_{P} : $\widehat{V}_{\text{ds},i}$, $\widehat{I}_{\text{d(rms)},i}$, $\widehat{V}_{\text{C},k}$, and $\widehat{q}_{\text{C},k}$. To formalize the analytical procedure, we define four topology-dependent characteristic vectors:

- Switch voltage stress vector $\widehat{\mathbf{V}}_{\text{ds}} = \left(\widehat{V}_{\text{ds},i} \right)_{1 \leq i \leq N_{\text{S}}}$
- Switch current stress vector $\widehat{\mathbf{I}}_{\text{d(rms)}} = \left(\widehat{I}_{\text{d(rms)},i} \right)_{1 \leq i \leq N_{\text{S}}}$
- Capacitor voltage vector $\widehat{\mathbf{V}}_{\text{C}} = \left(\widehat{V}_{\text{C},k} \right)_{1 \leq k \leq N_{\text{C}}}$
- Capacitor charge vector $\widehat{\mathbf{q}}_{\text{C}} = \left(\widehat{q}_{\text{C},k} \right)_{1 \leq k \leq N_{\text{C}}}$

with which we can rearrange (11.2) and (11.21) as

$$M_{\text{S}} = K_{\text{tot}} \widehat{\mathbf{V}}_{\text{ds}}^{\top} \widehat{\mathbf{I}}_{\text{d(rms)}}, \quad (11.31)$$

and

$$M_{\text{P}} = M_{\text{P,L}} + M_{\text{P,C}}, \quad (11.32)$$

where $M_{\text{P,L}}$ is the normalized inductor volume

$$M_{\text{P,L}} = \frac{(1 + \alpha_{\text{I}})^2}{4\alpha_{\text{I}}} \left(1 - \frac{K_{\text{SC}}}{K_{\text{tot}}} \right), \quad (11.33)$$

and $M_{\text{P,C}}$ is the normalized capacitor volume

$$M_{\text{P,C}} = \frac{(1 + \alpha_{\text{V}})^2}{4\alpha_{\text{V}}\beta} K_{\text{tot}} \widehat{\mathbf{V}}_{\text{C}}^{\top} \widehat{\mathbf{q}}_{\text{C}}, \quad (11.34)$$

in which $\cdot^{\top}$ denotes the transpose of a vector. The characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies are listed in Appendix C.

Equations (11.31) and (11.32) provide a formalized analytical procedure of M_{S} and M_{P} that can be automated. Equations (11.33) and (11.34) reveal two properties of $M_{\text{P,L}}$ and $M_{\text{P,C}}$:

- As the SC stage conversion ratio (K_{SC}) increases, the normalized inductor volume ($M_{\text{P,L}}$) decreases and the normalized capacitor volume ($M_{\text{P,C}}$) increases. This is intuitive because increasing the SC stage conversion ratio means shifting more voltage conversion burden from the buck-type stage to the SC stage, reducing the inductor volume but necessitating a higher-order SC network, which requires more and larger flying capacitors.

- Topologies with the same SC stage conversion ratio (K_{SC}) have the same normalized inductor volume ($M_{P,L}$) because the only topology-independent parameter in (11.33) is K_{SC} , while K_{tot} , α_I , α_V and β are all constants. Therefore, the difference in the normalized passive component volume among different topologies with the same SC stage conversion ratio only comes from the difference in the normalized capacitor volume ($M_{P,C}$).

These two properties will be used in the comparative analysis of the normalized passive component volume in Section 11.4.3.

11.4 Comparative Performance Analysis of 48-V-to-PoL Regulated Hybrid SC Topologies

Based on the analytical framework established in Section 11.4, this section performs a comparative analysis of state-of-the-art 48-V-to-1-V hybrid SC topologies and demonstrates the benefits of a larger SC stage conversion ratio.

11.4.1 Performance Comparison

Table 11.3 summarizes the key characteristics and the three normalized metrics of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. The year listed for each topology is when it was first proposed. If a topology has yielded more than one publication, the two most representative references are provided in the citation: 1) the earliest publication where the topology was first proposed, and 2) the latest publication that provides the most thorough explanation of the topology and/or includes experimental results from the best-performing hardware prototype.

The normalized passive component volume (M_P) of each topology is calculated using the following ripple ratios: $\alpha_I = 15\%$ and $\alpha_V = 5\%$. The reasons for selecting these ripple ratios are explained below. As a rule of thumb, the peak-to-peak inductor current ripple ($\Delta i_{L,pp}$) of a buck converter is typically designed to be between 20% and 40% of the full-load output current [90]. In this analysis, it is assumed that $\Delta i_{L,pp}$ is 30% (average of 20% and 40%) of the per-branch averaged current at full load, resulting in $\alpha_I = 15\%$. In addition, the peak-to-peak capacitor voltage ripple ($\Delta v_{C,pp}$) is assumed to be 10% of the mid-range capacitor voltage, following the rule of thumb for the small-ripple approximation to be valid, which yields $\alpha_V = 5\%$.

The normalized switch stress (M_S) of each topology is calculated under the assumption of negligible inductor current ripples and capacitor voltage ripples, as mentioned in Section 11.3.1. Inductor current ripples can be ignored in the analysis of the normalized switch stress because their influence on switch RMS current stress is typically very small. For example, the RMS value of the current flowing through the high-side switch in a buck converter,

Table 11.3: Topological comparison of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion

Year	Topology	SC Stage Conversion Ratio ($K_{SC} : 1$)	Buck-Type Stage Conversion Ratio ($K_{buck} : 1$)	Buck-Type Stage Duty Ratio		Complete Soft-Charging?
				Nominal (D)	Maximum (D_{max})	
2005	Series-capacitor buck with multi-phase operation [60]	2:1	24:1	0.042	0.5	Yes
		3:1	16:1	0.063	0.333	
2011	Series-capacitor buck with two-phase operation [89]	4:1	12:1	0.083	0.5	Yes
2020	Crossed-coupled QSD buck [70]	4:1	12:1	0.083	0.5	Yes
2018	DIH [81, 129]	6:1	8:1	0.125	0.5	Yes, with split- phase control
2019	LEGO [73, 83]	6:1	8:1	0.125	1.0	No
2023	Mini-LEGO [98, 114]					
2021	CaSP [64]	6:1	8:1	0.125	0.333	Yes
2022	SDIH [82, 130]	6:1	8:1	0.125	0.5	Yes, with split- phase control
2020	MLB [65, 76]	8:1	6:1	0.167	0.5	Yes
2020	VIB [74, 77]	8:1	6:1	0.167	0.25	No
2022	MSC [97, 131]	8:1	6:1	0.167	0.25	Yes
2022	Dickson ² [75]	9:1	5.33:1	0.188	0.333	Yes
2023	16-to-1 switching bus converter (SBC) [115, 119]	16:1	3:1	0.333	0.5	Yes
2023	20-to-1 switching bus converter (SBC) [96, 123]	20:1	2.4:1	0.417	0.5	Yes

TABLE 11.3 (continued): Topological comparison of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion

Year	Topology	Normalized Switch Stress (M_S)	Normalized Passive Component Volume (M_P)			Normalized Total Inductor Current Slew Rate	
			$\beta = 500$	$\beta = 100$	$\beta = 50$	Falling Rate ($\widehat{SR}_F$)	Rising Rate ($\widehat{SR}_R$)
2005	Series-capacitor buck with multi-phase operation [60]	31.6	2.12	2.14	2.17	1.04	11.5
		23.1	2.08	2.12	2.18	1.07	4.62
2011	Series-capacitor buck with two-phase operation [89]	18.7	2.04	2.10	2.19	1.09	5.45
2020	Crossed-coupled QSD buck [70]	24.2	2.03	2.08	2.13	1.09	5.45
2018	DIH* [81, 129]	14.7	2.02	2.40	2.87	1.14	3.43
2019	LEGO [†] [73, 83]	17.6	2.03	2.41	2.89	1.14	8.00
2023	Mini-LEGO [†] [98, 114]						
2021	CaSP [64]	23.5	1.95	2.02	2.11	1.14	1.90
2022	SDIH* [82, 130]	14.7	2.02	2.40	2.84	1.14	3.43
2020	MLB [65, 76]	23.7	1.88	2.03	2.22	1.20	2.40
2020	VIB [‡] [74, 77]	14.3	1.88	2.07	2.3	1.20	0.60
2022	MSC [97, 131]	15.1	1.86	1.95	2.06	1.20	0.60
2022	Dickson ² [75]	14.8	1.81	1.90	2.01	1.23	0.96
2023	16-to-1 switching bus converter (SBC) [115, 119]	10.2	1.51	1.69	1.91	1.50	0.75
2023	20-to-1 switching bus converter (SBC) [96, 123]	8.99	1.34	1.56	1.84	1.71	0.34

* In [81, 82, 129, 130], all flying capacitor voltage ripples are designed to be the same, which enables simple split-phase control timing. Since the mid-range voltages across different flying capacitors are different, the voltage ripple ratios of different flying capacitors in these two works are not uniform. Nevertheless, the normalized passive component volume (M_P) listed in this table assumes uniform voltage ripple ratios for all flying capacitors, which requires more complex split-phase control timing.

[†] Small filter capacitors (C_{filter}) are not taken into account in the capacitor volume analysis, although they are used in the hardware prototype in [73, 83, 98, 114] to filter the high-frequency pulsating current from the buck-type stage. Additionally, the charge-sharing loss between the filter capacitors and the flying capacitors is not captured in this analysis.

[‡] In addition to flying capacitors, an intermediate bus capacitor (C_{IB}) is included in the capacitor volume calculation as well. As mentioned in [74, 77], its value is chosen to be $C_{\text{IB}} = C_F/2.34$, where C_F is the charge pump capacitance. The normalized voltage stress on C_{IB} is 1/2. The charge-sharing loss between the intermediate bus capacitor and the flying capacitors is not captured in this analysis.

which exhibits a pulsating current waveform with linear ripple, can be given as

$$I_{d(\text{rms})} = I_L \sqrt{D} \sqrt{1 + \frac{1}{3} \alpha_I^2}, \quad (11.35)$$

where I_L is the average inductor current, D is the duty ratio, and α_I is the inductor current ripple ratio as defined in (11.5). Even if $\alpha_I = 20\%$ (i.e., $\Delta i_{L,\text{pp}} = 0.4 I_L$), the RMS current ($I_{d(\text{rms})}$) changes by only 0.7% ($\sqrt{1 + \frac{1}{3} \times 0.2^2} = 1.007$). Therefore, inductor current ripples are typically negligible in the calculation of switch RMS current stress. Similarly, capacitor voltage ripples are ignored in the calculation of switch voltage stress because they are assumed to be small compared to the mid-range voltages ($\alpha_V = 5\%$).

11.4.2 Analysis of Normalized Switch Stress

To better visualize the influence of the SC stage conversion ratio (K_{SC}), Fig. 11.7 plots the normalized switch stress (M_S) of different topologies against their SC stage conversion ratio (K_{SC}). Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. Some extendable topologies are plotted with dashed curves connecting different possible implementations at different SC stage conversion ratios. As shown in Fig. 11.7, with a larger SC stage conversion ratio, the buck-type stage duty ratio (D) can be extended.

The series-capacitor-buck (SCB) topology was first proposed in [60] with multi-phase operation and then extended in [89] with two-phase operation. Fig. 11.8(a) shows a four-phase SCB converter as an example. In the multi-phase operation illustrated in Fig. 11.8(b), each inductor operates in an individual phase; in the two-phase operation illustrated in Fig. 11.8(c), the inductors are divided into two groups: the odd-numbered group and the even-numbered group, each operating in an individual phase with a 180° phase shift. Compared to multi-phase operation, the two-phase operation can extend the maximum duty ratio from $\frac{1}{N}$ to $\frac{1}{2}$, where N is the number of branches. As a result, the upper limit on the number of branches can be increased from $N_{\text{m-ph}}$ to $N_{2\text{-ph}}$:

$$\text{Multi-phase operation: } N_{\text{m-ph}} < \sqrt{\frac{V_{\text{in(SCB)}}}{V_{\text{out(SCB)}}}} \quad (11.36)$$

$$\text{Two-phase operation: } N_{2\text{-ph}} < \frac{V_{\text{in(SCB)}}}{2V_{\text{out(SCB)}}}, \quad (11.37)$$

where $V_{\text{in(SCB)}}$ and $V_{\text{out(SCB)}}$ are the input and output voltages of the SCB converter, respectively. For 48-V-to-1-V conversion ($V_{\text{in(SCB)}} = 48 \text{ V}$ and $V_{\text{out(SCB)}} = 1.0 \text{ V}$), the maximum allowable numbers of branches for multi-phase operation and two-phase operation are $N_{\text{m-ph(max)}} = 6$ and $N_{2\text{-ph(max)}} = 20$, respectively. Since the SC stage conversion ratio

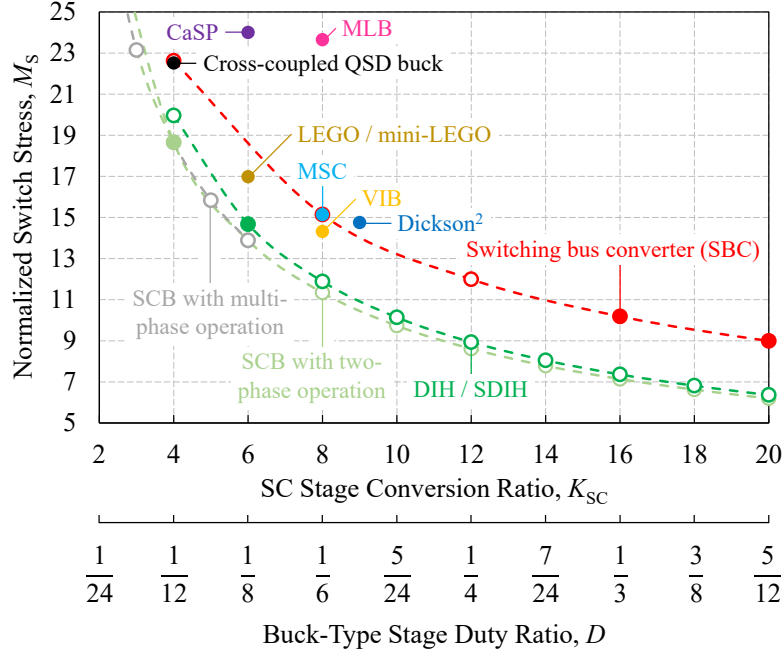


Figure 11.7: Normalized switch stress (M_s) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A lower normalized switch stress (M_s) is more desirable.

(K_{SC}) of a SCB converter is equal to its number of branches (N), the maximum SC stage conversion ratio for multi-phase operation and two-phase operation are $K_{SC,m-ph(max)} = 6$ and $K_{SC,2-ph(max)} = 20$, respectively. As K_{SC} increases, the voltage stress on all switches decreases while the current stress on most switches increases. Nevertheless, the increase in switch current stress does not offset the voltage stress reduction. Therefore, as shown in Fig. 11.7, the net result is that the normalized switch stress of a SCB converter decreases as K_{SC} increases. This means that a SCB converter with a larger SC stage conversion ratio has the theoretical potential of achieving higher efficiency. Compared to multi-phase operation, two-phase operation can better leverage the benefits of a larger SC stage conversion ratio since it extends the upper limit on the number of branches.

Although two-phase operation does result in a larger net output current ripple than multi-phase operation, this does not necessarily require a larger output capacitor in PoL applications. The size of the output capacitor in these applications is mainly dictated by transient performance requirements, such as limiting the maximum output voltage overshoot and undershoot. Typically, an output capacitor that is sufficiently large to meet these transient requirements also ensures that the steady-state output voltage ripple stays well

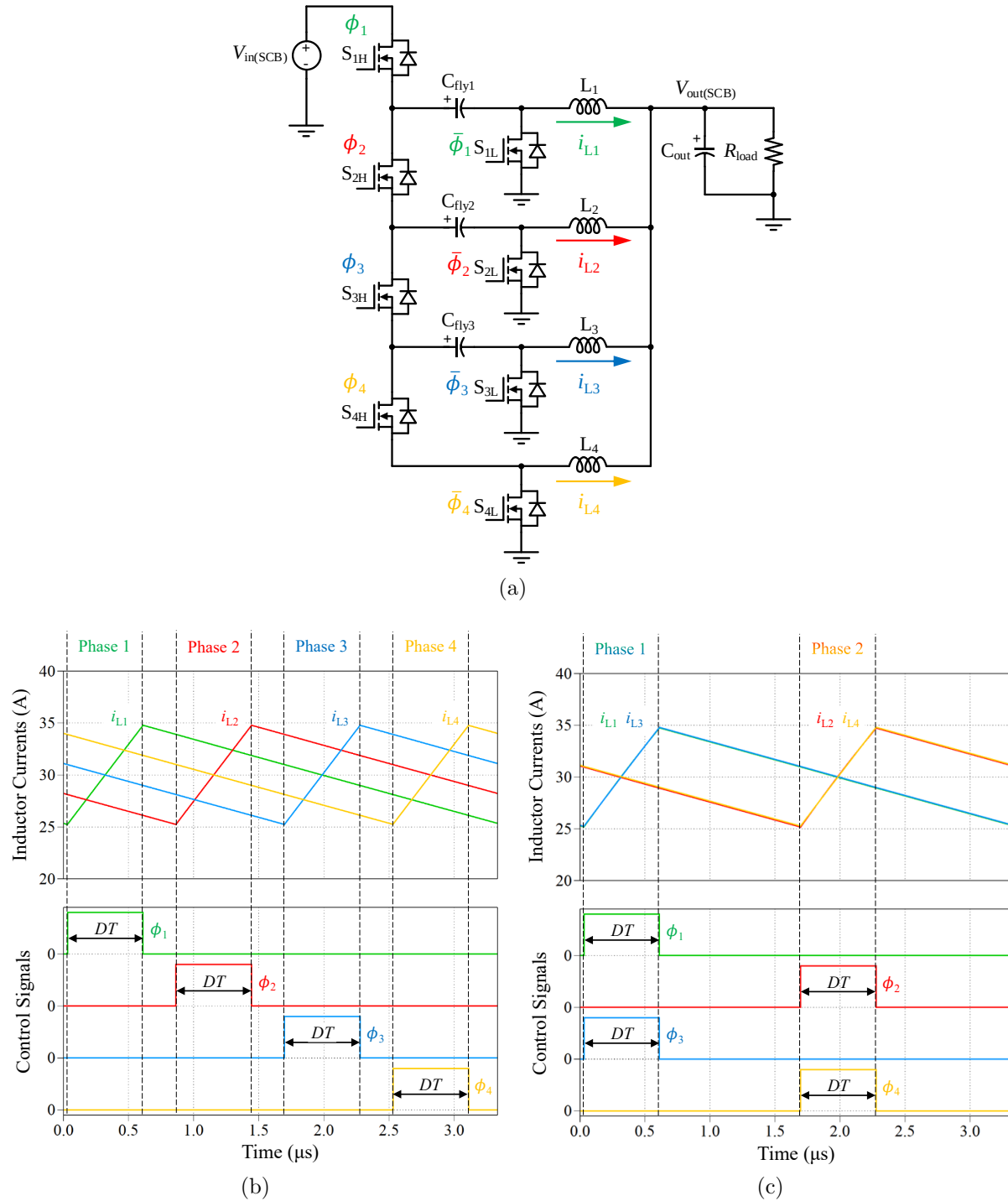


Figure 11.8: Four-branch SCB converter. (a) Schematic drawing. (b) Multi-phase operation. (c) Two-phase operation.

below the maximum acceptable levels. Therefore, there is no need to increase the output capacitance when changing from multi-phase operation to two-phase operation. In fact, as will be explained in Section 11.4.4, since two-phase operation enables a faster transient response than multi-phase operation, the output capacitance can potentially be reduced.

The DIH [81, 129] and SDIH [82, 130] topologies can be viewed as SCB topologies under two-phase operation, but with the inductors operating in the same phase merged into one large inductor by short-circuiting the odd-numbered and even-numbered switch nodes, respectively. Given that the scaling law of magnetics favors larger components [146], combining multiple small inductors into one large inductor can typically improve the overall performance of magnetic components. However, short-circuiting the switch nodes brings about the hard-charging of flying capacitors, which can only be overcome by the split-phase control [72]. The additional secondary phases introduced by the split-phase control reduce the effective duty ratio, resulting in slightly higher normalized switch stress for the DIH and SDIH topologies compared to a SCB topology under two-phase operation, as shown in Fig. 11.7. Due to the sensitivity of split-phase control timing to component sizing, either capacitors with high stability, such as Class I multilayer ceramic capacitors (MLCCs) that have lower energy densities, or active split-phase control [147, 148] must be used to ensure complete soft-charging.

The switching bus converter (SBC) [96, 115, 119, 123] merges a 2-to-1 SC front-end with two SCB modules through two switching buses with intermediate bus capacitors and redundant switches removed. The advantages of the switching-bus-based architecture over the existing dc-bus-based architecture are explained in Chapter 7. Each SCB module operates in the two-phase fashion illustrated in Fig. 11.8(c). Therefore, the switching bus converter extends the maximum duty ratio to 50% and enables a larger SC stage duty ratio. As can be seen in Fig. 11.7, the normalized switch stress (M_S) of the switching bus converter decreases as the SC stage conversion ratio (K_{SC}) increases, which shows the benefits of a larger SC stage conversion ratio. As discussed in [119], the switching-bus-based architecture ensures complete soft-charging operation, thus avoiding the need for the split-phase control. The switching bus concept was first introduced in [75] with the Dickson² topology. Other switching-bus-based topologies include MLB [65, 76] and CaSP [64] topologies.

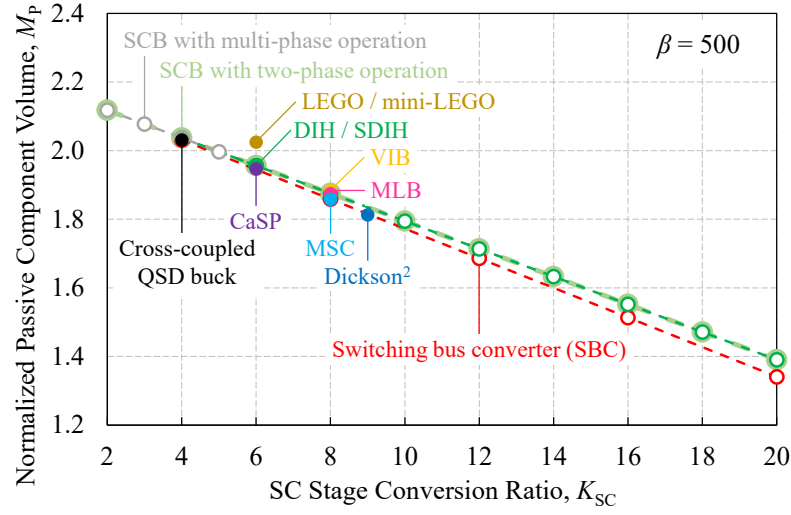
Fig. 11.7 shows that, in general, increasing the SC stage conversion ratio of a regulated hybrid SC topology reduces its normalized switch stress, thereby improving efficiency. One possible concern about using the normalized switch stress as an indicator of efficiency is that it only captures the power losses in semiconductor switches but excludes the losses in flying capacitors and inductors. Flying capacitor equivalent series resistance (ESR) conduction loss is typically lower than 5% of total loss and is thereby negligible. However, inductor core loss and winding loss cannot be neglected. As the SC stage conversion ratio increases, the voltage stress (V_{buck}) on the subsequent buck-type stage is reduced, and therefore, the inductor size is decreased, resulting in a smaller core volume and lower dc resistance (DCR). This means that the inductor losses are reduced when the SC stage conversion ratio is increased. Consequently, the conclusion that increasing the SC stage conversion ratio is favorable for efficiency improvement holds, even with the inductor losses taken into consideration.

11.4.3 Analysis of Normalized Passive Component Volume

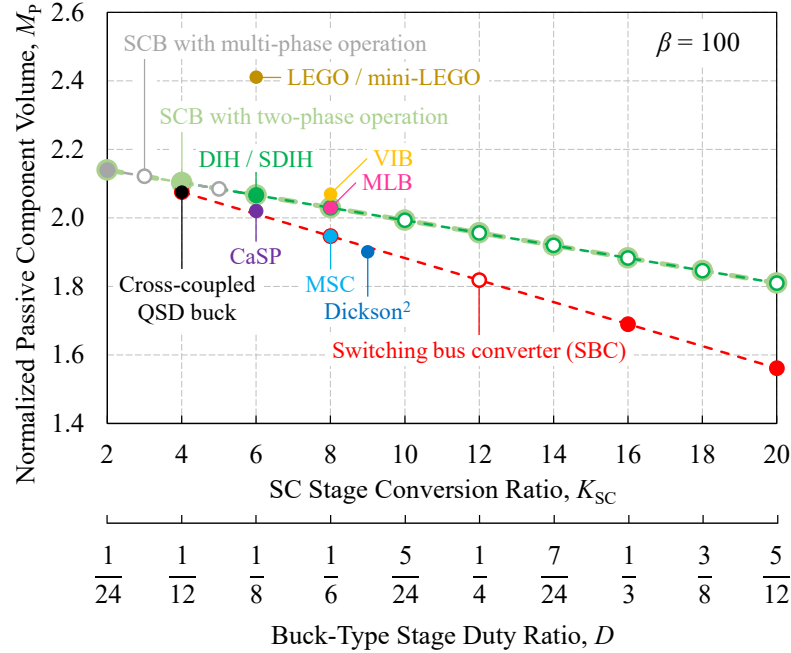
Fig. 11.9 shows the normalized passive component volume (M_P) of different topologies against their SC stage conversion ratio (K_{SC}), assuming an inductor current ripple ratio of $\alpha_I = 15\%$, a capacitor voltage ripple ratio of $\alpha_V = 5\%$, and three different energy density ratios of capacitors to inductors: $\beta = 500, 100, 50$. Table 11.4 lists three practical examples for calculating the energy density ratio (β) between capacitors and inductors. The commercial capacitor component TDK C3216X7R1H106K160AE [149] is rated at 50 V and is assumed to withstand a peak voltage of 25 V. Under a dc bias of 25 V, its capacitance derates to 3.5 μF . Therefore, the volumetric energy density of this capacitor component, when biased at a dc voltage of 25 V, is calculated as $\frac{1}{2}CV^2$ divided by its volume, which is equal to 134 $\mu\text{J}/\text{mm}^3$. Similarly, the volumetric energy density of a commercial discrete inductor component, Coilcraft SLR1065-301KEC [150], at its saturation current (32 A) is calculated as $\frac{1}{2}LI^2$ divided by its volume, yielding 0.256 $\mu\text{J}/\text{mm}^3$. Therefore, in this example, the energy density ratio between these two commercial components is $\beta_{DL} = \frac{134}{0.256} = 523$, which is representative of the energy density ratios between commercial Class II MLCCs and discrete inductors. Note that this example assumes 50% voltage utilization of the capacitor component, meaning that it is assumed to operate at 50% of its rated voltage. When fully utilized, commercial Class II MLCCs can achieve an approximately 1000 times higher energy density compared to commercial discrete inductors [1]. Due to DC flux cancellation, coupled inductors can achieve the same per-phase steady-state inductance with a smaller core volume compared to discrete inductors [125]. As listed in Table 11.4, the customized four-phase coupled inductor presented in [96] achieves a volumetric energy of 1.69 $\mu\text{J}/\text{mm}^3$ at its saturation current, which is 6.6 times higher than the commercial discrete inductor component. The energy density ratio between the commercial capacitor component (TDK C3216X7R1H106K160AE) and this customized four-phase coupled inductor is $\beta_{CL} = \frac{134}{1.69} = 79$. These practical examples demonstrate that $\beta = 500$ can be used in topological comparisons involving commercial discrete inductors, while β may decrease to 100 or even 50 when customized coupled inductors are used.

As can be seen in Fig. 11.9(a), when $\beta = 500$ (for example, when discrete inductors are used), the normalized passive component volume (M_P) of the regulated hybrid SC topologies decreases as their SC stage conversion ratio (K_{SC}) increases. The normalized passive component volume is the sum of the normalized inductor volume and the normalized capacitor volume (i.e., $M_P = M_{P,L} + M_{P,C}$). Recall the first property of $M_{P,L}$ and $M_{P,C}$ mentioned at the end of Section 11.3.5: as K_{SC} increases, $M_{P,L}$ decreases and $M_{P,C}$ increases. However, since capacitors have much higher volumetric energy densities compared to discrete inductors, as demonstrated in Table 11.4, the increase in capacitor volume does not offset the inductor volume reduction. As a result, the total passive component volume goes down as the SC stage conversion ratio increases. This shows that when discrete inductors are used, increasing the SC stage conversion ratio of a regulated hybrid SC topology reduces its normalized passive component volume, thereby improving power density.

As β decreases (for example, when coupled inductors with higher energy densities are



(a)



(b)

Figure 11.9: Normalized passive component volume (M_P) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion ($\alpha_I = 15\%$, $\alpha_V = 5\%$). (a) $\beta = 500$. (b) $\beta = 100$. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A smaller normalized passive component volume (M_P) is more desirable.

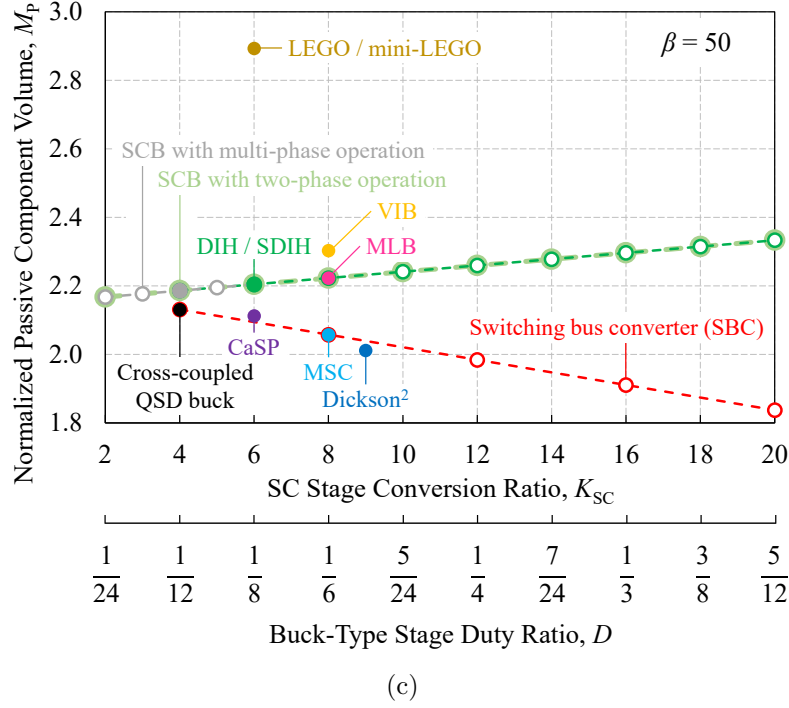


TABLE 11.9 (continued): Normalized passive component volume (M_P) of state-of-the-art regulated hybrid SC topologies for 48-V-to-1-V conversion ($\alpha_I = 15\%$, $\alpha_V = 5\%$). (c) $\beta = 50$. Solid dots represent topologies with hardware demonstrations in previous literature, while hollow circles represent theoretically-existent topologies that have not been implemented previously. A smaller normalized passive component volume (M_P) is more desirable.

used), the inductor volume reduction rate with respect to the SC stage conversion ratio (K_{SC}) drops and gradually approaches the capacitor volume increase rate. As a result, the slope of the M_P lines becomes less negative when β decreases from 500 to 100, as can be observed in Figs. 11.9(a) and (b). This means that the increase in the capacitor volume plays a more important role in the total volume change as K_{SC} increases when inductors are more energy-dense (i.e., when β decreases). It can be anticipated that when β decreases to a certain extent, the inductor volume reduction rate with respect to K_{SC} will be smaller than the capacitor volume increase rate. As a result, the increase in the capacitor volume will dominate the total volume change, meaning that M_P will rise as K_{SC} increases. This is indeed what happens when β decreases from 100 to 50. As shown in Fig. 11.9(c), when $\beta = 50$, the normalized passive component volume of the SCB [60, 89], DIH [81, 129], and SDIH [82, 130] topologies rises as the SC stage conversion ratio increases, resulting from the increase in the capacitor volume. Therefore, these topologies cannot leverage the benefits of a larger SC stage conversion ratio when high-density coupled inductors are used.

Table 11.4: Practical examples for calculating the energy density ratio (β) between capacitors and inductors

Component	Part Number	Parameters	Dimensions	Volumetric Energy Density
Capacitor	TDK C3216X7R1-H106K160AE [149]	Rated voltage: 50 V Capacitance: 3.5 μ F (@ 25 V)	$3.2 \times 1.6 \times 1.6 \text{ mm}^3$	134 μ J/mm ³ (@ 25 V)
Discrete Inductor	Coilcraft SLR1065-301KEC [150]	Saturation current: 32 A Inductance: 275 nH (@ 32 A) DCR: 0.48 m Ω	$10.4 \times 8.0 \times 6.6 \text{ mm}^3$	0.256 μ J/mm ³ (@ 32 A) ($\beta_{DL} = \frac{134}{0.256} = 523$)
Coupled Inductor	Customized four-phase coupled inductor presented in [96]	Saturation current: 45 A Inductance: 260 nH* (@ 45 A) DCR: 0.16 m Ω	$18.5 \times 10.5 \times 3.2 \text{ mm}^3$	1.69 μ J/mm ³ (@ 45 A) ($\beta_{CL} = \frac{134}{1.69} = 79$)

* Per-phase steady-state inductance (four-phase average value at $D = 0.417$).

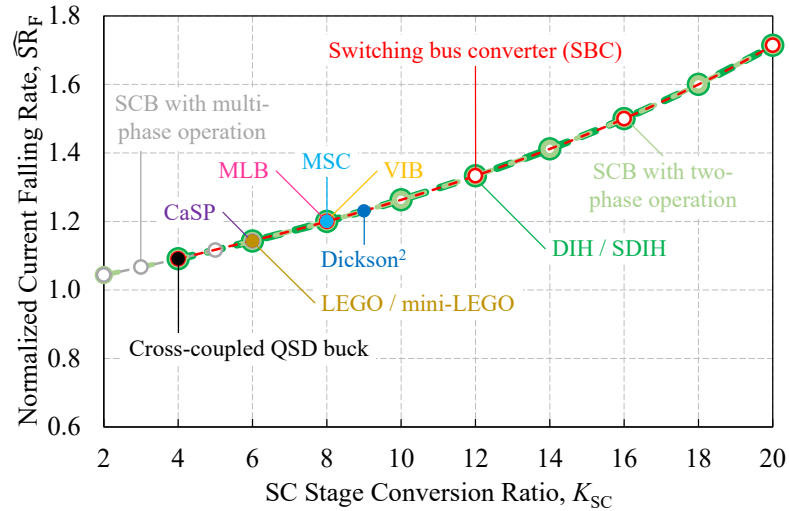
Nevertheless, even when $\beta = 50$, the switching bus converter (SBC) [96, 115, 119, 123] maintains a decreasing normalized passive component volume as the SC stage conversion ratio increases. This demonstrates its capability of leveraging the benefits of a larger SC stage conversion ratio and the high energy densities of coupled inductors simultaneously. Moreover, it requires a smaller normalized passive component volume compared to the SCB, DIH, and SDIH topologies at the same SC stage conversion ratio, showing its potential to achieve higher power density. Recall the second property of $M_{P,L}$ and $M_{P,C}$ mentioned at the end of Section 11.3.5: topologies with the same SC stage conversion ratio have the same normalized inductor volume. Therefore, at the same SC stage conversion ratio, the difference in the normalized passive component volume among different topologies only comes from the difference in the normalized capacitor volume. In the SCB, DIH, and SDIH topologies, the mid-range flying capacitor voltages are $\frac{k}{K_{SC}}V_{in}$ ($k = 1, 2, \dots, K_{SC} - 1$), with half of the capacitor voltages beyond $\frac{1}{2}V_{in}$. In contrast, the flying capacitor voltages in the switching bus converter are $\frac{1}{2}V_{in}$ and $\frac{k}{K_{SC}}V_{in}$ ($k = 1, 2, \dots, K_{SC}/2 - 1$), with all capacitor voltages lower than or equal to $\frac{1}{2}V_{in}$. Consequently, by halving the input voltage with an additional 2-to-1 SC front-end, the switching bus converter reduces the requirement for capacitive energy storage, thereby reducing the flying capacitor volume and total passive component volume.

11.4.4 Analysis of Normalized Total Inductor Current Slew Rate

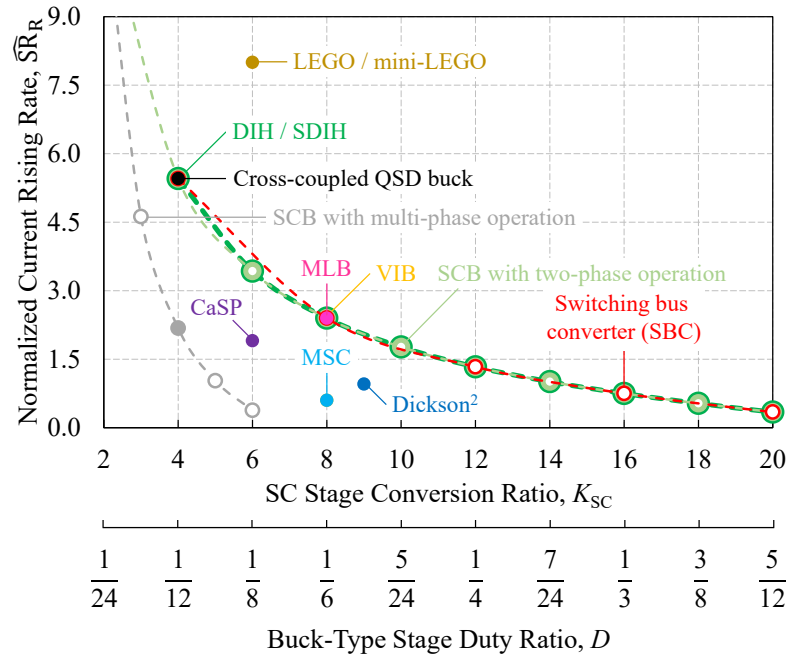
Fig. 11.10 presents the normalized falling and rising rates ($\widehat{SR}_F$ and $\widehat{SR}_R$) of the total inductor current for different topologies against their SC stage conversion ratio (K_{SC}).

As can be seen in Fig. 11.10(a), the normalized current falling rate ($\widehat{SR}_F$) increases with the SC stage conversion ratio, which implies that a larger SC stage conversion ratio is favorable for better load step-down transient performance. As the SC stage conversion ratio increases, the voltage conversion burden on the buck-type stage is alleviated, resulting in reduced inductor values. Since the optimal control strategy during a load step-down transient is to ground all switch nodes, the voltage applied across the inductors remains constant at the output voltage (V_{out}), regardless of the circuit topology. Consequently, benefiting from the smaller inductors, a regulated hybrid SC topology with a larger SC stage conversion ratio can achieve faster load step-down transient response. In addition, it is not surprising that the normalized current falling rates of all topologies fall on the same trend line, since the only topology-dependent parameter in (11.25) is K_{SC} .

Fig. 11.10(b) depicts how the normalized current rising rate ($\widehat{SR}_R$) of different topologies change with their SC stage conversion ratios (K_{SC}). In general, the normalized current rising rate of these regulated hybrid SC topologies decreases with a larger SC stage conversion ratio, meaning slower dynamic response. This is mainly because an increased K_{SC} leads to a decrease in V_{buck} , which is applied to the inductors during the load step-up transient to ramp up the inductor current. Although the inductor value in the buck-type stage reduces as K_{SC} increases, which helps improve the load step-up transient performance, the inductor size reduction does not offset the impact of a lower V_{buck} voltage.



(a)



(b)

Figure 11.10: Normalized total inductor current slew rate. (a) Normalized total inductor current falling rate ($\widehat{SR}_F$). (b) Normalized total inductor current rising rate ($\widehat{SR}_R$). Larger current slew rates are more desirable since they indicate faster dynamic response and better transient performance.

Moreover, many of these regulated hybrid SC topologies have an upper limit on the duty ratio of the buck-type stage that is lower than 100%. This limits the maximum average voltage applied to the inductors during a load step-up transient, which reduces the current rising rate. For example, as mentioned earlier in Section 11.4.2, the maximum duty ratio of a SCB converter with multi-phase operation is $\frac{1}{N}$, where N is the number of branches, and that of a SCB converter with two-phase operation is $\frac{1}{2}$. Benefiting from the extended duty ratio enabled by the two-phase operation, the SCB with two-phase operation achieves a faster current rising rate and improved load step-up performance compared to the SCB with multi-phase operation, as demonstrated in Fig. 11.10(b) with the light-green curve and the gray curve, respectively. Additionally, the switching bus converter (SBC) also achieves improved load step-up transient performance through two-phase operation due to the same reason.

One noticeable difference between Fig. 11.10(a) and Fig. 11.10(b) is that the normalized current rising rate ($\widehat{SR}_R$) is typically larger than the normalized current falling rate ($\widehat{SR}_F$). This is mainly because the average voltage applied to the inductors during a load step-up transient ($D_{\max}V_{\text{buck}}$, as shown in (11.27)) is typically higher than that during a load step-down transient (V_{out}). For a 12-V-to-1-V buck converter, the inductor current rising rate is 11 times faster than its falling rate, meaning that the step-down transient is typically much worse than the step-up transient. Therefore, in the design of existing multi-phase-buck-based VRMs, the step-down transient is usually the primary concern [151]. In contrast, regulated hybrid SC topologies offer the opportunity to achieve similar rising and falling rates of the inductor current, which balances the load step-up and step-down transient performance. For example, a SC stage conversion ratio of $K_{\text{SC}} = 12$ enables the SCB with two-phase operation [89], the switching bus converter (SBC) [96, 115, 119, 123], and the DIH [81, 129] and SDIH [82, 130] topologies to equalize the normalized falling and rising rates ($\widehat{SR}_F$ and $\widehat{SR}_R$) of the total inductor current and achieve balanced step-up and step-down transient performance.

11.4.5 Summary of Comparative Performance Analysis

The conclusions from this comparative performance analysis can be summarized as follows:

- Increasing the SC stage conversion ratio decreases the normalized switch stress, which is beneficial for lowering power losses and achieving higher efficiency.
- Increasing the SC stage conversion ratio reduces the normalized passive component volume, which is favorable for converter miniaturization and achieving higher power density.
- A larger SC stage conversion ratio speeds up the falling slew rate of the total inductor current, which improves load step-down transient performance. However, it slows down the rising rate of the total inductor current, leading to slower load step-up dynamic

responses. However, regulated hybrid SC topologies offer the opportunity to achieve balanced load step-up and step-down transient performance with proper designs.

11.5 Chapter Summary

This chapter proposed an analytical framework for comparing the performance of 48-V-to-PoL regulated hybrid SC topologies. In this framework, three metrics are defined and calculated for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. Through comprehensive comparative analysis, this framework reveals the benefits of a larger SC stage conversion ratio: increasing the SC stage conversion ratio reduces switch stress and passive component volume while accelerating the falling rate of inductor current, thereby improving efficiency, power density, and load step-down transient performance simultaneously. Although a larger SC step-down ratio typically slows down the rising rate of inductor current, which can potentially impair the load step-up transient performance, properly designed regulated hybrid SC topologies can achieve balanced load step-up and step-down transient performance with similar rising and falling rates of the total inductor current.

Chapter 12

Conclusion

This dissertation explores the circuit topologies, control techniques, and analytical models for hybrid SC converters and demonstrates their great potential to achieve improved performance in data center applications, including 48-V-to-12-V and direct 48 V to point-of-load (PoL) power conversions.

The first part of this dissertation proposes a general modeling and analysis methodology for fixed-ratio pure and resonant SC converters to quantitatively characterize the effects of finite terminal capacitances. For pure SC converters, it is revealed that insufficient input capacitance can lead to a dramatic increase in output impedance and cause a considerable efficiency drop. Conversely, decreasing the output capacitance can counter-intuitively reduce the output impedance, which contributes to both higher efficiency and higher power density. Additionally, the output capacitance has a stronger effect on the output impedance in the slow switching region, while the input capacitance is more influential in the fast switching region, especially around the knee of the output impedance curve, which is the typical operating point of pure SC converters. For resonant SC converters, insufficient terminal capacitances can result in higher critical switching frequencies and higher output impedance, and the input capacitance has a stronger influence on the critical switching frequency than the output capacitance. To reduce terminal capacitances without sacrificing efficiency, this dissertation proposes a multi-resonant compensation control technique for resonant SC converters that can adaptively compensate for the negative effects of finite terminal capacitances by ensuring multi-resonant and full zero-current switching operation with adjusted duty ratio and switching frequency. The proposed control technique is implemented in a 2-to-1 ReSC converter prototype for experimental verification. It is shown that the proposed control technique can reduce the terminal capacitances by at least a factor of 5 without harming overall efficiency.

The second part of this dissertation explores high-performance hybrid SC converters for direct 48 V to PoL power conversion in data centers. In pursuit of a more efficient and compact alternative to the existing dc-bus-based architecture, where two conversion stages are merged through an intermediate dc bus, this dissertation introduces a new method of merging two or more SC stages through intermediate *switching buses*. Compared to the

existing dc-bus-based architecture, the proposed switching-bus-based architecture has three advantages that promise higher performance: 1) It eliminates the need for bus capacitors to maintain a stiff dc bus voltage. 2) One redundant switch can be removed on each switching bus while merging two stages. 3) It ensures complete soft-charging operation. Based on the switching bus concept, this dissertation proposes a family of high-performance hybrid SC voltage regulators, named the switching bus converter.

To theoretically compare the performance of the proposed topology to the existing regulated hybrid SC topologies for direct 48-V-to-PoL conversion, this dissertation establishes an analytical framework and conducts a comparative performance analysis. In the proposed framework, a regulated hybrid SC topology is depicted as a fixed-ratio SC stage merged with a subsequent regulated buck-type stage. The total conversion ratio is allocated between these two conversion stages. Three metrics are defined and calculated for performance comparison: a) normalized switch stress as an indicator of efficiency, b) normalized passive component volume as an indicator of power density, and c) normalized total inductor current slew rate as an indicator of transient performance. Through the comprehensive comparative analysis, this framework reveals the benefits of a larger SC stage conversion ratio: increasing the SC stage conversion ratio reduces switch stress and passive component volume while accelerating the falling rate of inductor current, thereby improving efficiency, power density, and load step-down transient performance simultaneously. Although a larger SC step-down ratio typically slows down the rising rate of inductor current, which can potentially impair the load step-up transient performance, properly designed regulated hybrid SC topologies can achieve balanced load step-up and step-down transient performance with similar rising and falling rates of the total inductor current. Through a two-phase operation of the series-capacitor buck modules, the proposed switching bus converter extends the maximum duty ratio and enables a larger SC conversion ratio, showing great potential to achieve higher efficiency and higher power density concurrently when compared to existing regulated hybrid SC topologies.

To verify the theoretical benefits of the proposed switching-bus-based architecture, various circuit topologies from the switching bus converter family and their hardware prototypes are presented, including a high-efficiency prototype and a high-density prototype. The high-efficiency prototype was designed and built with customized four-phase coupled inductors and hybrid gate drive daughterboards. It is capable of sourcing an output current of 1500-A at 48-V-to-1-V conversion and achieved 92.7% peak system efficiency, 85.7% full-load system efficiency (including gate drive loss), and 759 W/in³ power density (by box volume) without any heat sink and with air cooling only. Additionally, compared to the state-of-the-art, the high-density prototype doubled the power density while maintaining the same full-load efficiency, with a height of 4.7 mm. Due to its high current density and low profile, this high-density prototype can be placed on the bottom side of the motherboard directly underneath the processor, which allows it to deliver high current vertically to the top side through vias, enabling vertical power delivery. This not only significantly reduces the size of the power distribution network (PDN) and associated conduction losses but also saves the valuable topside area on the motherboard for high bandwidth memory (HBM) and high-speed

communication. Together, these two switching bus converter prototypes create an improved performance boundary for 48-V-to-PoL power conversion in data center applications.

Finally, the proposed topologies and switching bus concept are synthesized and extended as a generalized switching-bus-based architecture for regulated hybrid switched-capacitor converters. Based on this generalized architecture, a family of regulated switching-bus-based topologies can be constructed by strategically merging two or more SC conversion stages.

Appendix A

Derivation of Switching Device Figure-of-Merit

A.1 Power Semiconductor Device Loss Analysis

The total loss of a power semiconductor device can be obtained as

$$P_{\text{semi}} = P_{\text{cond}} + P_{\text{sw}}, \quad (\text{A.1})$$

where P_{cond} and P_{sw} represent the conduction and switching losses, respectively. The conduction loss is given by

$$P_{\text{cond}} = R_{\text{ds,on}} I_{\text{d(rms)}}^2, \quad (\text{A.2})$$

where $R_{\text{ds,on}}$ is the on-state resistance of the device, and $I_{\text{d(rms)}}$ is the RMS value of the current following through the device. The switching loss generally consists of the capacitive C_{oss} loss, the V – I overlap loss, and the gate drive loss. In this analysis, the gate drive loss is neglected since it is typically much smaller than the other two types of switching losses at heavy-load conditions. According to [4], the V – I overlap loss can be assumed to be negligible to obtain the minimum hard-switching energy dissipated per cycle in a half-bridge (HB) consisting of two identical devices:

$$E_{\text{sw,HB}} = C_{\text{oss,Q}} V_{\text{dc}}^2, \quad (\text{A.3})$$

where $C_{\text{oss,Q}}$ represents the charge-equivalent output capacitance [2, 3] of the devices, and V_{dc} denote the dc-link voltage. Assuming the two devices are identical and thus generate the same switching loss, the minimum switching loss in one semiconductor device operating at a switching frequency of f_{sw} is

$$P_{\text{sw}} = \frac{1}{2} f_{\text{sw}} C_{\text{oss,Q}} V_{\text{dc}}^2. \quad (\text{A.4})$$

Substituting (A.2) and (A.4) into (A.1) yields the minimum total loss of a hard-switched semiconductor device as

$$P_{\text{semi}} = R_{\text{ds,on}} I_{\text{d(rms)}}^2 + \frac{1}{2} f_{\text{sw}} C_{\text{oss,Q}} V_{\text{dc}}^2. \quad (\text{A.5})$$

A.2 Derivation of Switching Device Figure-of-Merit

To derive the switching device FOM, we rewrite the on-state resistance ($R_{\text{ds,on}}$) and charge-equivalent output capacitance ($C_{\text{oss,Q}}$) as the area-specific forms:

$$R_{\text{ds,on}} = \frac{R'_{\text{ds,on}}}{A_{\text{die}}} \quad (\text{A.6})$$

$$C_{\text{oss,Q}} = C'_{\text{oss,Q}} A_{\text{die}}, \quad (\text{A.7})$$

where A_{die} is the device die area; $R'_{\text{ds,on}}$ and $C'_{\text{oss,Q}}$ are the area-specific on-state resistance and the area-specific charge-equivalent output capacitance, respectively.

Therefore, the semiconductor device loss given in (A.5) can be rewritten as a function of the die area as

$$P_{\text{semi}}(A_{\text{die}}) = I_{\text{d(rms)}}^2 \frac{R'_{\text{ds,on}}}{A_{\text{die}}} + \frac{1}{2} f_{\text{sw}} C'_{\text{oss,Q}} V_{\text{dc}}^2 A_{\text{die}}. \quad (\text{A.8})$$

This loss function can be minimized with the optimal die area that balances the conduction and switching losses (i.e, $P_{\text{cond}} = P_{\text{sw}}$), and the minimized semiconductor device loss is

$$P_{\text{semi(min)}} = V_{\text{dc}} I_{\text{d(rms)}} \sqrt{\frac{1}{2} f_{\text{sw}} R'_{\text{ds,on}} C'_{\text{oss,Q}}}. \quad (\text{A.9})$$

For a device operating at given dc-link voltage (V_{dc}), RMS current ($I_{\text{d(rms)}}$), and switching frequency (f_{sw}), this minimized semiconductor device loss is proportional to $\sqrt{R'_{\text{ds,on}} C'_{\text{oss,Q}}}$. Note that

$$R'_{\text{ds,on}} C'_{\text{oss,Q}} = R_{\text{ds,on}} C_{\text{oss,Q}}, \quad (\text{A.10})$$

according to (A.6) and (A.7). This means

$$P_{\text{semi(min)}} = V_{\text{dc}} I_{\text{d(rms)}} \sqrt{\frac{1}{2} f_{\text{sw}} R_{\text{ds,on}} C_{\text{oss,Q}}} \propto \sqrt{R_{\text{ds,on}} C_{\text{oss,Q}}}. \quad (\text{A.11})$$

Therefore, the switching device FOM can be defined as

$$\text{Switching device FOM} \triangleq \sqrt{R_{\text{ds,on}} C_{\text{oss,Q}}}. \quad (\text{A.12})$$

A.3 Derivation of Extended Normalized Switch Stress

To incorporate the semiconductor performance scaling, the voltage dependence of the area-specific on-state resistance ($R'_{\text{ds,on}}$) and the area-specific charge-equivalent output capacitance ($C'_{\text{oss,Q}}$) has to be considered. With technology-specific constants (k_{R} and k_{C}) and voltage-scaling factors (α_{R} and α_{C}), $R'_{\text{ds,on}}$ and $C'_{\text{oss,Q}}$ can be expressed as the following exponential functions of the device's voltage rating (V_{rated}):

$$R'_{\text{ds,on}} = k_{\text{R}} V_{\text{rated}}^{\alpha_{\text{R}}} \quad (\text{A.13})$$

$$C'_{\text{oss,Q}} = k_{\text{C}} V_{\text{rated}}^{\alpha_{\text{C}}}, \quad (\text{A.14})$$

where k_R , k_C , $R'_{ds,on}$, and $C'_{oss,Q}$ can be obtained through curve-fitting for each device technology (e.g., Si, SiC, and GaN) with empirical data [4]. In this analysis, we assume that there are devices available at any voltage rating. Under this assumption, we can rate each device exactly at its peak blocking voltage:

$$V_{rated} = V_{ds}. \quad (A.15)$$

Also, note that the peak blocking voltage (V_{ds}) across a device in a half-bridge is equal to the dc-link voltage (V_{dc}):

$$V_{ds} = V_{dc}. \quad (A.16)$$

With (A.13)-(A.16), equation (A.9) can be extended as

$$\begin{aligned} P_{semi(min)} &= V_{ds}^{1+\frac{\alpha_R+\alpha_C}{2}} I_{d(rms)} \sqrt{\frac{1}{2} f_{sw} k_R k_C} \\ &\propto V_{ds}^{1+\frac{\alpha_R+\alpha_C}{2}} I_{d(rms)}. \end{aligned} \quad (A.17)$$

Therefore, $V_{ds}^{1+\frac{\alpha_R+\alpha_C}{2}} I_{d(rms)}$ can be defined as an extended switch VA stress. By replacing the VA product in (11.2) with this extended VA stress and keeping it dimensionless through normalization, we obtain the extended normalized switch stress

$$M_{S(ext)} = \frac{\sum_{\text{switches}} V_{ds,i}^{1+\frac{\alpha_R+\alpha_C}{2}} I_{d(rms),i}}{V_{out}^{1+\frac{\alpha_R+\alpha_C}{2}} I_{out}}. \quad (A.18)$$

Appendix B

Derivation of General Output Impedance Model for Pure and Resonant Switched-Capacitor Converters

B.1 Detailed Model Derivation for Pure Switched-Capacitor Converters

Denote

$$\begin{cases} \hat{i}_k(t) = \hat{I}_{0k} e^{-\frac{t}{\tau_k}} \\ \hat{I}_{0k} = I_{0k} - I_{fk} \end{cases} \quad (\text{B.1})$$

and

$$\hat{q}_k = \int_0^{T_{k(\text{eff})}} \hat{i}_k(t) dt = \hat{I}_{0k} \tau_k \left(1 - e^{-\frac{T_{k(\text{eff})}}{\tau_k}} \right). \quad (\text{B.2})$$

Then

$$i_k = \hat{i}_k + I_{fk} \quad (\text{B.3})$$

so that the transferred charge in phase k can be calculated as

$$q_k = \int_0^{T_{k(\text{eff})}} i_k(t) dt = \hat{q}_k + I_{fk} T_{k(\text{eff})}. \quad (\text{B.4})$$

On the other hand, q_k and I_{out} can be expressed as

$$\begin{cases} q_k = a_k q_{\text{out}} \\ I_{\text{out}} = f_{\text{sw}} q_{\text{out}} \end{cases} \quad (\text{B.5})$$

where q_{out} is the total transferred charge to the output in a switching cycle.

Substituting (2.6) and (B.5) into (B.4) yields the relationship between $\hat{q}_k$ and q_{out} as

$$\hat{q}_k = \hat{a}_k q_{\text{out}} \quad (\text{B.6})$$

in which the coefficient $\hat{a}_k$ has been given in (2.9).

Substituting (B.1) and (B.6) into (B.2) yields

$$\hat{I}_{0k} = \frac{\hat{a}_k q_{\text{out}}}{\tau_k \left(1 - e^{-\frac{T_{k(\text{eff})}}{\tau_k}} \right)}. \quad (\text{B.7})$$

Denote

$$\hat{E}_k = \int_0^{T_{k(\text{eff})}} R_k \hat{i}_k^2(t) dt = \frac{R_k \hat{I}_{0k}^2 \tau_k}{2} \left(1 - e^{-\frac{2T_{k(\text{eff})}}{\tau_k}} \right). \quad (\text{B.8})$$

Then substituting (B.5) and (B.7) into (B.8) yields the expression of $\hat{R}_{\text{out}}$ that has been given in (2.9) as

$$\hat{R}_{\text{out}} = \frac{f_{\text{sw}} \sum_k \hat{E}_k}{I_{\text{out}}^2} = \frac{1}{2f_{\text{sw}}} \sum_k \frac{\hat{a}_k^2}{C_{k(\text{eff})}} \coth \left(\frac{T_{k(\text{eff})}}{2\tau_k} \right). \quad (\text{B.9})$$

Substituting (B.3) and (B.8) into (2.3) yields

$$E_k = \hat{E}_k + R_k I_{fk} (2\hat{q}_k + I_{fk} T_{k(\text{eff})}). \quad (\text{B.10})$$

Additively combing (B.10) over all phases and substituting the summation into (2.1) and (2.2) yields the final expression of R_{out} that has been given in (2.8) as

$$\begin{aligned} R_{\text{out}} &= \frac{f_{\text{sw}} \sum_k E_k}{I_{\text{out}}^2} \\ &= \frac{f_{\text{sw}} \sum_k \hat{E}_k}{I_{\text{out}}^2} + \frac{f_{\text{sw}} \sum_k R_k I_{fk} (2\hat{q}_k + I_{fk} T_{k(\text{eff})})}{I_{\text{out}}^2} \\ &= \hat{R}_{\text{out}} + \sum_k R_k p_k (2a_k - p_k f_{\text{sw}} T_{k(\text{eff})}). \end{aligned} \quad (\text{B.11})$$

B.1.1 Model Approximation by Taylor Expansion

By Taylor expansion, the hyperbolic function $\coth(x)$ ($x > 0$) can be approximated as

$$\coth(x) \approx \begin{cases} \frac{1}{x} + \frac{x}{3}, & 0 < x \leq \sqrt{3} \\ 1, & x > \sqrt{3} \end{cases}. \quad (\text{B.12})$$

For simplicity, here we consider a two-phase SC converter with 50% duty ratio and negligible deadtime (i.e. $T_{1(\text{eff})} = T_{2(\text{eff})} = \frac{1}{2f_{\text{sw}}}$). Substituting (B.12) into (2.8) yields the contribution of phase k ($k = 1, 2$) to R_{out} as

$$\begin{cases} 2R_k \left[p_k \left(a_k - \frac{p_k}{4} \right) + \frac{\hat{a}_k^2}{4f_{\text{sw}}\tau_k} \right], & 0 < 4f_{\text{sw}}\tau_k < \frac{1}{\sqrt{3}} \\ 2R_k \left[a_k^2 + \frac{1}{3} \cdot \frac{\hat{a}_k^2}{(4f_{\text{sw}}\tau_k)^2} \right], & 4f_{\text{sw}}\tau_k \geq \frac{1}{\sqrt{3}} \end{cases}. \quad (\text{B.13})$$

Substituting the topology-dependent parameters mentioned in Section 2.3.1 and additively combining the components in all phases yields the SSM and FSM for the 2-to-1 SC converter that has been given in (2.12) and (2.13).

B.2 Detailed Model Derivation for Resonant Switched-Capacitor Converters

As explained in Section 3.2, to derive the general output impedance model shown in (3.11), we need to first obtain the unknowns A_k and φ_k in (3.4) which give the analytical expression of i_k and then calculate the output impedance with i_k through (3.1)-(3.3).

B.2.1 Calculation of A_k and φ_k

To calculate A_k and φ_k , two additional conditions are needed: a) the continuity of inductor current that is mathematically described in (3.7), and b) the charge balance in the flying capacitor(s) as as been described in (3.9).

First, with the continuity of inductor current, we can substitute (3.4) into (3.7) and obtain (B.14).

$$\begin{cases} A_1 \cos(\varphi_1) + I_{\text{f1}} = A_2 e^{-\beta_2} \cos(\gamma_2 + \varphi_2) + I_{\text{f2}} & (\text{B.14a}) \\ A_2 \cos(\varphi_2) + I_{\text{f2}} = A_1 e^{-\beta_1} \cos(\gamma_1 + \varphi_1) + I_{\text{f1}} & (\text{B.14b}) \end{cases}$$

where β_k and γ_k ($k = 1, 2$) have been defined in (3.13).

Second, with the charge balance in the flying capacitor(s), we can substitute (3.4) into (3.9)-(3.10) and obtain (B.15).

To solve for φ_1 , we need to 1) express A_1 in terms of φ_1 , and 2) substitute A_1 into (B.15a) for $\tan(\varphi_1)$.

$$\left\{ \begin{array}{l} \frac{A_1}{\omega_{01}^2} \{ \omega_1 [e^{-\beta_1} \sin(\gamma_1 + \varphi_1) - \sin(\varphi_1)] - \alpha_1 [e^{-\beta_1} \cos(\gamma_1 + \varphi_1) - \cos(\varphi_1)] \} + I_{f1} D_1 T = a_1 I_{\text{out}} T \\ \frac{A_2}{\omega_{02}^2} \{ \omega_2 [e^{-\beta_2} \sin(\gamma_2 + \varphi_2) - \sin(\varphi_2)] - \alpha_2 [e^{-\beta_2} \cos(\gamma_2 + \varphi_2) - \cos(\varphi_2)] \} + I_{f2} D_2 T = a_2 I_{\text{out}} T \end{array} \right. \quad (\text{B.15a})$$

$$\left\{ \begin{array}{l} \frac{A_1}{\omega_{01}^2} \{ \omega_1 [e^{-\beta_1} \sin(\gamma_1 + \varphi_1) - \sin(\varphi_1)] - \alpha_1 [e^{-\beta_1} \cos(\gamma_1 + \varphi_1) - \cos(\varphi_1)] \} + I_{f1} D_1 T = a_1 I_{\text{out}} T \\ \frac{A_2}{\omega_{02}^2} \{ \omega_2 [e^{-\beta_2} \sin(\gamma_2 + \varphi_2) - \sin(\varphi_2)] - \alpha_2 [e^{-\beta_2} \cos(\gamma_2 + \varphi_2) - \cos(\varphi_2)] \} + I_{f2} D_2 T = a_2 I_{\text{out}} T \end{array} \right. \quad (\text{B.15b})$$

$$\omega_2 [e^{-\beta_2} A_2 \sin(\gamma_2 + \varphi_2) - A_2 \sin(\varphi_2)] - \alpha_2 [e^{-\beta_2} A_2 \cos(\gamma_2 + \varphi_2) - A_2 \cos(\varphi_2)] = \omega_{02}^2 (a_2 I_{\text{out}} - D_2 I_{f2}) T \quad (\text{B.16})$$

$$\left\{ \begin{array}{l} A_2 \sin(\gamma_2 + \varphi_2) = \sin(\gamma_2) [A_2 \cos(\varphi_2)] + \cos(\gamma_2) [A_2 \sin(\varphi_2)] \\ A_2 \cos(\varphi_2) = A_1 e^{-\beta_1} \cos(\gamma_1 + \varphi_1) + I_{f1} - I_{f2} \end{array} \right. \quad (\text{B.17a})$$

$$\left\{ \begin{array}{l} A_2 \cos(\varphi_2) = A_1 e^{-\beta_1} \cos(\gamma_1 + \varphi_1) + I_{f1} - I_{f2} \\ e^{-\beta_2} A_2 \cos(\gamma_2 + \varphi_2) = A_1 \cos(\varphi_1) + I_{f1} - I_{f2} \end{array} \right. \quad (\text{B.17b})$$

$$\left\{ \begin{array}{l} A_2 \cos(\varphi_2) = A_1 e^{-\beta_1} \cos(\gamma_1 + \varphi_1) + I_{f1} - I_{f2} \\ e^{-\beta_2} A_2 \cos(\gamma_2 + \varphi_2) = A_1 \cos(\varphi_1) + I_{f1} - I_{f2} \end{array} \right. \quad (\text{B.17c})$$

$$e^{-\beta_2} \{ \cos(\gamma_2) [A_2 \cos(\varphi_2)] - \sin(\gamma_2) [A_2 \sin(\varphi_2)] \} = A_1 \cos(\varphi_1) + I_{f1} - I_{f2} \quad (\text{B.18})$$

$$A_2 \sin(\varphi_2) = \frac{\cos(\gamma_2) [A_1 e^{-\beta_1} \cos(\gamma_1 + \varphi_1) + I_{f1} - I_{f2}] - e^{\beta_2} [A_1 \cos(\varphi_1) + I_{f1} - I_{f2}]}{\sin(\gamma_2)} \quad (\text{B.19})$$

$$A_1 = \frac{e^{\beta_1} I_{\text{out}} T}{\cos(\varphi_1)} \cdot \frac{(a_2 - p_2 D_2) \omega_{02}^2 \cdot \frac{\sin(\gamma_2)}{\omega_2} - 2(p_1 - p_2) f_{\text{sw}} [\cosh(\beta_2) - \cos(\gamma_2)]}{P_{1,1} \cos(\gamma_1) + e^{\beta_1} P_{1,2} - P_{1,1} \sin(\gamma_1) \tan(\varphi_1)} \quad (\text{B.20})$$

1) *Express A_1 in terms of φ_1 .* Rearrange (B.15b) as (B.16). To express A_1 in terms of φ_1 , we need to substitute A_2 and φ_2 for A_1 and φ_1 in (B.16), meaning $A_2 \sin(\gamma_2 + \varphi_2)$, $A_2 \sin(\varphi_2)$, $A_2 \cos(\gamma_2 + \varphi_2)$, and $A_2 \cos(\varphi_2)$ should be expressed in terms of A_1 and φ_1 . According to the trigonometric angle sum identity and (B.15), $A_2 \sin(\gamma_2 + \varphi_2)$, $A_2 \cos(\gamma_2 + \varphi_2)$, and $A_2 \cos(\varphi_2)$ can be expressed as (B.17). To solve for $A_2 \sin(\varphi_2)$, first expand (B.17c) as (B.18) and then substitute (B.17b) into it, yielding (B.19). Substituting (B.17) and (B.19) into (B.16) gives the expression of A_1 in terms of φ_1 as (B.20), in which $P_{1,1}$ and $P_{1,2}$ follow the same definition in (3.13).

2) *Solve for $\tan(\varphi_1)$.* Substituting (B.20) into (B.15a) yields an equation in terms of $\tan(\varphi_1)$, with which we can solve for $\tan(\varphi_1)$ as

$$\tan(\varphi_1) = \frac{P_{1,1} \cos(\gamma_1) + e^{\beta_1} P_{1,2} + P_{1,3} M_{1,2}}{P_{1,1} \sin(\gamma_1) - P_{1,3} M_{1,1}} \quad (\text{B.21})$$

where $P_{1,1}$, $P_{1,2}$, $P_{1,3}$, $M_{1,1}$, and $M_{1,2}$ follow the same definition in (3.13).

Similarly, we can obtain $\tan(\varphi_2)$ in the same way as how we solve for $\tan(\varphi_1)$ above. Denote

$$T_k = \tan(\varphi_k) \quad (k = 1, 2). \quad (\text{B.22})$$

which is actually the same as the T_k defined in (3.13).

With T_1 and T_2 calculated in (3.13), A_1 and A_2 can be determined by substituting T_1 and T_2 into (B.20). However, to calculate the output impedance, the explicit expressions of A_1 and A_2 do not need to be obtained. Instead, they can be substituted with T_1 and T_2 in the calculation, which will be explained in the next subsection.

B.2.2 Calculation of the output impedance

Denote

$$\hat{i}_k(t) = A_k e^{-\alpha_k t} \cos(\omega_k t + \varphi_k) \quad (\text{B.23})$$

and

$$\hat{E}_k = \int_0^{D_k T} R_k \hat{i}_k^2(t) dt. \quad (\text{B.24})$$

Then

$$i_k = \hat{i}_k + I_{fk}. \quad (\text{B.25})$$

Therefore, the conduction energy loss in phase k can be calculated as

$$E_k = \int_0^{D_k T} R_k i_k^2(t) dt. \quad (\text{B.26})$$

Substituting (3.5), (3.9) and (B.25) into (B.26) gives

$$E_k = \hat{E}_k + R_k p_k (2a_k - D_k p_k) T I_{\text{out}}^2. \quad (\text{B.27})$$

To calculate $\hat{E}_k$, we can substitute (B.23) into (B.24) and obtain

$$\hat{E}_k = \frac{R_k}{4} \cdot \left(\frac{A_k e^{-\beta_k}}{\omega_{0k}} \right)^2 \cdot [G_k + H_{k,1} \sin(2\varphi_k) + H_{k,2} \cos(2\varphi_k)] \quad (\text{B.28})$$

where G_k , $H_{k,1}$, and $H_{k,2}$ follow the same definition in (3.13). According to (B.15), $A_k^2 e^{-2\beta_k} / \omega_{0k}^2$ can be expressed as (B.29).

$$\frac{A_k e^{-\beta_k}}{\omega_{0k}} = \frac{(a_k - D_k p_k) \omega_{0k} I_{\text{out}} T}{\omega_k [\sin(\gamma_k + \varphi_k) - e^{\beta_k} \sin(\varphi_k)] - \alpha_k [\cos(\gamma_k + \varphi_k) - e^{\beta_k} \cos(\varphi_k)]} \quad (\text{B.29})$$

Note that

$$\begin{cases} \sin(2\varphi_k) = \frac{2 \tan(\varphi_k)}{1 + \tan^2(\varphi_k)} \\ \cos(2\varphi_k) = \frac{1 - \tan^2(\varphi_k)}{1 + \tan^2(\varphi_k)} \end{cases} \quad (\text{B.30})$$

According to (3.1) and (3.2), we can calculate the output impedance as

$$R_{\text{out}} = \frac{f_{\text{sw}} \sum_{k=1,2} E_k}{I_{\text{out}}^2}. \quad (\text{B.31})$$

Substituting (B.27)-(B.30) into (B.31) yields the final expression of R_{out} that has been given as (3.11).

Appendix C

Characteristic Vectors of State-of-the-Art 48-V-to-PoL Regulated Hybrid SC Topologies

Table [C.1](#) lists the characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature, including switch voltage stress vector $\hat{\mathbf{V}}_{\text{ds}}$, switch current stress vector $\hat{\mathbf{I}}_{\text{d(rms)}}$, capacitor voltage vector $\hat{\mathbf{V}}_{\text{C}}$ and capacitor charge vector $\hat{\mathbf{q}}_{\text{C}}$.

Table C.1: Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \quad N_L \quad N_C]$	$\hat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\hat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
Switching bus converter (SBC) [115, 119], [96]	$K_{SC} \in \{4k k \in \mathbb{N}, 1 \leq k \leq 6\}$ $[N_S \quad N_L \quad N_C] =$ $[2K_{SC} + 2 \quad K_{SC} \quad K_{SC} - 1]$	$\frac{1}{K_{SC}} \begin{bmatrix} \frac{K_{SC}}{2} \\ \frac{K_{SC}}{2} + 1 \\ \frac{K_{SC}}{2} - 1 \\ \frac{K_{SC}}{2} \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \left\{ \begin{array}{l} K_{SC-2} \\ K_{SC} \end{array} \right\}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \sqrt{1-D} \end{bmatrix} \left\{ \begin{array}{l} K_{SC+2} \\ K_{SC-2} \end{array} \right\}$	$\frac{1}{K_{SC}} \begin{bmatrix} \frac{K_{SC}}{2} \\ 1 \\ 1 \\ 2 \\ 2 \\ \vdots \\ \vdots \\ \frac{K_{SC}}{2} - 1 \\ \frac{K_{SC}}{2} - 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \left\{ \right\}_{N_C}$
SCB [60, 89]	• Multi-phase operation [60]: $K_{SC} \in \{k k \in \mathbb{N}, 2 \leq k \leq 6\}$ • Two-phase operation [89]: $K_{SC} \in \{2k k \in \mathbb{N}, 1 \leq k \leq 12\}$ $[N_S \quad N_L \quad N_C] =$ $[2K_{SC} \quad K_{SC} \quad K_{SC} - 1]$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \\ 1 \end{bmatrix} \left\{ \begin{array}{l} K_{SC-1} \\ K_{SC-1} \end{array} \right\}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \end{bmatrix} \left\{ \begin{array}{l} K_{SC-1} \\ K_{SC-1} \end{array} \right\}$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 2 \\ \vdots \\ N_C \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \left\{ \right\}_{N_C}$
Dickson ² [75]	$K_{SC} = 9$ $[N_S \quad N_L \quad N_C] =$ $[22 \quad 9 \quad 8]$	$\frac{1}{K_{SC}} \begin{bmatrix} 3 \\ 3 \\ 3 \\ 6 \\ 4 \\ 2 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \left\{ \begin{array}{l} 8 \\ 9 \end{array} \right\}$	$\frac{1}{N_L} \begin{bmatrix} \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \sqrt{1-D} \\ \sqrt{1-D} \end{bmatrix} \left\{ \begin{array}{l} 13 \\ 6 \end{array} \right\}$	$\frac{1}{K_{SC}} \begin{bmatrix} 6 \\ 3 \\ 2 \\ 2 \\ 2 \\ 1 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \left\{ \right\}_{N_C}$

TABLE C.1 (continued): Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \ N_L \ N_C]$	$\hat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\hat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
CaSP [64]	$K_{SC} = 6$ $[N_S \ N_L \ N_C] =$ $[11 \ 3 \ 3]$	$\frac{1}{K_{SC}} \left\{ \begin{array}{l} 3 \\ \vdots \\ 3 \\ 2 \\ 2 \\ 1 \\ \vdots \\ 1 \end{array} \right\} \begin{array}{l} 5 \\ \\ 4 \end{array}$	$\frac{1}{N_L} \left\{ \begin{array}{l} \sqrt{D/2} \\ \vdots \\ \sqrt{D/2} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \sqrt{1+2D} \\ \sqrt{1-D} \end{array} \right\} \begin{array}{l} 4 \\ \\ 4 \end{array}$	$\frac{1}{K_{SC}} \begin{bmatrix} 3 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$
MLB [65, 76]	$K_{SC} = 8$ $[N_S \ N_L \ N_C] =$ $[10 \ 2 \ 3]$	$\frac{1}{K_{SC}} \left\{ \begin{array}{l} 4 \\ \vdots \\ 4 \\ 2 \\ 2 \\ \vdots \\ 2 \\ 1 \\ 1 \end{array} \right\} \begin{array}{l} 4 \\ \\ 4 \end{array}$	$\frac{1}{N_L} \left\{ \begin{array}{l} \sqrt{D}/2 \\ \vdots \\ \sqrt{D}/2 \\ \sqrt{D/2} \\ \sqrt{D/2} \\ \sqrt{D/2} \\ \sqrt{D} \\ \sqrt{1+2D} \\ \sqrt{1-D} \end{array} \right\} \begin{array}{l} 4 \\ \\ 4 \end{array}$	$\frac{1}{K_{SC}} \begin{bmatrix} 4 \\ 2 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$

TABLE C.1 (continued): Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \quad N_L \quad N_C]$	$\hat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\hat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
LEGO [73, 83] Mini-LEGO [98, 114]	$K_{SC} = 6$ $[N_S \quad N_L \quad N_C] =$ $[40 \quad 12 \quad 5]$	$\frac{1}{K_{SC}} \left\{ \begin{array}{l} 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{array} \right\} \begin{array}{l} 4 \\ \\ 36 \end{array}$	$\frac{1}{N_L} \left\{ \begin{array}{l} \sqrt{2D} \\ \vdots \\ \sqrt{2D} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1-D} \\ \vdots \\ \sqrt{1-D} \end{array} \right\} \begin{array}{l} 16 \\ \\ 12 \\ 12 \end{array}$	$\frac{1}{K_{SC}} \begin{bmatrix} 5 \\ 4 \\ 3 \\ 2 \\ 1 \end{bmatrix}$	$\frac{7D}{N_L} \left\{ \begin{array}{l} 1 \\ 1 \\ \vdots \\ 1 \end{array} \right\}_{N_C}$
VIB [74, 77]	$K_{SC} = 8$ $[N_S \quad N_L \quad N_C] =$ $[40 \quad 16 \quad 15]$	$\frac{1}{K_{SC}} \left\{ \begin{array}{l} 4 \\ \vdots \\ 4 \\ 1 \\ \vdots \\ 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{array} \right\} \begin{array}{l} 8 \\ 4 \\ 12 \\ 16 \end{array}$	$\frac{1}{N_L} \left\{ \begin{array}{l} \sqrt{D/2} \\ \vdots \\ \sqrt{D/2} \\ \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \vdots \\ \sqrt{1-D} \end{array} \right\} \begin{array}{l} 8 \\ 16 \\ 12 \\ 4 \end{array}$	$\frac{1}{K_{SC}} \begin{bmatrix} 6 \\ 3 \\ 2 \\ 2 \\ 2 \\ 1 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \left\{ \begin{array}{l} 1 \\ 1 \\ \vdots \\ 1 \end{array} \right\}_{N_C}$

TABLE C.1 (continued): Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \quad N_L \quad N_C]$	$\hat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\hat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\hat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
MSC [97, 131]	$K_{SC} = 8$ $[N_S \quad N_L \quad N_C] =$ $[18 \quad 8 \quad 7]$	$\frac{1}{K_{SC}} \left\{ \begin{array}{c} 4 \\ 5 \\ 3 \\ 4 \\ 2 \\ \vdots \\ 2 \\ 1 \\ \vdots \\ 1 \end{array} \right\} \begin{array}{l} 6 \\ 8 \end{array}$	$\frac{1}{N_L} \left\{ \begin{array}{c} \sqrt{D} \\ \vdots \\ \sqrt{D} \\ \sqrt{1+2D} \\ \vdots \\ \sqrt{1+2D} \\ \sqrt{1-D} \\ \sqrt{1-D} \end{array} \right\} \begin{array}{l} 10 \\ 6 \end{array}$	$\frac{1}{K_{SC}} \begin{bmatrix} 4 \\ 1 \\ 1 \\ 2 \\ 2 \\ 3 \\ 3 \end{bmatrix}$	$\frac{D}{N_L} \left\{ \begin{array}{c} 1 \\ 1 \\ \vdots \\ 1 \end{array} \right\}^{N_C}$
Crossed- coupled QSD buck [70]	$K_{SC} = 4$ $[N_S \quad N_L \quad N_C] =$ $[8 \quad 2 \quad 3]$	$\frac{1}{K_{SC}} \left\{ \begin{array}{c} 2 \\ \vdots \\ 2 \\ 3 \\ 1 \\ \vdots \\ 1 \end{array} \right\} \begin{array}{l} 4 \\ 3 \end{array}$	$\frac{1}{N_L} \left\{ \begin{array}{c} \sqrt{D}/2 \\ \vdots \\ \sqrt{D}/2 \\ \sqrt{1+D/4} \\ \sqrt{1+D/4} \end{array} \right\} 6$	$\frac{1}{K_{SC}} \begin{bmatrix} 2 \\ 1 \\ 1 \end{bmatrix}$	$\frac{D}{N_L} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$

TABLE C.1 (continued): Characteristic vectors of state-of-the-art 48-V-to-PoL regulated hybrid SC topologies presented in previous literature

Topology	K_{SC} and $[N_S \quad N_L \quad N_C]$	$\widehat{\mathbf{V}}_{ds} \in \mathbb{R}^{N_S \times 1}$	$\widehat{\mathbf{I}}_{d(rms)} \in \mathbb{R}^{N_S \times 1}$	$\widehat{\mathbf{V}}_C \in \mathbb{R}^{N_C \times 1}$	$\widehat{\mathbf{q}}_C \in \mathbb{R}^{N_C \times 1}$
DIH [81, 129]	$K_{SC} \in \{2k k \in \mathbb{N},$ $2 \leq k \leq 12\}$ $[N_S \quad N_L \quad N_C] =$ $[K_{SC} + 2 \quad 2 \quad K_{SC} - 1]$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ 1 \end{bmatrix} \left\}^{K_{SC}-1} \frac{1}{N_L} \right.$	$\begin{bmatrix} 2\sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ 2\sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ 2\sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \vdots \\ 2\sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \sqrt{1+2D} \\ \sqrt{1+2D} \end{bmatrix} \left\}^{K_{SC}-2} \frac{1}{K_{SC}} \begin{bmatrix} K_{SC}-1 \\ K_{SC}-2 \\ \vdots \\ 1 \end{bmatrix} \frac{2D}{N_L K_{SC}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \right\}^{N_C}$		
SDIH [82, 130]	$K_{SC} \in \{2k k \in \mathbb{N},$ $2 \leq k \leq 12\}$ $[N_S \quad N_L \quad N_C] =$ $[2K_{SC} + 2 \quad 2 \quad 2K_{SC} - 2]$	$\frac{1}{K_{SC}} \begin{bmatrix} 1 \\ 1 \\ 2 \\ \vdots \\ 2 \\ 1 \\ 1 \end{bmatrix} \left\}^{2K_{SC}-2} \frac{1}{N_L} \right.$	$\begin{bmatrix} \sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ \vdots \\ \sqrt{\frac{2D}{K_{SC}(K_{SC}+2)}} \\ \sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \vdots \\ \sqrt{\frac{D}{(K_{SC}-2)(K_{SC}+2)}} \\ \sqrt{1+2D} \\ \sqrt{1+2D} \end{bmatrix} \left\}^4 \frac{1}{K_{SC}} \begin{bmatrix} K_{SC}-1 \\ K_{SC}-1 \\ K_{SC}-2 \\ K_{SC}-2 \\ \vdots \\ \vdots \\ 1 \\ 1 \end{bmatrix} \frac{D}{N_L K_{SC}} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \right\}^{N_C}$		

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