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Stress and Fracture of Crystalline Silicon Cells in Solar Photovoltaic Modules – A Synchrotron X-ray Microdiffraction based Investigation

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ABSTRACT

Fracture of crystalline silicon (c-Si) solar cells in photovoltaic modules is a big concern to the photovoltaics (PV) industry. Cell cracks cause performance degradation and warranty issues to the manufacturers. The roots of cell fractures lie in the manufacturing and integration process of the cells and modules as they go through a series of elevated temperature and pressure processes, involving bonding of dissimilar materials, causing residual stresses. Evaluation of the exact physical mechanisms leading to these thermomechanical stresses is highly essential to quantify them and optimize the PV modules to address them. We present a novel synchrotron X-ray microdiffraction based techniques to characterize the stress and fracture in the crystalline silicon PV modules. We show the detailed stress state after soldering and lamination process, using the synchrotron X-ray microdiffraction experiments. We also calculate the maximum tolerable microcrack size in the c-Si cells to sustain the residual stress after lamination. We further demonstrate the effect of these residual stresses on the cell fractures using the widely accepted fracture (4-point bending) tests. These test results show that the soldering and lamination induced localized residual stresses indeed reduce the load-carrying capacity of the c-Si cells.

1. INTRODUCTION:

Fracture of crystalline silicon (c-Si) solar cells in photovoltaic (PV) modules is a well-known issue and a major concern to the PV industry [1-10]. Crystalline silicon solar cells contain microcracks (length < 1 mm) that originated from the wafer slicing process, which reduces their mechanical strength [11-13]. Etching processes are used to minimize the defects or microcracks in the as-cut wafers, leading to the increased mechanical strength of the etched silicon wafers [14, 15]. However, it should be noted that the complete removal of defects or microcracks is not possible, due to processing time and cost limitations. The PV module integration processes, soldering, and encapsulation induces thermomechanical deformations and residual stresses in PV modules and cells [5-10]. Apart from these residual stresses, loads due to mechanical handling of cells during various operations could also cause momentary high stresses and lead to the propagation of microcracks [16]. However, the high residual stresses due to soldering and lamination could act as crack localization points to propagate the microcracks in the c-Si cells upon further loading due to handling, transportation, installation and operation of the modules [6, 8-10]. Especially in the case of thin c-Si wafer (< 180 μm) cells, the effect of these residual stresses is much more intense due to the increased fragility of the thin cells [7, 9]. In this scenario, the quantitative characterization of these residual stresses is highly necessary to estimate their effect on the cell fractures and damage tolerance, and also to identify the physical mechanism that drives these high residual stresses. There are only a few quantitative stress characterization techniques that exist for the c-Si wafers and cells [17-19]. However, these techniques are not proven to quantitatively probe the stresses in the encapsulated c-Si cells, except the very recently reported Raman based technique [20]. Synchrotron scanning X-ray microdiffraction (μSXRD) was recently proven by our group to be capable of penetrating the encapsulated c-Si cells to probe the stress in silicon [21, 22]. We developed a μSXRD based stress evaluation methodology, which could probe the localized stress in the encapsulated c-Si cells. Using this method, the highly localized stress near the solder joints in the c-Si cells could be quantitatively determined and we demonstrated the elegance of this method in the case of interdigitated back contact (IBC) c-Si cells in our earlier reports [23, 24]. Apart from the microdiffraction, various other synchrotron X-ray probing techniques were used by research groups in the world to characterize the solar cells and PV modules [25-33]. For e.g. Colli *et al.*, 2016 [30], Meng *et al.*, 2017 [32], and Meng *et al.*, 2018 [33] used X-ray topography to correlate the defects and deformations of the encapsulated silicon cells.

In this research paper we report the residual stress near soldered copper ribbons in the generic design single crystalline silicon (sc-Si) cells, for post-soldering and post-lamination conditions, using the μSXRD technique. Further, we present simplified linear elastic fracture mechanics (LEFM) based calculations to evaluate the maximum tolerable crack length of the c-Si cells to sustain the residual stresses, based on our quantitative residual stress characterization. Finally, we show the significant effect of residual stress on the cell fracture strength through the widely accepted fracture testing procedure.

2. MATERIALS AND METHODS:

2.1 Experimental Samples

In this experimental study we used standard generic design sc-Si solar cells of thickness 0.18 mm, with three busbars (3BB). The cell has continuous silver busbars and grid of silver finger on the front side and aluminium back surface field (Al-BSF) contact layer on the backside, as shown in Figure 1(a). The cells were soldered on an automatic solar cell stringer machine, with a typical lead-free solder (Sn3.9Ag0.6Cu) coated Cu ribbons. The thickness and width of the ribbon are 0.18 mm and 1.8 mm respectively. The thickness of the solder layer over the ribbon is ~0.02 mm. Single-cell PV module samples, as shown in Figure 1(b), were later prepared by encapsulating these soldered cells in a semiautomatic photovoltaic module laminator at 150 ^{o}C under 0.1 MPa vacuum pressure. The front layer of the sample PV modules is made of tempered glass sheet of thickness 3.2 mm and the encapsulant is EVA. A detailed description of the lamination process is given in our earlier report [23]. Further, we also prepared two different sets of mini PV modules with soldered and unsoldered (pristine) cells for fracture testing, as shown in Figure 2.

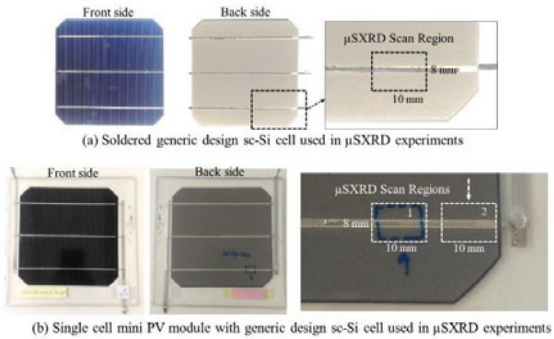

Figure 1: Samples of silicon cells and mini PV modules used in μSXRD experiments

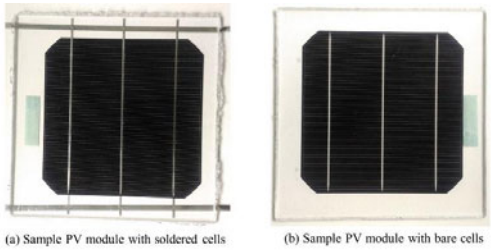

Figure 2: Sample mini PV modules used in fracture testing

2.2 Experimental Setup of Synchrotron Scanning X-ray Microdiffraction

The synchrotron scanning X-ray microdiffraction (μSXRD) experiments were conducted at the beamline 12.3.2 at the advanced light source (ALS) of Lawrence Berkeley national laboratory (LBNL), Berkeley [34, 35]. The energy bandpass of the X-ray beam at this beamline is 5 keV to 25 keV. A schematic of the experimental setup of synchrotron X-ray microdiffraction of a PV module sample is shown in Figure 3(a) and the actual experimental setup is shown in Figure 3(b). In this technique, the sample is subjected to a high intensity polychromatic X-ray beam of submicron size (~ 0.8 μm) and the resulting diffraction pattern is recorded by the X-ray detector mounted over the sample stage. This is a reflection experiment, where the detector is perpendicular to the incident X-ray beam and the sample is mounted at 45° to the incident X-ray beam as shown in Figure 3(a). The samples are raster-scanned over a grid of points in the scanned regions (refer to Figure 1). The distance between each scanned point in X and Y directions is 0.1 mm and the exposure time at each scan point is ~ 90 sec. This calls for a scan time of ~ 3 – 4 hours for a scan area of 10 x 8 mm^2. The sample is scanned from the backside of the cell, as the front glass in the sample PV module absorbs X-rays.

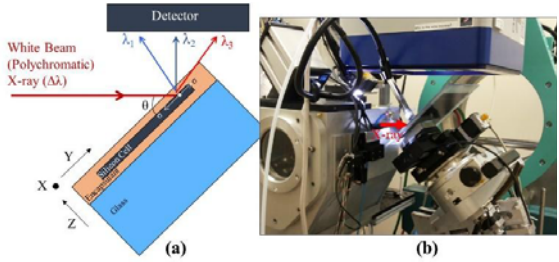

Figure 3: μSXRD setup of mini PV module (a) Schematic, (b) Actual picture

The polychromatic (Laue) diffraction patterns, recorded at each scan point are pre-processed (indexed) using a specialized software XMAS [36]. This gives the crystal structure, crystal plane misorientation and deviatoric stress in the silicon cells, at each scanned point. During mounting the soldered cells on the sample stage, no change in the as-soldered deformation and stress state of the cells was ensured to get accurate results. No such precautions are required for encapsulated cells (sample PV modules). A more detailed description of the experimental procedure is presented in our earlier reports [22, 23]. Further, a more detailed description of the beamline construction and the experimental procedure is available elsewhere [34 - 36].

2.3 Curvature Based Stress Evaluation from μSXRD Data

Figure 4(a) shows a schematic of the μSXRD scan region and the crystal plane misorientation angles φ_x and φ_y about the X and Y axes respectively. The pre-processing of the μSXRD scans gives the crystal plane misorientation angles, as explained in the previous section. As stated earlier, we developed a curvature-based stress evaluation methodology to accurately characterize the residual stress in the sc-Si cells [23], which is

briefly explained here. As shown in the schematic in Figure 4(b), the crystal plane misorientation angle about X-axis, φ_x defines the change of orientation of the deformed crystal plane of the sc-Si cell with respect to the undeformed silicon. From this, we can calculate the curvature of the cell in the YZ plane (around X-axis) using equation 1. Similarly, we can calculate the curvature of the cell in the XZ plane (around Y-axis) from the misorientation angle φ_y, as shown in equation 2. Note that the negative sign in equation 2 is because of moving the sample stage while keeping the X-ray beam constant.

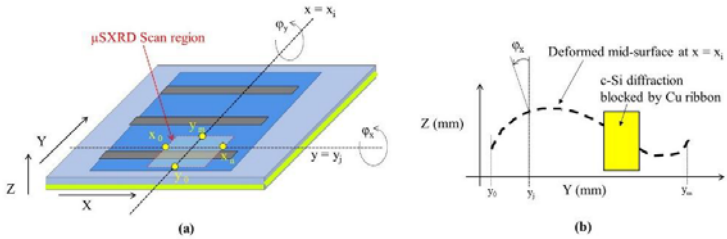

Figure 4: (a) Schematic of μSXRD scan region, showing crystal plane misorientation angles, (b) Schematic of deformed mid-surface of the c-Si cell across the Cu ribbon.

$$\kappa_{yy} = \frac{\partial \varphi_x}{\partial y}\Big|_{x=const}, \ \varphi_x \text{ in radians} \tag{1}$$

$$\kappa_{xx} = -\frac{\partial \varphi_y}{\partial x}\Big|_{y=const}, \ \varphi_y \text{ in radians} \tag{2}$$

From these curvatures, the respective bending strains in the cell can be calculated using equations 3 and 4.

$$\varepsilon_{xx} = -\frac{t}{2}\kappa_{xx}, \tag{3}$$

$$\varepsilon_{yy} = -\frac{t}{2}\kappa_{yy} \tag{4}$$

As the sc-Si cell is an anisotropic material with its sides parallel to <100> and <010> crystal directions and the surface normal to <001> direction, its elasticity tensor is defined by equation 5, where the individual modulus values are in GPa.

$$C = \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{21} & C_{22} & C_{23} & 0 & 0 & 0 \\ C_{31} & C_{32} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{55} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{66} \end{bmatrix} = \begin{bmatrix} 166 & 64 & 64 & 0 & 0 & 0 \\ 64 & 166 & 64 & 0 & 0 & 0 \\ 64 & 64 & 166 & 0 & 0 & 0 \\ 0 & 0 & 0 & 80 & 0 & 0 \\ 0 & 0 & 0 & 0 & 80 & 0 \\ 0 & 0 & 0 & 0 & 0 & 80 \end{bmatrix} \tag{5}$$

The stresses in the cell in X and Y directions can be calculated from these strains using Hooke's law. As the cell is thin (thickness 0.18 mm) compared to its surface area (156 x

156 mm^2), it can be assumed to have a plane stress condition, leading to the stress in the normal direction to be zero, as given in equation 6. Substituting equations 3, 4, 5 and 6 in Hooke's law, we can calculate the bending stresses in the cell in X and Y directions, as shown in equations 7 and 8.

$$\sigma_{zz} = 0 \tag{6}$$

$$\sigma_{xx} = \left(C_{11} - \frac{C_{12}^2}{C_{11}}\right)\varepsilon_{xx} + \left(C_{12} - \frac{C_{12}^2}{C_{11}}\right)\varepsilon_{yy} \tag{7}$$

$$\sigma_{yy} = \left(C_{12} - \frac{C_{12}^2}{C_{11}}\right)\varepsilon_{xx} + \left(C_{11} - \frac{C_{12}^2}{C_{11}}\right)\varepsilon_{yy} \tag{8}$$

We subject the backside of the sample to the X-ray diffraction. The synchrotron X-ray beam passes through the thickness of the silicon cell. However, the energy of the beam gets attenuated as it passes through the silicon and hence, the diffraction signal is more biased towards the backside of the sample. As we use the crystal plane misorientation angles, which remain the same throughout the thickness of the deformed cell, our curvature-based stress evaluation is free from the averaging of tensile and compressive stresses. In fact, we adopt this methodology for the very reason as the deviatoric stress, directly evaluated from the Laue-diffraction analysis is affected by the averaging of stress in the probe volume.

2.4 Fracture Testing

Figure 5(a) shows a schematic of the fracture testing by 4-point bend (4PB) setup. The loading span, l is 80mm and the support span L is 170 mm. Figure 5(b) shows the actual 4PB test setup on Instron 5982 mechanical tester. This setup is used to test the fracture strength (load at fracture) of the sc-Si cells in mini PV modules shown in Figure 2. The change of slope in the load-deflection curve, as indicated in Figure 5(c) is used to identify the cell cracks. In the case of samples with soldered cells, electroluminescence (EL) imaging is performed before and after fracture testing to visualize the cracked cells.

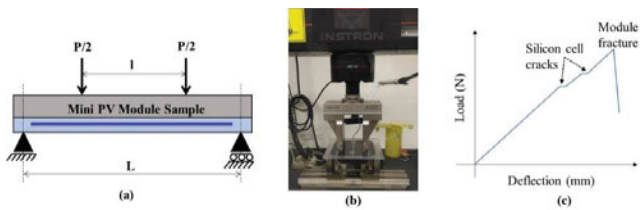

Figure 5: (a) Schematic and (b) Actual picture of the 4-point bending test of mini PV module sample on Instron 5982 mechanical tester, (c) Typical load-deflection curve, indicating silicon cracks and final module fracture.

3. RESULTS AND DISCUSSION:

3.1 State of Residual Stress after Soldering and Lamination

Figures 6(a) and 6(b) show the residual stress maps of the backside of the scanned region in the soldered cells. The maximum residual tensile stress in both X and Y directions is ~30 MPa after soldering. These stress maps correspond to a region where the cell is soldered to the Cu ribbons on both front and back sides. Due to the symmetry of the Cu-Si-Cu solder joint, the soldering induced CTE mismatch (differential contraction of silicon and copper) leads to compressive stress in the silicon in the joined region (white region in the experimental stress maps with no stress measurement due to the blockage of the X-ray beam from the silicon cell by the copper ribbon).

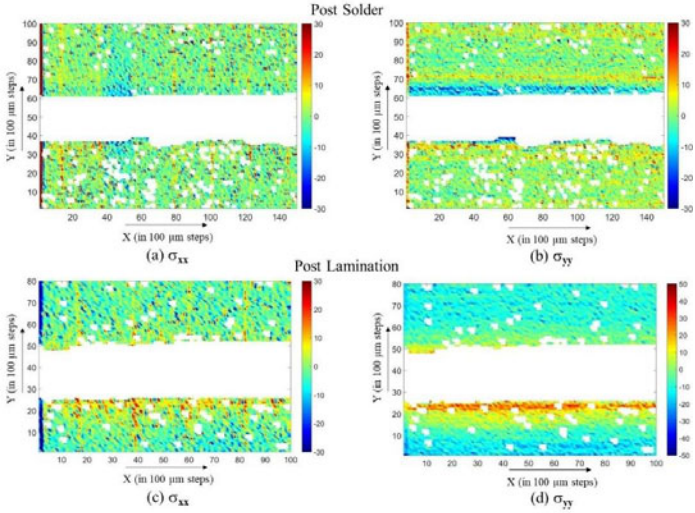

Figure 6: Residual stresses (MPa) in the generic design silicon cell from µSXRD, (a) Post-solder residual stress in the X-direction, (b) Post-solder residual stress in the Y-direction, (c) Post-lamination residual stress in the X-direction, (d) Post-lamination residual stress in the Y-direction. Note: Positive stress is tensile and negative stress is compressive, white regions inside the maps indicate interconnect/thick solder layer, which the X-ray beam could not penetrate

Interestingly, a band of compressive stress (~ -20 MPa) is seen above the Cu ribbon (white region) in the Y-direction stress map (Figure 6(b)). It could be due to a slight misalignment of the front and back ribbons during the soldering process. The rest of the regions in the post soldered stress maps show negligible small stress, randomly varying from +10 MPa (tensile) to -10 MPa (compressive), which is due to the effect of porous aluminium back surface layer (Al-BSF) on the silicon cell. This effect of the Al-BSF is seen in all the subsequent stress maps also.

Figures 6(c) and 6(d) show the residual stress maps of the scanned region 1 (refer Figure 1(b)), corresponding to the scanned region in the encapsulated cells. Not much change is

noticed in the X-direction stress, but the Y-direction stress increased to ~ 50 MPa which is concentrated along the edge of the Cu ribbon as shown in Figure 6(d). This is because, the cell bends over the front ribbon under the action of vacuum pressure, during the lamination process [37, 38]. Subsequently, due to the melting of the encapsulant, the bending of the cell reduces, and the overall appearance of the encapsulated cell remains flat. However, near the edges of the interconnect, the cell is still bent slightly, leading to tensile residual stress of ~ 50 MPa on the backside surface of the cell. This is a considerable increase in stress and could lead to cell cracks upon further loading during handling, transportation, installation, and operation.

Near the edges of the cells, either the front ribbon or the back ribbon is slightly shorter (refer Figure 1), leading to an asymmetric one-sided Cu-Si solder joint. In such a case, the CTE mismatch induces bending stress due to curvature induced by the differential contraction between Cu and Si [39]. This is because, at the interface of the Cu-Si joint, they are constrained to have the same strain. But, at the outward surfaces, they are free to contract (or expand) according to their own CTE value. This induces a bending moment across the joined region, leading to curvature of the joint. This curvature induces bending stress both in Si and Cu. In the case of Si, it leads to compressive stress at the joined surface and tensile stress on the opposite surface [39]. Figure 7 shows residual stress maps of the scan region 2 (Figure 1(b)) in the encapsulated cells. This region is near the edge of the cell, where the backside Cu ribbon is shorter compared to the front side Cu ribbon. As explained above, this asymmetry of the solder joint causes high residual stress and warpage of the cell after soldering. We did not perform a μSXRD scan of soldered cells in this region due to cracked samples.

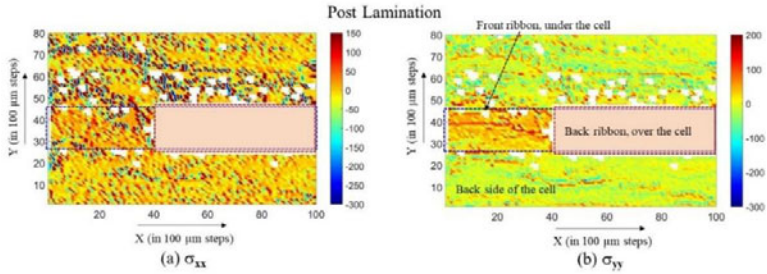

Figure 7: Residual stresses (MPa) in the generic design silicon cell from μSXRD, near edge of the cell (refer scan region 2 in Figure 1(b)), (a) Post-lamination residual stress in the X-direction, (b) Post-lamination residual stress in the Y-direction. Note: Positive stress is tensile and negative stress is compressive, region covered by the back ribbon has no result from μSXRD.

However, the post soldering condition can be simulated with reasonable accuracy using finite element analysis (FEA) [23, 24]. We performed a simulation of post-soldering cooldown to room temperature, RT (25 ^{o}C) using a 3D FEA sub-model of the cell covering the μSXRD scan region in Figure 7, using the modelling procedure and material properties from our recent earlier report [40]. Figure 8 shows the simulated post-soldering residual stresses in the region near the edge of the cell with an asymmetric solder joint. The stress contours are comparable with the post-lamination stress maps shown in Figure 7. The maximum stress after soldering near the edge of the cell is

around ~ 90 – 130 MPa, which increases to ~100 – 200 MPa due to flattening of the cell during the lamination process [23]. This experimental observation of high residual stress is in good agreement with the reported crack initiation observed in the encapsulated cells during mechanical testing and thermal cycling [10] and previously reported coupon level simulations [10, 41, 42].

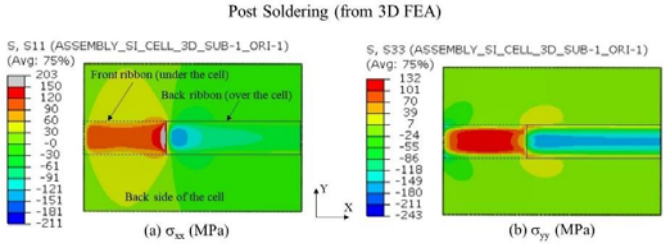

Figure 8: Residual stresses (MPa) in the generic design silicon cell from 3D FEA, near edge of the cell (corresponding to scan region 2 in Figure 1(b)), (a) Post-soldering residual stress in the X-direction, (b) Post-soldering residual stress in the Y-direction. Note: Positive stress is tensile and negative stress is compressive, the front and back Cu ribbons are not shown, only the region covered by them is marked for clarity

In a full-size module, the nominal residual stress in the cells (ignoring the interconnects) varies with the location of the cell and the size of the module [43]. However, the stresses shown in this manuscript are the localized stresses in the cell, around the soldered Cu ribbons. In this case, the residual stress is sensitive to the soldering temperature, lamination conditions, and Cu ribbon geometry, and less sensitive to the overall deformation of the PV module as shown in our previous studies [37, 38].

To date, these high stresses were not quantitatively characterized in the generic design cells by experimentation. Such high stresses significantly affect the fracture of c-Si cells during operation and could lead to premature failures of PV modules. In the case of thin silicon cells, the stresses at these locations could further aggravate and could lead to cell fractures even during soldering and lamination.

3.2 Estimation of Damage Tolerance

These high residual stresses also tend to propagate the existing microcracks in the c-Si cells, leading to a reduction of damage tolerance. We estimated the maximum tolerable microcrack length to sustain the lamination process, using the experimentally observed stresses. Figure 9 shows the map of the mode-I stress intensity factor, K_I of a straight edge crack in a silicon cell for different crack lengths and stress magnitudes. The stress intensity factor is calculated for the given stress and crack length using 2D finite element simulations, as explained in the Appendix-A. The fracture toughness (K_{IC}) values of monocrystalline silicon range from 0.62 MPa.m$^{1/2}$ to 1.29 MPa.m$^{1/2}$ [44 - 46]. Figure 7 shows that the residual stress in the cell varies from 100 to 200 MPa. But the maximum value of 200 MPa is highly localized. Hence, we considered the average value of 150

MPa for calculation of the upper limit of tolerable crack length. Using these values, the maximum tolerable crack lengths to sustain the post-lamination residual stress is calculated to be between 4.5 µm to 11 µm, as highlighted in Figure 9. Note that this is an approximate analysis considering the worst-case condition, ignoring the complexities like the inclination of the crack to the wafer surface and anisotropy of fracture toughness in the sc-Si cells. A more accurate calculation, considering the initial and propagating angles of angled cracks is possible [47]. However, our estimates show that the stress intensity factors, and the tolerable crack lengths shown in Figure 9 are comparable with such advanced calculations.

As the silicon wafers and cells contain randomly distributed microcracks, their fracture strength is probabilistic and depends on the longest microcrack (across the wafer thickness) in them [11-14]. In such a scenario, the above-presented estimation of the tolerable crack sizes under the given stress levels is essential to evaluate the probability of wafer or cell fractures [13]. Especially, in the case of altered wafer slicing processes or wafer thickness which leads to deeper microcracks, the probability of fracture could be readily estimated with this methodology even before the actual manufacturing of the cells and modules. Further, this methodology could be extended to the through-thickness surface cracks in the encapsulated silicon cells in PV modules to evaluate the probability of cell breakage under different external loading conditions.

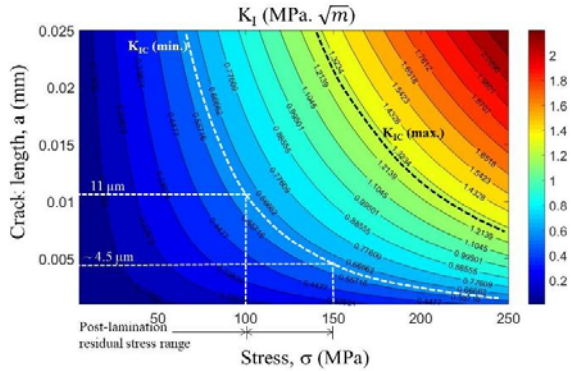

Figure 9: Variation of mode-I stress intensity factor with crack length "a" and stress "σ" for a c-Si cell with a straight edge crack with marking of the maximum tolerable crack length to sustain lamination process

In the case of a thinner c-Si cell, the damage tolerance will be much lesser due to the reduced thickness. Based on standard linear elastic fracture mechanics concepts, the mode-I stress intensity factor of an edge crack in a finite thickness wafer is a function of the crack length to thickness ratio (a/t) as shown in equation 9 [47]. Hence, the stress intensity of a thinner cell for a given crack length exceeds the fracture toughness of the material at lower stress levels.

$$K_I = f\left(\frac{a}{t}\right)\sigma\sqrt{\pi a} \tag{9}$$

3.3 Effect of Residual Stresses on the Fracture Strength of Cells

Figure 10 shows load-deflection plots of 4-point bend (4PB) testing of mini PV modules with soldered and unsoldered (pristine) generic design sc-Si cells. In all the four samples with soldered cells (Figure 10(a)), the cells fractured but at different loads between 862 N to 1472 N. Such variation of strength among the samples is common in c-Si cells due to the random size and distribution of microcracks in them [48]. In the case of samples with unsoldered cells (Figure10(b)), none of the cells broke, even at 2 kN (maximum test load). In these samples, the localized residual bending stresses due to soldering induced deformation and subsequent flattening of the cell are absent, as we used unsoldered cells. This test clearly indicates that the soldering and lamination induced localized residual stresses in the cells significantly reduce the cell fracture strength [49, 50]. This is because, the distribution of microcracks in the cells, resulting from the wafer cutting process [11 -13] and subsequent damage-etch treatments [14, 15] dictates the fracture strength of the cells. Later processes like handling, screen printing, firing, soldering, and lamination induce residual stresses but need not necessarily cause microcracks (< 1 mm long) [49].

However, we do agree that the residual stresses could go to higher magnitudes, in the case of the poorly controlled processes (e.g. overheating, excessive soldering time, ribbon misalignment, etc.) and may cause microcracks or even severe cracking of the cells, which is not the subject of the current manuscript.

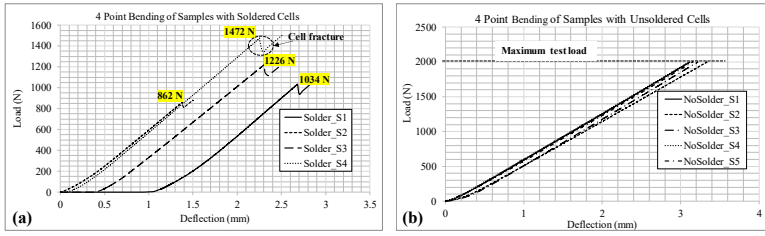

Figure 10: Load-deflection plots from 4-point point bending of mini PV modules with generic design mono c-Si cells, (a) Soldered, (b) Unsoldered.

The stresses induced during these processes could propagate the existing microcracks into macro size cracks (> 1 mm), which could then be visible under inspection techniques such as electroluminescence (EL). In the case of a well-controlled soldering process of standard generic design c-Si cells, the residual stress levels are ~ 100 MPa, which are not sufficient to form fresh microcracks. The remaining possibility is the existence of microcracks in the highly stressed regions in the soldered cells, leading to the propagation and thus reduction of the cell strength. In this case, the residual stress reduces as well due to the release of strain energy. However, in such a case, the crack should generally extend to millimeter size and should be visible in the EL imaging. The EL images of the samples with soldered cells did not show any cracks before 4PB

(Figure 11(a)). Therefore, the soldering and lamination process did not lead to the propagation of microcracks in these samples. Hence, the reduction of the fracture load of the soldered cells can be attributed to the residual stresses [49, 50]. To be precise, the fracture strength of the cell may be unaffected (assuming no microcrack propagation during the soldering and encapsulation processes). But the external load carrying capacity of the cell reduces significantly, due to these pre-existing bending (tensile) residual stresses. Thus, the soldered and encapsulated cell fractures at a much lower load (862 N to 1472 N) compared to the encapsulated pristine cell (> 2000 N), as shown by these 4PB test results. This result reinforces the importance and necessity of our experimental measurements and simulations of the residual stresses in the sc-Si cells.

The post-test EL images (Figure 11(b)) show fractured sc-Si cells with dendritic crack patterns, which are similar to those reported in the literature [1, 2]. The density of cracks is high at the edges of the middle Cu ribbon (within the loading span), indicating higher bending stress. The density of cracks is higher near ends of the middle ribbons in all the samples, indicating good agreement with the high residual stresses shown by experimental stress maps at these locations (refer Figure 7). Another interesting observation from these cracked cells is that the density of the cracks appears to be directly proportional to the fracture load. This may be due to the higher strain energy release at higher fracture loads [51, 52]. This observation could be useful to control fracture in the c-Si cells and needs to be studied further with more experiments.

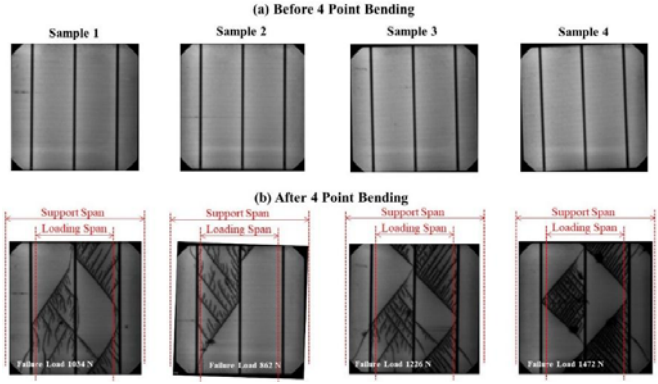

Figure 11: Electroluminescence images of the sample PV modules with soldered cells, (a) Before 4PB test, (b) After 4PB test.

In order to compare the magnitudes of the residual stresses in the sc-Si cell (Figures 6 and 7) with the mechanical stresses in the sc-Si cell during the 4PB tests of the sample PV modules (Figure 10(a)), we performed a simple 2D plane-strain FE simulation, ignoring the residual stresses. The variation of maximum stress in the sc-Si cell with the 4PB load is shown in Figure 12. The stress in the silicon cell is ~ 50 MPa at 1000 N load and it is ~ 170 MPa at 2000 N load. Note that these stresses do not include residual stresses. The fracture load of the cells in our tests ranged from 862 N to 1472 N, corresponding stress values range from 35 MPa to 110 MPa.

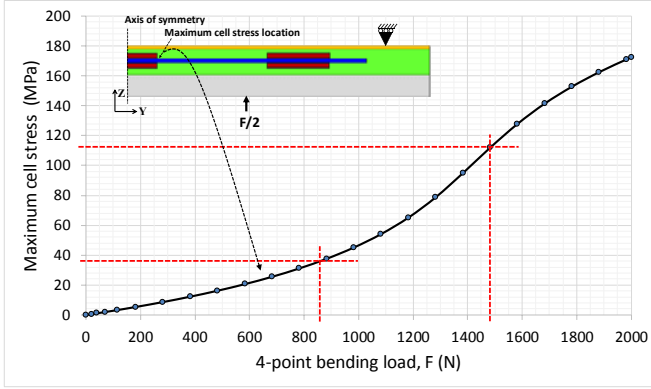

Figure 12: Variation of maximum stress in the silicon cell with the 4-point bending load (F) from a 2D plane strain FE simulation, ignoring residual stresses.

Clearly, the stress of 35 MPa is not sufficient to propagate the microcracks in the cells. Superposing the residual stress (~100 MPa), we get the actual stress range from ~135 MPa to 210 MPa, which is in good agreement with the reported fracture stress values by other groups [48, 50]. However, lower fracture stress values were reported in the case of bigger module coupons with multiple cells and full-size modules due to size effect [51]. Hence, it is clear that the residual stresses due to the soldering and lamination process are of considerable magnitude compared to the stress due to external loading [42]. However, the 4PB test needs to be correlated with a realistic loading case, such as snow load. A heavy snow load corresponds to 5.4 kPa pressure on the front glass of a full-size PV module, which leads to ~ 80 MPa tensile stress on the backside of cells at the corners of the modules (ignoring the residual stress) [51]. This corresponds to a 4PB load of 1.3 kN in our coupon level test as shown in Figure 12.

4. CONCLUSIONS:

Residual stresses in the generic design sc-Si cells are quantitatively characterized in this manuscript for the first time, using synchrotron X-ray microdiffraction experiments and subsequent curvature-based stress evaluation. The results show that the residual stress magnitude in the cell, near the edge of the Cu ribbons, increases during the lamination process. Further, the post-lamination stress maps near the edge of the cell shows high residual stress (~ 100 – 200 MPa). This is due to the CTE mismatch induced stress and warpage of the cell after soldering, as revealed by our 3D FE simulations. These residual stresses are very high and could lead to premature cell fractures and associated performance degradation in PV modules. In the case of thin silicon cells, these stresses could be fatal and could lead to cell fractures during module manufacturing. We estimated the tolerable crack length to sustain these high stresses using simple LEFM methodology, which shows that the tolerable crack length ranges between 4.5 μm to 11 μm, based on the minimum value of the fracture toughness of sc-Si. Our fracture testing results further reinforce that the soldering induced localized residual stress and

deformation leads to high residual stress in the cells after the lamination process and reduces the fracture strength (load-carrying capacity of the cells before fracture) of the cells. These results show the significance and necessity of accurate quantitative characterization of the residual stress in the encapsulated c-Si cells, which we presented for the first time in this manuscript.

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Appendix-A: 2D Finite Element Simulation of Straight Edge Cracks

A schematic of the 2D plane strain FE model used for simulation of c-Si wafer with a straight edge crack is shown in Figure A.1(a). The corresponding FE mesh with details at the crack tip is shown in Figure A.1(b). This model is meshed by quadrilateral elements with 8 nodes (CPE8R). Special elements with quarter point singularity were used at the crack tip to model the stress intensity accurately [53]. The silicon wafer was assumed to be isotropic in this simulation. The silicon wafer in a solar cell is oriented such that, the edges (along the X and Y directions) are parallel to the (100) and (010) crystal planes and the surface is normal to the (001) crystal plane. For such a case, the wafer is actually orthotropic and the equivalent elastic modulus and Poisson's ratio in X, Y and Z directions are 130 GPa and 0.28 respectively [54]. These values work as good approximations for the multi c-Si cells as well. Simulations of 4-point bending were performed for different crack lengths using this model, to evaluate the mode-I stress intensity factor (K_I) of the edge crack, under a pure bending load. Based on the theory of the linear elastic fracture mechanics (LEFM), the K_I of a straight edge crack of length 'a' can be calculated by the Equation A.1 [47].

$$K_I = Y\sigma\sqrt{\pi a} \tag{A.1}$$

Where, Y is the geometric factor of the crack geometry and σ is the applied bending stress. When K_I exceeds the fracture toughness (K_{IC}) of the material, crack propagation

occurs, leading to fractures in brittle materials [47]. The geometric factor Y is a function of the plate dimensions, crack length and loading.

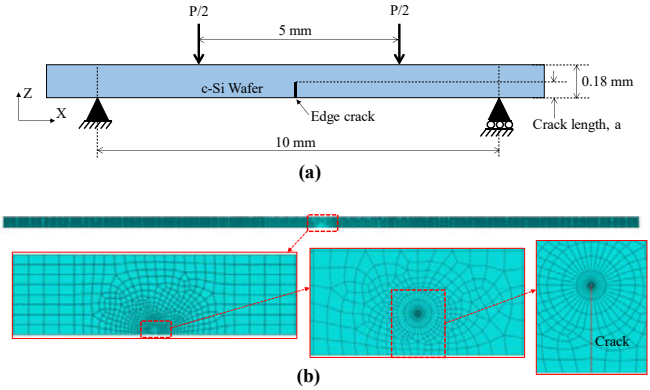

Figure A.1: 2D plane strain FE model of a c-Si wafer with an edge crack. (a) Schematic (not to scale) showing dimensions and loading setup (b) Full FE model with mesh details.

Figure A.2(a) shows the variation of the maximum principal stress field in the vicinity of the crack tip. We used the resulting variation of 'Y' with 'a' from the finite element simulations to fit an empirical formula for 'Y', as shown in the Figure A.2(b). The later was then used to calculate a map of K_I for any crack length, under the given bending stress, as shown in Figure 9 of the main manuscript.

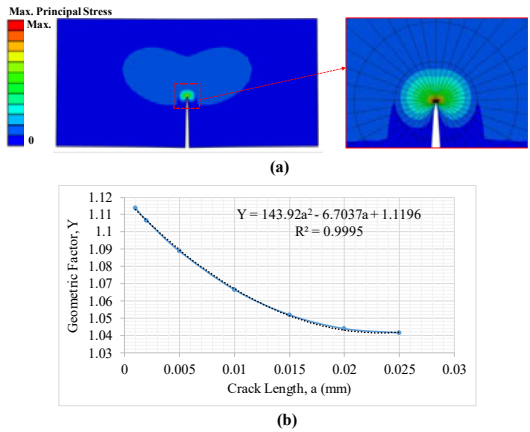

Figure A.2: (a) Simulated crack tip stress field. (b) Variation of geometric factor (Y) with crack length.

References:

1. S. Kajari-Schröder, I. Kunze, U. Eitner and M. Köntges, 37th IEEE PVSC, Seattle, WA, USA, 2011.
2. M. K¨ontges, S. Kajari-Schr¨oder, I. Kunze, and U. Jahn, 26th EUPVSEC, Hamburg, Germany, 2011.
3. M. Köntges, I. Kunze, S. Kajari-Schröder, X. Breitenmoser, B. Bjørneklett, Sol. Energy Mater. Sol. Cells, 95(4), 1131-1137 (2011).
4. M. Köntges, S. Kurtz, C. Packard, U. Jahn, K. A. Berger, K. Kato, T. Friesen, H. Liu, M. V. Iseghem, Review of Failures of PV Modules, Report: IEA-PVPS T13-01:2014, Photovoltaic Power Systems Program, International Energy Agency.
5. M. Abdelhamid, R. Singh and M. Omar, IEEE J. of Photovoltaics, 4(1), 514-524 (2014).
6. A. M. Gabor, M. Ralli, S. Montminy, L. Alegria, C. Bordonaro, J. Woods, L. Felton, 21st EUPVSEC, Dreseden, Germany, 2006.
7. I.J. Bennet et al., 22nd EUPVSEC, Milan, Italy, 2007.
8. J. Wendt, M. Träger, M. Mette, A. Pfennig, B. Jaeckel, 24th EUPVSEC, Hamburg, Germany, 2009.
9. S. Pingel, Y. Zemen, T. Geipel, J. Berghold, 24th EUPVSEC, Hamburg, Germany, 2009.
10. M. Sander, S. Dietrich, M. Pander, S. Schweizer, M. Ebert, L. Bagdahn, Proceedings of SPIE 8112, Reliability of Photovoltaic Cells, Modules, Components, and Systems IV, 811209, 2011.
11. A. Bohne,S. Schoenfelder, J. Bagdahn, 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, 1-5 September, 2008.
12. A. Grün, A. Lawerenz , R. Porytskyy, O. Anspach, 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, Sep. 5–6, 2011.
13. H. Wu, S. N. Melkote, S. Danyluk, Advanced Engineering Materials14, 342–348 (2012).
14. V.A. Popovich, A. Yunus, M. Janssen, I.M. Richardson, I.J. Bennett, 95 (1), 97-100 (2011).
15. Popovich V, Riemslag A, Janssen M, Bennett I, Richardson I., Int. J. Mater. Sci., 9-17 (2013)
16. X. F. Brun, S. N. Melkote, Sol. Energy Mater. Sol. Cells, 93, 1238–1247 (2009)
17. V. Ganapati, S. Schoenfelder, S. Castellanos, S. Oener, R. Koepge, A. Sampson, M. A. Marcus, B. Lai, H. Morhenn, G. Hahn, J. Bagdahn, T. Buonassisi, J. Appl. Phy., 108, 063528 (2010).
18. G. Sarau, M. Becker, G. Andrä, S. Christiansen, 23rd EUPVSEC, Valencia, Spain, 2008.
19. V. A. Popovich, N. M. van der Pers, M. Janssen, I. J. Bennett, I. M. Richardson, (2011), 37th IEEE PVSC, Seattle, WA, 2011.
20. A. J. Beinert, A. Büchler, P. Romer, V. Haueisen, L. C. Rendler, M. C. Schubert, M. Heinrich, J. Aktaa, U. Eitner, Sol. Energy Mater. Sol. Cells, 193, 351-360 (2019).
21. A.S. Budiman, G. Illya, V. Handara, W.A. Caldwell, C. Bonelli, M. Kunz, N. Tamura, D. Verstraeten, Sol. Energy Mater. Sol. Cells, 130, 303-308 (2014).
22. V.A. Handara, I. Radchenko, S.K. Tippabhotla, Karthic. R.Narayanan, G. Illya, M. Kunz, N. Tamura, A.S. Budiman, Sol. Energy Mater. Sol. Cells, 162, 30-40 (2017).
23. S. K. Tippabhotla, I. Radchenko, W. J. R. Song, G. Illya, V. Handara, M. Kunz, N. Tamura, A. A. O. Tay and A. S. Budiman, Prog. Photovolt: Res. Appl., 25, 791–809 (2017).
24. S. K. Tippabhotla, I. Radchenko, W. Song, N. Tamura, A. A. O. Tay and A. S. Budiman, IEEE 18th EPTC, Singapore, 734-737 (2016).
25. Tonio Buonassisi, Andrei A. Istratov, Matthew A. Marcus, Barry Lai, Zhonghou Cai, Steven M. Heald, Eicke R. Weber, Nature Materials, 4, 676–679 (2005).
26. M. I. Bertoni, D. P. Fenning, V. Rose, M. Holt, J. Maser and T. Buonassisi, 37th IEEE Photovoltaic Specialists Conference, Seattle, WA, 000154-000156 (2011).
27. V.A. Popovich, N. M. van der Pers, M. Janssen, I.J. Bennett, K.M.B. Jansen, J. Wright, I.M. Richardson, 38th IEEE Photovoltaic Specialists Conference, Austin, TX, 000442-000447 (2012).
28. Takayoshi Shimura, Takuya Matsumiya, Naoki Morimoto, Takuji Hosoi, Kentaro Kajiwara, Jun Chen, Takashi Sekiguchi, Heiji Watanabe, Materials Science Forum, 725, 153-156 (2012).
29. T A Lafford, J. Villanova, N. Plassat, S. Dubois and D. Camel, J. Phys.: Conf. Ser. 425 192019 (2013).
30. A. Colli, K. Attenkofer, B. Raghothamachar and M. Dudley, IEEE J. Photovolt., 6 (5), 1387-1389 (2016).
31. Stuckelberger, M., West, B., Nietzold, T., Lai, B., Maser, J., Rose, V., & Bertoni, M., J. Mat. Res., 32(10), 1825-1854 (2017).
32. X. Meng, M. Stuckelberger, P. Hacke and M. Bertoni, IEEE 44th Photovoltaic Specialist Conference, Washington, DC, 2854-2857(2017).
33. X. Meng, M. Stuckelberger, L. Ding, B. West, A. Jeffries and M. Bertoni, IEEE J. Photovolt., 8 (1), 189-195 (2018).

34. M. Kunz, N. Tamura, K. Chen, A. A. MacDowell, R. S. Celestre, M. M. Church, et al., Rev. Sci. Instr., 80(3), 035108 (2009).
35. N. Tamura, M. Kunz, K. Chen, R. S. Celestre, A. A. MacDowell, T. Warwick, Mater. Sci. Eng., A: Stru. Mater.: Prop., Microstr. and Proc., 524, 28–32 (2009).
36. N. Tamura, in Strain and Dislocation Gradients from Diffraction, edited by R. Barabash (World Scientific Publishing: Singapore, 2014) p. 125-155.
37. W. J. R. Song, S. K. Tippabhotla, A. A. O. Tay and A. S. Budiman, IEEE J. Photovolt., 8 (1), 210-217 (2018).
38. W.J.R. Song, S.K. Tippabhotla, A.A.O. Tay, A.S. Budiman, Sol. Energy Mat. Sol. Cells, 187, 241-248 (2018).
39. Ridhuan, S. W., Tippabhotla, S. K., Tay, A. A. and Budiman, A. S. Adv. Eng. Mater., (2019)
40. S. K. Tippabhotla, W.J.R. Song, A. A.O. Tay, A. S. Budiman, Sol. Energy, 182, 134-147 (2019).
41. Dietrich S, Pander M, Sander M, Schulze SH, Ebert M, Proc. SPIE 7773, 18 August 2010
42. Sascha Dietrich, Matthias Pander, Martin Sander, Ulli Zeller, Matthias Ebert, Proc. SPIE 8825, 882505, 24 Sep. 2013.
43. Eitner U., Kajari-Schröder S., Köntges M., Altenbach H., In: Altenbach H., Eremeyev V. (eds) Shell-like Structures. Advanced Structured Materials, 15, Springer, Berlin, Heidelberg, 2011.
44. F. Ebrahimi, L. Kalwani, Fracture anisotropy in silicon single crystal, Mater. Sci. Eng. A, 268, 116–126 (1999).
45. R. F. Cook, J. Mater. Sci., 41, 841–872 (2006).
46. A. Masolin, P. Bouchard, R. Martini, M. Bernacki, J. Mater. Sci., 48, 979–988 (2013).
47. T. L. Anderson, Fracture Mechanics: Fundamentals and Applications, 3rd Ed., Talyor & Francis Group, Florida, USA, 2005.
48. F. Kaule, W. Wang, S. Schoenfelder, Sol. Energy Mater. Sol. Cells, 120, 441-447 (2014).
49. E. Cereceda, J.R. Gutiérrez, J.C. Jimeno, J. Barredo, A. Fraile, E. Alarcón, S. Ostapenko, A. Martínez, M. A.Vázquez, 22nd European Photovoltaic Solar Energy Conference, Milan, Italy, 3-7 September 2007.
50. Felix Kaule, Matthias Pander, Marko Turek, Michael Grimm, Eckehard Hofmueller, Stephan Schoenfelder, SiliconPV-2018, AIP Conf. Proc. 1999, 020013-1–020013-9 (2018)
51. Martin Sander, Sascha Dietrich, Matthias Pander, Matthias Ebert, Jörg Bagdahn, Sol. Energy Mat. Sol. Cells, 111, 82-89 (2013).
52. Michael W. Rowell, Shandor G. Daroczi, Duncan W.J. Harwood, Andrew M. Gabor, 4th World Conference on Photovoltaic Energy Conversion (WCPEC-4), Hawaii USA, June 15, 2018.
53. Fracture Mechanics, ABAQUS Theory Manual, ABAQUS Documentation, Version 6.14, SIMULIA, Dassault Systèmes Simulia Corp., 2015.
54. M. A. Hopcroft, W. D. Nix and T. W. Kenny, J. Microelectromechanical Sys., 19 (2), 229-238 (2010).