UNIVERSITY OF CALIFORNIA SAN DIEGO

Higher-order VCO-based ADCs for Sensor Interfaces

A Dissertation submitted in partial satisfaction of the requirements

for the degree Doctor of Philosophy

in

Electrical Engineering (Medical Devices and Systems)

by

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The Dissertation of Corentin Pochet is approved and is acceptable in quality and form for publication on microfilm and electronically.

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EPIGRAPH

The clearest way into the Universe is through a forest wilderness.

– John Muir

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ACKNOWLEDGEMENTS

When I joined the University of California San Diego as a Master's student in 2016, I was excited and just as nervous about what lay ahead. I moved to the US for a Masters degree in Medical Devices and Systems with the goal of transitioning to a Ph.D. to research and explore ways devices could be miniaturized and open new opportunities in medical diagnostics and monitoring. Six years later, as this chapter of my life closes, I can confidently say that I could not have been prouder of what I accomplished at the University of California San Diego. I was able to carry out impactful research and explore the field of bioelectronics, and I also met wonderful friends and colleagues and made connections that I will cherish for the rest of my life.

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Chapter 4 is based on the material in C. Pochet and D. A. Hall, "A pseudo-virtual ground feedforwarding technique enabling linearization and higher-order noise shaping in VCO-based ΔΣ modulators," *2022 IEEE Journal of Solid- State Circuits Conference (JSCC)*. The dissertation author was the primary investigator and author of this paper.

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ABSTRACT OF THE DISSERTATION

Higher-order VCO-based ADCs for sensor interfaces

by

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Doctor of Philosophy in Electrical Engineering (Medical devices and systems)

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The rapid proliferation of Internet of Things (IoT) devices has revolutionized the technological landscape, permeating various domains and significantly impacting how we

interact with the digital and physical realms. As everyday objects become imbued with the capability to collect, manipulate, and acquire data autonomously. Smart distributed sensor networks are formed and are expected to allow transformative changes in sectors such as healthcare, industrial production, and agriculture by allowing continuous monitoring and data-supported decision-making, improving outcomes and efficiency.

The design of these highly advanced sensor nodes presents challenges as they must be extremely power efficient to allow for continuous long-term monitoring with a small battery or energy harvester to ensure unobtrusive form factors. A key component to reducing the power consumption and allowing large-scale deployment of IoT sensors is the use of on-device data processing, which reduces the data-transmission bandwidth, latency, and power consumption. This digital heavy preprocessing drives the system design towards selecting highly integrated system-on-chip (SoC) solutions that rely on the advanced process nodes for highly efficient operation of the digital core in charge of data processing at the sensor nodes. However, these advanced technologies do not scale as well for analog front-ends in charge of acquiring the sensor data as they do for digital signal processing with second-order effects significantly degrading key analog transistor parameters (gain, gate leakage, mismatches, etc.), making the design of high-performance analog circuits increasingly difficult. A lot of research has been dedicated to developing alternative architectures that are more resilient or even benefit from technology scaling. Among these architectures, voltage-controlled oscillator (VCO) based analog-to-digital converters (ADC) leverage digital-friendly ring oscillators to perform signal processing and quantization, providing highly scalable analog-to-digital interfaces.

These VCO-based ADCs have been mostly designed for high-speed applications with MHz of bandwidth but have started showing their potential for lower bandwidth sensor nodes

thanks to their supply insensitivity, infinite DC gain, and compact area. However, many challenges are associated with designing high dynamic range (DR) ADCs using VCO-based integrators as they have limited intrinsic linearity and require a large oversampling ratio due to being limited to 1st-order noise shaping.

This dissertation presents several innovations at the circuit and architecture level that can increase the noise-shaping order of VCO-based ADCs and achieve outstanding linearity. These techniques were integrated into two prototype chips: 1) an ADC for the direct-digitization of biopotential signals and 2) a purpose sensor front-end ADC for ultra-low-power IoT nodes.

The first prototype is intended to be used for wearable continuous health monitoring. It was designed to interface directly with high-impedance recording electrodes and provide a wide dynamic range and linearity to absorb motion artifacts and correct them in the digital domain. The prototype ADC achieves 2nd-order noise-shaping with high linearity and power efficiency using a novel Gated-inverted-ring-oscillator(GIIRO)-based time-to-digital converter and a multi-quantizer scheme. The ADC achieves a dynamic range greater than 90 dB and above 110 dB of linearity while consuming only 5.4 μW of power. This corresponds to a Schreier Figure of Merit (FoM) of 174.7 dB, which was state-of-the-art for VCO-based ADCs at the time of publication.

The second prototype was developed by building upon the feedforwarding techniques commonly used in the standard voltage domain ADC architectures and applying them to capacitively coupled VCO-based ADCs. Using the pseudo-virtual ground (PVG) at the input of the VCO integrator and feeding it further down the loop, we showed that high linearity and higher-order noise-shaping shaping could be achieved extremely power-efficiently. The prototype achieved 3rd-order noise-shaping with a 92.1 dB SNDR and a peak linearity of 123

dB while consuming only 4.4 μW. This led to a Schreier FoM of 179.6 dB, indicating how efficient the proposed structure is and showing comparable performance to standard voltage domain architectures.

CHAPTER 1: INTRODUCTION

1.1 Motivation: A scaling problem

The past decades have seen a tremendous increase in the use of electronic devices in our everyday lives. This increase has been largely fueled by the exponential shrinking of transistor feature size driven by Moore's law, allowing for more power-efficient and cost-efficient semiconductor production and enabling a range of new applications in industries such as healthcare, entertainment (virtual reality and augmented reality), and wearable/dispersible sensor nodes. The technology scaling that powers these advancements has been driven by reducing the feature size of transistors, thus increasing the density, yielding significant benefits in terms of cost, power efficiency, capabilities, and speed with each semiconductor generation. However, this reduction in feature size comes with its own set of challenges: 1) the supply has reduced from 3.3 V in the 330 nm process to less than 0.8 V in the latest sub-10 nm process, which has also caused a lowering of the supply voltage, lowering the headroom and thus the signal-to-noise ratio (SNR), 2) While the reduction in feature size has come with an increase in speed due to the reduction in intrinsic capacitance, it also has caused a reduction in intrinsic gain, a key parameter for analog design. 3) The reduction in minimum size also comes at the cost of higher variability, increased layout-dependent effects (LDE), and flicker (1/*f*) noise, which all affect the performance of analog blocks [1].

Despite these challenges, integrating analog and digital functions on the same die is beneficial economically and for system-level performance. In advanced system-on-chips, the boundary between the analog and digital worlds is starting to blur as digital cores rely on

distributed on-chip sensors for performance optimization, and analog block performance is enhanced through digital calibration and/or correction. Therefore, enhancing the performance of analog building blocks (amplifiers, ADCs, etc.) in highly advanced nodes remains a key challenge and need for future applications.

1.2 Time-domain signal processing

Time-domain signal processing has been proposed as an alternative to address some challenges associated with technology scaling. The key concept is to convert voltage-domain signals to equivalent time-domain signals represented by varying pulse widths or phase differences. This encoding method is independent of the signal amplitude and can, therefore, leverage the transistors' increased speed and smaller feature size while being supply-agnostic, thus benefiting greatly from transistor scaling. Chapter 2 will delve deeper into this architecture, focusing on a key element of time-based architectures, the voltage-controlled oscillator (VCO). These VCO blocks convert variation in voltage at its input to variation in frequency and have been used in several prototypes to perform key analog functions such as amplification, filtering, or quantization of the input signal. However, achieving performance on par with their voltage counterpart remains challenging and has been mostly demonstrated at very high-speed specs such as linearity and dynamic range, which are less of a concern. Whether this time-based architecture can compete with standard architectures in sub-100 kHz sensor applications with wide dynamic range and high linearity requirements remains to be seen.

1.3 High dynamic range time-based ADCs for sensor applications

The healthcare industry has been a driver for developing high-performance sensors. The past few decades have seen advancement in many biosensor applications, ranging from high-precision, high-density electrochemical sensors [2] to background noise-free magnetic biosensors

[3]. One of the main applications of interest is continuously monitoring biopotential signals, such as electrocardiograms, with wearable sensors [4]. These sensor nodes enable patients and healthcare professionals to access real-time, longitudinal health information for improved health monitoring and decision-making. Accurate wearable monitoring is challenging due to multiple factors: the wearable sensors must be small, low power, accurate and provide data even in the event of large variation such as sudden movements or a shock. These challenging specifications and the competitivity of the medical wearable sensor field make it an ideal case-study for the use of time-based ADCs for sensor applications and was chosen as the target for the prototypes presented in this thesis.

1.4 Dissertation organization

This thesis presents several techniques to achieve high precision and power efficient analog to digital conversion for sensing applications using time-domain signal processing. Chapter 2 describes the basics of time-domain processing and VCO-based ADCs. In Chapter 3, a 2^{nd}-order VCO-based ADC enabling direct digitization of ExG signals is presented with the measurement of a prototype fabricated in a 65 nm CMOS process. The focus of Chapter 4 is on the design of a 3^{rd}-order VCO-based ADC, which adapts the concept of feedforwarding that is popular in voltage domain architecture to time-domain architectures and shows that it can allow for very efficient digitization in a single loop. The theory of operation and the measurement results of a prototype fabricated in a 65 nm process are shown. Finally**,** Chapter 5 concludes the thesis with a summary of the work accomplished and discusses future research direction in the time-domain analog to digital conversion.

CHAPTER 2: TIME-BASED ANALOG-TO-DIGITAL CONVERTERS

2.1 Basic operation of VCO-based integrators

As mentioned in the introduction, VCO-based ADCs have been proposed as an alternative to standard voltage domain architecture, which suffers from the supply voltage and intrinsic gain reduction associated with advanced nodes. In this section, we will describe the operation of the VCO-based integrator, which is at the core of the time-based architectures presented later in this thesis.

As their name indicates, VCOs are a circuit architecture where the oscillation frequency, f_{VCO}, depends on an input voltage. The instantaneous frequency can be expressed as

$$f_{\mathrm{VCO}}(t) = K_{\mathrm{VCO}} v(t) \tag{2.1}$$

where K_{VCO} is the voltage-to-frequency gain in Hz/V and v(t) is the instantaneous input voltage. Equation (1) indicates that there is a proportional relationship between the oscillator frequency and the input voltage, but perhaps more interestingly, one can show that the relationship between the phase of the VCO and the input can be expressed as

$$\phi_{\mathrm{VCO}}(t) = \int_0^t 2\pi\, K_{\mathrm{VCO}} v(t) \tag{2.2}$$

where it is apparent that in the phase domain, the VCO can be used to perform the role of an integrator and thus provide high gain and enable analog signal processing. This integrator-like behavior is the key to using a VCO to replace analog-heavy amplifiers in many applications. In the past several decades, VCO-based integrators have leveraged this voltage-to-phase relationship to replace standard analog domain circuit blocks and perform functions such as amplification [5],

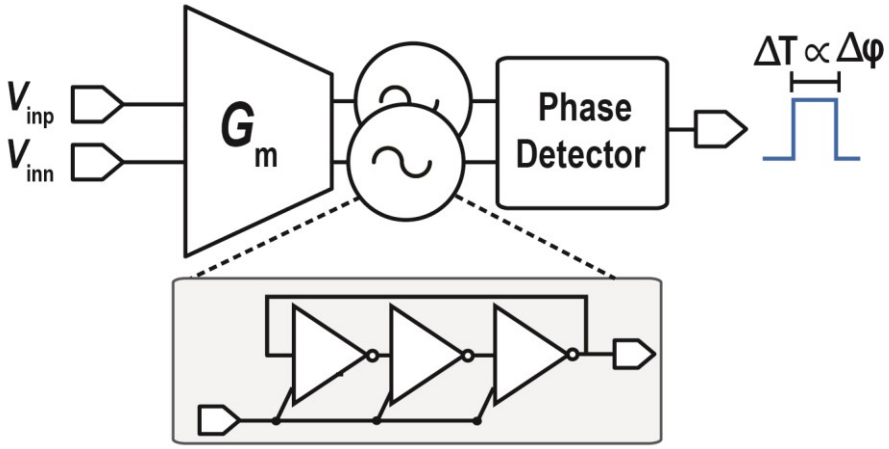

Figure 2.1. Circuit block diagram of a VCO-based integrator.

[6], voltage regulation [7], filtering [8], and analog-to-digital conversion [9]. The latter application is the focus of this chapter, where the phase integration properties of the VCO shown in equation (2.2) will be leveraged to replace the analog-heavy integrator in standard delta-sigma ADC architectures.

As shown in equation (2.2), the integrator gain is set by the open-loop parameter K_{VCO}, which will depend on the architecture and sizing of the oscillator; it is therefore important to be able to control this gain. A typical VCO-based integrator implementation is shown in Figure 2.1. The integrator is composed of a transconductor (G_m) that converts the input voltage to an output current, which is then used to drive two pseudo-differential current-controlled oscillators (CCO) composed of several inverter-like cells. The phase difference between the two oscillators, $\Delta\varphi$, can be extracted with a phase detector (PD), leading to a time-domain representation of the integrator's output value with longer pulses corresponding to a larger phase difference. One can easily show that for this architecture, the integrator gain, K_{int}, can be expressed as

$$K_{\text{int}} = G_{\text{m}} K_{\text{CCO}}\, G_{\text{PD}} \tag{2.3}$$

where G_m is the transconductance, K_{CCO} is the CCO gain in Hz/A, and G_{PD} is the phase detector gain, which will depend on the detector implementation. This equation is key to implementing the desired integrator gain and will be used in the design phase of the ADCs presented in this thesis.

2.2 Quantizer implementations

As discussed in the previous section, the VCO converts an input voltage to a frequency with a linear gain (Equation 2.1). Therefore, the quantizer of the VCO is often operated as a frequency-to-digital converter (FDC) to extract the input component in the digital domain. Two solutions have been popularized over the years with different complexity and properties, but they operate on the same principle: the phase difference of the VCO is sampled and differentiated to obtain the frequency and thus resolve the input signal. As explained later, this is also key to providing the noise-shaping property in a VCO-based ADC. The two main techniques to digitize the phase of the VCO are 1) an XOR-based FDC, where each node of the VCO is tapped, and 2) a counter connected to a single phase of the VCO. These techniques are illustrated in Figure 2.2, and the pros and cons are discussed next.

2.3 XOR-based FDC

The XOR-based FDC takes advantage of all the phases of the VCO. As shown in Figure 2.2(a), each node of the VCO is sampled and compared to the previous sample using an XOR gate. This enables the comparison of the phase between two samples and allows for the VCO frequency to be extracted. To avoid overflow, the designer must ensure that the VCO frequency, f_{vco}, is bounded by the sampling frequency fs such that $0.5f_s < f_{vco} < 1.5f_s$. If either of these bounds is exceeded, it will cause phase wrapping and an incorrect output. An advantage of the XOR-based FDC is that it can be shown to naturally provide Dynamic Weighted Averaging (DWA) [10] of the quantizer

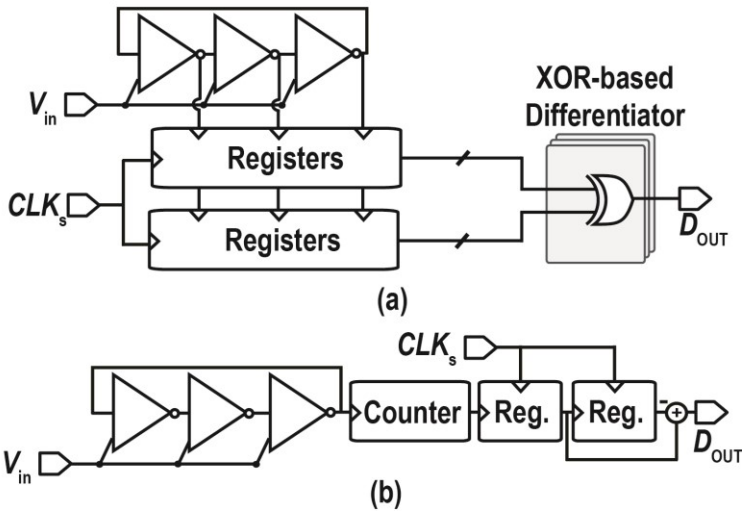

Figure 2.2. Schematics of an (a) XOR-based FDC and (b) Counter-based FDC.

output such that any mismatch between the inverter stages is shaped and that if the output is used to drive a feedback DAC, it also shapes the DAC mismatch. The XOR-based FDC is very compact and efficient; however, it is complicated to implement more than a 4-bit quantizer due to the thermometer encoding leading to a rapidly increasing number of wires complicating the layout.

2.4 Counter-based FDC

The counter-based FDC, illustrated in Figure 2.2(b), operates by counting the number of VCO edges in a sampling period. The sampling clock is typically much slower than f_{cco} to achieve high accuracy, so multiple edges are counted each period. The phase is differentiated using the difference between the counter's end value after two sampling instances, and the input signal can be extracted. The counter does not need to be reset, and 2's complement arithmetic can be used to calculate the result of the subtraction between the two results if the system is designed such that only one wrap-around can occur by limiting the maximum VCO frequency. This counter-based technique is popular for large quantizers (>4-bit) and an area-efficient architecture as it allows for a small VCO due to the relaxed requirements on f_{vco} and the need for high-frequency operation. It

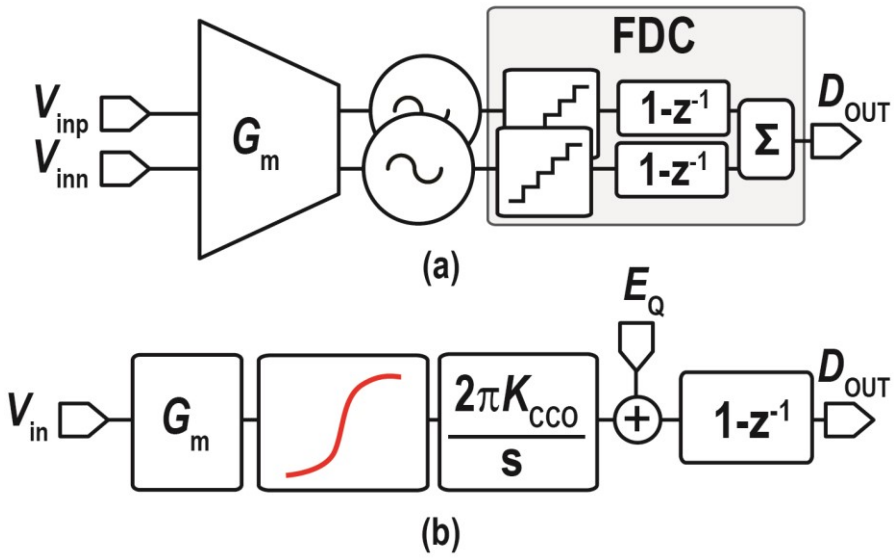

Figure 2.3. (a) Open-loop VCO-based ADC, (b) s-domain block diagram

should be noted that the counter is typically implemented with a gray counter to avoid causing a large quantization error when the sampling edge is triggered close to the asynchronous VCO edge and, thus, during a counter transition. One drawback of the counter-based technique is that the quantizer output must go through a separate mismatch-shaping algorithm to guarantee high linearity if it is to be used in a closed-loop design with a multi-bit feedback DAC.

2.5 Properties of VCO-based ADCs

This section will go over several key properties of VCO-based ADCs. To this end, the simplest implementation of a VCO-based ADC will be studied. This implementation comprises an open-loop VCO-based integrator and a quantizer, as shown in Figure 2.3(a), with an s-domain model of the ADC in Figure 2.3(b). Using this simplified model, we will explain the properties and challenges inherent in using VCO-based ADCs before looking into the literature on previous works and how these challenges were met.

2.5.1 1st-order noise shaping and anti-aliasing

Analyzing the block diagram in Fig 1.3(b), the block diagram behavior is expressed as

$$D_{\text{out}}[n] = \int_{(n-1)T_s}^{nT_s} K_{\text{vco}} v(t)dt + (E_Q[n] - E_Q[n-1]) \tag{2.4}$$

where D_{out} is the digital representation of the input signal, and E_Q is the quantization error. The second term highlights that the differentiation at the output effectively high-pass filters the quantization error, thus providing 1st-order noise shaping to the system. The first term, on the other hand, can also be expanded and shown to be equivalent to passing the input signal v(t) through a sinc filter with a frequency response, H_F, of

$$H_F(f) = \frac{K_{\text{VCO}} e^{-j\pi T_s f} \sin(\pi T_s f)}{\pi f} \tag{2.5}$$

At low frequencies, the filter response is ~1; thus, the output approximates the input voltage. It also shows that, like a standard voltage domain architecture, the VCO-based ADC provides anti-aliasing by filtering the input signal at high frequencies and has nulls around multiples of the sampling frequency, f_s. Another advantage of using VCO as integrators is that the dc gain is infinite, which is a key factor in avoiding issues such as dead-bands and SQNR degradation in CT-DSM architectures due to the limited dc gain of the opamps in the *RC* integrators [11].

2.5.2 Linearity

A key challenge in VCO-based ADCs is the non-linearity of the voltage-to-frequency gain. This non-linearity has two key origins: the non-linear transconductor (V → I) and the non-linear response of the current-controlled oscillator (I → F). While the even-order harmonics can be canceled by a pseudo-differential implementation, as shown in Figure 2.3, the odd-order harmonics typically limit the harmonic distortion to less than 50 dB in open-loop [12]. This limited linearity has been one of the main challenges in the design of high SNDR VCO-based

ADCs, and, as such, many techniques have been explored to enhance the voltage-to-frequency conversion linearity using techniques such as calibration [13] and feedback [10].

2.5.3 Metastability

Metastability is a major concern when implementing multi-bit quantizers, especially with low supply voltages. A quantizer with a large number of bits, N, reduces the quantization step, V_{DD}/N, which is challenging when decreasing the supply voltage as it increases the power and area of the comparator. However, the inner stages of the VCO-based integrators are mostly either at ground or V_{DD}, except for the state that is currently transitioning. This significantly reduces the likelihood of a metastable state.

2.6 VCO-based sensor front-end: Review of the prior-art

While much of the research in VCO-based ADCs has been for high-speed applications with bandwidths >10MHz [13], [14], [15], [16], [17], VCO-based ADCs also offer significant advantages for sensor applications with kHz bandwidths [18]. This is exemplified by the growing number of sensor-focused, VCO-based ADCs reported in the literature [19], [20], [21], [22], [23]. However, designing high-precision VCO-based ADCs is challenging due to two main factors, namely: 1) The voltage-to-frequency operation relies on an intrinsically non-linear voltage-to-frequency conversion, limiting their linearity to <50dB in open-loop without linearity compensation techniques [13], 2) The typical VCO-based ADC has a very limited input range due to the open-loop operation.

Several techniques have been reported to address this linearity and input range limitation and are illustrated in Figure 2.4. In [19], Jiang *et al*. proposed using an open-loop VCO and linearizing it with digital non-linearity correction [Figure 2.4(a)]. While this non-linearity correction algorithm increases the SFDR to ~70 dB, the input amplitude is limited to 50 mV_{pp}. To

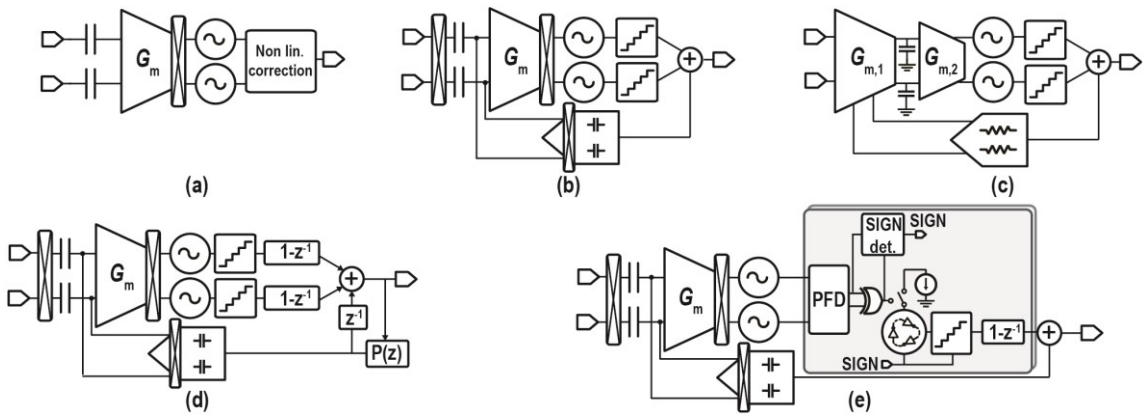

Figure 2.4. Direct digitization VCO-based sensor front-end architectures: (a) Open-loop with digital correction, (b) Closed-loop ac-coupled, (c) Hybrid dc-coupled, (d) DPCM-based, and (e) Proposed 2nd-order multi-phase quantizer.

further improve the system's linearity and increase the input range, a closed-loop architecture was reported in [20]. As shown in Figure 2.4(b), this design achieved 90 dB SFDR, but the input range was still only 100 $mV_{pp,}$ and the 1st-order noise shaping required a high oversampling ratio (OSR) and thus a high chopping frequency leading to a low input impedance (220 kΩ). In [22], a dc-coupled architecture combines a G_m-C integrator with a VCO-based quantizer, as shown in Figure 2.4(c). The dc-coupled architecture ensures a high input-impedance, but it comes at the cost of sensitivity to input common-mode and an analog-heavy first-stage. A differential pulse-code modulation (DPCM)-based predictor is used in [24] to maintain 1st-order quantization noise shaping while allowing for second-order shaping of the input, as shown in Figure 2.4(d). However, this requires a large 9-bit capacitive DAC (CDAC) with a large input cap, resulting in low input impedance. The ADC proposed in Chapter 3 is illustrated in Figure 2.4 (e).

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Chapter 2, in part, is a reprint of the material as it appears in Pochet, C. and Hall, D.A. (2023). VCO-Based ADCs for Direct Digitization of ExG Signals. In: Harpe, P., Baschirotto, A.,

Makinwa, K.A. (eds) Biomedical Electronics, Noise Shaping ADCs, and Frequency References. Springer, Cham. https://doi.org/10.1007/978-3-031-28912-5_2. The dissertation author was the primary investigator and author of this paper.

CHAPTER 3 : A SECOND ORDER VCO-BASED DIRECT-DIGITIZATION EXG FRONTEND

3.1 Introduction

With the rise of the Internet-of-things (IoT), there has been mounting interest in wearable devices for long-term, continuous health and wellness monitoring [4], [25], [26], [27], [28]. However, there are many challenges in acquiring high-fidelity, clinical-grade physiological data from a person outside a stationary, controlled environment like a hospital or clinic. For example, a wearable device must tolerate motion artifacts and power line interference (*e.g.*, 50/60Hz) while having ultra-low power consumption to ensure high-quality measurements over an extended period on a single charge.

Electrocardiography (ECG), electroencephalography (EEG), and electromyography (EMG) are examples of biopotential recording applications. The signals recorded from these are collectively called ExG signals [29], [30]. When recorded using non-invasive electrodes, ExG signals have amplitudes between a few μVs and 10s of mV over a 1 kHz bandwidth (BW), thus requiring an input-referred noise <5 μV_{rms}. The electrodes also introduce up to 100 mV dc offset. The electrode impedance depends on the electrode material, area, and presence/absence of a conductive gel. Several studies have characterized the impedance of different electrodes and shown that the resistance per area in the sub-kHz, ranges from ~1 to 100 $k\Omega/cm^2$ [31], [32]. This results in electrodes with an impedance between 10 kΩ and 5 MΩ, requiring a front-end with high input impedance to not attenuate the signal. More challenging, motion artifacts can induce large in-band signals (common- and differential-mode), requiring >200 mV input range [33]. Thus, an

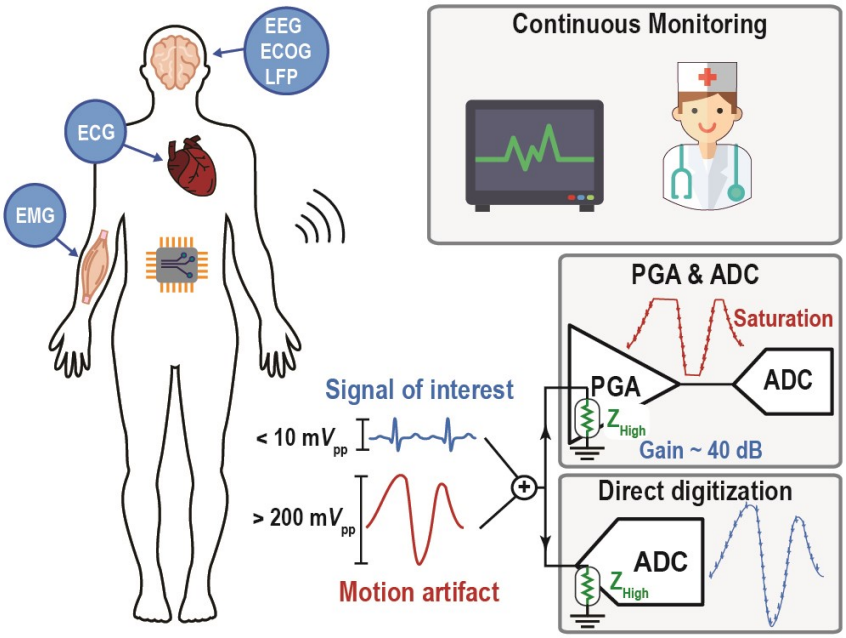

Figure 3.1. ExG signal acquisition systems.

ExG analog front-end (AFE) for wearable applications requires a dynamic range (DR) >90 dB to digitize the ExG signal in the presence of electrode offset and motion artifacts without saturation. Importantly, most motion artifact removal algorithms assume that the acquired signal is a linear combination of the artifact and ExG signal [34], [35], thus imposing a strict linearity requirement.

A conventional AFE for biopotential acquisition is illustrated in Figure 3.1. It is composed of a high-gain programmable gain amplifier (PGA) that amplifies and filters the ExG signal before digitization while also providing high input-impedance (>10 MΩ). This structure works well for stationary recording, but motion artifacts can cause saturation and/or distortion due to the PGA's limited DR and linearity. As such, there has been increasing effort toward removing the PGA and directly digitizing the signal [19], [20], [21], [24], [25], [36], [37], [38], [39], as shown in Figure 3.1.

Continuous-time (CT) delta-sigma modulators (DSM) are one candidate to replace the classic PGA and ADC front-end as they have intrinsic antialiasing, can achieve high DR, and can

be designed to have high input-impedance [19], [20], [25], [40]. Several designs have achieved the necessary DR for wearable applications [25], [37], [38]; however, they typically do not have sufficient linearity, complicating downstream signal processing and analysis. Conventionally, CT-DSMs are designed using amplifiers and comparators processing the signal in the voltage domain.

While this can achieve excellent performance [40], [41], designing these analog-heavy implementations is becoming complicated with technology scaling, which reduces the supply voltage and intrinsic gain [1]. A key element to achieving high DR and linearity with a DSM relies on multi-bit internal quantizers, which require a mismatch shaping technique to remove mismatch-induced non-linearities in the feedback path, adding delay and power. Due to these drawbacks, there has been growing interest in using time-domain CT-DSMs with phase-domain integration using voltage-controlled oscillators (VCO). By processing the signal in the time-/phase-domain, VCO-based ADCs do not suffer as much from the supply voltage reduction and benefit from the shorter transition times associated with advanced process nodes. Furthermore, in some implementations, the circular nature of the ring oscillator can be leveraged to provide intrinsic data-weighted averaging (DWA) [9, 13].

This chapter reports an ExG front-end that achieves both high DR (>90 dB) and SFDR (>110 dB) in a 1 kHz BW with a 400 mV_{pp} input range. This is accomplished using a single-loop, 2^{nd}-order VCO-based ADC that incorporates a novel multi-phase, multi-quantizer noise-shaped time-to-digital converter (TDC) to achieve high DR and SNDR in a power-efficient fashion. Auxiliary input-impedance boosters provide a high input impedance [33]. The time-domain operation also allows for dynamic power scaling through the amplitude-dependent duty cycling of the ADC's second integrator and quantizer, leading to ~35% savings in the absence of artifacts.

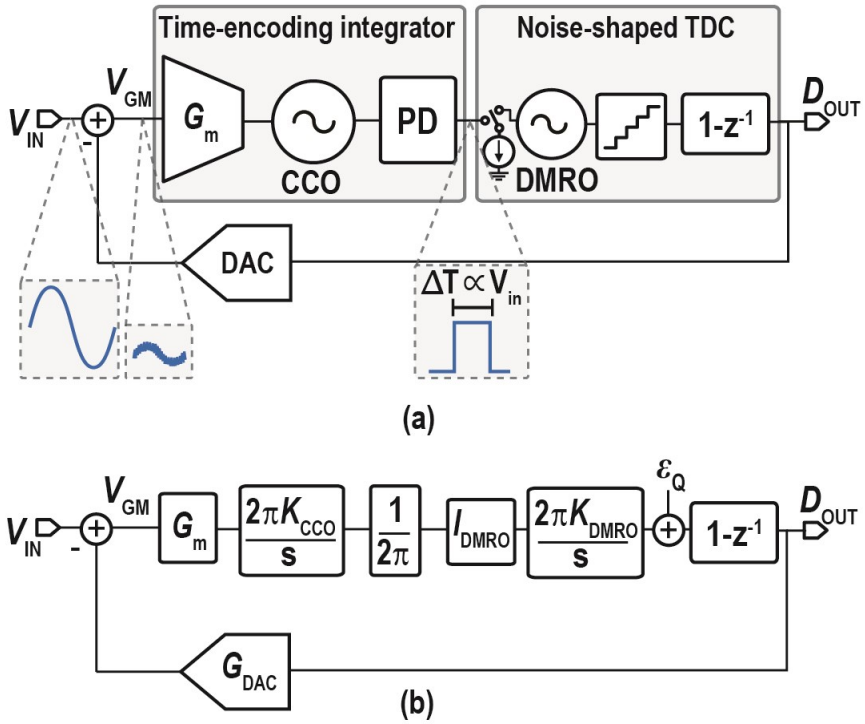

Figure 3.2. (a) Simplified single-ended ADC diagram and node waveforms (b) ADC's block diagram.

3.2 Architecture

3.2.1 Basic Operation

We propose a single-loop, 2nd-order VCO-based ADC that leverages a novel multi-phase, multi-quantizer noise-shaped TDC second stage to achieve high DR and SNDR in a power-efficient fashion. The approach is combined with an auxiliary input-impedance booster for high input impedance. The proposed architecture is inspired by [42], a high-speed ADC with 2nd-order noise-shaping using only ring oscillator-based integrators. As illustrated in Figure 3.2 (a), the ADC is composed of a G_m stage and a current-controlled oscillator (CCO) followed by a phase detector (PD). The PD output is quantized by a dual-mode ring oscillator (DMRO) TDC and fed back to the input. The first G_m-CCO acts as an integrator in the phase domain, accumulating the difference between the input voltage and the DAC. The PD compares the phase between two differential

CCOs, resulting in a time encoding of the integration value. This time-based encoding has two notable benefits: 1) It enables a low supply voltage after the first stage since the information is in the pulse width, not the amplitude, and 2) The 2nd stage's linearity is guaranteed since a two-level signal drives it. The noise-shaped TDC quantizes the pulse width while providing an additional order of noise-shaping, resulting in 2nd-order noise-shaping for the system. Feedback through a multi-bit DAC ensures low input swing at the G_m-cell input, which helps ensure high linearity despite using a non-linear G_m-CCO integrator in the 1st stage.

3.2.2 Loop Dynamics

The equivalent block diagram of the ADC is shown in Figure 3.2(b). The loop has two integrators, so its stability must be evaluated. Since the loop contains CT integrators and a discrete-time (DT) differentiator, it must be converted to one domain for analysis using the techniques described in [11]. The equivalent DT model allows the signal transfer function (STF) and noise transfer function (NTF) to be computed as

$$STF(z) = \frac{2FT_s^2}{2 + (FG_{\mathrm{DAC}}T_s^2 - 2)z^{-1} + FG_{\mathrm{DAC}}z^{-2}} \tag{3.1}$$

$$NTF(z) = \frac{2(1 - z^{-2})}{2 + (FG_{\mathrm{DAC}}T_s^2 - 2)z^{-1} + FG_{\mathrm{DAC}}z^{-2}} \tag{3.2}$$

where $F = 2\pi G_m K_{CCO} I_{DMRO} K_{DMRO}$, G_m is the input stage's transconductance, K_{CCO} is the CCO's current-to-frequency gain, I_{DMRO} is the current pulse driving the DMRO, K_{DMRO} is the DMRO's current-to-frequency gain, G_{DAC} is the equivalent DAC gain, and T_s is the sampling period. The NTF confirms the system's 2nd-order noise-shaping behavior. The loop dynamics were further explored and characterized in [43], and the system was shown to be stable over a wide range of

coefficients and excess loop delay (ELD) up to an entire clock cycle. This can be explained by the fact that despite having two integrators in the loop, the differentiator effectively "cancels" the effect of an integrator, thus making the system equivalent to a 1st-order ΔΣ.

3.2.3 Implementation

The practical implementation of this architecture poses several challenges. First, this architecture relies on pseudo-differential encoding at the PD output, which makes it very sensitive to mismatch and limits the linearity (SFDR < 80 dB) in previous designs [42], [43], [44]. Second, prior art used a switched-ring oscillator (SRO) TDC, which offers excellent linearity [45] but increases the power consumption, making the system less efficient. This is evident when the 2nd integrator consumes as much (or more) power as the 1st integrator [42], [43], [44], which is far from ideal in a noise-limited design. Finally, the integrator's time-encoded output ensures intrinsic linearity from the second stage, but it generates large tones around the CCO frequency, f_{CCO}, like a pulse-width modulation (PWM) encoded signal. To avoid folding these PWM tones in-band and degrading the SQNR, f_{CCO} must be higher than the sampling frequency, f_s, and thus consumes higher power [43].

We tackle these implementation challenges through several innovations. The TDC quantizer is based on a novel gated-inverted-ring oscillator (GIRO) structure that significantly improves power efficiency, mismatch tolerance, and thus the SFDR. This is coupled with a multi-phase, multi-quantizer architecture that relaxes the power required by the first CCO and improves the power efficiency while maintaining high linearity. Finally, we use a counter-based quantizer [24] instead of a phase domain sense-amplifier DFF-based quantizer [20], allowing signal-dependent power savings in the absence of motion artifacts.

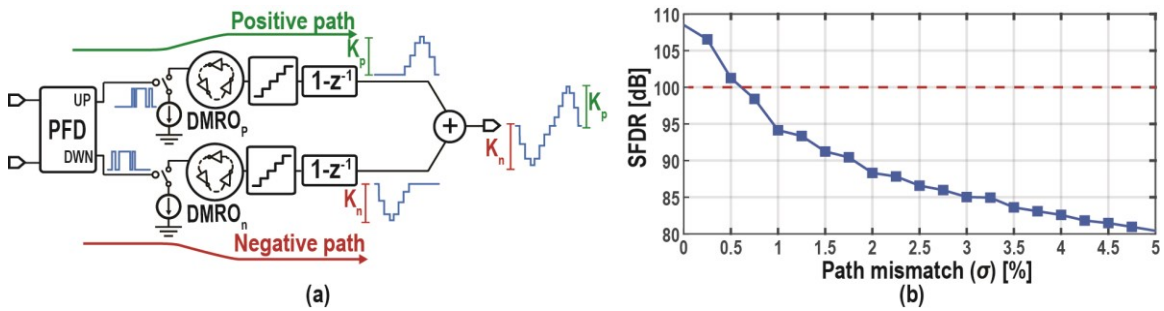

Figure 3.3. (a) Block diagram of mismatch induced non-linearity in a dual-path TDC. (b) Simulated SFDR as a function of path mismatch.

3.2.4 Mismatch resilient GIRO-bases quantizer

As illustrated in Figure 3.2(b), the TDC is modeled as a CT integrator followed by a digital differentiator, which is equivalent to having a block with $2\pi K_{DMRO}$ gain [45]. For correct operation, the pulse width must be proportional to the input amplitude. Therefore, the non-saturating range of the PD directly defines the ADC's input range, as an overflow would cause the loop to be unstable. Typically, the PD is implemented using a phase-frequency detector (PFD), which has a 2× larger non-saturating input range than an XOR-based PD [8]. Figure 3.3(a) shows the PFD-based TDC operation, where the positive or negative path is activated depending on the signal polarity. Despite the high loop gain, this pseudo-differential operation leads to significant SFDR degradation with path mismatch. Figure 3.4(b) shows the simulated linearity where the path mismatch was varied from 0 to 5%. To achieve >100 dB SFDR, the mismatch between the two paths must be <0.5% and degrades rapidly, reaching 80 dB with 5% mismatch due to even-order harmonic distortion. This SFDR degradation also exists in prior-art dual-path DMRO TDCs, where simulation results show >100 dB linearity while measurement results have an SFDR <80 dB [42], [43], [44].

There are two common implementations of a DMRO noise-shaped TDC, both based on a current-starved ring-oscillator: a gated-ring oscillator (GRO) [46] and an SRO [45]. While a GRO

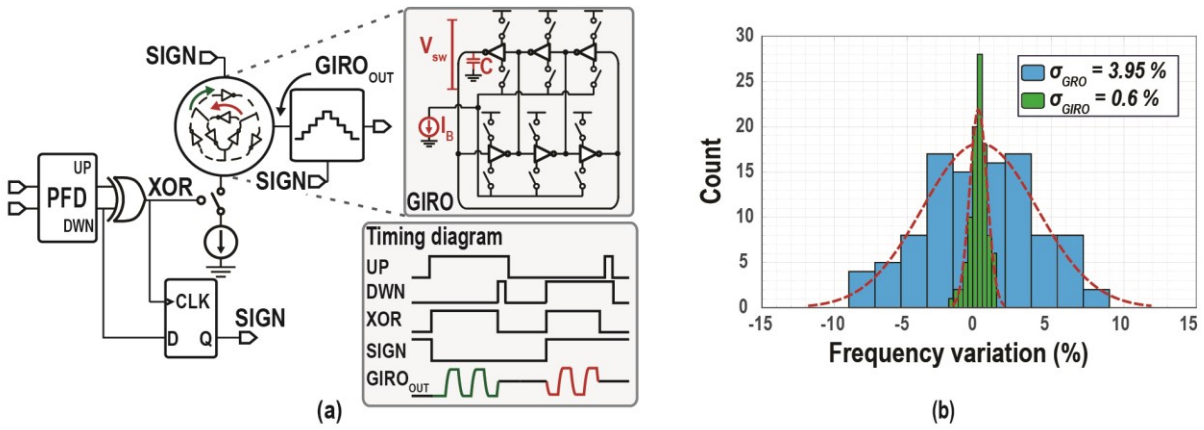

Figure 3.4. (a) GIRO and sign detection circuit with timing diagram, and (c) Monte Carlo simulation results comparing a GRO and GIRO.

has lower power and better noise performance due to the on/off behavior, the SRO reduces the timing skew and thus improves the linearity. The three major sources of frequency mismatch in a current-starved ring oscillator are: 1) The total node capacitance, C_{tot}, which is influenced by variation in sizing and the oxide capacitance; 2) The voltage swing, V_{sw}, due to threshold voltage variation; and 3) Bias current variation, I_B. To improve the path matching of a GRO, we propose the GIRO structure shown in Figure 3.4. The GIRO combines an inverted ring oscillator-based TDC [47] and a sign-detection circuit, similar to a digital PLL [48]. The sign detection is implemented with an XOR gate and a DFF. The XOR takes the "absolute value," outputting only the pulse width, and clocks the DFF, which samples the DWN path, thus extracting the "sign" information. This slightly differs from [48], where the other PFD output clocked the sign detection circuit. Clocking with the XOR gate ensures that the SIGN bit updates at the start of the XOR pulse instead of flipping between the start and end, as in the original implementation. With this sign detection circuit, the two TDC paths can be merged into a single path, and the polarity correction is pushed to the digital domain.

The noise-shaping is maintained using an inverted ring oscillator structure, which merges two ring oscillators such that the TDC oscillates in a clockwise or counter-clockwise direction, depending on the SIGN bit polarity. This allows the nodes to share the same capacitance and bias current, significantly improving the matching. The path merging also reduces the leakage by ensuring that the TDC only holds the charge during the short time between pulses instead of between polarity flips, as required in a dual-path GRO.

Figure 3.4(b) shows Monte Carlo simulation results (n = 100) of the frequency variation of a GRO and GIRO. For the GRO, the mismatch is zero-mean with a 4% variance, limiting the SFDR to ~82 dB, per Figure 3.4(b). The GIRO also has zero-mean mismatch, but the variation is reduced to 0.6%. For similar matching, the size of the dual-path DMRO would need to be increased by ~36× based on Pelgrom's Law, which would require significantly increasing the power consumption of the quantizer. Thus, the GIRO structure improves the matching by 6.5× over a GRO, enabling the system to achieve 100 dB much more efficiently than the two-path approach.

3.2.5 Multi-Quantizer TDC

The 1st integrator's output after the PFD is represented by a PWM-encoded signal at f_{CCO}. This PWM signal contains the result of the integration information at low-frequency and high-frequency tones around f_{CCO}. Despite being partially filtered by the second integrator, these high-frequency tones can fold back in-band and degrade the SQNR [43]. To reduce this effect, the CCO can be designed to oscillate at a frequency higher than f_s [43]; however, this has the significant drawback of increasing power consumption. The integrator gain, K_{int}, is

$$K_{\text{int}} = G_{\text{m}} K_{\text{CCO}} \propto \frac{G_{\text{m}}}{I_{\text{B}}} f_{\text{CCO}} \tag{3.3}$$

This shows that for a target K_{int}, a higher f_{CCO} reduces the G_m-cell's efficiency. Since the noise

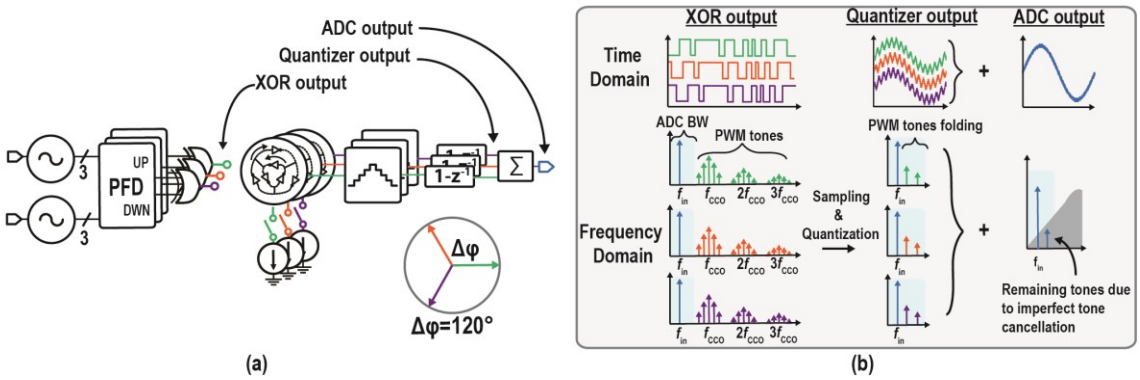

Figure 3.5. (a) Multi-quantizer based TDC ($N = 3$); (b) Time and frequency domain operation of the constructive and destructive summing.

target sets G_m, it is critical to minimize f_{CCO} to minimize the integrator's power.

In [42], a multi-phase approach was proposed to break this tradeoff, where f_{CCO} is virtually increased by tapping and combining multiple phases of the ring oscillator in the current domain. While this technique lowers f_{CCO}, it comes at the cost of losing the intrinsic linearity of the TDC-based quantizer. We propose using multiple noise-shaped TDCs in parallel, which maintains the intrinsic linearity of each channel and allows a lower f_{CCO}. This approach is illustrated in Figure 3.5(a) using three phases. Similar to [42], multiple out-of-phase components of the ring oscillator are tapped, but instead of being combined in an analog fashion using a current summer, each of the individual channel's SIGN bit is detected, and then the output of the XOR gate is fed to the GIRO-based TDC. The results are then summed digitally. We ensure that each channel only operates between two levels by pushing this summation to the digital domain, thus preserving the inherent linearity.

Figure 3.5(b) illustrates how the digital tone cancellation works. Each XOR output pulse contains the integration information and high-frequency tones quantized by a separate TDC. Each TDC output comprises input tones scaled by $1/N$, where N is the number of channels, and folded back tones. The phase and frequency of the input tone are matched across the channels, while the

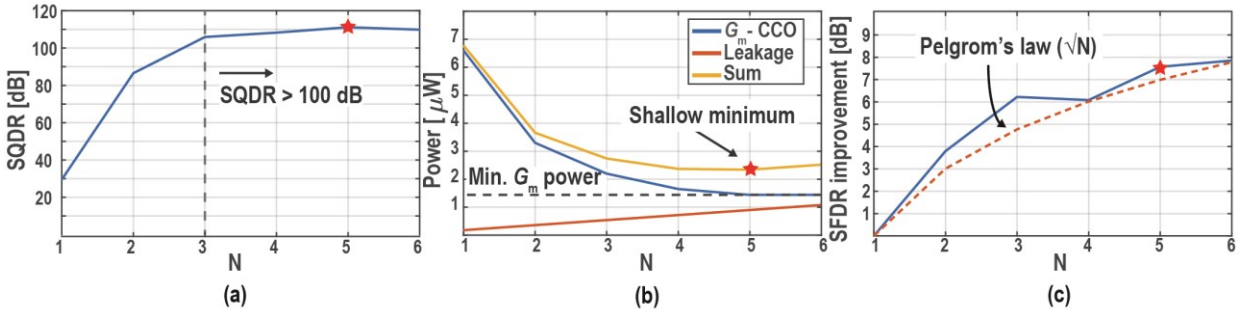

Figure 3.6. (a) SQDR vs N, (b) Power vs. N, and (c) SFDR improvement vs. N.

folded tones generated by the PWM encoding are both out-of-phase *and* at the same folded frequency. These conditions enable the signal tones to add constructively during digital summation while the folded tones add destructively. This leads to a high SQNR and is reasonably insensitive to phase and gain mismatch between the channels. Selecting N is a tradeoff between area, power, and target signal-to-quantization and distortion ratio (SQDR). As illustrated in Figure 3.6(a) and (b), as the number of phases increases, the SQDR increases while the power required by the G_m-CCO decreases. However, the digital cells' leakage power increases, leading to a shallow power optimum. Balancing these tradeoffs, $N = 5$ was selected for this design.

Another advantage of the multi-quantizer approach is that it improves the linearity due to averaging by reducing the distortion and the quantization noise, as observed in [49]. The multiple TDCs act as staggered quantizers, improving the SQNR and linearity. This was simulated and is shown in Figure 3.6(c), where the matching increases with N and follows the well-known Pelgrom's Law [50], [51], which trades-off area (the number of quantizers) for improved matching. For $N = 5$, this improves the SFDR by 7 dB. This multi-quantizer averaging also reduces the effect of inter-channel gain and phase mismatch. Simulations showed no SQNR degradation occurs for gain and phase mismatch <15%, which is easily achieved with appropriate sizing and layout.

3.3 Circuit Implementation

3.3.1 System Architecture

The ADC architecture is shown in Figure 3.7. A 200 kHz sampling frequency was selected for an OSR of 100 and a 1 kHz BW. The loop coefficients (G_m = 18 µS, K_{CCO} = 74 GHz/A, K_{DMRO} = 10 THz/V, and I_{DMRO} = 200 nA) were selected through extensive behavioral simulations using *Simulink* and *Spectre*, trading off the SQNR and the loop stability. A 7-bit DAC was selected for an SQNR >110 dB and to guarantee a small swing at the G_m-cell input. These parameters tolerate up to 2% delay from the digital logic and DEM without additional compensation.

The first integrator is chopped at $f_s/2$ (100 kHz) to reduce 1/*f* noise. This chopping frequency was picked to avoid quantization noise folding. The input capacitance is 900 fF, implemented with a metal-insulator-metal (MIM) capacitor. This capacitance forms a high pass filter (corner frequency < 10 Hz) with the pseudo-resistors that bias the G_m-cell. The 7-bit CDAC designed with custom 1.85 fF metal-oxide-metal (MOM) capacitors guarantees that the input swing is <15 mV_{pp}. The MOM capacitors were sized to achieve <0.2% matching, according to [52]. The total CDAC capacitance is 300 fF, so the input capacitive attenuation is 0.7. A switched capacitor resistor is formed by chopping before the input capacitance, significantly reducing the input-impedance (~5 MΩ). This impedance is too low to interface with small electrodes, which have impedances of several MΩ. An auxiliary amplifier precharges the input capacitance after the chopping clock, thus reducing the charge that needs to be supplied from the electrode and increasing the input impedance. The input-impedance booster was implemented similarly to [33] using buffer duty-cycling for power savings and capacitive charge sharing for fast charging. Two factors limit the maximum achievable input impedance: 1) The input impedance due to chopping the auxiliary buffer, which is needed to eliminate its offset and 1/*f* noise [33]; and 2) The duty-

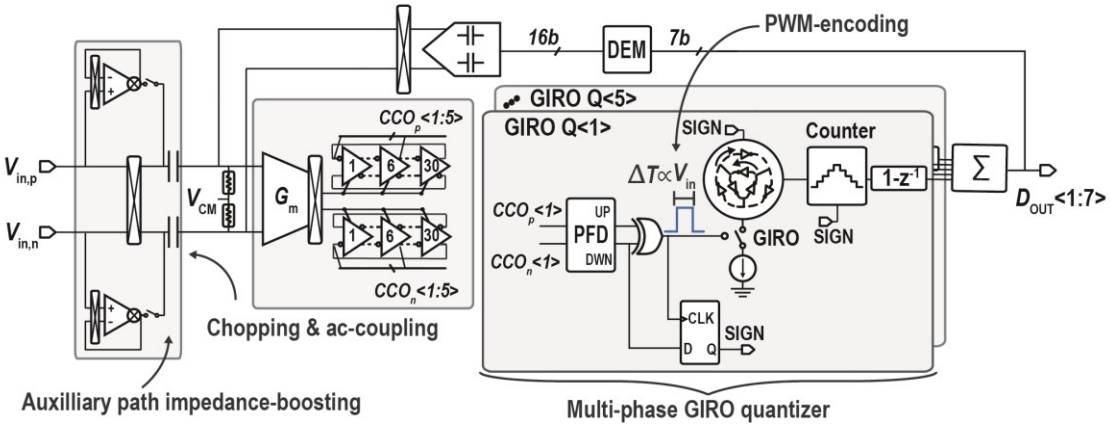

Figure 3.7. ADC architecture.

cycle needs to be <5% of T_s to maintain low power and avoid SNDR degradation, which leaves 250 ns to precharge the input capacitor. These factors limit the maximum input impedance with auxiliary input-impedance boosting to a few 10s of MΩ in a CT-DSM-based direct-digitization architecture [25].

3.3.2 G_m-CCO Integrator

The 1st integrator comprises a chopped G_m and two 30-stage ring oscillators. The chopping reduces the 1/*f* noise so that the system is thermal noise-limited. The G_m is a differential pair for direct current control of the CCO and to avoid the power overhead required for common-mode feedback and the non-linearity of a two-stage current-reuse topology [24]. It is source degenerated by a 12 kΩ tunable resistor (±10%) to linearize the G_m that tunes the loop parameters while maintaining a constant f_{CCO}. The input transistors are thick-gate oxide NMOS devices to reduce gate leakage and avoid common-mode drift from the pseudo-resistors. As shown in Figure 3.8, dead-band switches in front of the G_m are opened for 300 ns during chopping, and the differential switching artifacts are converted to a common-mode signal. The dead-band switch pulse width was chosen to absorb the digital propagation delay while minimally affecting the input-referred noise.

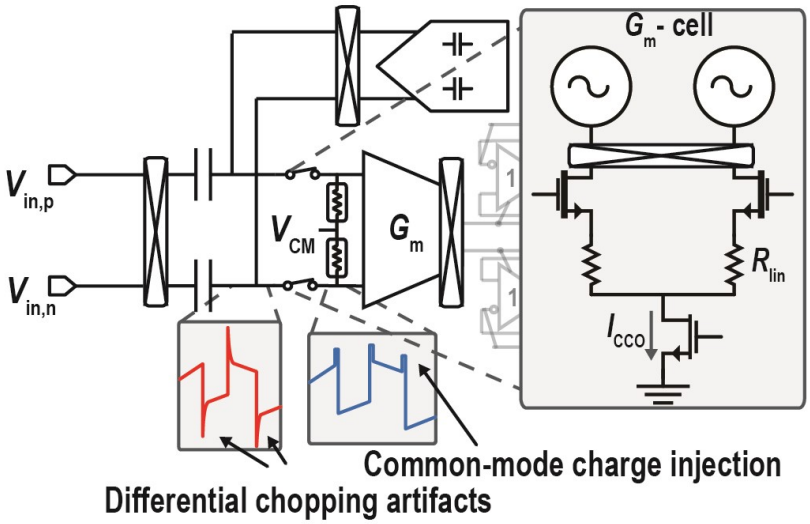

Figure 3.8. Schematic of the chopped G_m.

Each ring oscillator stage is a cross-coupled PMOS due to its superior noise performance [36]. The loop parameters determined the sizing, and 30 stages were chosen for flexibility as it could be easily reconfigured to work with $N = 6$ based on post-layout simulations. Every 6th node of the CCO is tapped, such that the five outputs are separated by 72°. As described earlier, this relaxes the requirement on f_{CCO} so that it can be reduced to 120 kHz.

3.3.3 GIRO Quantizer

Each TDC channel has a PFD, a sign detector, and a GIRO. The PFD is implemented using the well-known NAND structure. The UP and DOWN outputs are fed to the XOR gate and the DFF. The XOR is designed so that the propagation delay is long enough to allow the DFF to settle and avoid settling errors. While this could cause incorrect polarity extraction, this can only happen if the UP and DOWN pulses are extremely close to each other, which is a negligible error as it means the signal is extremely close to a polarity flip. An additional cross-coupled delay chain is added between the XOR and the GIRO input to generate differential signals and ensure a 2 ns

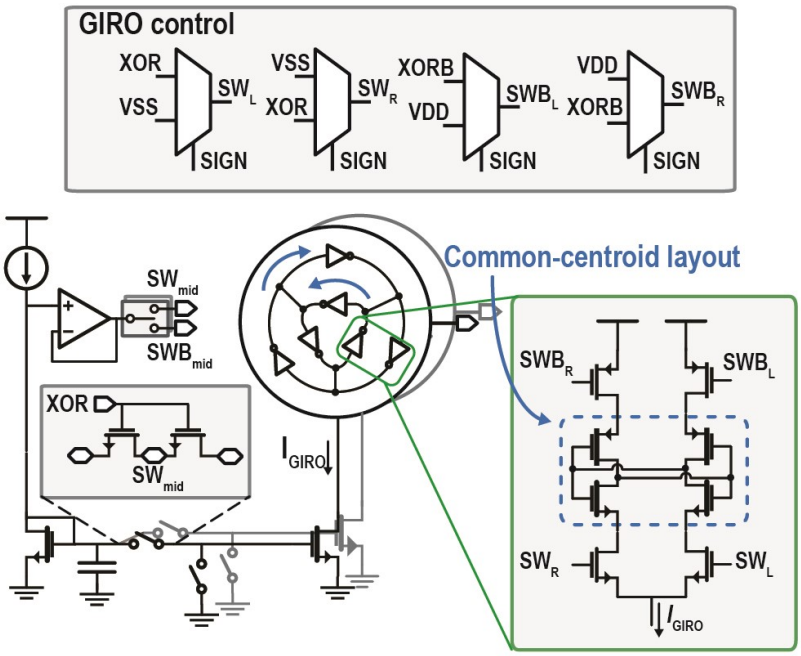

Figure 3.9. Schematic of the GIRO.

delay between the polarity flipping and the first GIRO edge. This delay allows the settling of the counters across process variation and corners. The delay chain output controls the GIRO behavior through digital muxes, as shown in Figure 3.9.

Each stage of the GIRO is implemented using single-ended, thick-oxide inverters to reduce leakage. They are laid out in a common-centroid fashion to improve the matching between the two paths. The inverter switches are minimum-sized transistors to reduce charge injection and leakage. The bias current generation is shared among all channels, and each independent current source is gate-switched. A large MIM capacitor enables quick charge sharing for rapid turn on/off and reduces skew. Due to the shared bias and the low current reference (200 nA), the large switches' leakage can modulate the current source's bias voltage, leading to non-linearity. A low-leakage switch structure was used to ensure this effect is limited and does not degrade the linearity [2], as illustrated in Figure 3.9. The buffer only consumes 100 nA and is shared by the 5 channels.

3.3.4 Digital Blocks

Each GIRO output is fed to a counter, triggered by the rising or falling edge, depending on whether the polarity bit is positive or negative. Since the counter's output is updated asynchronously with the sampling clock, this leads to potential sampling errors. Multiple bits could flip during a sampling instant for a binary counter, leading to a significant output error. Instead, the counter is implemented with a gray counter that guarantees only a 1-bit flip, limiting the sampling error. The output of each counter is passed through a gray-to-binary encoder and combined to obtain the final ADC output.

Given the multi-bit inner quantizer and feedback, mismatch shaping is needed. While DWA is a popular choice in high-precision ADCs due to its low SQNR degradation, segmented DEM is used since the number of wires required for DWA ($2^7 = 128$) would have severely complicated the CDAC layout. On the other hand, segmented-tree DEM only requires ($2^4 = 16$) wires, leading to a more straightforward layout and routing, and does not generate any tones at the cost of a higher noise floor. Simulink simulations confirmed that an SQNR >100 dB could be achieved with up to 1% DAC mismatch (5× our design target). All digital logic was written in Verilog and synthesized using a standard digital flow.

3.4 Measurement Results

The VCO-based ADC was fabricated in a 65 nm TSMC LP process and occupied an active area of 0.075 mm^2. An annotated die micrograph is shown in Figure 3.10. The 1st integrator, impedance-booster, and CDAC are powered from a 1.2 V supply, while the multi-phase TDC quantizer and the digital blocks containing the summer and DEM logic operate at 0.8 V.

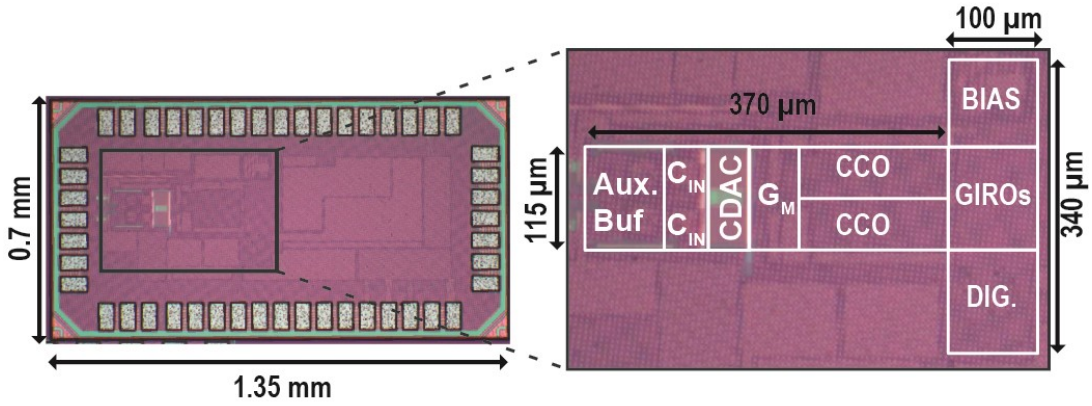

Figure 3.10. Die micrograph

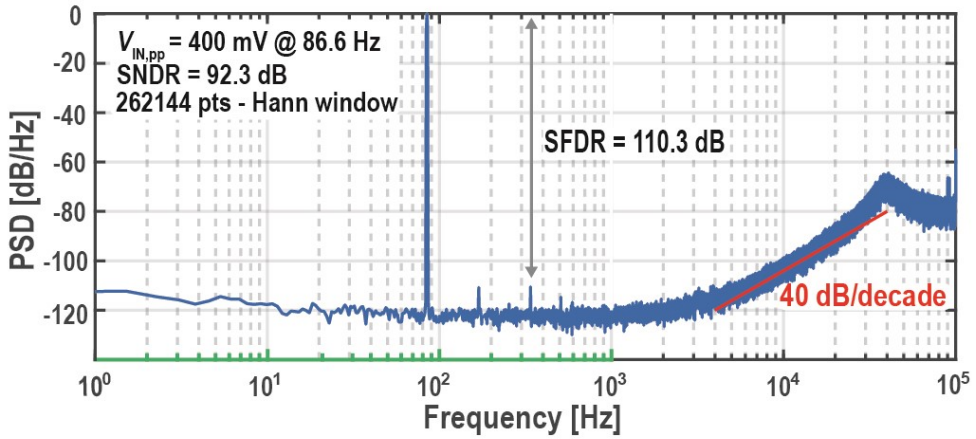

Figure 3.11. Measured ADC output spectrum.

3.4.1 Electrical Characterization

The ADC's SNDR, SFDR, and DR were characterized by an ultra-low distortion signal generator (APx555) that generated a full-scale, 400 mV_{pp} sinusoid. The measured output spectrum is shown in Figure 3.11. The ADC achieved an SNDR of 92.3 dB in 1 kHz BW and a 110.3 dB SFDR, limited by the 3rd harmonic. The 40 dB/decade noise-shaping expected from the 2nd-order NTF is evident. To assess the mismatch resilience, the SFDR of 5 devices was measured (Figure 3.12). The average SFDR is 107.9 dB and consistently above 104 dB. The SNDR as a function of

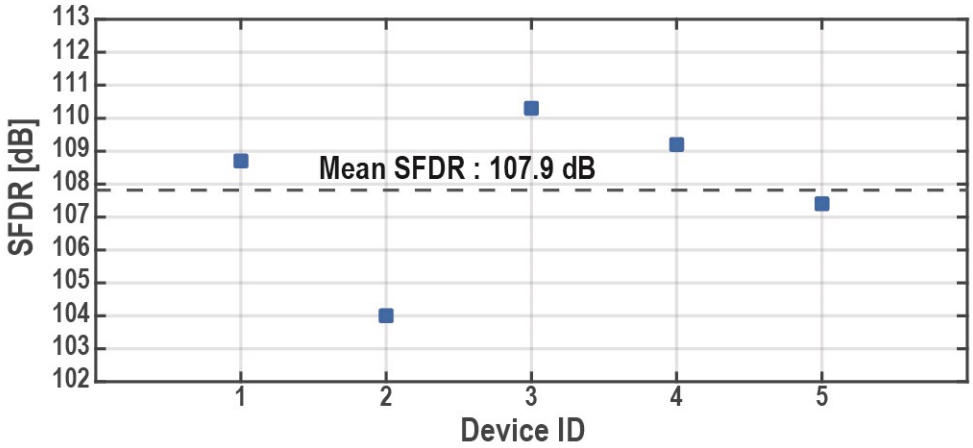

Figure 3.12. Measured ADC SFDR for 5 devices.

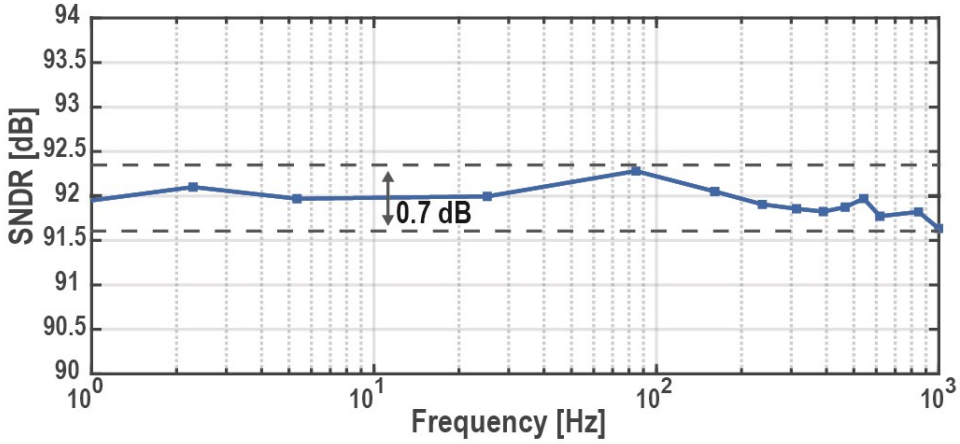

Figure 3.13. Measured ADC SNDR over its bandwidth.

frequency from 1 Hz to 1 kHz is shown in Figure 3.13. The SNDR varies by less than 0.7 dB across the entire frequency range due to chopping with ac-coupling at the input.

The ADC input-referred noise was measured with shorted inputs. The PSD is shown in Figure 3.14. The integrated noise from 1 Hz to 1 kHz is 3.5 $\mu V_{rms,}$ and the spot noise is 110 nV/√Hz. The 1/*f* noise in the spectrum is mainly due to the inverters in the 1st CCO, which are not chopped. However, this is less than 15% of the integrated noise.

Figure 3.15 shows the measured 92.3 dB DR and the power as a function of the amplitude. The pie charts show that the system power reduced from 5.8 to 4.25 µW (35%) when the input

amplitude was below 10 mV. As expected, the power of the GIRO and digital blocks is reduced significantly, and the power consumption is dominated by the input G_m-cell. This results from the input-dependent quantizer duty-cycling, enabling low power in the absence of motion artifacts.

The ADC was excited with two tones at 200 mV_{pp} to evaluate the impact of large motion artifacts on the linearity. Figure 3.16 shows the measured intermodulation distortion (IMD) was

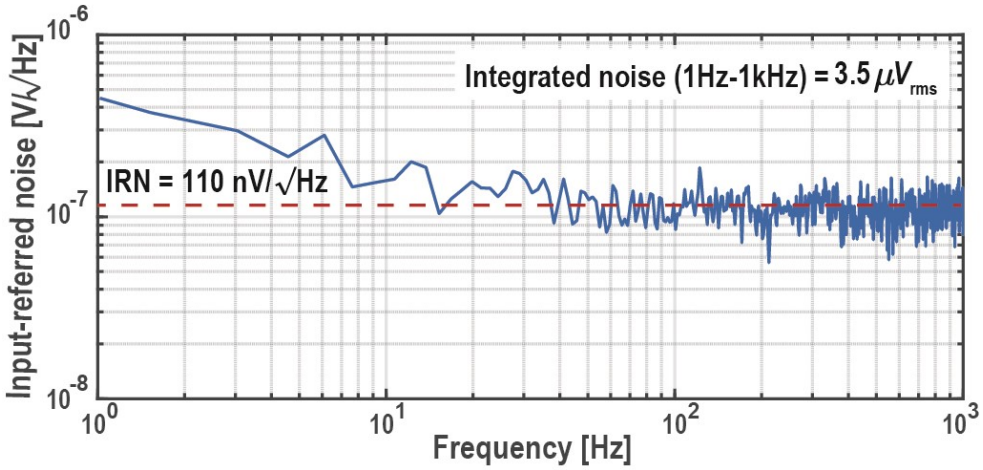

Figure 3.14. Measured ADC input-referred noise spectrum.

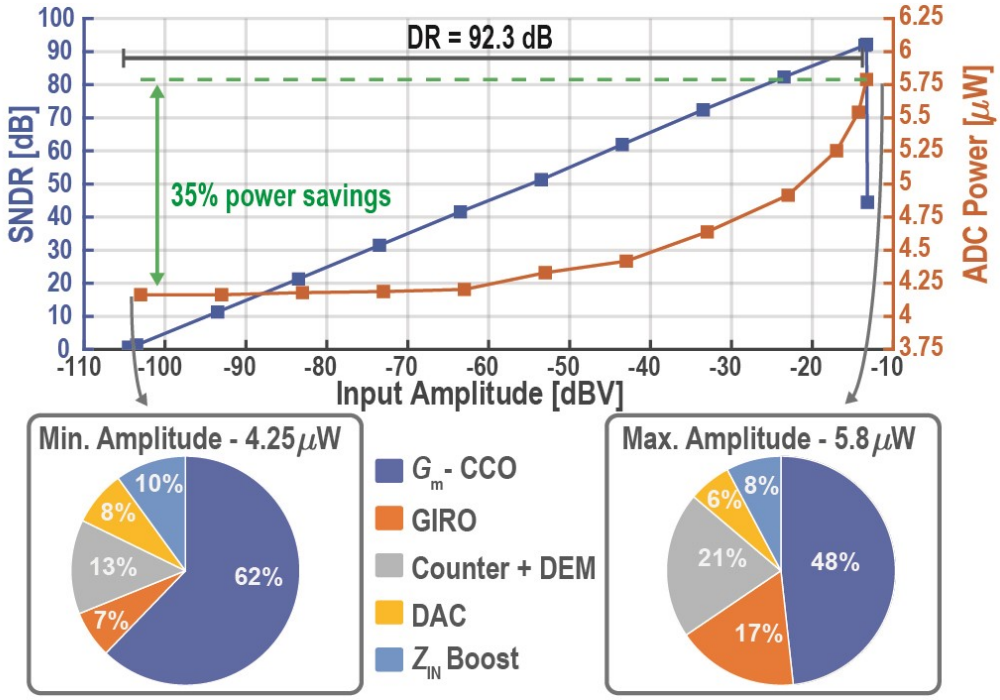

Figure 3.15. Measured SNDR and power vs. input amplitude.

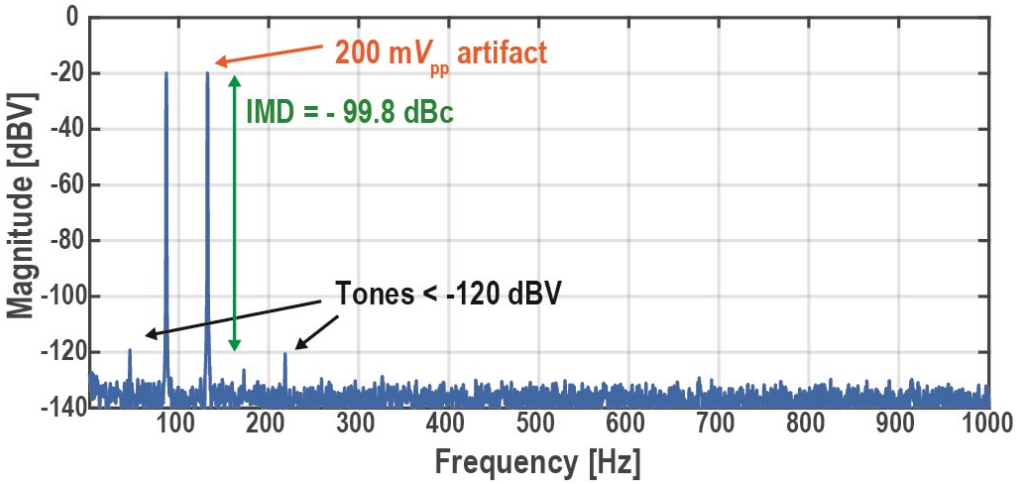

Figure 3.16. Measured intermodulation distortion (IMD).

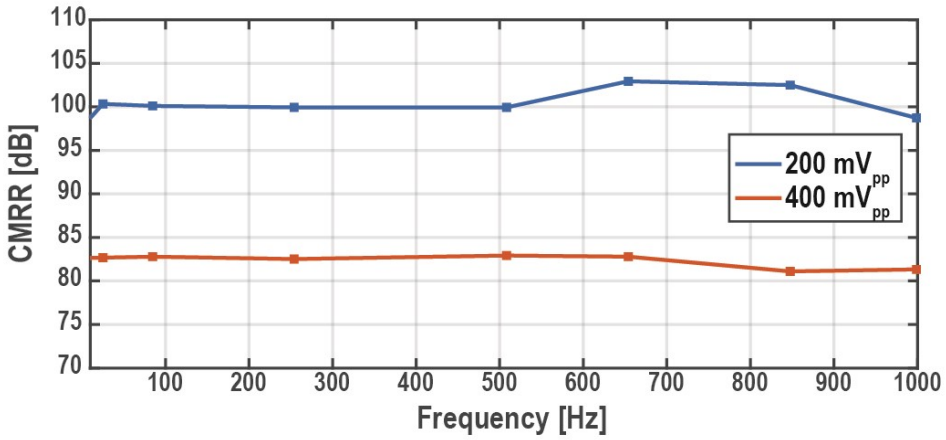

Figure 3.17. Measured common-mode rejection ratio (CMRR) with a 200 mVpp (orange) and a 400 mVpp (blue) common-mode input

99.8 dBc with the intermodulation products ~1 µV, which is below the 3.5 μV_{rms} integrated noise of the AFE. This demonstrates that even in the presence of significant motion artifacts/interference, the distortion would be below the noise floor, thus not introducing any unwanted signals.

As illustrated in Figure 3.17, the common-mode rejection ratio (CMRR) was measured across the bandwidth with a full-scale ADC input (200 mV_{pp} single-ended) and was above 95 dB over the entire frequency range. Since a larger common-mode artifact is expected in a wearable

device (up to 400 mV_{pp}), the ADC's CMRR was measured with this larger input to be 82 dB. Common-mode artifacts larger than 400 mV_{pp} cause the ADC's loop stability to degrade, leading to a loss in performance. It should be noted that the results are better than those reported in the original paper [53] due to an improvement in the testing setup. The insensitivity to large and rapid artifacts was tested by superimposing a 150 μV_{pp} sinusoid signal on a 300 mV_{pp} squarewave. As illustrated in Figure 3.18, the ADC quickly recovers from the artifact, allowing the small sinusoidal to be clearly observed. To measure the input impedance, Z_{in}, high precision 1 MΩ resistances were placed in series with the ADC inputs, and an instrumentation amplifier amplified the voltage across

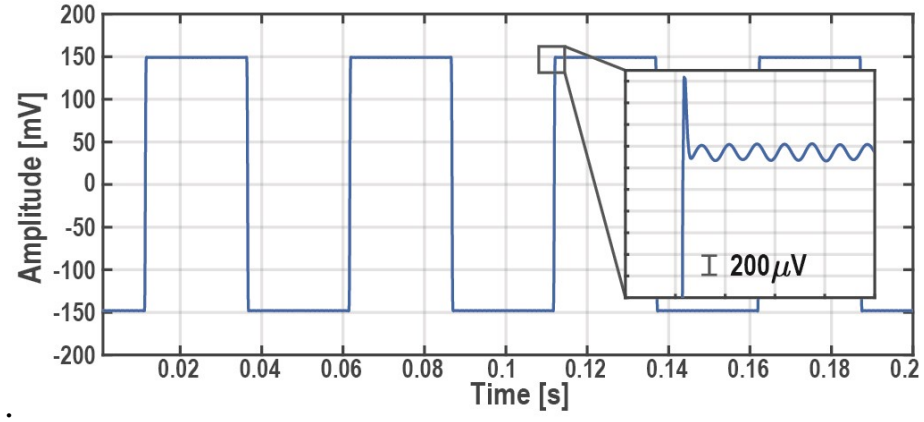

Figure 3.18. Square wave and sinusoid combined.

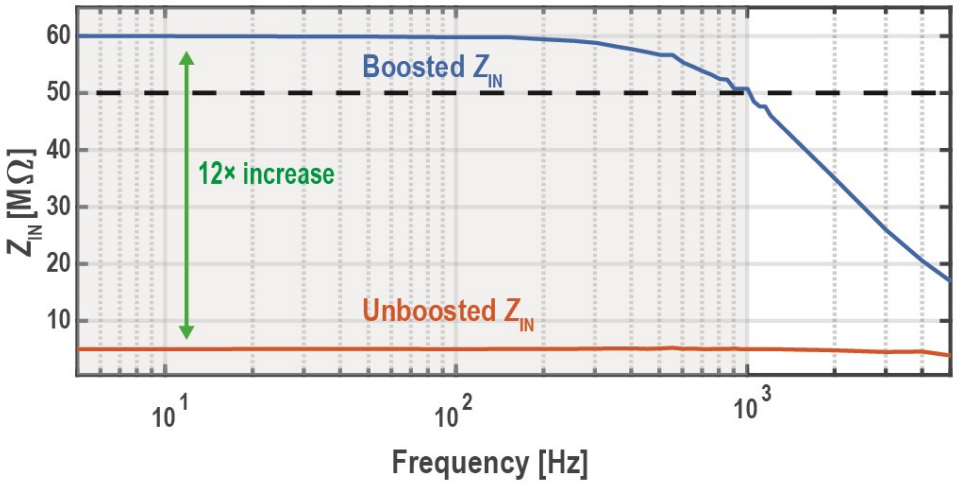

Figure 3.19. Measured input impedance with and without impedance boosting.

them. Figure 3.19 shows Z_{in} measured across the bandwidth with and without activating the auxiliary path booster. Z_{in} is boosted by 12× when the auxiliary path is enabled and is >50 MΩ across the entire bandwidth.

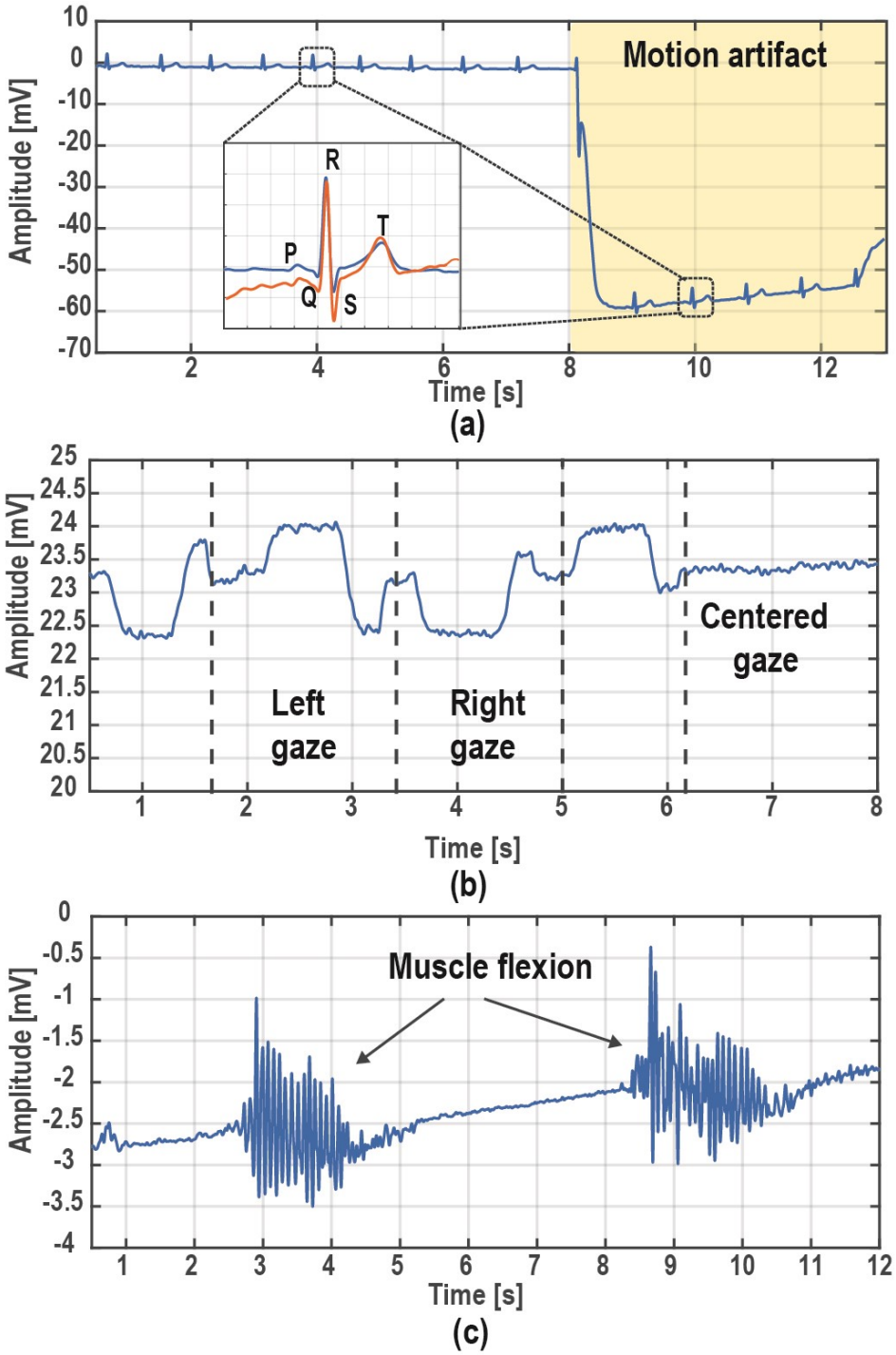

Figure 3.20. ExG measurements: (a) ECG, (b) EOG, and (c) EMG.

3.4.2 Biological Measurements

This ADC was validated by measuring various ExG signals with 3M red dot electrodes on a healthy volunteer. Figure 3.20(a) shows the waveform from a three-lead chest ECG recording. Around 8 seconds into the recording, motion artifacts were purposely generated to showcase the ability of the system to correctly digitize the ECG waveform in the presence of large motion artifacts like one would encounter with a wearable in a non-stationary environment. The system does not saturate, and the ECG waveform can be observed and extracted despite the large motion artifact. The system was also used to measure EOG [Figure 3.20(b)] and EMG [Figure 3.20(c)], showing that the system can measure standard ExG waveforms.

Table 3.1. Performance summary and comparison to the state-of-the-art

	[19]	[24]	[20]	[22]	[41]	[40]	This work
Integration domain	Time	Time	Time	Hybrid	Voltage	Voltage	Time
Topology	Open-loop	1^{st}-ord.	1^{st}-ord.	2^{nd}-ord.	3^{rd}-ord.	CCIA + 3^{rd}-ord.	2^{nd}-ord.
Technology[nm]	40	65	40	65	180	65	65
Area [mm^2]	0.135	0.08	0.025	0.078	0.5	0.113	0.075
Supply (A/D)[V]	1.2/0.45	0.8	0.8/0.6	1	1	1.2	1.2/0.8
Power [µW]	7	1.68	4.5	6.5	6.5	7.3	4.25-5.8
Coupling	ac	ac w/chop	ac w/chop	dc	ac w/chop	ac w/chop	ac w/chop
Input-range [mV_{pp}]	100	460	100	300	360	200	400
Sampling frequency[kHz]	3	64	2500	1280	12.8	400	200
BW [kHz]	0.2	0.5	10	10	0.3	5	1
CMRR [dB]	66	97	83	76	84	78	100.2
Input-referred noise [nV/√Hz]	367	118	36	95	265	90	110
SNDR [dB]	75.2	94.2	78.5	80.4	84.3	78	92.3
DR [dB]	77.4	95.1	79	80.4	84.3	81	92.3
SFDR [dB]	79	128	91	92.2	104.7	81	110.3
Z_{in} at DC / BW [MΩ]	∞ / 8	8 / 8	0.22 / 0.22	∞ / 13.3	39 / 39	1500 / 19.6	60 / 50
FoM_{SNDR}[dB]	149.6	178.9	172	172.3	160.9	166.4	174.7

3.4.3 Comparison to the State-of-the-Art

Table 3.1 compares this work with recently published direct digitization ADCs operating in the time and voltage domains. This work achieves excellent linearity due to the improved matching of the proposed GIRO-based quantizer. The time-domain signal processing also enables significant power savings in the "nominal" operating state (*i.e.,* in the absence of artifacts). This work achieves a competitive Schreier figure-of-merit (FoM) of 174.7 dB while maintaining an input impedance >50 MΩ over the entire bandwidth of interest.

3.5 Conclusion

This chapter presents a direct-digitization VCO-based ADC for biopotential sensing application that achieves over 90 dB SNDR and 100 dB SFDR, enabling it to digitize small ExG signals in the presence of large motion artifacts and interference. This is accomplished by enabling second-order noise-shaping using an integrating and time-encoding VCO-based 1st stage followed by a multi-phase, multi-quantizer noise-shaped TDC. The system's linearity is further improved using a GIRO that significantly reduces the mismatch sensitivity. Leveraging the time-based processing of the ADC, the system's power is naturally duty-cycled with the input amplitude, leading to 35% power savings in the absence of artifacts. To achieve the high-input impedance required to interface with small electrodes, an input-impedance boosting circuit is placed around the input chopper, boosting the input impedance by a factor of 12× and guaranteeing >50 MΩ input-impedance over the entire bandwidth while achieving very high linearity, low noise, and power-efficiency.

Acknowledgments

Chapter 3, in full, is a reprint of the material as it appears in C. Pochet, J. Huang, P. Mercier, and D. A. Hall, "A 174.7-dB FoM, 2nd-Order VCO-Based ExG-to-Digital Front-End

Using a Multi-Phase Gated-Inverted-Ring Oscillator Quantizer," in *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, vol. 15, no. 6, pp. 1283-1294, Dec. 2021, doi: 10.1109/TBCAS.2021.3133531.

The dissertation author was the primary investigator and author of this paper.

CHAPTER 4: THIRD ORDER VCO-BASED DIRECT-DIGITIZATION

4.1 Introduction

The rise of the internet-of-things (IoT) and distributed sensor nodes with on-chip machine-learning and edge processing drive the need for low-power, high-precision ADCs. These highly digital system-on-chips (SoCs) are best implemented in advanced process nodes that have low intrinsic gain and low supply voltages. These, unfortunately, make designing the high-performance amplifiers required in high-resolution delta-sigma (ΔΣ) ADCs challenging [1].

Several techniques have been explored to enable low-supply voltage operation, such as bulk input amplifiers, tail-less inverters, and bulk biasing [54], [55], [56], [57]. However, these techniques often require removing the amplifier's tail-biasing to maintain enough voltage swing at low supply voltages, which involves trading the power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) for swing, ultimately compromising the robustness. Another route is to exploit time-based encoding since it is supply voltage agnostic and benefits from the faster switching times in advanced process nodes. Time-domain architectures are frequently realized using a voltage-controlled oscillator (VCO) where VCOs have been used to implement analog operations such as amplification, filtering, and integration [7], [58], [59], [60], fundamental blocks needed in many mixed-signal systems. The most common use of these time-domain blocks is in ΔΣ ADCs, as illustrated in Figure 4.1, where VCO-based integrators are popular due to their intrinsic phase quantization, open-loop noise-shaping [61], and, more

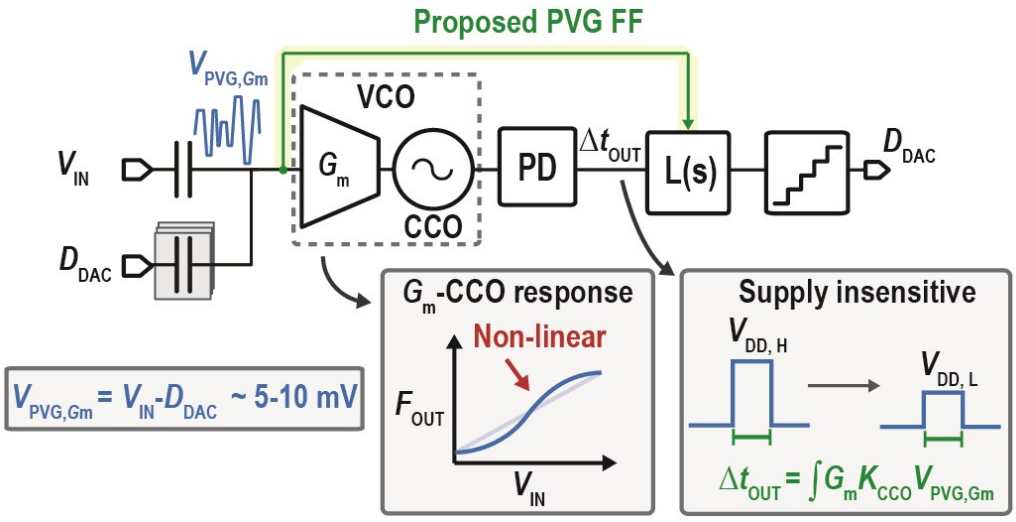

Figure 4.1. Capacitively coupled VCO-based ADC, highlighting advances and challenges of VCO-based ADCs and the proposed PVG FF technique.

importantly, their supply agnostic operation due to the time encoding of the phase information.

While most of the early research on VCO-based ADCs focused on high-speed applications with bandwidths above 10 MHz [9], [62], [63], [64], [65], the past decade has seen a growing interest in leveraging the small area and low supply operation of VCO-based ADCs for distributed sensing applications [10], [12], [24], [66], [67], [68]. These sensor front-ends typically require a wide dynamic range (DR) and linearity to capture sensor signals accurately. However, achieving high linearity has been challenging since the voltage to frequency gain of VCO-based ADCs is nonlinear, limiting the spurious-free dynamic range (SFDR) to only ~50 dB if used in open-loop. As such, significant research effort has focused on linearization techniques, such as adding feedback and/or digital calibration [9], [10], [24], [67]. However, as illustrated in Figure 4.1, even with feedback, the first integrator swing can still be a few 10s of mV due to the high-impedance node at the input of the integrator. This can limit the linearity and further cause quantization noise folding. Another challenge in time-domain ΔΣ architectures is that they are typically limited to 1st-order noise shaping. There have been attempts to increase the loop order, thus relaxing the

requirement on the quantizer resolution and the oversampling ratio (OSR); however, these relied on hybrid voltage- and time-domain architectures [17], [69], [70], [71], which unfortunately lose the scaling advantages of the time-domain-only architectures.

A few time-domain-only ΔΣ architectures have achieved higher-order noise shaping in a single loop. For instance, a 2nd-order VCO-only architecture used a time-encoding integrator in the first stage, followed by a closed-loop, noise-shaped time-to-digital converter (TDC) [12], but it required adding additional blocks to reduce the quantizer path mismatch and improve the SFDR. In [72], 3rd-order noise shaping is achieved through inner loop feedback. However, the first integrator is open-loop, which significantly degrades the linearity. Critically, the performance of these higher-order systems was lower than that of a 1st-order architecture due to the added complexity, and they were still far from their voltage-domain counterparts.

This work proposes an architecture building upon a typical time-domain capacitive DAC (CDAC)-based ΔΣ with a VCO-based integrator as the 1st stage, as illustrated in Fig. 4.1. A transconductor, G_m, and a current-controlled oscillator (CCO) form the VCO core, while a phase detector (PD) extracts the phase difference between the pseudo-differential CCOs. Due to the closed-loop operation, a pseudo-virtual ground (PVG) is created at the ADC input, reducing the swing seen by the VCO and thus linearizing the system. The PD guarantees supply voltage resilience due to the time-encoding. The core concept for the proposed technique relies on feeding forward the residue at the PVG to change the loop dynamics and linearize the first integrator by having it only process the quantization noise. This work demonstrates a 3rd-order, VCO-only ΔΣ ADC achieving 92.1 dB SNDR over a 2.5 kHz bandwidth (BW) using the proposed pseudo-virtual ground feedforward (PVG FF) technique. This approach enables a high DR due to the 3rd-order noise-shaping and >120 dB SFDR due to the linearization. The prototype ADC consumes 4.4 μW

from a 0.8 V supply, achieving the best-reported Schreier SNDR figure-of-merit (FoM) for VCO-based ADCs at 179.6 dB. This paper extends the work presented in [73].

4.2 Loop Filter Design

4.2.1 Architecture

The proposed architecture is best explained by starting with the well-known cascade of integrators with feedback (CIFB) architecture shown in Figure 4.2(a), where the loop is stabilized through a distributed feedback network. This structure leads to a natural implementation of the loop filter coefficients and is well known for its robustness and high anti-aliasing filtering [11]. However, it suffers from a few drawbacks that have pushed researchers to explore alternative architectures. Since the loop dynamics force the first integrator's output to cancel the DAC output, the integrator input is very tonal, and the integrator output amplitude scales with the input amplitude. This limits the coefficient scaling, which increases the ADC's area and the impact of noise from the subsequent stages, reducing the overall power efficiency. This input-dependent integrator output swing also increases the signal-to-quantization noise ratio (SQNR) degradation for a nonlinear integrator due to quantization noise folding [74].

Adding a feedforward path, as illustrated in Figure 4.2(b), solves some of these issues. Since the DAC at the output of the integrator contains a scaled copy of the input, feeding forward the ADC input to the integrator's output cancels the signal component from the DAC [75]. The feedforward path thus reduces the integrator swing at the expense of signal transfer function (STF) peaking and reduces the anti-alias filtering since the integrator is bypassed. The lower integrator

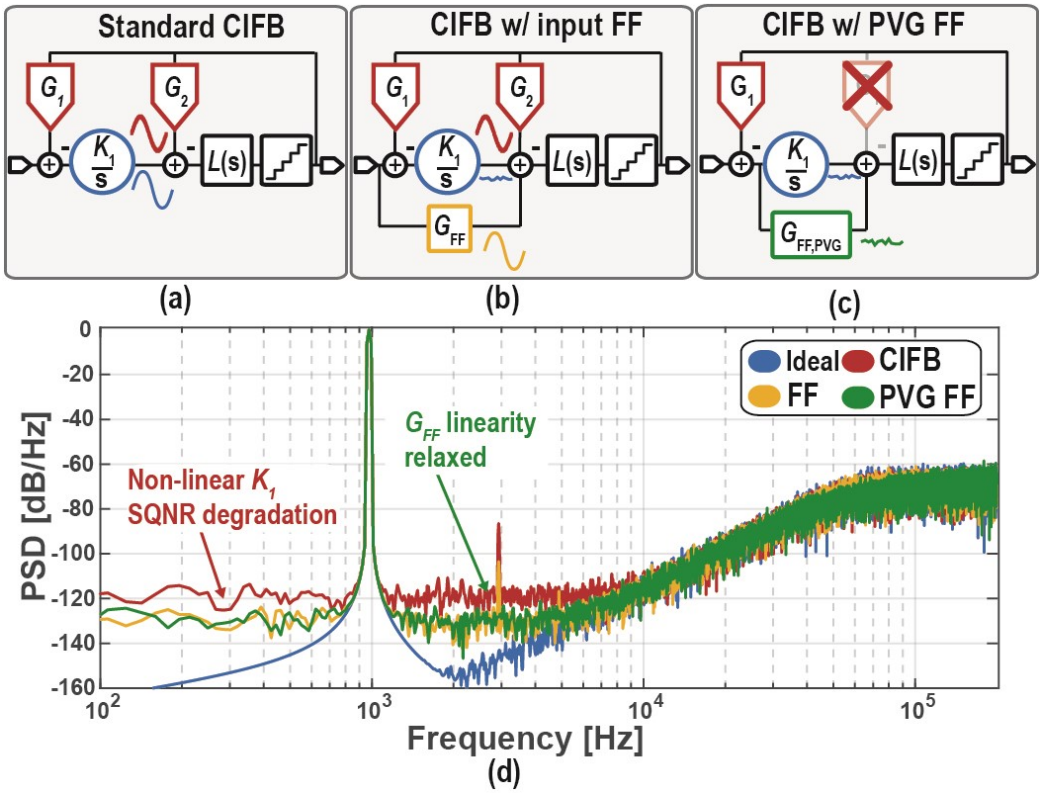

Figure 4.2. Comparison of (a) CIFB, (b) CIFB w/ FF, and (c) the proposed CIFB w/ PVG FF architectures. (d) Respective output spectra of each architecture.

output swing allows for more aggressive coefficient scaling and linearizes the integrator because it now mainly processes quantization noise. However, the feedforward path processes the full-swing input signal and must be linear despite the gain attenuation due to the first integrator. To abide by this strict linearity requirement, the feedforward path is typically implemented by a resistor connected from the input to the virtual ground of a closed-loop *RC* integrator further down the loop.

Finally, Figure 4.2(c) shows the proposed PVG FF architecture block diagram. It builds on the FF architecture by noticing that for ideal signal cancellation, the FF/DAC nodes and the ADC input node perform the same operation, *i.e.*, V_{in}-V_{DAC}. While the path gains differ, the path gain ratios, *i.e.*, $G_2/G_{FF} = G_1$, are the same. This allows the signal to be fed forward from the ADC's

pseudo-virtual ground (the output of the first DAC) instead of the input with the appropriate scaling factor. This enables the loop to operate with the same dynamics as the standard FF-based architecture while eliminating the internal feedback DAC(s) and having the feedforward path process only a small swing, helping with its linearization.

Behavioral simulations of the three architectures show how they perform in the presence of nonlinearities. Based on simulation results, a G_m-CCO integrator has ~50 dB SFDR for a 50 mV_{pp} swing, similar to previous work [67]. The spectra with a nonlinear first integrator, K_1, and feedforward elements, G_{FF}, are compared to the ideal CIFB architecture for a 3rd-order loop filter. Figure 4.2(d) shows that the CIFB significantly degrades performance when introducing nonlinearities with noticeable tones and quantization noise folding. There is less quantization noise folding when the input is fed forward, but the feedforward element's nonlinearities still cause significant distortion. On the other hand, due to the reduced input swing of the FF element, the PVG FF architecture's performance is superior to the CIFB and the input-FF architectures with a similar SQNR as the input-FF but without the tones caused by the nonlinearity of the FF path. This demonstrates that high SNDR can be achieved despite the large PVG swing using the PVG-FF architecture. This leads to more power-efficient architecture as the linearity of the integrator and feedforward elements can be relaxed for a target SNR.

This architecture closely resembles the CIFF architecture as it uses feedforwarding to remove the need for internal DACs. It, therefore, shares the characteristics of the CIFF loop filter family, such as STF peaking and reduced anti-aliasing. It should be noted that the CIFF architecture could not be implemented straightforwardly in a VCO-based ADC as the final integrator and quantizer are merged, and feedforwarding directly to the quantizer is not possible.

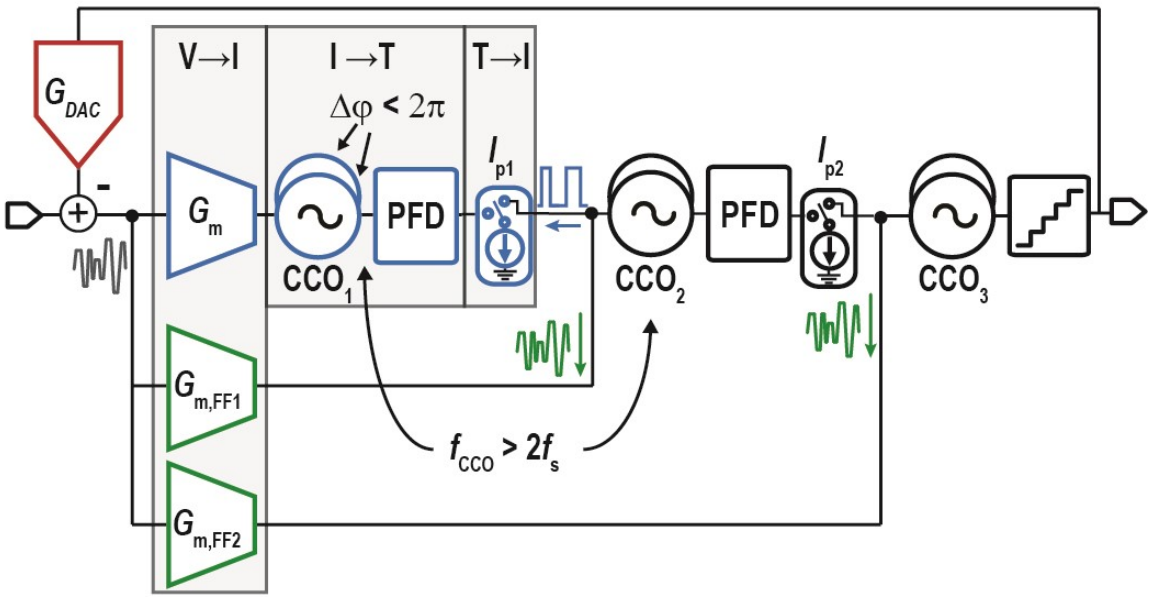

Figure 4.3. Block diagram of a VCO-based PVG-FF architecture.

Similarly, the PVG-FF technique would not be easy to implement with a closed-loop voltage-domain integrator, as the integrator's gain attenuates the virtual ground node, and loading this node slows down the integrator.

4.2.2 Loop Design

A block diagram of a 3rd-order PVG-FF architecture implemented using VCO-based integrators is shown in Figure 4.3. The feedback DAC generates a voltage that cancels the input voltage, leaving the residue voltage at the ADC's PVG. This voltage is converted to a current through a G_m-cell and fed to a pseudo-differential CCO. The CCO phase difference, $\Delta\varphi$, is extracted using a PD and then converted back into a current, where it is combined with the feedforward path, which is implemented with a transconductor due to the relaxed linearity. The time-domain integration and current-domain summation operations are repeated for the second integrator before the final VCO-based integrator. The last integrator's phase is quantized and fed back to the input.

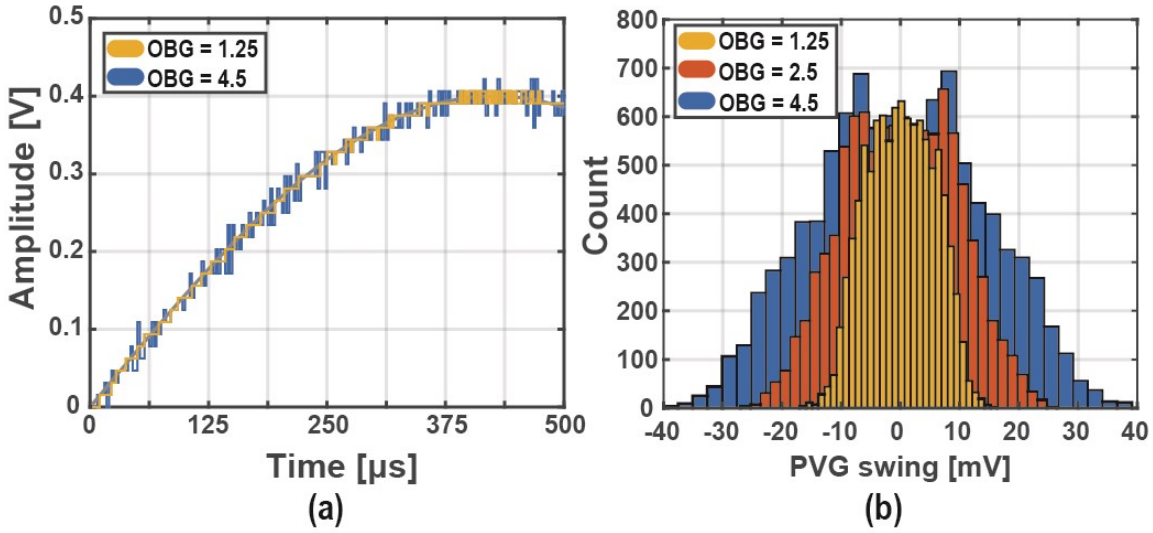

Figure 4.4. (a) ADC's scaled output for an OBG = 1.25 and OBG = 4.5; (b) PVG swing as a function of the OBG.

Designing the loop for a target SQNR depends on selecting key parameters such as the quantizer resolution, OSR, and out-of-band gain (OBG). The target SNR was 95 dB in a 2.5 kHz bandwidth; thus, the SQNR was designed to be 110 dB in *Simulink*, 15 dB above the target SNR, to ensure that the system is thermal noise limited and allow for some degradation when other non-idealities such as chopping artifacts, parasitics, and DAC mismatch are added later in the design phase. The DAC resolution was selected by trading off two parameters: the PVG node swing and the DAC layout complexity. Adding more bits results in a lower swing at the PVG node, allowing for better G_m-cell linearity and power efficiency. Simulations showed that an OBG of 2.5 and a 6-bit DAC had a maximum PVG swing of 50 $mV_{pp,diff}$ while maintaining a simple enough DAC layout. An OSR of 80 is then needed to achieve the target SQNR, considering the first integrator's nonlinearity. These parameters are similar to the state-of-the-art voltage-domain ADC reported in [40], which allows us to compare time- and voltage-domain architectures.

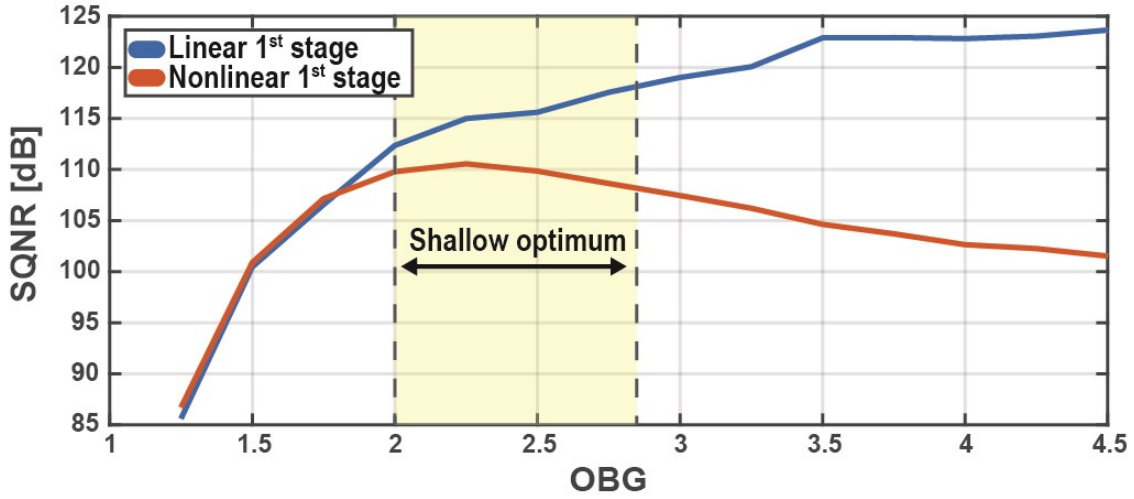

Figure 4.5. SQNR vs. the OBG for an ideal and nonlinear 1st stage.

The only remaining parameter to be selected is the OBG. Increasing the OBG results in a higher SQNR due to increased quantization noise filtering but affects the stability of the design; thus, the lowest OBG achieving the target SQNR should be selected. Interestingly, the OBG increase also affects the PVG swing. As illustrated in Figure 4.4(a), increasing the high-frequency gain creates "fuzziness" and increases the swing at the PVG. Figure 4.4(b) shows a histogram of the integrator input where the swing increases by ~4× from an OBG of 1.25 to 4.5. This increased swing causes the achievable SQNR to be limited by the integrator's nonlinearity due to quantization noise folding. This tradeoff is shown in Figure 4.5, where the SQNR is calculated for a linear and nonlinear integrator. One can see that the SQNR has a shallow optimum between 2 and 2.75, so we chose an OBG of 2.5 to allow for good performance even in the presence of coefficient variation. It should be noted that this optimum point will depend on several factors such as OSR, number of bits in the DAC and G_m-CCO linearity. The PVG swing also affects the maximum g_m/I_D of the G_m-cell in the integrators, as a large swing requires a lower g_m/I_D to avoid full current steering. The ADC's maximum signal amplitude (MSA) depends on the OBG;

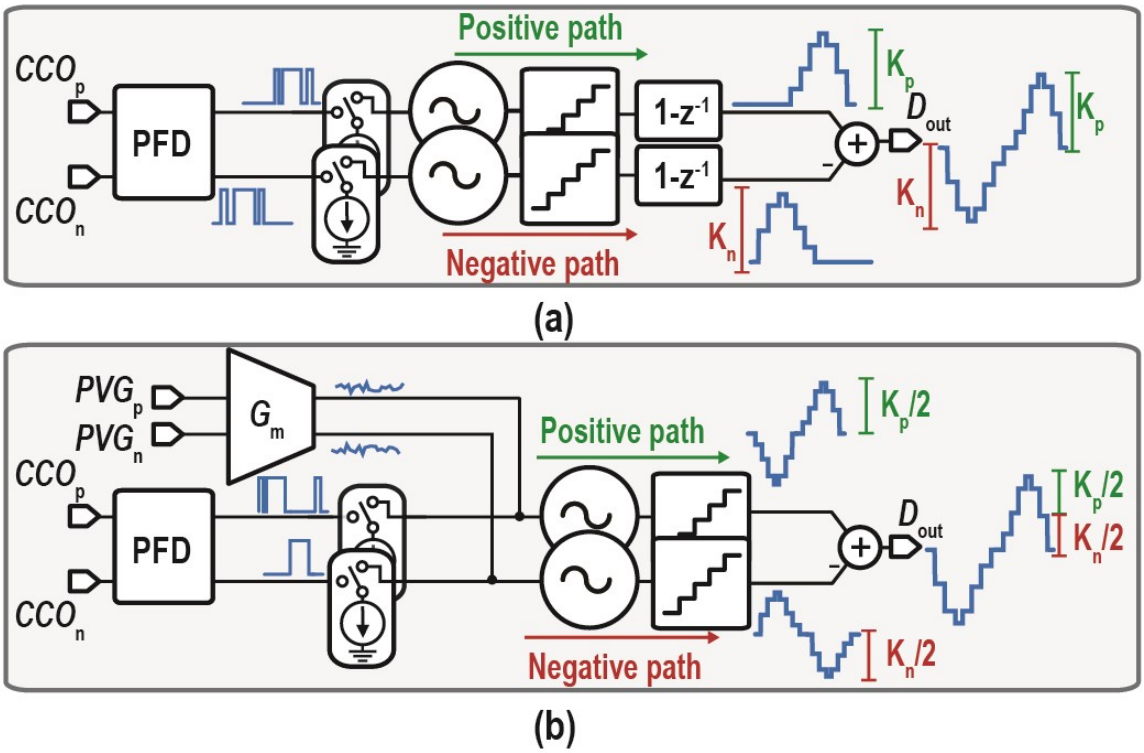

Figure 4.6. Block diagram of (a) frequency-domain and (b) phase-domain quantizers.

however, with a 6-bit DAC, the MSA is ~90% with <3% variation between an OBG of 1.25 and 4.5 due to the number of quantizer levels.

Another critical parameter for higher-order VCO-based ADCs is the SQNR dependence on the CCO frequency, f_{CCO}, and matching [12], [76]. Two types of VCO-based quantizers have been proposed in the literature – frequency-domain and phase-domain quantizers [64]. While these were used in hybrid voltage-/time-domain ADCs, they can also be used in time-domain-only architectures, as illustrated in Figure 4.6. Frequency-based quantization, where the VCO-based integrator in the quantizer is followed by a differentiator acting as a gain stage [12], [64], is illustrated in Figure 4.6(a). In this architecture, the loop dynamics force the time-domain encoding at the quantizer input to match the ADC input, thus leading to a pulse width modulated (PWM)-based polarity-dependent encoding of the input signal. This makes the quantizer sensitive to path

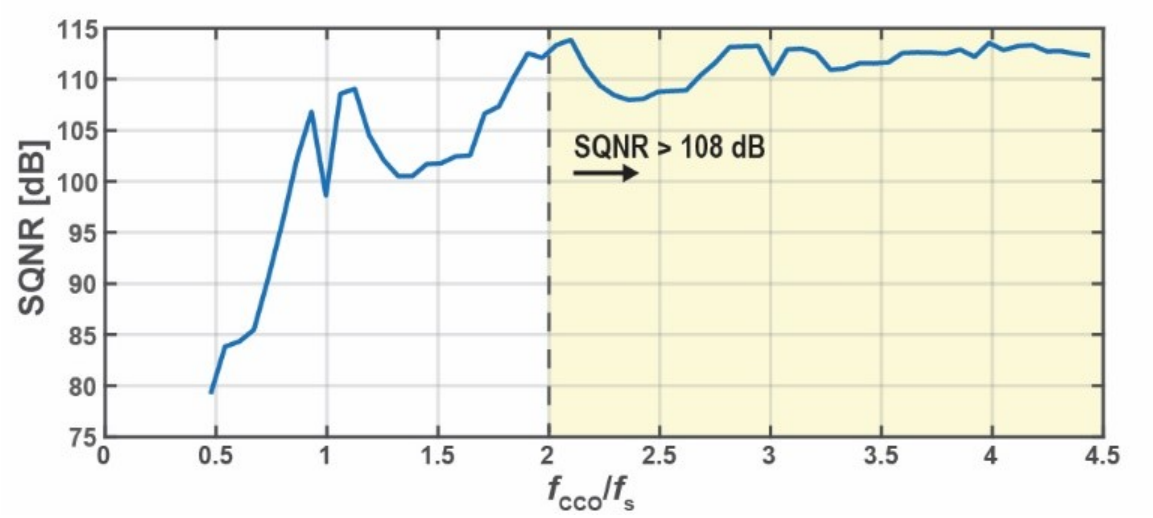

Figure 4.7. SQNR vs. the CCO frequency normalized to the sampling frequency.

mismatch (between the positive and negative quantization paths) and the preceding CCO's f_{CCO} due to the high-frequency content of the PWM encoding [16].

This is not the case for a phase-domain quantizer, where the quantizer acts as an integrator, and thus, the quantizer input is a representation of the derivative of the ADC input signal [64]. The quantizer is fed the PFD output and the G_m-FF signal, thus relaxing the frequency requirement, as only part of the input is PWM encoded and requiring that f_{CCO} just be higher than $2f_s$ to update the loop with the phase information at least once per sample. As illustrated in Figure 4.7, this ensures loop stability and SQNR > 108 dB. The derivative encoding in the phase-domain quantizer also benefits from being independent of the input signal polarity, which significantly relaxes the matching between the pseudo-differential VCO-based quantizers and does not require mismatch improvement using a gated-inverted ring-oscillator (GIRO), as was done in [12], [77]. If f_{CCO} cannot be reached with the desired coefficient, it is possible to virtually increase it by tapping multiple phases of the CCO [58], [62].

4.2.3 Coefficient Scaling

In voltage-domain architectures, the internal node's swing in the loop filter is limited by the supply voltage of the operational amplifiers in the integrators. Therefore, the coefficients must be scaled to avoid saturation, as saturation would cause a large SNDR degradation and can push the loop into an unstable state. In time-based ADCs, this constraint on the voltage swing is transferred to the time domain. Thus, the coefficients must limit the phase difference between the pseudo-differential CCO, $\Delta\varphi$, to avoid phase wrapping in the phase detector. This highlights the importance of the PD implementation, as its gain directly affects the loop dynamics and the inner loop's DR. The most popular PDs are an XOR gate and a phase-frequency detector (PFD). An XOR PD is duty-cycle sensitive and has a phase range limited to π (*i.e.,* the effective gain is $1/\pi$). On the other hand, a PFD-based PD has a $\pm\pi$ phase range and is edge-triggered. Maximizing the PD DR enables one to maximize the coefficient scaling and thus achieve better power efficiency. Therefore, a PFD-based PD was selected.

Referring to Figure 4.3 and using the PFD's gain, the K_1 coefficient can be derived as

$$K_1 = G_{\mathrm{m}} K_{\mathrm{CCO}} I_{\mathrm{p}} \tag{4.1}$$

where G_{m} is the transconductance, K_{CCO} is the CCO's current-to-frequency gain, and I_{p} is the amplitude of the pulsed current source. The noise requirement sets the G_{m}, leaving K_{CCO} and I_{p} to achieve the target gain. K_{CCO} should be maximized (up to the limit allowed by the PFD) to allow for higher f_{CCO} and minimize I_{p}, thus improving power efficiency. The loop parameters were extracted from behavioral simulations and extensively studied to ensure that the loop remained stable and $\Delta\varphi$ was limited to 2π for all signals in the band of interest.

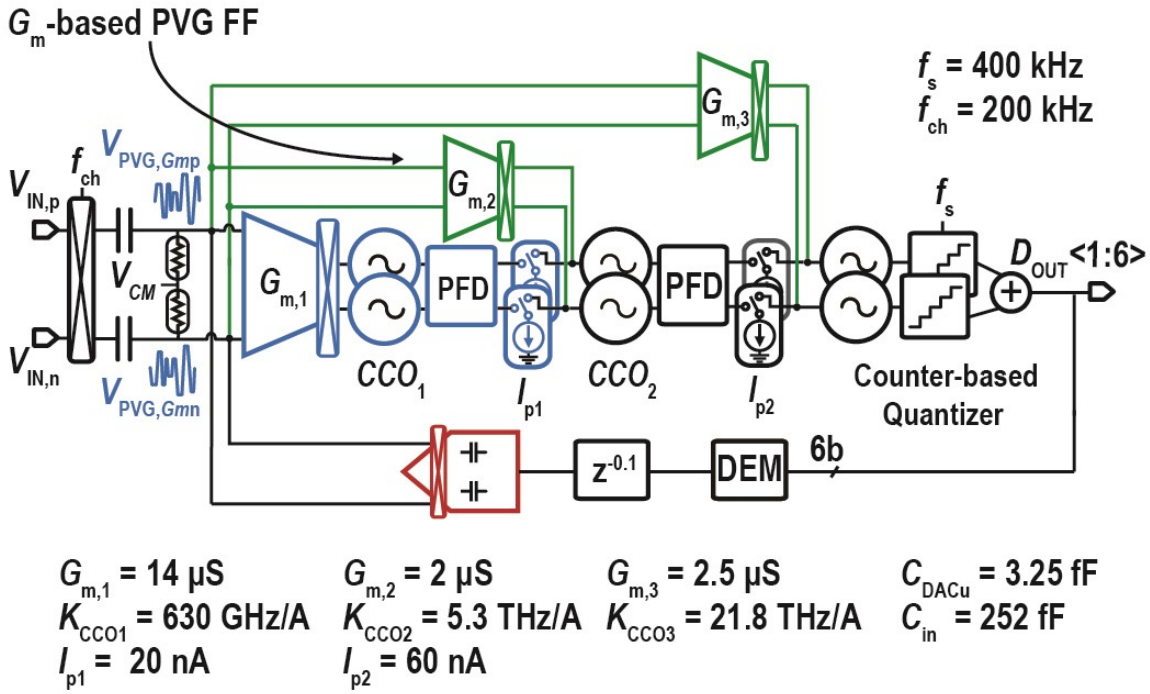

Figure 4.8. Block diagram of the proposed architecture and key coefficients.

4.3 Circuit Design

The proposed ADC is illustrated in Figure 4.8 with the relevant coefficients, the sampling frequency, f_s, and the chopping frequency, f_{ch}. The ADC input is chopped and capacitively coupled through two 252 fF metal-insulator-metal (MIM) capacitors onto the pseudo-virtual ground, a high-impedance node. Chopping pushes the flicker noise out of band and improves the ADC's CMRR. f_{ch} is set to $f_s/2$ to avoid quantization noise folding [78]. The output of each G_m-cell is chopped to ensure correct polarity in the loop. Due to the preceding gain, the G_m and power of the second and third VCO-based integrators are scaled by 10×. The final CCO's $\Delta\varphi$ is quantized with a 6-bit gray counter. A segmented dynamic element matching (DEM) algorithm [79] is applied to the output to ensure that the multibit DAC has high linearity. The DEM output is resampled after $0.1/f_s$ (125 ns) to allow time for the logic to settle and synchronize the DAC.

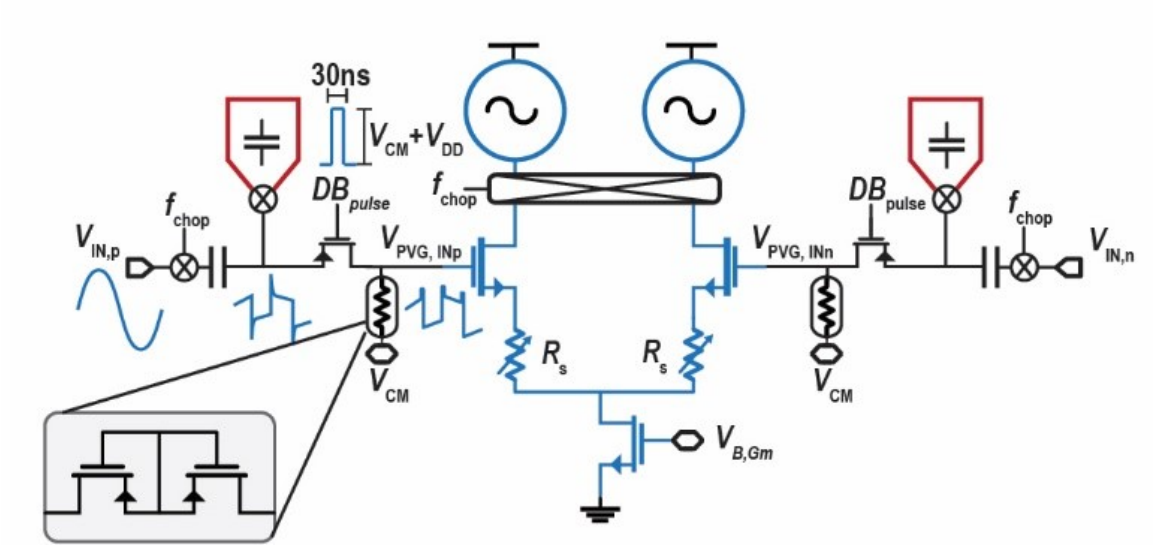

Figure 4.9. Schematic of the input transconductor with dead band switch.

4.3.1 G_m-cells

A schematic of the first G_m is illustrated in Figure 4.9 with the input chopper switches and ac-coupling capacitors. The input and DAC are capacitively coupled, and the input common-mode voltage, V_{cm}, is set through a pseudoresistor. All the G_m-cells share this node. The input chopper switches are clock boosted to $2V_{DD}$ to reduce the switches' on-resistance and allow for inputs above V_{DD} while maintaining high linearity. Chopping the CDAC induces large differential-mode chopping artifacts at the high-impedance PVG node due to the sudden switching and settling of the DAC capacitors upon a polarity swap. These artifacts significantly degrade the ADC performance by pushing the G_m-cell out of saturation, causing harmonics and quantization noise folding. It was proposed in [31] to remedy this issue by adding dead-band switches that isolate the G_m-cell from the large differential artifact. By opening the dead-band switches for a short time around the chopping instant, these artifacts are converted to common-mode charge injection and attenuated by the G_m-cell's CMRR [12], [40]. This allows the ADC's performance to be minimally impacted by the artifacts and maintain a high SQDR. An on-chip pulse generator creates the 30 ns

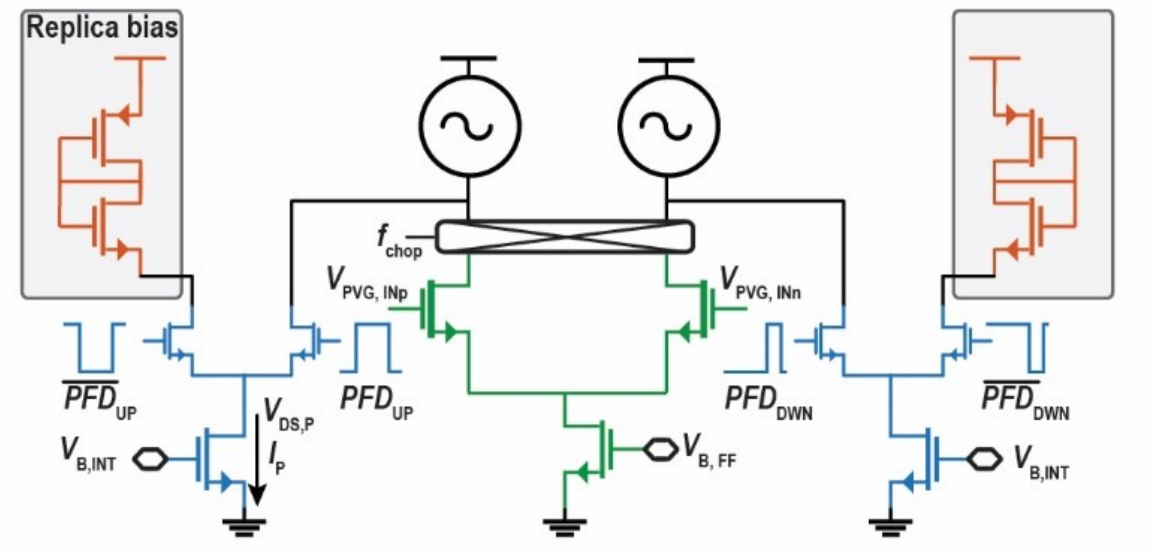

Figure 4.10. Schematic of the second and third integrator transconductors.

dead-band pulse and boosts the gate to $V_{CM}+V_{DD}$ to guarantee that the PMOS switches remain off even with artifacts above V_{DD}.

The first G_m-cell is implemented with NMOS thick-gate oxide devices to minimize gate leakage and source-degenerated by a 3-bit programmable resistor. The G_m-cell's current and source degeneration provide coefficient tuning and linearity adjustment post-fabrication to optimize the loop filter coefficients and the achievable SNDR. The output current is down-chopped and connected directly to the CCO for maximum current reuse and power efficiency. The second and third-stage CCO inputs combine the FF path and the PFD-driven integration pulse currents. Due to the architecture's relaxed FF path linearity requirement, the FF G_m-cells are implemented with standard differential pairs using thick-gate oxide devices for low gate leakage and biased in weak inversion ($g_m/I_D > 15$), as illustrated in Figure 4.10.

To ensure a fast and sharp rise time of the PFD-driven pulsed current sources, they are never turned off and instead shunted to a replica CCO in the off state, similar to a current steering DAC [80], thus maintaining a relatively constant V_{DS} across the current source. The switch does

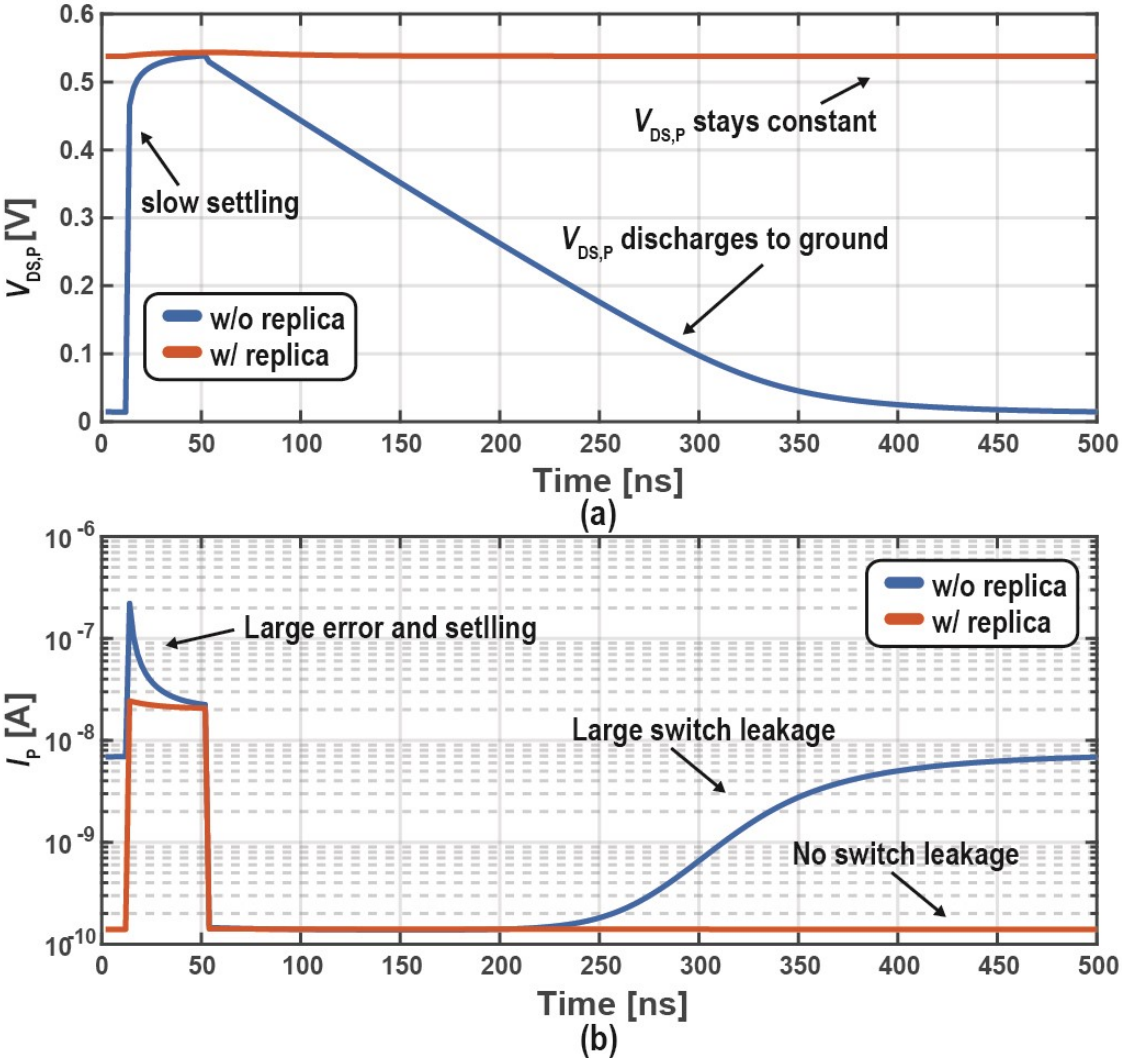

Figure 4.11. Simulated (a) voltage and (b) current transient waveforms with and without the replica circuit.

not require any calibration or specialized synchronization as this pulser appears after the integrator; thus, any error is shaped when input-referred. The power cost of this is negligible since $2I_{p1}+2I_{p2}$ ≈ 150 nA. This has significant performance benefits, as demonstrated in the simulation results shown in Figure 4.11(a), where the circuit is simulated for a 40 ns pulse with and without the replica branch. Without the replica circuit, the current source's V_{DS} settles slowly to its nominal value and discharges when the switch is off. This causes the voltage across the switch at the drain

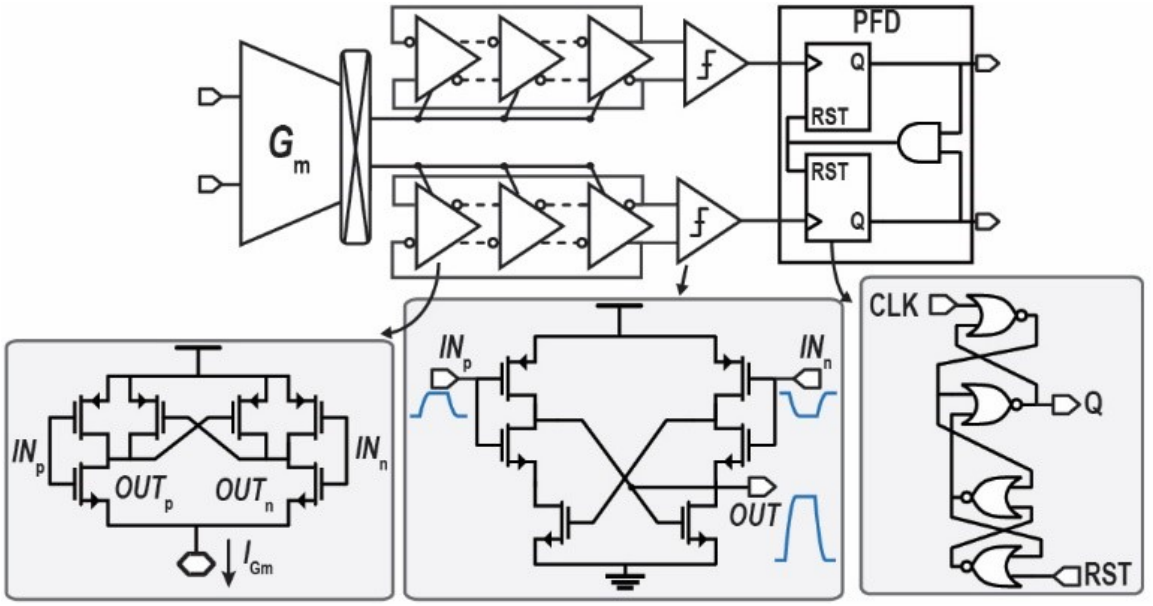

Figure 4.12. Schematic of the current-controlled oscillator and phase frequency detector.

of the current source to increase, leading to significant leakage, as shown in Figure 4.11(b). When the replica is added, V_{DS} stays constant at ~540 mV, and the current settles much faster to the desired value while guaranteeing <200 pA of leakage in the off state.

Simulations showed that mismatch between the pulsed current sources (σ = 5%), easily achieved through layout and sizing, causes an SQNR variance of 0.3 dB, which is negligible because the mismatch appears after the first integrator. The three G_m-cells attached to the PVG-FF node add 90 fF of parasitic capacitance, which is compensated by tuning the loop filter coefficients. The input transistors were sized to achieve the target G_m, and the area was selected to ensure the flicker noise corner was less than 100 kHz (f_{chop}/2).

4.3.2 CCO and PFD

The ring-oscillator-based CCO implementation is shown in Figure 4.12. The ring is current starved by the NMOS-based G_m-cells and implemented as pseudo-differential PMOS cross-coupled stages for low-phase noise [10]. Low-V_T (LVT) devices guarantee a small ring-oscillator swing, 200 to 300 mV, over the frequency range. The inverter is sized for symmetric transitions to

minimize phase noise and the number of stages selected to achieve the target K_{CCO}. As illustrated in Figure 4.12, the level-shifters following the CCO to allow for rail-to-rail logic are implemented from [20] and consume negligible power. The PFD is built using a standard NOR-based DFF with custom logic gates implemented using high-V_T (HVT) devices to decrease the leakage power, leading to a 2 ns reset delay. This delay is sufficient to ensure settling time for the current pulser, even for small $\Delta\varphi$.

4.3.3 Quantizer and DAC

The VCO's phase is quantized using a counter-based quantizer [12], [66]. The VCO edges are asynchronous to the sampling instant; as such, the counter topology must be chosen carefully to avoid sampling the counter output during the transition of multiple internal bits [24]. To this end, the counter uses a gray code that allows only one internal transition during counting and guarantees minimal transition errors [24]. The counter accumulates $\Delta\varphi$, adding the difference to the ADC output. This result is then passed through a segmented DEM algorithm [79], simplifying the DAC implementation by reducing the number of elements compared to data-weighted averaging (DWA) and allowing for 1st-order shaping of the DAC mismatch. The DAC unit elements are custom metal-oxide-metal (MOM) capacitors for more flexibility during the layout of the DAC, with a 3.25 fF unit capacitance for a total DAC capacitance of ~250 fF. The capacitor variation was expected to be ~0.25% [52], degrading the ADC's performance by less than 1 dB in simulation.

4.4 Measurement Results

The proposed ADC was fabricated in a 65 nm LP-CMOS process and occupies 0.1 mm^2. An annotated chip micrograph is shown in Figure 4.13, where the feedforward transconductors were laid out near the main G_m-cell to minimize the parasitic loading at the input node, maximize

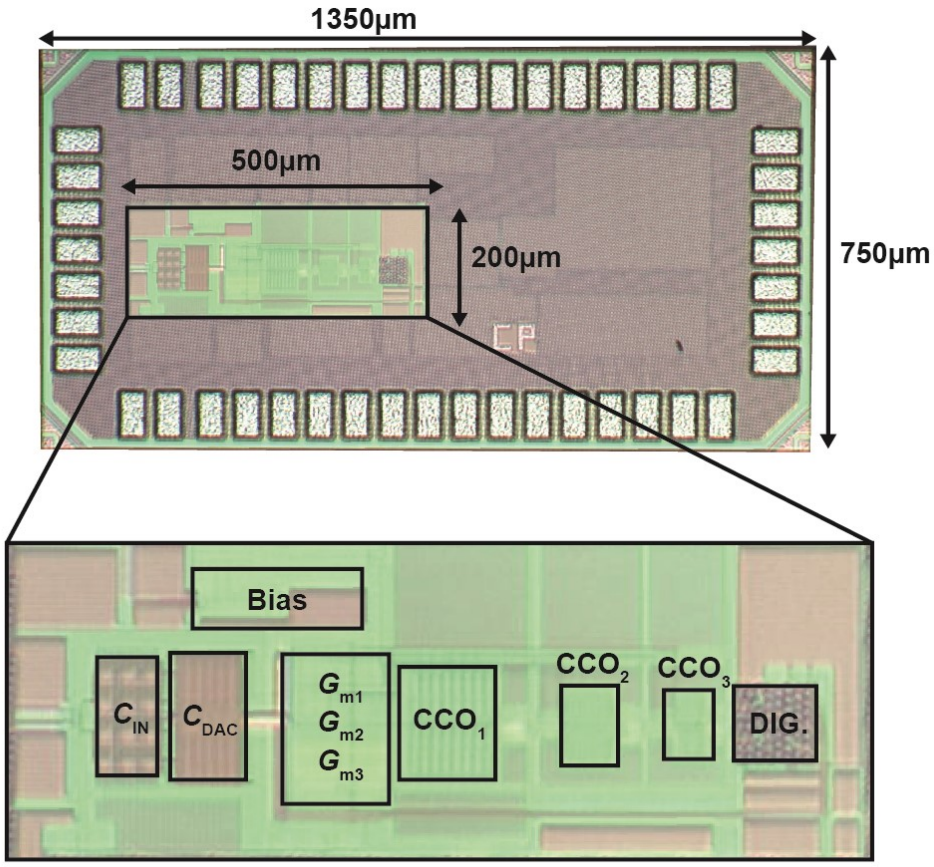

Figure 4.13. Annotated chip micrograph.

matching, and avoid resistive loss. The ADC consumes 4.4 µW from a 0.8 V supply, as shown in Figure 4.14(a). The CDAC reference voltage is 1.2 V to maximize the ADC input range. The power consumption is dominated by the first integrator, followed by the on-chip digital blocks, such as the counter and DEM algorithm, which would benefit from technology scaling. Figure 4.14(b) shows that the shaped CDAC mismatch (from the DEM) dominates the input-referred noise power. This could be remedied by using DWA, which would increase the tonality but decrease the in-band noise generated by the mismatch shaping by 6 dB, or by improving the CDAC layout and increasing the unit capacitors' area for improved matching. It is estimated that this would lead to a ~2 dB improvement in the ADC performance. The active area of the ADC is only

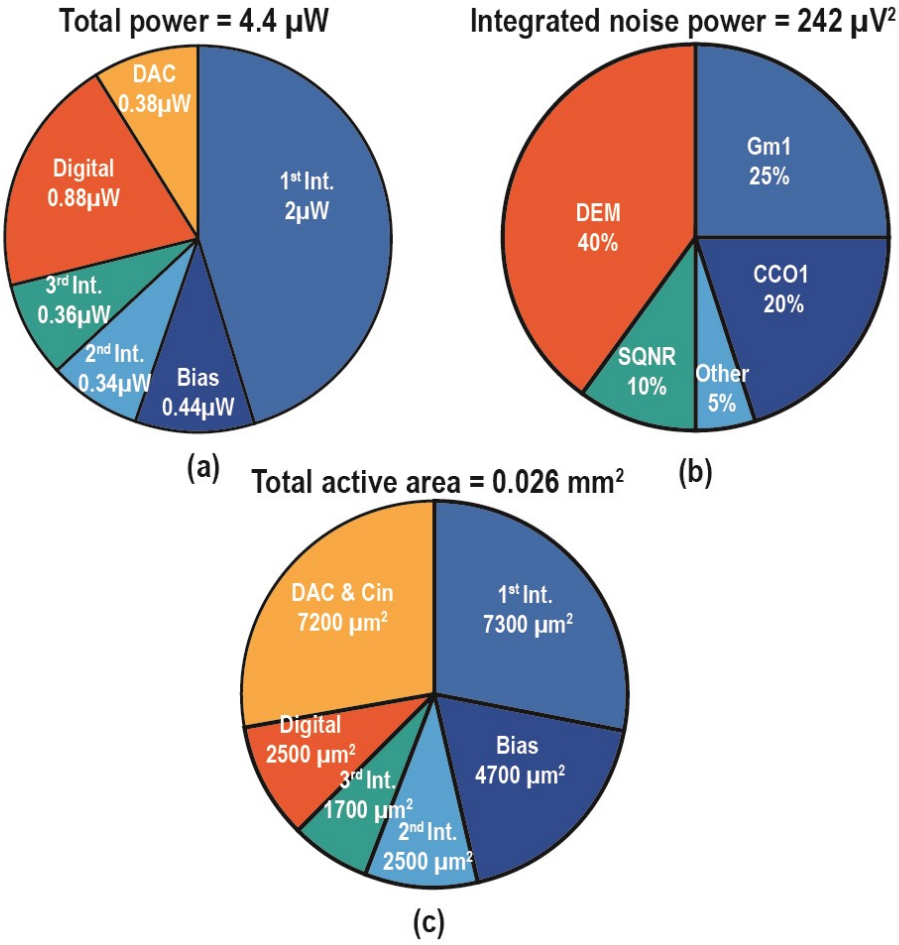

Figure 4.14. (a) Power, (b) noise power, and (c) area distributions.

0.026 mm^2, largely due to the first integrator, DAC, and input capacitors, as shown in Figure 4.14(c).

4.4.1 Spectral Characterization

The chip was tested using an Audio Precision APx555B ultra-low distortion signal source applying a 1.8 V_{pp} full-scale sinusoidal input at 322 Hz. The input common-mode was set to 500 mV, so each differential input varies between 50 mV and 950 mV with a 1.8 V_{pp} differential input. Despite the large voltage across the clock-boosted chopping switches, no reliability issues were observed. Figure 4.15(a) shows the output spectrum where the ADC achieves a peak SNDR of 92.1 dB in a 2.5 kHz bandwidth and an SFDR of 123 dB. The 60 Hz and 180 Hz tones are caused

by power line interference, as this was not tested in a Faraday cage. The characteristic 60 dB/decade noise-shaping from a 3rd-order modulator is apparent, confirming the proper operation of the loop. The spectrum when DEM is deactivated is shown in Figure 4.15(b), demonstrating a significant degradation in linearity (>60 dB) without the mismatch shaping algorithm. This also shows that the noise-shaping is degraded below 10 kHz due to DEM's 1st-order mismatch shaping. This amount of degradation was unexpected and indicates that the DAC mismatch is higher than the 0.25% anticipated. The authors believe that a 0.5% mismatch, which would decrease the SQNR to about 95 dB, as illustrated in the noise breakdown, causes a significant loss in performance as the quantization and DAC error shaping contribute to about 40% of the input-referred noise. The flicker noise corner is at ~60 Hz due to the CCO, which can not be chopped. It was sized to have symmetric rise and fall times while maximizing the area. However, the flicker noise still contributes ~15% of the ADC's noise. The dynamic range was characterized by sweeping the input amplitude, achieving a 92.1 dB DR. The SNDR was then measured with a full-scale input sinusoid from 50 Hz to 2.5 kHz, where <0.5 dB variation was observed [see Figure 4.16]. Due to the high number of bits in the internal quantizer, the SNR and DR should have similar values.

The ADC's linearity was measured across the ADC's bandwidth and dominated by the third-order harmonic distortion (HD3). As shown in Figure 4.17, the maximum in-band HD3 is 119.6 dBc. Above 833 Hz, the third harmonic lies out of band while the second harmonic (HD2) remains below 121 dBc up to $f_s/2$. The measured intermodulation distortion (IMD) was 114.2 dB with -6bdBFs inputs operating at 789 Hz and 961Hz, as shown in Figure 4.18, limited by the APx555B, which only guarantees the IMD residual to be <110 dB. CT-ΔΣ ADCs are also known to exhibit anti-alias filtering behavior, enabling them to filter out-of-band signals and avoid noise folding. This attribute was measured, and the results are shown in Figure 4.19 for a -33 dBFS (40 mV_{pp})

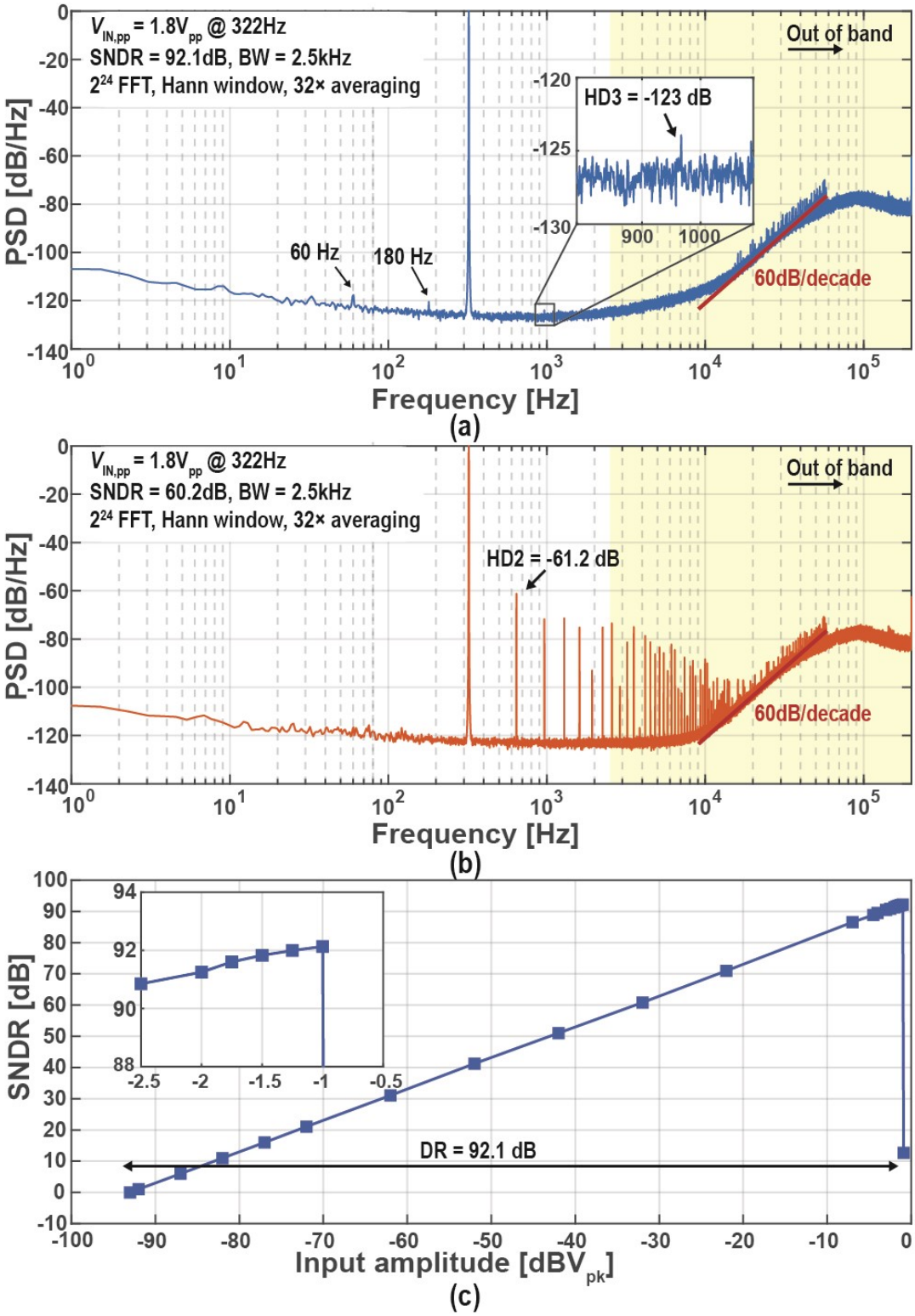

Figure 4.15. Measured ADC (a) spectrum with DEM, (b) spectrum without DEM, and (c) dynamic range.

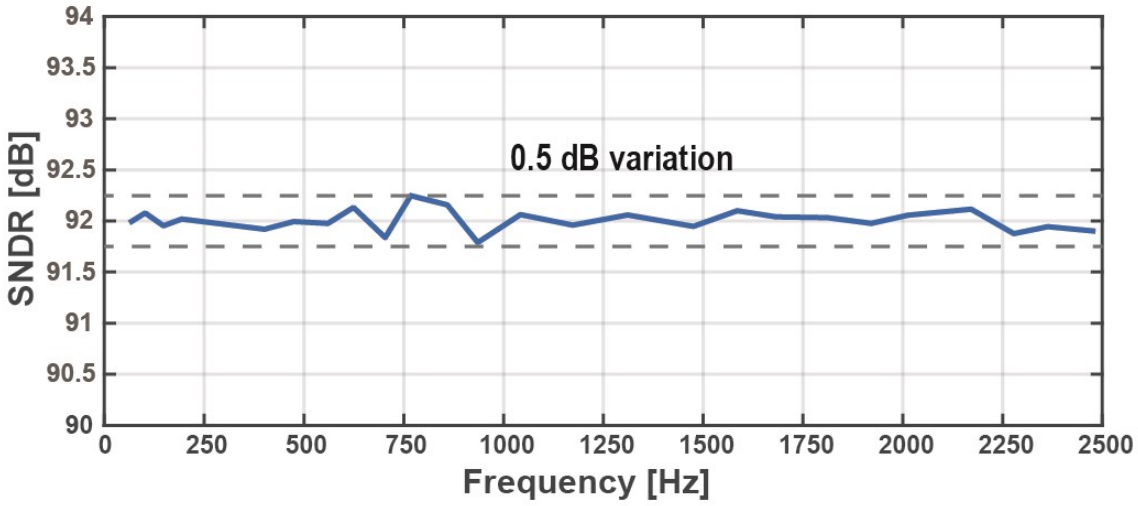

Figure 4.16. Measured ADC SNDR across its bandwidth

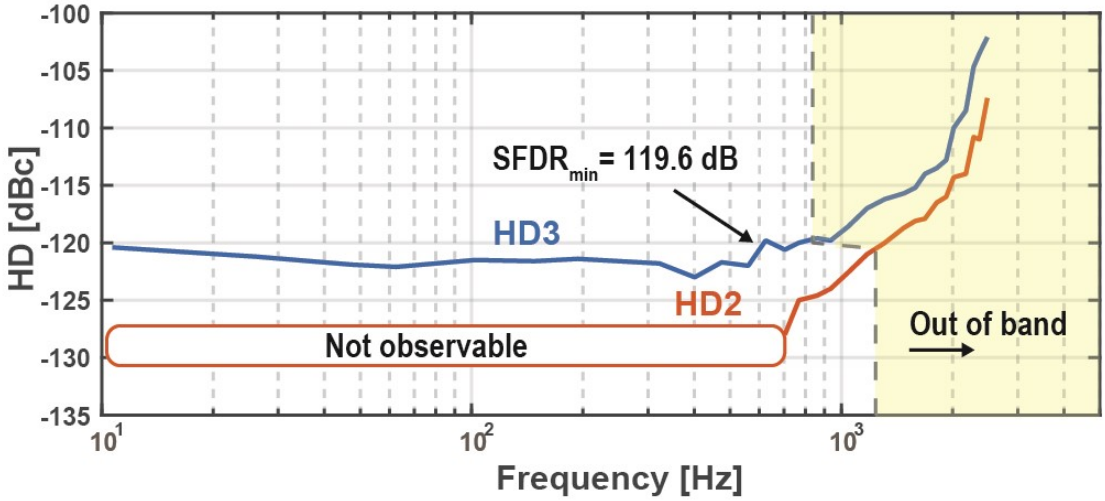

Figure 4.17. Harmonic distortion (HD2 and HD3) as a function of frequency.

input signal from f_s – BW to f_s + BW (BW = 2.5 kHz). The tone folded back in-band was measured, and the rejection in-band was ~42 dB. This is lower than a 3rd-order CIFB structure due to the feedforward paths. The anti-alias filtering is also reduced by the dead-band switch at the input, which operates at f_s and demodulates part of the signal back in-band before the loop can filter it out [40]. It should be noted that with an OSR of 80, adding a 1st-order low-pass filter at the input would provide an extra 38 dB of filtering at f_s, bringing the total to 80 dB.

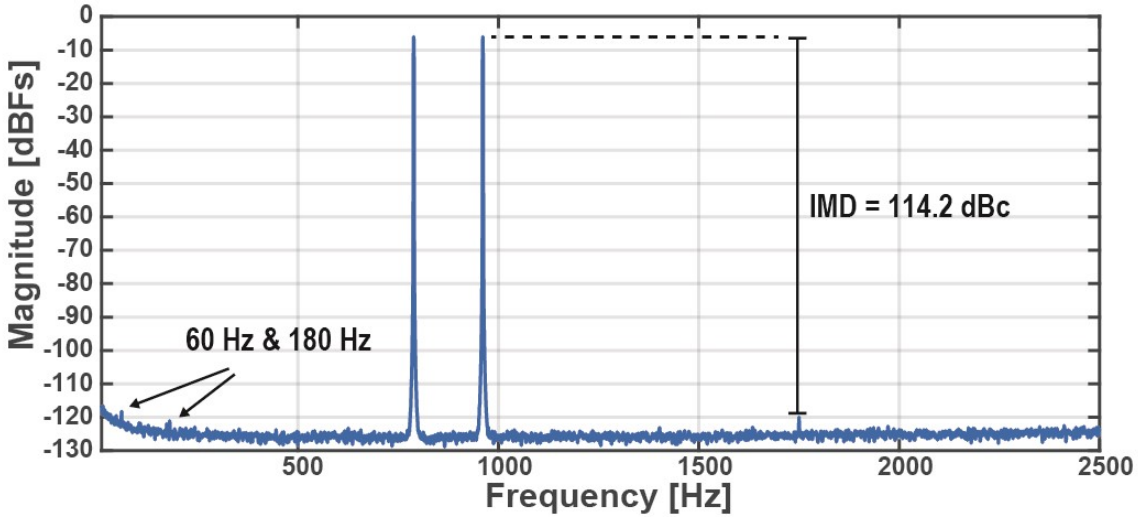

Figure 4.18. Measured intermodulation distortion.

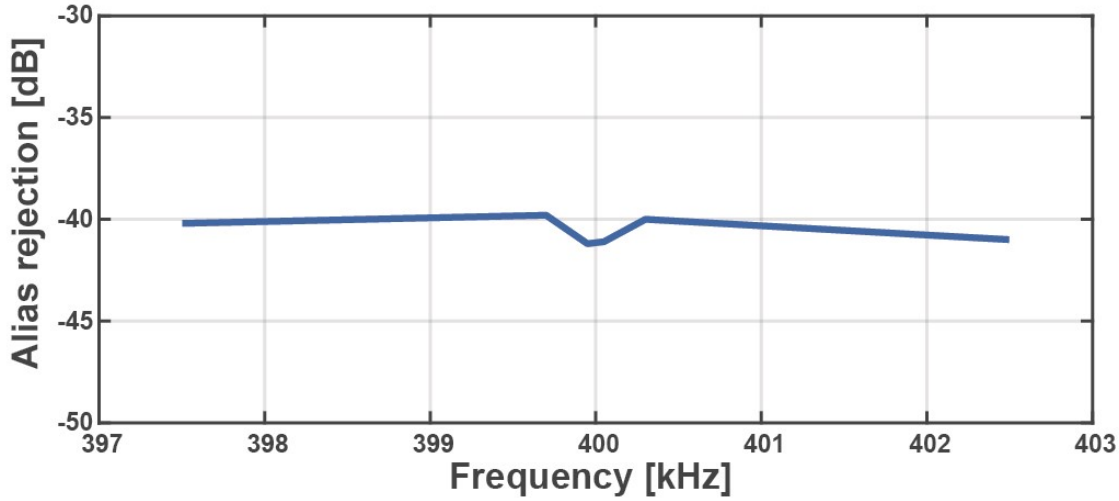

Figure 4.19. Measured alias rejection with a -33 dBFS input tone around f_s.

4.4.2 Robustness to Variation

Achieving robust performance with a VCO-based ADC is a well-known challenge due to its open-loop nature and the coefficients set by G_m and K_{CCO} (1), which are notoriously sensitive to process, voltage, and temperature (PVT) variation. This sensitivity can cause the loop coefficients to vary significantly with temperature and process. This was partially addressed in the system's design, where a constant-G_m biasing circuit was used to stabilize G_m, and current-starving the CCO guarantees a supply-independent swing. Simulations show that the loop coefficients vary by ±10%

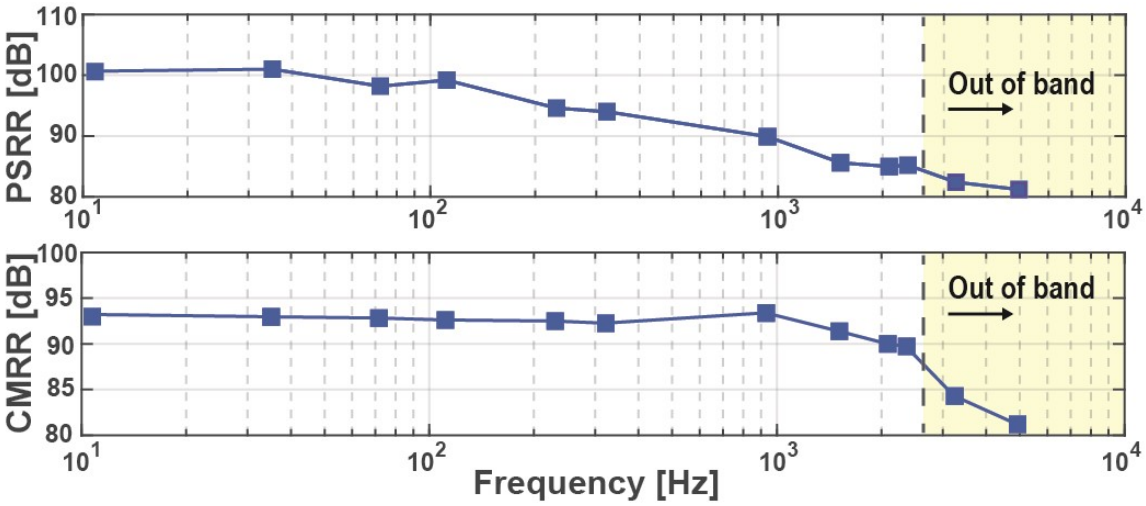

Figure 4.20. Measured ADC (a) PSRR and (b) CMRR.

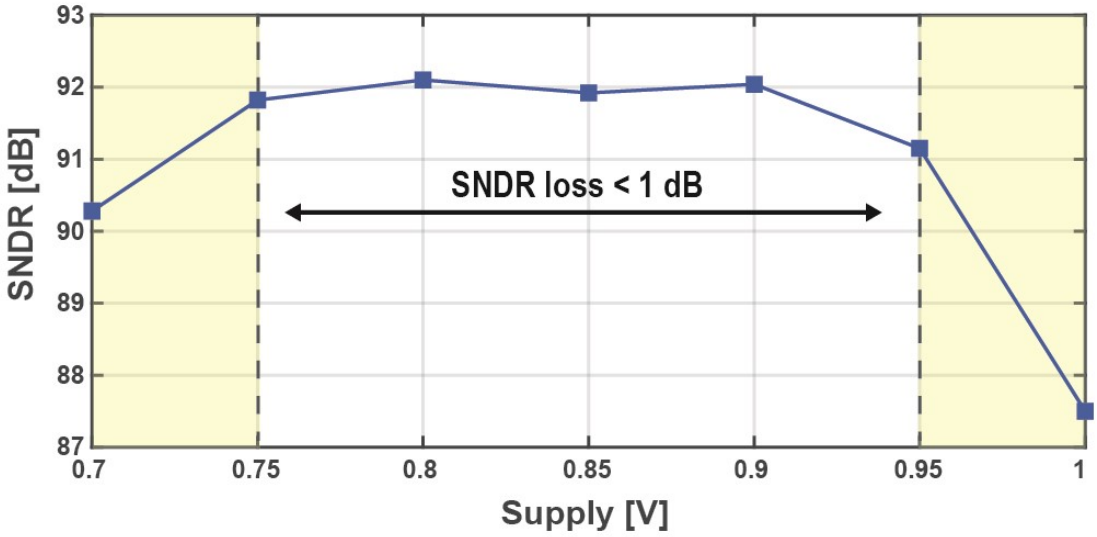

Figure 4.21. Measured ADC SNDR across analog supply voltage.

with process and temperature (0-70 °C) and by less than 0.2 %/V with supply variation. As shown previously, f_{CCO} variation is also acceptable (provided $f_{CCO} > 2f_s$), minimally degrading the SQNR.

The loop coefficients were tuned manually to the correct operating point post-fabrication by controlling the current in the G_m-cell and the pulsed current sources. This robustness with supply voltage variation is shown in Figure 4.20, where the measured PSRR with a 100 mV_{pp} tone added

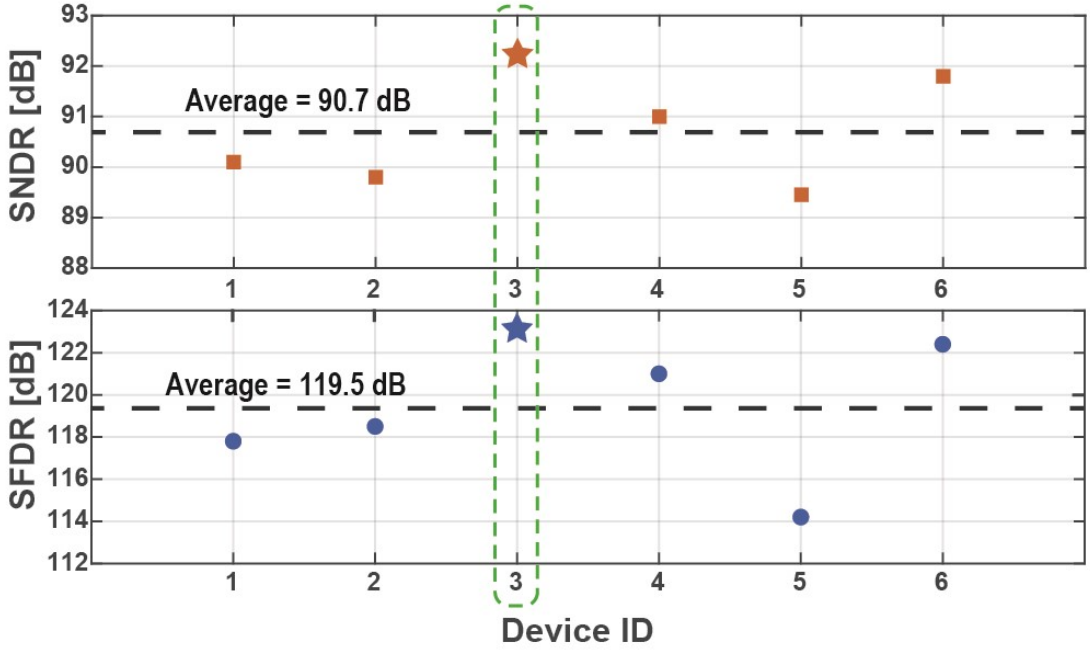

Figure 4.22. Measured SNDR and SFDR (n = 6 devices).

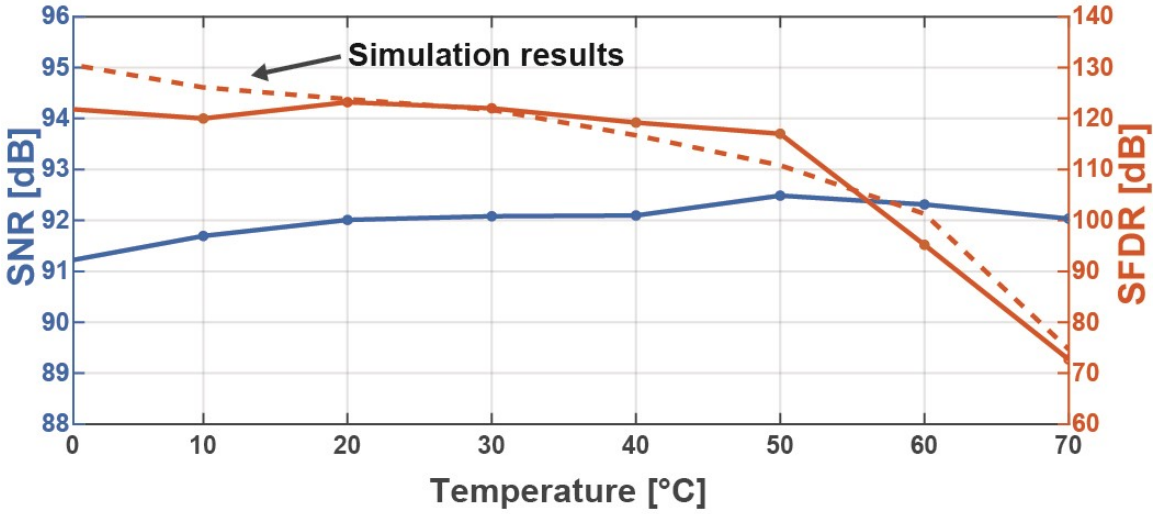

Figure 4.23. Measured SNR (blue) and SFDR (orange) as a function of temperature and simulated SFDR of chopping switch (orange dash).

to V_{DD} and the CMRR with a full-scale common-mode sinusoidal input stay above 80 dB from dc to 5 kHz. The SNDR was also measured as a function of the supply voltage from 0.7-1 V, as shown in Figure 4.21, where the performance varied by less than 1 dB between 0.75-0.95 V,

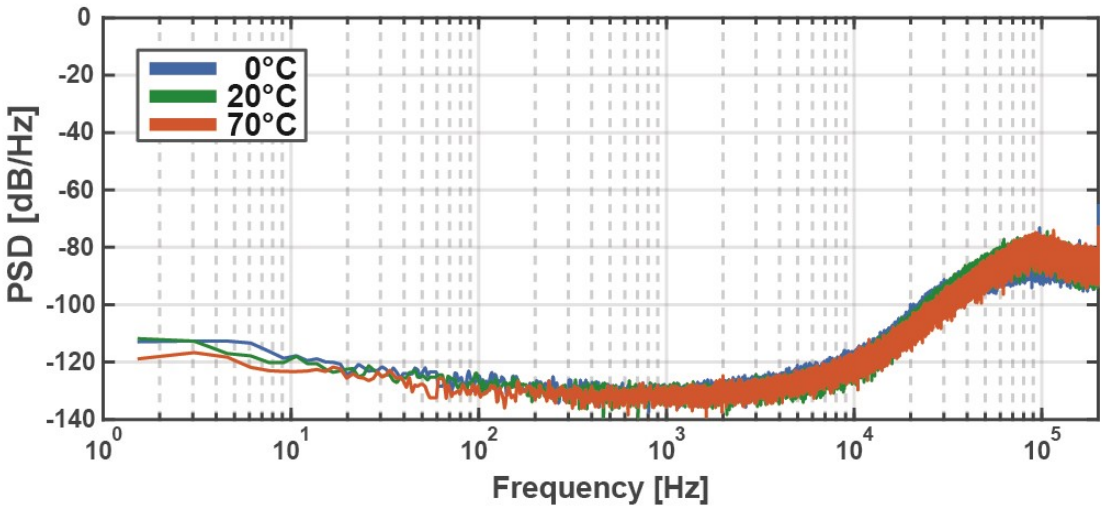

Figure 4.24. Measured output spectra with no input at 0, 20, and 70 °C.

demonstrating the ADC's robustness. The steep degradation at higher supply voltages is due to the CCO level-shifters failing and missing edges.

To assess the performance variation of the ADC across different die, the loop parameters were optimized for a specific device (Device #3), and then the same control bits were used on the 5 other devices. Figure 4.22 shows the measured SNDR and SFDR, where the average SNDR and SFDR were 90.7 dB and 119.5 dB, respectively. Optimizing the loop parameters separately for each device exhibited a 1 dB improvement in performance. This shows good performance across multiple devices and the loop's reliability across process variation and mismatch.

The ADC's temperature resilience was characterized across the commercial range (0 to 70 °C) by placing the device in a temperature chamber (Test Equity model 106) without any calibration or retuning of the loop parameters. As shown in Figure 4.23, the SNR varies negligibly, by only 1 dB, across the entire temperature range, demonstrating the robustness of the proposed design. The linearity stays above 117 dB for temperatures below 50 °C but degrades significantly at higher temperatures. This degradation with temperature was verified in simulation and found to be caused by leakage of the bootstrapped voltage circuit that drives the input chopping switches. The gate

Table 4.1 Performance summary and comparison to the state-of-the-art

	JSSC 2018 [40]	VLSI 2021 [54]	JSSC 2020 [69]	ISSCC 2022[81]	JSSC 2019 [10]	JSSC 2021 [39]	ISSCC 2021 [53]	**This Work**
Integration domain	Voltage	Voltage	Hybrid	Hybrid	Time	Time	Time	**Time**
Topology	3rd -ord.	3rd-ord.	2nd -ord.	2nd -ord.	1st -ord.	1st -ord.	2nd -ord.	**3rd -ord.**
Technology [nm]	65	28	65	65	40	65	65	**65**
Area [mm^2]	0.053	0.12	0.078	0.108	0.025	0.075	0.075	**0.1**
Supply (A/D) [V]	1.2	0.6	1	0.7	0.8 / 0.6	0.8	1.2 / 0.8	**0.8**
Power [µW]	4.5	33.6	6.5	5	4.5	1.68	5.8	**4.4**
DAC type	Capacitive	Resistive	Resistive	Capacitive	Capacitive	Capacitive	Capacitive	**Capacitive**
Input range [V_{pp}]	1.77	0.8	0.3	0.56	0.1	0.46	0.4	**1.8**
Sampling freq. [kHz]	400	12,800	1,280	2,560	2,500	64	200	**400**
BW [kHz]	5	40	10	10	10	0.5	1	**2.5**
CMRR [dB]	N/A	55	76	88	83	97	89	**80-93**
SNDR [dB]	93.5	83	80.4	85.1	78.5	94.2	92.3	**92.1**
DR [dB]	96.5	86.5	81	87.3	79	95.1	92.3	**92.1**
SFDR [dB]	101.4	94.2	92.2	97.1	91	128	110.3	**119.6 - 123**
FoM_{SNDR} [dB]	184	173.8	172.3	178.1	172	178.9	174.7	**179.6**

voltage drops below the maximum input voltage, which causes nonlinearity due to leakage through the chopping switches. The simulated chopping switch SFDR (all other blocks are ideal) is overlaid on the measured SFDR, exhibiting good agreement between simulation and measurement. This degradation could be avoided by increasing the bootstrapping capacitor to ensure a constant voltage, even at higher temperatures. Finally, to demonstrate the correct operation of the loop across temperature, spectra were recorded with shorted inputs at 0, 20, and 70 °C. As seen in Figure 4.24, the 3rd-order noise shaping is maintained, and the noise floor stays nearly constant across the temperature range.

4.4.3 Comparison to the State-of-the-Art

Table 4.1 compares recently published high-performance time- and voltage-domain ADCs. This work is the first 3rd-order VCO-only ADC enabling low supply operation and high DR. The DAC reference voltage was increased to 1.2 V to maximize the input range and allow a large differential swing of 1.8 V_{pp}. When operating the DAC at 0.8 V, the SNDR decreases by 2 dB, and the

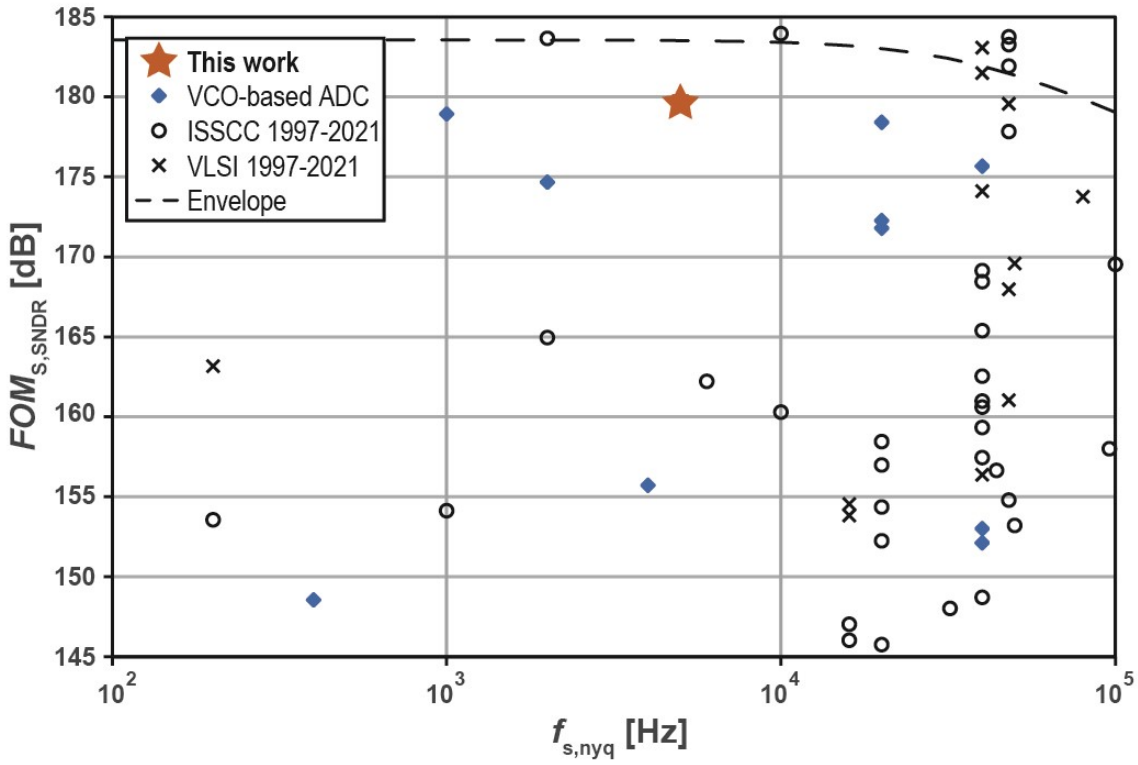

Figure 4.25. State-of-the-art landscape.

maximum differential input range decreases to 1.2 V_{pp}. The SNDR does not decrease by the expected 3.5 dB since the ADC noise is dominated by the CDAC mismatch, not the thermal noise. The reduced swing at the PVG due to the smaller reference voltage also allows for a more aggressive g_m/I_D in the first integrator. Due to the PVG-FF technique, extremely high linearity (>119.6 dB) and SNDR (92.1 dB) were achieved while consuming just 4.4 µW. As apparent from the table, the performance of the proposed ΔΣ ADC approaches that of voltage-domain ΔΣ modulators and achieves the highest Schreier FoM amongst time-domain architectures. Figure 4.25 plots the Schreier FoM ($FoM_{S,SNDR}$) of ADCs with bandwidths below 50 kHz as a function of their Nyquist frequency ($f_{s,nyq}$). The proposed ADC significantly advances the state-of-the-art.

4.5 Conclusion

This work demonstrates a feedforward technique that enables a highly efficient 3rd-order VCO-only ADC by linearizing the 1st integrator and removing the need for inner feedback DACs. The ADC structure is robust, maintaining performance over a wide temperature and supply voltage range. This PVG FF technique can be generalized to higher-order architectures or used with other open-loop integrators, such as a G_m-C, which would also benefit from the linearization and improved coefficient scaling offered by the PVG-FF technique. The proposed ADC is the first high linearity single loop 3rd-order ADC with time-only integrators, and it achieves a state-of-the-art 179.6 dB FoM among VCO-based ADCs and a 123 dB peak SFDR while operating from a low supply voltage. This work demonstrates that time-based modulators are competitive with standard voltage-domain architectures.

Acknowledgments

Chapter 4, in full, is a reprint of the material as it appears in C. Pochet and D. A. Hall, "A Pseudo-Virtual Ground Feedforwarding Technique Enabling Linearization and Higher Order Noise Shaping in VCO-Based ΔΣ Modulators," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 57, no. 12, pp. 3746-3756, Dec. 2022, doi: 10.1109/JSSC.2022.3202040. The dissertation author was the primary investigator and author of this paper.

CHAPTER 5 : SUMMARY

5.1 Summary of Dissertation

This dissertation presented several innovations at the circuit and system level to improve the efficiency and performance of time-based ADCs. These innovations allowed for the development of multiple VCO-based ADCs with >100 dB linearity and state-of-the-art performance. This section summarizes this thesis's findings and each prototype's key results.

Chapter 2 provides the reader with an introduction to the basics of time-based analog-to-digital converters. The advantages of time-based architectures over voltage-based ADCs, such as supply insensitivity and better scaling with process nodes, are highlighted, and the challenges of achieving high SNDR with time-based ADCs are demonstrated. A literature review was conducted, and different techniques described in the literature to address the limited linearity and noise-shaping order of the VCO-based ADCs were also presented.

In Chapter 3, a direct digitization AFE for ExG application is introduced. At the core of the AFE is a single loop 2^{nd}-order VCO-based ADC, which leverages a novel 1^{st}-order shaped TDC with a 3-state gated-inverted ring oscillator to achieve very high linearity while being very power-efficient. When integrating this ADC with an input-impedance booster, the proposed AFE achieves the very high input impedance required to interface with electrodes, low noise, and a high input range and linearity required to absorb motion/stimulation artifacts.

In Chapter 4, A technique to stabilize and linearize higher-order delta-sigma ADCs is presented and applied to a 3^{rd}-order VCO-based ADC. This technique, pseudo-virtual ground feedforwarding, reduces the signal's tonality in the 1st stage of the loop and allows the prototype ADC to achieve state-of-the-art power efficiency and linearity amongst time-based ADCs.

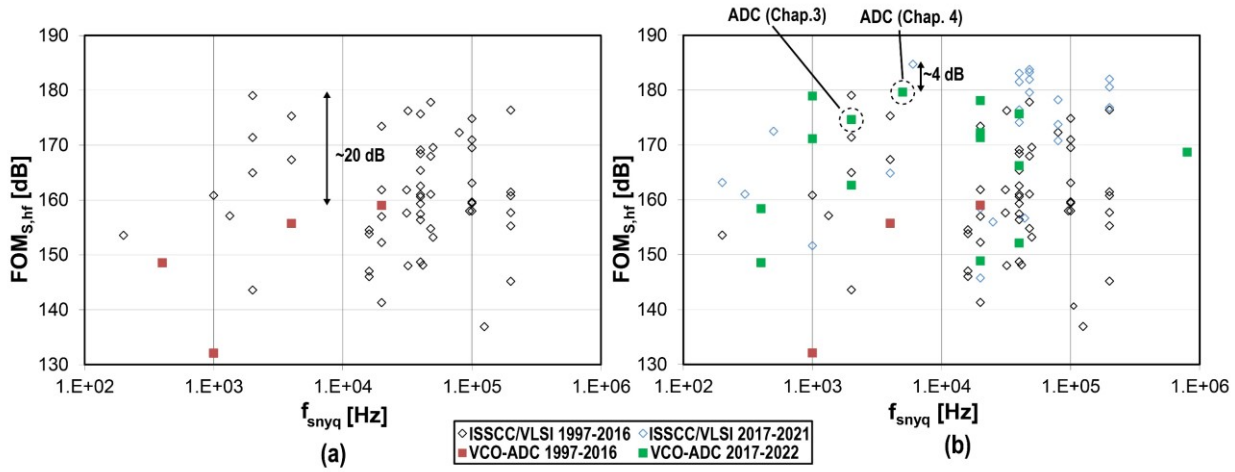

Figure 5.1. State-of-the-art landscape in (a) 2016 and (b) 2022

Overall, the techniques presented in this thesis were key to significantly improving the performance of time-based ADC, with the final prototype demonstrating that VCO-based ADCs could be designed to achieve performance on par with standard voltage domain architectures.

5.2 Evolution of the VCO-based ADCs throughout this work

To highlight the contributions of this thesis, it is interesting to observe the evolution of the performance of VCO-based ADCs during the time frame of this research project (2016-2022). To this end, we use the well-known Murmann ADC survey [82] as well as a collection of work published in highly regarded venues (*JSSC, TCASI, TCASII*) to map the state of ADC research for sub-MegaHertz Nyquist frequency throughout the years. As illustrated in Figure 5.1(a), the VCO-based ADCs in 2016, while possessing interesting features of time-based architectures, were far from equaling the performance of standard voltage domain architecture with over 10× higher power dissipation for similar noise/dynamic range performance. Figure 5.1(b) is updated with designs published between 2017 and 2022 , and the works presented in this thesis are highlighted. Two remarkable observations can be made: first, the number of VCO-based ADCs has greatly increased with over 15 new time-based designs. Second, the gap between the best-in-class VCO-

based ADC and the best-in-class voltage domain ADC has significantly shrunk to < 4 dB. These observations show the tremendous increase in interest in time-based ADC by the academic community and the effort by researchers to improve the linearity and power efficiency of time-based ADCs.

5.3 Areas of future work

The contributions made in this thesis to higher-order VCO-based ADCs can be expanded in several ways. The ADCs presented in this dissertation have been targeted at sensor applications with bandwidth limited below 10 kHz. While this is sufficient for most sensor applications, there is also interest in quantizing signals with wider bandwidth (>100 kHz) for a wide range of applications. As the bandwidth is increased, the clock frequency of the ADCs must be increased, which reduces the settling time for the inner nodes of the quantizer and requires longer relative resampling times (*e.g.,* on the order of $0.5T_s$). These longer resampling times will require excess loop delay (ELD) compensation techniques to be developed and added to the loop through additional feedback/feedforward paths. Implementing these ELD paths in VCO-based ADC is more complex than in standard voltage domain architecture due to the integrator and the quantizer being merged and thus not having direct access to the quantizer needed for ELD compensation [83]. Investigating ELD techniques that could be adapted to VCO-based ADCs would be interesting.

Another potential area for future work could be to expand on the PVG-FF technique and add resonance paths to achieve more efficient noise-shaping by moving the poles of the NTF poles away from dc. This could further improve the ADC's efficiency by improving the noise shaping. It could be interesting to explore the use of time domain feedforwarding and feedback using voltage-controlled delay cells and digital-to-time converters, which have also seen significant

development in the past decades. These time-based blocks could add delay in the loop and further highlight the need for research in time-based delay compensation techniques suggested in the previous paragraph.

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