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Process Development and Optimization of Via Laser Drilling and Cu Electroplating for Through-wafer Vias (TWVs) in Silicon-Interconnect Fabric (Si-IF)

A thesis submitted in partial satisfaction of the

requirements for the degree Master of Science

in Materials Science and Engineering

by

Dharani Jaya Yakkaluru

2023

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2023

ABSTRACT OF THE THESIS

Process Development and Optimization of Via Laser

Drilling and Cu Electroplating for Through-wafer Vias (TWVs)

in Silicon-Interconnect Fabric (Si-IF)

by

Dharani Jaya Yakkaluru

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2023

Professor Subramanian Srikanteswara Iyer, Chair

Through Silicon vias (TSVs) have become the basis for 3D integration packaging systems such as Samsung's High-Bandwidth Memory (HBM) and 3D Hybrid Cube (H-Cube) DRAM, TSMC's Chip on Wafer on Substrate(CoWoS) packaging, and others. They enable power delivery, signal transmission, and heat dissipation by passing through several chips stacked on top of each other. They also serve a similar purpose in wafer scale systems (WSS). As an aim to replace PCB with

Silicon, a WSS known as Silicon Interconnect Fabric (Si-IF) is being developed for heterogeneous integration, high power applications, and high interconnect density. For power delivery, the interconnections that pass through the wafer are fabricated named as Through wafer Vias (TWVs).

TWVs involve a complex fabrication process that includes etching the via, deposition of various layers like seed and barrier layer, followed by electroplating of copper. Challenges do arise in etching large diameters of vias on a wafer, choosing the appropriate geometry for uniform seed layer deposition by Denton and Ulvac sputter machines, and achieving defect-free electroplating.

In this thesis, we first used the laser drilling process to etch the via, as it provides flexibility with the via geometry, a mask-free process, and lower fabrication costs than other processes. We optimized the laser drilling parameters and later sputtered and electroplated the vias with Copper. Finally, we did a comparative study between two sputter machines for achieving a good quality seed layer and also proposed the optimized laser parameters that helps in obtaining defect-free plating

The thesis of Dharani Jaya Yakkaluru is approved.

Aaswath Pattabhi Raman

Jaime Marian

Subramanian Srikanteswara Iyer, Committee Chair

University of California, Los Angeles

2023

Dedicated to my parents

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Chapter 1 Introduction

3D packaging has become one of the promising solutions to improve the performance of the device. Interconnects play an important role in signal and power delivery of these packages. Wire bond and flip chip technologies have limited the size reduction of 3D packages, leading to the development of Through Silicon Vias (TSVs). TSVs are vertical interconnections that pass through the interposer or die stacked upon one another. They were first proposed by William Shockley from Bell Labs in his patent "Semiconductive Wafer and Method of Making the Same" and later developed by IBM [1]. In addition to their advantages for size reduction, the characteristics of TSVs also make them the heart of 3D packaging, such as short electric path for less signal and power loss, lightweight [2], enhanced functionality with increased number of connections per unit area, and better thermal management, making them imperative for Chip Stack MCM, DRAM, Heterogeneous Integration systems, etc.

Depending on fabrication requirements and design, TSVs are categorized in three ways: via-first, via-middle, and via-last. Via-first involves manufacturing TSVs before any front-end process of the device takes place. In this category, the TSVs need to undergo many thermal processing steps, which can incur material usage

based limitations for TSVs for achieving better properties. Via-middle includes fabricating TSVs after the front-end process but prior to the back-end, where metal routing is performed. Via-last involves fabrication post front-end and back-end processes [4]. Via-last is economical and has a lower interconnect density. For the Si-IF, we will be using the via-last procedure [5], as our main focus is power delivery, and it also gives flexibility with fabrication as it does not affect the succeeding processes. Furthermore, Si-IF is a Wafer Scale System; the interconnects should pass through a wafer and provide a similar purpose as TSVs for which we developed TWVs.

1.1 Differences between TSVs and TWVs

TSVs are the interconnects that pass through a stack of dies or chips. The purpose of these can be signal transmission or power delivery [6]. TWVs are the interconnects that pass through a single wafer and the main purpose of these are to deliver power. These are blind vias which will be thinned to make through vias. *Figure 1.1 a* and *b* shows TWVs and TSVs.

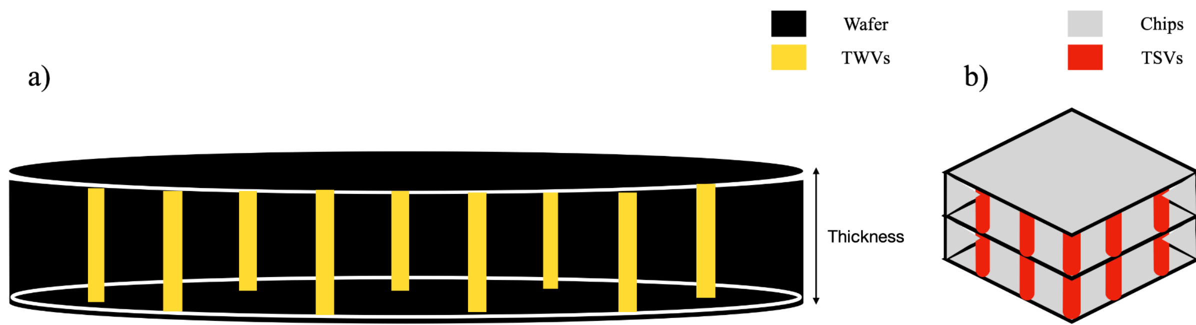


Figure 1.1 a) 3D representation of TWVs passing through a Wafer b) 3D representation of TSVs passing through a chip

1.2 Fabrication process

The general steps involved in the fabrication of the TSVs/TWVs as shown in *Figure 1.2* and classified as follows:

1.2.1 Via Etching:

Etching is used to create vias in a wafer. There are different methods for etching, which can be categorized as either wet etching or dry etching. Wet etching method includes KOH-wet etching and photo-assisted electrochemical etching, while dry etching includes Deep Reactive Ion Etching (DRIE) and laser drilling.

KOH-wet etching is an anisotropic etching process that involves reacting silicon with KOH liquid to remove required areas of the material. Other etchants like HMA and TMAH can also be used. Photo-assisted electrochemical etching involves using

ultraviolet light along with an electrochemical process. Electrochemical process oxidizes and removes the silicon and light helps in accelerating this process [7].

Incase of dry etching process: the DRIE process uses SF_6 reactive gas to etch the silicon, the chemical nature of the gas reacts with the material and pressure of the gas removes reacted silicon to create a via. C_4F_8 is also used periodically to protect the sidewall profile. In wet etching and DRIE process, a mask is used to drill the vias at specific regions. The other dry etching process is laser drilling which involves using a laser to drill the vias. The heat generated by the laser melts the material and evaporates the liquid, or the laser can directly break atomic bonds. It requires a layout design instead of a mask to drill vias at specific regions [7].

Different etching methods can produce different etch side-wall profiles. For example, dry etching processes can create deep, vertical vias, while KOH-wet etching produces shallow, inverted pyramid-shaped vias, and photo-assisted electrochemical etching creates deep grooves.

1.2.2 Deposition of thin films:

After etching the via, liners like SiO_2 or SiN or Al_2O_3 are deposited throughout the via for the purpose of electrical insulation from the material surrounding the via. SiO_2 can be deposited by using thermal oxidation or Chemical Vapour Deposition (CVD). SiN by CVD and Al_2O_3 can be deposited by Atomic Layer Deposition (ALD). After the insulating layer is deposited, TiN or TaN is deposited as a barrier layer. This layer avoids diffusion of Cu into the Si or SiO_2. These layers are followed by seed layer deposition which provides a conductive path for Cu filling through electroplating. Al,Ti, Cu, Pt and some other metals can be used. However, using Cu has an advantage of avoiding intermetallic formation at high temperatures. Seed layer is generally deposited by the sputtering process. All these 3 layers should be conformal and must have good adhesion with each other [3].

1.2.3 Cu filling:

Cu has been used for interconnections from the past generations due to its low resistivity. In TSVs/TWVs, Cu is filled using electroplating, where chemical reactions undergo and Cu gets deposited on the material with the passage of current. The basic setup consists of Cu or Pt as anode, the TSV/TWV-etched silicon

wafer as the cathode, copper sulfate along with additives as an electrolyte, and a power supply.

Once the connections are made, an oxidation reaction occurs at the anode, leading to the release of electrons. These electrons will be taken up by the cathode to reduce the Cu^{+2} ions present in the electrolyte. The reduction reaction reduces Cu^{+2} ions into Cu metal, which gets deposited on the cathode. In case of Cu anode, the anode gets consumed during the oxidation reaction providing Cu^{+2} ions into the solution, maintaining the bath concentration.

The oxidation and reduction reactions are as follows:

$$Cu \rightarrow Cu^{+2} + 2e^{-} \qquad \text{(Anode)}$$

$$Cu^{+2} + 2e^{-} \rightarrow Cu \qquad \text{(Cathode)}$$

Electrolyte also consists of other additives such as brighteners, carriers and levelers to modify the reaction dynamics. Brighteners are organic compounds that accelerate the reaction rate. They aid in bottom-up electroplating because they are smaller than the carrier molecules, leading to faster diffusion into the via and enhancing the reaction rate at the bottom. Carriers are polymer molecules added to suppress the reaction rate at the via openings. Their heavy weight and small diffusion rates makes them settle at the via openings. Levelers are used for uniform deposition of

the Cu inside the Via which helps in avoiding the formation of voids and protrusions [9].

In addition, HCl is added to assist in the bottom-up filling of the via by accelerating the reaction of copper. However, at high concentrations of chloride ions, an inhibiting effect can occur due to higher localized concentrations [9].

There are three different ways that copper can be filled into the via: 1) sub-conformal, 2) conformal, and 3) super-conformal. Sub-conformal filling occurs when sidewall deposition dominates over deposition on the bottom side, which leads to a void in the via. This type of filling mostly occurs at high current densities. Conformal filling occurs when uniform deposition occurs at the sidewall and bottom of the via. This filling leads to the formation of a seam in the via and generally occurs at low current densities. Super-conformal filling is the desired type of filling that leads to a defect-free via. This occurs when deposition at the bottom of the via dominates sidewall deposition. This type of filling can be achieved at moderate current densities, optimized additive additions, and good seed layer quality. *Figure 1.3* shows different types of filling mechanisms[9].

1.2.4 Thinning:

Wafer thinning is performed to open the blind via from the backside to make it a through-via. The wafer is attached to a carrier wafer for support and grinding is done to thin the wafer. Grinding leads to a rough surface of the wafer, hence it is better to perform until the sample reaches a specific thickness; afterward, mechanical polishing is done for achieving smooth surfaces [3].

In this current work, we have developed TWVs using the laser drilling process for etching vias, followed by seed layer deposition and Cu electroplating. The laser drilling process gives us the flexibility to obtain a large range of via diameters, which will be useful for power delivery in Si-IF. Additionally, larger diameters enhance the sputtering capabilities. We optimized the laser drilling parameters and compared two sputtering machines to obtain high-quality vias, which help in achieving defect-free Cu-filled via.

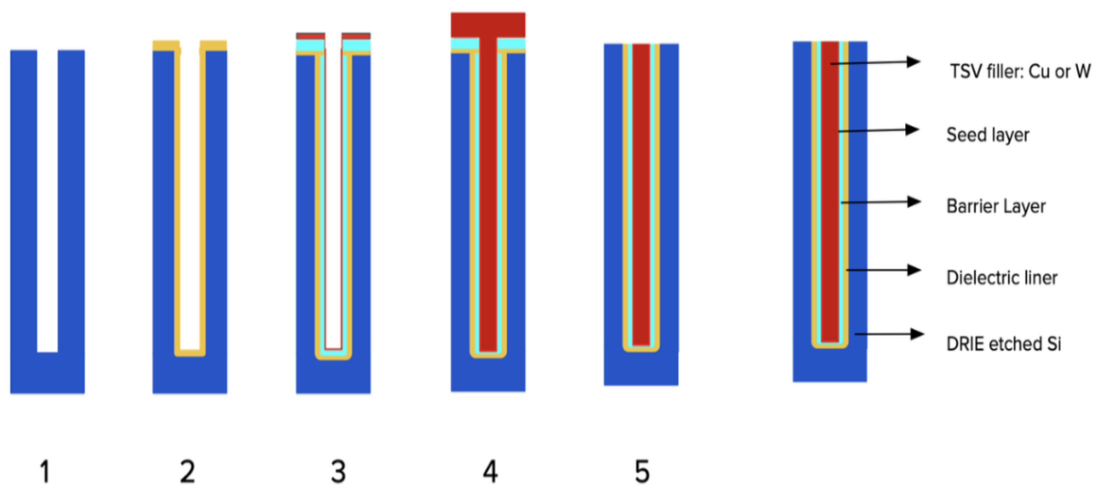


Figure 1.2 Fabrication process for TWVs 1)Via Etching 2) Dielectric liner deposition 3) Barrier and seed layer deposition 4) Cu-filling 5) Thinning [8]

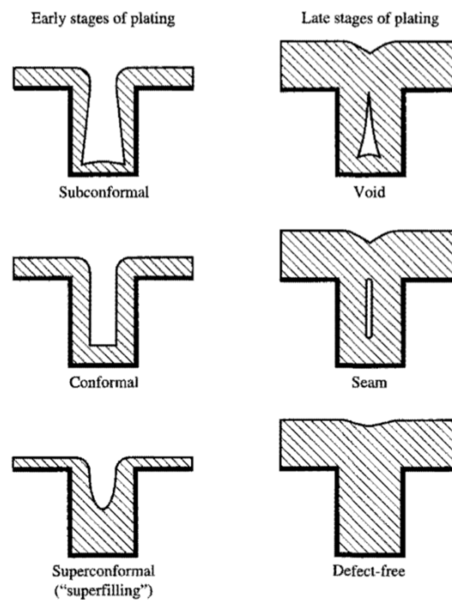


Figure 1.3 Different filling mechanisms of Cu [9]

Chapter 2 Laser Drilling

As discussed earlier, laser drilling can be used to etch a via into the wafer. Before understanding the influence of the laser parameters on the depth of the via and it's profile, let us see how the laser drilling process works:

2.1 Working mechanism of the laser drilling:

A laser beam is directed on to a wafer with the help of a focusing lens. As it purges the wafer or substrate, the material rapidly heats up, leading to melting, and finally evaporating the material for easy removal. The material is removed by the ablation process, where the laser spot on the wafer is divided into four regions: peak energy, ablation, melting, and irradiation, as shown in *Figure 2.1*. The energy follows a Gaussian profile, where the peak energy leaves a crater formation at the center. The surrounding region of the peak energy leads to the evaporation of the material, i.e., the ablation area. As the energy lowers, the amount of heat is just sufficient for melting the material known as melting area, and this region is surrounded by the irradiated layer. The vaporized and melted zones are removed with the help of a gas. [10]

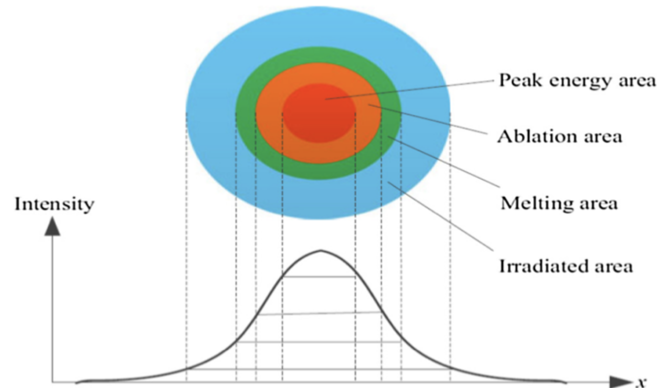


Figure 2.1 Material removal mechanism of laser drilling process [10]

There are two different techniques for laser drilling via: static drilling and dynamic drilling. Static drilling involves keeping the laser beam and work piece stationary. The laser beam can either be a single pulse or a finite number of pulses. The latter is called percussion drilling. Dynamic drilling, on the other hand, involves movement of either the beam or the work piece, and is classified into Trepan and Helical drilling. In Trepan, the laser beam moves in a spiral fashion starting from the center of the via. In helical drilling the beam follows a helical path and the beam rotates around its axis with respect to the work piece [11]. *Figure 2.2* shows the 4 types of techniques.

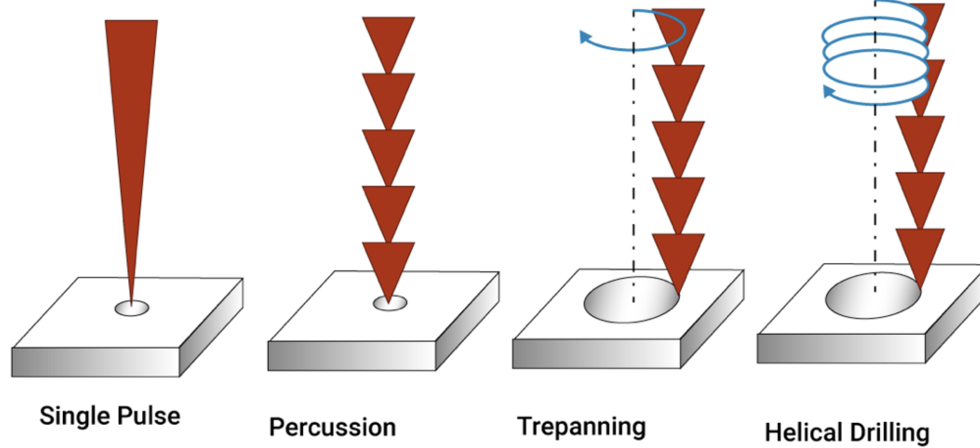


Figure 2.2 Different types of laser drilling techniques [12]

Laser drilling is a simple process that doesn't involve usage of the mask or any chemicals. The less complicated nature of the process decreases the fabrication costs compared to other etching processes. Additionally, it provides flexibility to achieve various ranges of diameters. However, laser drilling also has a few demerits namely the heat generated during the process can damage the material surrounding the via, creating a Heat Affected Zone (HAZ). Moreover, if the energy used is too high, it may result in microcracks. Another drawback is the recast layer that forms around the via, which can negatively impact subsequent processing steps. Finally, the accuracy of the via diameter is often poor due to non-uniform heat distribution.

2.2 Equipment Characteristics:

In our work, we have utilized the LPKF U4 proto laser tool to drill silicon vias with diameters ranging from 100-600 μm. The tool uses a UV laser with a wavelength of 355 nm, and the frequency of pulses as 50 kHz, with a laser spot size of 15 μm [13]. The penetration depth of the light falls within the range of 10-100 nm. During the drilling process, N_2 gas is used for the removal of material in the via. All the vias are drilled in unplated and cut inside modes. *Figure 2.3* shows the U4 proto laser.

Figure 2.3 LPKF U4 Proto Laser

We used the trepanning method to drill the vias, which produces better quality vias than static drilling techniques. The maximum beam diameter achieved by the proto

laser tool is 150 µm, limiting the usage of static drilling for diameters greater than 150 µm because both workpiece and the beam are stationary.

To minimize the disadvantages of laser drilling and to obtain a good quality via and desired aspect ratio, we varied different parameters of the laser beam. We also varied the geometry parameters to obtain a defect-free electroplating of the vias. The parameter variation is shown in *Figure 2.4*. The scan speed determines how fast the laser beam travels around the via, while power indicates the peak energy of the beam. Repetitions (reps) refer to the number of times the laser travels along a particular path. The overlap percentage indicates how much the current path of the laser overlaps the previous path . For instance, a 15% overlap means that the laser covers only 15% of the previous path. Defocusing the laser makes the laser beam less focused to avoid trepanning, but we obtained through vias even at low powers therefore, we only considered the focused laser with z-offset 150 µm for the rest of the experiments. Scan speed, repetitions, peak powers and overlap percentages are varied to understand their influence on depth, via circularity, via taper, via profile, and the quality of plating. The study investigates these parameters for different diameters ranging from 100 µm to 600 µm.

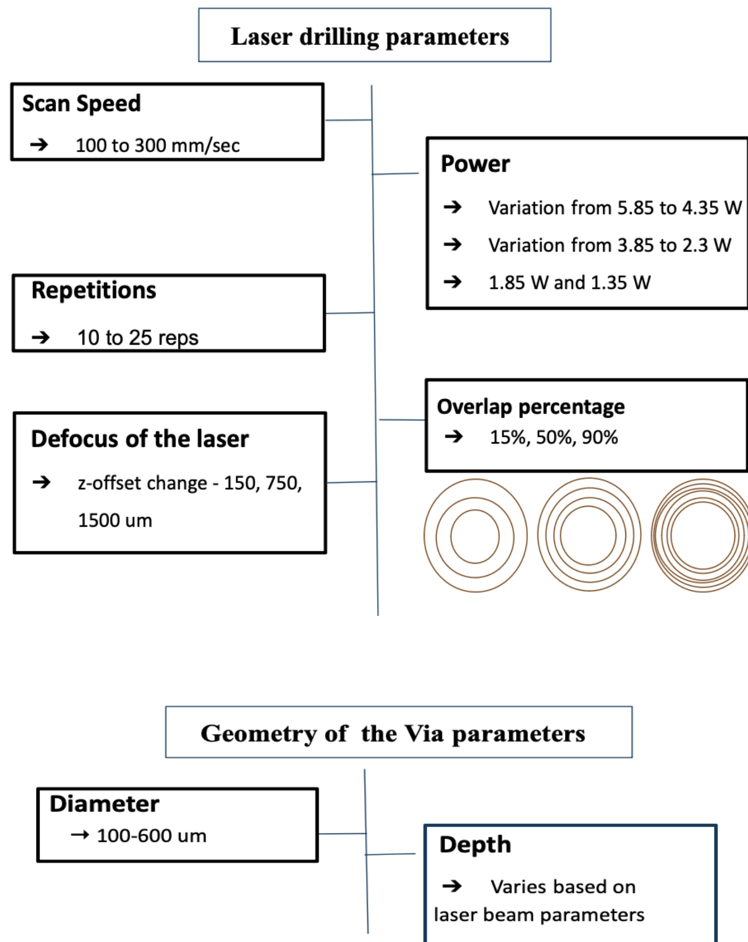


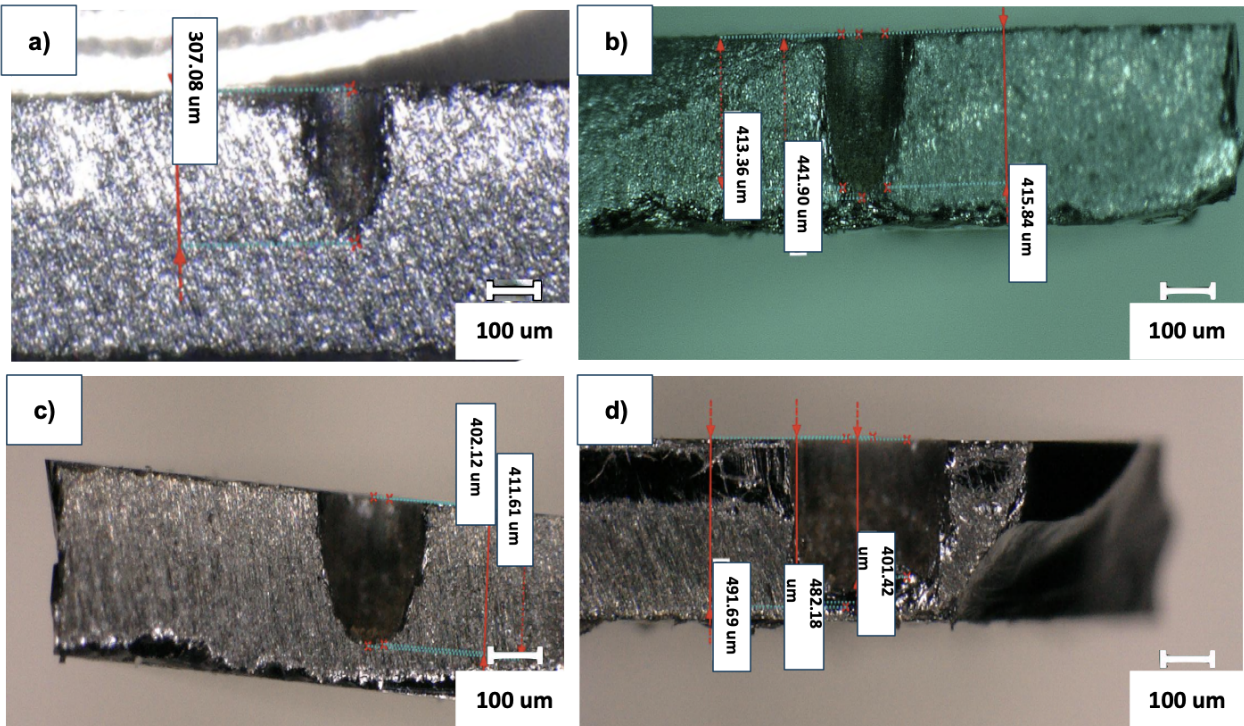
Figure 2.4 : Parameter variation of laser beam and via

2.3 Influence of Peak Power on via parameters:

2.3.1 Depth:

Vias were drilled for different peak powers by keeping the other parameters constant and as follows 25 repetitions, 150 mm/sec scan speed, 15% overlap percentage, and 150 um Z-offset focused laser. The maximum power was varied

from 5.85 to 1.35 W. Cross-sections were taken at the center of the vias with diameters ranging from 200-600 µm drilled at 5.85 W, 4.85 W, and 4.35 W powers, as shown in *Figure 2.5*. The cross-sections provided the profile and depth of the via. Optical profilometry was used to estimate the depth of vias with diameters ranging from 200-500 µm for the powers 3.85 W, 3.3 W, 2.85 W and 2.3 W. Optical profilometry measurements for 2.3 W power samples are shown in *Figure 2.6*.



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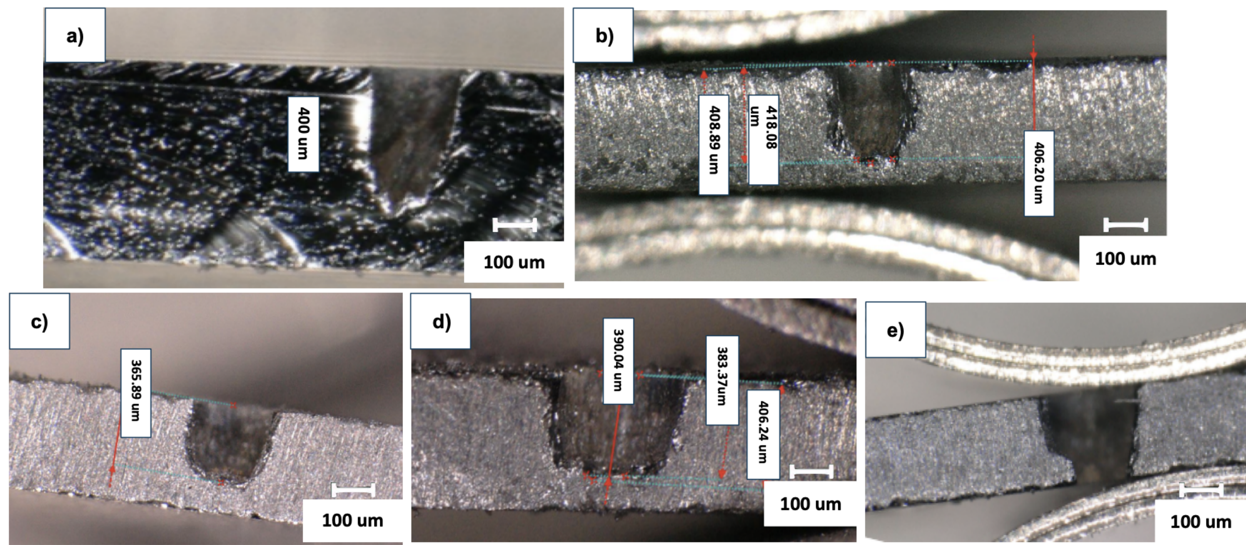

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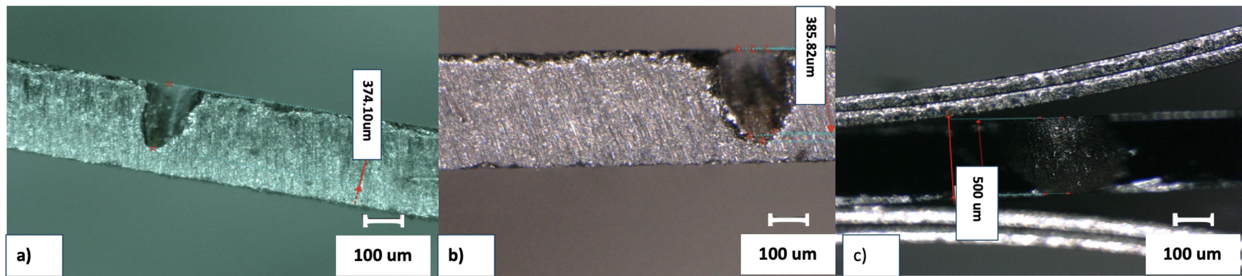


(3)

Figure 2.5 (1) Cross-section images at peak power 4.35 W, 25 reps, 150 mm/sec, 15% overlap a) 200 um b) 300 um c) 400 um d) 600 um (2) Cross-section images at peak power 4.85 W, 25 reps, 150 mm/sec, 15% overlap a) 200 um b) 300 um c) 400 um d) 500 um e) 600 um (3) Cross-section images at peak power 5.85 W, 25 reps, 150 mm/sec, 15% overlap a) 100 um b) 200 um c) 300 um

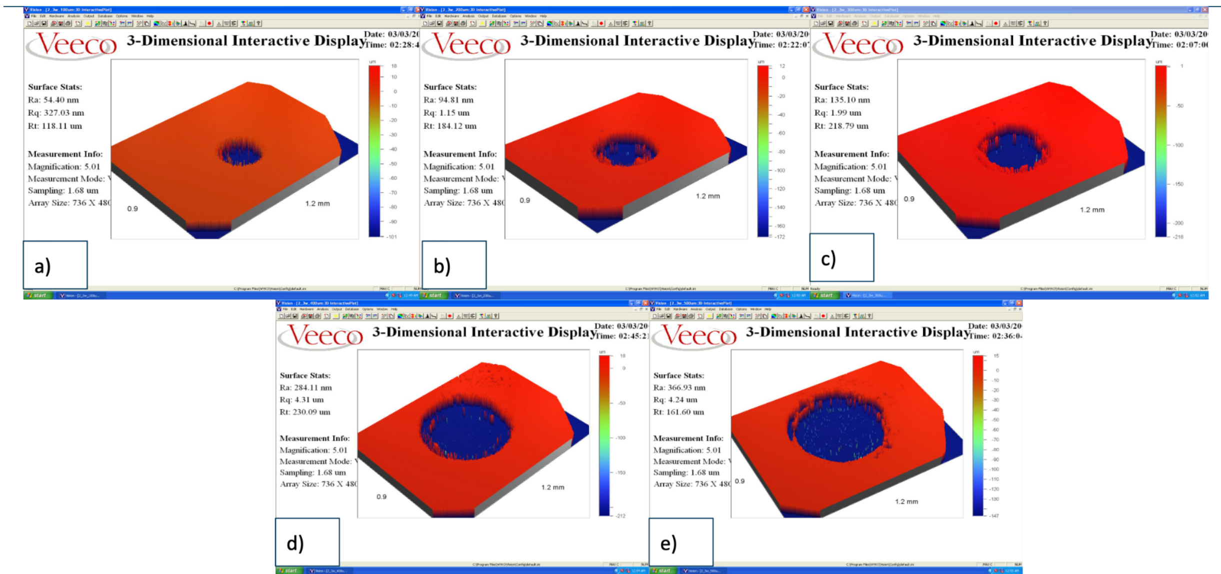


Figure 2.6: Depth measurements for Power 2.3 W, 25 reps, 150 mm/s, 50% overlap a) 100 um b) 200 um c) 300 um d) 400 um e) 500 um

For the same peak power, it has been observed that the depth increases until it reaches 300 or 400 µm diameter, after which it starts decreasing. This could be due to the difference in the exposed area for the laser. For understanding, let's consider a spot in the whole travel path of the laser and the laser reaches that spot in each turn until the given number of reps. In case of smaller exposure areas, such as 100, 200, and 300 µm, the laser reaches the particular spot very quickly as the travel path is less, leading to more melting of the material at that spot. In case of larger diameters, the travel path is long and by the time the laser reaches the spot, it would have solidified, leading to lower depths. This variation in heat distribution between

smaller and larger diameters, will change the trend of the curve between diameter and depth at constant power. This can be clearly seen in *Figure 2.7*.

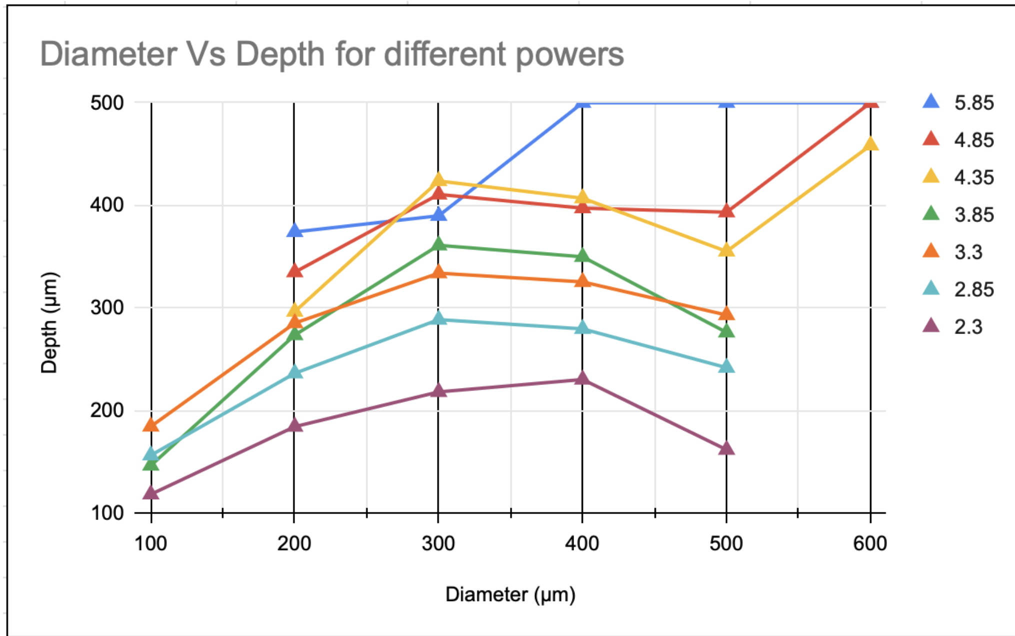
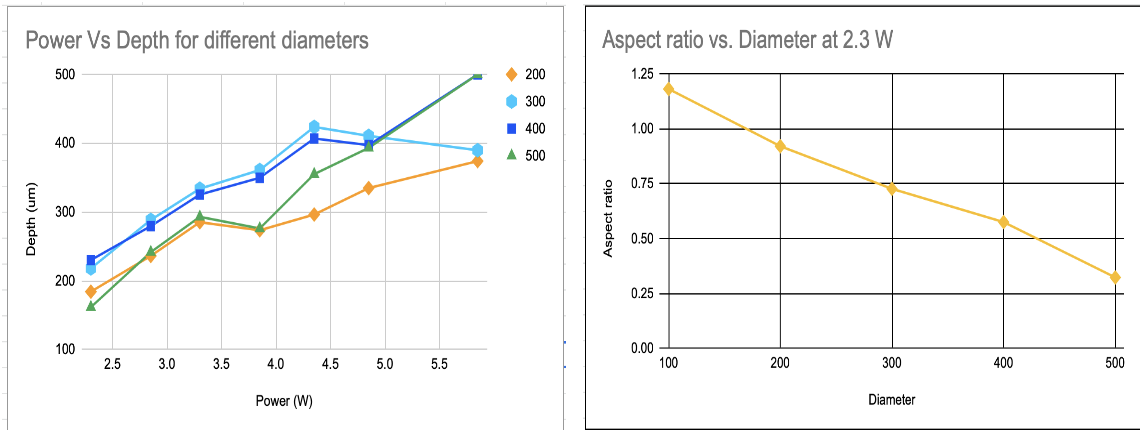
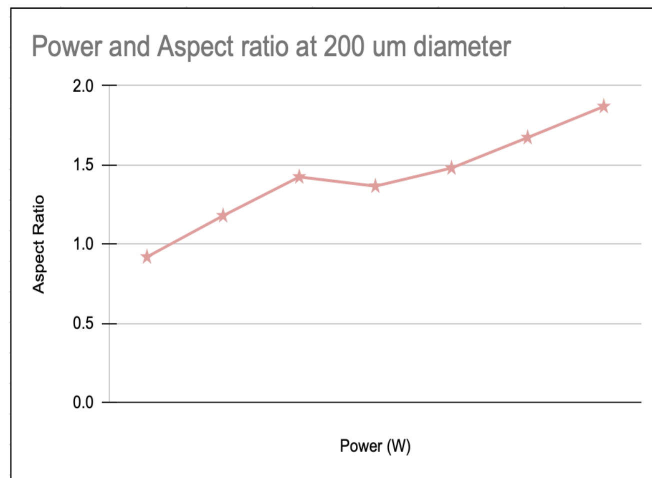


Figure 2.7 Depth variation at different diameters for different powers at 25 reps, 150 mm/s and 15% overlap

From *Figure 2.8(a)* we can observe that as the peak power increases, the depth also increases for a constant diameter, due to the increase in energy of the beam with power. The aspect ratio (depth/diameter) decreases with increasing diameter at constant power as in *Figure 2.8(b).* Moreover, when the diameter remains constant, the aspect ratio increases with power (*Figure 2.8 (c)*). It ranged from 0.8 to 1.87. Since the desired aspect ratio for TWVs should be below 1, we opted to use lower powers.



(a) (b)



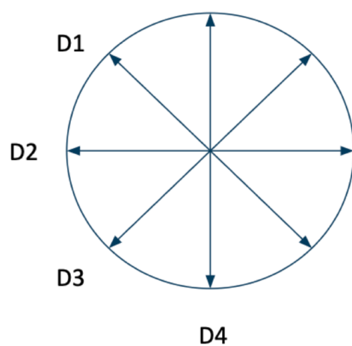
(c)

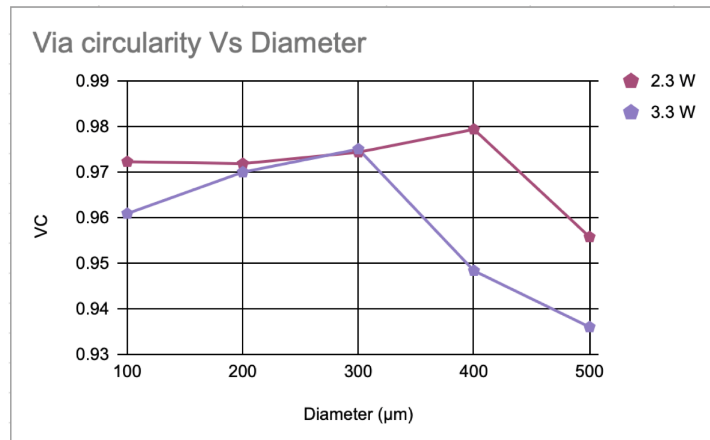
Figure 2.8 (a) Depth variation with power for different diameters at 25 reps, 150 mm/s and 15% overlap (b) Aspect ratio variation with diameter at 2.3 W, at 25 reps, 150 mm/s and 15% overlap (C) Aspect ratio varying with power for 200 um diameter via at 25 reps, 150 mm/s and 15% overlap.

2.3.2 Via circularity:

Via circularity gives the degree of the roundness of the via. Due to the thermal effects of the LASER , the via won't be perfectly circular. This can be measured as

via circularity (VC) = D_{min} / D_{max} [11]





a) b)

Figure 2.9 (a) Via circularity (VC) measurements (b) Variation of VC with diameters for different powers at 25 reps, 150 mm/s and 15% overlap, 150 µm Z-offset with focused beam.

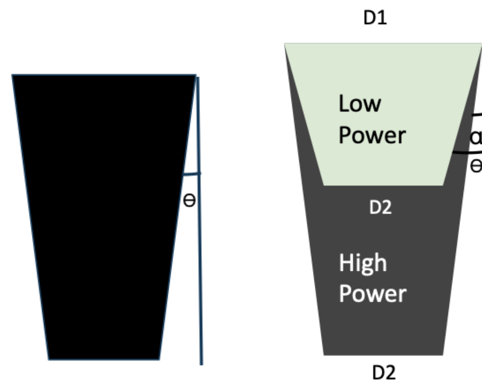
Diameters are measured at different points, as shown in *Figure 2.9 (a)*, and the minimum and maximum values were taken to calculate the VC. *Figure 2.9 (b)* shows the variation of via circularity for peak powers 2.3 W and 3.3 W. We can observe that the accuracy of VC is almost the same until 300 µm, and then decreases around 400 µm and 500 µm. This could be due to the larger interaction

time of the melt zones at the edges, leading to the erosion of material, affecting circularity [14]. Additionally, for higher power, the error is more than the lower powers. This may be due to thermal effects caused by the high energy input of high peak powers [15].

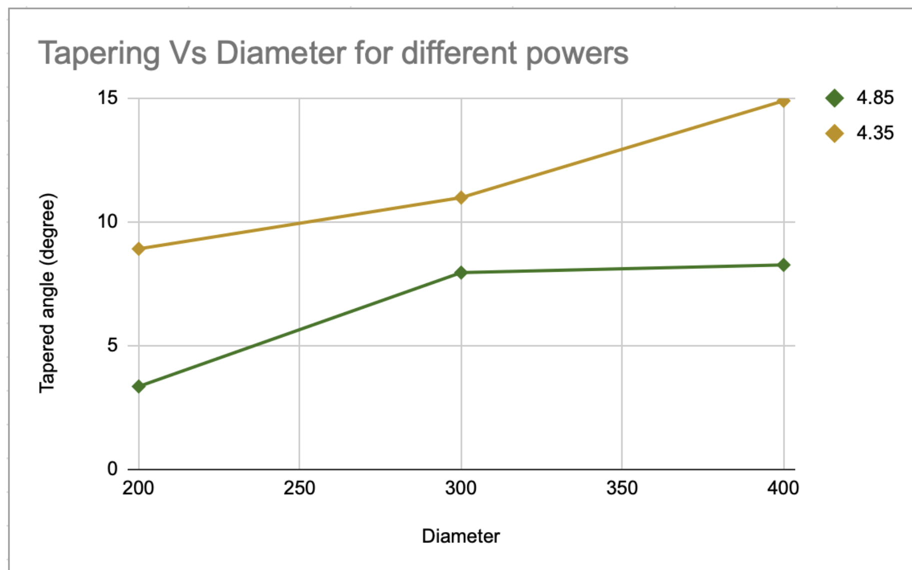
2.3.3 Via taper:

Via taper is the angle that sidewall makes with the perpendicular as in *Figure 2.10(a)* [16]. The divergence and convergence of the laser results in non uniform drilling while moving down the depth causing taperness [11].

It can be observed from *Figure 2.10 (c)* that as the diameter increases, the tapered angle also increases. However, it is not necessary for all diameters to follow this trend as variations in heat distribution can lead to barrelling of the via. Additionally, it can be seen that as power decreases, the tapered angle increases. This can be mathematically proven through *Figure 2.10 (b)*, for the same diameters D1 and D2, the tapering decreases with increase in the depth ($\alpha < \theta$) The same trend was also observed in A.K Nath et al. [17]. Theoretically, higher power should result in more material removal, leading to a more uniform profile giving less taper angle.



(a) (b)



(c)

Figure 2.10 (a) Measurement of tapering (b) Influence of powers on taper angle (c) Tapering variation with diameter for different powers at 25 reps, 150 mm/s and 15% overlap.

2.4 Influence of repetitions on Via parameters

2.4.1 Depth:

The variation of repetitions is performed for 200-500 µm diameter drilled at 2.3 W, 150 mm/sec scan speed, and 15% overlap. As the number of repetitions increases, the amount of heat generated increases, leading to more material removal through vaporization and melting. This leads to an increase in depth, as observed by Hermann Uchtmann et al. [20], which can also be seen in *Figure 2.11*. For the same number of repetitions, the depth increases with diameter. However, at 500 µm, the depth decreases compared to the other diameters due to differences in heat distribution, similar to that observed with peak power variations.

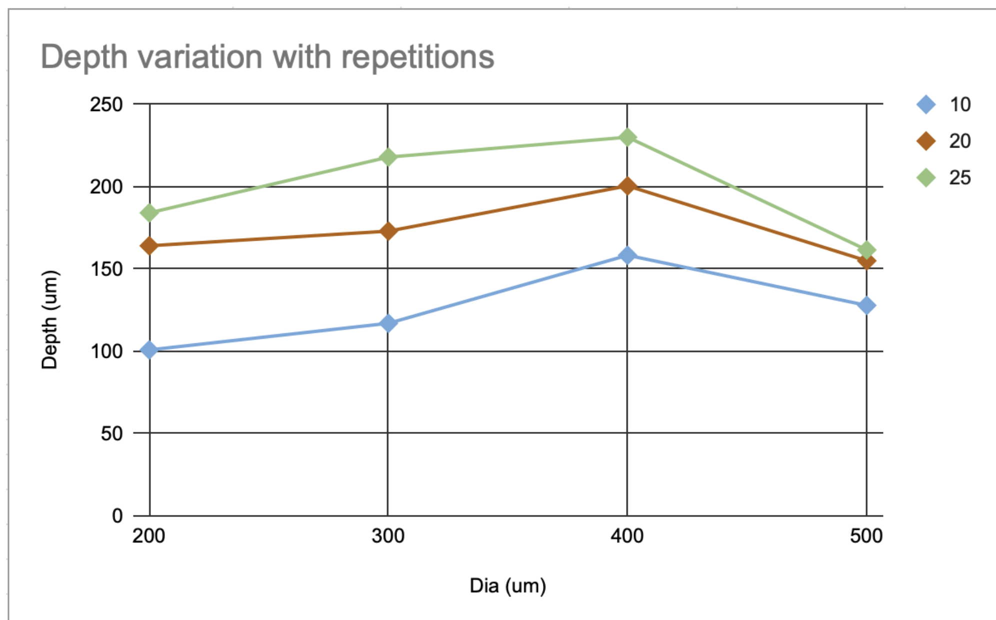


Figure 2.11 Depth Vs diameters for different repetitions at 2.3 W, 150mm/sec and 15% Overlap

2.4.2 Via circularity:

As the number of repetitions increases, the laser beam moves in the same path for a greater number of times, leading to the proper removal of material at points that were not drilled correctly in the previous path. This results in an increase in the precision of circularity with repetitions. This holds true until a certain number of repetitions, after that a further increase in repetitions will lead to a decrease in VC due to the damage of the material caused by thermal effects. This trend was observed by Sun et al. [19].

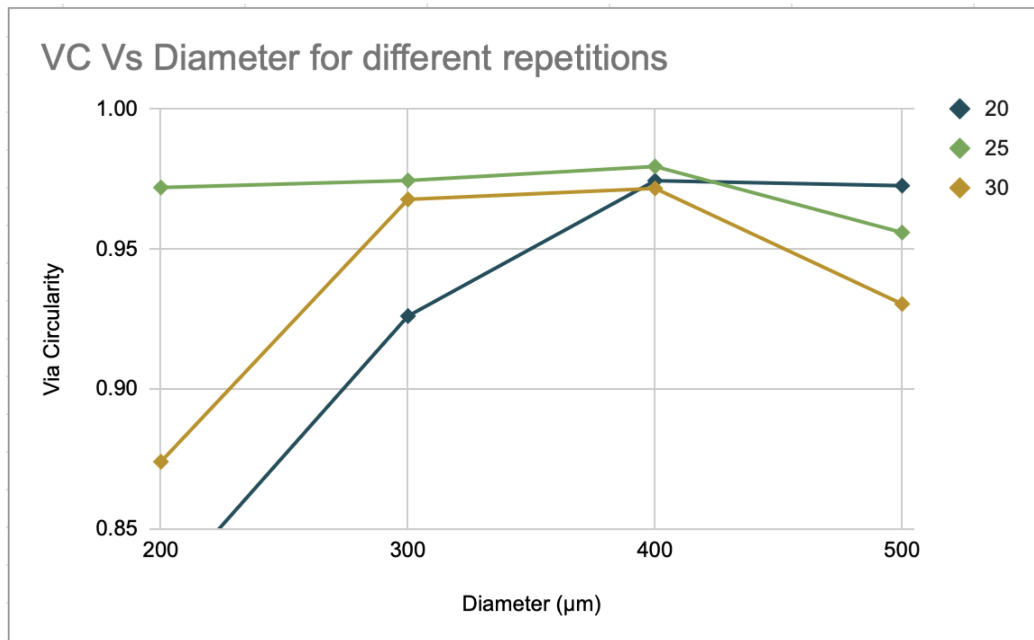


Figure 2.12 VC Vs Diameter for different Repetitions at 2.3 W, 150mm/sec and 15% Overlap

In *Figure 2.12*, we can see that for most diameters, VC is higher for 25 and 30 repetitions compared to 20 repetitions. If the number of repetitions exceeds 25, VC decreases due to the irregularities caused by thermal effects; this can be seen in the case of 30 reps. Below 25 repetitions, the laser does not provide sufficient energy to drill the via properly leading to poor VC; this can be seen in the case of 20 reps. Therefore, at a power of 2.3W, a scan speed of 150 mm/sec and an overlap of 15%, 25 repetitions would be the optimal number to achieve a good rounded via.

2.4.3 Via Taper:

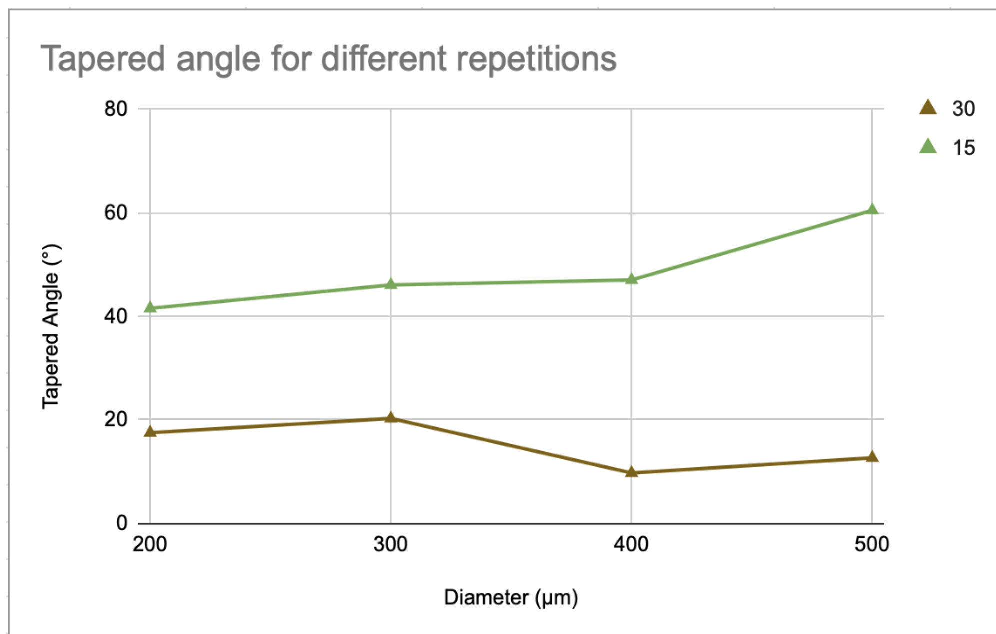


Figure 2.13 Tapered angle Vs Diameter for different Repetitions at 2.3 W, 150mm/sec and 15% Overlap

From *Figure 2.13* we can see that there is no clear trend in the tapered angle as the diameter varies. But the variation can be observed with repetitions, with increase in repetitions, the tapered angle decreases because more material is removed and the profile tends to become more uniform, reducing the amount of tapering, similar to what happens at high peak powers.

2.5 Influence of Scan Speed on Via parameters

2.5.1 Depth

Higher scan speeds are generally expected to decrease the depth. As the laser beam moves fast, it doesn't have enough time to distribute the necessary amount of heat required to create higher depths. However, for low powers, the differences in heat distribution may not be as apparent, as shown in *Figure 2.14*, where the vias were drilled at scan speeds of 100, 200, and 300 mm/sec with a power of 2.3 W, 25 repetitions, 15% overlap, and a focused laser with a 150 µm Z-offset.

Figure 2.14 Depth Vs diameters for different Scan speed at 2.3 W, 25 reps, 15% overlap

2.5.2 Via Circularity

At high scanning speeds, the laser beam may not have enough time to fully remove the material at the edges, resulting in an irregular via. Additionally, the laser beam may deviate from its intended path, causing the via to be off-center and non-circular. This trend was also observed by Zhang et al. [21]. Therefore, as shown in *Figure 2.15*, if the scanning speed is too high, such as 300mm/sec, the Via quality

is poor. On the other hand, if the scanning speed is very low, the laser beam will have too much time to melt the material at one spot, leading to material

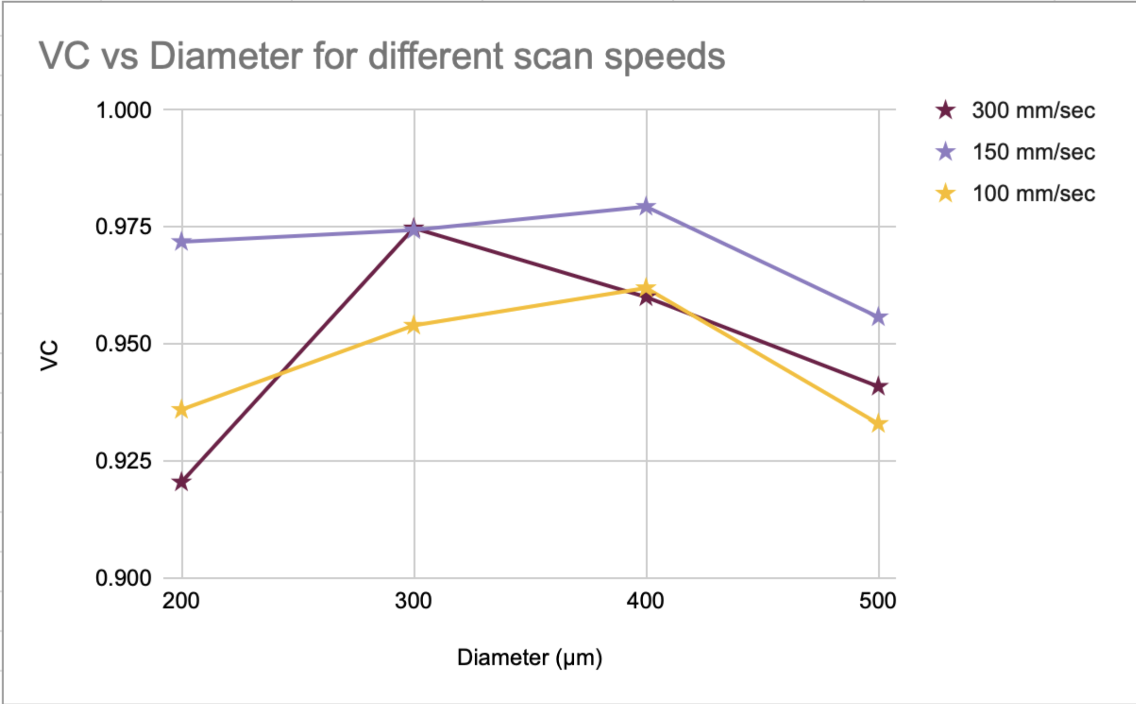


Figure 2.15 VC Vs Diameter for different Scan speeds at 2.3 W, 25 reps, 15% overlap

damage and poor quality of the via. Thus, to achieve high via quality in terms of roundness, it is essential to select an optimum scanning speed, such as 150 mm/sec, as shown in *Figure 2.15*.

2.5.3 Via Taper:

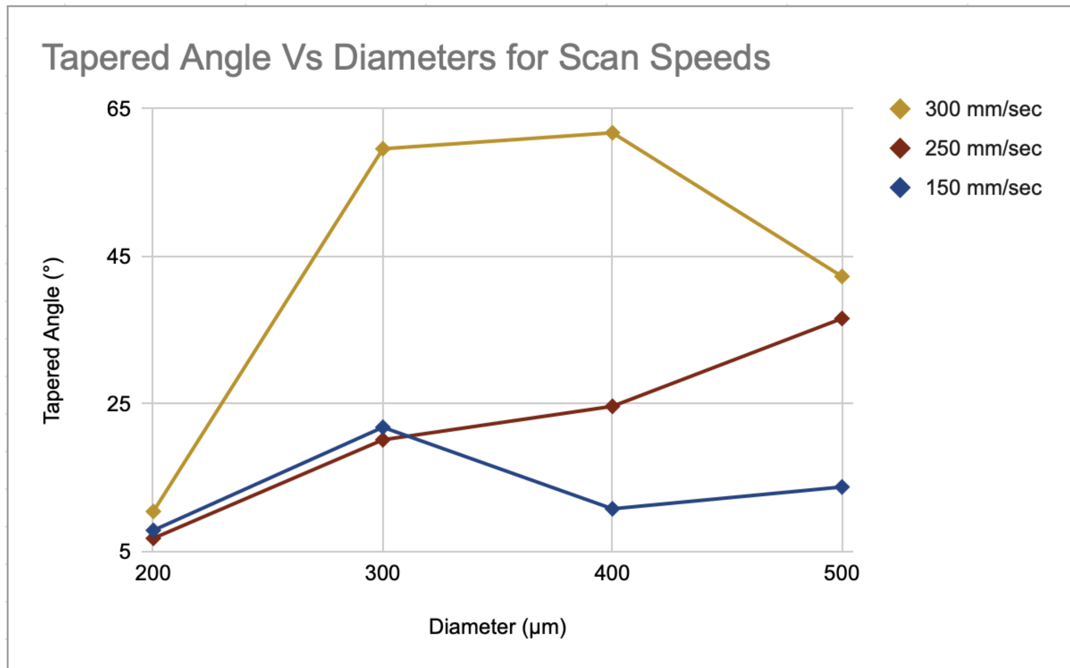
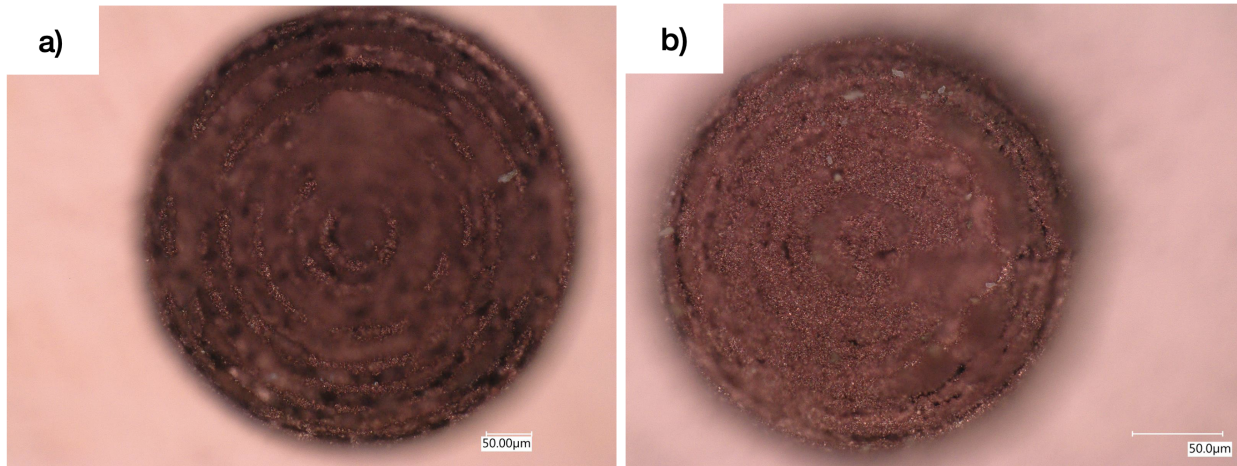


Figure 2.16 Tapered angle Vs Diameter for different Scan speeds at 2.3 W, 25 reps, 15% overlap

Scan speed has a significant influence on the tapered angle. As we can see in *Figure 2.16*, as the scan speed decreases, the amount of energy required to remove material increases, leading to a more uniform profile. This trend is also observed in the work of Shoaib Sarfraz et al. [18]. However, at lower diameters such as 200 and 300 µm, the tapered angles for both 150 mm/sec and 250 mm/sec are almost the same. This might be due to the excessive energy input of 150 mm/sec for lower diameters, resulting in a wider and shallower via giving a higher taper angle.

2.6 Influence of Overlap percentage on Via

The overlap percentage of the via influenced mainly the bottom surface and not the sidewall. The lower the percentage, the higher will be the roughness of the bottom surface. Also, the removal rate of the material will decrease[22]. In *Figure 2.17*, we can see the top-down view of the three vias drilled at 2.3 W, 25 reps, 150 mm/sec with overlap percentages as 15%, 50% and 90%. The images were taken after sputtering. Roughness was observed through the cross sections, which can be seen in Chapter 3 Section 3.3.5.



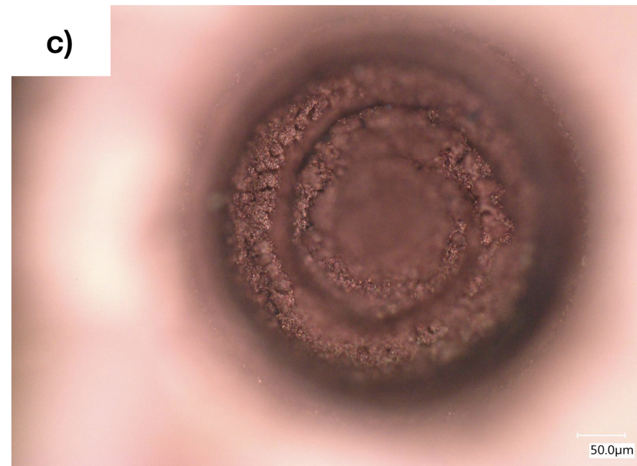


Figure 2.17 Bottom surfaces of sputtered vias drilled at 2.3 W, 25 reps, 150 mm/sec a) 15% b) 50 % c) 90%

2.7 Resolving disadvantages of laser drilling:

As discussed earlier, one of the main disadvantages of laser drilling is the deposition of melted and vaporized material surrounding the drilled via, known as the recast layer [23]. This layer adversely affects the physical and electrical performance of the via, as it contains voids that increase electrical resistance, making it difficult for redistribution layers [24]. The recast layer also creates a thermal barrier, which makes it challenging to establish thermal bonding or electrical contacts. If the layer is too thick, it takes a lot of time and money for cleaning it. Additionally, laser drilling produces debris or small particles surrounding the via, which affects its electrical performance unless it is cleaned.

To remove the recast layer and debris with less investment of time and cost, a protective layer was spin-coated on top of the wafer before laser drilling. The recast material and debris get deposited over this protective layer, and it is removed using IPA through ultrasonic cleaning. The differences were observed using a microscope and AFM. *Figure 2.18* clearly shows the complete removal of recast and debris for the via with a protective layer.

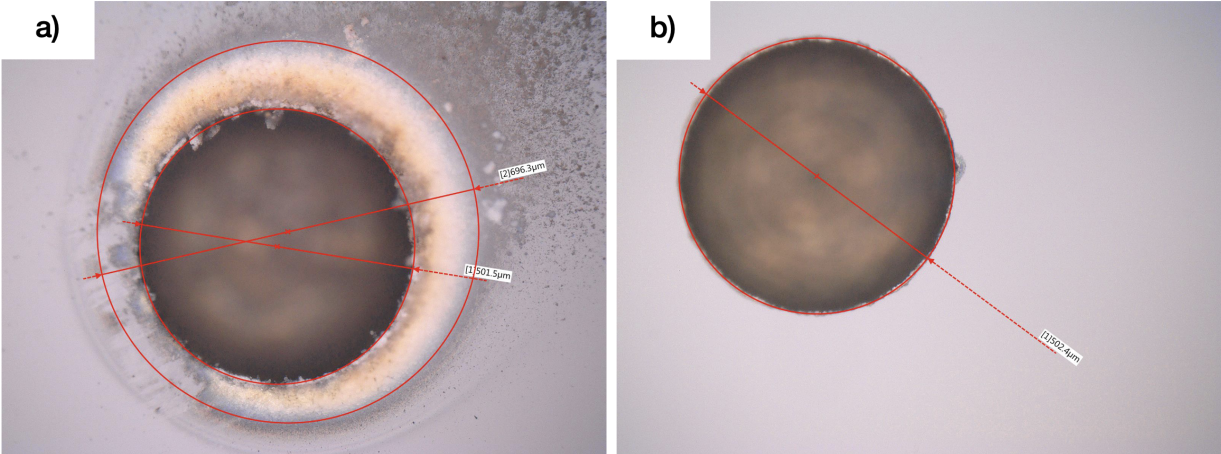
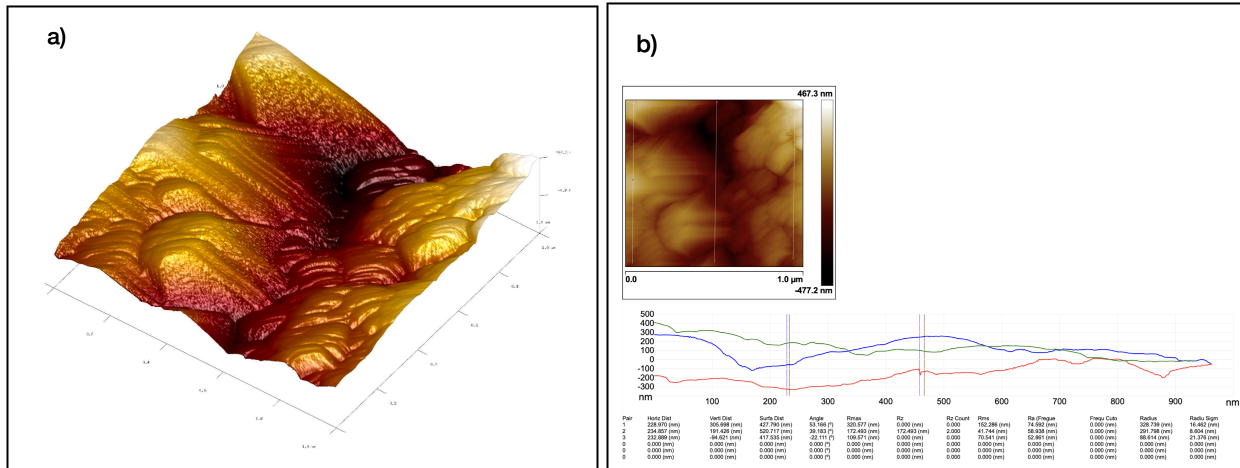


Figure 2.18 (a) 500 um via manufactured without having a protective layer (b) 500 um via manufactured with protective layer



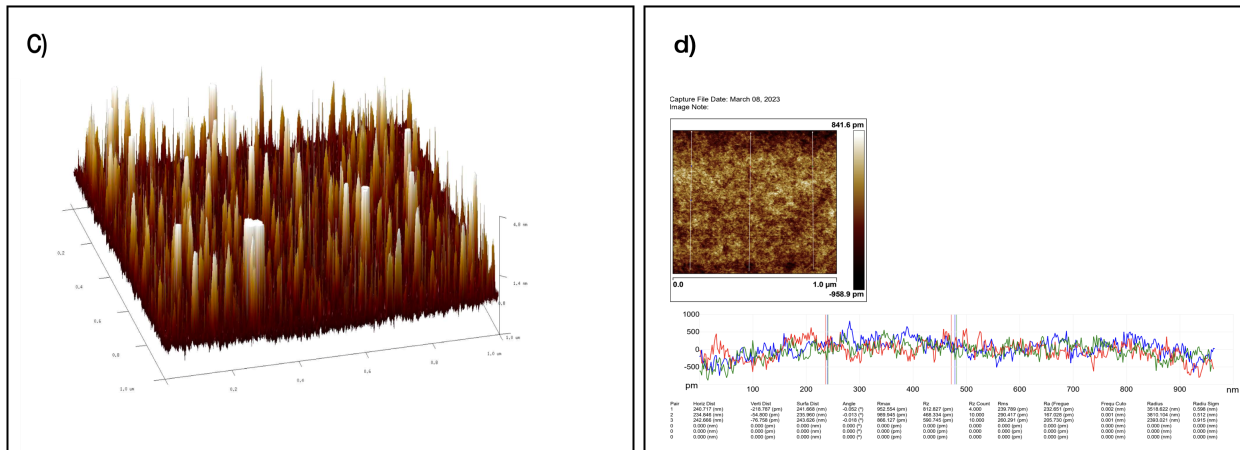


Figure 2.19 (a) 3D image of surrounding area of a 500 um via manufactured without having a protective layer (b) Surface roughness scan for 1 um around the area of the via (c) 3D image of surrounding area of a 500 um via manufactured with a protective layer (d) Surface roughness scan for 1 um around the area of the via manufactured with a protective layer.

In Figure 2.19, through the AFM images, it can be understood that the surface roughness is in the range of picometers for the via covered with the protective layer

and in the nanometers range for the one without the protective layer. This proves that the protective layer will help in avoiding the formation of the recast layer on the sample.

Another disadvantage of laser drilling is the formation of the Heat Affected Zone (HAZ) due to the thermal effects of laser beams [25]. We checked for the presence of the HAZ region around a single via with the help of the Rocking curve and ω:2θ Curve through XRD. The measurements were taken at three points for the rocking curve. The first point was taken very far (~10mm) from the via to understand how the pristine Si curve looks. The second point was taken within 1-10 um from the via to check for damage due to the via. The third point was taken within 1-2 mm from the via to see if there was any stress or cracks propagated. The penetration depth of these measurements (G = 0.99) is 88 μm beneath the surface. If there were any crystal imperfections or the presence of dislocations, rocking curves should be broadened. However, in Figure 2.20, we can see that the curves do not conclusively show any broadening effects. This indicates that a single via does not provide enough energy to damage the surrounding material.

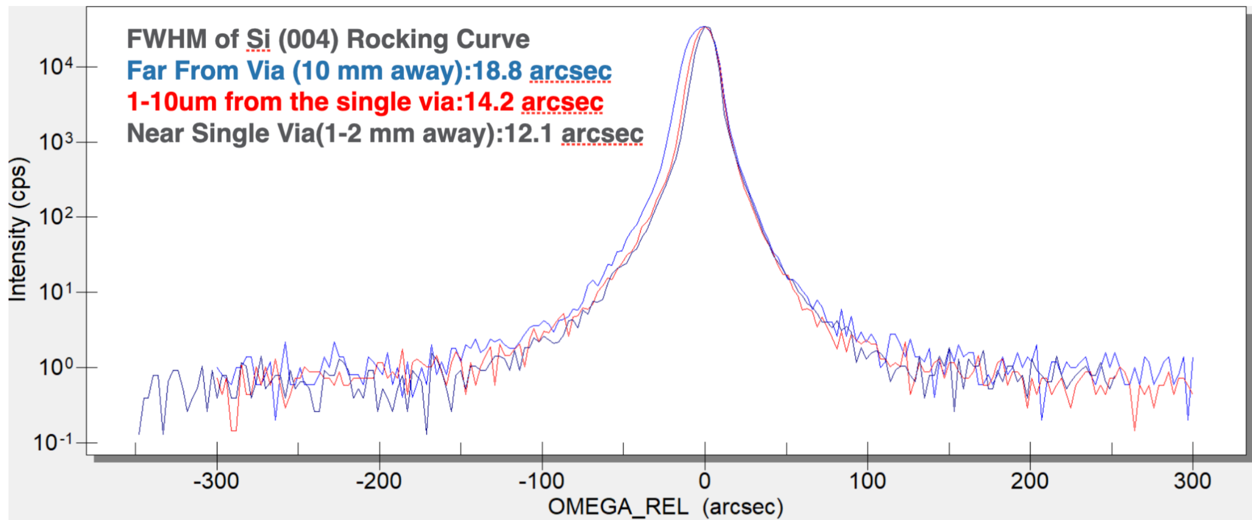


Figure 2.20 Si (004) rocking curve analysis

ω:2θ curves were also observed to check for any out-of-plane strain distribution. Measurements were taken at four different spots, three of which were the same as before, while the fourth spot was located approximately 1-10 μm away from another via. The penetration depth was 88 μm. From Figure 2.21, it can be seen that there is no broadening of the curves compared to the pristine curve taken 10 mm away. Therefore, we can conclude that no significant damage was caused by laser drilling at 2.3 W, 25 reps, 150 mm/sec, and 15% overlap.

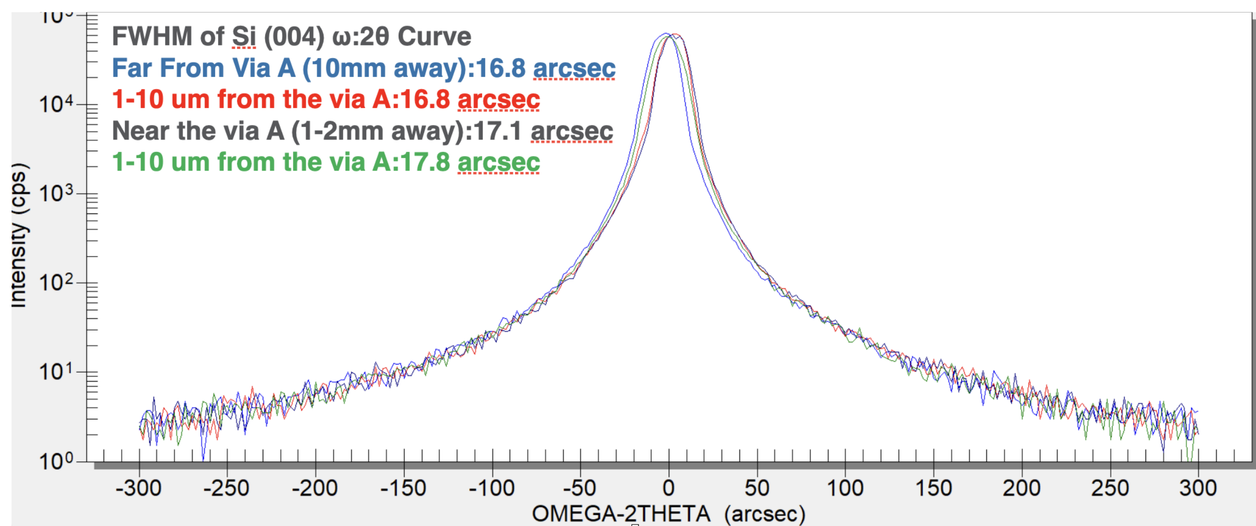


Figure 2.21 Si (004) ω:2θ Curve

Chapter 3 Seed layer deposition and Electroplating

The next steps for fabricating a via after laser drilling are thermal oxidation, seed layer deposition, and electroplating. Wet thermal oxidation was performed at 1050°C for a 2 µm thickness. Afterward, sputtering was done using two different machines: Ulvac 8000 and Denton Discovery Sputterer, to determine which produces higher-quality vias. Finally, electroplating is used to fill the Cu into the via. *Figure 3.1* depicts the schematic of the via fabrication process.

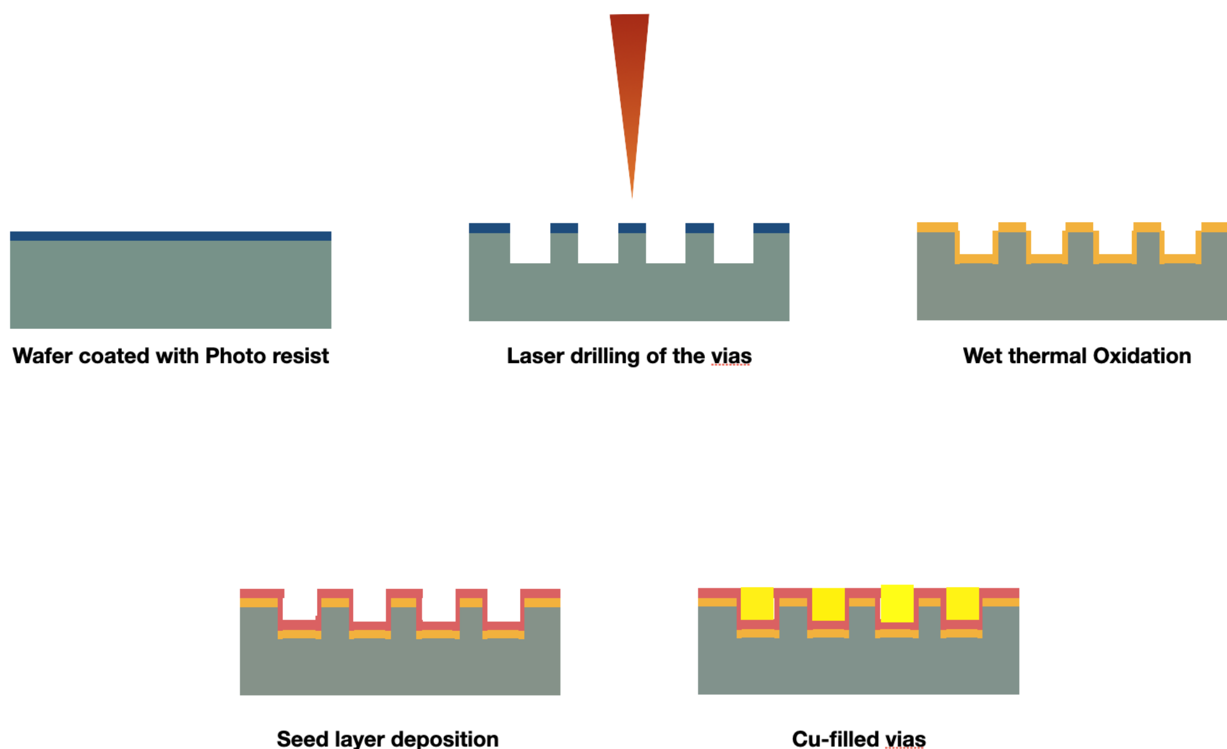


Figure 3.1 Via fabrication process

3.1 Differences between Ulvac 8000 and Denton Discovery Sputterer:

For comparison, we sputtered vias using the Ulvac 8000 and Denton Discovery sputterers, both of which use a magnetron sputtering source. We deposited 50 nm thick Ti followed by 300 nm thick Cu on 200 µm and 500 µm diameter vias drilled at various ranges of parameters. The Ulvac 8000 has 4" targets, while the Denton Discovery has 3" targets. The vacuum level of the Ulvac 8000 is better than that of the Denton Discovery. Both machines use Argon gas for sputtering, but the Denton Discovery uses a gas flow rate of 40 standard cubic centimeters per minute (sccm) and has a process pressure of 5mT, while the ULVAC uses a flow rate of 10 sccm and a process pressure of about 6.5mT. As the flow rates are different, the deposition rates differ [28], giving the Denton Discovery sputterer a deposition rate of 3.33 nm/sec and the Ulvac 8000 a deposition rate of 0.1 nm/sec. The throughput of the Ulvac 8000 is higher than that of the Denton Discovery sputterer

a)

b)

Figure 3.2 (a) Denton Discovery sputterer [26] (b) Ulvac 8000 [27]

3.2 Electrochemical deposition or Electroplating:

We used the Cu Elevate 6388 chemistry provided by Technic, Inc. [38] as the electrolyte, which consists of 988 ml of electrolyte 30 - a premixed solution of copper sulfate, sulfuric acid, and chloride, 7ml of Elevate Cu 6388 brightener and 5ml of Elevate Cu 6388 carrier. Brighteners and carriers were added to regulate the dynamics of the deposition at the bottom and sidewalls of the via. The concentrations of these chemicals were measured using the Electroplating Bath Analyzer provided by Technic, Inc., as shown in Figure 3.3 (a). The analyzer requires a mixture of 25 ml of bath solution with 75 ml of the working solution provided by the company. The measurements were taken at 24.75 C temperature. Brightener and carrier concentration was observed to be 5.41mL/L and 2.35 mL/L respectively.

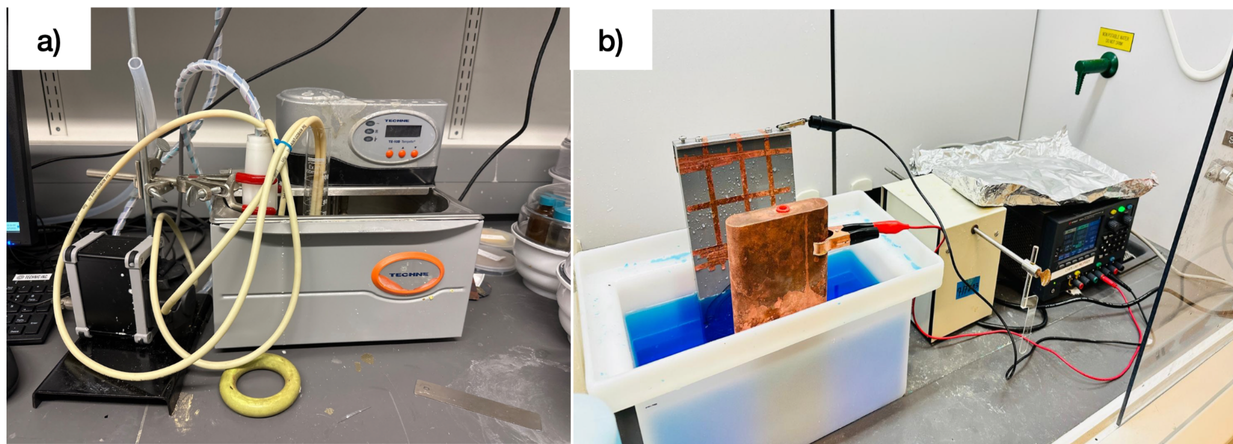


Figure 3.3 (a) Electroplating bath analyzer (b) Electroplating equipment

Cu bar as an anode and vias attached to the holder as a cathode were used for electroplating. This can be seen in *Figure 3.3 (b)*.

3.3 Results and discussion of ECD:

200 and 500 um vias are selected for understanding how lower diameters and higher diamers can influence the quality of cu-filling in the via.

3.3.1 Differences due to sputtering on a 500 um diameter via:

Kapton tape was attached to the samples and removed quickly to examine the adhesiveness of the seed layer. For a few sets of Denton-sputtered samples, the Cu coating got removed. However, this was not the case with Ulvac 8000-sputtered samples. This indicates the Ulvac 8000 provides better adhesion than the Denton. This was even evident with the Cu filling of vias as in Figure 3.4 (a) and (b). Denton and Ulvac sputtered, 500 µm diameter samples drilled at 2.3 W, 150 mm/sec, 25 reps, and 50% overlap were considered. They were plated for 14 hours at a 20mA current for an area of 0.4 x 0.4 cm^2, resulting in a current density of 125 mA/cm^2.

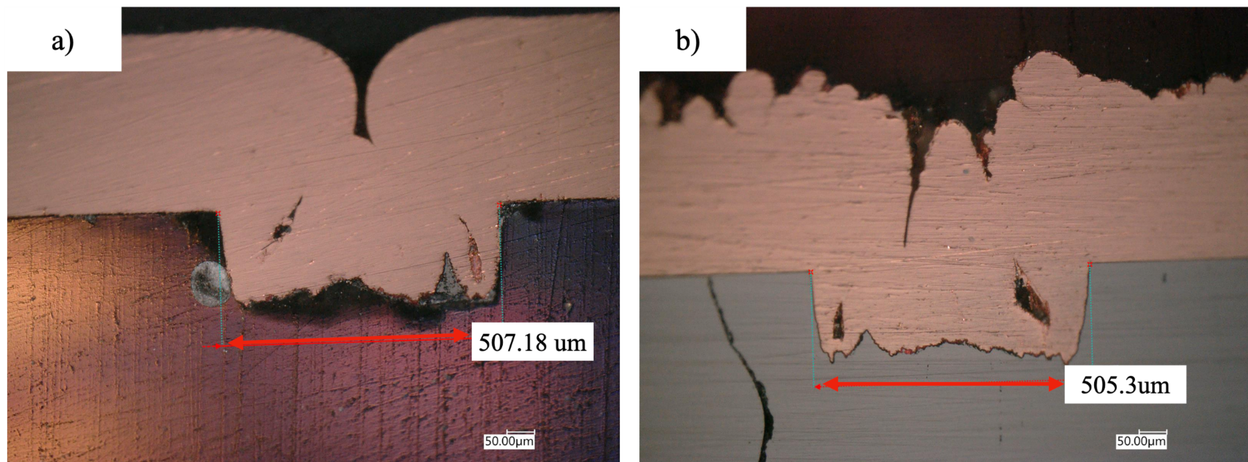


Figure 3.4 a) Cu-filled TSV sputtered by Ulvac 8000 b) Cu-filled TSV sputtered by Denton Disvoery sputtered

The Cu seed layer acts as a nucleation site for electroplated Cu. Due to poor adhesion, the seed layer on the sidewall or at the bottom can become detached, leading to irregularities in the deposition of plated Cu and causing voids. Additionally, metal ions may not attach to the seed layer properly due to poor adhesion, which can form islands or clumps, leading to the formation of voids as plating continues. Denton Discovery sputtered TWVs showed larger voids than Ulvac sputtered TWVs. As the size of the void can influence the electrical properties, Ulvac would be a better choice for 500 µm diameter vias. The differences in the quality of these vias might be due to poor vacuum control of the Denton sputterer leading to lower-quality films.

3.3.2 Differences due to sputtering on a 200 um diameter via:

Figure 3.5 shows that both the vias contain a large void at the center. However, it is noticeable that the Denton Discovery sputterer was able to sputter 200 µm diameter vias at the bottom, whereas the Ulvac 8000 couldn't completely sputter the bottom area. This could be due to the differences in flow rates between the two sputterers. Generally, the probability of high energy sputter particles reaching the bottom of the small diameter vias is low, because of the small exposure area and larger depths. Lower flow rates decrease the number of particles reaching the target, decreasing the probability. As the flow rate of the Ulvac 8000 is very low, it results in insufficient coverage of 200 µm diameter vias.

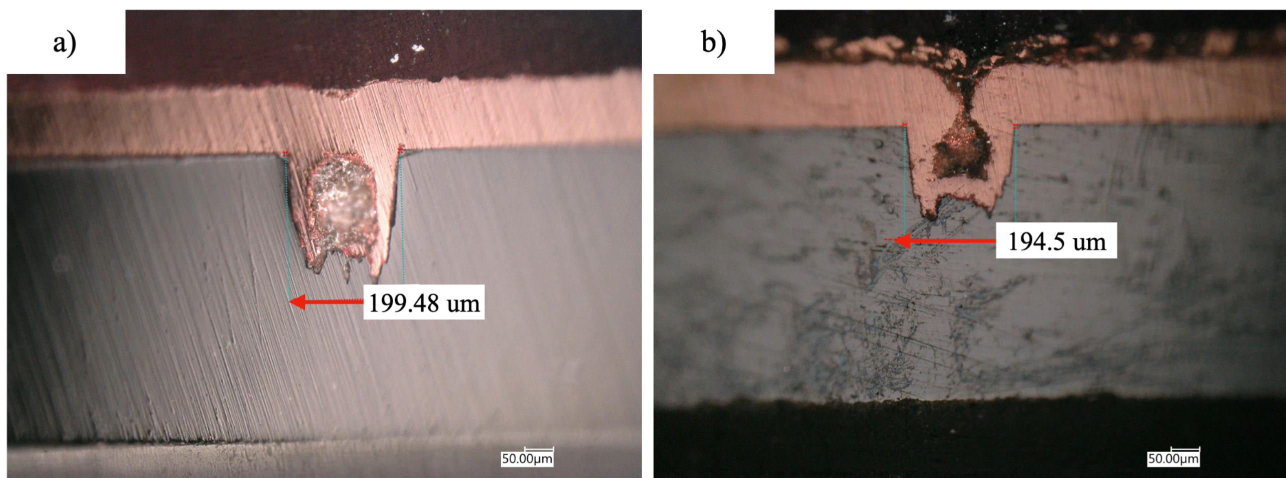


Figure 3.5 a) Cu-filled TSV sputtered by Ulvac 8000 b) Cu-filled TSV sputtered by Denton Discovery sputtered

3.3.3 Influence of laser drilled parameters: Peak Power

We plated 200 µm diameter, Ulvac sputtered vias at 80 mA/cm^2 for 7 hours. As previously discussed, the bottom coverage of the Ulvac samples is very poor for 200 µm diameter vias. The vias were drilled at 25 repetitions, 150 mm/sec, and 50% overlap using two different peak powers: 2.3 W and 1.85 W. From Figure 3.6, we understood that the via depth and tapered angle varies with power, but these factors did not significantly influence via filling or sputtering. For both samples, the seed layer distribution was poor resulting in voids. As the 2.3 W via is deeper than the 1.85 W via, the 7 hour plating time was insufficient for joining the two sidewalls.

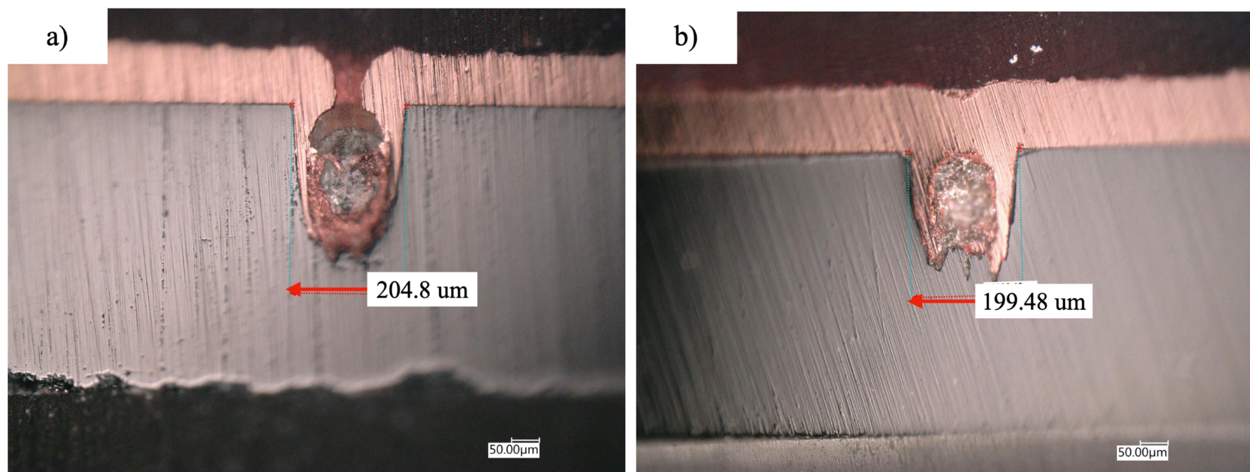


Figure 3.6 a) 2.3 W, 25 reps, 150 mm/sec, 50 % overlap b) 1.85 W, 25 reps, 150 mm/sec, 50 % overlap

3.3.4 Influence of laser drilled parameters: Repetitions and Scan Speed.

To understand the influence of repetitions, the via was drilled at 2.3 W, 150 mm/sec, and 50% overlap. Only repetitions were decreased from 25 to 15. The via was sputtered by a Denton discovery sputterer and plated at 80 mA/cm^2 for 7 hours. We can see that the bottom surface is covered completely, but the via is showing a void. This could be due to the high current density. Decreasing the current density can give a void-less via.

To understand the influence of scan speed, the scan speed was increased to 300 mm/sec from 150 mm/sec. Plating was done at 80 mA/cm^2 for 6 h. We decreased the plating time to reduce the overburden, but we can clearly see that 6h is not enough for the complete plating of the via. Also, if it was plated for a longer time it would have given a void because sidewall growth is dominating bottom-side growth. Lower current densities might give a void-free via. But from both the vias we understood the laser drilled parameters are not affecting the Cu filling, it only influences the sidewall profile and bottom surface.

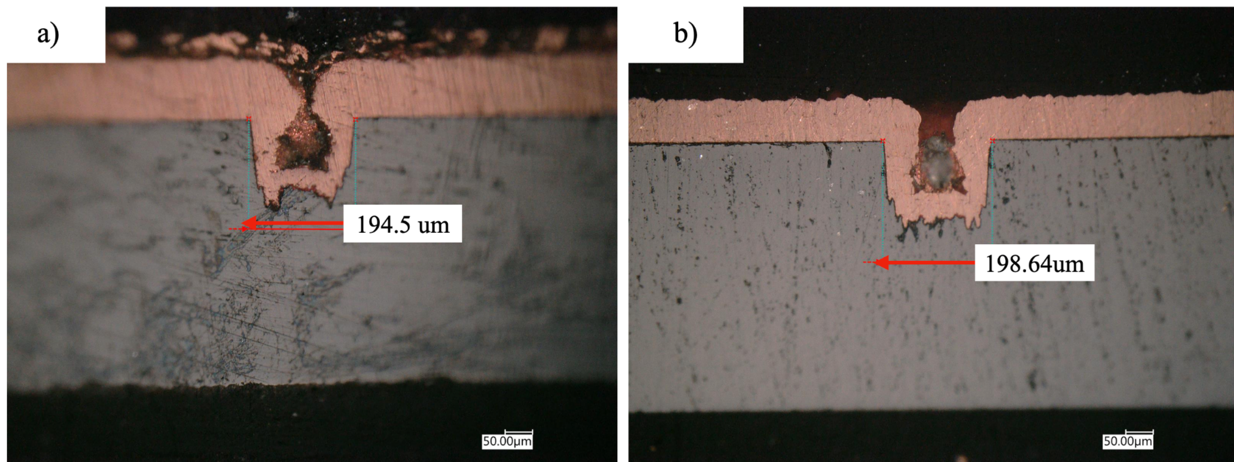
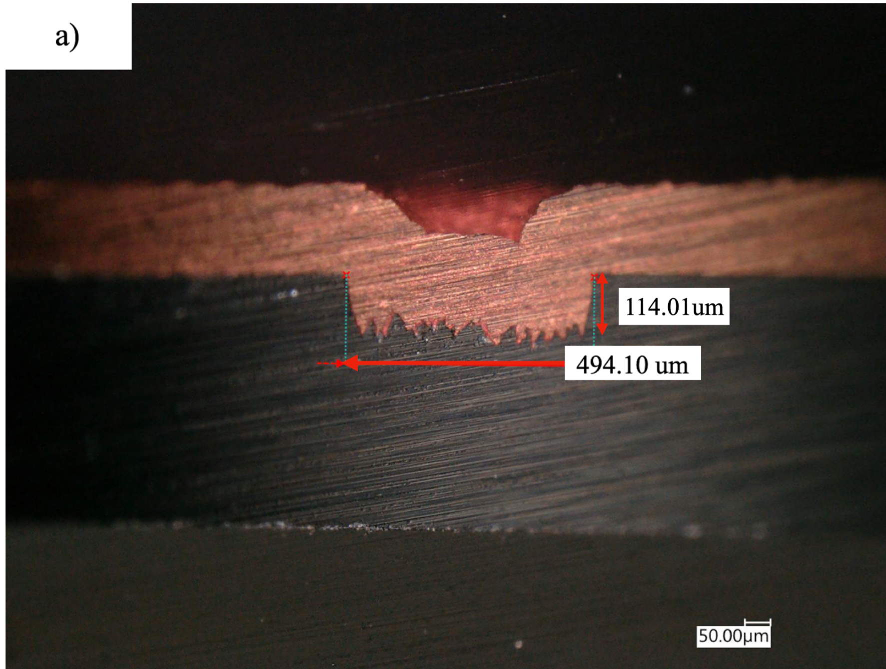
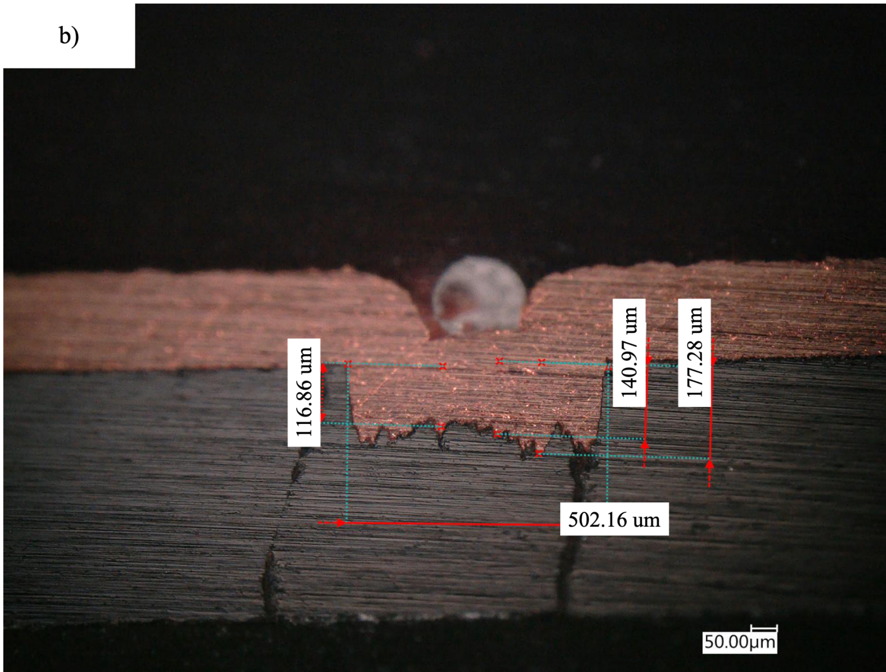


Figure 3.7 a) 2.3 W, 25 reps, 150 mm/sec, 50 % overlap b) 1.85 W, 25 reps, 150 mm/sec, 50 % overlap

3.3.5 Influence of laser drilled parameters: Overlap Percentage.

The influence of overlap percentage was observed using 500 µm diameter vias. As discussed previously, the Ulvac 8000 sputtering system is well-suited for fabricating large diameter vias, and we have lowered the current density to 80 mA/cm^2 from 125 mA/cm^2 that was reported in section 3.3.1


a)
114.01um
494.10 um
50.00µm


b)
116.86 um
140.97 um
177.28 um
502.16 um
50.00µm

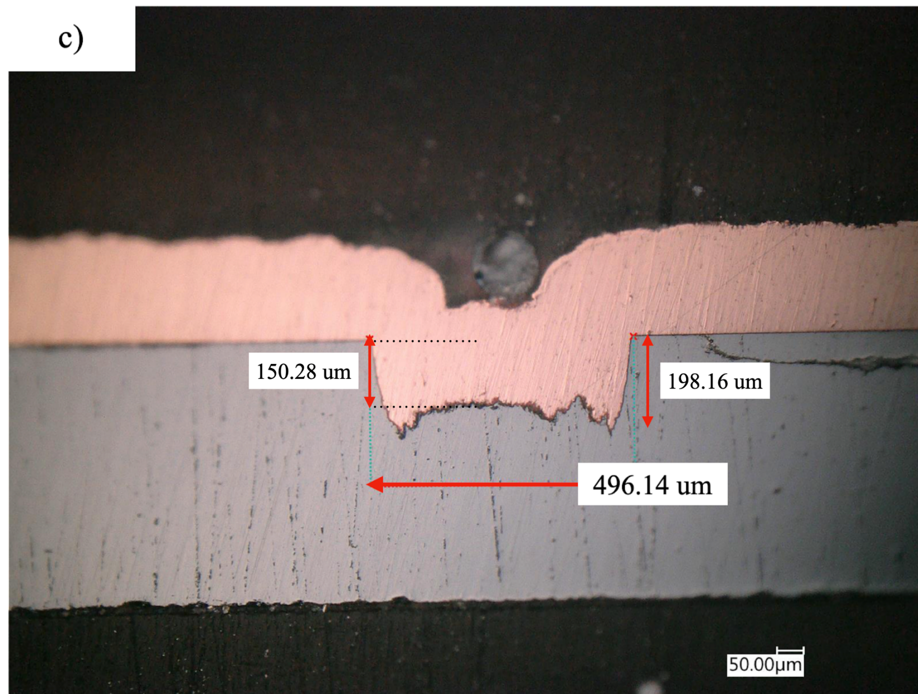


Figure 3.8 a) 2.3 W, 15 reps, 150 mm/s, 15% Overlap (polished at 800 grade) b) 2.3 W, 15 reps, 150 mm/s, 50 % overlap (polished at 800 grade) c) 2.3 W, 15 reps, 150 mm/s, 90% Overlap (polished at 1200 grade)

As shown in *Figure 3.8 (a)*, the bottom surface of the 15% overlap via is very rough compared to the 50% overlap via in *Figure 3.8 (b)*, and the 50% overlap via is rougher than the 90% overlap via in *Figure 3.8 (c)*. Although the 15% overlap via takes less time to fabricate and has less depth, the high roughness at the bottom surface leads to non-uniform distribution of grains, which affects the electrical properties and reliability of the TSVs. On the other hand, the 90% overlap via is deeper and takes more time to fabricate, but the surface is smoother, providing a

more uniform distribution of large grains. Grain structure and grain size have significant influence on hybrid and thermal compression bonding. More about grain structure is discussed in the future work.

3.3.6 Current density Variation for Denton sputtered sample:

In section 3.3.1, we observed the presence of voids in a Denton sputtered sample at 125 mA/cm^2. To understand if lowering the current density can help in forming defect-free Via, we decreased the current density to 40 mA/cm^2 and kept it for 28 hours. The sample was drilled at 2.3 W, 25 repetitions, 150 mm/sec, and 50% overlap. From *Figure 3.9*, it can be seen that even at lower current densities, voids are being formed, indicating that Denton-sputtered samples provide a non-uniform and poor adhesive seed layer for large-diameter vias.

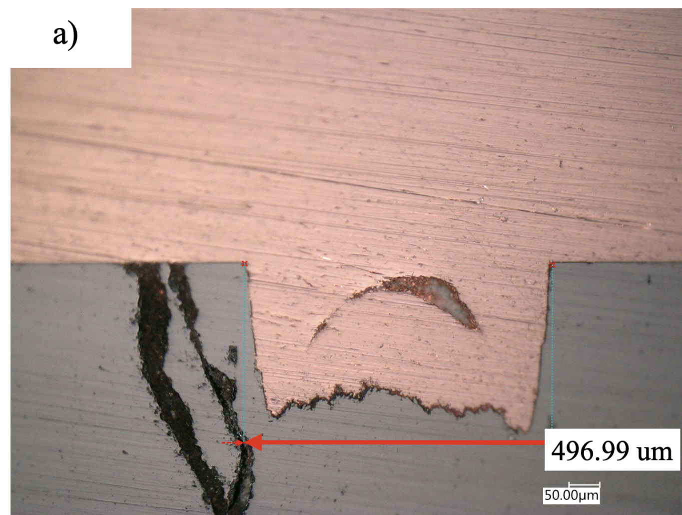


Figure 3.9 2.3 W, 25 reps, 150 mm/sec and 50% overlap plated at 40 mA/ cm^2

3.3.7 Influence of diameter on plating quality at same current density:

A 200 µm via and a 500 µm via were drilled using 2.3 W, 15 reps, 150 mm/sec, and 50% overlap for understanding the influence of diameter. The 200 µm via was plated with Denton, and the 500 µm via was plated with Ulvac, as Denton was found to be more suitable for the 200 µm diameter and Ulvac for the 500 µm diameter. At 80 mA/cm^2 current density, 200 µm gives a void, whereas 500 µm gives a void-free via as in *Figure 3.10*. Lowering the current density for 200 µm can help in obtaining a void-free via.

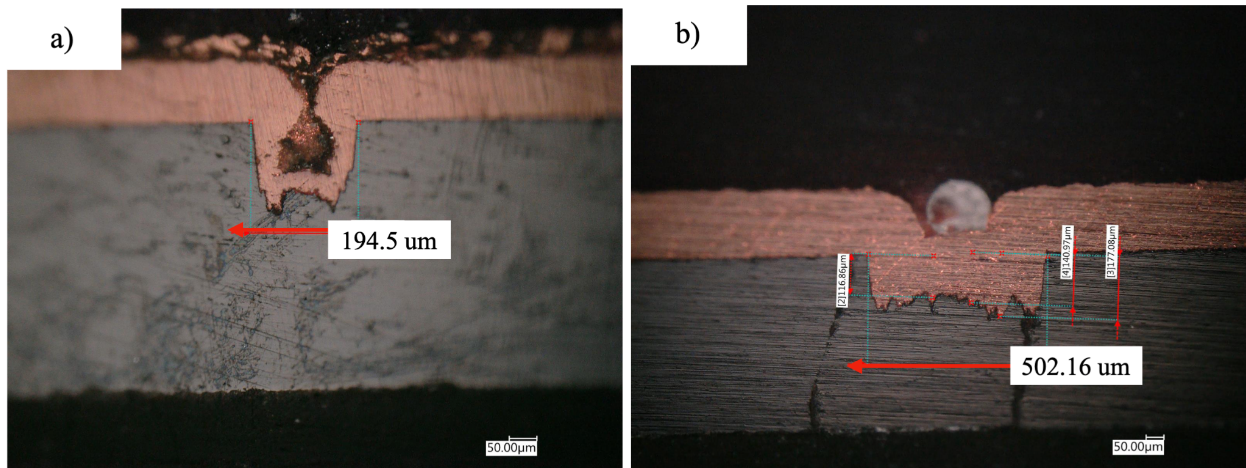


Figure 3.10 a) 200 µm via drilled at 2.3 W, 15 reps, 150 mm/sec and 50% overlap at 300X **b)** 500 µm via drilled at 2.3 W, 15 reps, 150 mm/sec and 50% overlap at 200 X.

Chapter 4 Conclusion and Future work

4.1 Conclusion:

In this thesis, we fabricated TWVs using laser drilling as the etching process, followed by thermal oxidation, sputtering, and electroplating. Laser drilling was chosen to provide flexibility with diameters that can be used for power vias of Si-IF. To achieve the desired depth of 100-200 um and a good quality via, we have varied laser parameters like peak power, repetitions, scan speeds, overlap percentage, etc to understand the influence on via's depth, via taperness, via circularity, and roughness. Here are the observations in the considered range of parameters:

As the peak power increased, the depth of the via increased. For the same peak power, the depth of the via increased with an increase in diameter up to 300 µm or 400 µm after that, it decreased. This is because as the exposure area increases, the distribution of energy differs leading to shallower vias. Via circularity improved, and taperness increased with the decrease in power.

As the number of repetitions increased, the depth of the via increased. At the same number of repetitions, the depth variation with diameter was similar to that observed at constant peak powers. The via circularity was good at the optimum

number of repetitions, 25, and via taper angle decreased with the increase in the number of repetitions because of more material removal.

Scan speed didn't have an influence on the depth. A scan speed of 150 mm/sec showed better VC. The tapered angle was observed to be lower for small scan speeds such as 150 mm/sec. However, if the scan speeds are very low, it leads to excessive heating, forming a shallower Via.

Overlap percentage influences the roughness of the bottom surface of the via. 15% overlap had higher roughness, and 90% had a smooth bottom surface.

Based on the observations, to obtain desired depths, 2.3 W and 1.85 W, 15 and 25 repetitions, 150 mm/sec and 300 mm/sec scan speeds at 50% overlap were selected for analyzing sputtering and electroplating characteristics. Ulvac 8000 showed better performance for 500 µm diameter vias due to better adhesion of the seed layer, whereas Denton showed better performance for 200 µm diameter vias due to high Ar flow rates. It was observed that Ulvac sputtered 500 µm vias drilled at 2.3 W, 15 reps, 150 mm/sec at all three overlaps gave a void-free via at 80 mA/cm2 plated for 14 h. The 90% overlap at these parameters will be a better choice as its bottom surface is smooth, which leads to large uniform distributed grains.

4.2 Future work:

After plating the blind vias, Chemical Mechanical Polishing (CMP) should be performed to remove the overburden, and machining to make it a through via. Electrical characteristics, bonding characteristics, and reliability should be measured to understand the performance of the via. The grain structure of Cu plays a major role in enhancing the via performance. Various factors like seed layer deposition, current density, bath chemistry, and annealing can help in obtaining desired grain structures. Each of these factors is discussed in detail below:

Grain structure significantly varies with the seed layer deposition, as the seed layer provides the nucleation sites for grain growth. Grain orientation and roughness of the seed layer can affect the grain size, grain orientation, and morphology of the electroplated copper. For example, a strong <111> oriented seed layer structure with pulsed plating can give rise to nano-twinned structures [29]. The smooth surface of the seed layer provides larger grains in comparison to a rough surface due to reduced number of nucleation sites [30]. The thickness of the seed layer doesn't affect the grain structure in TSVs [31].

Electroplating characteristics like type of current applied, current density, bath additives play an important role in altering the grain structure as it helps in changing the kinetics of the reactions. For example direct current (dc) gives a regular Cu

grain structure with annealing twins and pulsed current gives rise to nano twins [32]. Additives like gelatin will give nano twinned structures in a blind via. Gelatin is used to suppress the evolution of hydrogen gas in the bath [33]. The combination of high current density and high additives will lead to fine grain formation [34].

Annealing is a post processing technique commonly used to alter the grain structure, mechanical and electrical properties. Material is heated to a certain temperature, soaked for a period of time and cooled down slowly or rapidly. Annealing at recrystallized temperatures which is 0.5-0.7 times the melting point gives rise to fine grains. At room temperature and temperatures higher than recrystallized temperature will give rise to large grains [35]. Once a desired structure is formed, rapid cooling is performed to obtain the same structure at room temperatures.

Current research shows nano twin structures formed inside the grains show very good properties like high conductivity, ultra high strength, improved electro-migration induced diffusion for good bonding [33]. Crystals oriented in <111> consist of a larger number of electrons decreasing the resistance. Coarse grains have better conductivity but poor inter diffusion of Cu that might lead to issues at the interface of the metal-metal bonds or D2W bonds formed by thermal compression bonding or hybrid bonding. Large grains might also give rise to

vacancies at the interface. Fine grains with twin structures will provide better inter diffusion increasing the bonding strength. [36][37]. Fine grain with nano twin structure can be a better solution for obtaining high bond strength and increased conductivity and above mentioned factors can be varied to obtain a high quality, reliable TWVs.

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