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# Modeling Guidelines for ASIC Reuse

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## Abstract

In this report, we discuss the various issues and problems associated with ASIC reuse. We describe the different models of communication between components and the essential issues in interfacing ASICs that use different communication protocols. We come up with guidelines that help in modeling for reuse. We also propose a new HDL, SpecC, that has the desirable characteristics for co-designing systems. This language is suited for ASIC reuse and overcomes the limitations of VHDL.

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## Abstract

In this report, we discuss the various issues and problems associated with ASIC reuse. We describe the different models of communication between components and the essential issues in interfacing ASICs that use different communication protocols. We come up with guidelines that help in modeling for reuse. We also propose a new HDL, SpecC, that has the desirable characteristics for co-designing systems. This language is suited for ASIC reuse and overcomes the limitations of VHDL.

## 1 Introduction

In the last decade, digital electronic systems have been growing in complexity and functionality very rapidly. Explorations must be done at the system level to reduce the number of objects that have to be dealt with. The design-turnaround time and design costs can be reduced by *reusing* existing designs. However, reusing application-specific ICs (ASICs) is not an easy task. Components need to communicate with other components in the system for data transfer and synchronization. ASICs may have to be redesigned when reuse is employed because of communication protocol mismatches. It is now obvious that ASICs must be modeled in a way that supports ease of reuse. In this report, we outline the guidelines for modeling ASICs with a goal of achieving reusability.

The report is organized as follows. We first describe the reuse problem and the *plug-and-play* capability in Section 2. This section also defines the concept of a channel and emphasizes the dichotomy of communication and computation. Section 3 gives an overview of the experiments performed to understand the is-

issues involved in the reuse problem. We then present our guidelines for modeling in Section 4. Our critique of VHDL as a modeling language leads us to present SpecC as a preferred language for reuse in Section 5. Finally, we conclude in Section 6.

## 2 The Reuse Problem

The reuse problem is well illustrated by the *plug-and-play* feature. Consider a system shown in Figure 1 where it is desired to replace ASIC B with another ASIC E that provides the same functionality. This task is non-trivial in the general case because the communication protocols of B and E might be different.

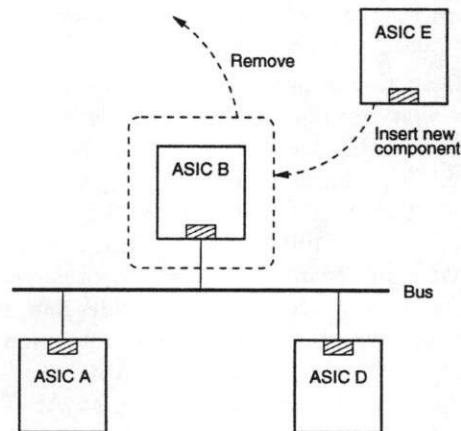


Figure 1: *Plug-and-play*: change an ASIC

Similarly, in Figure 2, Bus 1 that connects ASIC A to ASIC B has to be replaced with a new bus, Bus 2. Again, this is not easy since the ASICs A and B used the Bus 1 protocol earlier and now need to use the

## Bus 2 protocol.

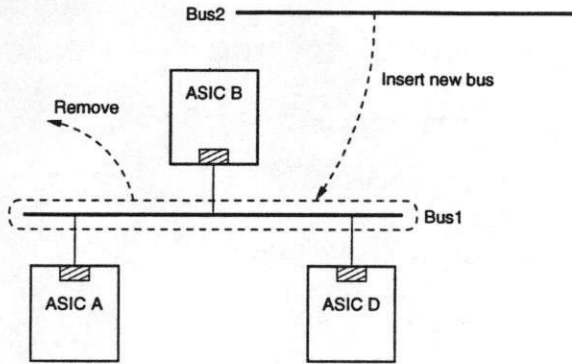


Figure 2: *Plug-and-play*: change a bus

The *plug-and-play* capability essentially means ease of replacing a component with a new component that has the same functionality but different implementation. A system configuration consisting of three ASICs, (A, B, D), is shown in Figure 3. It is desired that ASIC B be replaced with a new ASIC E. The new ASIC has the same functionality as B but possibly a different design, e.g. it may be pipelined, or may be area/power optimized. The new ASIC, in general, will use a different communication protocol. Hence, it cannot be directly connected in the existing system. A *protocol transducer* is required to translate the protocols. Thus, whenever an ASIC is replaced and there is a protocol mismatch, a new transducer has to be used.

Similarly, there may be protocol mismatches when the bus itself is replaced, e.g., a VME bus might be replaced by a PCI bus. A system configuration with three ASICs connected through a bus is shown in Figure 4. Bus 1 is replaced with Bus 2. The new bus, Bus 2, uses a different communication protocol. Hence, transducers must be inserted for each component since the components used the older Bus 1 protocol. This is shown in Figure 4 where three new transducers are required to connect the ASICs to the new bus. This is in contrast to replacing an ASIC where only one transducer might be modified or where only one new transducer has to be inserted. When a bus is replaced then all the components connected to the bus need new transducers.

## 2.1 Communication vs. Computation

The biggest obstacle to reuse is the communication protocol mismatch problem. As a first step towards reuse, the distinction between *computation* and *communication* must be emphasized. In an ASIC design model, **the communication portion needs to be separated from the computation portion**. If communication is mixed with the computation in a component then every time there is a mismatch in the communication protocols, the components have to be redesigned to reflect the new protocol. However, if communication is separated from the computation, then the basic core that defines the ASIC functionality remains the same. Only the communication block needs to be modified for the new protocol. This dichotomy between computation and communication is achieved naturally if *communication channels* are used and modeling is done at higher abstraction levels as explained below.

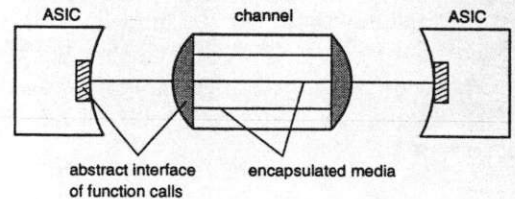


Figure 5: A generic communication model with a channel

A generic communication model [3] using a channel is shown in Figure 5. The main idea is to dissociate the detailed communication protocol from the ports of the component. Like the bus widths, number of control signals, timing and so forth from the ports of the component. The computation in the ASIC component makes calls to abstract function calls in order to read/write variables and exchange data. It does not even need to know what kind of channel will be used eventually for the actual communication. All that is required is that the channel conforms to the port interface. The port interface of the ASIC consists of function calls while the actual communication media is encapsulated in the channel. The data transport methods in the channel do the actual implementation of the protocol.

The port interfaces of ASICs would be comprised of function calls whose primary purpose is to transfer *information* across the port. It is upto the communicating ASICs to give it a meaning and interpret the information being transferred in different ways de-

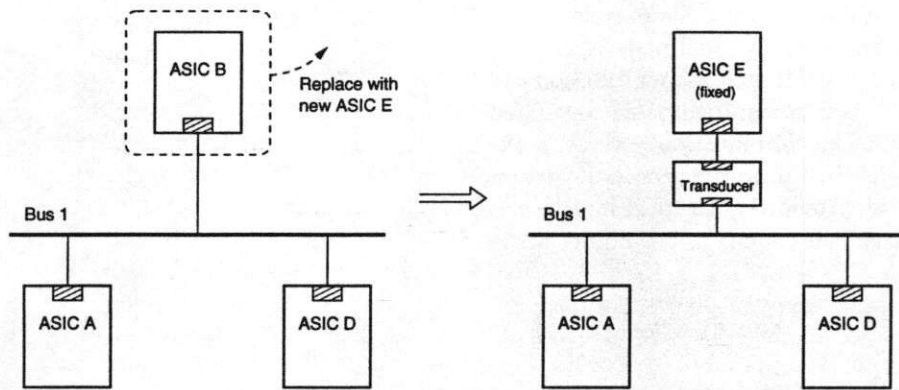


Figure 3: Effect of replacing an ASIC in a system

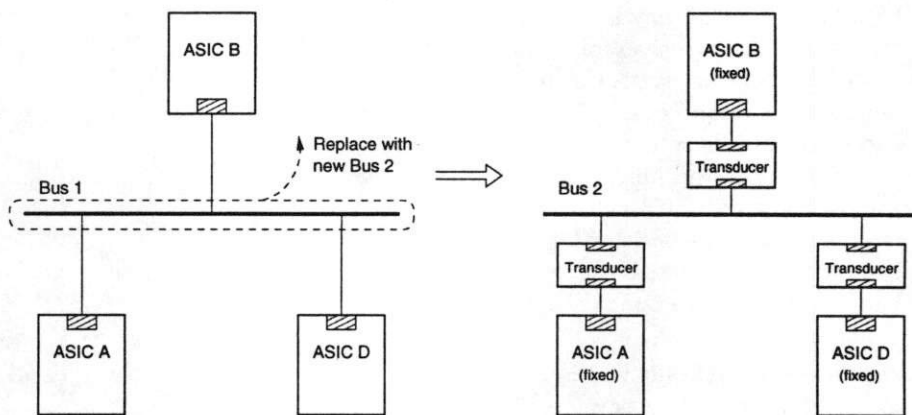


Figure 4: Replacing a bus necessitates change of transducers



pending on the protocol. Typical function calls would include `read()` and `write()`. An example is shown in Figure 6. A skeletal code fragment and port interface declaration is shown in Figure 6(a). The port interface consists of detailed bit level signals and the code includes the detailed timing. However, compare this to the code fragment shown in Figure 6(b). The port interface now consists of an abstract function call called `write()`. The transfer protocol is encapsulated in this function call. The computation process in the ASIC does not use detailed timing protocol. It just invokes the function call provided in the port interface as shown on the line "`write (local);`" in Figure 6(b).

<pre> .... port ( ....   clk : in bit;   dout : out integer;   start : out bit ); .... begin ....   start &lt;= '1';   wait until clk = '1';   dout &lt;= local;   start &lt;= '0'; .... end; (a) </pre>	<pre> .... port ( ....   function write (data : integer);   ); .... begin ....   write (local); .... end; (b) </pre>
--	--

Figure 6: ASIC Port Interfaces: (a) Detailed Bit-level (b) Abstract Function calls

Generic function calls such as `read_word()` and `write_word()` can be used to transfer any kind of information. Thus, the sender and receiver of words can transfer data of various widths, control signals, exceptions etc. using such function calls. There is another option. The port interfaces can be modeled differently to actually reflect the kind of transaction occurring across the port. If such is the case, then the port interface will consist of function calls like `request_and_wait()`, `data_size()`, `component_exception()`, `terminate_operation()`, `priority_trigger()`, `component_idle()` etc.

The port interfaces do not include bit-widths and timing details. It is, therefore, easier to develop the protocol transducers at a behavioral level rather than at detailed bit level. It may even be possible to generate the transducers automatically. Secondly, generic transducers that do translations between typical protocols can be designed and stored in a library. Furthermore, customization of a generic transducer is simpler if the models are at a higher level and do not include

timing details.

We next look at the implementation issues for systems containing channels. This will help us to determine the effect of using channels on the *plug-and-play* problem. Consider a typical system of two synthesizable ASICs as shown in Figure 7. ASICs A and B

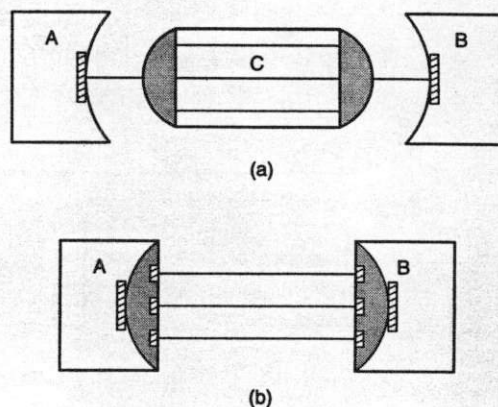


Figure 7: Channel inlining for synthesizable ASICs: (a) before inlining (b) after inlining

are synthesizable components and use a channel C for communication. When the system is implemented, the methods of the channel are **inlined** into the connected ASICs. Figure 7(a) shows the model at the higher level before the system is implemented. The channel methods are moved into the ASICs during implementation and the resulting model is shown in Figure 7(b). The bus wires that were originally encapsulated by the channel are now exposed.

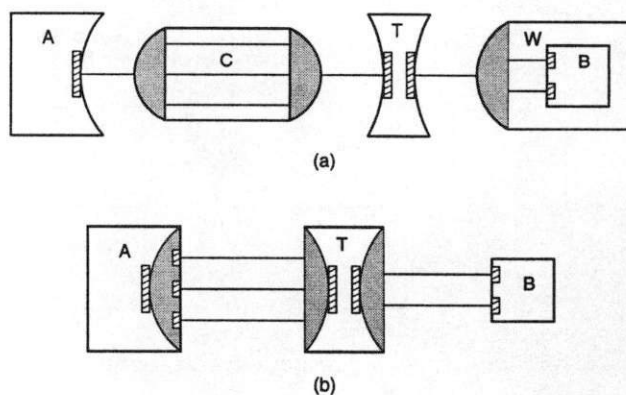


Figure 8: Channel inlining for a synthesizable ASIC and a fixed component: (a) before inlining (b) after inlining

When B in Figure 7 is replaced with a fixed component, we get a system as shown in Figure 8, where a synthesizable ASIC A communicates with B. We encapsulate B in a wrapper W since B is not synthesizable and has a low-level port interface. Thus, The function of the wrapper is to provide an abstract port interface for the fixed component, a port interface that consists of function calls instead of the detailed bit-level interface that a fixed component has. This model before system implementation is shown in Figure 8(a). The protocol of B as encapsulated by wrapper W may be different from that used by the channel C. A protocol transducer T will then have to be inserted between the channel C and the wrapper W. If wrapper W and channel C use the same protocol then the transducer will basically be an *identity* component or one that has just a memory element. The primary function of this transducer is to translate all communication transactions between the fixed component B and ASIC A. When the system is implemented, the methods on the side of the synthesizable ASIC are moved into the ASIC. The methods of the channel on the side of the fixed component are joined with the wrapper and implemented together with the protocol transducer as shown in Figure 8(b).

Thus, the process of IP reuse involves modeling components at a higher level and declaring port interfaces using function calls. ASICs with such generic interfaces are stored in a library. Any ASIC with the desired functionality can be chosen and plugged into the system model. An appropriate generic transducer is picked from the library and modified for doing protocol translation between this particular ASIC and the system being designed. This higher level system model is then refined and the channel methods are inlined into the ASIC, as discussed above. The transducer is also refined during system implementation along with other components.

Similarly, the channel can be replaced with any other bus channel in the library as long as it provides the abstract function calls used inside the component and specified by the port interface, e.g., a channel might encapsulate a VME bus and provide an ASIC with methods for reading and writing word a from memory. This channel can be replaced by another that encapsulates a PCI bus for instance but provides the same interface that consists of the read/write methods. In addition, the channel can also be incrementally refined. It can provide communication methods using simple function calls and shared variables in the

earlier phases of specification and partitioning. Later the channel can be refined into a detailed timing model that reflects an actual physical bus protocol.

## 2.2 Communication Implementations

Another important issue for reuse is the presence of a rigorous methodology to design the system from a high level specification. The methodology will consist of well defined transformations and intermediate models. This provides documentation and helps in reuse since reuse is difficult both at the final implementation level which is too detailed as well as the high level specification which is too abstract.

A generic methodology for hardware-software co-design for ASICs [1] is shown in Figure 9. The design steps include *allocation*, *partitioning*, *scheduling* and *communication refinement*, which form the synthesis flow of the methodology. The task of allocation determines the number and types of the system components, such as processors, ASICs and busses, used to implement the system behavior. The task of partitioning maps the sub-behaviors in the specification to the system component. Scheduling determines the ordering of execution of the sub-behaviors on a sequential processor. The task of communication refinement selects the appropriate protocols and resources to implement the abstract communications between the sub-behaviors. It also generates protocol transducers used for interfacing components with different protocols.

Such a methodology with well defined design steps can go a long way in keeping the design modular and reducing debug/test time. Each design step generates a more refined model, preferably in the same language. This provides a standard documentation and improves communication between the designers. The well defined models and transformations also provide a good base for formal verification of the refined models. The intermediate models also make the design more manageable and maintainable for future upgrades, thus, encouraging IP reuse.

The different components in a system may communicate using different architecture implementations. We next describe the different communication models. Communication between two components would use one of these styles. It is, thus, important to describe the models so that abstract interfaces may be defined for them. Later, this information can be used to generate generic transducers for interfacing to these

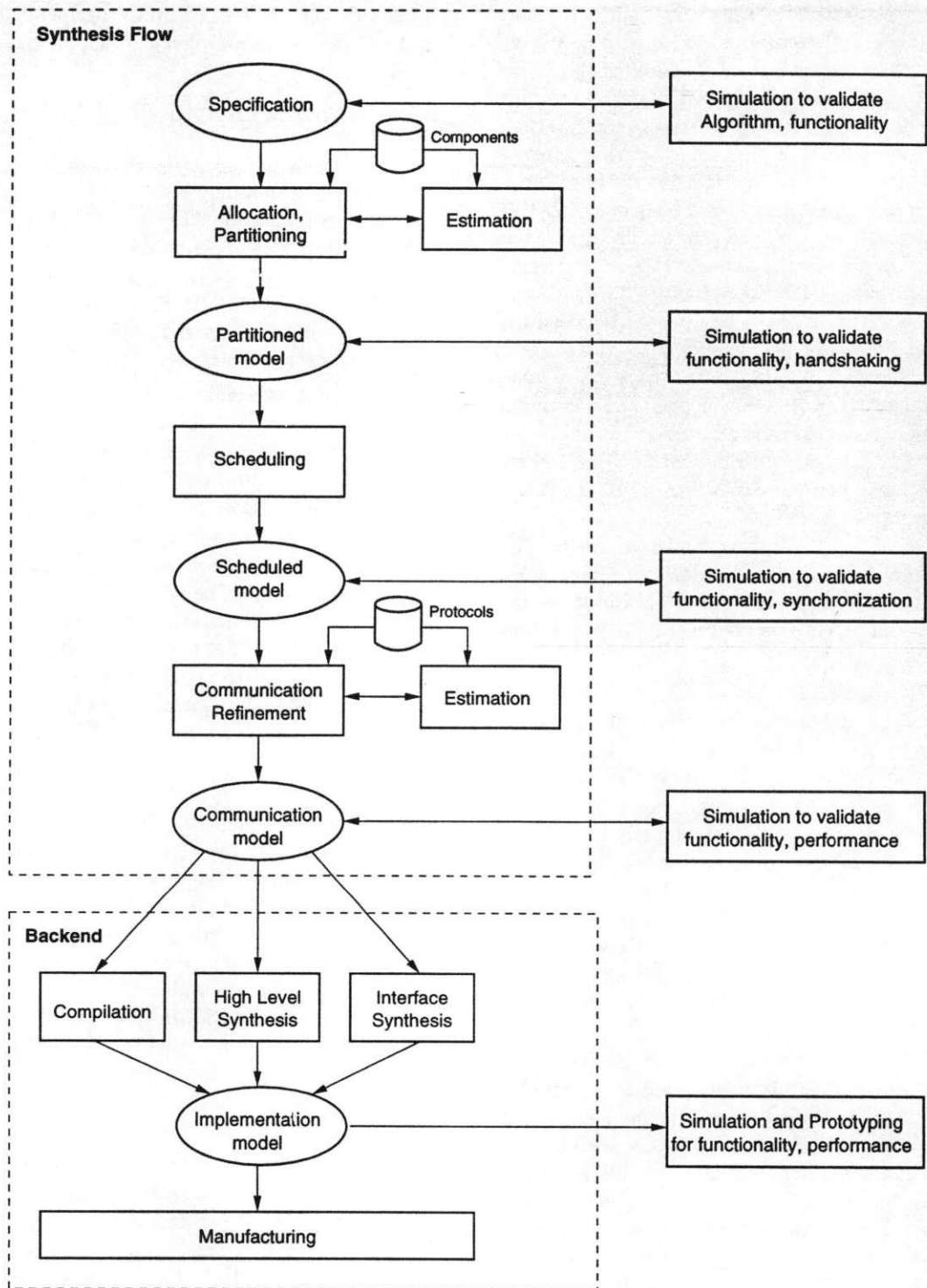


Figure 9: A generic co-design methodology

communication models.

**Direct Connection using a Bus:** In the simplest case, the two ASICs communicate using the same protocol. The components can then be di-

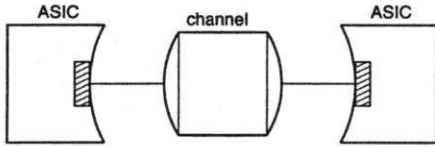


Figure 10: Direct connection of two ASICs

rectly connected to each other using a channel as shown in Figure 10. This channel encapsulates a communication bus like the VME or the PCI or an application specific bus.

**Protocol Translation:** If the ASICs have different protocols for communication, then the protocols need to be translated. This protocol translation is done by a *transducer* as shown in Figure 11. The transducer is basically a finite state machine. It uses a few registers that may be required for protocol translation, e.g., one communication protocol uses a 16-bit wide data bus while the other uses only an 8-bit wide bus. The transducer then uses a register to first read the 16-bit word and then sends out one byte at a time. Another example might be that of a parallel to serial converter using a shift register.

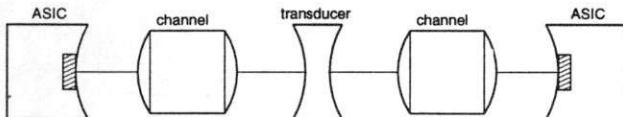


Figure 11: Simple protocol translation

Proper synchronization of the communication components must be ensured for correct results. The rate of data production and consumption may not be identical. If the system specification and implementation guarantee equal production and consumption rates then no translation effort is required. However, if this is not assured then handshaking must be used, e.g., if the producer generates data at a faster rate than used by the consumer, then the producer is restricted to generate the next set of data until it gets an **acknowledge** signal. This signal is given

when the consumer reads the data. Similarly, a faster consumer will wait for a data valid signal from the producer that denotes presence of a new data word. If handshaking signals cannot be used, the data will have to be buffered using other schemes as discussed below.

**FIFO queue:** The ASICs may produce and consume data in a burst mode. In such a case, storing the data in an intermediate buffer may be a better solution than operating the system at the speed of the slowest block. Data can be transferred between the functional blocks using a First-In First-Out (FIFO) queue as shown in Figure 12. There can be two types of interfaces: *blocking*

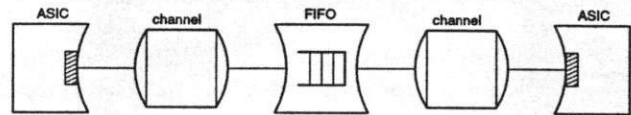


Figure 12: Communication using a FIFO queue

and *non-blocking*. The blocking interface uses **full** and **empty** lines for synchronization. Thus, the producer writes data into the buffer only if the **full** line is low. When the FIFO becomes full, the **full** line is asserted. Similarly, the consumer reads data from the buffer only when the **empty** line is low. This protocol then ensures that the slower component is not overwhelmed with data by the faster one and that no data is lost.

The non-blocking FIFO buffer does not use any extra signals to flag the current status of the buffer. Such an interface is used if the producer-consumer specifications ensure that they synchronize in such a manner that neither is overwhelmed by the other. If this is not possible, the FIFO will need to be large enough. In either case, however, data will be lost if too many burst requests occur.

**Memory buffer:** The inter-component communication can also be done using a random access memory in the interface as shown in Figure 13. An advantage of using memories over FIFO buffers is that they provide random access to the data stored. In the case of FIFOs the consumer must necessarily consume data in the same order as supplied by the producer. The data is removed from the FIFO queue as it is being read

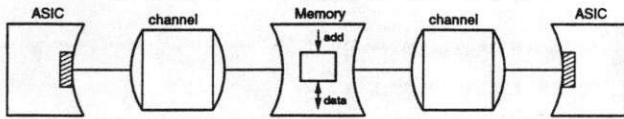


Figure 13: Communication using a memory buffer

by the consumer. Hence, if the consumer needs to use a data-set again, it must be stored internally. On the other hand, the data continues to reside in the memory even after being read so data may be read and written in different order.

The downside of using a memory is the added complexity of addressing. In addition, an arbiter may be required since both components access the memory. The arbiter needs to sequentialize requests that occur at the same time. Multi-ported memories may also be used to service more memory access requests at the same time. A memory is less restrictive than a FIFO because it can be used for bi-directional data transfer. A shared memory can also be used to exchange data amongst more than two ASICs and for multicasting data.

### 3 Modeling DCT as an example

We next describe modeling of Discrete Cosine Transform (DCT) as an illustrative example. Discrete Cosine Transform [2] is widely used in DSP applications for image compression in both still and motion picture standards. The DCT problem can be expressed as follows (details in Appendix A).

$$OutBlock = CosBlock \times InBlock \times CosBlock^T$$

where  $InBlock$  is the input  $8 \times 8$  block of pixels,  $f$ .  $OutBlock$  is the output matrix in the frequency domain  $F$  and  $CosBlock$  is defined above. The DCT can, thus, be modeled as two  $8 \times 8$  matrix multiplications. These matrix multiplications (MM) can be serialized in time.

$$TempBlock = InBlock \times CosBlock^T \quad (MM1)$$

and

$$OutBlock = CosBlock \times TempBlock \quad (MM2)$$

The DCT transformation can then be modeled as two processes. The first process completes the

first matrix multiplication and generates the  $8 \times 8$   $TempBlock$  matrix. The results of this matrix multiplication is then used by the second process that generates the final output matrix,  $OutBlock$ . Both processes have an internal copy of the  $CosBlock$  matrix.

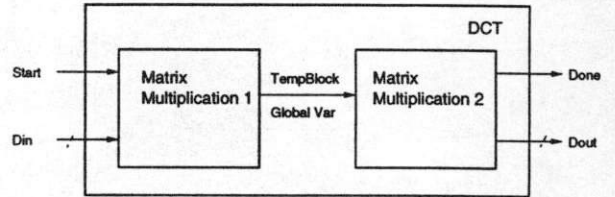


Figure 14: DCT modeled as two serialized matrix multiplications

The DCT can be modeled as two communicating processes as shown in Figure 14. The design of this ASIC, then, includes specifying the protocol of communication between the two processes and synthesizing the communication interface. The high-level *specification* of the problem is given in Appendix B. This high-level specification is partitioned into two processes each performing a single matrix multiplication. This model is shown in Figure 15. At this level of modeling, communication is done through *global variables*. The complete VHDL model is given in Appendix C.

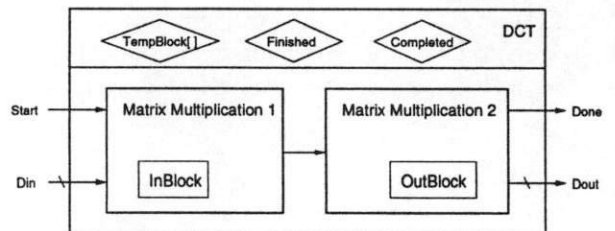


Figure 15: Global variables in the partitioned model

Process 1 reads the input data and stores the results of the first matrix multiplication in the global variable  $TempBlock$  and makes a flag  $Finished$  high to denote that it is done with its computation. This flag is a global variable and hence accessible to the second process also. The second process polls the  $Finished$  flag and when it sees that the first process is over with its computation, it goes ahead and does the second matrix multiplication, sets the  $Completed$  flag and finally puts the results on the output signal pins. Process 1 proceeds only after the second process has read the  $TempBlock$  matrix, i.e. it waits for the  $Completed$  flag

to be set. The *InBlock* and the *OutBlock* matrices are stored in local memories of the first and second processes respectively.

The DCT specification is partitioned into two communicating processes. The first process generates the  $8 \times 8$  *TempBlock* matrix. The 64 bytes of this matrix have to be transferred to the second process for the second matrix multiplication. There are various possible schemes for communicating this set of data. We next explore some of the different styles of model implementation and how components may be reused.

### 3.1 Protocol 1: Handshaking for each byte

We first look at direct communication between the two components without any intermediate storage elements. The two components can communicate using a dedicated bus with handshaking on every byte as shown in Figure 16. This protocol uses four control signals and separate address and data lines. The first process stores the result of the matrix multiplication, *TempBlock*, in local memory. When it is done with the computation, it sends a transmit request signal on TxReq. The second process responds with a TxAck signal. The 64 bytes of data are then transferred over the data bus with handshaking for each byte. The detailed protocol is described below. MM1 is matrix multiplication 1, MM2 is matrix multiplication 2, P1 is process 1 and P2 is process 2.

1. MM1 complete, P1 raises TxReq
2. P2 acknowledges when ready with a high on TxAck
3. P1 raises DReq and waits for ack
4. P2 sends DAck when ready to receive a byte
5. P1 places the address and data and pulls DReq low
6. P2 reads the address and data when DReq goes low
7. P2 pulls DAck low to signal completion of transfer of 1 byte
8. steps 3-7 repeated for a total of 64 times
9. P1 lowers TxReq
10. P2 lowers TxAck

The VHDL model for this protocol is given in Appendix D. This protocol dedicates 4 control signals for synchronization between the processes. The *TempBlock* matrix is duplicated in the two processes. Even though memory is wasted due to duplication and extra time is required for transferring the entire matrix from one block to the other, this might be the only option in certain cases. If the producer and consumer produce and consume data at the same rate, then the consumer need not acknowledge receipt of data. Data may be strobed on every low→high transition of a Req signal or clock. However, if such assumptions about the relative rates cannot be made then the system must be operated at the speed of the slowest component by using request and acknowledge signals.

### 3.2 Protocol 2: Handshaking for every byte-pair

A dedicated bus may use protocols for communication that differ from the one described above. The various parameters in the protocol specification include the number of control wires, if the protocol is synchronous or asynchronous, the clock rate for synchronous protocols, type/width of data/address busses and the exact timing specification. Another protocol for communication over a dedicated bus is shown in Figure 17.

The first process stores the result of the matrix multiplication (*TempBlock*) in local memory. When it is done with the computation, it initiates data transfer with a request on the Req signal. The second process responds with an Ack signal. The 64 bytes of data are transferred over an 8-bit bus with handshake for every two bytes. The protocol can be specified as follows. MM1 is matrix multiplication 1, MM2 is matrix multiplication 2, P1 is process 1 and P2 is process 2.

1. MM1 complete in P1
2. P1 raises Req
3. P2 acknowledges when ready with a high on Ack
4. P1 places the address and pulls Req low at next clock
5. P2 reads the address when Req goes low
6. P1 places data byte on bus at next clock
7. P2 reads the data byte
8. P1 places the next data byte on bus at next clock

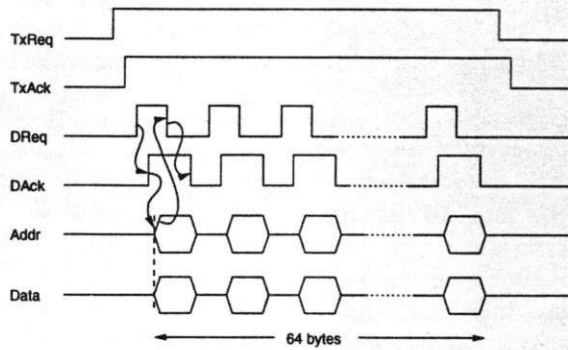
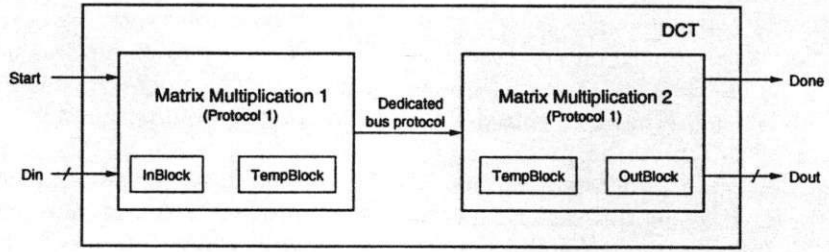


Figure 16: Bus with handshaking for each transmitted byte

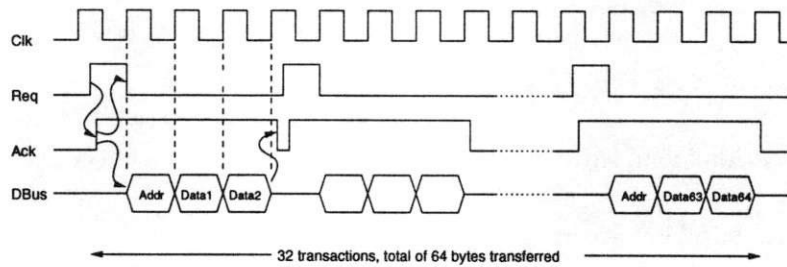
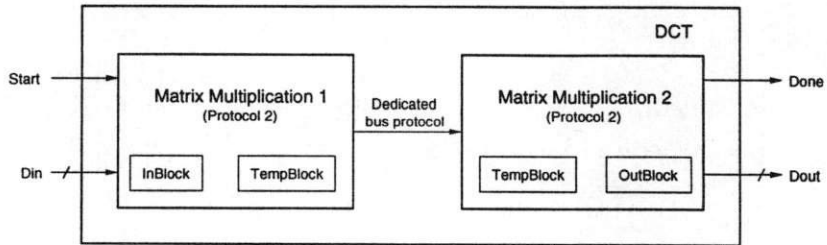


Figure 17: Bus with handshaking for every byte-pair

9. P2 read the data byte and pulls the Ack low
10. steps 2-9 repeated for a total of 32 times

The VHDL model for this protocol is given in Appendix E. This protocol multiplexes address and data on a single bus. The first process places only the even addresses on the bus. It sends out 2 data bytes for each address that it puts on the bus. The model uses only 2 control signals but the data transfer is synchronized with a common clock edge. The second process must count the number of bytes received since there is no transmission request signal. It interprets the first data byte to be for the address supplied and the second data byte for the next contiguous location.

### 3.3 Reusing an ASIC

The various components of a system may not have the same communication protocol. It may not be possible to synthesize the components to obey the protocol of the other component. Communication between components with different protocols for data transfer is a major hurdle in ASIC reuse. If protocols of processes that need to communicate with each other do not match then a proper interface must be generated that translates the protocols. We next describe experiments done on this problem. Consider the DCT system made up of two components that communicate using Protocol 1 (described in Section 3.1). Now, Process 2 which does the second matrix multiplication is removed and replaced by a component that uses Protocol 2 (described in Section 3.2). This is similar to the generic example shown in Figure 3.

Protocol 1 uses 4 control signals and a separate address and data bus. It is a completely asynchronous protocol. Protocol 2, however, uses only 2 control signals and a single bus. The address and data are multiplexed on this bus and two data bytes are transferred for each address put on the bus. After the data transfer cycle has been initiated using the request and acknowledge signals, the two data bytes are strobed on consecutive clock edges. A transducer is required between the two blocks since they do not use the same protocol. The DCT model composed of processes with different protocols is shown in Figure 18. The transducer (interface) needs to generate the proper control signals and do the protocol translation. The exact sequence of steps for the transducer can be listed as follows.

1. wait for the TxReq signal from process 1
2. send the TxAck signal
3. wait for a DReq signal from process 1
4. send the DAck signal
5. wait for DReq to go low
6. read the address and the first data byte from process 1
7. lower the DAck signal
8. wait for the next DReq signal
9. send the DAck signal
10. wait for DReq to go low
11. read the address and the second data byte from process 1
12. send the Req signal to process 2
13. wait for Ack signal from process 2
14. put the first address on bus at the rising edge of clock
15. put the first data byte at the next clock edge
16. put the second data byte at the next clock edge
17. wait until Ack from process 2 goes low
18. lower the DAck signal for process 1
19. repeat steps 3-18 while TxReq is high
20. lower TxAck signal to process 1

The interface, thus, first gets the address and data from the first process according to its protocol. It stores them internally and does not give the final acknowledge signal to the first process. It returns this acknowledgment only when it completes the data transfer to the second process. This way, it needs limited buffering. Other implementations of the interface are also possible. The interface can be modeled as an FSMD as shown in Figure 19. The actions are associated with the edges which represent the state transitions. The complete VHDL code is given in Appendix F.

### 3.4 Replacing the Bus

In the previous section, we discussed replacement of a component with another that has the same functionality but different communication protocol. The communication bus itself may be changed with another that has a different protocol. Consider the DCT



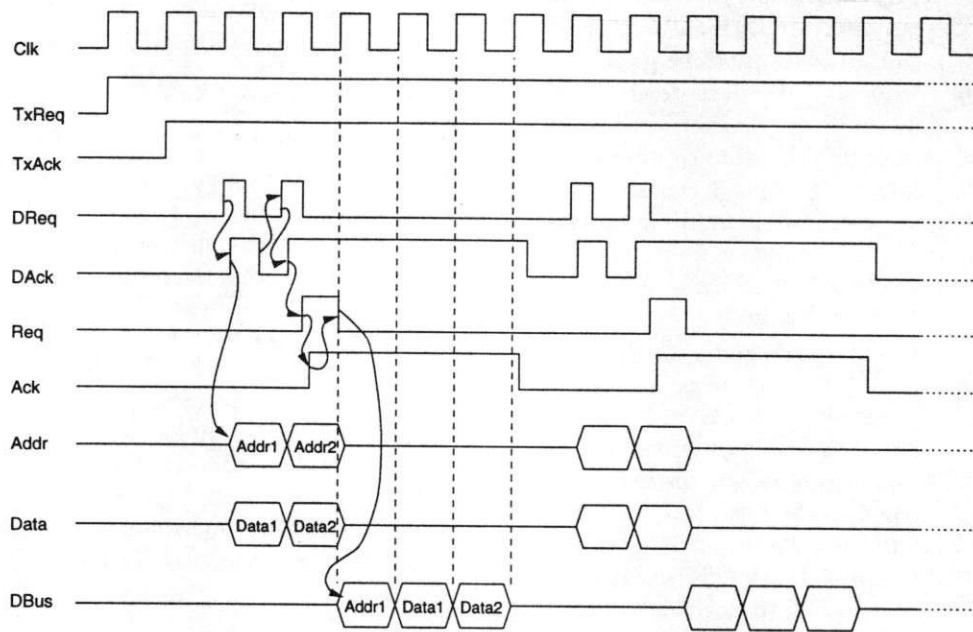
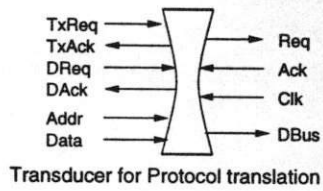
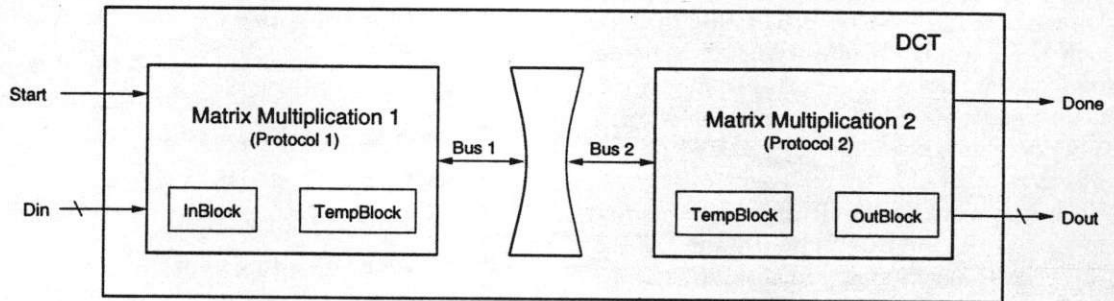


Figure 18: Replacing a component with different protocol

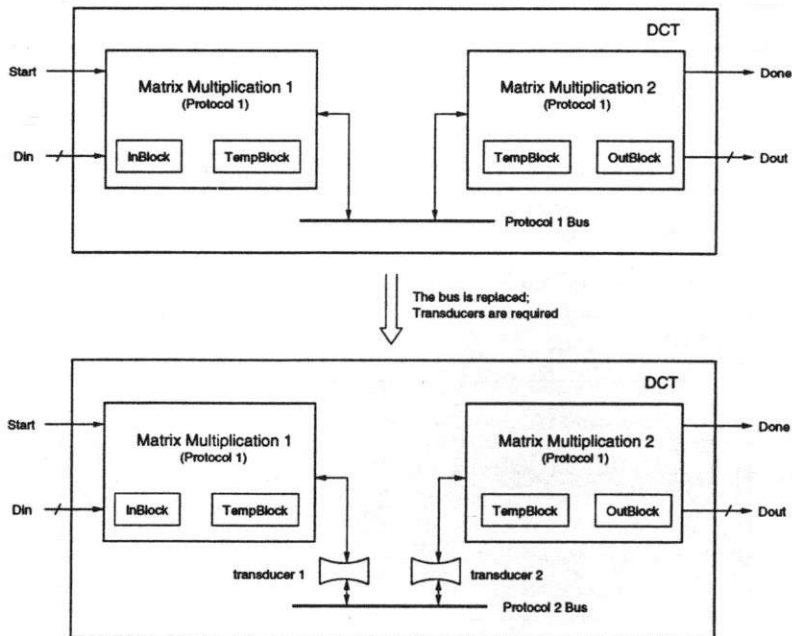


Figure 20: Replacing Protocol 1 bus with Protocol 2 bus in DCT system

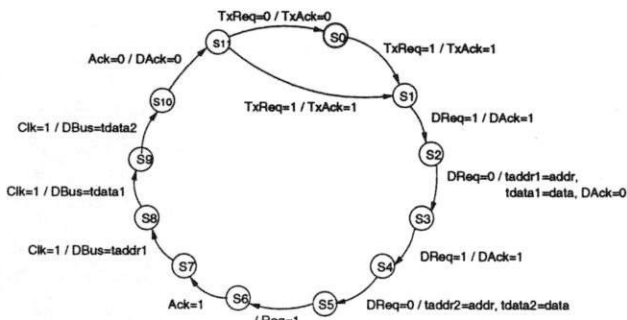


Figure 19: FSM for protocol translation

example where both components use Protocol 1 as described in Section 3.1. The bus used for communication between them is also a Protocol 1 bus. Hence, transducers are not required for connecting the components to the bus as shown in Figure 20. The protocol 1 bus which uses 4 control signals and handshakes on every byte is then replaced by the protocol 2 bus that has only 2 control signals and transfers two data bytes for every handshaking transaction. Two new transducers are needed to translate the protocols and connect the components to the new bus as shown in Figure 20. The complete VHDL model is given in Appendix G.

### 3.5 Communication using a FIFO

In the previous protocols the *TempBlock* matrix was duplicated. Both the matrix multiplication units had a copy of the matrix. The first process, MM1, stored the computed results in a local memory and then transferred the matrix to the second process, MM2, which first saved a copy in local memory and then proceeded with the computation. However, the memory duplication overhead can be avoided by sharing the storage between the two components.

For this example and similar problems, bounded First-in First-out (FIFO) queues can be used as means of communication. FIFOs also avoid the data duplication problem. The advantage of using a FIFO is that the consumer and producer can operate concurrently. It is especially useful when the producer and consumer data at approximately the same rate. The producer and consumer do not require extra bits for addressing. The arbiter which is required for shared memory access (discussed in Section 3.6) is also not required. FIFOs, however, do not provide the random access capability that memories provide. The consumer must read the data in the order in which the producer supplies it. Thus, if the producer does not need to reuse the data it produces, it can immediately transfer it to the queue without storing it in local memory and then

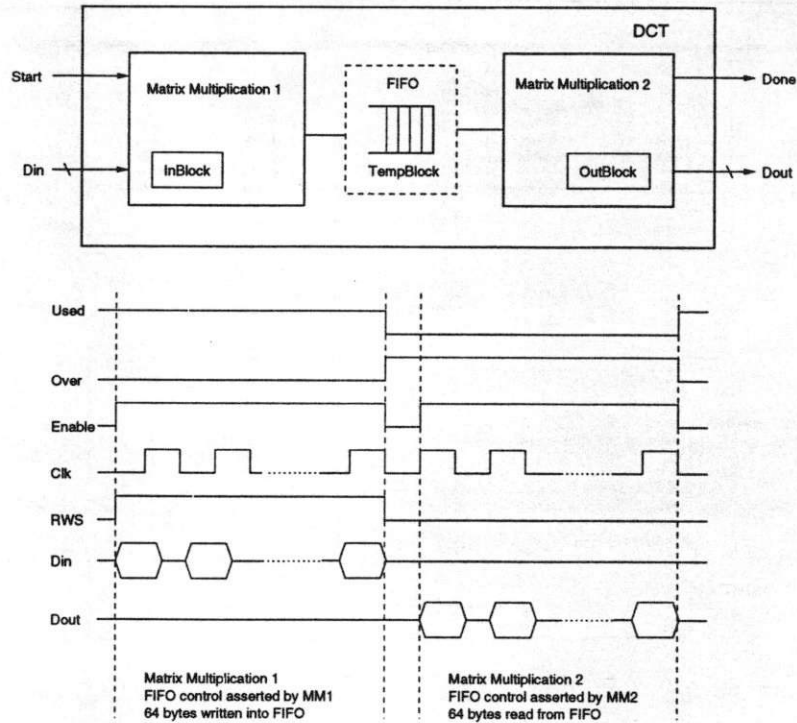


Figure 21: Communication using a FIFO queue

at a later stage reading from there and transferring it. The consumer can read the data from the queue in the first-in first-out discipline.

The protocol for communication using a FIFO is shown in Figure 21. The complete VHDL code is given in Appendix H. The operation is similar to the shared memory protocol. MM1 computes the first matrix multiplication and stores the 64 bytes of data in the FIFO. After the computation is over, it sends an **Over** signal to the other process. MM2 then reads the 64 bytes of data from the FIFO and does the second matrix multiplication. When it is done with the computation, it sends a **Used** signal to MM1 which denotes that MM1 can proceed ahead and do another matrix multiplication.

FIFOs are an efficient way of communicating between two processes. However, reading the data removes it from the queue. Thus, if the consumer needs to access some data repeatedly, it must store it inside. This is not the case for random access memories. The second matrix multiply unit, MM2, needs to use a *TempBlock* byte repeatedly for the matrix multiplication. It must either buffer the bytes internally or use another matrix multiplication algorithm. This al-

gorithm will read a value from the FIFO (an element of the *TempBlock* matrix), performs all the multiplications which require this value and then discards this value. This approach has been adopted in our case. If the size of FIFO is the same as the amount of data to be transferred, then dedicated control lines between the two matrix multiply units are not necessary. The *full* and *empty* lines from the FIFO can be used to synchronize the two processes. If dedicated lines for synchronization are used in conjunction with the *full* and *empty* lines both the blocks may operate concurrently.

### 3.6 Communication using a Memory

The duplication of data and memory in the two components can also be avoided by sharing a memory between the two components. This achieves the same goal as the FIFO in the previous section. In the general case, random access memory and FIFO provide different benefits and have their own limitations.

The protocol for communication using a random access memory with implicit arbitration is demonstrated in Figure 22. The two units do not have local mem-

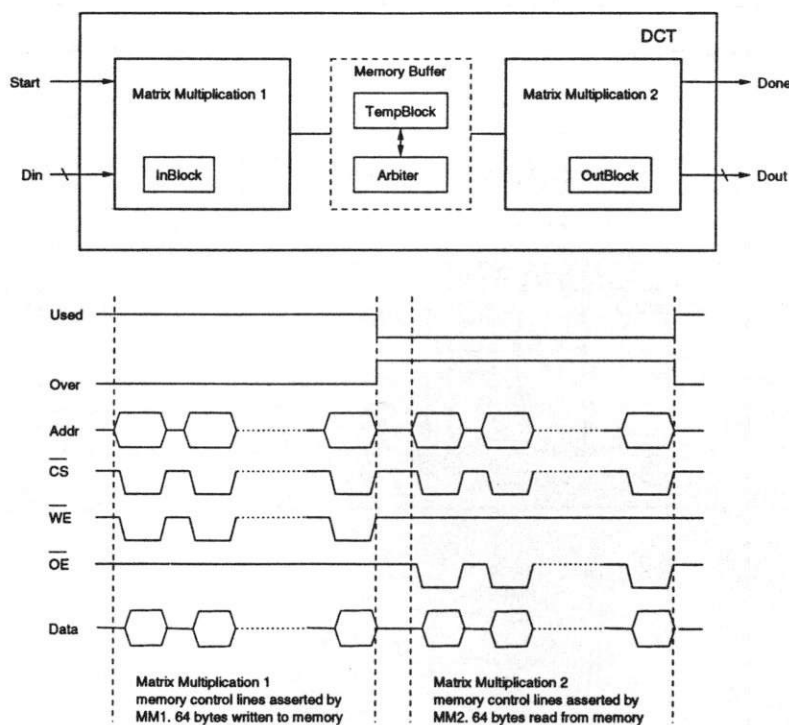


Figure 22: Communication through random access memory

ory for the *TempBlock* matrix. They use a random access memory for storing the matrix. This memory is shared between the two components. During the first half of the computation, the first matrix multiply unit writes into the memory. During this time the address, data and control lines of the memory are asserted by the first matrix multiply unit. MM1 gives the address of the data byte being written and asserts the  $\overline{CS}$  and  $\overline{WE}$  control lines according to the timing diagram of the memory. MM1 send a computation complete signal on the over line to MM2 and relinquishes control of the address and data busses. In the next phase, the second multiply unit, MM2, controls the random access memory after receiving the over signal from MM1. MM2 supplies the address and asserts the  $\overline{CS}$  and  $\overline{OE}$  lines to read the matrix values for the computation. When the computation is over, MM2 relinquishes control of the address bus and floats the CS and OE lines. It then sends a used signal to MM1 which denotes that the data from the random access memory has been read and that MM1 can start the next computation.

A NEC 1 M-bit (128K by 8-bit) CMOS static RAM [5] (part number  $\mu PD431008L$ ) has been used

for modeling the random access memory between the two processes. It has a read-write cycle time of 17 ns. The complete VHDL code is given in Appendix I.

In this case, the arbiter is very simple and its job is to turn around the data busses. The two components do not try to access the memory buffer at the same time. They communicate between themselves using dedicated control lines to make sure that only one unit accesses the memory at a time. This is possible since the matrix multiply processes do not have any interleaved memory accesses. MM2 reads the memory only after MM1 has written all the data into the memory. However, a priority resolution method and recovery method in case of clashes will need to be determined for the general case of accesses to a random access memory. In this example, however, there is no need for the arbiter to acknowledge successful grant of the busses since it is guaranteed that the processes synchronize between themselves and the arbiter does not need to provide this functionality.

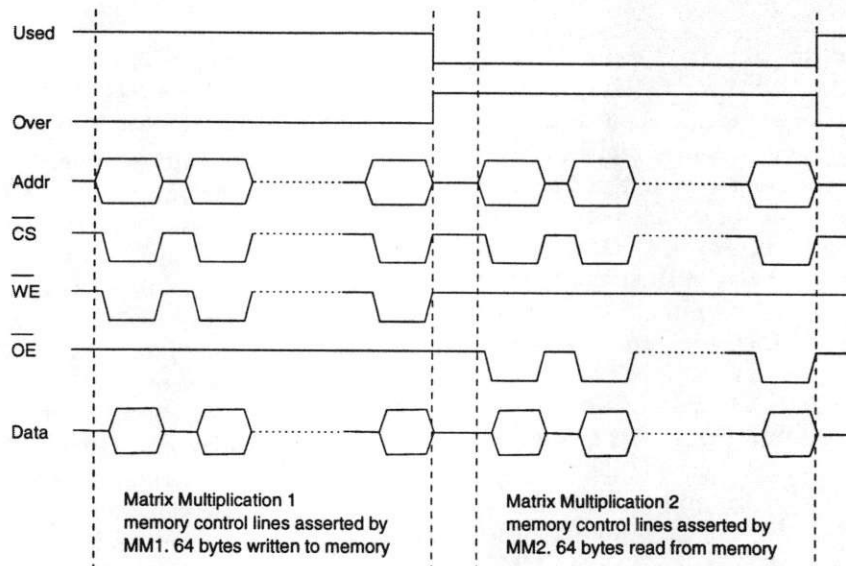
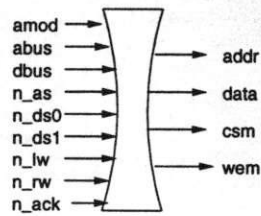
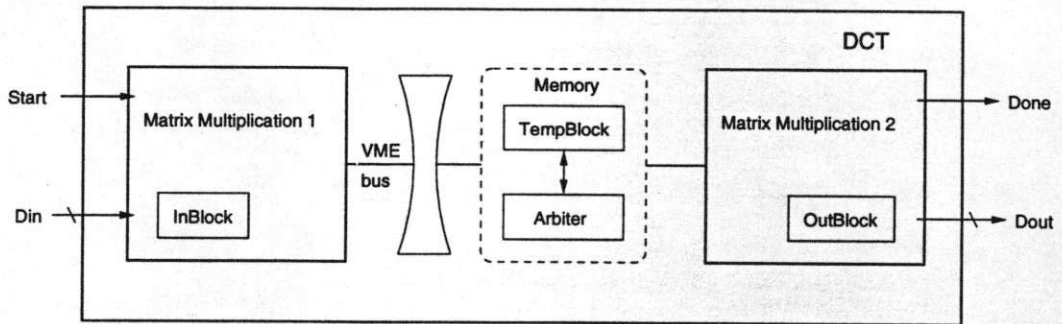


Figure 23: Communication using a Memory and VMEbus

### 3.7 Communication using a Memory buffer and VMEbus

In the previous sections, we have looked at designs that all use dedicated application specific resources. In particular, the communication busses have been all configured to best suit the example in terms of number of control signals and bus widths. However, this kind of facility may not always be available. One or more of the components might have been defined for some particular protocol. There may not be the flexibility of re-designing the entire component for the particular communication scheme. Otherwise, system considerations might force the designer to choose some standard bus for communication even if the components are being synthesized. This section discusses use of a VMEbus [6] as means of communication between a component and the memory.

As shown in Figure 23, the component MM1 is a VME Master component and communicates in the VMEbus protocol. The component writes the *TempBlock* matrix data bytes in the VMEbus protocol. The shared memory, however, is not a VME slave component. Hence, an interface is used between the VMEbus and the SRAM. The interface unit in this case is minimal since the VME master only does single byte transfers on the lower 8 bits of the data bus. There are no double, quad byte or burst mode transfers. It generates the chip select signal from the address strobe signal of the bus and sends an acknowledgment based on the timing characteristics of the SRAM.

Industry standard busses are commonly used for communication between components. If the components cannot be synthesized for the particular bus protocol then transducers (interfaces) must be created for protocol translation. The interface can be quite complicated with internal buffering along with a state machine for generating the proper control signals.

Experimentation with the DCT example has demonstrated the issues in modeling for reuse. We explored different communication schemes between the two components of DCT. We were able to look at the IP reuse problem by changing an ASIC with another that uses a different communication protocol. We also looked at the effect of changing the bus on the system models. These experiments lead us to propose some guidelines for modeling in VHDL which we present next.

## 4 Modeling for Reuse

In this section, we discuss some of the essential issues in modeling for reuse. A system consists of various components that communicate amongst themselves for exchanging data and synchronizing computation. In a hardware system, a component refers to any of the processors, ASICs, FIFOs, random access memories that comprise the system. Thus, it is important to ensure that there is no protocol mismatch amongst the various components. Some of the important issues regarding modeling and implementation of a system are as follows.

- Whenever there is a protocol mismatch between two components or between a component and a bus, a *transducer* must be used for protocol translation. If the ASIC is a synthesizable component then the transducer is not a separate entity but can be integrated with the ASIC during the synthesis process. Otherwise, the transducer will exist as a separate component in the system.
- Whenever a component (ASIC, memory, FIFO) is replaced with another that has a different communication protocol, the existing transducer has to be redesigned. If there was no transducer initially, then a new transducer must be inserted.
- The components might communicate using a common bus. Every time a bus is replaced, all the transducers that are used to connect ASICs to this particular bus will need to be redesigned.

Reuse is encouraged if the ASIC does not have the detailed communication protocol in its description. It is extremely difficult to modify a system model if communication is interleaved with computation. Changing the communication protocols then amounts to rewriting the entire model since the communication steps are distributed all over the model. In addition, it is hard to determine what constitutes internal computation and what constitutes external communication. Thus, reuse is encouraged if communication is separated from computation and is moved outside the component model. If this is done then the port interface of the component model consists of function calls instead of bit signals. This is helpful because the components are generic and not restricted to a particular protocol. They can be stored in a library and generic interfaces also facilitate automatic generation of transducers which is rather hard to do if the interfaces specify timing on bit signals.

## 4.1 Using VHDL as a modeling language

The above mentioned guidelines though highly recommended cannot be put into practice easily when VHDL is used as a modeling language. VHDL is inherently *flat* which means layered protocol specification is not possible. VHDL requires that the **entity** declaration of models be at the bit-level and hence, communication must necessarily be modeled at the physical level, i.e., transitions on signals [7]. But if the communication has to be removed from the component model, then the **entity** interface to the external world will consist of function calls. However, in VHDL an **entity** cannot consist of function calls. It must use the standard data types like **bit**, **integer** or **std\_logic**. The model then also defines the timing specification on these signals. Thus, the interface is *too* detailed and cannot be used for incremental refinement and reuse at the behavioral model.

However, communication can still be separated from computation by using a separate **process** inside the behavioral VHDL **architecture** of the ASIC for just communication. This process encapsulates the entire communication protocol and the computation is done in other processes of the same architecture. The computation processes do not access the **ports** of the **entity**. They request the **communication process** for all read/write requests. This is done using global variables which are essentially **signal** declarations inside the **architecture** of the model. A typical model looks like the one shown in Figure 24.

Now consider replacing an ASIC model with another that uses a different communication protocol. Typically, the entire model for this new ASIC will need to be rewritten to reflect the different protocol. However, now the communication is clearly demarcated and separated from all the computation since it is in a separate process. Thus, only the **communication process** needs to be redesigned and the computation processes do not need to be modified. This modeling technique is illustrated in Appendix D, E.

When an ASIC is replaced with a new ASIC, the VHDL models need to be modified if the communication protocol of the new ASIC is different from the earlier protocol. The **communication process** of either of the two ASICs between which there is a protocol mismatch needs to be modified. The changes must reflect the protocol of the other ASIC. This might also necessitate modifications in the **port** declarations

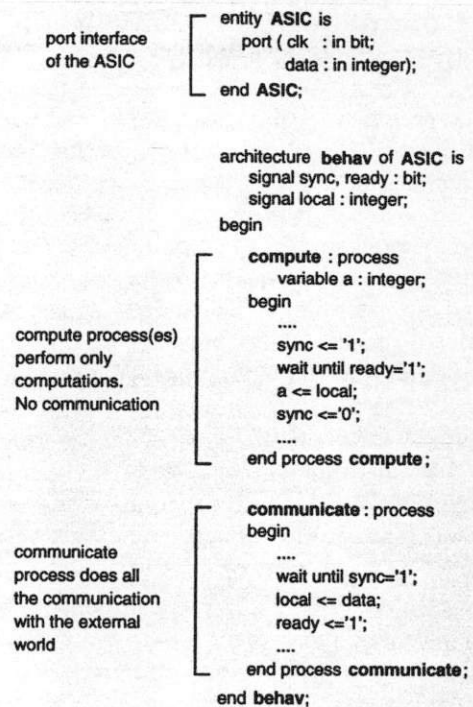


Figure 24: Separate communication and computation processes in VHDL

of the ASIC **entity**. However, if none of the ASIC is synthesizable then the models cannot be changed and a transducer needs to be inserted. This transducer is a separate **entity** which interfaces to the two ASICs. The **architecture** of the transducer has a model for the finite state machine that does the protocol translation as described for the DCT example in Figure 19. When a bus is replaced, then the same procedure needs to be applied for each of the components connected to the bus. If they are not synthesizable then transducers need to be developed and inserted in the top level **entity** that encapsulates all the different components.

The inability to model at a higher level in VHDL leads us to propose the use of the new language, SpecC. SpecC is an executable hardware modeling language suited for co-design and component reuse. In the next section, we discuss the benefits of SpecC and how it supports ASIC reuse.

## 5 Modeling in SpecC

There is a modeling need to separate the computation from communication, as discussed in Section 2.1. The ports of entities can then be made abstract in terms of number and width of signals. A port of a particular type will then be specified by the *function calls* it will support, e.g., `read_word()` and `write_word()`. This port will be resolved to a real channel that has the actual details at the later time of component instantiation. The SpecC language supports these features and makes modeling for reuse a natural and easy task. It is able to separate the computation specification in a component from the communication protocols by using the concept of channels and the software modeling techniques of data abstraction and information hiding.

### 5.1 Modeling Refinement in SpecC

A key feature of the SpecC language is that the designer can model the system at a behavioral level and the models can then be refined for system implementation. We next present how modeling refinement is done in the SpecC methodology.

#### 5.1.1 Global Variables

At the highest level, the models are composed of system behaviors that communicate using *global variables*. This kind of modeling is closer to the conceptual model of the system. There is no notion of ports of sub-behaviors or protocol transfers. It is the simplest model that captures the algorithm being used for solving the problem. The designer is not burdened with communication protocols and target architecture at this stage and uses such a model for verification of the algorithms and functionality of the system under design.

A typical system model at this level is shown in Figure 25. The system behaviors see the communication variables as any other local variable since they are declared as global in the specification.

#### 5.1.2 Global variables through ports

The behaviors may also access the global variables through their ports. This model is shown in Figure 26. This model is in essence the same as the earlier one that uses only global variables. The only difference

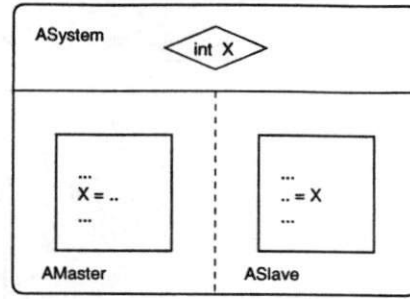


Figure 25: Global variables in a SpecC model

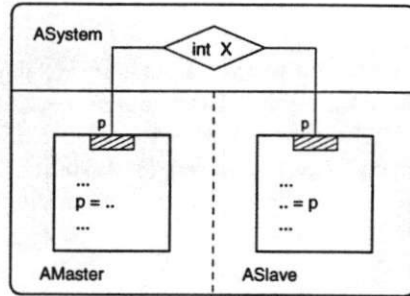


Figure 26: Global variables through ports in a SpecC model

is that in this model, the behaviors explicitly declare the global variables as ports. They access the global variables only through the formal port variable names.

The high level behavioral specification of the system can be composed using either of the two models. They are both at a high level and do not include any notion of communication protocol and channels. This model with ports can be generated automatically from the previous model in a pre-processing step. It is useful to have this model as it clearly defines the interface of a behavior and what variables are internal and what are accessed from outside the system behavior.

#### 5.1.3 Variable inside a channel

The global variable model is refined automatically to a model that includes channels. Each global variable is encapsulated in a channel and the channel defines interfaces for accessing this variable. The behaviors use function calls that are part of the port interface to read and write these variables, as shown in Figure 27.

☞ There is no timing information in either the behavior or the channel. Transfers take place by simply



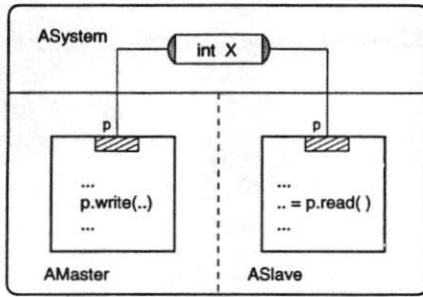


Figure 27: *One-shot transfer* using channels in a SpecC model

reading or writing into the variable inside the channel using the function calls of the interface. This model is used for performing the *allocation, partitioning* and *scheduling* operations required for system implementation as shown in the co-design methodology of Figure 9.

#### 5.1.4 Protocol inside a channel

Allocation and partitioning determine how the system behaviors are mapped and what is the connectivity between components. Channels between behaviors that get mapped to the same component become local variables. The channels then get discarded. The channels going across behaviors on different components are mapped to the common bus that connects the components. A protocol is selected for this bus. The bus is encapsulated in a channel that includes the detailed protocol for the bus. The system behaviors still use function calls for communication as shown in Figure 28.

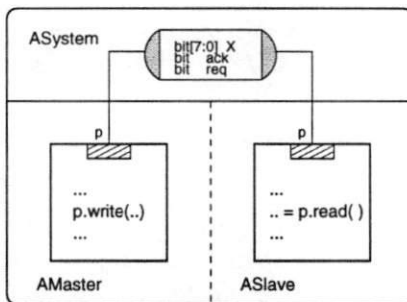


Figure 28: *Protocol transfer* using channels in a SpecC model

The channel has the different bit level signals for

shared variable access like `req`, `ack` and defines the bit-widths and timing of data transfer. These channels encapsulate a particular bus protocol and can be stored in a library. Both the ASICs and the busses can be replaced by new components with different protocols. Reuse is performed at this level and behavioral transducers may have to be introduced.

#### 5.1.5 Inlined channel

After the different options for the components have been explored on the channel model, communication synthesis is done. This process inlines the channel functions to synthesizable ASICs or along with the wrappers as separate components. The refined model again consists of ports that are connected to global variables, as shown in Figure 29.

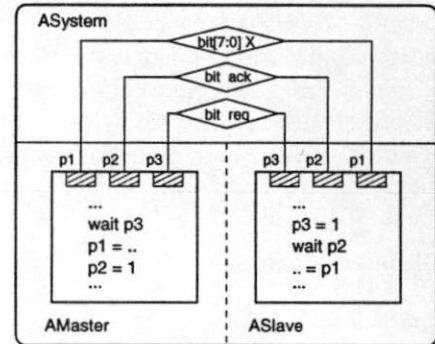


Figure 29: Inlined channel in a SpecC model

This model is, thus, similar to the *global variable through ports* model. However, the important difference is that the model is refined and the ports are now bit signals instead of abstract data types like `int`, `float` etc. The behaviors, too, have the detailed communication protocol that was introduced in them as a result of the inlining process. This model basically consists of a component netlist and can be synthesized using traditional back-end tools.

We next describe some examples in SpecC [4] and how models can be written with desirable features for reuse. We first describe a simple shared variable model and then describe communication over a synchronous bus.

## 5.2 Shared Memory Channel

A shared memory channel which can be accessed by concurrent processes is shown in Figure 30. For the

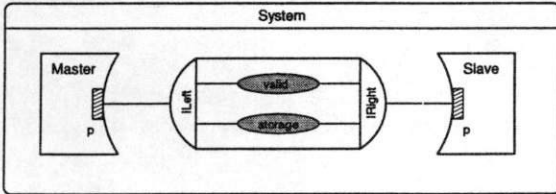


Figure 30: A shared memory channel

sake of simplicity, consider the case when only one of the processes writes into the shared variable and the other reads from it. A typical system using such a shared memory system can be modeled in SpecC as follows (SpecC keywords are in boldface).

```

1 interface ILeft (void) {
2   void write (int val);
3 };
4
5 interface IRight (void) {
6   int read (void);
7 };
8
9 channel CShared (void) implements ILeft, IRight {
10  int storage;
11  bool valid;
12
13  void write (int val) {
14    storage = val;
15    valid = 1;
16  }
17
18  int read (void) {
19    while (!valid);
20    return storage;
21  }
22 };
23
24 behavior Master (ILeft p) {
25   int local;
26
27   void main (void) {
28     ...
29     p.write(local);
30     ...
31   }
32 };
33
34 behavior Slave (IRight p) {
35   int local;
36
37   void main (void) {
38     ...
39     local = p.read();
40     ...

```

```

41   }
42 };
43
44 behavior System () {
45   CShared var;
46
47   Master X (var);
48   Slave Y (var);
49
50   void main (void) {
51     par {
52       X.main();
53       Y.main();
54     }
55   }
56 };

```

The actual variable, **storage**, is encapsulated by the channel **CShared** which also has the synchronization **valid** bit. The write operation stores the value and sets the valid bit and the read operation spin-waits on the valid bit. This simple example brings out the concept of information hiding and how computation is distinguished from the communication. The processes (behaviors) themselves do only the computation and just make function calls to **write()** and **read()** operations. The details of the shared variable access are described in the functions encapsulated in the channel.

The behavior entities have ports in the form of *interfaces*. A channel relates to interfaces by the *implements* keyword by which it is guaranteed that the channel will implement the methods declared in the interfaces that it *implements*. Thus, any other channel that implements the same interfaces **ILeft** and **IRight** can be used in place of the **CShared** channel. This kind of modeling is obviously conducive to reuse of components.

## 5.3 Synchronous Bus Channel

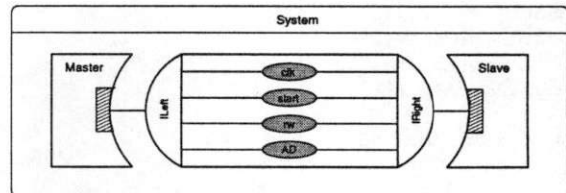


Figure 31: Synchronous bus channel

As a more complex example than shared memory channel consider a synchronous bus channel as shown in Figure 31. This example models read and write of

memory over a bus using a simple synchronous bus protocol which is detailed in Figure 32.

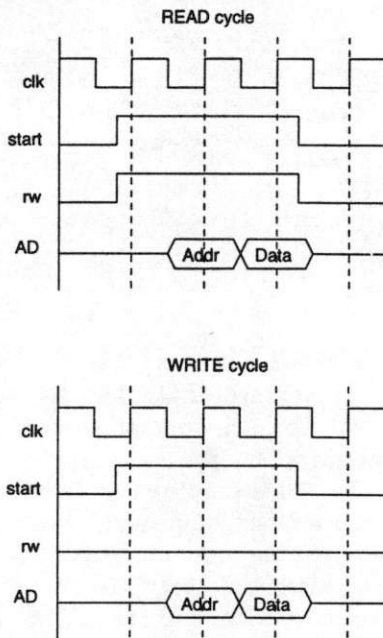


Figure 32: Simple bus protocol

Such a system can be modeled in SpecC as follows (SpecC keywords are in boldface).

```

1 interface ILeft (void) {
2     void read (word addr, word *d);
3     void write (word addr, word d);
4 };
5
6 interface IRight (void) {
7     void monitor(
8         void (*grab)(word addr, word *d),
9         void (*deliver)(word addr, word d));
10 };
11
12 channel CBus (void) implements Ileft, IRight {
13     clock      clk;
14     signal<bit> start;
15     signal<bit> rw;
16     signal<word> AD;
17
18     void read (word addr, word *d) {
19         start=1, rw=1,    clk.tick();
20         AD=addr,         clk.tick();
21         *d=AD, start=0,  clk.tick();
22     }
23
24     void write (word addr, word *d) {
25         start=1, rw=1,    clk.tick();
26         AD=addr,         clk.tick();
27         AD=d, start=0,   clk.tick();
28     }

```

```

29
30 void monitor (
31     void (*grab)(word addr, word *d),
32     void (*deliver)(word addr, word *d)) {
33     word a, d;
34
35     while (start==0) clk.tick();
36     if (rw==1) {
37         clk.tick();
38         a = AD,          clk.tick();
39         (*grab)(a, &d), AD=d,    clk.tick();
40     } else {
41         clk.tick();
42         a = AD,          clk.tick();
43         d=AD, (*deliver)(a, d), clk.tick();
44     }
45 }
46 };
47
48 behavior Master (Ileft bus) {
49     word local;
50
51     void main (void) {
52         ...
53         bus.read(0x10, &local);
54         ...
55         local++;
56         bus.write(0x10, local);
57         ...
58     }
59 };
60
61 behavior Slave (IRight bus) {
62     word storage[0x100];
63
64     void my_grab (word addr, word *d) {
65         *d = storage(addr);
66     }
67     void my_deliver (word addr, word *d) {
68         storage(addr) = d;
69     }
70
71     void main (void) {
72         for (; ; ) {
73             bus.monitor(my_grab, my_deliver);
74         }
75     }
76 };
77
78 behavior System (void) {
79     CBus bus;
80     Master master(bus);
81     Slave slave(bus);
82
83     void main (void) {
84         par {
85             master.main();
86             slave.main();
87         }
88     }
89 };

```

This example again brings out the distinction be-

tween computation and communication achieved in SpecC models. The channel CBus encapsulates the wires in the simple bus, viz., `clk`, `start`, `rw` and `AD`. The interface ports of the components (behaviors) consist of only abstract methods for communication. These methods just specify the behavior that is used by the components. The actual procedure of these methods is moved to the methods in the channel. Thus, the component only needs to make a functional call to methods like `read()` and `write()`. The detailed timing of `clk`, `start` and `rw` signals as specified by the protocol is moved inside the channel.

The ports of the behaviors can be mapped to the channel when they are instantiated. In this way, *late binding* can be achieved. Thus, the behavior need not know what channel it will eventually be mapped to and hence the communication details are removed from the functional specification of the component. This also permits *reuse* because any other channel can be used. The channel can use not only a different timing specification but even with different number of wires. The only requirement is that it should implement the interfaces of the ports of the components.

#### 5.4 Abstraction Levels

The co-design methodology given in Figure 9 uses models at different levels of abstraction. At the highest level, there is a *behavioral specification* of the system in the SpecC language. Allocation and partitioning on this model lead to the *partitioning model*. Scheduling is performed on this model which generates the *scheduling model*. Finally, communication refinement leads to the *communication model*. These abstraction levels are helpful for co-design since the design can be debugged, validated and refined incrementally. Each abstraction level refines the level that is higher in the hierarchy. The different levels are essential for reuse since the final implementation model is too detailed and cannot be easily reused. The rigorous synthesis flow provides models with documentation at higher levels of abstraction which can then be reused.

However, the models at the different level of abstraction have different accuracy. The performance metrics of these models may be quite far from that of the final implementation model. The initial specification is only functionally accurate. The SpecC model can be simulated and validated for correctness of results. There is no implementation detail in this model.

At the next level, the partitioning model includes the software and hardware components of the system. The different behaviors, however, execute concurrently on the processing element on which they are allocated. The performance accuracy at this abstraction level depends on the accuracy of the estimation tools. The performance of the hardware component can be computed approximately but there are no interface models for communication between the components. It is also difficult to get the complete performance estimates for software too because all the software behaviors execute concurrently, contrary to the actual final implementation. However, good estimates for each behavior may be computed separately.

The partitioning model is scheduled which serializes the behaviors on the processing elements. Thus, the software too can be estimated quite accurately. However, the models at this level still do not include the communication details. The communication refinement step introduces protocol transducers, communication primitives and inlines the channel methods. The communication model is, thus, complete in terms of specification of the final implementation. The performance is still not accurate because there is scope for optimizations during high level synthesis and compilation.

The software component of the communication model is compiled and the hardware component is synthesized using HLS tools and techniques. Cycle-based simulators and instruction set simulators can be used to validate the design and estimate the performance. The design may also be prototyped using FPGAs. The implementation model is then quite close to the final manufactured component and the performance of the prototype with appropriate estimators may be accurate enough for most purposes.

We note that even though the performance accuracy of models at higher abstraction levels is not high, the hierarchy is still acceptable. This is because the fidelity [8] of the estimators is usually high. Thus, experience with the estimator tools can be used to get better performance accuracy than suggested by preliminary estimates.

#### 5.5 Proposed "Co-design Explorer"

We propose to develop and implement a co-design system, the "*Co-design Explorer*" [9]. This system will be based on the new SpecC language [3]. SpecC is able to

model mixed abstraction levels as discussed earlier. It can also capture the characteristic features of embedded systems [8], such as concurrency, state transitions, structural and behavioral hierarchy, exception handling, timing, communication and synchronization.

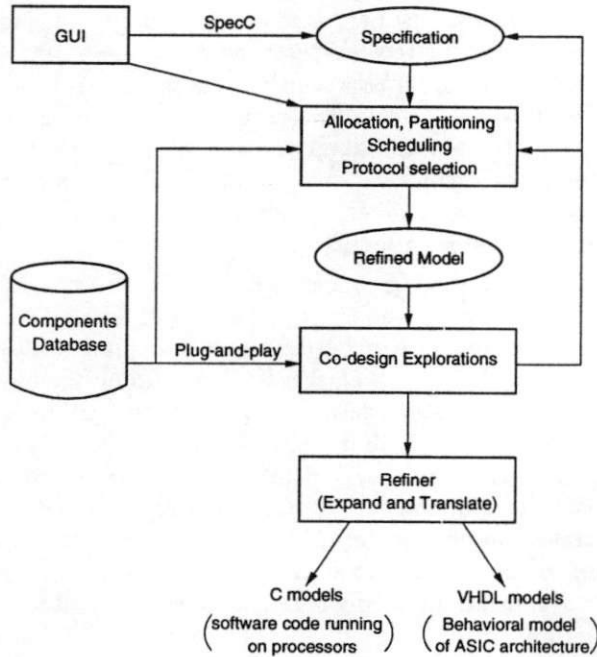


Figure 33: Proposed *Co-design Explorer* System

This system will be based on the co-design methodology presented in Figure 9 and use the *channel* concept illustrated in Figure 5, 7, 8. An overview of the system is given in Figure 33. A graphical user interface (GUI) is used to generate the specification of the system without learning SpecC. The GUI helps in specifying hierarchical and concurrent behaviors. It can be used for specifying the state transition functions and connectivity of behaviors. The GUI generates a specification of the system in SpecC. This model uses global variables for communication as shown in Figure 25. It is internally pre-processed to convert global variables into channels. This model is then be used for manual allocation, partitioning and scheduling with assistance from estimator tools. *Plug-and-play* is performed on the refined model using components from a database. The database also stores generic transducers and busses encapsulated in channels. Explorations are done to meet the performance and cost requirements.

Finally, a *Refiner* tool is used to expand and trans-

late the model generated after explorations. This step includes channel inlining (as discussed in Section 2.1), generation of C code that will run on processors and generation of VHDL behavioral models for the hardware architecture. These low level models can then be compiled and synthesized using traditional techniques to get the implementation model. The advantage of using this methodology is that it uses SpecC which provides a minimal and complete set of constructs required to model embedded systems at various abstraction levels. Furthermore, the designer does not have to know the intricacies of hardware modeling as the graphical user interface can be used to specify hierarchy, concurrency, timing and state transitions.

## 6 Conclusion

In this report, we have outlined a generic co-design methodology that supports component reuse. We have talked about the various steps in the methodology and discussed the step of communication synthesis in detail. We stress that computation needs to be separated from communication. This distinction needs to be made to generate reusable components. This is because then only the communication part needs to be re-designed. Separation can be achieved by declaring the ports of the component at levels higher than bit signals. The protocol can be abstracted away into the channels used for connecting components.

We have also described different communication models and done explorations using different communication protocols between two components that as a system compute the Discrete Cosine Transform. It is important that all communicating processes use the same protocol. If a component uses a different protocol then a transducer must be used between the components. This transducer will do the protocol translation. The transducer will, in general, be complicated and may have internal buffering of data and ensure correct timing of signals.

Using this exploratory example, we have come up with a set of guidelines for modeling in VHDL. Our critique of VHDL led us to propose the use of the new co-design language, SpecC. We have described some examples from SpecC which support its use for ASIC reuse and incremental refinement. We need to do more research to solve the open problems related to ASIC reuse and use of SpecC. As future work, we need to implement the DCT example at various abstraction

levels in SpecC to evaluate the effectiveness of proposed modeling techniques. We also need to compile a list of all possible transaction level function calls in order to study their effect on development of channels and generic transducers. Finally, we propose to develop a new *Co-design Explorer* using the concepts developed.

## Acknowledgements

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## A Formal Specification of DCT

The formal specification of the Discrete Cosine Transform (DCT) operation is as follows [2].

$$F_{uv} = \frac{c(m)c(n)}{4} \sum_{m=0}^{N-1} \sum_{n=0}^{N-1} f_{mn} \cos \frac{(2m+1)u\pi}{2N} \cos \frac{(2n+1)v\pi}{2N}$$

where:

$f_{mn}$  = gray level of pixel at  $(m, n)$  in the  $N \times N$  image ( $0 \leq m, n \leq N - 1$ )

$u, v$  = discrete frequency variables ( $0 \leq u, v \leq N-1$ )

$F_{uv}$  = coefficient at point  $(u, v)$  in spatial frequency domain

In typical designs (like the MPEG standard), the image is sub-divided into  $8 \times 8$  blocks of pixels. We also use a value of  $N = 8$  in this example. Furthermore, let *CosBlock* be a  $8 \times 8$  matrix defined by

$$CosBlock_{un} = round(factor * (\frac{1}{8} \cos \frac{(2n+1)u\pi}{16}))$$

An important property of the cosine transform is that the two summations are separable. Thus, the DCT can be expressed as two matrix multiplications, one after the other.

$$TempBlock = InBlock \times CosBlock^T \quad (MM1)$$

and

$$OutBlock = CosBlock \times TempBlock \quad (MM2)$$

## B High-level Specification of DCT

The high-level specification of the DCT algorithm in VHDL is given below. The incoming matrix is first read into the *InBlock* matrix. The first matrix multiplication generates the *TempBlock* matrix using the *InBlock* and *CosBlock* matrices. The second matrix multiplication generates the *OutBlock* matrix using the *CosBlock* and *TempBlock* matrices. Finally the outgoing transform matrix is written out.

```
1
2 --- Rockwell ASIC Reuse Modeling Project
3 --- Oct 23, 1997
4 ---
5 --- High Level specification of the DCT component
6 --- behavioral level model with only one process
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity dct is
12   port (
13     start : in std_logic;
14     clk   : in std_logic;
15     din   : in integer;
16     done  : out std_logic;
17     dout  : out integer);
18 end dct;
19
20 architecture behavior of dct is
21 begin
22   process
23     type mem is array (0 to 7, 0 to 7) of integer;
24     variable InBlock, TempBlock, OutBlock : mem;
25     variable CosBlock : mem :=
26       ((125, 122, 115, 103, 88, 69, 47, 24),
27        (125, 103, 47, -24, -88, -122, -115, -69),
28        (125, 69, -47, -122, -88, 24, 115, 103),
29        (125, 24, -115, -69, 88, 103, -47, -122),
30        (125, -24, -115, 69, 88, -103, -47, 122),
31        (125, -69, -47, 122, -88, -24, 115, -103),
32        (125, -103, 47, 24, -88, 122, -115, 69),
33        (125, -122, 115, -103, 88, -69, 47, -24));
34     variable a, b, p, sum : integer;
35   begin
36     wait until start = '1';
37
38     -----
39     --- read the input data matrix
40     -----
41     for i in 0 to 7 loop
42       for j in 0 to 7 loop
43         wait until clk = '1';
44         InBlock (i, j) := din;
45       end loop;
46     end loop;
47
48     -----
```



```

49  -- matrix multiplication 1
50  -----
51  for i in 0 to 7 loop
52      for j in 0 to 7 loop
53          for k in 0 to 7 loop
54              a := InBlock (i, k);
55              b := CosBlock (j, k);
56              p := a * b;
57              if (k = 0) then
58                  sum := p;
59              else
60                  sum := sum + p;
61              end if;
62              if (k = 7) then
63                  TempBlock (i, j) := sum;
64              end if;
65          end loop;
66      end loop;
67  end loop;
68
69  -----
70  -- matrix multiplication 2
71  -----
72  for i in 0 to 7 loop
73      for j in 0 to 7 loop
74          for k in 0 to 7 loop
75              a := TempBlock (k, j);
76              b := CosBlock (i, k);
77              p := a * b;
78              if (k = 0) then
79                  sum := p;
80              else
81                  sum := sum + p;
82              end if;
83              if (k = 7) then
84                  OutBlock (i, j) := sum;
85              end if;
86          end loop;
87      end loop;
88  end loop;
89
90  -----
91  -- output the matrix
92  -----
93  done <= '1';
94  for i in 0 to 7 loop
95      for j in 0 to 7 loop
96          wait until clk = '1';
97          dout <= OutBlock (i, j);
98      end loop;
99  end loop;
100 done <= '0';
101 end process;
102 end behavior;

```

## C Partitioned model for DCT with global variables

```
1
2 -- Rockwell ASIC Reuse Modeling Project
3 -- Oct 25, 1997
4
5 -- DCT example with 2 components for the 2 matrix multiplications
6 -- The two components communicate using global variables
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity dct is
12     port ( start : in std_logic;
13           clk : in std_logic;
14           din : in integer;
15           done : out std_logic;
16           dout : out integer);
17 end dct;
18
19 architecture beh of dct is
20     type mem is array (0 to 7, 0 to 7) of integer;
21     signal tempblock : mem;
22     signal finish : std_logic;
23     signal cosblock : mem :=
24         ((125, 122, 115, 103, 88, 69, 47, 24),
25          (125, 103, 47, -24, -88, -122, -115, -69),
26          (125, 69, -47, -122, -88, 24, 115, 103),
27          (125, 24, -115, -69, 88, 103, -47, -122),
28          (125, -24, -115, 69, 88, -103, -47, 122),
29          (125, -69, -47, 122, -88, -24, 115, -103),
30          (125, -103, 47, 24, -88, 122, -115, 69),
31          (125, -122, 115, -103, 88, -69, 47, -24));
32 begin
33     mml : process
34         variable inblock : mem;
35         variable a, b, p, sum : integer;
36     begin
37         wait until start = '1';
38         finish <= '0';
39         -- read the input data matrix
40         for i in 0 to 7 loop
41             for j in 0 to 7 loop
42                 wait until clk = '1';
43                 inblock (i, j) := din;
44             end loop;
45         end loop;
46
47         -- do the computation
48         for i in 0 to 7 loop
49             for j in 0 to 7 loop
50                 for k in 0 to 7 loop
51                     a := inblock (i, k);
52                     b := cosblock (j, k);
53                     p := a * b;
```

```

54
55         if (k = 0) then
56             sum := p;
57         else
58             sum := sum + p;
59         end if;
60
61         if (k = 7) then
62             tempblock (i, j) <= sum;
63         end if;
64     end loop;
65 end loop;
66 end loop;
67
68     -- done with the computation, make finish true
69     finish <= '1';
70 end process;
71
72 mm2 process
73     variable outblock : mem;
74     variable a, b, p, sum : integer;
75 begin
76     wait until finish = '1';
77     -- do the computation
78     for i in 0 to 7 loop
79         for j in 0 to 7 loop
80             for k in 0 to 7 loop
81                 a := tempblock (k, j);
82                 b := cosblock (i, k);
83                 p := a * b;
84
85                 if (k = 0) then
86                     sum := p;
87                 else
88                     sum := sum + p;
89                 end if;
90
91                 if (k = 7) then
92                     outblock (i, j) := sum;
93                 end if;
94             end loop;
95         end loop;
96     end loop;
97
98     -- give the done signal and output the output matrix
99     done <= '1';
100    for i in 0 to 7 loop
101        for j in 0 to 7 loop
102            wait until clk = '1';
103            dout <= outblock (i, j);
104        end loop;
105    end loop;
106    done <= '0';
107 end process;
108 end beh;

```

## D Protocol 1: Handshaking for each byte transfer

```
1
2 --- Rockwell ASIC Reuse Modeling Project
3 --- Oct 30, 1997
4 ---
5 --- DCT example with 2 components for the 2 matrix multiplications
6 --- communication over a dedicated bus with handshaking for each byte
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10 use ieee.std_logic_arith.all;
11
12 entity mml is
13     port ( start : in std_logic;
14           clk : in std_logic;
15           din : in std_logic_vector(7 downto 0);
16           txreq : out std_logic;
17           txack : in std_logic;
18           dreq : out std_logic;
19           dack : in std_logic;
20           addr : out std_logic_vector(5 downto 0);
21           data : out std_logic_vector(7 downto 0));
22 end mml;
23
24 architecture behav of mml is
25     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
26     signal InBlock, TempBlock : mem;
27     signal ready, over : std_logic;
28 begin
29     compute: process
30         variable cosblock : mem := (
31             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
32             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
33             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
34             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
35             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
36             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
37             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
38             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
39         );
40         variable a, b : std_logic_vector(7 downto 0);
41         variable p, sum : std_logic_vector(15 downto 0);
42     begin
43         wait until ready = '1';
44         over <= '0';
45
46         -- first matrix multiplication calculation
47         for i in 0 to 7 loop
48             for j in 0 to 7 loop
49                 for k in 0 to 7 loop
50                     a := InBlock (i, k);
51                     b := CosBlock (j, k);
52                     p := signed(a) * signed(b);
53
```

```

54         if (k = 0) then
55             sum := p;
56         else
57             sum := signed(sum) + signed(p);
58         end if;
59
60         if (k = 7) then
61             TempBlock (i, j) <= sum(15 downto 8);
62         end if;
63     end loop;
64 end loop;
65 end loop;
66
67     -- done with the computation
68     over <= '1';
69 end process compute;
70
71 communicate: process
72 begin
73     ready <= '0';
74     wait until start = '1';
75     txreq <= '0';
76     dreq <= '0';
77
78     -- read the input data matrix
79     for i in 0 to 7 loop
80         for j in 0 to 7 loop
81             wait until clk = '1';
82             InBlock (i, j) <= din;
83         end loop;
84     end loop;
85     ready <= '1';
86
87     -- transfer the data
88     wait until over = '1';
89     ready <= '0';
90     txreq <= '1';
91     wait until txack = '1';
92
93     for i in 0 to 7 loop
94         for j in 0 to 7 loop
95             wait until clk = '1';
96             dreq <= '1';
97             wait until dack = '1';
98             addr <= conv_std_logic_vector(8*i+j, 6);
99             data <= tempblock (i, j);
100            dreq <= '0' after 3 ns; --mem read time
101            wait until dack = '0';
102        end loop;
103    end loop;
104    txreq <= '0';
105 end process communicate;
106 end behav;
107
108 library ieee;

```

```

109 use ieee . std_logic_1164 . all ;
110 use ieee . std_logic_arith . all ;
111
112 entity mm2 is
113     port ( done : out std_logic ;
114           clk : in std_logic ;
115           data : in std_logic_vector(7 downto 0) ;
116           addr : in std_logic_vector(5 downto 0) ;
117           txreq : in std_logic ;
118           txack : out std_logic ;
119           dreq : in std_logic ;
120           dack : out std_logic ;
121           dout : out std_logic_vector(7 downto 0) ) ;
122 end mm2 ;
123
124 architecture behav of mm2 is
125     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0) ;
126     signal TempBlock, OutBlock : mem ;
127     signal ready, over : std_logic ;
128 begin
129     compute : process
130         variable CosBlock : mem := (
131             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
132             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
133             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
134             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
135             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
136             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
137             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
138             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
139         ) ;
140         variable a, b : std_logic_vector(7 downto 0) ;
141         variable p, sum : std_logic_vector(15 downto 0) ;
142     begin
143         wait until ready = '1' ;
144         over <= '0' ;
145
146         -- second matrix multiplication computation
147         for i in 0 to 7 loop
148             for j in 0 to 7 loop
149                 for k in 0 to 7 loop
150                     a := TempBlock (k, j) ;
151                     b := CosBlock (i, k) ;
152                     p := signed(a) * signed(b) ;
153
154                     if (k = 0) then
155                         sum := p ;
156                     else
157                         sum := signed(sum) + signed(p) ;
158                     end if ;
159
160                     if (k = 7) then
161                         OutBlock (i, j) <= sum(15 downto 8) ;
162                     end if ;
163                 end loop ;
164             end loop ;
165         end loop ;

```

```

164         end loop;
165     end loop;
166
167     -- over with the computation
168     over <= '1';
169 end process compute;
170
171 communicate: process
172     variable tempi, tempj : integer;
173 begin
174     txack <= '0';
175     dack <= '0';
176     done <= '0';
177     wait until txreq = '1';
178     wait until clk = '1';
179     txack <= '1' after 1 ns;
180
181     while (txreq = '1') loop
182         wait until (dreq = '1' OR txreq = '0');
183         if (txreq = '1') then
184             dack <= '1' after 1 ns;
185             wait until dreq = '0';
186             tempi := conv_integer(unsigned(addr)) / 8;
187             tempj := conv_integer(unsigned(addr)) mod 8;
188             TempBlock (tempi, tempj) <= data;
189             dack <= '0' after 8 ns; --mem write time
190         end if;
191     end loop;
192
193     wait until clk = '1';
194     txack <= '0';
195     ready <= '1';
196
197     -- output the computed matrix
198     wait until over = '1';
199     ready <= '0';
200
201     done <= '1';
202     for i in 0 to 7 loop
203         for j in 0 to 7 loop
204             wait until clk = '1';
205             dout <= OutBlock (i, j);
206         end loop;
207     end loop;
208     done <= '0';
209 end process communicate;
210 end behav;
211
212 library ieee;
213 use ieee.std_logic_1164.all;
214
215 entity dct is
216     port ( start : in  std_logic;
217           clk   : in  std_logic;
218           din   : in  std_logic_vector(7 downto 0);

```

```

219     done : out std_logic;
220     dout : out std_logic_vector(7 downto 0);
221 end dct;
222
223 architecture struct of dct is
224     component mml
225     port ( start : in std_logic;
226           clk : in std_logic;
227           din : in std_logic_vector(7 downto 0);
228           txreq : out std_logic;
229           txack : in std_logic;
230           dreq : out std_logic;
231           dack : in std_logic;
232           addr : out std_logic_vector(5 downto 0);
233           data : out std_logic_vector(7 downto 0));
234     end component;
235
236     component mm2
237     port ( done : out std_logic;
238           clk : in std_logic;
239           data : in std_logic_vector(7 downto 0);
240           addr : in std_logic_vector(5 downto 0);
241           txreq : in std_logic;
242           txack : out std_logic;
243           dreq : in std_logic;
244           dack : out std_logic;
245           dout : out std_logic_vector(7 downto 0));
246     end component;
247
248     signal txreq, txack, dreq, dack : std_logic;
249     signal data : std_logic_vector(7 downto 0);
250     signal addr : std_logic_vector (5 downto 0);
251 begin
252     u1 : mml
253     port map (start, clk, din, txreq, txack, dreq, dack, addr, data);
254
255     u2 : mm2
256     port map (done, clk, data, addr, txreq, txack, dreq, dack, dout);
257 end struct;

```



## E Protocol 2: Handshaking for each byte pair

```
1
2 --- Rockwell ASIC Reuse Modeling Project
3 --- Nov 6, 1997
4 ---
5 --- DCT example with 2 components for the 2 matrix multiplications
6 --- components communicate using a dedicated bus and handshaking
7 --- bus multiplexed between address and data. 2 bytes of data for
8 --- each address written on bus.
9
10 library ieee;
11 use ieee.std_logic_1164.all;
12 use ieee.std_logic_arith.all;
13
14 entity mml is
15     port ( start : in  std_logic;
16           clk   : in  std_logic;
17           din   : in  std_logic_vector(7 downto 0);
18           dreq  : out std_logic;
19           dack  : in  std_logic;
20           dbus  : out std_logic_vector(7 downto 0));
21 end mml;
22
23 architecture behav of mml is
24     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
25     signal InBlock, TempBlock : mem;
26     signal ready, over : std_logic;
27 begin
28     compute: process
29         variable cosblock : mem := (
30             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
31             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
32             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
33             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
34             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
35             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
36             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
37             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
38         );
39         variable a, b : std_logic_vector(7 downto 0);
40         variable p, sum : std_logic_vector(15 downto 0);
41     begin
42         wait until ready = '1';
43         over <= '0';
44
45         --- first matrix multiplication computation
46         for i in 0 to 7 loop
47             for j in 0 to 7 loop
48                 for k in 0 to 7 loop
49                     a := InBlock(i, k);
50                     b := CosBlock(j, k);
51                     p := signed(a) * signed(b);
52
53                     if (k = 0) then
```

```

54         sum := p;
55     else
56         sum := signed(sum) + signed(p);
57     end if;
58
59     if (k = 7) then
60         TempBlock (i, j) <= sum(15 downto 8);
61     end if;
62     end loop;
63 end loop;
64 end loop;
65
66 -- computation over
67 over <= '1';
68 end process compute;
69
70 communicate: process
71 begin
72     ready <= '0';
73     wait until start = '1';
74     dreq <= '0';
75     dbus <= (others => 'Z');
76
77 -- read the input data matrix
78 for i in 0 to 7 loop
79     for j in 0 to 7 loop
80         wait until clk = '1';
81         InBlock (i, j) <= din;
82     end loop;
83 end loop;
84 ready <= '1';
85
86 -- transfer the data
87 wait until over = '1';
88 ready <= '0';
89 wait until clk = '1';
90 for i in 0 to 7 loop
91     for j in 0 to 3 loop
92         dreq <= '1' after 2 ns;
93         wait until dack = '1';
94         wait until clk = '1';
95         dbus <= conv_std_logic_vector(8*i+2*j, 8);
96         dreq <= '0';
97         wait until clk = '1';
98         dbus <= tempblock (i, 2*j);
99         wait until clk = '1';
100        dbus <= tempblock (i, 2*j+1);
101        wait until clk = '1';
102        dbus <= (others => 'Z');
103        wait until dack = '0';
104    end loop;
105 end loop;
106 end process communicate;
107 end behav;
108

```

```

109 library ieee;
110 use ieee.std_logic_1164.all;
111 use ieee.std_logic_arith.all;
112
113 entity mm2 is
114     port ( done : out std_logic;
115           clk : in std_logic;
116           dbus : in std_logic_vector(7 downto 0);
117           dreq : in std_logic;
118           dack : out std_logic;
119           dout : out std_logic_vector(7 downto 0));
120 end mm2;
121
122 architecture behav of mm2 is
123     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
124     signal TempBlock, OutBlock : mem;
125     signal ready, over : std_logic;
126 begin
127     compute: process
128         variable cosblock : mem := (
129             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
130             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
131             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
132             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
133             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
134             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
135             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
136             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
137         );
138         variable a, b : std_logic_vector(7 downto 0);
139         variable p, sum : std_logic_vector(15 downto 0);
140     begin
141         wait until ready = '1';
142         over <= '0';
143
144         -- second matrix multiplication computation
145         for i in 0 to 7 loop
146             for j in 0 to 7 loop
147                 for k in 0 to 7 loop
148                     a := TempBlock(k, j);
149                     b := CosBlock(i, k);
150                     p := signed(a) * signed(b);
151
152                     if (k = 0) then
153                         sum := p;
154                     else
155                         sum := signed(sum) + signed(p);
156                     end if;
157
158                     if (k = 7) then
159                         OutBlock(i, j) <= sum(15 downto 8);
160                     end if;
161                 end loop;
162             end loop;
163         end loop;

```

```

164
165     -- over with computation
166     over <= '1';
167 end process compute;
168
169 communicate: process
170     variable tempi, tempj : integer;
171 begin
172     dack <= '0';
173     done <= '0';
174     ready <= '0';
175
176     for i in 0 to 7 loop
177         for j in 0 to 3 loop
178             wait until dreq = '1';
179             dack <= '1' after 1 ns;
180             wait until dreq = '0';
181             wait until clk = '1';
182             tempi := conv_integer(unsigned(dbus)) / 8;
183             tempj := conv_integer(unsigned(dbus)) mod 8;
184             wait until clk = '1';
185             TempBlock (tempi, tempj) <= dbus;
186             wait until clk = '1';
187             TempBlock (tempi, tempj+1) <= dbus;
188             dack <= '0' after 1 ns; --mem write time
189         end loop;
190     end loop;
191     wait until clk = '1';
192     ready <= '1';
193
194     -- output the matrix
195     wait until over = '1';
196     ready <= '0';
197     done <= '1';
198     for i in 0 to 7 loop
199         for j in 0 to 7 loop
200             wait until clk = '1';
201             dout <= OutBlock (i, j);
202         end loop;
203     end loop;
204     done <= '0';
205 end process communicate;
206 end behav;
207
208 library ieee;
209 use ieee .std_logic_1164 .all;
210
211 entity dct is
212     port ( start : in  std_logic;
213           clk   : in  std_logic;
214           din   : in  std_logic_vector(7 downto 0);
215           done  : out std_logic;
216           dout  : out std_logic_vector(7 downto 0));
217 end dct;
218

```

```

219 architecture struct of dct is
220   component mml
221     port ( start : in  std_logic;
222           clk   : in  std_logic;
223           din   : in  std_logic_vector(7 downto 0);
224           dreq  : out std_logic;
225           dack  : in  std_logic;
226           dbus  : out std_logic_vector(7 downto 0));
227   end component;
228
229   component mm2
230     port ( done  : out std_logic;
231           clk   : in  std_logic;
232           dbus  : in  std_logic_vector(7 downto 0);
233           dreq  : in  std_logic;
234           dack  : out std_logic;
235           dout  : out std_logic_vector(7 downto 0));
236   end component;
237
238   signal dreq, dack : std_logic;
239   signal dbus       : std_logic_vector(7 downto 0);
240 begin
241   u1 : mml
242     port map(start, clk, din, dreq, dack, dbus);
243
244   u2 : mm2
245     port map(done, clk, dbus, dreq, dack, dout);
246 end struct;

```

## F Replacing an ASIC

```
1
2 -- Rockwell ASIC Reuse Modeling Project
3 -- Nov 13, 1997
4
5 -- DCT example with 2 components for the 2 matrix multiplications
6 -- components have different protocols. an interface is used
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10 use ieee.std_logic_arith.all;
11
12 entity mml is
13     port ( start : in std_logic;
14           clk : in std_logic;
15           din : in std_logic_vector(7 downto 0);
16           txreq : out std_logic;
17           txack : in std_logic;
18           dreq : out std_logic;
19           dack : in std_logic;
20           addr : out std_logic_vector(5 downto 0);
21           data : out std_logic_vector(7 downto 0));
22 end mml;
23
24 architecture behav of mml is
25     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
26     signal InBlock, TempBlock : mem;
27     signal ready, over : std_logic;
28 begin
29     compute: process
30         variable cosblock : mem := (
31             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
32             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
33             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
34             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
35             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
36             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
37             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
38             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
39         );
40         variable a, b : std_logic_vector(7 downto 0);
41         variable p, sum : std_logic_vector(15 downto 0);
42     begin
43         wait until ready = '1';
44         over <= '0';
45
46         -- first matrix multiplication computation
47         for i in 0 to 7 loop
48             for j in 0 to 7 loop
49                 for k in 0 to 7 loop
50                     a := inblock (i, k);
51                     b := cosblock (j, k);
52                     p := signed(a) * signed(b);
53
```

```

54         if (k = 0) then
55             sum := p;
56         else
57             sum := signed(sum) + signed(p);
58         end if;
59
60         if (k = 7) then
61             TempBlock (i, j) <= sum(15 downto 8);
62         end if;
63     end loop;
64 end loop;
65 end loop;
66
67     -- computation over
68     over <= '1';
69 end process compute;
70
71 communicate: process
72 begin
73     ready <= '0';
74     wait until start = '1';
75     txreq <= '0';
76     dreq <= '0';
77
78     -- read the input data matrix
79     for i in 0 to 7 loop
80         for j in 0 to 7 loop
81             wait until clk = '1';
82             InBlock (i, j) <= din;
83         end loop;
84     end loop;
85     ready <= '1';
86
87     -- transfer the data
88     wait until over = '1';
89     ready <= '0';
90     txreq <= '1';
91     wait until txack = '1';
92
93     for i in 0 to 7 loop
94         for j in 0 to 7 loop
95             wait until clk = '1';
96             dreq <= '1';
97             wait until dack = '1';
98             addr <= conv_std_logic_vector(8*i+j, 6);
99             data <= tempblock (i, j);
100            dreq <= '0' after 3 ns; --mem read time
101            wait until dack = '0';
102        end loop;
103    end loop;
104    txreq <= '0';
105 end process communicate;
106 end behav;
107
108

```

```

109 library ieee;
110 use ieee.std_logic_1164.all;
111 use ieee.std_logic_arith.all;
112
113 entity mm2 is
114     port ( done : out std_logic;
115           clk : in std_logic;
116           dbus : in std_logic_vector(7 downto 0);
117           dreq : in std_logic;
118           dack : out std_logic;
119           dout : out std_logic_vector(7 downto 0));
120 end mm2;
121
122 architecture behav of mm2 is
123     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
124     signal TempBlock, OutBlock : mem;
125     signal ready, over : std_logic;
126 begin
127     compute: process
128         variable cosblock : mem := (
129             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
130             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
131             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
132             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
133             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
134             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
135             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
136             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
137         );
138         variable a, b : std_logic_vector(7 downto 0);
139         variable p, sum : std_logic_vector(15 downto 0);
140     begin
141         wait until ready = '1';
142         over <= '0';
143
144         -- second matrix multiplication computation
145         for i in 0 to 7 loop
146             for j in 0 to 7 loop
147                 for k in 0 to 7 loop
148                     a := TempBlock(k, j);
149                     b := CosBlock(i, k);
150                     p := signed(a) * signed(b);
151
152                     if (k = 0) then
153                         sum := p;
154                     else
155                         sum := signed(sum) + signed(p);
156                     end if;
157
158                     if (k = 7) then
159                         OutBlock(i, j) <= sum(15 downto 8);
160                     end if;
161                 end loop;
162             end loop;
163         end loop;

```



```

164
165     -- over with computation
166     over <= '1';
167 end process compute;
168
169 communicate: process
170     variable tempi, tempj : integer;
171 begin
172     dack <= '0';
173     done <= '0';
174     ready <= '0';
175
176     for i in 0 to 7 loop
177         for j in 0 to 3 loop
178             wait until dreq = '1';
179             dack <= '1' after 1 ns;
180             wait until dreq = '0';
181             wait until clk = '1';
182             tempi := conv_integer(unsigned(dbus)) / 8;
183             tempj := conv_integer(unsigned(dbus)) mod 8;
184             wait until clk = '1';
185             TempBlock (tempi, tempj) <= dbus;
186             wait until clk = '1';
187             TempBlock (tempi, tempj+1) <= dbus;
188             dack <= '0' after 1 ns; --mem write time
189         end loop;
190     end loop;
191     wait until clk = '1';
192     ready <= '1';
193
194     -- output the matrix
195     wait until over = '1';
196     ready <= '0';
197     done <= '1';
198     for i in 0 to 7 loop
199         for j in 0 to 7 loop
200             wait until clk = '1';
201             dout <= OutBlock (i, j);
202         end loop;
203     end loop;
204     done <= '0';
205 end process communicate;
206 end behav;
207
208
209 library ieee;
210 use ieee.std_logic_1164.all;
211
212 entity transducer is
213     port ( clk : in std_logic;
214           txreq : in std_logic;
215           txack : out std_logic;
216           dreq : in std_logic;
217           dack : out std_logic;
218           addr : in std_logic_vector(5 downto 0);

```

```

219     data : in  std_logic_vector(7 downto 0);
220     dbus : out std_logic_vector(7 downto 0);
221     req  : out std_logic;
222     ack  : in  std_logic);
223 end transducer;
224
225 architecture behav of transducer is
226 begin
227     process
228         variable taddr1, taddr2 : std_logic_vector(7 downto 0);
229         variable tdata1, tdata2 : std_logic_vector(7 downto 0);
230     begin
231         txack <= '0';
232         req <= '0';
233         dack <= '0';
234
235         wait until txreq = '1';
236         wait until clk = '1';
237         txack <= '1';
238
239         while txreq = '1' loop
240             wait until (dreq = '1' OR txreq = '0');
241             if (txreq = '1') then
242                 dack <= '1' after 1 ns;
243                 wait until dreq = '0';
244                 -- receive first address and data byte
245                 taddr1 := "00" & addr;
246                 tdata1 := data;
247                 dack <= '0' after 2 ns;
248                 wait until dreq = '1';
249                 dack <= '1' after 1 ns;
250                 wait until dreq = '0';
251                 -- receive second address and data byte
252                 taddr2 := "00" & addr;
253                 tdata2 := data;
254                 -- ready to send two bytes
255                 req <= '1';
256                 wait until ack = '1';
257                 wait until clk = '1';
258                 dbus <= taddr1;
259                 req <= '0';
260                 wait until clk = '1';
261                 dbus <= tdata1;
262                 wait until clk = '1';
263                 dbus <= tdata2;
264                 wait until clk = '1';
265                 dbus <= (others => 'Z');
266                 wait until ack = '0';
267                 -- give the ack signal to first process
268                 dack <= '0' after 2 ns;
269             end if;
270         end loop;
271         txack <= '0' after 2 ns;
272     end process;
273 end behav;

```

```

274
275
276 library ieee;
277 use ieee.std_logic_1164.all;
278
279 entity dct is
280     port ( start : in std_logic;
281           clk : in std_logic;
282           din : in std_logic_vector(7 downto 0);
283           done : out std_logic;
284           dout : out std_logic_vector(7 downto 0));
285 end dct;
286
287 architecture struct of dct is
288     component mml
289         port ( start : in std_logic;
290               clk : in std_logic;
291               din : in std_logic_vector(7 downto 0);
292               txreq : out std_logic;
293               txack : in std_logic;
294               dreq : out std_logic;
295               dack : in std_logic;
296               addr : out std_logic_vector(5 downto 0);
297               data : out std_logic_vector(7 downto 0));
298     end component;
299
300     component mm2
301         port ( done : out std_logic;
302               clk : in std_logic;
303               dbus : in std_logic_vector(7 downto 0);
304               dreq : in std_logic;
305               dack : out std_logic;
306               dout : out std_logic_vector(7 downto 0));
307     end component;
308
309     component transducer
310         port ( clk : in std_logic;
311               txreq : in std_logic;
312               txack : out std_logic;
313               dreq : in std_logic;
314               dack : out std_logic;
315               addr : in std_logic_vector(5 downto 0);
316               data : in std_logic_vector(7 downto 0);
317               dbus : out std_logic_vector(7 downto 0);
318               req : out std_logic;
319               ack : in std_logic);
320     end component;
321
322     signal txreq, txack, dreq, dack, req, ack : std_logic;
323     signal data, dbus : std_logic_vector(7 downto 0);
324     signal addr : std_logic_vector(5 downto 0);
325
326 begin
327     ul : mml
328         port map (start, clk, din, txreq, txack, dreq, dack, addr, data);

```

```
329
330     u2 : mm2
331         port map (done, clk, dbus, req, ack, dout);
332
333     u3 : transducer
334         port map (clk, txreq, txack, dreq, dack, addr, data, dbus, req, ack);
335 end struct;
```

## G Replacing the bus

```
1
2 --- Rockwell ASIC Reuse Modeling Project
3 --- Dec 2, 1997
4 ---
5 --- replace a bus with another bus that has different protocol
6 --- two transducer need to be used
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10 use ieee.std_logic_arith.all;
11
12 entity mml is
13     port ( start : in std_logic;
14           clk : in std_logic;
15           din : in std_logic_vector(7 downto 0);
16           txreq : out std_logic;
17           txack : in std_logic;
18           dreq : out std_logic;
19           dack : in std_logic;
20           addr : out std_logic_vector(5 downto 0);
21           data : out std_logic_vector(7 downto 0));
22 end mml;
23
24 architecture behav of mml is
25     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
26     signal InBlock, TempBlock : mem;
27     signal ready, over : std_logic;
28 begin
29     compute: process
30         variable cosblock : mem := (
31             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
32             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
33             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
34             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
35             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
36             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
37             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
38             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
39         );
40         variable a, b : std_logic_vector(7 downto 0);
41         variable p, sum : std_logic_vector(15 downto 0);
42     begin
43         wait until ready = '1';
44         over <= '0';
45
46         -- first matrix multiplication calculation
47         for i in 0 to 7 loop
48             for j in 0 to 7 loop
49                 for k in 0 to 7 loop
50                     a := InBlock (i, k);
51                     b := CosBlock (j, k);
52                     p := signed(a) * signed(b);
53
```

```

54         if (k = 0) then
55             sum := p;
56         else
57             sum := signed(sum) + signed(p);
58         end if;
59
60         if (k = 7) then
61             TempBlock (i, j) <= sum(15 downto 8);
62         end if;
63     end loop;
64 end loop;
65 end loop;
66
67     -- done with the computation
68     over <= '1';
69 end process compute;
70
71 communicate: process
72 begin
73     ready <= '0';
74     wait until start = '1';
75     txreq <= '0';
76     dreq <= '0';
77
78     -- read the input data matrix
79     for i in 0 to 7 loop
80         for j in 0 to 7 loop
81             wait until clk = '1';
82             InBlock (i, j) <= din;
83         end loop;
84     end loop;
85     ready <= '1';
86
87     -- transfer the data
88     wait until over = '1';
89     ready <= '0';
90     txreq <= '1';
91     wait until txack = '1';
92
93     for i in 0 to 7 loop
94         for j in 0 to 7 loop
95             wait until clk = '1';
96             dreq <= '1';
97             wait until dack = '1';
98             addr <= conv_std_logic_vector(8*i+j, 6);
99             data <= tempblock (i, j);
100            dreq <= '0' after 3 ns; -- mem read time
101            wait until dack = '0';
102        end loop;
103    end loop;
104    txreq <= '0';
105 end process communicate;
106 end behav;
107
108

```

```

109 library ieee;
110 use ieee.std_logic_1164.all;
111 use ieee.std_logic_arith.all;
112
113 entity mm2 is
114     port ( done : out std_logic;
115           clk : in std_logic;
116           data : in std_logic_vector(7 downto 0);
117           addr : in std_logic_vector(5 downto 0);
118           txreq : in std_logic;
119           txack : out std_logic;
120           dreq : in std_logic;
121           dack : out std_logic;
122           dout : out std_logic_vector(7 downto 0));
123 end mm2;
124
125 architecture behav of mm2 is
126     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
127     signal TempBlock, OutBlock : mem;
128     signal ready, over : std_logic;
129 begin
130     compute: process
131         variable cosblock : mem := (
132             ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
133             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
134             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
135             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
136             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
137             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
138             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
139             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
140         );
141         variable a, b : std_logic_vector(7 downto 0);
142         variable p, sum : std_logic_vector(15 downto 0);
143     begin
144         wait until ready = '1';
145         over <= '0';
146
147         -- second matrix multiplication computation
148         for i in 0 to 7 loop
149             for j in 0 to 7 loop
150                 for k in 0 to 7 loop
151                     a := TempBlock(k, j);
152                     b := CosBlock(i, k);
153                     p := signed(a) * signed(b);
154
155                     if (k = 0) then
156                         sum := p;
157                     else
158                         sum := signed(sum) + signed(p);
159                     end if;
160
161                     if (k = 7) then
162                         OutBlock(i, j) <= sum(15 downto 8);
163                     end if;

```

```

164         end loop;
165     end loop;
166 end loop;
167
168     -- over with the computation
169     over <= '1';
170 end process compute;
171
172 communicate: process
173     variable tempi, tempj : integer;
174 begin
175     txack <= '0';
176     dack <= '0';
177     done <= '0';
178     wait until txreq = '1';
179     wait until clk = '1';
180     txack <= '1' after 1 ns;
181
182     while (txreq = '1') loop
183         wait until (dreq = '1' OR txreq = '0');
184         if (txreq = '1') then
185             dack <= '1' after 1 ns;
186             wait until dreq = '0';
187             tempi := conv_integer(unsigned(addr)) / 8;
188             tempj := conv_integer(unsigned(addr)) mod 8;
189             TempBlock (tempi, tempj) <= data;
190             dack <= '0' after 8 ns; --mem write time
191         end if;
192     end loop;
193
194     wait until clk = '1';
195     txack <= '0';
196     ready <= '1';
197
198     -- output the computed matrix
199     wait until over = '1';
200     ready <= '0';
201
202     done <= '1';
203     for i in 0 to 7 loop
204         for j in 0 to 7 loop
205             wait until clk = '1';
206             dout <= OutBlock (i, j);
207         end loop;
208     end loop;
209     done <= '0';
210 end process communicate;
211 end behav;
212
213 library ieee;
214 use ieee.std_logic_1164.all;
215
216 -- converts bus 1 protocol (4 control signals) to the
217 -- bus 2 protocol (2 control signals)
218 entity transducer1 is

```



```

219 port ( clk : in std_logic;
220         txreq : in std_logic;
221         txack : out std_logic;
222         dreq : in std_logic;
223         dack : out std_logic;
224         addr : in std_logic_vector(5 downto 0);
225         data : in std_logic_vector(7 downto 0);
226         dbus : out std_logic_vector(7 downto 0);
227         req : out std_logic;
228         ack : in std_logic);
229 end transducer1;
230
231 architecture behav of transducer1 is
232 begin
233     process
234         variable taddr1, taddr2 : std_logic_vector(7 downto 0);
235         variable tdata1, tdata2 : std_logic_vector(7 downto 0);
236     begin
237         txack <= '0';
238         req <= '0';
239         dack <= '0';
240
241         wait until txreq = '1';
242         wait until clk = '1';
243         txack <= '1';
244
245         while txreq = '1' loop
246             wait until (dreq = '1' OR txreq = '0');
247             if (txreq = '1') then
248                 dack <= '1' after 1 ns;
249                 wait until dreq = '0';
250                 -- receive first address and data byte
251                 taddr1 := "00" & addr;
252                 tdata1 := data;
253                 dack <= '0' after 2 ns;
254                 wait until dreq = '1';
255                 dack <= '1' after 1 ns;
256                 wait until dreq = '0';
257                 -- receive second address and data byte
258                 taddr2 := "00" & addr;
259                 tdata2 := data;
260                 -- ready to send two bytes
261                 req <= '1';
262                 wait until ack = '1';
263                 wait until clk = '1';
264                 dbus <= taddr1;
265                 req <= '0';
266                 wait until clk = '1';
267                 dbus <= tdata1;
268                 wait until clk = '1';
269                 dbus <= tdata2;
270                 wait until clk = '1';
271                 dbus <= (others => 'Z');
272                 wait until ack = '0';
273                 -- give the ack signal to first process

```

```

274         dack <= '0' after 2 ns;
275     end if;
276 end loop;
277 txack <= '0' after 2 ns;
278 end process;
279 end behav;
280
281
282 library ieee;
283 use ieee.std_logic_1164.all;
284 use ieee.std_logic_arith.all;
285
286 -- converts bus 2 protocol (2 control signals) to the
287 -- bus 1 protocol (4 control signals)
288 entity transducer2 is
289     port ( clk : in std_logic;
290           txreq : out std_logic;
291           txack : in std_logic;
292           dreq : out std_logic;
293           dack : in std_logic;
294           addr : out std_logic_vector(5 downto 0);
295           data : out std_logic_vector(7 downto 0);
296           dbus : in std_logic_vector(7 downto 0);
297           req : in std_logic;
298           ack : out std_logic);
299 end transducer2;
300
301 architecture behav of transducer2 is
302 begin
303     process
304         variable tadd : std_logic_vector (5 downto 0);
305         variable data1, data2 : std_logic_vector (7 downto 0);
306     begin
307         -- wait for protocol 1 to be ready
308         txreq <= '1';
309         wait until txack = '1';
310
311         for i in 0 to 7 loop
312             for j in 0 to 3 loop
313                 -- first read the addr and two data bytes
314                 wait until req = '1';
315                 ack <= '1' after 1 ns;
316                 wait until req = '0';
317                 wait until clk = '1';
318                 tadd := dbus(5 downto 0);
319                 wait until clk = '1';
320                 data1 := dbus;
321                 wait until clk = '1';
322                 data2 := dbus;
323                 -- send the two bytes with the addresses
324                 dreq <= '1';
325                 wait until dack = '1';
326                 addr <= tadd;
327                 data <= data1;
328                 dreq <= '0' after 3 ns;

```

```

329         wait until dack = '0';
330         wait until clk = '1';
331         dreq <= '1';
332         wait until dack = '1';
333         addr <= conv_std_logic_vector(conv_integer(unsigned(tadd)) + 1, 6);
334         data <= data2;
335         dreq <= '0' after 3 ns;
336         wait until dack = '0';
337
338         wait until clk = '1';
339         ack <= '0' after 1 ns;
340     end loop;
341 end loop;
342 txreq <= '0';
343 wait until txack = '0';
344 end process;
345 end behav;
346
347
348 library ieee;
349 use ieee.std_logic_1164.all;
350
351 entity dct is
352     port ( start : in std_logic;
353           clk : in std_logic;
354           din : in std_logic_vector(7 downto 0);
355           done : out std_logic;
356           dout : out std_logic_vector(7 downto 0));
357 end dct;
358
359 architecture struct of dct is
360     component mml
361         port ( start : in std_logic;
362               clk : in std_logic;
363               din : in std_logic_vector(7 downto 0);
364               txreq : out std_logic;
365               txack : in std_logic;
366               dreq : out std_logic;
367               dack : in std_logic;
368               addr : out std_logic_vector(5 downto 0);
369               data : out std_logic_vector(7 downto 0));
370     end component;
371
372     component mm2
373         port ( done : out std_logic;
374               clk : in std_logic;
375               data : in std_logic_vector(7 downto 0);
376               addr : in std_logic_vector(5 downto 0);
377               txreq : in std_logic;
378               txack : out std_logic;
379               dreq : in std_logic;
380               dack : out std_logic;
381               dout : out std_logic_vector(7 downto 0));
382     end component;
383

```

```

384 component transducer1
385     port ( clk : in std_logic;
386           txreq : in std_logic;
387           txack : out std_logic;
388           dreq : in std_logic;
389           dack : out std_logic;
390           addr : in std_logic_vector(5 downto 0);
391           data : in std_logic_vector(7 downto 0);
392           dbus : out std_logic_vector(7 downto 0);
393           req : out std_logic;
394           ack : in std_logic);
395 end component;
396
397 component transducer2
398     port ( clk : in std_logic;
399           txreq : out std_logic;
400           txack : in std_logic;
401           dreq : out std_logic;
402           dack : in std_logic;
403           addr : out std_logic_vector(5 downto 0);
404           data : out std_logic_vector(7 downto 0);
405           dbus : in std_logic_vector(7 downto 0);
406           req : in std_logic;
407           ack : out std_logic);
408 end component;
409
410 signal txreq1, txack1, dreq1, dack1, req, ack : std_logic;
411 signal txreq2, txack2, dreq2, dack2 : std_logic;
412 signal data1, data2, dbus : std_logic_vector(7 downto 0);
413 signal addr1, addr2 : std_logic_vector (5 downto 0);
414 begin
415     u1 : mml
416         port map(start, clk, din, txreq1, txack1, dreq1, dack1, addr1, data1);
417
418     u2 : mm2
419         port map(done, clk, data2, addr2, txreq2, txack2, dreq2, dack2, dout);
420
421     u3 : transducer1
422         port map(clk, txreq1, txack1, dreq1, dack1, addr1, data1, dbus, req, ack);
423
424     u4 : transducer2
425         port map(clk, txreq2, txack2, dreq2, dack2, addr2, data2, dbus, req, ack);
426 end struct;

```

## H Communication using a FIFO queue

```
1 -----
2 -- Rockwell ASIC Reuse Modeling Project
3 -- Nov 20, 1997
4 --
5 -- DCT example with 2 components for the 2 matrix multiplications
6 -- communication through a 64 byte FIFO queue with full/empty lines
7 -----
8
9 -- model of a 64 byte FIFO
10 library ieee;
11 use ieee.std_logic_1164.all;
12 use ieee.std_logic_arith.all;
13
14 entity fifo is
15     port ( enable : in  std_logic;
16           reset  : in  std_logic;
17           rws    : in  std_logic;
18           clk    : in  std_logic;
19           din    : in  std_logic_vector(7 downto 0);
20           dout   : out std_logic_vector(7 downto 0);
21           full   : out std_logic;
22           empty  : out std_logic);
23 end fifo;
24
25 architecture behav of fifo is
26 begin
27     process ( clk )
28         type storagetype is array(0 to 63) of std_logic_vector(7 downto 0);
29         variable storage : storagetype;
30         variable front, back : integer;
31         variable isempty, isfull : std_logic := '0';
32     begin
33         if ( clk = '1' ) then
34             -- reset counters and flags
35             if ( reset = '1' ) then
36                 front := 0;
37                 back := 0;
38                 isempty := '1';
39                 isfull := '0';
40             else
41                 -- read from fifo
42                 if ( rws = '0' and isempty = '0' and enable = '1' ) then
43                     dout <= storage(front);
44                     front := (front + 1) mod 64;
45                     if ( front = back ) then
46                         isempty := '1';
47                         isfull := '0';
48                     end if;
49                 end if;
50
51                 -- write into fifo
52                 if ( rws = '1' and isfull = '0' and enable = '1' ) then
53                     storage(back) := din;
```

```

54         back := (back + 1) mod 64;
55         if (front = back) then
56             isempty := '0';
57             isfull := '1';
58         end if;
59     end if;
60 end if;
61 empty <= isempty;
62 full <= isfull;
63 end if;
64 end process;
65 end behav;
66
67
68 library ieee;
69 use ieee.std_logic_1164.all;
70 use ieee.std_logic_arith.all;
71
72 entity mml is
73     port ( start : in std_logic;
74           clk : in std_logic;
75           din : in std_logic_vector(7 downto 0);
76           empty : in std_logic;
77           rws : out std_logic;
78           enable : out std_logic;
79           reset : out std_logic;
80           data : out std_logic_vector(7 downto 0));
81 end mml;
82
83 architecture behav of mml is
84     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
85     begin
86         process
87             variable inblock : mem;
88             variable cosblock : mem := (
89                 ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
90                 ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
91                 ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
92                 ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
93                 ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
94                 ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
95                 ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
96                 ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
97             );
98             variable a, b : std_logic_vector(7 downto 0);
99             variable p, sum : std_logic_vector(15 downto 0);
100         begin
101             wait until start = '1';
102             data <= (others => 'Z');
103
104             -- read the input data matrix
105             for i in 0 to 7 loop
106                 for j in 0 to 7 loop
107                     wait until clk = '1';
108                     inblock (i, j) := din;

```

```

109         end loop;
110     end loop;
111
112     -- reset the fifo
113     reset <= '1';
114     wait until clk = '1';
115     reset <= '0';
116
117     -- do the computation
118     for i in 0 to 7 loop
119         for j in 0 to 7 loop
120             for k in 0 to 7 loop
121                 a := inblock (i, k);
122                 b := cosblock (j, k);
123                 p := signed(a) * signed(b);
124
125                 if (k = 0) then
126                     sum := p;
127                 else
128                     sum := signed(sum) + signed(p);
129                 end if;
130
131                 -- computed one entry of matrix. write to FIFO
132                 if (k = 7) then
133                     enable <= '1';
134                     rws <= '1';
135                     data <= sum(15 downto 8);
136                     wait until clk = '1';
137                     enable <= '0';
138                     rws <= '0';
139                 end if;
140             end loop;
141         end loop;
142     end loop;
143 end process;
144 end behav;
145
146
147 library ieee;
148 use ieee.std_logic_1164.all;
149 use ieee.std_logic_arith.all;
150
151 entity mm2 is
152     port ( done : out std_logic;
153           clk : in std_logic;
154           data : in std_logic_vector(7 downto 0);
155           full : in std_logic;
156           rws : out std_logic;
157           enable : out std_logic;
158           dout : out std_logic_vector(7 downto 0));
159 end mm2;
160
161 architecture behav of mm2 is
162     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
163     type widemem is array (0 to 7, 0 to 7) of std_logic_vector(15 downto 0);

```

```

164 begin
165   process
166     -- this algorithm will use wider memory
167     variable outblock : widemem;
168     variable cosblock : mem := (
169       ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
170       ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
171       ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
172       ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
173       ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
174       ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
175       ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
176       ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
177     );
178     variable a, b : std_logic_vector(7 downto 0);
179     variable p, sum, temp : std_logic_vector(15 downto 0);
180   begin
181     enable <= '0';
182     rws <= '0';
183     wait until full = '1';
184     wait until clk = '1';
185
186     -- do the computation
187     for i in 0 to 7 loop
188       for j in 0 to 7 loop
189         -- read one entry of matrix
190         enable <= '1';
191         wait until clk = '1';
192         enable <= '0';
193         wait until clk = '1';
194         a := data;
195
196         -- add the product to all the partial sums
197         for k in 0 to 7 loop
198           if (i /= 0) then
199             temp := outblock(k, j);
200           end if;
201           b := cosblock(k, i);
202           p := signed(a) * signed(b);
203
204           if (i = 0) then
205             sum := p;
206           else
207             sum := signed(temp) + signed(p);
208           end if;
209           outblock(k, j) := sum;
210         end loop;
211       end loop;
212     end loop;
213
214     -- give the done signal and output the output matrix
215     done <= '1';
216     for i in 0 to 7 loop
217       for j in 0 to 7 loop
218         wait until clk = '1';

```



```

219         dout <= outblock (i, j) (15 downto 8);
220     end loop;
221 end loop;
222     done <= '0';
223 end process;
224 end behav;
225
226 library ieee;
227 use ieee.std_logic_1164.all;
228
229 entity dct is
230     port ( start : in std_logic;
231           clk : in std_logic;
232           din : in std_logic_vector(7 downto 0);
233           done : out std_logic;
234           dout : out std_logic_vector(7 downto 0));
235 end dct;
236
237 architecture struct of dct is
238     component mml
239         port ( start : in std_logic;
240               clk : in std_logic;
241               din : in std_logic_vector(7 downto 0);
242               empty : in std_logic;
243               rws : out std_logic;
244               enable : out std_logic;
245               reset : out std_logic;
246               data : out std_logic_vector(7 downto 0));
247     end component;
248
249     component mm2
250         port ( done : out std_logic;
251               clk : in std_logic;
252               data : in std_logic_vector(7 downto 0);
253               full : in std_logic;
254               rws : out std_logic;
255               enable : out std_logic;
256               dout : out std_logic_vector(7 downto 0));
257     end component;
258
259     component fifo
260         port ( enable : in std_logic;
261               reset : in std_logic;
262               rws : in std_logic;
263               clk : in std_logic;
264               din : in std_logic_vector(7 downto 0);
265               dout : out std_logic_vector(7 downto 0);
266               full : out std_logic;
267               empty : out std_logic);
268     end component;
269
270     signal rws1, rws2, rws, enable1, enable2, enable : std_logic;
271     signal full, empty, reset : std_logic;
272     signal dmm1, dmm2 : std_logic_vector(7 downto 0);
273

```

```
274 begin
275     u1 : mm1
276         port map (start , clk , din , empty , rws1 , enable1 , reset , dmm1);
277
278     u2 : mm2
279         port map (done , clk , dmm2 , full , rws2 , enable2 , dout);
280
281     enable <= enable1 OR enable2;
282     rws <= rws1 OR rws2;
283
284     u3 : fifo
285         port map (enable , reset , rws , clk , dmm1 , dmm2 , full , empty);
286 end struct;
```

# I Communication using a shared memory

```
1
2 -- Rockwell ASIC Reuse Modeling Project
3 -- Nov 28, 1997
4
5 -- DCT components communicate using a shared memory
6
7 library ieee;
8 use ieee.std_logic_1164.all;
9 use ieee.std_logic_arith.all;
10 use ieee.std_logic_signed.all;
11
12 entity mml is
13     port ( start : in std_logic;
14           clk : in std_logic;
15           din : in std_logic_vector(7 downto 0);
16           used : in std_logic;
17           over : out std_logic;
18           csm : out std_logic;
19           wem : out std_logic;
20           addr : out std_logic_vector(5 downto 0);
21           data : out std_logic_vector(7 downto 0));
22 end mml;
23
24 architecture behav of mml is
25     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
26     begin
27         process
28             variable inblock : mem;
29             variable cosblock : mem := (
30                 ("01111101", "01111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
31                 ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
32                 ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
33                 ("01111101", "00011000", "10001101", "10111011", "01011000", "01110011", "11010001", "10000110"),
34                 ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
35                 ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
36                 ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
37                 ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
38             );
39             variable a, b : std_logic_vector(7 downto 0);
40             variable p, sum : std_logic_vector(15 downto 0);
41         begin
42             wait until start = '1';
43             data <= (others => 'Z');
44
45             -- read the input data matrix
46             for i in 0 to 7 loop
47                 for j in 0 to 7 loop
48                     wait until clk = '1';
49                     inblock(i, j) := din;
50                 end loop;
51             end loop;
52
53             wait until clk = '1';
```

```

54 wem<= '1';
55 csm<= '0';    -- enable the chip
56 wait until clk = '1';
57
58 --do the computation
59 for i in 0 to 7 loop
60     for j in 0 to 7 loop
61         for k in 0 to 7 loop
62             a := inblock (i, k);
63             b := cosblock (j, k);
64             p := signed(a) * signed(b);
65
66             if (k = 0) then
67                 sum := p;
68             else
69                 sum := signed(sum) + signed(p);
70             end if;
71
72             if (k = 7) then
73                 -- write the sum to shared memory
74                 addr <= conv_std_logic_vector(i*8+j, 6);
75                 wait for 1 ns;
76                 wem<= '0';
77                 wait for 8 ns;           --tWHZ time
78                 data <= sum(15 downto 8);
79                 wait for 9 ns;         --tDW
80                 wem<= '1';
81                 wait for 1 ns;
82                 data <= (others => 'Z');
83                 wait for 2 ns; --next cycle after this
84             end if;
85         end loop;
86     end loop;
87 end loop;
88
89 -- done with the computation
90 csm<= '1';
91 wait until clk = '1';
92 over <= '1';
93
94 -- wait till second unit finishes
95 wait until used = '1';
96 end process;
97 end behav;
98
99 library ieee;
100 use ieee.std_logic_1164.all;
101 use ieee.std_logic_arith.all;
102
103 entity mm2 is
104     port ( done : out std_logic;
105           clk : in std_logic;
106           csm : out std_logic;
107           oem : out std_logic;
108           addr : out std_logic_vector(5 downto 0);

```

```

109     data : in  std_logic_vector(7 downto 0);
110     used : out std_logic;
111     over : in  std_logic;
112     dout : out std_logic_vector(7 downto 0));
113 end mm2
114
115 architecture behav of mm2 is
116     type mem is array (0 to 7, 0 to 7) of std_logic_vector(7 downto 0);
117     type widemem is array (0 to 7, 0 to 7) of std_logic_vector(15 downto 0);
118 begin
119     process
120         variable outblock : widemem;
121         variable cosblock : mem := (
122             ("01111101", "011111010", "01110011", "01100111", "01011000", "01000101", "00101111", "00011000"),
123             ("01111101", "01100111", "00101111", "11101000", "10101000", "10000110", "10001101", "10111011"),
124             ("01111101", "01000101", "11010001", "10000110", "10101000", "00011000", "01110011", "01100111"),
125             ("01111101", "00011000", "10001101", "10111011", "01011000", "01100111", "11010001", "10000110"),
126             ("01111101", "11101000", "10001101", "01000101", "01011000", "10011001", "11010001", "01111010"),
127             ("01111101", "10111011", "11010001", "01111010", "10101000", "11101000", "01110011", "10011001"),
128             ("01111101", "10011001", "00101111", "00011000", "10101000", "01111010", "10001101", "01000101"),
129             ("01111101", "10000110", "01110011", "10011001", "01011000", "10111011", "00101111", "11101000")
130         );
131         variable a, b : std_logic_vector(7 downto 0);
132         variable p, sum, temp : std_logic_vector(15 downto 0);
133     begin
134         used <= '0';
135         -- do not assert the memory control lines
136         oem <= '1';
137         csm <= '1';
138         -- wait for the first matrix mult to finish
139         wait until over = '1';
140         csm <= '0';
141         addr <= (others => '1');
142
143         wait until clk = '1';
144
145         -- do the computation
146         for i in 0 to 7 loop
147             for j in 0 to 7 loop
148                 -- get the (i,j) data from memory
149                 addr <= conv_std_logic_vector(i*8+j, 6);
150                 wait for 1 ns;
151                 oem <= '0';
152                 wait for 17 ns;
153                 oem <= '1';
154
155                 a := data;
156                 for k in 0 to 7 loop
157                     if (i /= 0) then
158                         temp := outblock(k, j);
159                     end if;
160
161                     b := cosblock (k, i);
162                     p := signed(a) * signed(b);
163

```

```

164         if (i = 0) then
165             sum := p;
166         else
167             sum := signed(temp) + signed(p);
168         end if;
169         outblock (k, j) := sum;
170     end loop;
171     wait for 3 ns; -- next cycle
172 end loop;
173 end loop;
174
175 csm <= '1';
176 oem <= '1';
177
178 -- give the done signal and output the output matrix
179 wait until clk = '1';
180 done <= '1';
181 for i in 0 to 7 loop
182     for j in 0 to 7 loop
183         wait until clk = '1';
184         dout <= outblock(i, j)(15 downto 8);
185     end loop;
186 end loop;
187 done <= '0';
188 end process;
189 end behav;
190
191 library ieee;
192 use ieee.std_logic_1164.all;
193
194 entity arbiter is
195     port ( cs1 : in std_logic;
196           cs2 : in std_logic;
197           cs  : out std_logic;
198           addr1 : in std_logic_vector(5 downto 0);
199           addr2 : in std_logic_vector(5 downto 0);
200           addr  : out std_logic_vector(5 downto 0);
201           data1 : in std_logic_vector(7 downto 0);
202           data2 : out std_logic_vector(7 downto 0);
203           data  : inout std_logic_vector(7 downto 0));
204 end arbiter;
205
206 architecture behav of arbiter is
207 begin
208
209     process (cs1, cs2, addr1, addr2, data1, data)
210     begin
211         -- only one component should access memory
212         assert (cs2/= '0' or cs1/= '0')
213             report "memory_access_clash"
214             severity warning;
215
216         -- unit 1 only writes to memory
217         if (cs1='0' and cs2/= '0') then
218             cs <= '0';

```

```

219         addr <= addr1;
220         data <= data1;
221         -- unit 2 only reads from memory
222         elsif (cs1/= '0' and cs2='0') then
223             cs <= '0';
224             addr <= addr2;
225             data2 <= data;
226         else
227             cs <= '1';
228         end if;
229     end process;
230 end behav;
231
232
233 library ieee;
234 use ieee.std_logic_1164.all;
235
236 entity dct is
237     port ( start : in std_logic;
238           clk : in std_logic;
239           din : in std_logic_vector(7 downto 0);
240           done : out std_logic;
241           dout : out std_logic_vector(7 downto 0));
242 end dct;
243
244 architecture struct of dct is
245     component mml
246     port ( start : in std_logic;
247           clk : in std_logic;
248           din : in std_logic_vector(7 downto 0);
249           used : in std_logic;
250           over : out std_logic;
251           csm : out std_logic;
252           wem : out std_logic;
253           addr : out std_logic_vector(5 downto 0);
254           data : out std_logic_vector(7 downto 0));
255     end component;
256
257     component mm2
258     port ( done : out std_logic;
259           clk : in std_logic;
260           csm : out std_logic;
261           oem : out std_logic;
262           addr : out std_logic_vector(5 downto 0);
263           data : in std_logic_vector(7 downto 0);
264           used : out std_logic;
265           over : in std_logic;
266           dout : out std_logic_vector(7 downto 0));
267     end component;
268
269     component sram
270     port ( nce : in std_logic;
271           noe : in std_logic;
272           nwe : in std_logic;
273           a : in std_logic_vector(5 downto 0);

```

```

274         d : inout std_logic_vector(7 downto 0));
275     end component;
276
277     component arbiter
278     port ( cs1 : in std_logic;
279           cs2 : in std_logic;
280           cs  : out std_logic;
281           addr1 : in std_logic_vector(5 downto 0);
282           addr2 : in std_logic_vector(5 downto 0);
283           addr  : out std_logic_vector(5 downto 0);
284           data1 : in std_logic_vector(7 downto 0);
285           data2 : out std_logic_vector(7 downto 0);
286           data  : inout std_logic_vector(7 downto 0));
287     end component;
288
289     signal csm1, csm2, cs, oem, wem, used, over : std_logic;
290     signal addr1, addr2, addr : std_logic_vector(5 downto 0);
291     signal data, data1, data2 : std_logic_vector(7 downto 0);
292
293 begin
294     u1 : mm1
295         port map (start, clk, din, used, over, csm1, wem, addr1, data1);
296
297     u2 : mm2
298         port map (done, clk, csm2, oem, addr2, data2, used, over, dout);
299
300     u3 : sram
301         port map (cs, oem, wem, addr, data);
302
303     u4 : arbiter
304         port map (csm1, csm2, cs, addr1, addr2, addr, data1, data2, data);
305 end struct;

```