Title

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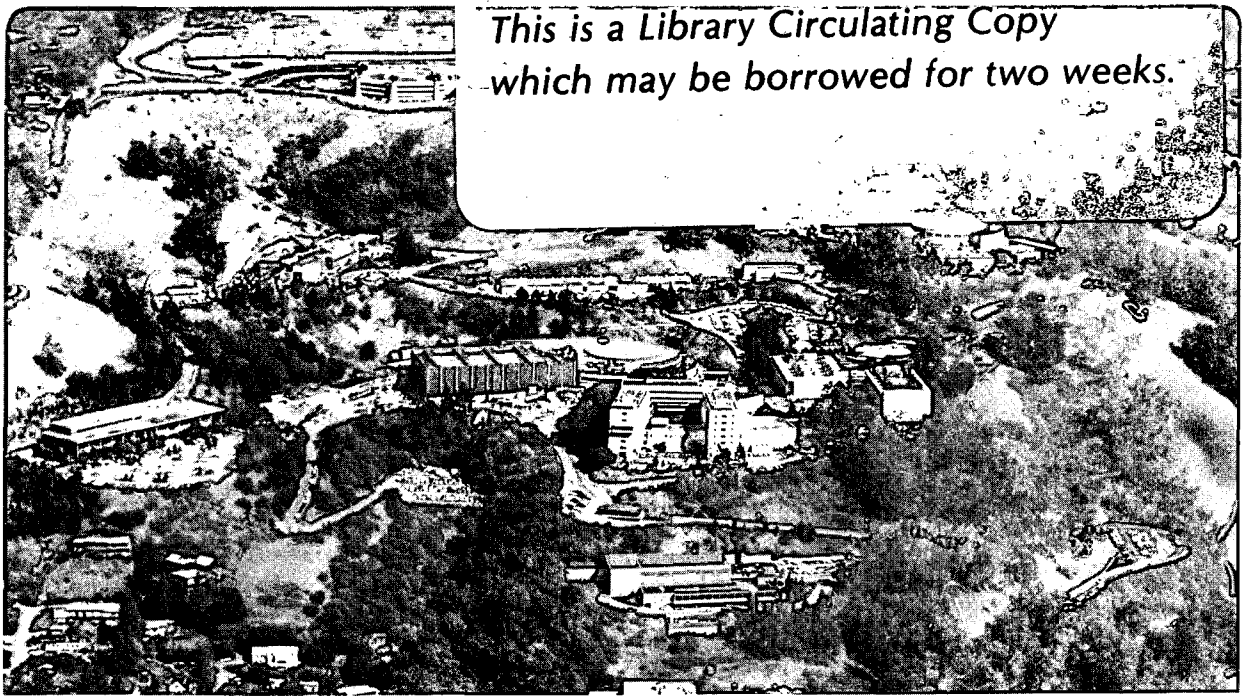

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DISCLAIMER

THE HYBRIDIZED FRONT END ELECTRONICS OF THE CENTRAL DRIFT CHAMBER IN THE STANFORD LINEAR COLLIDER DETECTOR

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ABSTRACT

In order to accommodate the high packaging density requirements for the front end electronics of the Central Drift Chamber (CDC) in the SLAC Linear Collider Detector (SLD), the CDC front end electronics has been hybridized. The hybrid package contains eight channels of amplifiers together with all the associated circuits for calibration, event recognition and power economy switching functions. A total of 1280 such hybrids are used in the CDC.

INTRODUCTION

The front end electronics for the Central Drift Chamber (CDC) in the SLAC Linear Collider Detector (SLD) has been hybridized because of the high packaging density requirements of SLD. The front end electronics of the CDC employs a charge division scheme (Fig. 1). A charge Q is injected at Xo on the sense wire N. The ratio of the charge collected at the two ends of the sense wire having a length L is:

$$Qa/Qb = (L - Xo)/Xo$$

and

$$Q = Qa + Qb$$

Detailed discussions of charge division can be found in Refs. 1, 2 and 3. This scheme requires two amplifiers per wire, i.e., one amplifier at each wire end. Since each cell in the CDC has eight sense wires, a cell requires a total of 16 amplifiers with 8 amplifiers on each end of the cell. Therefore, the design is based on 8 amplifiers per hybrid package. The outputs of the amplifiers are connected to the inputs of an equal number of Analog Memory Units (AMU's)[4,5]. The CDC has 640 cells and therefore requires a total of 1280 hybrids which contains a total of 10,240 amplifier channels. The conceptual design of the overall CDC electronics has been described in Ref. 6 and 7.

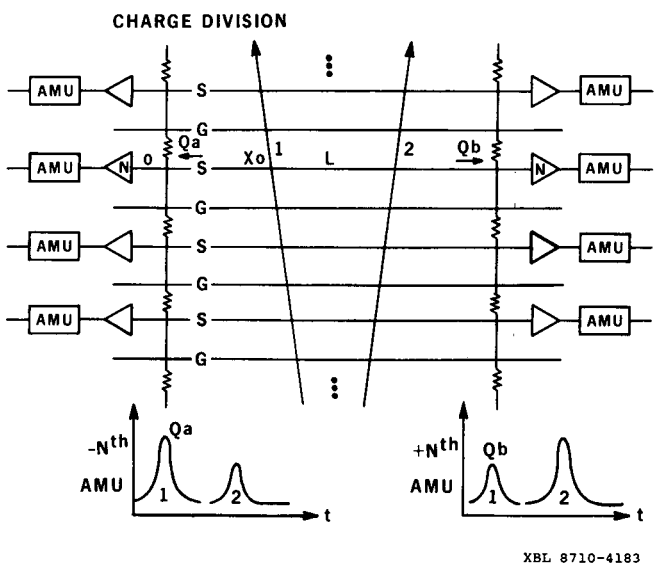

Fig. 1: Diagram of a charge division readout scheme.

SYSTEM ORGANIZATION

The hybridized front end includes eight channels of amplifiers, the calibration signal generation and its distribution network, the power switching circuit used to reduce power consumption, the leading edge trigger discriminators, the output hit registers and high current drivers. All of these circuits have been hybridized onto two interconnected substrates. The upper substrate contains the eight channels of amplifiers, while the bottom substrate contains the rest of the circuits. The amplifier substrate has dimensions of 3.2 cm x 6 cm, and the bottom substrate has dimensions of 4.3 cm x 6.6 cm. The amplifier substrate is mounted on top of the bottom substrate with spacers in between as standoffs. Connections between the two substrates are made via wire bondings. A metal layer with a one point ground was implemented on the bottom side of the amplifier substrate for shielding purposes. The completed hybrid package has dimensions of 4.3 cm x 6.6 cm with a height of 0.8 cm and a total of 50 input/output pins. Figure 2 is a block diagram of the CDC front end electronics. Figure 3 shows the eight amplifiers on the amplifier substrate; Fig. 4 shows the circuit layout of the bottom substrate which consists of the rest of the circuits in the system. The layout was designed with high level signal shielding in mind. The high

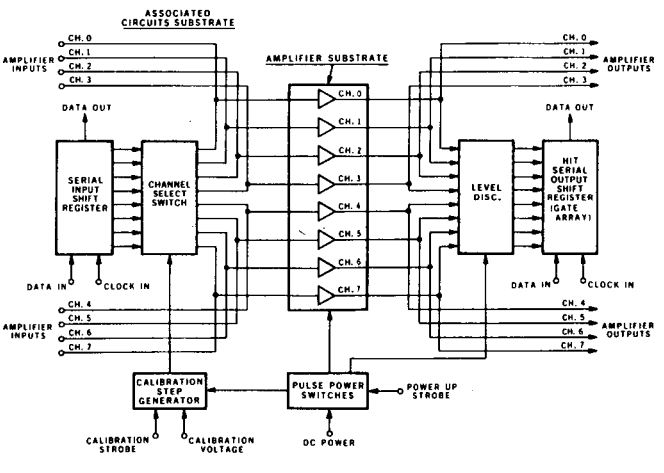

Fig. 2: Block diagram of the Central Drift Chamber (CDC) front end electronics.

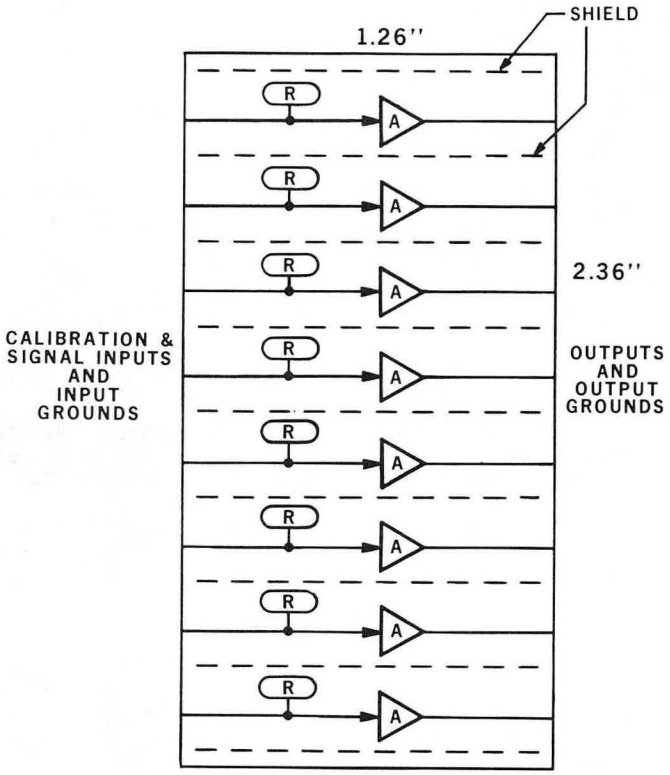

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Fig. 3: Circuit arrangement of amplifier substrate.

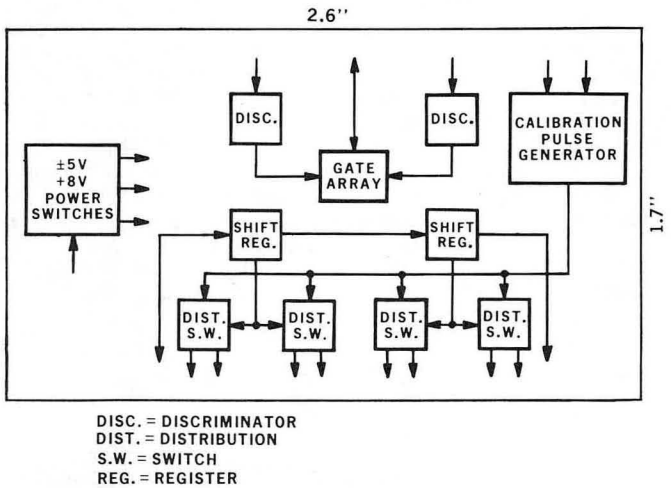

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Fig. 4: Circuit arrangement of bottom substrate.

level signals which would interfere with proper operation are the calibration strobe signal and the discriminator output signals. Figure 5 is a photograph of the CDC hybrid package. The eight well-defined sections are the eight amplifiers on the upper substrate. The 50 pads on the top and lower edges are the input and output connections which are located on the bottom substrate. The rest of the circuits are located on the bottom substrate underneath the upper substrate and hence are not visible in the photograph.

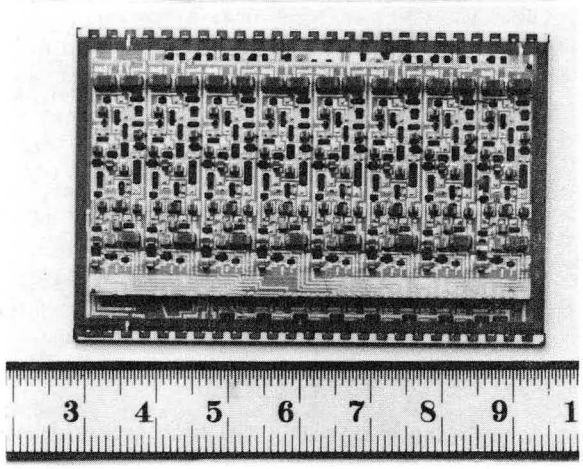

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Fig. 5: Photograph of the CDC hybrid package.

THE AMPLIFIER

On the amplifier substrate the eight amplifiers have been partitioned into eight well-defined sections which are partially shielded from one another by their voltage supply busses. Input and output signal grounds for each channel are kept separate so the source and load current return paths can be isolated to prevent ground loops and oscillations. Figure 6 shows a schematic diagram of one complete amplifier.

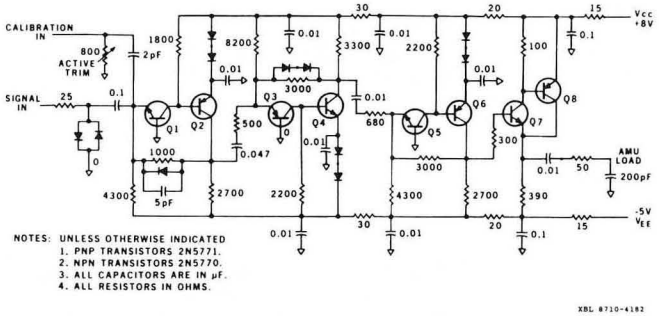

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Fig. 6: Schematic diagram of an amplifier.

Each amplifier contains three separate feedback stages and a high current output driver. The first stage serves as a transresistance amplifier. Due to feedback operation the impedence of the input node at the emitter of the first transistor is given by:

$$Zin' = Zin/(1 - AB)$$

where Zin is the input impedence without feedback, A is the forward gain with a sign change, B is the feedback transfer ratio and AB is the loop gain. In this case, Zin' is 5 ohms; hence, the input impedence of 30 ohms is easily achieved by adding a 25-ohm resistor in series with the input of the amplifier. The 5 pF capacitor connected across the feedback resistor is used to limit the bandwidth of the first stage to reduce the chance of oscillation. Due to the multi-layer construction of this hybrid and other restrictions, it is difficult to implement the ground plane normally preferred for high frequency circuits. The diode connected across the feedback resistor in the first stage is used to limit the gain of this stage when the output exceeds the forward voltage drop of this diode. The output voltage of the first stage is the product of the

current injected by the detector and the feedback resistor. The two limiting diodes in the second stage serve the same purpose as the one in the first stage. The gain of the second and third stages are defined by the ratio of their feedback and input resistors. The peaking time of the amplifier can be increased by adding capacitance across the feedback resistors. For the purpose of simplicity and keeping component count low, all stages are AC coupled which also causes some signal differentiation. The output stage is a White follower which serves as a high current driver for the 200 pF load of the AMU. The series resistor is used to form an integrator with the AMU's capacitive load. This resistor also serves as a damping resistor for the high Q circuit formed by the signal lead inductance and the 200 pF AMU capacitive load; the value of this resistor is especially important if the connecting lead going to the AMU is more than a few inches long.

AMPLIFIER PERFORMANCE

The amplifier has been designed to accept negative input signals and provide a positive output. The input impedence of the amplifier in the frequency range of 100 kHz - 30 MHz is given in Fig. 7. The transfer function of the amplifier is given in Fig. 8. The gain of the amplifier is 0.8 V/pC. The linearity of the amplifier is within ± 1 % in the 0 - 2 V output range. The 10 - 90 % risetime of an output pulse across a 200 pF load is typically 13 ns. The equivalent noise at the input is 6000 electrons (RMS) with 0 pF detector capacitance. With a 30 pF capacitor and a 348-ohm metal film resistor shunting the input, the noise increases to 7000 electrons (RMS). Crosstalk between channels is less than ± 1.5 %. The overload recovery time following the injection of a 125 pC charge is less than 500 ns. Amplifier gains are within 5 % from channel to channel. The signal propagation delay through the amplifier is typically 10 ns with a 200 pF load. The calibration signal is actively trimmed to bring the calibration system accuracy to within 1 %. Figure 9 shows the amplifier output waveshape of a Spice simulation with an input charge of 1 pC, whereas Fig. 10 shows a photograph of the actual output waveshape of the amplifier with the same input charge. Power consumption of eight channels of amplifiers is 80 mW at 5 % duty cycle operaton.

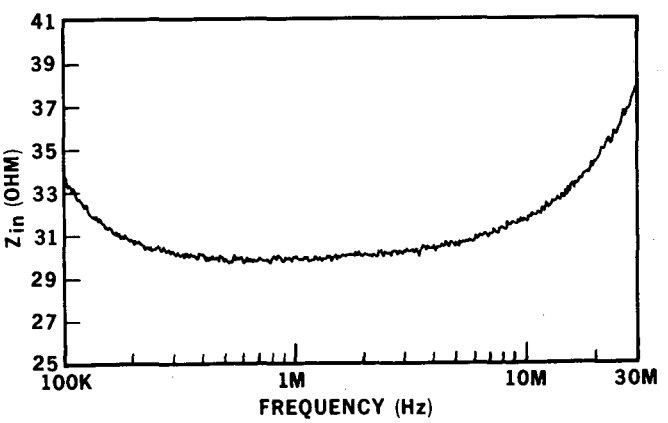

Fig. 7: Input impedence as a function of frequency of a typical amplifier.

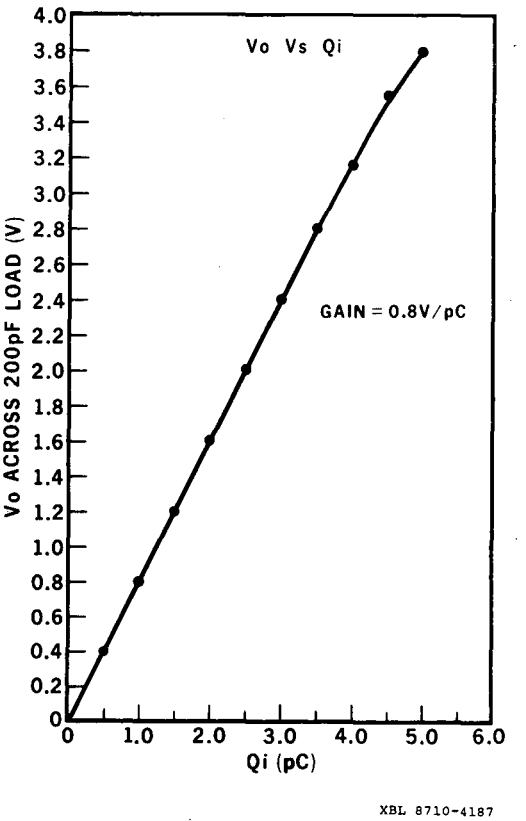

Fig. 8: Input-output transfer function of a typical amplifier.

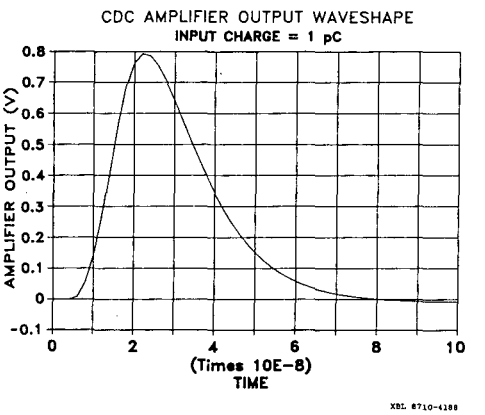

Fig. 9: Output waveshape of an amplifier with Spice simulation.

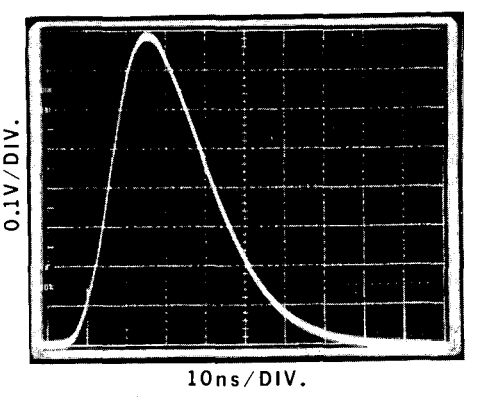

Fig. 10: Actual output waveshape of an amplifier.

ASSOCIATED CIRCUITS

The bottom substrate contains five circuits:

1. The calibration signal generator provides a voltage step whose amplitude is directly proportional to a DC calibration voltage. Minimal strobe feedthrough was achieved by careful design of the signal generator. Design details are given in Ref. 8.
2. The input shift register controls eight sets of CMOS analog switches. Each switch set is made up of two switches connected in a series-shunt configuration to pass or block the calibration signal to their respective amplifiers. The series-shunt configuration minimizes signal feedthrough when the calibration signal is not to be applied to an amplifier. A pattern of ones and zeroes is shifted into the shift register to determine which of the amplifiers is to receive the calibration signal. The output of a shift register on a hybrid can be applied to the shift register of the next hybrid so that a minimal number of wires is required to control many shift registers.
3. The pulsed power circuit uses three transistors to switch the +8V, +5V and -5V power supply buses. The inherent power loss through these switches is ~ 30 mW at 5 % duty cycle operation.
4. The eight discriminators have a common threshold setting which determines the level of triggering. These discriminators provide hit information to an output register.
5. The output register consisting of CMOS gates and shift registers is capable of operating at 20 MHz. This has been implemented in the form of a gate array. The hit information provided by the discriminators is sent to decision making circuits which determine whether the data provided by the amplifiers will be processed or discarded. Data input and output ports are provided for connecting many hybrids together in a daisy chain fashion.

PERFORMANCE OF ASSOCIATED CIRCUITS

All five functional blocks performed as expected with no serious problems. Because of high calibration strobe signal feedthrough due to circuit layout on the first version of the hybrid, the performance of the calibration signal distribution switches could not be evaluated. This part of the circuit has since been revised. However, discrete system testing showed the isolation performance of this switch was ~ 1 %. With all eight amplifiers in the circuit, the settling time of the power up operation was in the order of 350 μs. The output of the amplifier was used for measuring this settling time. Power consumption of the associated circuits is 70 mW at 5 % duty cycle operation.

CONCLUSION

The first version of the hybrid had been tested extensively. Resulting from these tests, changes have been made to minimize crosstalk and signal feedthrough. The high density of components on both substrates and the high level digital signals make the implementation of this front end hybrid very difficult.

ACKNOWLEDGMENTS

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