AlGaN/GaN current aperture vertical electron transistors with regrown channels

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AlGaN/GaN current aperture vertical electron transistors with regrown aperture and source regions have been fabricated and tested. A 2 μm thick GaN:Si drain region followed by a 0.4 μm GaN:Mg current-blocking layer were grown by metalorganic chemical vapor deposition on a *c*-plane sapphire substrate. Channel apertures were etched, and a maskless regrowth was performed to grow unintentionally doped GaN inside the aperture as well as above the insulating layer, and to add an AlGaN cap layer. Cl_2 reactive ion etching was used to pattern the device mesa, and source, drain, and gate metals were then deposited. Devices were achieved with a maximum source-drain current of 750 mA/mm, an extrinsic transconductance of 120 mS/mm, and a 2-terminal gate breakdown of 65 V while exhibiting almost no DC-RF dispersion for 80 μs pulsed $I-V$ curves. The suppression of DC-RF dispersion was shown to result from the absence of the large electric fields at the surface on the drain-side edge of the gate that are present in high electron mobility transistors. Parasitic leakage currents, which were present in all devices, have been studied in detail. Three leakage paths have been identified, and methods to eliminate them are discussed. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1641520]

I. INTRODUCTION

During the past few years, enormous progress has been made in the development of III-nitride semiconductor materials for high voltage, high power, and high temperature electronics applications.[1–3] High breakdown field strength in GaN (2 MV/cm[4]) permits very high voltages to be sustained during operation of these devices. In high electron mobility transistors (HEMTs), breakdown results from an avalanche process that usually occurs near the gate edge on the drain side,[5] where accumulation of charge at high gate-drain voltages results in large localized electric fields. Achieving a high breakdown voltage in a HEMT requires decreasing the electric field at the surface of the channel at the drain edge of the gate. In GaN HEMTs, this has been accomplished by Zhang *et al.* with the employment of an insulated gate structure, and source-drain breakdown voltages of over 1 kV have been achieved.[6] Another promising approach to achieving bulk breakdown limits in nitride-based electronic devices is to employ a current aperture vertical electron transistor (CAVET) structure.

A CAVET is similar to a double-diffused metal-oxide semiconductor (DMOS) structure,[7,8] as illustrated in Fig. 1. A CAVET consists of a source region separated from a drain region by an insulating layer containing a narrow aperture that is filled with conducting material. The source region is comprised of a two-dimensional electron gas (2DEG) formed in the GaN near the AlGaN/GaN heterointerface, while the drain region consists of *n*-type GaN. A device mesa is formed by reactive ion etching (RIE), and source contacts are deposited on either side of the aperture. The drain metal contacts the *n*-doped region below the aperture. Electrons flow from the source contacts along the 2DEG, then through the aperture into the *n*-type GaN and are collected at the drain. The conductivity of the material inside the aperture as well as in the drain region must be much larger than that of the 2DEG so that the total current passing through the device is determined by the conductivity of the 2DEG. Simultaneously, the conductivity of the 2DEG must be much higher than that of the adjacent bulk GaN directly below the 2DEG to ensure current flow through the 2DEG rather than through the bulk GaN. A Schottky gate, located directly above the aperture, is used to modulate the charge in the 2DEG, thereby controlling how much current passes through the aperture and is collected at the drain.

In a CAVET, because the virtual drain (or the pinched off region) is located underneath the gate, charge does not accumulate at the gate edge, so no large fields near the gate edge are present. Instead, our simulations show that the high field region in a CAVET is buried in the bulk below the gate metal. The CAVET, therefore, has the potential to support very large source-drain voltages, since surface related breakdown is eliminated. Additionally, surface related instabilities such as DC-RF dispersion are mitigated.

II. DEVICE FABRICATION

Device layer structures were grown by metalorganic chemical vapor deposition (MOCVD) on a *c*-plane sapphire substrate. The epitaxial growth began with a 2 μm *n*-type (Si doped) GaN drain layer, followed by a 0.4 μm insulating

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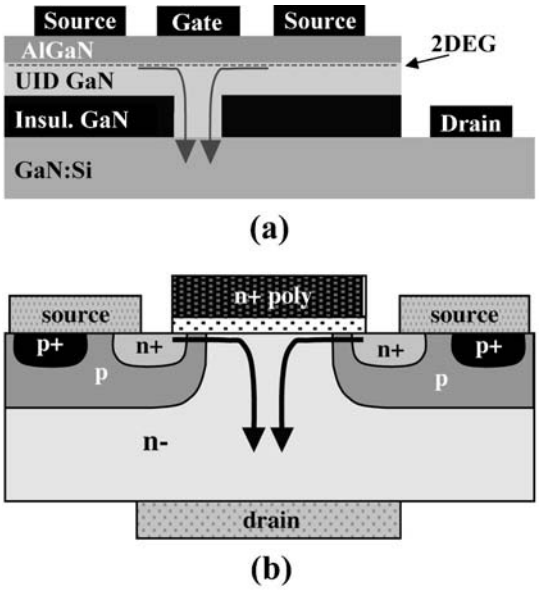

FIG. 1. Schematic diagram of (a) GaN-based Current Aperture Vertical Electron Transistor (CAVET) and (b) DMOS structure.

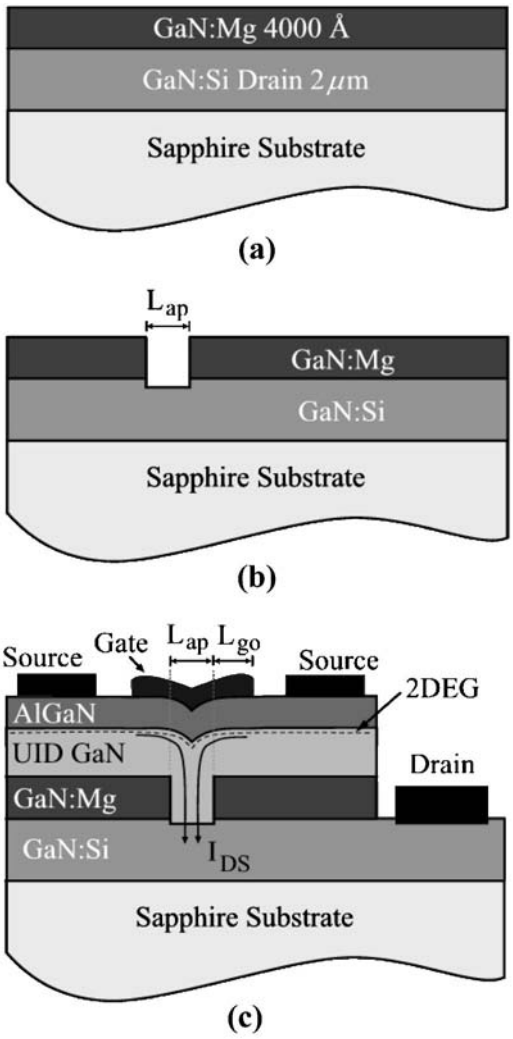

FIG. 2. Schematic diagrams of (a) initial layer structure for CAVET, (b) aperture etch, and (c) completed device.

(Mg-doped) GaN layer [see Fig. 2(a)]. Next, channel apertures were etched through the insulating GaN by Cl_2 reactive ion etching (RIE), as illustrated in Fig. 2(b). Aperture widths (L_{ap}) ranged from 0.6 to 3 μm, and gate overlap lengths (L_{go}) ranged from 0.3 to 5 μm. Alignment marks on each die were then covered by sputtering AlN so that the marks would be visible following regrowth. The wafer was then placed back into the MOCVD chamber and a maskless regrowth was performed. 1700–2500 Å of unintentionally doped (UID) GaN was grown, followed by a 250 Å AlGaN cap, resulting in the structure shown in Fig. 2(c). Interrupted growth studies indicated that the aperture partially filled with GaN while the sample was heated during the regrowth process as a result of mass transport of material from the surface into the aperture.[9,10] The surface directly above the apertures did not entirely planarize during the regrowth; a small depression could still be observed, as illustrated in Fig. 2(c). Material inside and above the aperture region, therefore, was not grown on the *c*-plane, but rather on an inclined or vertical facet. A two-dimensional electron gas (2DEG) is present in the GaN near the AlGaN/GaN heterointerface, enabling the formation of ohmic source contacts and providing the charge that is collected at the drain.

Next, a device mesa for the source and gate region was formed with Cl_2 RIE. Ti/Al/Ni/Au (200/1500/375/500 Å) were then evaporated and annealed at 870 °C for 30 s to form ohmic source and drain contacts. The source metal contacts the 2DEG near the AlGaN/GaN heterointerface, while the drain metal contacts the Si-doped GaN layer at the base of the structure. Finally, Ni–Au (300/3500 Å) was evaporated for a gate metallization, resulting in the device illustrated in Fig. 2(c). None of the devices contained any kind of surface passivation layer.

III. RESULTS AND DISCUSSION

A. Electrical characterization

A Tektronix 370A programmable curve tracer was used to perform the electrical characterization of these devices. The dc $I_{ds}-V_{ds}$ characteristics of a CAVET with a 2 μm wide aperture and a 1 μm gate overlap are illustrated in Fig. 3. This device had a maximum source-drain current ($I_{\max}$) of 750 mA/mm and an extrinsic transconductance (g_m) of $\sim$120 mS/mm at $I_{ds}\sim$650 mA/mm and $V_{ds}\sim$7 V. The pinch-off voltage V_p of this device was -6 V, and the 2-terminal breakdown voltage was $\sim$65 V. Relatively large parasitic leakage currents, which are evident in Fig. 3, prevented a meaningful measure of the 3-terminal breakdown voltage. A comparison of the DC device characteristics to those where the gate was pulsed from pinchoff to their final value reveals that these devices exhibit negligible dispersion for an 80 μs pulse width. Device DC electronic characteristics were found to be independent of the aperture length (L_{ap}) for aperture lengths ranging from 0.8 to 2 μm, indicating that the maximum current $I_{\max}$ in these devices is determined by the available charge in the 2DEG and not by

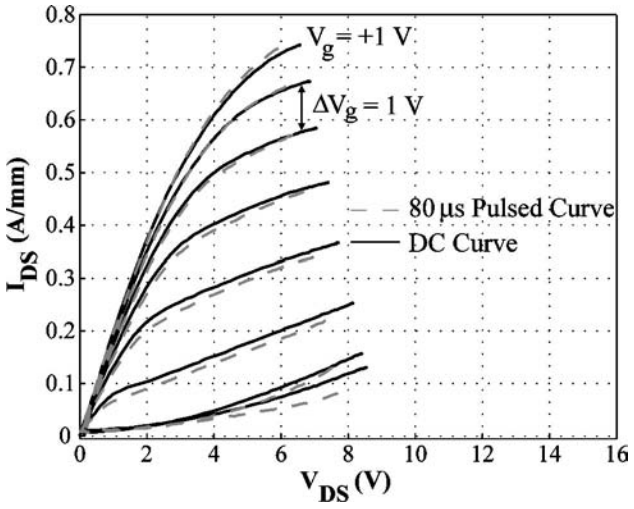

FIG. 3. $I_{ds}-V_{ds}$ characteristics of a CAVET with a regrown channel. Current densities reported here are normalized to the total source width ($W_{source}=2*W_{gate}$, since there are 2 sources, each with the same width as the gate).

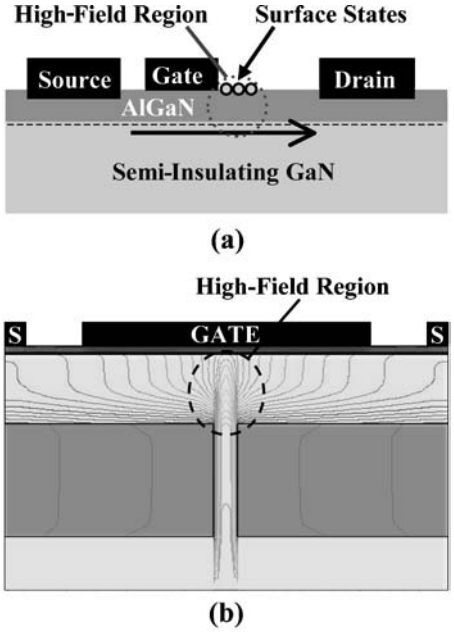

FIG. 4. (a) Schematic diagram of where the high field region occurs in a GaN-based HEMT. (b) Simulation cross section of an AlGaN/GaN CAVET, illustrating constant voltage contour lines and indicating where the highest fields occur. In a HEMT, the high surface fields cause AlGaN surface states to fill, resulting in DC-RF dispersion. In a CAVET, because the fields at the surface are small, surface states remain unoccupied.

the conductivity of the aperture region. The current in some devices which had an aperture length smaller than 0.8 μm was lower than those with larger apertures, indicating that the current in these devices was being limited by the conductivity of the aperture. It should be noted that the current densities (I_{ds}) and transconductances (g_m) reported here are per source pad, so that a meaningful comparison to HEMTs can be made.

B. DC-RF dispersion

In AlGaN/GaN HEMTs, DC-RF dispersion has been attributed to the charging of surface traps at the AlGaN surface in the gate-drain access region,[2,3] as illustrated in Fig. 4(a). When the device is under bias, large electric fields are present at the drain-side edge of the gate, which causes the surface states to fill with electrons until the surface is approximately at the same potential as the gate. When an rf signal is then applied to the gate, the surface states do not respond as quickly as the metallic gate, so the potential at the surface is not able to vary as quickly as the applied rf signal, resulting in the DC-RF dispersion that is commonly observed.

In a CAVET, the drain region is located beneath the gate. As a result, when the device is under bias, the high field region is buried in the bulk rather than at the surface, as indicated by our simulations in Fig. 4(b). The electric field at the surface, which results from the small potential difference between the gate and the source, is relatively small, so the surface states should not fill up with electrons and DC-RF dispersion should be mitigated. The $I-V$ characteristics shown in Fig. 3 support this hypothesis; the device shows negligible dispersion for 80 μs pulses.

In order to further verify this surface-state model for dispersion, the three structures illustrated in Fig. 5 were fabricated on the same material and then tested. The $I-V$ curves of each of these devices for DC and pulsed conditions are shown in Fig. 6. The device in Fig. 5(a) is similar to a standard CAVET. The gate metal extends all the way across the aperture, so the current does not flow underneath the surface on the drain-side of the gate. The only portion of the AlGaN surface that could affect the charge in the channel is the region between the source and the gate. Because the electric field in this region is small, the surface states there should not fill up with electrons, so we expect to see no dispersion in this device. We can see from Fig. 6(a) that this is indeed what occurs.

In the device shown in Fig. 5(b), the gate only extends part way across the aperture. This brings the surface on the drain-side edge of the gate closer to the path of current flow, depicted by the arrows in Fig. 5, which we now refer to as the channel. Occupied surface states in this region could potentially modulate the channel, although because the channel does not run directly under this region, we would expect the effect to be relatively small. Indeed, we see in the $I-V$ curves in Fig. 6(b) that a small amount of dispersion is present in this device.

The device illustrated in Fig. 5(c) is similar to a HEMT. In this device, the gate is completely offset from the aperture. Current passes directly underneath the AlGaN surface on the drain-side of the gate, so any changes in the potential at this surface will directly affect the amount of charge in the channel. We can see in Fig. 6(c) that this indeed results in a device with very high dispersion.

C. Parasitic leakage currents

Unfortunately, all AlGaN/GaN CAVETs with regrown aperture and source regions fabricated to date have exhibited relatively large parasitic leakage currents, often comprising

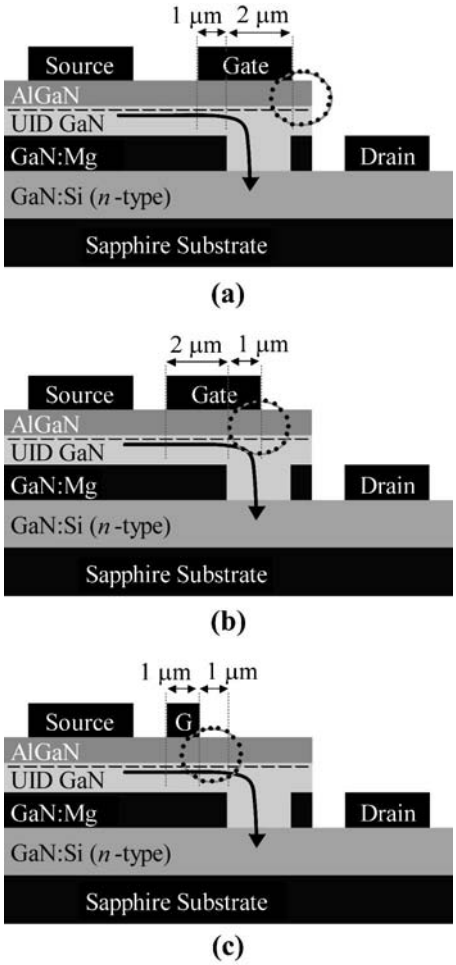

FIG. 5. Three CAVET structures fabricated in order to verify the surface-state model for DC-RF dispersion. (a) Gate completely covers the aperture, drain-side edge of gate is far from the current path. (b) Gate partially covers the aperture, drain-side edge of gate is near the current path. (c) Gate offset from aperture, current passes directly underneath drain-side edge of the gate.

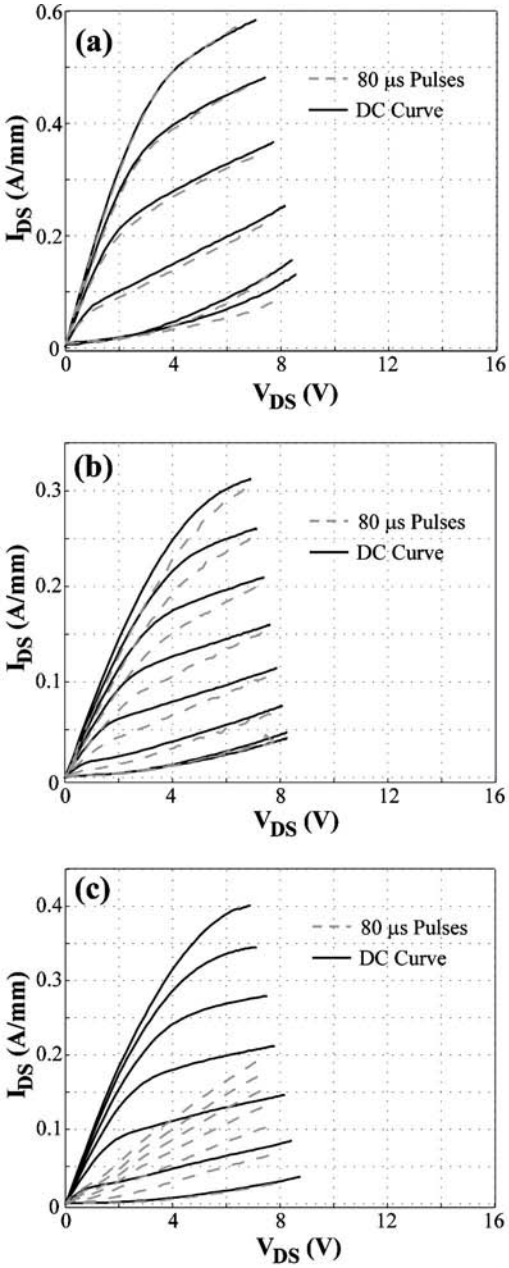

FIG. 6. Measured $I-V$ characteristics for the devices illustrated in Fig. 5. (a) The device in Fig. 5(a) exhibits negligible DC-RF dispersion. (b) The device in Fig. 5(b) shows a little dispersion. (c) The device in Fig. 5(c) shows very high dispersion.

as much as 15% of the total current. These leakage currents resulted in devices that do not pinch off, and they have prevented a meaningful measure of device 3-terminal breakdown voltages, making it impossible to determine whether the large predicted breakdown voltages for a CAVET can be realized. The entire current observed at pinch-off ($V_g = -6$ V) in Fig. 3 consists of leakage currents. In a CAVET, the total leakage current is comprised of three elements: Electrons from the source passing directly through the insulating layer, electrons from the source traveling through the aperture but underneath the 2DEG so that they are not modulated by the gate, and electrons traveling from gate to drain. A schematic diagram of these leakage paths is illustrated in Fig. 7.

In order to study leakage currents in CAVETs, it is important to determine how much each of the three components illustrated in Fig. 7 contribute to the total leakage current. Gate leakage can be measured independently by simply performing a 2-terminal gate-drain $I-V$ measurement. Source leakage through the insulating layer can be approximately measured by performing a 2-terminal source-drain $I-V$ measurement on a device that contains no aperture. Any remain-

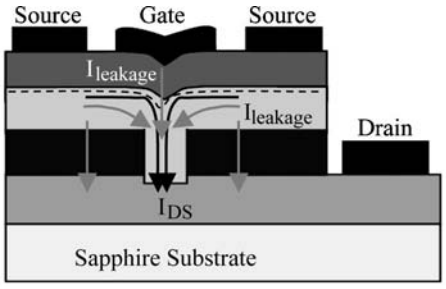

FIG. 7. Schematic of leakage paths in a CAVET (light arrows represent leakage paths).

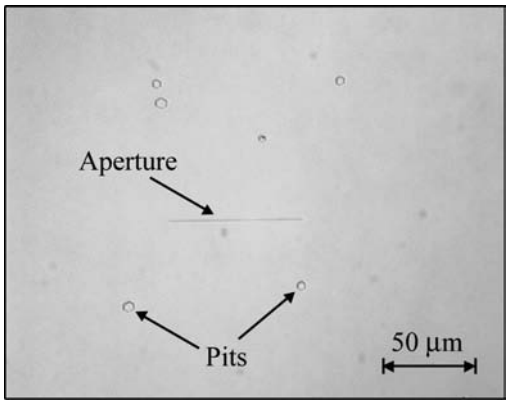

FIG. 8. Optical photograph of surface after it is heated to regrowth temperature and then immediately cooled back down. Pits and surface roughening can be observed. The straight line indicated in the middle is a 75 μm-long aperture.

ing leakage that is not accounted for by these two components must therefore result from electrons traveling through the aperture but underneath the 2DEG.

By performing the above measurements, all three leakage paths were shown to exist for the device with $I-V$ characteristics illustrated in Fig. 3. Subsequent studies were performed to determine what was causing each of the leakage paths to exist and how they could be eliminated.

1. Source leakage through the insulating layer

Interrupted growth studies confirmed that source leakage through the insulating layer resulted from pits formed on the surface at the onset of regrowth, as the sample was heated to growth temperature. A minimum regrowth temperature of 1160 °C was required in order for the region above the aperture to planarize. However, if the sample was heated to this temperature in 6 standard liters per minute (slpm) of NH_3 and 6 slpm of H_2 or N_2 at atmospheric pressure without injecting any trimethylgallium (TMGa), as is our standard procedure, then pits formed at the surface, as seen in Fig. 8. All devices for which the regrowth was performed under conditions leading to pits exhibited large leakage currents through the insulating layer. Eliminating this leakage path required reducing the reactor pressure, reducing the amount of hydrogen present in the reactor by growing in N_2 and reducing the NH_3 flow, and introducing a small flow of TMGa into the reactor prior to reaching growth temperature. Reducing the temperature also kept the pits from forming; however, for temperatures less than 1160 °C, the material above the aperture did not always planarize, in which case gate leakage was much more severe. In order to ensure that pits did not form during regrowth, subsequent devices were heated to regrowth temperature in 3 slpm of NH_3 and 9 slpm of N_2 at a pressure of 300 Torr. Additionally, a small amount of TMGa was injected into the reactor while the temperature was ramped from 1050 to 1160 °C. All devices for which the regrowth was performed under optimized conditions exhibited negligible leakage through the insulating layer.

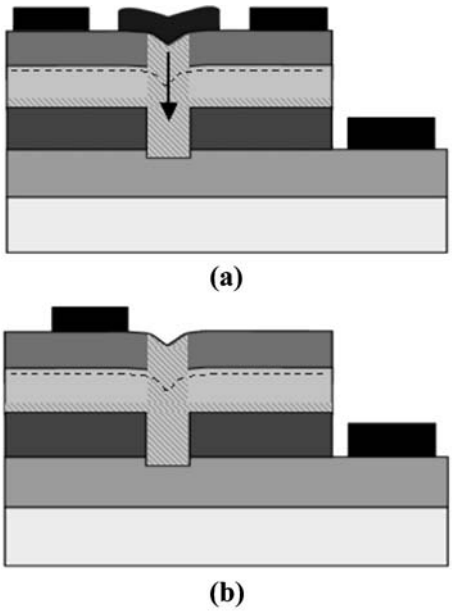

FIG. 9. (a) Schematic of CAVET. Shaded region is unintentionally doped highly n-type during regrowth. (b) Test structure with a gate that is offset from the aperture.

2. Source leakage underneath the 2DEG

It was stated earlier that the conductivity of the 2DEG needs to be much higher than that of the adjacent bulk GaN directly below the 2DEG to ensure current flow through the 2DEG rather than through the bulk GaN. Source leakage underneath the 2DEG occurred when these conditions were not met. Leakage through this path was reduced by keeping the UID layer as thin as possible, insuring that it was fully depleted all the way up to the 2DEG. For UID layers with thickness $\leqslant 1700$ Å, no leakage through this path was observed for drain voltages of up to ~ 50 V, which was the breakdown voltage of those devices. It is possible that in devices with larger breakdown voltages, leakage through this path may be observed at higher drain voltages. In addition, if the UID layer is too thin, the region above the aperture does not always planarize, and so gate leakage becomes more severe.

3. Gate leakage

As stated earlier, material inside as well as above the aperture region was not grown on the c-plane, but rather on an inclined or vertical facet. Other studies have found evidence that GaN which is grown on facets other than the (0001) plane tends to incorporate larger concentrations of n-type impurities.[11,12] We, therefore, believe that the material directly beneath the gate is highly n-type, resulting in a leaky gate Schottky barrier [see Fig. 9(a)]. Because the peak electric field in a CAVET is located directly beneath the gate, this n-type doping causes an increase in the peak field, which limits the breakdown voltage in these devices. Although it is possible that gate leakage results from the enhanced electric fields due to the indentation in the surface underneath the gate, our hypothesis is supported by the fact that in test structures where the gate is offset from the aperture, gate leakage

is eliminated while breakdown voltage remains the same [see test structure in Fig. 9(b)]. If gate leakage had resulted from the enhanced fields caused by the indentation in surface, an increase in the breakdown voltage would be expected when the gate was offset from the aperture.

In order to eliminate gate leakage, we attempted to find growth conditions that would cause the surface to completely planarize almost immediately during regrowth. Conditions that favored planarization included reducing the V/III ratio and increasing the temperature. However, the higher regrowth temperatures required to planarize the surface also resulted in increased source leakage due to the formation of pits while the sample was being heated. At temperatures in which source leakage was eliminated, the surface never fully planarized, so gate leakage was present in all devices. In order to eliminate gate leakage as well as to achieve the high predicted breakdown voltages, it is necessary to be able to better control the doping both within the aperture and underneath the gate. This can possibly be achieved by using an ion implantation to define the insulating layer. In addition, an insulator underneath the gate could be used to further reduce gate leakage. Despite the gate leakage, working devices were still fabricated.

IV. CONCLUSIONS

AlGaN/GaN current aperture vertical electron transistors (CAVETs) with regrown aperture and source regions were fabricated and tested. A device with a 2 μm aperture had a source-drain saturation current of 750 mA/mm, an extrinsic transconductance of 120 mS/mm, and a 2-terminal gate breakdown of 65 V while exhibiting negligible DC-RF dispersion for 80 μs pulsed $I-V$ curves. All devices exhibited parasitic leakage currents, which were broken down into three components and analyzed. Conditions that eliminate source-drain leakage paths both through the insulating layer as well as underneath the 2DEG have been identified and demonstrated. The largest impediment to completely eliminating leakage was the uncontrollable doping levels in the material directly underneath the gate, which led to high gate leakage and lower breakdown voltages. In order to fabricate a leakage-free device and increase breakdown, it is necessary to utilize a process in which doping levels in the aperture region and below the gate can be more precisely controlled, such as using an ion implantation to define the insulating layer.

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