University of California
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High Speed Transceiver Design for Broadband Communications

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of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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To my parents, Abdullah and Meftun, and my brother, Emre, for their unlimited love and support.

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Curriculum Vitæ

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Publications

1. **A. Simsek**, S. K. Kim, M. Abdelghany, S. H. Ahmed, A. Farid, U. Soylu, J. Buckwalter, U. Madhow, and M. J. W. Rodwell, "A 145 GHz multi-beam phased array transceiver using low-cost packaging techniques towards massive MIMO arrays," *in progress for IEEE Transactions of Microwave Theory and Techniques.*
2. **A. Simsek**, S. K. Kim, M. Abdelghany, A. S. H. Ahmed, A. Farid, U. Madhow, and M. J. W. Rodwell, "A 145 GHz fully packaged transceiver in 45-nm CMOS SOI with 5-GBaud data transmission using wirebonding interface to low-cost antenna array," *to be submitted shortly, in 2020 IEEE Radio Wireless Symposium (RWS)*, San Antonio, TX, USA.
3. **A. Simsek**, S. K. Kim, A. Ahmed, R. Maurer, M. Urteaga, and M. J. Rodwell, "A dual-conversion front-end with a W-Band first intermediate frequency for 1-30 GHz reconfigurable transceivers," *in IEEE Radio and Wireless Symposium (RWS)*, Orlando, FL, USA, 2019, pp. 1-4.
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6. **A. Simsek**, S. Arafin, S. K. Kim, G. Morrison, L. A. Johansson, M. Mashanovitch, L. A. Coldren, and M. J. Rodwell, "A chip-scale heterodyne optical phase-locked loop with low-power consumption," *in Optical Fiber Communications Conference (OFC)*, Los Angeles, CA, 2017, pp. 1-3.
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11. S. K. Kim, R. Maurer, **A. Simsek**, M. Urteaga, and M. Rodwell, "An ultra-low power dual-polarization transceiver front-end for 94-GHz phased arrays in 130-nm InP HBT," *in IEEE Journal of Solid-State Circuits*, vol. 52, no. 9, pp. 2267-2276, 2017.
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13. S. Arafin, **A. Simsek** et al., "Power-efficient Kerr frequency comb based tunable optical source," *in IEEE Photonics Journal,* vol. 9, no. 3, pp. 1-14, 2017.
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Abstract

High Speed Transceiver Design for Broadband Communications

by

Arda Simsek

The increasing data consumption due to the development in smart devices demands broadband, high-data-rate communication links both in the user end-point and backhaul links. Backhaul communication links over fiber can further be developed using optical technologies. Millimeter-wave wireless technologies can provide high data rates for both end-users and in base-stations. Millimeter-waves provide wide unlicensed and unallocated frequency bands, creating an opportunity for broadband wireless communications. At these frequencies the signal propagation range is limited and attenuation is high; but signal strength can be recovered in part by using phased arrays. In addition, short wavelengths at these frequencies allow one to place a massive number of antennas within even a small aperture, which can provide a massive number of simultaneous independent beams (multi-input multi-output: MIMO). MIMO can provide large increases in the overall system data rate.

In the first part of the dissertation, two optical phase-locked loops (OPLLs) are demonstrated. These consume 1.3 and 1.8 W of power respectively and have larger than 15 GHz locking ranges. These OPLLs were then integrated with a magnesium fluoride (MgF_2) microresonator-based optical frequency comb in order to show two chip-scale optical frequency synthesizers (OFSs). This comb has a 50-dB span of 25 nm ($\sim$ 3 THz) around 1550 nm with a 25.7 GHz repetition rate. The optical synthesizers consume 2 and 1.7 W of power within a 10 cm^3 volume respectively. The first generation OFS achieves a tuning resolution better than 100 Hz within $\pm$5 Hz accuracy, and can switch 5 nm in

wavelength in less than 200 ns by jumping over 28 comb lines.

In the second part of the dissertation, a broadband transceiver using 22 nm fully-depleted silicon on insulator (FD-SOI) complimentary-metal-oxide-semiconductor (CMOS) technology is demonstrated. The work includes transistor characterization and design of the circuit building blocks. The transmit and receive channels have more than 10 GHz 3-dB bandwidth, sufficient to support more than 10 GBaud data transmission rate. The thesis then reports transmission experiments using an earlier design generation of 140 GHz MIMO transceivers, which was fabricated in 45 nm SOI CMOS. In transmission experiments over 20 cm propagation distance in air, open eye diagrams were observed even at symbol rates as high as 8 GBaud using a 145.8 GHz carrier frequency.

We report low-cost, yet efficient printed circuit board (PCB) based off-chip antenna arrays, and IC-antenna transitions at D-Band. These are the first such reported designs working above 140 GHz. An 8-element single-row, series-fed patch antenna array shows 14 dB gain with 7 GHz bandwidth (S_{21}). It has 9° E-plane and 65° H-plane 3-dB beamwidths. Measurement results align well with the simulations, except that the antenna resonant frequency is 4 GHz higher than design and the gain is 1-1.5 dB lower. A wirebonding transition between the transceiver ICs and antenna arrays are designed. Its performance is evaluated using 3D full electromagnetic simulations in Ansys HFSS. The transition loss is low, only about 1.8 dB, with a 10 GHz bandwidth in simulations. These simulations align well with the measurements from packaged transceivers.

Finally, a fully-packaged 4-channel MIMO receiver and a fully-packaged 2-channel transmitter are demonstrated. In wireless data transmission experiments over a 25 cm propagation distance, a single-channel transceiver using these boards shows open eye patterns up to 5 GBaud data rate using a 146.7 GHz carrier frequency. The bit-error-rate (BER) is measured at less than 10^{-3} up to 2.5 GBaud data rate using the same data transmission experiment. The modules designed in this dissertation are the first fully

integrated phased array ICs working above 140 GHz to the best of the author's knowledge. These modules can support multi-beam communications for the next generation of wireless communications with a massive number of beams, each providing 1-10 Gb/s, approaching 1-10 Tb/s overall data rate.

The material in this dissertation is partly based on the following publications.

- **A. Simsek**, S. K. Kim, and M. J. W. Rodwell, "A 140 GHz MIMO Transceiver in 45 nm SOI CMOS," *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, San Diego, CA, 2018, pp. 231-234.

- **A. Simsek**, S. Arafin, S. K. Kim, G. Morrison, L. A. Johansson, M. Mashanovitch, L. A. Coldren, and M. J. Rodwell, "Evolution of chip-scale heterodyne optical phase-locked loops towards watt level power consumption," *in Journal of Lightwave Technology*, vol. 36, no. 2, pp. 258-264, 2018.

- **A. Simsek**, S. Arafin, S. K. Kim, G. Morrison, L. A. Johansson, M. Mashanovitch, L. A. Coldren, and M. J. Rodwell, "A chip-scale heterodyne optical phase-locked loop with low-power consumption," *in Optical Fiber Communications Conference (OFC)*, Los Angeles, CA, 2017, pp. 1-3.

- A. Farid, **A. Simsek**, A. Ahmed, and M. Rodwell, "A broadband direct conversion transmitter/receiver at D-band using CMOS 22nm FDSOI" *in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2019.

- S. Arafin, **A. Simsek** et al., "Towards chip-scale optical frequency synthesis based on optical heterodyne phase-locked loop," *in Optics Express*, vol. 25, no. 2, pp. 681-695, 2017.

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The dissertation author is the primary contributor of these published works and the coauthors have approved the use of the material for this dissertation.

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Chapter 1

Introduction

The demand for data has increased rapidly during the last few decades due to developments in smart devices and connectivity. Both the end-user and backhaul communications require much higher data rates. Between 2016 and 2022, traffic generated by smart-phones is expected to grow ten times. Moreover, the data traffic per active smartphone per month in 2022 is expected to be 25 GB in North America [3]. As a result, the data requirement in the backhaul links will also be significantly higher. In order to satisfy the data demand in backhaul links, current optical technologies can be further developed to improve the optical fiber-based backhaul links (Fig. 1.1). Although optical fiber links have been developed significantly over the last 3-4 decades, the optical domain is still missing well-defined frequency sources, unlike the microwave domain. A compact, chip-scale, and low-power optical frequency synthesizer can revolutionize optical communications and sensing. Similar revolution happened in the microwave domain 30-40 years ago with the invention of microwave phase-locked loops and frequency synthesizers.

The use of millimeter (mm) and sub-millimeter (sub-mm) waves can provide a broad available spectrum in order to create high-speed, broadband wireless communications. This can create high data rates both at the user-end point and the backhaul links (Fig.

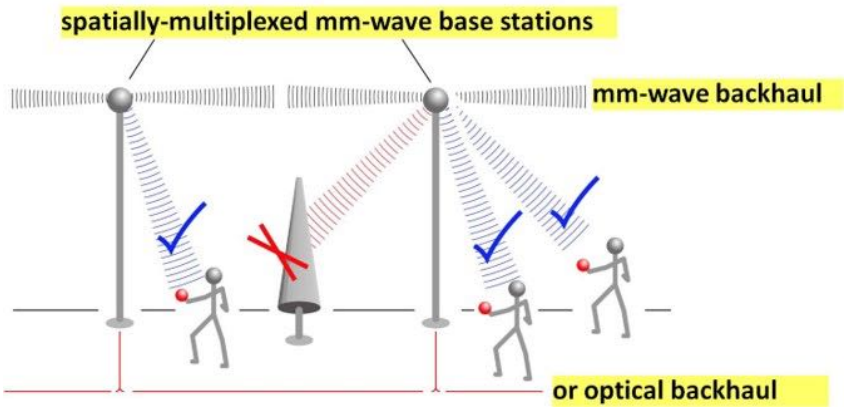

Figure 1.1: Spatially-multiplexed mm-Wave base stations or optical fiber for backhaul links and mm-Wave wireless communications for the user end point (*Courtesy of Prof. Mark J. W. Rodwell*).

1.1). There are some challenges at upper mm-Wave frequencies including the attenuation and signal blockage. However, the signal strength can be recovered using phased arrays, and blockage can be solved using mesh networks and beamforming. These frequencies provide small antennas and transceivers, which provide phased arrays with a massive number of elements. These phased arrays can support multiple independent beams, which can drastically improve the data bandwidth.

In this dissertation, we propose solutions for both the optical communications and the mm-Wave wireless communications, in order to create broadband, high data rate communications. To further develop optical communications, compact, chip-scale, and low-power heterodyne optical phase-locked loops (OPLLs) are proposed to realize chip-scale optical frequency synthesizers (OFSs). Broadband transceivers, antennas and antenna-chip transitions are developed at 140 GHz to create high data rate wireless communications.

1.1 Chip-Scale Optical Frequency Synthesis

Today, radio-frequency/microwave communications is a well-developed technology. It can use the frequency spectrum efficiently, thanks to the invention of chip-scale microwave phase-locked loops and frequency synthesizers. In addition, precise phase and frequency control is possible in the microwave domain using the microwave phase-locked loops. Before this era, systems were bulky and had 100s of crystal oscillators. In order to use the frequency spectrum, switching was performed between these crystal oscillators. Now, a very complicated radio which uses spectrum from 2.5 GHz to sub-6 GHz only requires one crystal reference oscillator. All other frequencies can be created from a well-defined reference using phase-locked loops and synthesizers.

Optical communications have advanced significantly over the last couple of decades, and it is now possible to transmit data rates larger than 100 Gb/s over fiber extending km ranges [4, 5, 6]. However, one of the missing pieces in the optical domain is a chip-scale optical frequency synthesis. This technology can allow optical channel spacing with sub-Hz precision, and create spectrally efficient, compact optical communications. For this revolution, critical components need to be further developed, including chip-scale optical frequency combs, chip-scale, low-power OPLLs, and the widely tunable compact, low-power lasers (Fig. 1.2). Such a synthesizer can also be used to create broadband wireless communications. Examples of these wireless communications have been previously demonstrated via optical frequency generation techniques [7, 8]. With further development in the optical frequency synthesizers, we can significantly improve the data rates both for the wire-line (over fiber) and wireless communications.

In the first part of this dissertation, we propose and demonstrate two generations of OPLLs. Then we present two chip-scale OFSs using these OPLLs. The second generation OPLL, and therefore the OFS, uses a novel, compact, and widely tunable receiver with

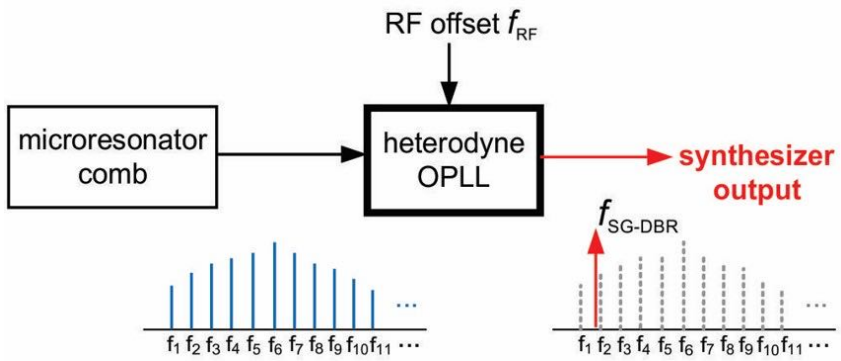

Figure 1.2: Chip-scale optical frequency synthesizer including ultra-stable broadband optical frequency comb generator, compact, low-power heterodyne optical phase-locked loop, and a widely tunable, compact, low-power laser

low power consumption. Low-power consumption makes the second generation systems more attractive. Previously, there has been significant research and development on OPLLs. Prior work demonstrated OPLLs with a larger than 1.1 GHz loop bandwidth [9], with up to 25 GHz offset locking ranges [10], and with phase-error variance of the generated heterodyne signal as low as 0.012 rad^2 for offsets between 1 kHz to 1 GHz [11]. However, most of these systems consume as much power as 3 Watts [12]. In this work, we demonstrated an OPLL with less than 1.3 W power consumption using a low-power photonic integrated circuit (PIC), designed and fabricated by Freedom Photonics LLC [13]. The system is highly integrated in a small volume using an aluminum-nitride (AlN) carrier with wirebonding connections. Without the low-power receiver the first generation OPLL consumes about 1.8 W of power. Both OPLLs can lock to offset frequencies up to 15.2 GHz. They demonstrate phase variances of 0.067 rad^2, and consequently $\sim$ 16 ps timing jitter from 1 kHz to 10 GHz offset frequencies [14].

These OPLLs were then integrated with the ultra-stable, compact microresonator-based optical frequency comb generators provided by OEWaves. There has been extensive research in the development of the optical frequency synthesizers mainly for optical frequency measurements [15], optical spectroscopy [16], light detection and ranging (Li-

DAR) [17], optical frequency metrology [18, 19], and most recently, for optical frequency generation for broadband wireless communications [7, 8]. However, present optical frequency synthesizers have found only limited use due to their cost, size, weight, and power requirements. Therefore, development of the compact, low-cost, and low-power optical frequency synthesizer is significant. In this work, we first developed a chip-scale optical frequency synthesizer using the first generation OPLL and a widely-tunable laser [20, 21, 22]. This is the first reported chip-scale optical frequency synthesizer to the best of the author's knowledge. It shows sub-100 Hz tuning resolution and less than 200 ns switching time between the comb lines separated by more than 5 nm. [20].

After the first realization, we created the second generation OPLL using low-power PIC. Then, we integrated this OPLL with the comb generator to show the lower power version of the synthesizer [23, 24]. This system consumes less than 2 W of power within a 10 cm^3 volume. Using these systems, ultra-stable optical frequencies can be created and utilized to develop optical communications. Using these chip-scale optical frequency synthesizer tools, data rates for the backhaul communication links can be improved either over fiber or through short-range, coherent, broadband wireless communications.

1.2 Millimeter Wave Wireless Communications

There is a large available frequency spectrum at mm-Waves, which can be utilized to create broadband, high-speed wireless communications. Until very recently, these frequencies were only candidates for military applications because the low-cost, high-yield complimentary-metal-oxide-semiconductor (CMOS) technologies had frequency limitations. Until 20 years ago, it was only a dream to design circuits above 60 GHz using CMOS. These frequencies could only be utilized using expensive, low-yield III-V technologies. Therefore, the applications were mostly limited to defense applications. With the

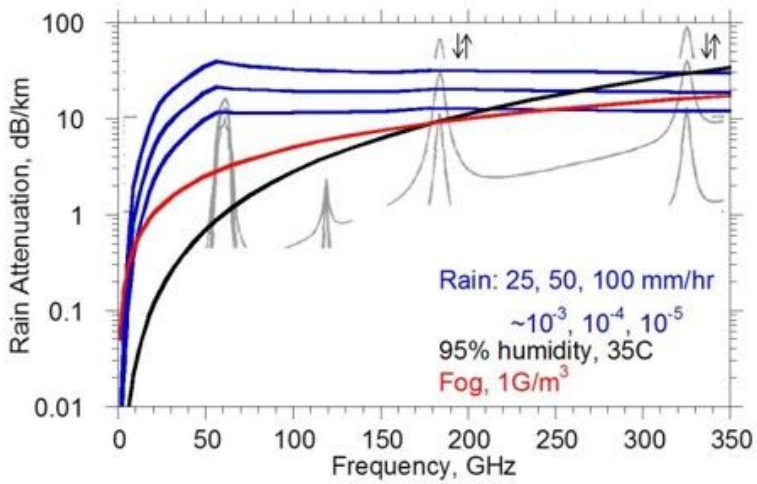

Figure 1.3: Atmospheric attenuation vs. frequency (*Courtesy of Mark J. W. Rodwell*)

improvements in CMOS, it is now possible to design and fabricate low-cost transceivers working above 100 GHz at high-yield [25, 26, 27]. This creates a possibility to use the available spectrum around these frequencies at low cost.

However, there are some challenges at these frequencies including high attenuation and signal blockage. Attenuation is even more severe at 60, 120, 180 and 330 GHz in clear weather due to the oxygen absorption (Fig. 1.3). However, at other frequencies oxygen absorption is not as strong, and lower losses in clear weather are possible. Therefore, frequencies including 90, 140, 220 and 300 GHz are good candidates for wireless communications. In foggy or rainy weather, attenuation is higher and dominant for the broad range of frequencies. The high attenuation problem can be solved using phased arrays, as the signal power can be increased by the number of transmit and receive antennas (Eq. 1.1). Blockage can be prevented using mesh networks and beamforming. Thanks to small antenna sizes at mm-Waves, plenty of base-stations can be placed tightly over light bulbs. If there are objects between the end-user and one base-station, the other base-station can communicate with the user instead, using beamforming. This is called

mesh networks. Beamforming allows the base-station to steer the beams.

$$\frac{P_{received}}{P_{transmitted}} = N_{receive} N_{transmit} \frac{\lambda^2}{R^2} e^{-\alpha R} \tag{1.1}$$

Millimeter-waves allow the placement of a massive number of antennas and transceivers in a small volume, thanks to the short wavelengths. Therefore, phased arrays with a massive number of antennas can be easily realized. This allows multiple independent beams, which increases the data rate linearly with the number of beams supported. This is called multi-input multi-output (MIMO) communications. MIMO provides many advantages, including array gain, spatial multiplexing and diversity gain, and interference reduction [28]. Through spatial multiplexing gain, and using a massive number of antennas, therefore a massive number of beams, MIMO can increase the system data rate significantly. Even with 1 Gb/s per beam, supporting 256 beams from 512 antennas per face of a light bulb, a total of 1024 beams can be supported from four faces with a 2:1 load factor. This creates a data link with a rate of 1 Tb/s. This can revolutionize wireless communications both at the user-end and the base-station.

Phased arrays can support either single beam or multi-beam. Single beam phased arrays increase the array gain to overcome the attenuation and improve the range (Fig. 1.4). However, data rates of the system can only be increased marginally using the available spectrum. Most of the prior work has focused on the single beam systems at mm-Waves, or with only dual-beam through polarization [29, 30, 31, 32, 33]. By using the multi-beam phased array topology in Fig. 1.5, multiple beams can be transmitted simultaneously. This can increase the data rate in proportion with the number of the independent beams. There is no prior multi-beam phased array demonstration at upper mm-Wave frequencies. Only a few works on mm-Wave MIMO systems below 60 GHz have been demonstrated previously [34, 35, 36]. However, for the frequencies above 140

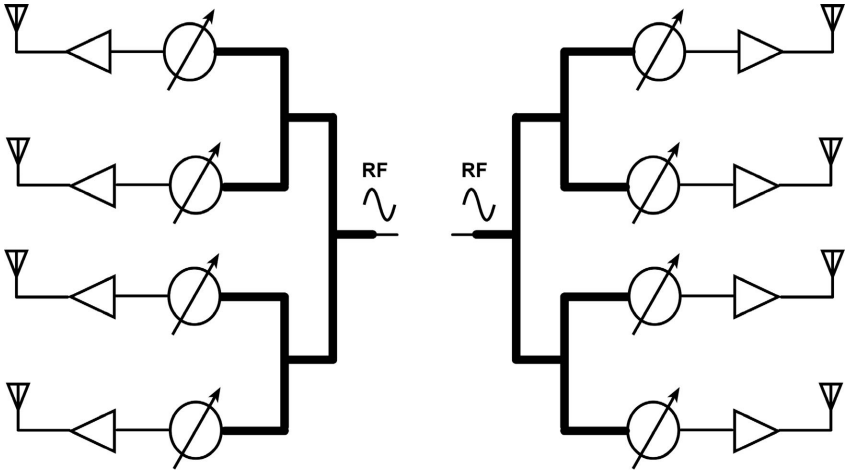

Figure 1.4: Single-beam phased array transceiver block diagram

GHz there is neither single nor multi-beam phased array demonstrations until today. In this work, we demonstrate the first phased array transceivers working above 140 GHz, which can support both single and multi-beam operations.

1.3 Dissertation Contributions and Organization

This work proposes solutions in optical and mm-Wave communications to provide high data rates for both the user-end point and backhaul communication links. Therefore, the work in this dissertation is separated into two main parts. Part I focuses on creating chip-scale, compact, and low-power optical frequency synthesizers using highly integrated low-power OPLLs. Part II focuses on mm-Wave wireless communications to create single and multi-beam phased arrays, to increase the data rates in mobile user end-points as well as the base-stations. This part starts with the design and experiments of direct conversion transceivers using sub-45 nm CMOS technologies. The low-cost antenna and transition designs are then presented to realize fully integrated 140 GHz phased array transceivers.

Chapter 2 demonstrates two highly integrated heterodyne OPLLs, using compact,

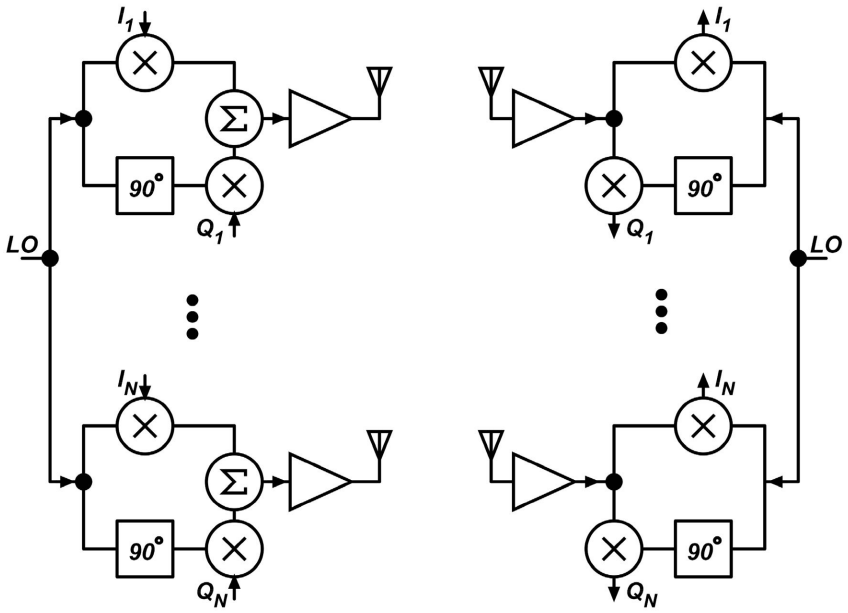

Figure 1.5: Multi-beam phased array transceiver block diagram

highly-integrated PICs, and commercial-off-the-shelf (COTS) electronics for the feedback loop. The first generation (gen-1) PIC consists of a 40 nm widely-tunable sampled-grating distributed-Bragg-reflector (SG-DBR) laser, a 2×2 multi-mode interference (MMI) coupler, a balanced photodetector pair, and a couple of semiconductor optical amplifiers (SOAs) on reference and local-oscillator (LO) optical paths. Gen-1 PIC consumes 660 mW of power, and the resulting OPLL consumes $\sim 1.8\,\mathrm{W}$ power within 2 cm^3 volume. Gen-1 OPLL can lock offset frequencies up to 15.4 GHz. Gen-2 PIC is designed for low power consumption. This PIC incorporates a 60 nm widely-tunable, compact Y-branch laser. The Y-branch laser has a compact cavity with short gain and mirror sections, requiring low current, and subsequently, low drive power. Consequently, gen-2 PIC consumes only 184 mW, and gen-2 OPLL consumes only 1.3 W of power, which is the lowest reported power level for an OPLL. Gen-2 OPLL can lock up to 17.2 GHz offset frequencies. Both OPLLs show $\sim 0.067\,\mathrm{rad}^2$ phase noise variance from 1 kHz to 10 GHz offset interval [13, 14].

Chapter 3 shows two generations of chip-scale optical frequency synthesizers (OFSs) using the OPLLs reported in Chapter 2. Gen-1 OFS consumes 2 W, whereas gen-2 OFS consumes roughly 1.7 W of power. Both OFS generations show a sub-100 Hz tuning resolution within 5 Hz accuracy, and gen-1 OFS demonstrates less than 200 ns switching time between two dozen comb lines ($\sim 5.6\,\text{nm}$). The phase noise variance from 1 kHz to 10 GHz is 0.08 rad^2 for the gen-1 OFS, corresponding to a 14° standard deviation from the locking point [20, 21, 22, 23].

Chapter 4 demonstrates the design and measurements of a broadband direct conversion transmitter and receiver channels at D-Band using 22 nm fully-depleted silicon on insulator (FD-SOI) technology. We also present the transistor characterization and circuit level simulation results. Conversion gain of the entire receiver channel is 27 dB with a 3-dB bandwidth of 20 GHz. The transmitter shows a conversion gain of 18 dB with a saturated output power of 3 dBm. The transmitter and receiver consumes 196 mW and 198 mW respectively, from a 0.8 V supply. The transmitter and receiver both have bandwidth sufficient for 10 GBaud data transmission. Therefore, these ICs can transmit and receive 20 Gb/s for QPSK, 40 Gb/s for 16-QAM, and 80 Gb/s for 64-QAM. To the best of the author's knowledge, this is the first sub-mm-Wave transmitter/receiver chain using 22 nm FDSOI with the lowest supply voltage (0.8V) and the highest bandwidth at D-Band [26].

Chapter 5 starts with the summary of the design and measurements of the previously designed 4-channel MIMO transceivers using 45 nm CMOS SOI technology. Then we report transmission experiments using one channel of these transceivers. In transmission experiments over 20 cm propagation distance in air, we observed open eye diagrams up to 8 GBaud at 145.8 GHz carrier frequency using horn-antennas. When all 4-channels are on, these transceivers consume $\sim 450-500$ mW for transmitter and receiver. The 3-dB IF bandwidth of the receiver is about 10-12 GHz, with 18 dB differential gain. Transmitter

output power is -2 dBm at 1V, and 1 dBm at 1.1 V supply with more than 10 GHz 3-dB bandwidth [37]. The receiver noise figure is simulated as 5.5 dB, but measured as 15 dB due to significant degradation in the measured conversion gain performance. Transmitter LO suppression is more than 20 dB.

Chapter 6 proposes low-cost, yet efficient off-chip antennas and wirebonding transition designs between the antennas and transceiver ICs. We used low-cost printed circuit board (PCB) technology with high performance Isola Astra MT77 material for these designs. We used separate PCBs for the antenna and CMOS carrier, and we adjusted the heights of two different PCBs to have minimum wirebond length. This maximizes the transition performance. Antennas show 13.5-14 dB measured gain, compared to 15-15.5 dB in simulation. They show similar 3-dB bandwidth (S_{21}), and 3-dB E-plane and H-plane beamwidths between simulation and measurements. The wirebonding transition loss between ICs and antennas is simulated as 1.8 dB using the 3D electromagnetic simulator, Ansys HFSS. Experimental results with packaged transceiver boards suggest that the experimental loss of the wirebonding transition compares reasonably well with the simulations. At the end of this chapter, we also propose an initial simulation and design of the more generic packaging, antenna and transition designs using low-temperature co-fired ceramic (LTCC) material to create 8-element modules. This module can easily be tiled to build arrays with a massive number of elements. This module can also incorporate the III-V based high performance amplifiers to increase the system dynamic range.

Chapter 7 presents the first fully packaged 4-channel receiver and a fully-packaged 2-channel transmitter phased arrays using the ICs and the antenna-transition designs reported in Chapter-5 and 6. In data transmission experiments over air with more than 25 cm propagation distance, a single-channel transceiver using these boards shows open eye patterns up to 5 GBaud data rate using a 146.7 GHz carrier frequency. The bit-

error-rate (BER) is measured at less than 10^{-3} up to 2.5 GBaud data rate using the same data transmission experiment. Moreover, beamforming gain is experimentally validated both in the transmitter and receiver. We have sent some working modules to our collaborator, Samsung Research America, to further explore single and multi-beam wireless communication capabilities using their baseband processor. The phased array transceivers demonstrated in this work can be extended to have a larger number of elements. This can either increase the range using a single beam or increase the overall data rate using multi-beam communications.

Part I

Optical Phase-Locked Loops for Chip Scale Optical Frequency Synthesis

Chapter 2

Heterodyne Optical Phase-Locked Loop Design and Demonstrations

2.1 Introduction

Optical phase-locked loops (OPLLs) have been of great interest for the last couple of decades due to the promising applications in the areas of communications, sensing and frequency control [38, 39]. These applications include short to medium range coherent optical communications [12], laser linewidth narrowing [40, 41, 42] terahertz signal generation [42, 43] and optical frequency synthesis [44, 45, 20, 46]. With the improvements in the photonic integration, OPLLs became more attractive since they can offer small loop delay, which allows having OPLLs with loop bandwidths as large as 1.1 GHz [12]. However, these prior OPLLs consume almost 3 Watts of electrical power [12]. This high-power consumption makes the use of OPLLs in practical applications questionable.

Therefore, realizing a low-power consumption OPLL is important to take advantage of recent advances in photonic integration. A chip-scale, compact, and low-power consumption OPLL can push the technology in the aforementioned application areas further

forward. With the proper design of compact photonic integrated circuits (PICs), power consumption in such PICs, and therefore OPLLs, can be lowered [13]. In this chapter, two chip-scale, highly-integrated OPLLs are designed and experimentally demonstrated using two different InP-based photonic integrated coherent receiver circuits. These OPLLs will be used in order to realize optical frequency synthesizers, which will be explained in detail in the next chapter. The whole system eventually will create a possibility to generate broad range of ultra-stable optical frequencies. This can provide a path towards the broadband communications.

The first generation OPLL consumes 1.78 W, whereas the second generation OPLL consumes 1.3 W of power. Both OPLLs have greater than 15 GHz locking range, with roughly 500 MHz loop bandwidth. Tuning range of the PICs used in these OPLLs exceeds 50 nm with a larger than 50 dB side-mode suppression ratio. Phase noise variance is less than 0.1 rad^2 from 1 KHz to 10 GHz offset interval. Proposed transimpedance amplifier (TIA) at the end can allow the OPLL to lock power levels as low as 25 pW.

This chapter begins with a short summary of OPLL system design, electronic loop design and the PIC design. Then the experimental results are presented for the two generations of OPLLs. After this, the power budgets for both OPLLs are provided. Finally, the sensitivity analysis and a proposed solution for a high sensitivity OPLL is provided. This provides a possible research direction to follow upon the findings in this dissertation.

2.2 Optical Phase-Locked Loop System Design

2.2.1 Photonic Integrated Circuit (PIC) Design

We used two different types of PICs in this study for demonstrating heterodyne OPLLs. Therefore, we have named them as gen-1 and gen-2 PICs for clarity. All active/passive components in these PICs are monolithically integrated on an InGaAsP/InP material platform. Details of the fabrication of such PICs can be found in [47, 48]. Microscope images of both PICs are shown in Fig. 2.1.

Out of two PICs, gen-1 PIC (see Fig. 2.1(a)) consists of a 40 nm widely-tunable sampled-grating distributed-Bragg-reflector (SG-DBR) laser, a 2×2 multi-mode interference (MMI) coupler, a balanced photodetector pair and a couple of semiconductor optical amplifiers (SOAs) on reference and local-oscillator (LO) optical paths. Reference optical signal is coupled into this PIC using the upper arm and amplified by two SOAs. SG-DBR laser output propagated in the lower arm. These two optical signals are then combined in a 2×2 MMI coupler and mixed in a balanced photodetector pair to produce the beat note for the electronics part. The SG-DBR laser also has a second output from its backside for monitoring purposes.

Gen-2 PIC (see Fig. 2.1(b)) is designed for low power consumption. This PIC incorporates a widely tunable, compact Y-branch laser, formed between a high-reflectivity coated back cleaved mirror and a pair of Vernier tuned sampled-grating front mirrors, as well as a 2×2 MMI coupler and a balanced photodetector pair. The optical output from one of the front mirrors is connected to the MMI coupler, while the other output from another front mirror is used externally for monitoring the OPLL operation. The Y-branch laser has a compact cavity with short gain and mirror sections, requiring low current and therefore low drive power. It is tuned via Vernier effect and designed for high efficiency at 30° C. The measured tuning range exceeds 60 nm with more than 50

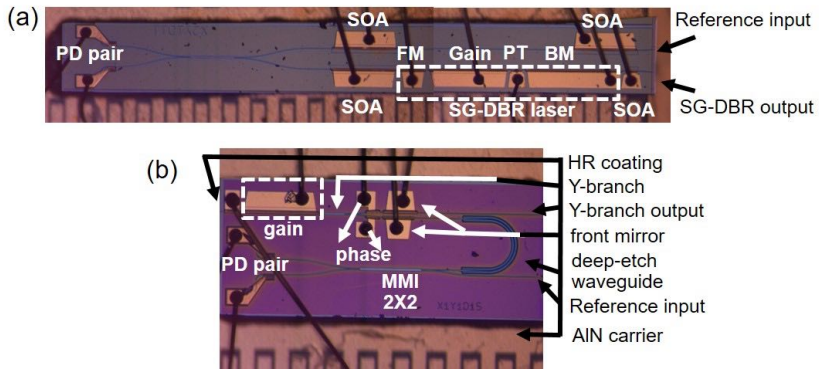

Figure 2.1: (a) Microscope image of the gen-1 InP based PIC. (b) Microscope image of low power consumption gen-2 InP based PIC. (BM: back mirror, FM: front mirror, PD: photodiode, PT: phase tuner, SG-DBR: sampled-grating distributed-Bragg-reflector, and SOA: semiconductor optical amplifier)

dB side-mode suppression ratio [24].

2.2.2 Feedback Electronics Design and OPLL Assembly

Both OPLLs use SiGe-based commercial-off-the-shelf (COTS) electronic ICs and loop filters built from discrete components as the control electronics. Fig. 2.2 shows an exemplary OPLL system assembled by mounting gen-1 PIC and electronic components on a patterned AlN carrier. PIC and electronic ICs are integrated using wirebonds.

In this study, both OPLLs are heterodyne-type, which takes input offset frequency from the external RF synthesizer and locks LO laser to the reference oscillator at this offset frequency. The second order loop filter with a fast feed-forward path is used in feedback electronics in order to get a high loop bandwidth. The circuit schematics of both OPLL systems can be seen in Fig. 2.3(a) and (b). Heterodyne OPLL eliminates the DC errors in the system, therefore it is more immune to optical imperfections.

A limiting amplifier with a 30 dB differential gain and 17 GHz 3-dB bandwidth, and a digital XOR gate functioning as a phase detector [49], together with an Op-amp-based loop filter is used in the feedback electronics. The on-chip LO laser of the PIC

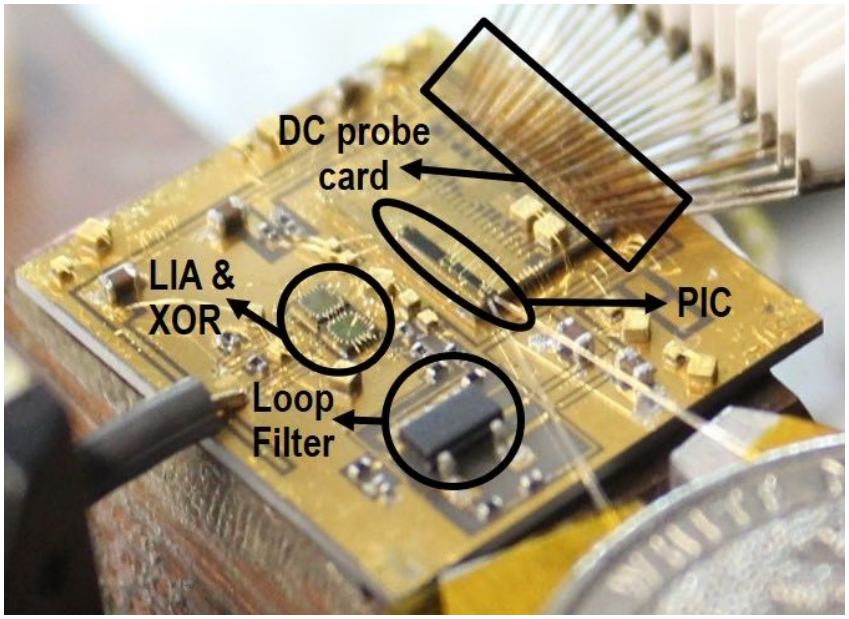

Figure 2.2: OPLL system under measurement setup integrated on an AlN carrier including gen-1 PIC and control electronics

is mixed via the external reference laser through the 2×2 MMI coupler and the PD pair to produce the beat note. This beat note then feeds the electronic ICs. First, it is amplified to logic levels through a limiting amplifier and then mixed via an external RF frequency synthesizer in order to produce an error signal. This error signal goes through the loop filter and feeds back to the phase-tuning section (PT) of the on-chip LO laser. With sufficient feedback gain, this error signal becomes zero and LO laser is locked to the external reference laser at a given RF offset frequency.

Open loop transfer function of an OPLL can be written as a product of gain, and the time constants of the loop [50]. Therefore, open loop transfer function of both OPLLs in this work can be expressed as follows:

$$T(s) = K_{PD}K_{CCO}\frac{1}{\tau_{laser}+1}e^{-\tau_d s}\left[\left(\frac{\tau_2 s+1}{\tau_1 s}\frac{1/R_{out}}{\tau_{opamp}s+1}\right)e^{-\tau_p}+\frac{C_{FF}}{2}\right] \tag{2.1}$$

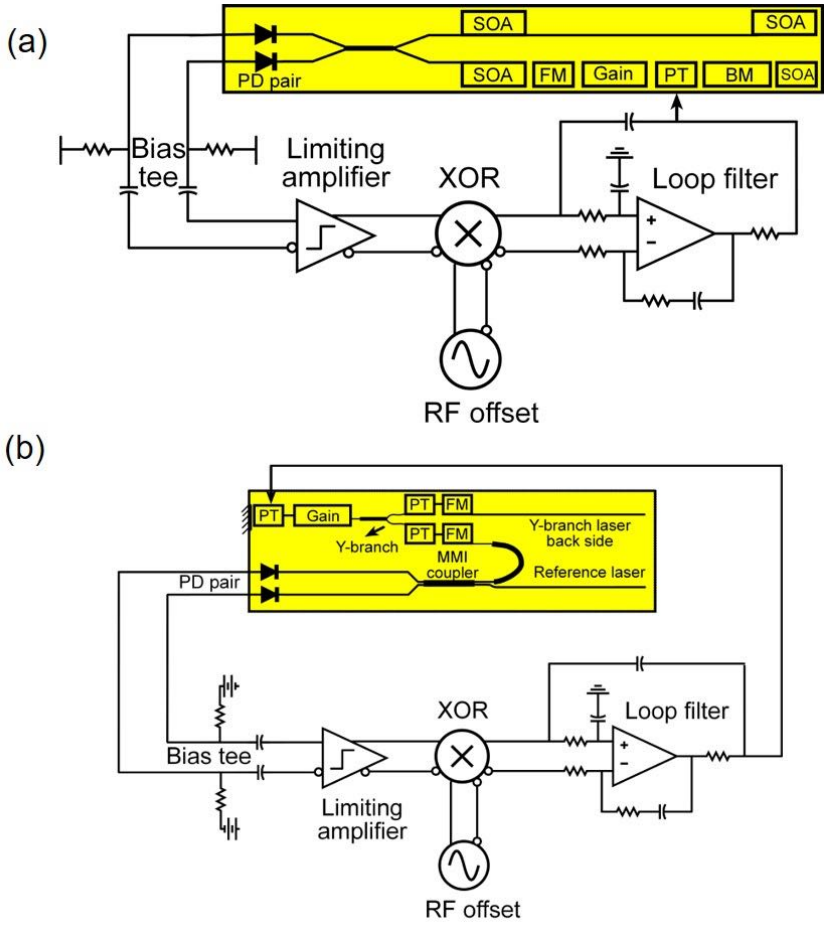

Figure 2.3: (a) Circuit diagram of the first generation OPLL including gen-1 PIC in yellow and the control electronics. (b) Circuit diagram of the second generation OPLL including gen-2 PIC in yellow, and the control electronics.

where K_{PD} is the phase detection gain, K_{CCO} is the laser tuning sensitivity, τ_{laser} is the laser tuning frequency responsivity, τ_1 is the loop filter pole, τ_2 is the loop filter zero, τ_{OP} is the op-amp parasitic pole, R_{out} is the voltage to current conversion resistance at the output, C_{FF} is the feed-forward capacitor and τ_{dop} is the op-amp delay, and τ_d is the total loop delay. Here K_{PD} is a constant value $(2 * V_{logic}/\pi)$ due to the limiting amplifier, which makes the system loop bandwidth insensitive to the optical power level variations. This loop was designed to have a safe phase margin of around $50 - 60^\circ$ at unity gain crossover frequency for both OPLLs in order to realize a robust and stable system.

Loop filter uses a fast feed-forward path through a capacitor in order to further improve the loop bandwidth. Loop equation was coded into Mathematica and loop filter component values were determined using the Mathematica code. Main objective was to get a higher than 500 MHz loop bandwidth with better than 30-40 degrees of phase margin. Detail design procedure of the loop-filter can be found in [9].

2.3 First Generation OPLL Experimental Results

The experimental setup, as shown in Fig. 2.4, was used in order to demonstrate the offset locking with the OPLL using the gen-1 PIC. The reference external cavity laser (ECL) was coupled into the PIC using a lensed fiber from the back side of the PIC. It was then combined with the tunable on-chip SG-DBR laser output in the MMI coupler and mixed to form the desired beat note in the PDs. Light from the SG-DBR laser was coupled out from the lower arm for monitoring purposes. The superimposed optical spectra of the reference laser together with an on chip SG-DBR laser were measured by an optical spectrum analyzer (OSA). At the same time, the resulting RF beat-note was measured by an electrical spectrum analyzer (ESA) through a high speed photodiode.

This experiment shows offset-phase locking between the on chip SG-DBR laser and the external cavity laser (ECL) as the reference. ECL used in this study has the optical linewidth of 100 kHz. Fig. 2.5(a) demonstrates the optical spectrum when the reference laser and the on chip SG-DBR are offset locked at 6 GHz, which is determined by the RF frequency synthesizer. As can be seen in the figure, the separation between the two peaks are about 0.05 nm, which corresponds to 6 GHz frequency separation. In Fig. 2.5(b), the RF beat-note of the reference laser and the on chip SG-DBR laser is presented both in locked and unlocked cases. The relative linewidth of the locked beat note at 6 GHz is in the order of sub-Hz, which is limited by the resolution bandwidth of the ESA. It

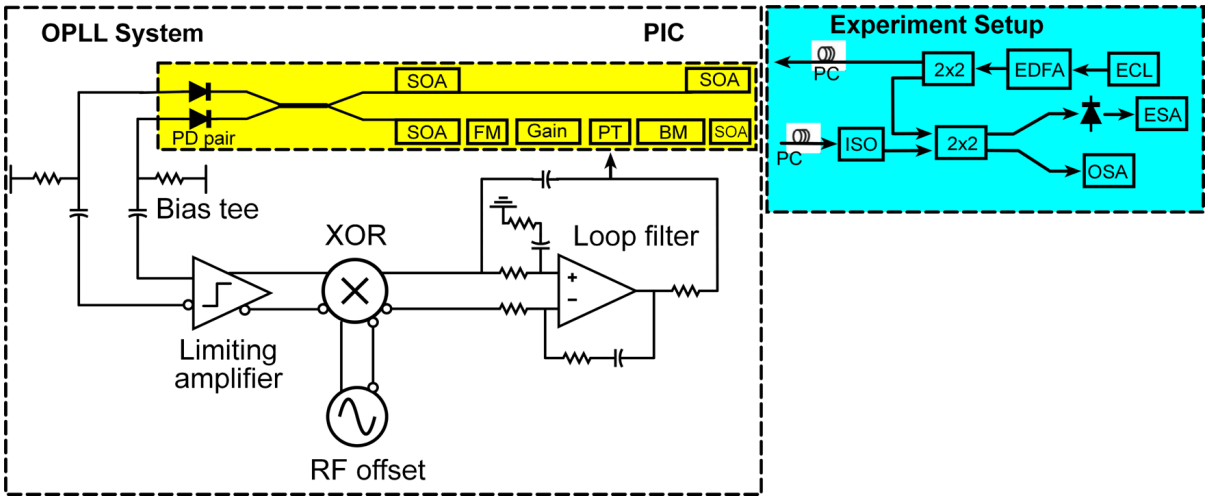

Figure 2.4: a) Experimental setup for the first generation OPLL system. (ECL: external cavity laser, ESA: electrical spectrum analyzer, OSA: optical spectrum analyzer, PC: polarization controller, ISO: isolator)

should be noted that the optical linewidth of our free-running on-chip laser is 10 MHz.

In order to measure the absolute linewidth of the locked beat note, the measurement was performed after adding 20 km of fiber between the upper and lower external 2×2 couplers to de-correlate the ECL from the SG-DBR. In this case, one would expect to get a linewidth of the RF beat note equal to the optical linewidth of the ECL. Fig. 2.6 demonstrates this result. On chip SG-DBR is offset locked at 4.4 GHz, but this time long fiber is added to de-correlate the ECL from the SG-DBR. In this case, the absolute linewidth of the locked beat tone was measured as 100 kHz, indicating the linewidth cloning of the SG-DBR to the ECL.

After proving the phase locking, the offset-locking range was demonstrated for different offset frequencies from 1.14 GHz up to 15.2 GHz as can be seen in Fig. 2.7. The higher the offset locking range, the easier it became for the OPLL to track the reference signal over a broad range of frequencies [11, 51].

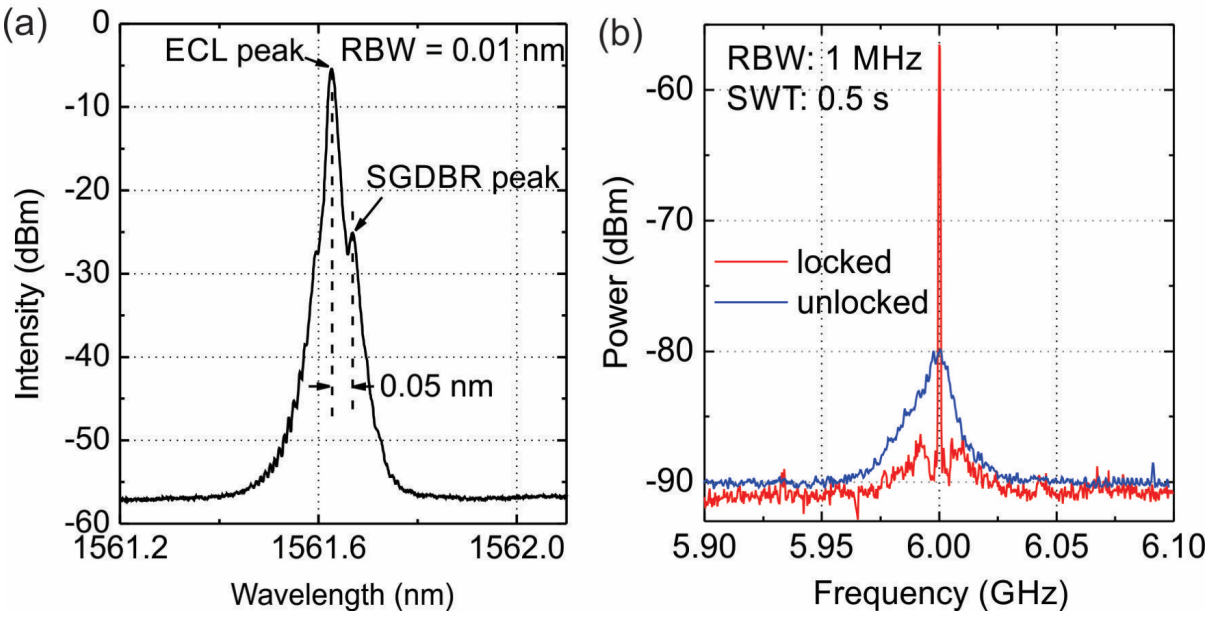

Figure 2.5: (a) OSA spectrum when SGDBR is offset locked to the reference laser at 6 GHz offset, which corresponds 0.05 nm separation in optical domain. (b) Corresponding ESA spectrum when SGDBR is offset locked to the reference laser at 6 GHz offset, blue is before locking and red is after locking.

2.4 Second Generation OPLL Experimental Results

Similar to the first generation OPLL, the experimental setup shown in Fig. 2.4 was used to demonstrate phase locking for the second generation OPLL. In this case, gen-1 PIC was replaced with the gen-2 PIC. This experiment demonstrates phase locking between the on-chip Y-branch laser and the reference laser. Fig. 2.8(a) shows the optical spectrum when the reference laser and the on chip Y-branch laser are offset locked at 8.6 GHz, which is determined by the RF frequency synthesizer. As can be seen in the figure, the separation between the two peaks are about 0.07 nm, which corresponds to 8.6 GHz frequency separation. In Fig. 2.8(b), the RF beat-note between the reference laser and the on chip Y-branch laser is displayed both before the locking and after the locking. The relative linewidth of the locked beat note at 8.6 GHz is in the order of sub-Hz, which is limited by the resolution bandwidth of the ESA. The beat note has a relative linewidth in

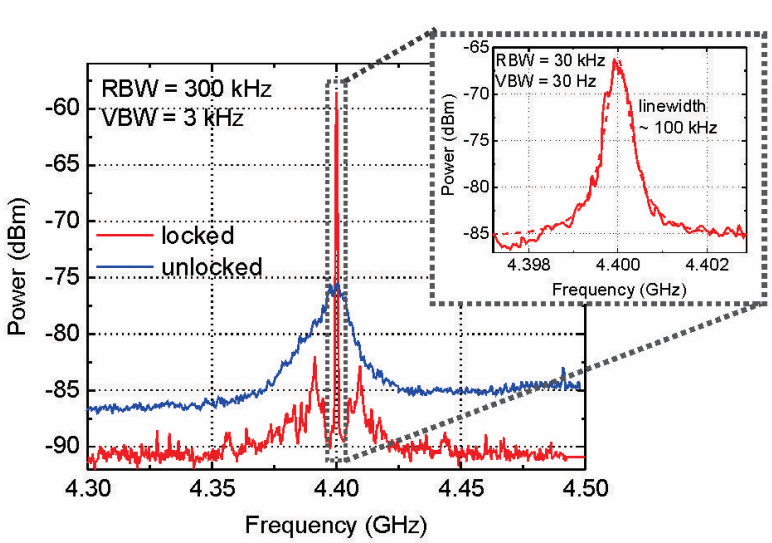

Figure 2.6: (a) ESA spectrum when SG-DBR is offset locked to the reference laser at 4.4 GHz offset. In this case, ECL and SG-DBR are de-correlated using a long fiber. Therefore, relative linewidth of the beat note is equal to 100 kHz, which is the linewidth of the ECL (reference laser).

the order of a MHz before the locking, which is the unlocked Y-branch laser's linewidth [13]. With similar arguments presented for the first generation OPLL, one can add a long enough fiber at the output between the upper and lower external 2×2 couplers to de-correlate the ECL from the Y-branch laser and measure the actual linewidth of the beat note, which is equal to the linewidth of the ECL $\sim$ 100 kHz.

As the next experiment, several offset frequencies from 1 GHz to 20 GHz were applied from the RF frequency synthesizer, and the same phase locking experiment was performed. Fig. 2.9 presents offset locking at several offset frequencies ranging from 1.6 GHz to 17.8 GHz. In addition to the phase locking experiments, the residual phase noise spectral density of the OPLL system was measured when on chip local oscillator is offset locked to the reference laser. Since the loop bandwidth, design procedure and order were not changed from the OPLL with gen-1 PIC to the gen-2 based OPLL, we only provide phase noise spectrum of the former one. Fig. 2.10 shows phase noise spectrum when

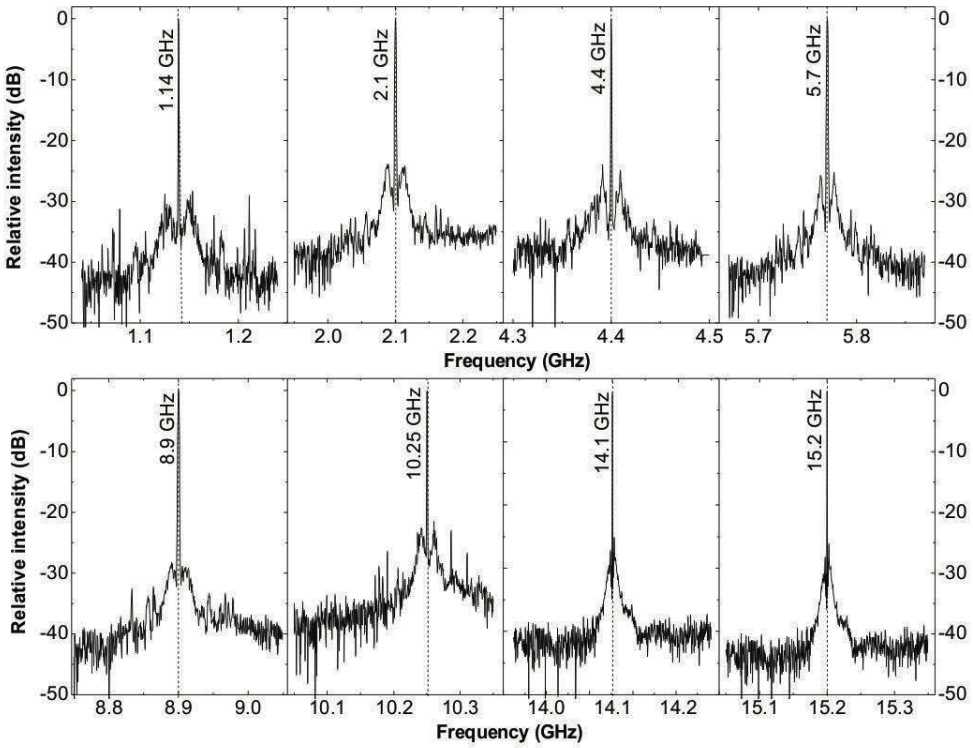

Figure 2.7: (a) Offset locking at multiple frequencies with the first generation OPLL at a RBW of 3 MHz

on chip SG-DBR laser is offset locked to reference ECL at 2.5 GHz. This figure also demonstrates the ESA background and RF synthesizer phase noise spectrum at 2.5 GHz. We calculated the phase noise variance as 0.067 rad^2 from 1 kHz to 10 GHz offset interval. This corresponds to 14.8° standard deviation from the locking point. This OPLL achieves -100 dBc/Hz phase noise at offset of 5 kHz. These results are comparable with the state of the art results in [52, 53].

For our OPLL system, the time domain equivalent of the phase error variance is equal to the timing jitter in the frequency range from 1 kHz to 10 GHz [54], which can

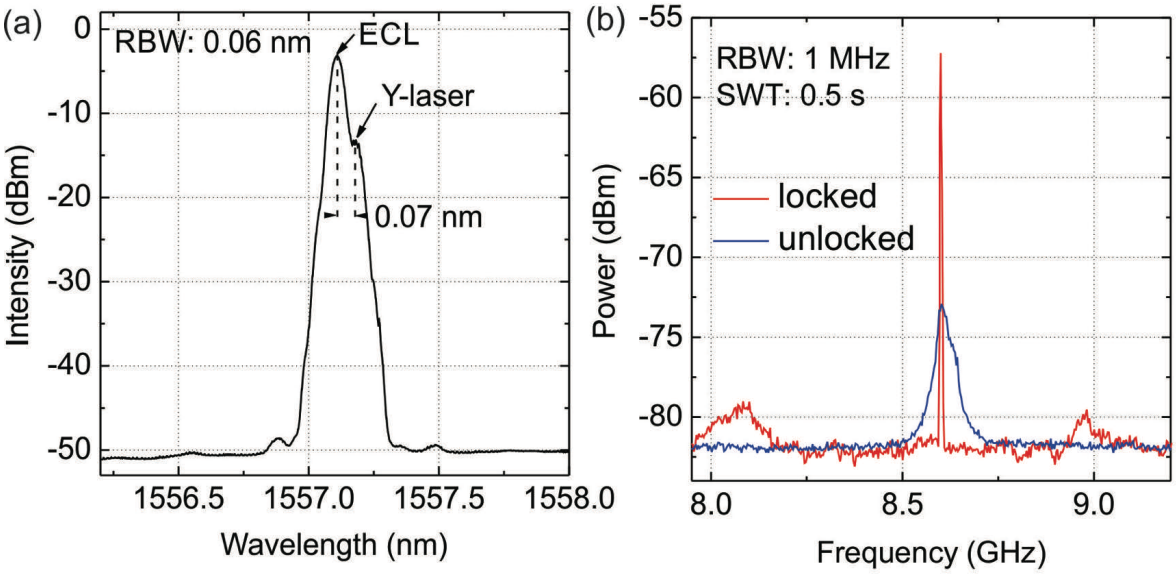

Figure 2.8: (a) OSA spectrum when on chip Y-branch laser is offset locked to the reference laser at 8.6 GHz offset, which corresponds 0.07 nm separation in optical domain. (b) Corresponding ESA spectrum when Y-branch laser is offset locked to the reference laser at 8.6 GHz offset.

be calculated as:

$$Jitter = \frac{\sigma}{2\pi \times f_{offset}} = \frac{0.067}{2\pi \times 2.5 \times 10^9} = 16.48\,\text{ps} \tag{2.2}$$

This chapter demonstrates a proof-of-principle demonstration of optical phase locking to a reference laser with low power consumption. This system can be integrated with a better reference sources such as microresonator-based optical frequency combs to synthesize arbitrary pure optical frequencies [20, 24]. Also, such narrow RF beat tones generated by beating on-chip laser with the comb lines can be used in wide range of applications, including short to medium range optical communications, as well as broadband wireless communication in microwave photonic link technology. This way we can create broadband wireless communications to overcome the demand for the ultra wideband and high speed wireless communications. Locking these OPLLs to microresonator-based

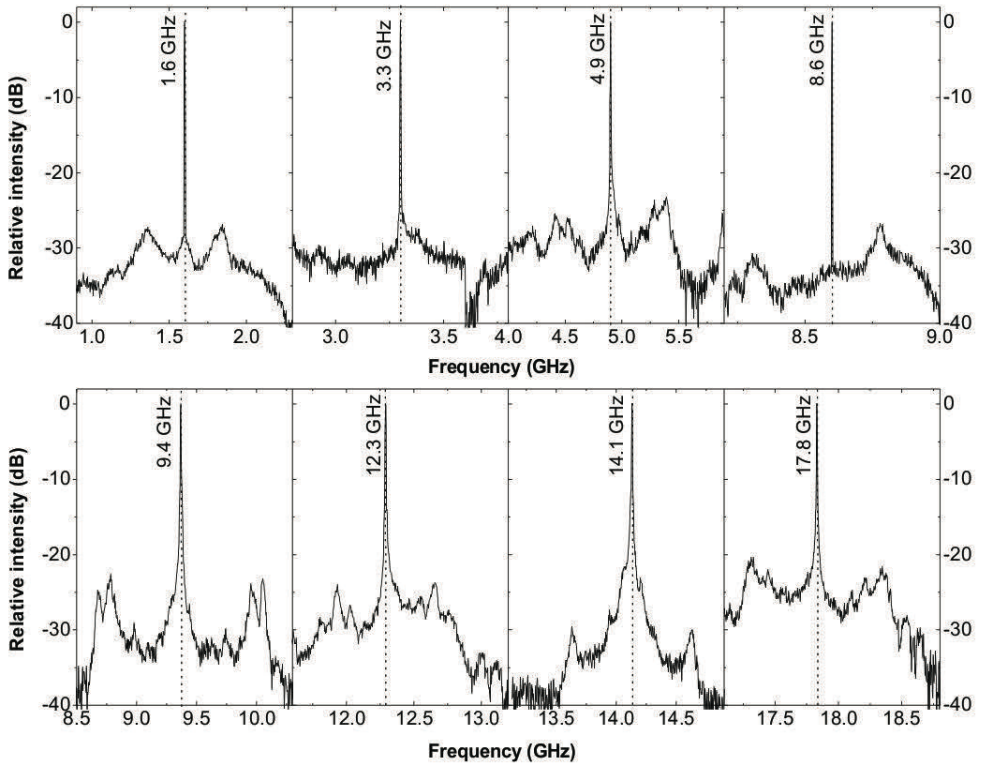

Figure 2.9: Offset locking at multiple frequencies with the second generation OPLL at a RBW of 3 MHz

comb sources will be presented in the next chapter.

2.5 Power Budgets for Both OPLLs

As mentioned, one of the primary objectives for this work was to realize a compact, chip-scale OPLL with Watt-level power consumption. This low power consumption OPLL, eventually will be integrated with a microresonator-based comb source to realize Watt level chip-scale optical frequency synthesizer. In order to reduce the power consumption of an OPLL, one can improve the control electronics, PIC or both. In this work a novel, compact, and low power consumption PIC is utilized with moderate power

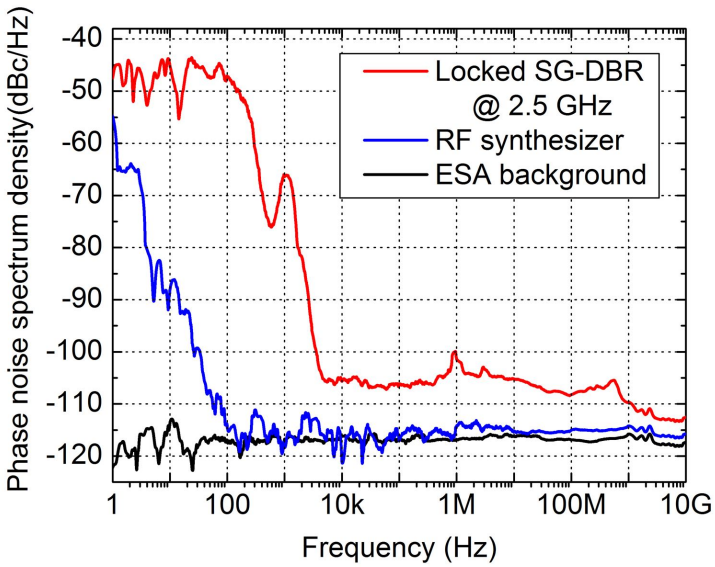

Figure 2.10: Single-sideband residual phase noise of the heterodyne OPLL at 2.5 GHz offset locking. Phase noise results of the RF synthesizer at 2.5 GHz, and background is also shown here.

consumption COTS ICs as a possible solution to realize a chip scale, Watt level OPLL. Table 2.1 and 2.2 provides the power consumption of gen-1 PIC, gen-2 PIC, control electronics and overall OPLL systems. (Numbers in the parentheses for each section in the PIC part tell how many of them are integrated in the PIC, BM: back mirror, FM: front mirror, LIA: limiting amplifier, PD: photodiode, PT: phase tuner, SOA: semiconductor optical amplifier)

As can be seen from table 2.1 and table 2.2 gen-1 PIC consumes 660 mW, whereas gen-2 PIC consumes only 184 mW. Together with the control electronics, the OPLL with gen-2 PIC only consumes record-low 1.3 Watts of electrical power.

	Section	Current (mA)	Voltage (V)	Power (mW)
Gen-1 PIC	**Gain (1)**	73	1.5	109.5
	FM (1)	30	1.5	45
	PT (1)	7	1.3	9.1
	PD (2)	1	2	4
	BM (1)	120	1.5	180
	SOA (3)	70	1.5	315
PIC-1 TOTAL				**662.6**
Electronic ICs	**LIA**	180	3.3	594
	XOR	130	3.3	429
	Op-amp	16	6	96
Electronic ICs TOTAL				**1119**
Total Power Consumption Gen-1 OPLL				**1.78 (W)**

Table 2.1: Power budget for the first generation OPLL, PIC provides 10 mW optical power

	Section	Current (mA)	Voltage (V)	Power (mW)
Gen-2 PIC	**Gain (1)**	73	1.5	109.5
	FM (2)	20	1.3	52
	PT (2)	7	1.3	18.2
	PD (2)	1	2	4
PIC-2 TOTAL				**184**
Electronic ICs	**LIA**	180	3.3	594
	XOR	130	3.3	429
	Op-amp	16	6	96
Electronic ICs TOTAL				**1119**
Total Power Consumption Gen-1 OPLL				**1.3 (W)**

Table 2.2: Power budget for the second generation OPLL, PIC provides 10 mW optical power

2.6 Sensitivity of the OPLL System

For practical applications including coherent optical communications and optical frequency synthesis, OPLLs should be able to lock to input reference power levels in the order of μWs or even 10s of nWs. In this section, we provide a sensitivity analysis and experimental results of the OPLL. In addition to these results, we present a novel high gain trans-impedance amplifier (TIA) and a possible OPLL using this TIA. This TIA

can lock to input power levels as low as 25 pW.

Both OPLLs in this work employs SiGe based COTS limiting amplifier, which has 30 dB differential gain. InP based PICs have on chip tunable lasers, which produces reasonable amount of optical power. This is mixed with the reference input power through 2×2 MMI coupler and the PDs. The detected electrical signal is then fed into the limiting amplifier having a 50 Ω common mode logic interface. In this system, the minimum required input current level from the balanced PD pair can be found as follows, where $V_{INPUT,MIN}$ represents the minimum required voltage level just before the limiting amplifier and $I_{BEAT,MIN}$ represents the minimum required beat current produced by the photodiodes:

$$Gain_{LIA} = 30\,\mathrm{dB} = 31.6 \tag{2.3}$$

$$V_{INPUT,MIN} = \frac{300\,\mathrm{mV}}{31.6} = 9.5\,\mathrm{mV} \tag{2.4}$$

$$I_{BEAT,MIN} = \frac{9.5\,\mathrm{mV}}{50} = 0.19\,\mathrm{mA} \tag{2.5}$$

From the above equations, we found out that the minimum input current level for offset locking with the designed OPLLs is around 0.19 mA. Given the responsivity of the on-chip PDs is around 1 ($\frac{A}{W}$), the minimum input beat power is around 0.19 mW. If we use this in the coherent detection equation, we can get the minimum required input power level from the reference laser as follows, where I_{BEAT} represents the beat current produced by the PDs, I_{LO} is the current produced by LO laser and I_{INPUT} is the current

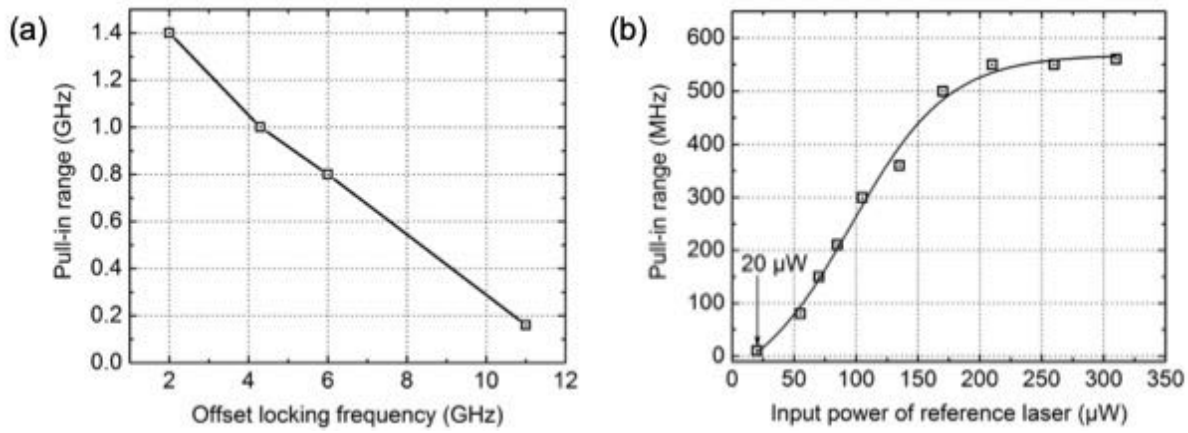

Figure 2.11: (a) Pull-in range vs. offset locking frequency (b) Pull in range vs. input power of the reference external cavity laser. Minimum input power required for locking was found 20 W experimentally.

produced by the reference laser.

$$I_{BEAT} = 2 \times \sqrt{I_{LO} \times I_{INPUT}} \tag{2.6}$$

$$I_{INPUT,MIN} = \frac{I^2_{BEAT,MIN}}{4 \times I_{LO}} \tag{2.7}$$

$$I_{INPUT,MIN} = 9\,\mu\text{A} \tag{2.8}$$

Therefore, the minimum input power required to offset lock this OPLL is theoretically about 9 μW, which is close to the experimental results demonstrated in Fig. 2.11(b). The minimum input power level required to operate the OPLL system is 20 μW experimentally.

Fig. 2.11(a) and (b) demonstrates the pull-in range of the OPLL system with respect to offset locking frequency and input power levels respectively. Pull-in range varies from 1.4 GHz to 200 MHz depending on the offset frequency range. As expected, the pull-in range decreases with increasing offset frequencies, since the gain of the overall loop

reduces. Similarly, decreasing input power levels reduces the pull-in range, and eventually at some point OPLL stops working with the certain input power levels. This minimum input power level is 20 μW (Fig. 2.11(b)). In order to improve the sensitivity of the OPLL further, an application specific trans-impedance amplifier (TIA) with low noise, high gain and wide bandwidth using 130nm SiGe HBT process was designed. This chip was designed for 80 dB voltage gain and 120 dBΩ trans-impedance gain with 30 GHz 3-dB bandwidth. It has less than 10 pA$\sqrt{\text{Hz}}$ input referred noise current density up to 20 GHz with respect to 50 fF photodiode capacitance according to the circuit level simulations. With this TIA minimum input power level of reference signal can be reduced to as low as 22.5 pW as follows, where each symbol is used the same way as explained previously:

$$Gain_{TIA} = 120\,\text{dB}\Omega = 1\,\text{M}\Omega \tag{2.9}$$

$$I_{BEAT,MIN} = \frac{300\,\text{mV}}{10^6\,\Omega} = 0.3\,\mu\text{A} \tag{2.10}$$

$$I_{BEAT} = 2 \times \sqrt{I_{LO} \times I_{INPUT}} \tag{2.11}$$

$$I_{INPUT,MIN} = \frac{I^2_{BEAT,MIN}}{4 \times I_{LO}} \tag{2.12}$$

$$I_{INPUT,MIN} = 22.5\,\text{pA} \tag{2.13}$$

Using this TIA, one can make a highly sensitive OPLL, which can be used in optical communications and optical frequency synthesis systems. Fig. 2.12 shows the proposed OPLL system using this novel TIA. The COTS SiGe limiting amplifier is replaced by this

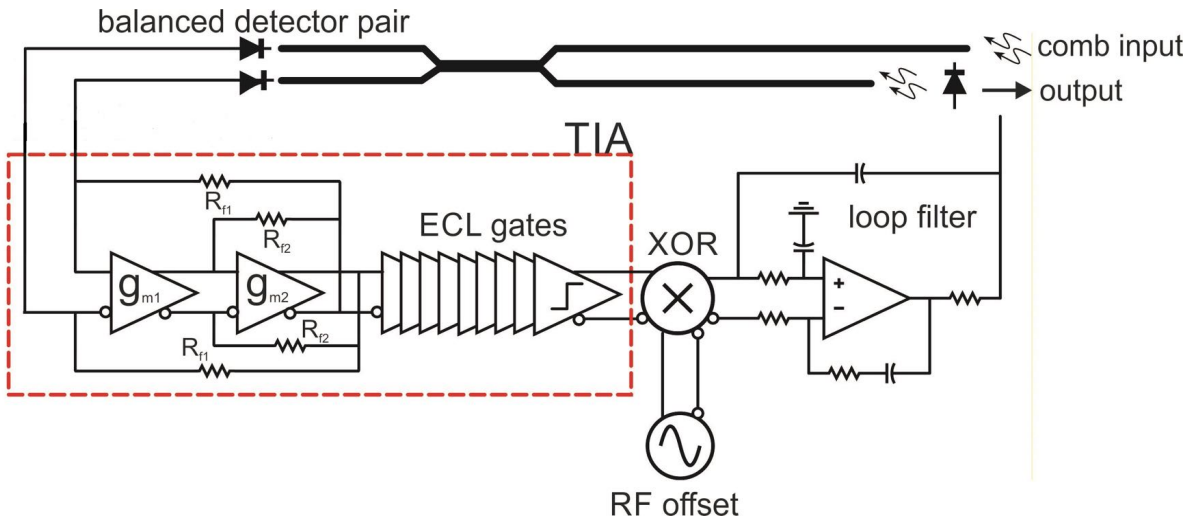

Figure 2.12: Schematic of the sensitive OPLL with low noise, high gain trans-impedance amplifier.

TIA in the proposed OPLL system. Please note that TIA gain was measured functionally to be 60 dB without DC restoration loop. With a proper DC restoration loop, one can get the simulated gain of 80 dB from the TIA. The study relating to the sensitive OPLL system with these high-performance TIAs have not been completed due to the other priorities for the projects and the time-line. However, here this is documented so that this approach can be further investigated as a future extension of this work.

2.7 Conclusion

In this chapter of the dissertation, two chip-scale OPLLs are designed and demonstrated. Using a novel, low power consumption InP-based photonic integrated receiver circuit overall power consumption of the first generation OPLL is significantly reduced. The second generation OPLL consumes only 1.35 W of electrical power, which is the lowest power consumption reported for an OPLL to the best of author's knowledge. Both OPLLs have roughly 500 MHz loop bandwidth, with 0.067 rad^2 phase noise variance from 1 kHz to 10 GHz. Offset locking ranges are 15.2 GHz and 17.8 GHz respectively.

Minimum input power level required from the reference side for phase locking was measured to be 20 μW. Novel application specific electrical IC is proposed for lowering the sensitivity of such OPLLs to as low as 25 pW. For the future, the sensitivity of the OPLL can be increased significantly using the proposed TIA designs. Also these ICs can be designed using sub-45 nm CMOS processes to further reduce the power consumption of the electronic feedback loop. With these developments, highly integrated OPLLs with less than 0.5 W of power consumption can be realized. This allows us to create chip-scale, low-power, and broadband optical frequency synthesizers. These synthesizers can be used to develop broadband communications.

Chapter 3

Chip Scale Optical Frequency Synthesis

3.1 Background and Motivation

There has been recent and extensive research in the development of optical frequency synthesizers (OFSs) with applications including absolute optical frequency measurements [15], optical spectroscopy [16], gas sensing [55], light detection and ranging (LiDAR) [17], and optical frequency metrology [18, 19]. Despite their widespread potential applications, present optical frequency synthesizers have found only limited use due to their cost, size, weight, and DC power requirements. Considering this, realization of a compact, low-cost, and low-power OFS is a key requirement. These goals suggest highly-integrated chip-scale designs. However, it is challenging to integrate various optical and electronic devices on the same chip. Low power consumption is especially important because thermal cross-talk and associated thermal management may prevent the tight integration of the optical components.

An OFS includes several key elements. An optical frequency comb with stable lines

covering a broad range of frequencies defines the frequency of the generated optical signal. A broadly tunable laser or bank of lasers are required to be locked to the optical frequency comb. High speed electronic circuits are required to achieve this offset locking between the tunable laser and the optical frequency comb.

Despite being fully-locked and referenced, commercially-available optical frequency synthesizers involve bulk optics and electronics. They consume power on the order of kW. This power is primarily consumed by the optical frequency comb generators. Mode-locked femtosecond optical frequency combs lay in the core of the OFS approaches [56, 57, 58, 59]. Commercially available systems based on titanium sapphire or fiber laser based femtosecond mode-locked lasers are 0.14 m^3 in volume and consume 0.5 kW power [60].

The problem of the power-efficient optical frequency comb generator can be solved using optical microresonators [61]. Microresonator-based Kerr frequency combs are suitable for on-chip integration [62]. Another advantage is that compared to traditional mode-locked or femtosecond laser-based optical frequency comb (OFC), a microresonator-based comb uses few hundreds of mW power. It provides ultralow noise and phase-coherent output with spectral linewidths on the order of sub-Hz. While monolithic planar resonators integrated on various platforms were demonstrated [63, 64], none of them were integrated with the pump laser. Hence none of them represent complete chip-scale devices. The reason is that the power required to produce the frequency combs is usually in hundreds of mW range, which makes the chip integration impractical. The large power consumption by the laser as well as significant attenuation of the pump light in the microresonator complicates the thermal management of the system as the whole. To reduce the power consumption, one needs high quality (Q) factor microresonators.

The frequency comb generator is based on the crystalline whispering gallery mode (WGM) resonator that has the following advantages over other devices of this kind [65,

66]. Firstly, it has low intrinsic loss (if overloaded) and high intrinsic Q-factor [66]. As the result, it is possible to reduce absorption of the light in the resonator. Secondly, the resonator has outstanding thermo-mechanical properties that allow realizing ultra-narrow linewidth lasers on a chip using self-injection locking of the laser to the resonator. The optical frequency comb oscillator benefits from the laser and, as the result, the relative optical stability of each comb harmonic does not exceed 10^{-10} at 1 second [2]. Thirdly, high optical Q allows reducing fundamental noises of the Kerr comb oscillator. The noises are further reduced since proper design of the resonator morphology results in increase of the volume of the optical mode need for reduction of the thermodynamic noise associated with the resonator. Fourthly, the resonator has small mass and large mechanical Q that reduces its acceleration and vibration sensitivity[67]. This feature is supported by the low acceleration sensitivity of the whole oscillator platform. Despite the fact that WGM resonators were created on a chip, the efficient planar couplers are yet to be developed for them. Preliminary studies show that it is possible [68, 69].

The Kerr frequency comb generated in the microresonator results from the process of four-wave mixing [70]. The comb emerges when the pump power exceeds a certain threshold. Pump power is produced by the continuous-wave laser, self-injection locked to a mode of the resonator. The resonator is characterized with the ultimate anomalous group velocity dispersion and supports formation of the intra-cavity dissipative solitons [71]. The frequency comb stability is defined by the stability of the pump light, on one hand, and the repetition rate of the soliton train, on the other. Both values are extremely good. As the result, the whole oscillator represents an ultimate reference for creation of the OFS.

The OFC coherence can change through its spectrum, resulting a broader spectral linewidth for comb components that are away from the pump wavelength [72]. However, for a practically realizable spectrally narrow mode-locked Kerr frequency comb, this is

not the case as the phase noise of the comb repetition rate is low [2], if compared with the properly normalized noise of the pump laser [1]. Moreover, in an ideal case, the repetition-rate noise of the Kerr frequency comb does not depend on the pump laser noise and can be extremely low [73, 74]. It means that for the narrow OFC reported here, we can neglect repetition rate induced phase noise and assume that all the optical harmonics have sub-Hz linewidth corresponding to the pump laser.

An optical frequency comb generates a series of discrete optical frequency harmonics, whereas an OFS has to provide a continuous tuning of the optical frequency. To realize this functionality, one needs a widely tunable laser that can be frequency locked to the optical frequency comb. There are several locking approaches such as optical injection locking (OIL), optical injection phase-lock loop (OIPLL) and optical phase-lock loop (OPLL) to achieve this functionality. Optical frequency synthesis with a wide tuning range is not possible using OIL approach alone due to the system instability above critical injection levels[75, 41]. Moreover, OIL is purely a homodyne technique which does not allow for continuous tuning of an offset between the slave laser and the comb. Continuous tuning over a wide range of frequencies was achieved through the combination of OIL and OPLL technologies[76, 45]. However, such a hybrid system increases the system complicity and the issue of offset tuning still remains.

Phase locking a tunable local oscillator to the OFC using chip scale OPLLs is, therefore, considered as the most popular ways of achieving OFSs [77, 78, 79]. With the developments in PIC and electronic IC integration, small loop delays and large loop bandwidths are possible. Hence the realization of OPLLs is a more appealing solution compared to OIL, and OIPLL [53]. Two such examples of these OPLLs are demonstrated in the previous chapter. The so-called heterodyne OPLL [42] is the concept by which chip-scale and highly integrated OFSs were demonstrated. The optical frequency comb with spectral span ~ 3 nm was generated with a modest linewidth of 100 kHz external-

cavity laser and two cascaded modulators [46]. In addition, similar type of frequency synthesis was shown by offset-locking a widely tunable on-chip laser to mode-locked laser comb which also needs to be stabilized by second phase-locking to a narrow-linewidth reference laser [12, 80], introducing more complexity. All of these solutions are power hungry, difficult to integrate and complex unlike the work reported here.

In this chapter, we report on the experimental demonstration of two chip-scale optical frequency synthesizers where each of them use the OPLLs explained in the previous chapter. Second generation OFS consumes less power than the first one using the low power consumption OPLL, through a novel, compact and low-power PIC design. Both OFSs use same microresonator based optical comb source as frequency reference, which is designed and fabricated by OEWaves. Frequency synthesis is achieved by offset-locking an on-chip widely tunable laser to a magnesium fluoride (MgF_2) microresonator-based optical frequency comb. This comb has a 50-dB span of 25 nm (∼3 THz) around 1550 nm with a 25.7 GHz repetition rate. The physical package of the comb source, that includes the pump laser, the optical coupling element, the high-Q microresonator, and support electronics and thermal control has volume less than $0.2\,cm^3$ and total electrical power consumption of 400 mW. This study also reports the demonstration of tuning between comb lines with a tunable RF synthesizer for offset locking. Tuning resolution better than 100 Hz within ±5 Hz accuracy is also accomplished. As a further evaluation of the OFS, the frequency switching time with a wavelength separation $> 5\,nm$ by jumping over 28 comb lines is also experimentally measured. The total power consumption of the entire gen-1 OFS system is roughly 2 W (excluding EDFA), whereas the gen-2 OFS only consumes 1.7 W. To the best of our knowledge, the OFSs reported in this dissertation were the first demonstration of a chip-scale OFS with fastest switching time between the comb lines, highest tuning resolution and lowest power consumption at the time of their publication. This chapter begins with a discussion on the concept of the optical frequency

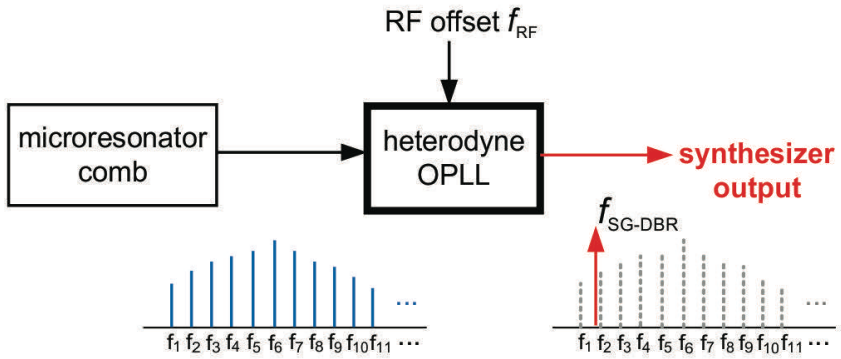

Figure 3.1: Optical frequency synthesizer system showing two main building blocks a comb source and a heterodyne OPLL. The optical spectra are also plotted at the output of each block.

synthesizer, followed by the operation of Kerr frequency comb generation. Then, the design and experimental results of the two generation of the optical synthesizers are provided.

3.2 Concept and Design of Frequency Synthesis

The basic idea of a compact and chip-scale OFS is illustrated in Fig. 3.1. A microresonator-based optical frequency comb is used as the ultra-stable and narrow linewidth source, serving as a master laser. The comb lines are then used as the reference for the heterodyne OPLL. A RF frequency f_{RF} from a tunable RF synthesizer is applied to feedback electronic circuits of the OPLL to introduce a frequency offset. By tuning the phase section current of the slave laser as well as f_{RF}, the slave laser is phase-locked to the comb lines. The two basic requirements to be met in order for an OFS to cover all the frequencies between comb lines are: (i) the heterodyne OPLL offset frequency range must be at least half of the comb's free-spectral-range (FSR), and (ii) the FSR of the comb must be less than the slave laser's mode-hop free tuning range. In such a way, continuous tuning is achieved.

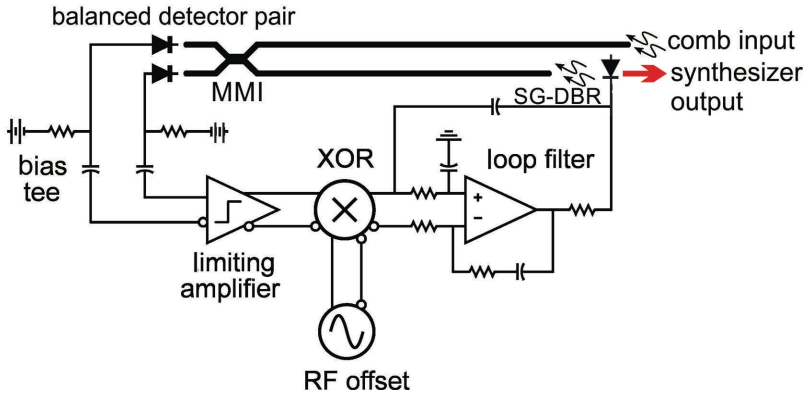

Figure 3.2: Circuit schematic of the heterodyne OPLL used in optical frequency synthesizer

From the two building blocks of the OFS shown in Fig. 3.1, a more detailed view of the thick-lined rectangle block, labelled as heterodyne OPLL, is displayed in Fig. 3.2. This block is already explained in the previous chapter. The heterodyne OPLL system consists of a photonic integrated circuit (PIC) and feedback electronic circuits. The latter is composed of electronic ICs (EICs) and a loop filter (LF). The master (injected single comb line in this case) and slave lasers in a PIC oscillate at different frequencies, producing a beat signal at this offset frequency on the balanced photodetector pair. The beat signal is then amplified by the limiting amplifier (LIA) to make the system insensitive to intensity fluctuation from the PIC. In other words, LIA limits the optical beatnote signal to logic values so that system is unresponsive to any changes in optical intensity. A phase detector (logic XOR gate in this case) compares the phase of the beat signal with a reference signal from a tunable RF synthesizer, thus generating the phase error signal. This is then fed back through the loop filter to control the slave laser phase and hence lock the phase of the slave laser to a single comb line at the given offset frequency.

Fig. 3.3 shows an optical microscope photo of the heterodyne OPLL system board where PIC, EIC and loop filter were assembled closely together by wirebonding. The inset shows the picture of the test bench. The PIC consists of a widely tunable sampled-

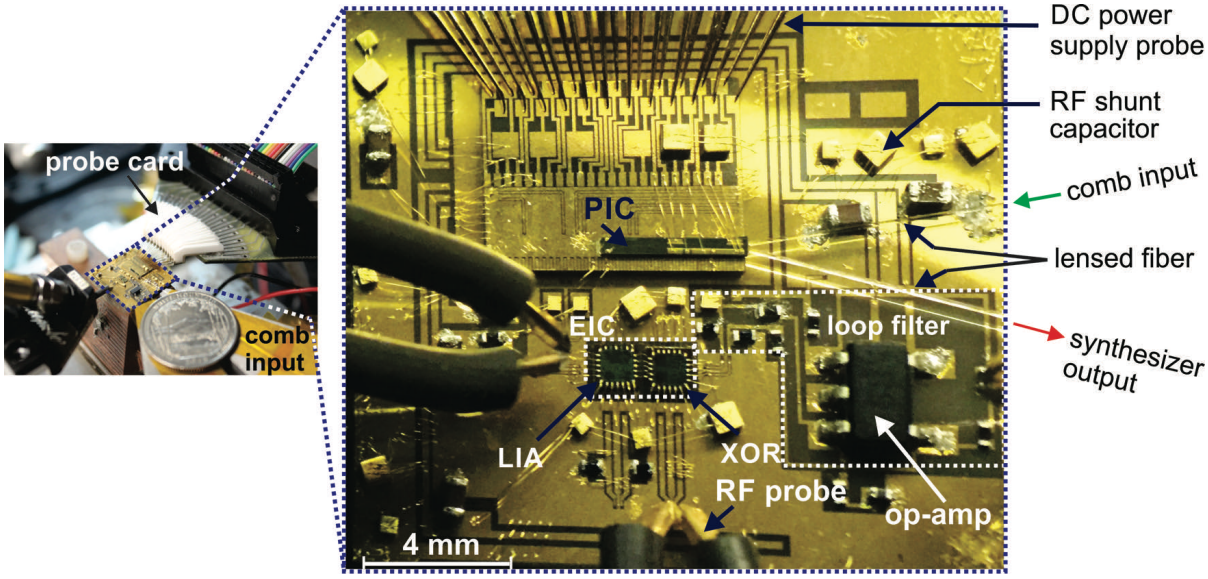

Figure 3.3: The heterodyne OPLL (used in gen-1 OFS) on the test bench where the US quarter shown as a scale and a close-up view of the heterodyne OPLL board.

grating distributed Bragg reflector (SG-DBR) laser, a 2×2 multi-mode interference (MMI) coupler, a couple of semiconductor optical amplifiers (SOAs) to pre-amplify the input comb lines, and two high-speed quantum well (QW)-based waveguide photodetectors (PDs). All are integrated on an InGaAsP/InP platform. The on-chip SG-DBR laser has a wavelength tuning range of 40 nm.

With a -3 V bias, the 3-dB RF bandwidth of the QW PDs can be as high as 14 GHz[48]. For the high-speed LIA and logic XOR gate, commercial-off-the-shelf (COTS) SiGe elements were employed for the electronics part, whereas discrete surface-mount device (SMD) components were used to build up the loop filter circuit whose loop bandwidth is designed to be ∼400-500 MHz. LIA has a differential gain about 30 dB with a 3-dB bandwidth of 17 GHz. XOR can work at least up to 13 GHz input clock frequencies. The details of these COTS ICs can be found in [49]. The OPLL system size is around $1.8 \times 1.6\,\mathrm{cm}^2$. A 24-pin DC probe card was used to power up the OPLL system, and two signal-line GSGSG RF probes were used to monitor the device performance and supply

the RF offset reference signal to the XOR. The maximum offset frequency our OPLL can lock the tunable laser to a reference laser at was verified to be as high as 15.6 GHz, allowing the OFS to be continuously tuned. Details of the OPLL and loop design are presented in the previous chapter.

3.3 Optical Frequency Comb Generation

To create the Kerr frequency comb generator, OEWaves fabricated a high-Q MgF_2 whispering gallery mode resonator (WGMR) out of a cylindrical crystalline preform using mechanical grinding and polishing. The resonator is approximately 2.7 mm in diameter and 0.1 mm in thickness (Fig. 3.4(b)). The intrinsic optical Q-factor of the resonator exceeds 5×10^9. The resonator has a FSR of 25.7 GHz. It shows anomalous group velocity dispersion resulting in 3 kHz difference between two adjacent FSRs.

The resonator was integrated with two coupling prisms and the loaded Q-factor was reduced to 5×10^8. The over coupling of the WGMR is useful for reduction of the thermal instabilities of the resonator occurring because of the light attenuation in the resonator host material.

Light emitted by a semiconductor distributed feedback (DFB) laser was collimated and sent to the resonator. When the light hit a WGM, the laser frequency was locked to the mode due to the optical feedback from the mode occurring because of resonant Rayleigh scattering. As the result of the locking the linewidth of the laser reduced to a sub-kHz level. As illustrated in Fig. 3.4(a), the light exiting the resonator through add and drop prism couplers was sent to a fast RF photodiode and an output optical coupler, respectively.

When the laser power exceeds a certain threshold (approximately 3 mW laser power corresponding to 1 mW in the mode) the unit produces a coherent frequency comb

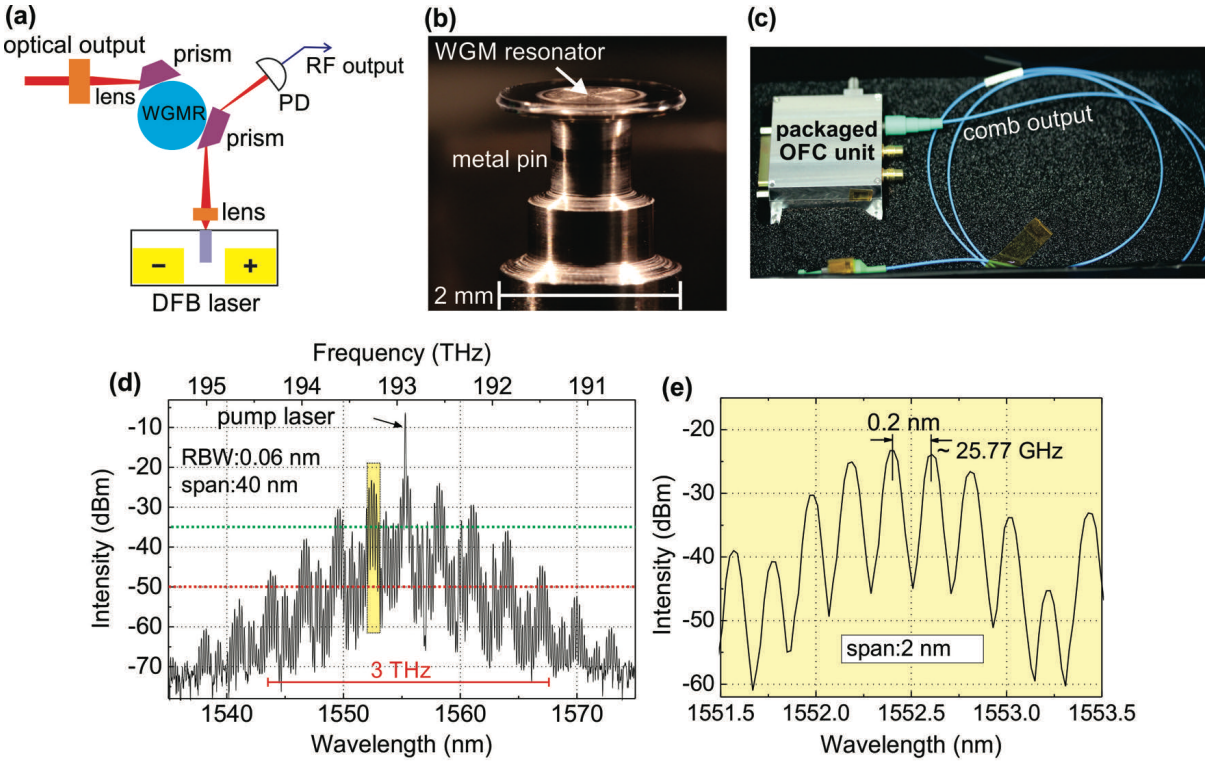

Figure 3.4: (a) The set-up of the optical frequency comb (OFC) in a MgF_2 crystalline whispering gallery mode (WGM) resonator, (b) optical microscope image of the MgF_2 crystal forming optical WGM resonators, (c) packaged OFC unit, (d) optical spectrum of a stabilized Kerr frequency comb generated in the unit, (e) Closer view of the lines of a multi-soliton Kerr frequency comb with a spacing of 0.2 nm.

operating in the self-injection locked regime. The demodulating the frequency combs on a fast photodiode results in spectrally pure RF signal. Fig. 3.4(d) shows the measured optical spectrum of the generated comb in the C-band under 20 mW laser power. The total power output from the fiber is $\sim$ 335 μW and the comb envelope is 15 dB lower than the carrier.

3.4 First Generation Optical Frequency Synthesizer

3.4.1 Experimental Setup

The comb output from the packaged and fiber-pigtailed optical frequency comb unit goes through an erbium-doped fiber amplifier (EDFA) and finally coupled into the OPLL PIC using lensed fiber. The power requirement per comb line for stable offset-locking is measured to be 20 μW (17 dBm) in the fiber near 1550 nm operating wavelength. Detailed sensitivity measurements of the OPLL can be found in Chapter-2. As the comb output is only 10 dBm in the fiber and divided over several comb lines, the EDFA is necessary to provide adequate power levels. The SG-DBR laser signal was coupled out from the back mirror and through a short semiconductor optical amplifier (SOA) using similar lensed fiber for monitoring purposes. To measure the OPLL tone, the output from the SGDBR was mixed with the comb in a 2×2 coupler, detected via an external high speed photodetector, and measured on an electrical signal analyzer (ESA), as shown in Fig. 3.5. The other output of this coupler is connected to the optical spectrum analyzer (OSA) to measure the optical spectra of SG-DBR laser and the comb output. Note that the linewidth of the unlocked SG-DBR is on the order of 10 MHz. A signal with a frequency equal to the beat-note frequency, f_{RF} as frequency offset is applied from the RF synthesizer to XOR within the EIC.

3.4.2 Experimental Results

The phase-locking of the SG-DBR laser to the comb lines is achieved. Fig. 3.6 shows the optical and electrical spectra when two lasers are phase-locked with an offset frequency of 11 GHz. The combined optical spectra of the SG-DBR and the comb lines are shown in Fig. 3.6(a) where both light source peaks around 1562 nm with a

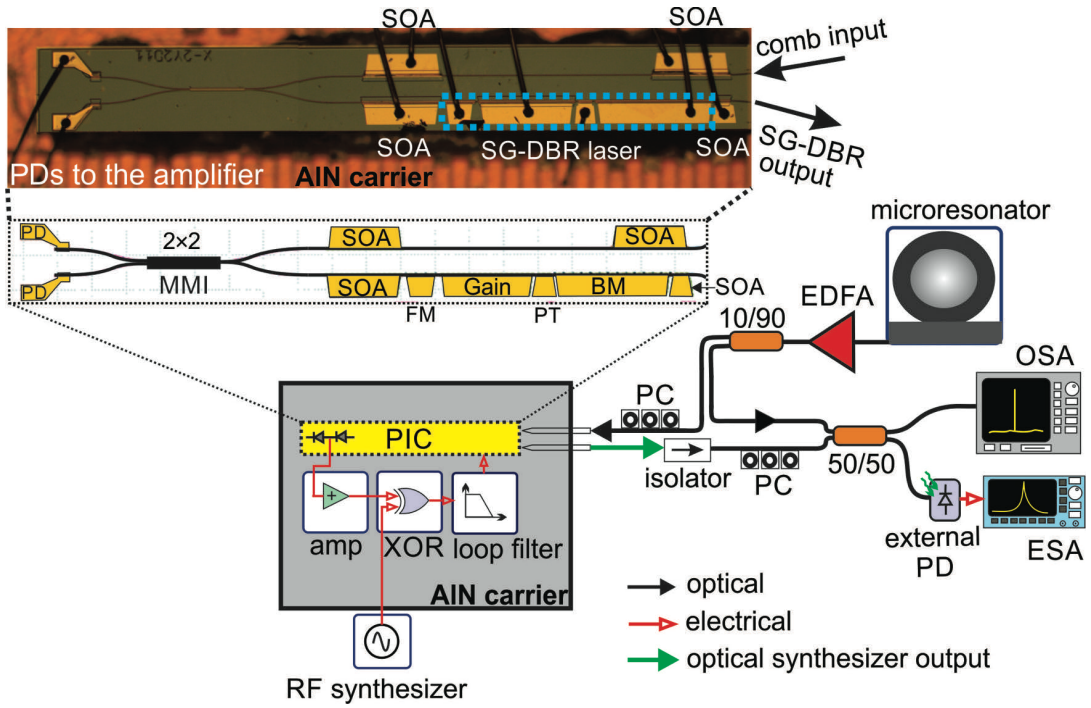

Figure 3.5: The test setup of the optical frequency synthesizer using heterodyne OPLL locking scheme. A microscope picture of the fully fabricated PIC mounted on AlN carrier with wirebonding shown at the top. (amp: amplifier, BM: back mirror, ESA: electrical spectrum analyzer, EDFA:erbium doped fiber amplifier, FM: front mirror, MMI: multi-mode interference, OSA:optical spectrum analyzer, PC: polarization controller, PT: phase tuner, PD:photodetector, PIC: photonic integrated circuit, SOA: semiconductor optical amplifier).

wavelength separation of 0.09 nm. Since the comb lines are uneven in amplitude, and they are roughly equally amplified by EDFA, some of the lines are buried by the amplified spontaneous emission (ASE) noise floor. The RF spectra of the beat-note at an offset frequency of 11 GHz, in cases of locked and free running are shown in Fig. 3.6(b). In the locked case, the RF linewidth is reduced significantly, indicating the coherence between the SG-DBR laser and comb. The beat-tone generated between the locked SG-DBR and the adjacent comb line is seen at 14.7 GHz (i.e. $25.7 - 11$ GHz). This is expected, since comb lines are stable in phase with respect to each other and the OPLL is phase-locked to the central comb line, consequently the adjacent comb line. Also, the RF beat-tone produced between comb lines is observed at 25.7 GHz (not shown).

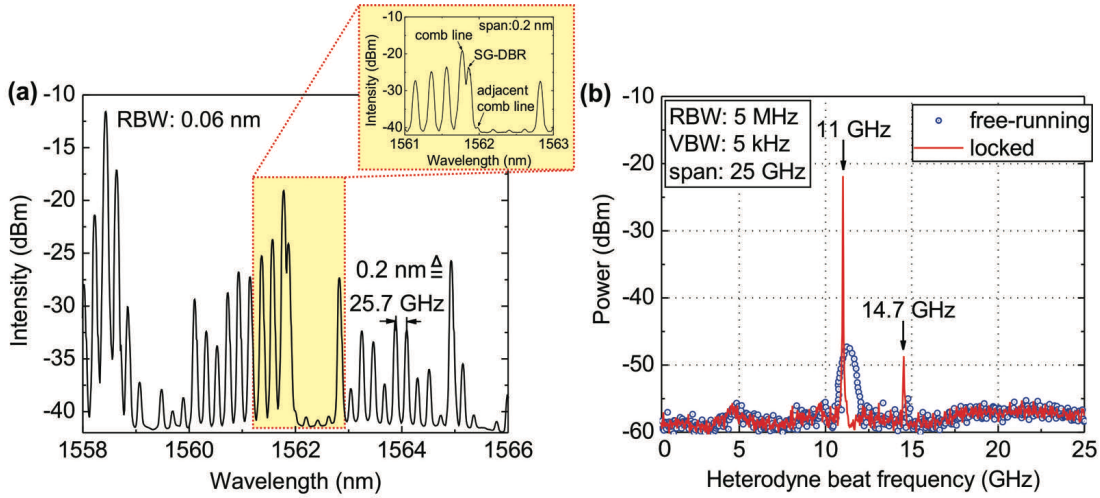

Figure 3.6: (a) Optical spectrum when SG-DBR laser and comb are phase-locked with a frequency difference of 11 GHz. The locking is to the comb line at 1561.77 nm. The zoom-in spectrum with a span of 2 nm is shown as inset, and (b) the RF spectrum shows the locked beat-note between SG-DBR and comb at 11 GHz. The beat-note generated between SG-DBR and adjacent comb line is also visible. Both the phase-locked and free-running cases are shown to illustrate the improved relative spectral coherence between the on-chip tunable laser and comb.

The RF signal generated by beating between comb lines on a fast photodiode was measured. An exceptionally high spectrally pure RF line is observed (Fig. 3.7(b)). The 3-dB beat width of the RF tone at 25.7 GHz is < 100 Hz, limited by the resolution bandwidth (RBW) of the ESA. This clearly suggests that this ultra-narrow linewidth and frequency stabilized optical comb source itself could be used as a reference light source for measuring the tuning resolution of our developed OFS. As a part of the experiment, the OFS output from our integrated OPLL system was mixed with the phase-coherent OFC output. As can be seen in Fig. 3.7(a), the mixed optical outputs are then beat down to a RF frequency by detecting that light on a high-speed external photodiode for precise measurement. The RF synthesizer connected to the XOR of our OPLL system was tuned in by a number of 100 Hz steps. The RF spectra were then recorded using ESA when the optical beat-note is offset-locked at 2.5 GHz, as displayed in Fig. 3.7(c). The output optical beatnote frequency shift $\triangle f_{optical}$ was then plotted as a function of

change in RF frequency $\triangle f_{RF}$ (Fig. 3.7(d)). Deviation from 100 Hz is observed to be on the order of ± 5 Hz. In such a way, our optical synthesizer achieves sub-100 Hz tuning resolution, which is the highest resolution so far reported for a chip-scale OFS. It should be noted that the optical beatnote, shown in Fig. 3.7(c), is formed by beating the locked laser to the reference laser, indicating relative linewidth between these two light sources.

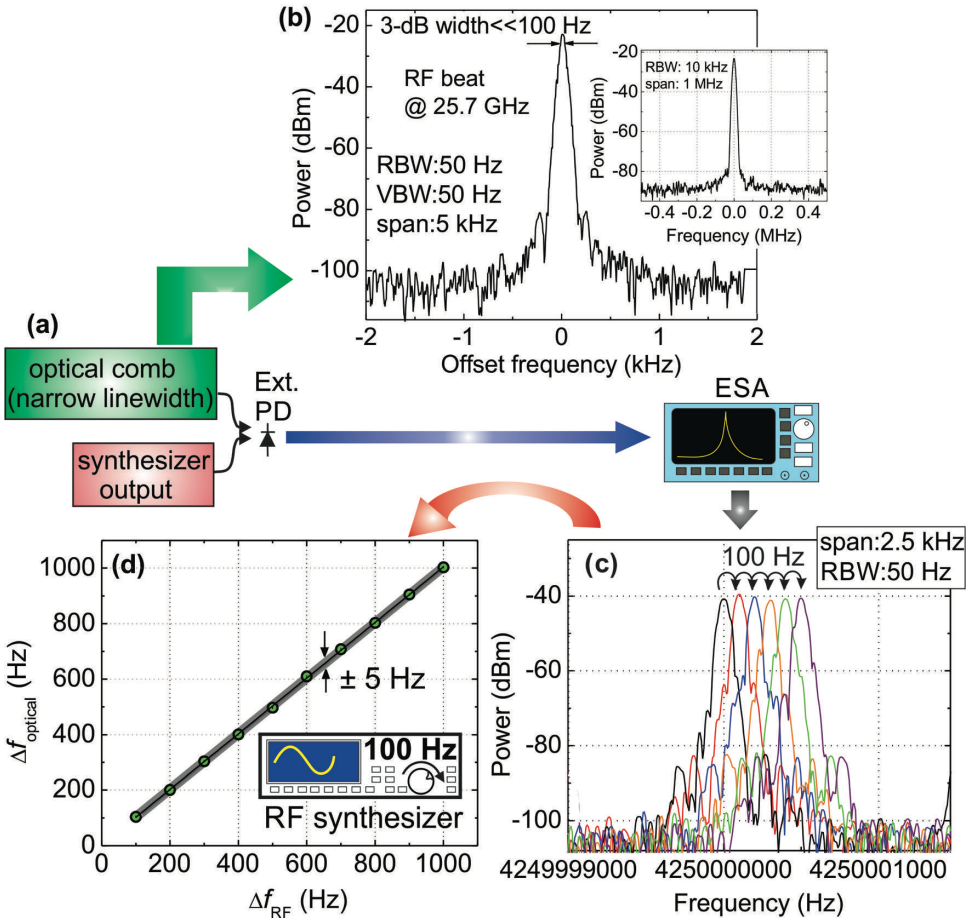

Figure 3.7: (a) The measurement setup for the tuning resolution of the OFS, (b) Power spectra of an RF frequency signal at 25.7 GHz generated by beating between comb lines on a high-speed photodiode with different resolution bandwidths. The smaller peaks are of 60 Hz and its harmonics, appearing from the power source, (c) locked beat signal between reference comb line and the SG-DBR laser and its movement by 100 Hz, and (d) plot of change in the optical beat-note with respect to change in the RF offset frequency.

Fig. 3.8(a) shows the measurement setup for the switching speed of the OFS. The front mirror section of the SG-DBR laser was modulated by square wave signal with a frequency of 800 kHz and 50% duty cycle from a function generator; whereas the back mirror remained open. A bias tee was used to add such a time-varying signal upon the DC bias. The square-wave signal into the front mirror modulates the lasing wavelength between two values with a separation of 5.6 nm. The peak-to-peak amplitude of modulation current applied into the front mirror was 1.6 mA, measured using current probe. Laser output was then passed onto manually tunable bandpass optical filter with a 3 dB bandwidth of 0.95 nm, which allows only one wavelength component to pass through. Optical signals were then detected by an external high-speed photodetector and the traces on the real-time oscilloscope were analyzed. When the modulation is on, the wavelength is switched between two values separated by 5.6 nm at 800 kHz speed, which is much faster than spectrum capturing rate the optical spectrum analyzer (OSA). Therefore, both wavelength values on the OSA are observed simultaneously, as shown in Fig. 3.8(b). The DC offset and amplitude of the square wave are carefully selected in a way so that two output wavelengths of SG-DBR lasers can beat against two comb lines with a reasonably good optical intensity and generate a RF beat-note with the same frequency. The superimposed optical spectra of comb output and laser at these two specific states are shown in Fig. 3.8(c). Note that the oscilloscope was triggered with the sync. output signal of the function generator. The wavelength separation between the two peaks of SG-DBR laser and comb output in two different spectral regions is 0.024 nm, corresponding to an offset frequency $\sim$ 2.5 GHz, when they beat with each other.

During the wavelength switching of SG-DBR laser, the electrical spectrum measured in ESA is shown in Fig. 3.9. The sharp single peak at an offset frequency of 2.5 GHz generated between SG-DBR and comb lines around 1550 nm and 1555 nm is the clear evidence for phase locking of on-chip noisy lasers to comb output. The beating tone

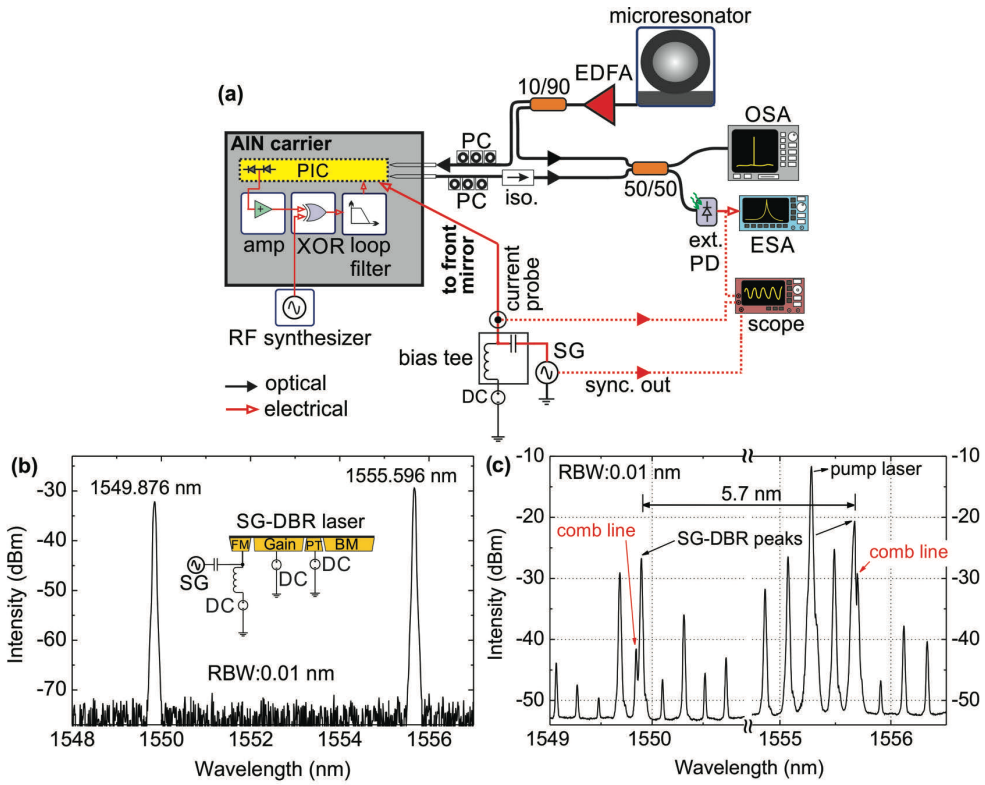

Figure 3.8: (a) The measurement setup for the switching speed, (b) the optical spectrum of SG-DBR laser when the front mirror is modulated by a 800 kHz square-wave from a signal generator with a constant gain current of 130 mA, resulting wavelength switching between $\lambda_{1,SG-DBR}$ = 1549.876 nm and $\lambda_{2,SG-DBR}$ = 1555.596 nm, and (c)superimposed optical spectra of comb output and SG-DBR laser, where both comb peaks separated by 0.024 nm from their corresponding SG-DBR laser peaks can be resolved. (BM= back mirror, DC= direct current, EDFA= erbium doped fiber amplifier, ext. PD = external photodetector, FM= front mirror, PIC= photonic integrated circuit, PC= polarization controller, PT= phase tuner, RBW = resolution bandwidth)

between the SG-DBR laser and the adjacent comb lines at 23.2 GHz as well as the tone at 25.7 GHz between comb lines are also seen here.

The OPLL will lock the on-chip SG-DBR laser to comb when the whole system including the right offset frequency from the RF synthesizer is on. This is clearly evidenced by Fig. 3.8(c) and 3.9 where one can see that two wavelengths of SG-DBR line up with two lines of the comb, generating single sharp RF beat-note at 2.5 GHz. This time the output of the external photodiode is monitored on a wide-bandwidth real-time oscillo-

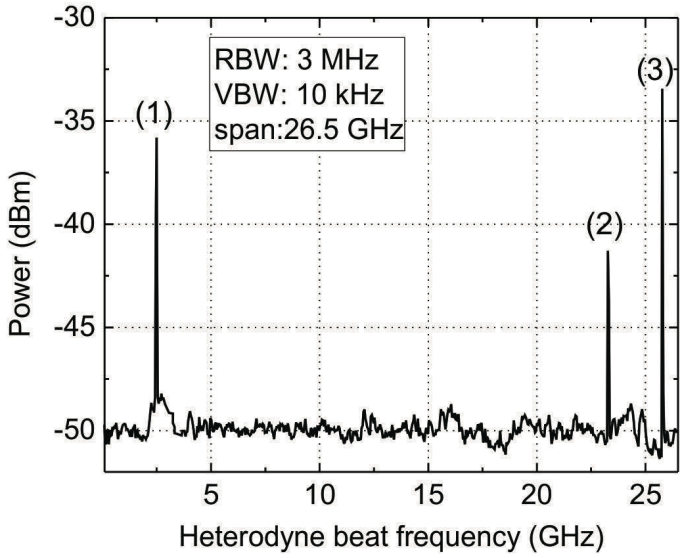

Figure 3.9: RF spectrum measured at the ESA of modulated SG-DBR laser beating with the comb output during dynamic wavelength switching of SG-DBR. Three peaks are seen, (1) the locked beatnote is at 2.5 GHz, produced by beating between both SGDBR peaks and the corresponding comb lines, (2) The beatnote generated between both SG-DBR peak and adjacent corresponding comb line is at 23.3 GHz, and (3) the beatnote produced between comb lines is at 25.7 GHz

scope instead of connecting with ESA, illustrated by the dotted electrical path shown in Fig. 3.8(a). The oscilloscope trace, displayed in Fig. 3.10, is showing that the SG-DBR laser is phase-locked most of the time except for a short period of OPLL transient time. Importantly, this is happening periodically at a modulation frequency 800 kHz. The time interval in between two high states of such a trace can be considered as wavelength switching of SG-DBR and OPLL locking time which is extracted as 200 ns. In the time interval of phase locking, a sinusoidal signal at 2.5 GHz, representing the locked beat-note, is observed, which is shown in Fig. 3.10(b). Hence, this synthesizer achieves sub $-\ \mu$s switching and locking time.

To evaluate further the performance of the OFS using the heterodyne OPLL, phase noise of the OPLL locked to the comb line was measured from 10 Hz to 1 GHz using the

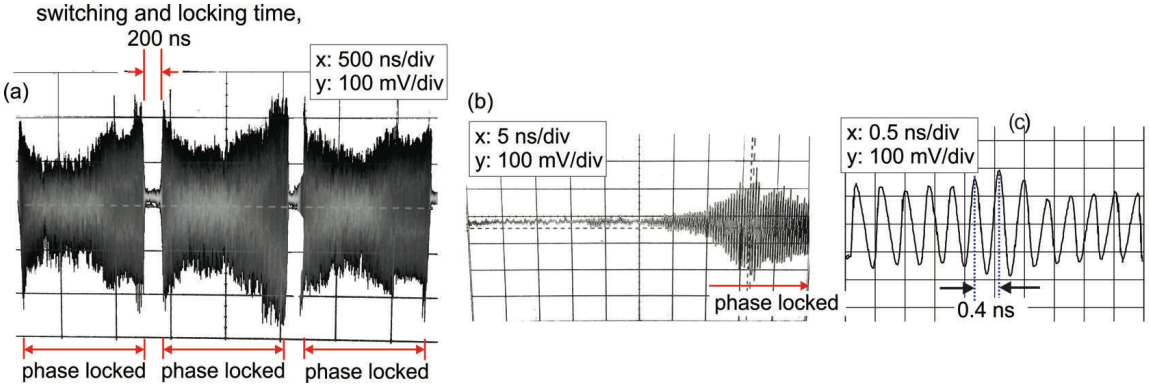

Figure 3.10: (a) A real-time oscilloscope trace of the external photodiode output of both wavelength component of SG-DBR laser during wavelength switching in order to measure the locking time of the OPLL system. Three periods are shown here which corresponds to the modulation frequency of front mirror, i.e. 800 kHz, (b) trace with a smaller span, showing the transition to phase-locking, and (c) trace with smallest span to show 2.5 GHz signal during phase-locking.

setup shown in Fig. 3.5. The locked beat-note at 2.9 GHz produced between SG-DBR and comb was connected to the ESA and the single-sideband (SSB) phase-noise spectral density (PNSD) was then measured. The signal power level of this measurement was 42 dBm. Fig. 3.11 shows the residual OPLL phase noise at offsets from 10 Hz to 1 GHz. For the comparison, PNSD of the background, RF synthesizer at 2.9 GHz, and comb source (through the RF beat-note generated between comb lines) are superimposed in Fig. 3.11. The output signal power levels were kept the same during the measurement in order to obtain consistency.

The phase noise variance from 1 kHz to 10 GHz is calculated to be 0.08 rad^2, corresponding to 14° standard deviation from the locking point. This result is better than the one reported in [80]. As can be seen in Fig. 3.11, low frequency noise with a value less than 80 dBc/Hz at an offset above 200 Hz for PNSD was achieved, whereas the same value at an offset above 10 kHz was achieved in [41, 80]. Lu et al. also reported better than 80 dBc/Hz at offsets above 5 kHz which is again worse than the performance reported here [53]. However, the phase variance of our results is comparable with [41, 80],

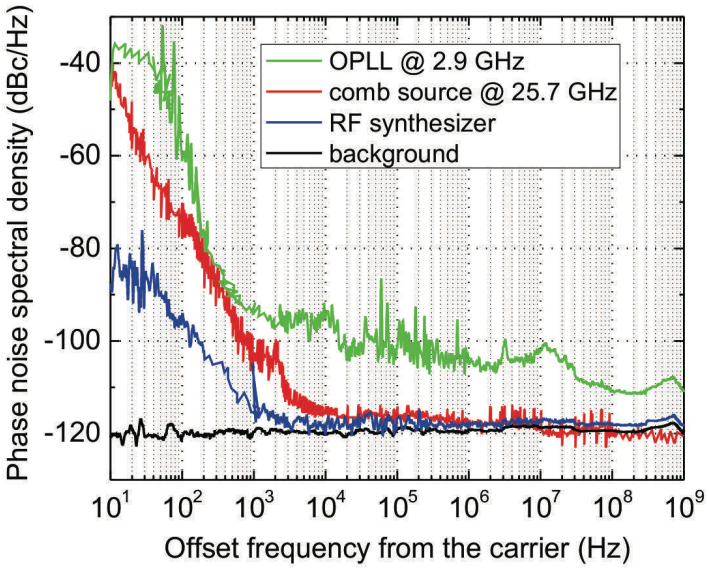

Figure 3.11: Single-sideband residual phase noise of the heterodyne OPLL when it is locked to a comb line with 2.9 GHz offset. Phase noise results of the RF signal at 25.7 GHz generated between comb lines, RF synthesizer, and background is also shown here for comparison.

which could be attributed to the pedestal after 1 kHz which can potentially be caused by a fiber path length mismatch between the comb and OPLL laser paths (see Fig. 3.5). Thus, after 1 kHz some additional noise from the slave laser is observed and contributes to the overall phase variance. Matched path length needs to be used in the future work.

3.5 Second Generation Optical Frequency Synthesizer

3.5.1 Compact and Low-Power Receiver Design

A widely-tunable compact Y-branch laser, a 2×2 multi-mode interference (MMI) coupler, a balanced photodetector pair and input waveguide are monolithically integrated

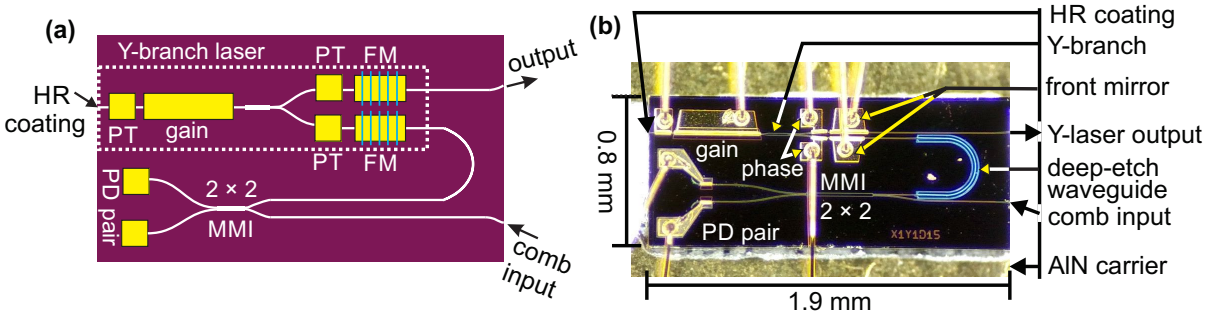

Figure 3.12: (a) Functional schematic of the photonic integrated receiver circuit composed of a Y-branch laser, two MMI couplers, and a balanced photodetector pair, and (b) microscope image of the PIC mounted on a separate aluminum-nitride (AlN) carrier and wire-bonded. (FM: front mirror, HR: high reflection, MMI: multi-mode interference, PD: photodetector, and PT: phase tuner.)

on an InGaAsP/InP material platform. A schematic of the coherent receiver PIC is shown in Fig. 3.12(a). The device size is 1.9 mm × 0.8 mm. For the integration, the offset quantum well (OQW) platform is employed, where the active-region quantum-wells are first grown on top of a common waveguide, and then removed in the regions that are to become passive prior to the regrowth of the top cladding and contact layers. Details of the processing steps for the well-established OQW-based material structure can be found elsewhere [81]. This PIC is designed and fabricated by Freedom Photonics LLC. Microscope image of the processed chip is shown in Fig. 3.12(b), where two output ports after a 2×2 MMI coupler can be seen. For the Y-branch laser design, front grating mirrors on both ports are incorporated. One port is coupled to the integrated coherent receiver, while the second port provides the output signal.

One of the key components in this integrated chip is the Y-branch laser which consumes most of the power. Similar to the sampled-grating distributed Bragg reflector (SG-DBR) laser, the Y-branch laser uses Vernier tuning to reach a wide tuning range. This design is optimized with a shorter cavity and a highly-reflecting back cleaved, high-reflectivity-coated mirror for low-power consumption. The high-reflection (HR) coating with a reflectivity of $> 95\%$ at back facet enables a short gain section further shortening

the overall length. The front sampled-grating mirrors select wavelength through Vernier tuning, but have lower reflection for better efficiency and higher output power. Phase sections are included for continuous tuning. No long absorber section or integrated booster preamplifier was included in this design so that the power consumption and chip-size could be reduced further. The output and input waveguide cleaved facets were coated with anti-reflection (AR) coating to suppress parasitic reflections.

Fig. 3.13(a) shows the superimposed measured lasing spectra from 1502 nm to 1562 nm. Electrical current in both front mirrors is adjusted to obtain such wide tuning. As can be seen, the tuning range of such a laser is about 60 nm, covering the entire C-band. Any wavelengths can be obtained in this range by setting a combination of these mirror currents to set the approximate wavelength window, and then fine tuning of the cavity mode with the phase section, which is controlled by the OPLL in the phase-locked source. Tuning to a particular wavelength is, thus, not done by continuously tuning across the spectrum, but by digitally tuning to the desired wavelength in these two steps. Spurious outputs could be avoided by blanking the output during this process. The peak gain wavelength of the device being tested is blue-shifted. This induces the tuning range of the laser to be shifted towards the shorter wavelength.

Fig. 3.13(b) shows a typical single-mode lasing spectrum of the Y-branch laser at the emission wavelength of 1543 nm. The laser shows good single-mode working performance with a side-mode suppression ratio (SMSR) of 53 dB. SMSRs above 45 dB across the whole tuning range with typical values greater than 48 dB are observed. The linewidths of the Y-branch lasers were also measured, using a heterodyne technique. First, we beat this laser with a narrow linewidth external-cavity laser (ECL) and the beat-note is detected to an external fast photodetector (PD) which converts it into an electrical tone. The RF signal was then measured with an electrical spectrum analyzer (ESA). Thus, before phase-locking, the 3-dB linewidth is measured to be 12 MHz, as shown in

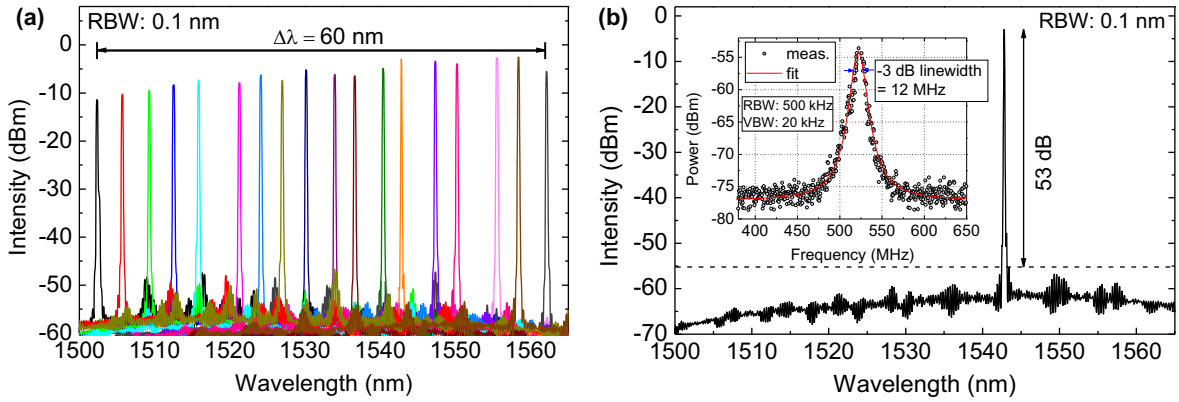

Figure 3.13: (a) Superimposed measured lasing spectra of the Y-branch laser with an emission wavelength, ranging from 1502 to 1562 nm, and (b) typical single-mode lasing spectrum at a wavelength of 1543 nm with a side-mode suppression ratio of 53 dB. Beat spectrum of the laser is shown in the inset.

the inset of Fig. 3.13(b).

High bandwidth, low dark current, and high saturation power are the desired characteristics of on-chip photodiodes (PDs). The coherent receiver PIC was characterized by measuring the dark current and bandwidth of the balanced PD pair. The current-voltage ($I-V$) characteristics at room-temperature are shown in Fig. 3.14(a) for both PDs. For the quantum-well (QW) PD with the size $3.3 \times 50\,\mu m^2$, the dark current is $-10\,\mu A$ at $-3\,V$. The bandwidth of these PDs was measured using a lightwave network analyzer. By sweeping the modulation frequency from the network analyzer, the relative RF response of the photodetectors (PDs) biased at a $-3\,V$ was measured. The response, as shown in Fig. 3.14(b), is normalized at 1 GHz due to the low-frequency noise from the measurement system. In addition to the noise, gain ripples with ± 3 dB were observed at frequencies below 1 GHz, possibly due to the impedance mismatch between devices under study and the system. The modulation characteristics of these PDs were measured with the device wirebonded. By direct probing on chip, a better performance is expected. Importantly, the bandwidth of the PDs is large enough that our OPLL system with the sensitive feedback electronic circuits can exhibit the offset locking range as high as 18

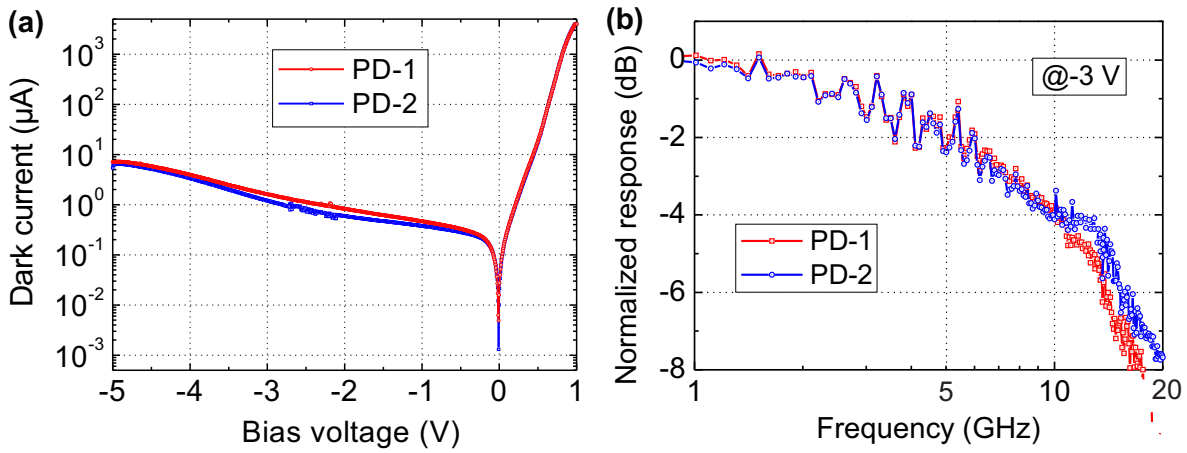

Figure 3.14: (a) Dark currents, and (b) modulation characteristics of the two on-chip photodiodes in InP monolithic coherent receiver PIC shown in Fig. 3.12.

GHz [13, 14].

Table 3.1 presents the total maximum power consumption of the second generation optical frequency synthesizer during the full operation. Total power consumption of the optical frequency synthesizer is about 1.7 W including the optical frequency comb generator (excluding EDFA). It is 0.3-0.4 W better than the previous generation due to the novel PIC used (detailed power consumption tables of OPLLs in Table 2.1 and 2.2) There are three phase tuning sections integrated in the receiver circuit. The ones, located after the Y-branch and next to the front mirror, are responsible for super-mode jumping. In other words, those two phase sections allow us to tune the reflection envelope unlike the one which is located at the far left in Fig. 3.12. The phase section at the left side of the gain section is responsible for fine emission wavelength tuning, i.e., cavity mode tuning, which was connected to the feedback electronic circuits. It should be noted that it is possible to achieve full wavelength coverage using only two phase sections of the Y-branch laser. One of the phase sections next to the front mirrors can be considered as a redundant.

PIC	**Section**	**Current (mA)**	**Voltage (V)**	**Power (mW)**
	Gain (1)	73	1.5	109.5
	FM (2)	20	1.3	52
	PT (2)	7	1.3	18.2
	PD (2)	1	2	4
PIC-1 TOTAL				**184**
Electronic ICs	**LIA**	180	3.3	594
	XOR	130	3.3	429
	Op-amp	16	6	96
Electronic ICs TOTAL				**1119**
OFC	**Pump Laser (1)**	165	2.4	**396**
Total Power Consumption Gen-2 OFS				**1.7 (W)**

Table 3.1: Power budget for the second generation OFS

3.5.2 Electronic-Photonic Integration

Fig. 3.15 shows an image of the heterodyne OPLL system board on the test stage, where PIC, EIC and loop filter (LF) were assembled closely together by wirebonding. This assembly was done by mounting all these three parts on a patterned ceramic super-carrier in close proximity to minimize loop delay. An AC-coupled system was prepared by forming an on-chip bias tee in order to continuously remove DC offsets from the balanced-PD signals. The balanced-PDs reduce the influence of relative intensity noise (RIN) from the LO laser, since this noise is common to both detectors. The procedure is similar to the first generation OFS, and explained in detail in the previous chapter for the OPLL designs as well.

As a part of the feedback electronics, similar to the previous generation, SiGe-based limiting amplifier (LIA) and logic XOR gate, both manufactured by ADSANTEC [49], are employed. A high-speed emitter coupled logic differential amplifier with a 30 dB differential gain is used as a LIA. It is connected to the balanced PD pair in order to limit and square-up the input PD signals. This helps to make the OPLL system insensitive to PD power fluctuations. This LIA is followed by a high-speed digital XOR gate to obtain

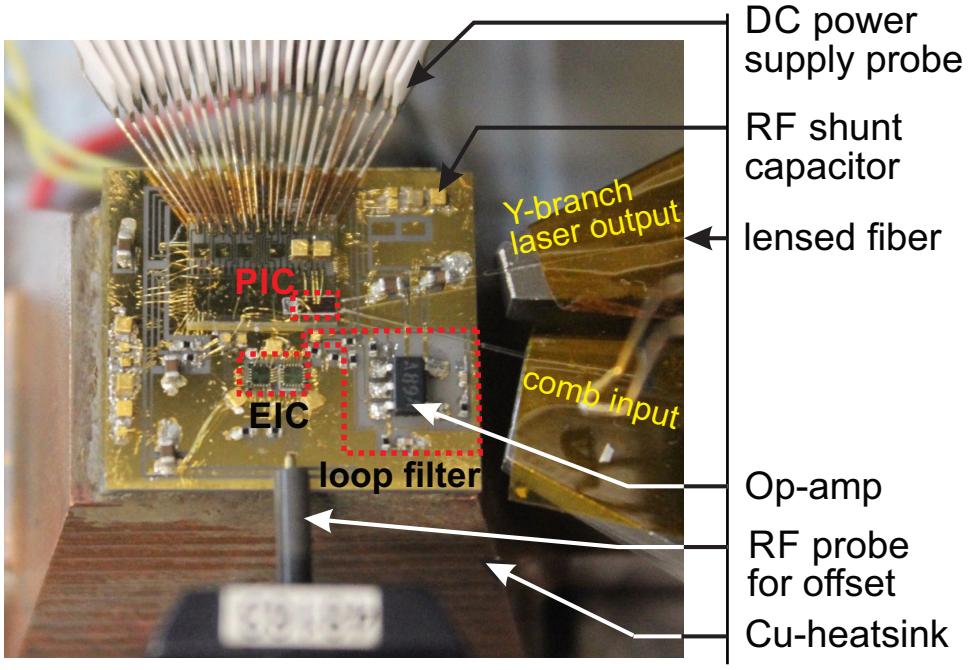

Figure 3.15: Microscope image of the entire heterodyne OPLL system (used in gen-2 OFS) where PIC, COTS ICs and loop filter are highly integrated on a separate AlN super-carrier. Finally, it rests on a copper heat-sink for the measurement. Two lensed fibers at the right are butt-coupled to the waveguide end-face of the photonic chip.

the phase difference between the RF beat-note resulting from the beating of the two lasers and a reference signal from a tunable RF synthesizer. Both are commercial-off-the-shelf (COTS) SiGe elements whose details can be found in [49]. A commercial LMH6609 op-amp and discrete surface-mount device (SMD) components are used to build up the LF circuit and its design details are listed in [14, 48]. An additional fast feed-forward path is also included in the loop filter to increase the loop bandwidth. The output from the XOR gate is filtered out by the loop filter to control the LO laser phase and hence lock the phase of the LO to a single comb line. The OPLL system size is approximately $1.8 \times 1.6\,\mathrm{cm}^2$. The system could be made as compact as $1\,\mathrm{cm}^2$ easily by optimizing the carrier design. Further details are also provided in the previous chapter.

3.5.3 Experimental Results

An optical comb source generated using a semiconductor laser pumping a crystalline MgF_2 resonator with a mode spacing of 25.7 GHz was used in this study similar to the first generation OFS explained in this chapter. The unit was packaged in 1 inch cubed form factor and its fiber-coupled output was sent to an OSA. The measured optical spectrum with a 50-dB span of 23 nm is shown in Fig. 3.16(a). The strongest central line at 1555.27 nm originates from residual light of the pump laser. The RF signal generated by beating between comb lines on a fast PD integrated in the packaged unit was measured to distinguish between chaotic and coherent regimes of the frequency comb. An exceptionally high spectrally pure RF line with the coherent comb is observed. The 3-dB beat width of the RF tone at 25.7 GHz is <100 Hz, limited by the resolution bandwidth (RBW) of the ESA [20]. The phase noise of this RF tone is shown in Fig. 3.16(b). The noise was measured using OEwaves' phase noise test system.

Depending on the initial conditions, the OFC unit produces frequency combs with envelopes varying in shape. The variations can be linked to the generation of a different number of optical pulses within the WGMR. While all the realized coherent states are intrinsically stable and suitable for LO stabilization, the state corresponding to the single pulse localized in the resonator is advantageous as it does not have any envelope structure. Changing of the power of the comb lines makes the offset locking to some of the modes of the OFC a hard task. We tried to utilize the frequency combs with the smoothest envelope.

Fig. 3.16(b) shows the measured single sideband (SSB) phase noise of the beat of two self-injection locked pump lasers. One of the pump lasers is integrated in our packaged OFC unit. The optical phase noise corresponds to less than 100 Hz instantaneous linewidth of the pump laser is shown in the inset. To determine an effective linewidth,

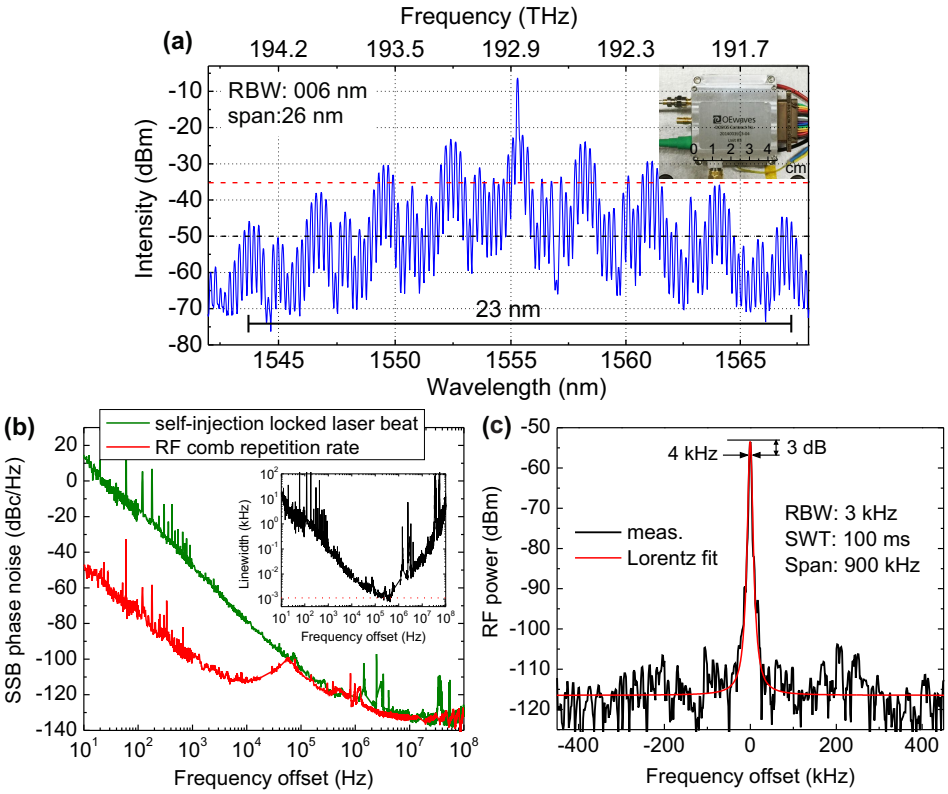

Figure 3.16: (a) Optical spectrum of a stabilized Kerr frequency combs generated in the unit, shown in inset. (b) single sideband (SSB) phase noise of the injection-locked DFB laser, used as a pump laser, integrated in the packaged OFC unit and the RF signal generated by the Kerr comb repetition rate. The instantaneous linewidth of the pump laser is extracted from its phase noise, as shown in the inset. (c) RF beatnote, resulting from beating one of the comb lines with ultra-narrow linewidth lasers [1]

the frequency noise spectrum is derived from the phase noise spectrum by the following relation [82]:

$$S_\nu(f) = 2f^2\mathcal{L}(f) \tag{3.1}$$

where, $\mathcal{L}(f)$ [Hz^{-1}] is the SSB power density of the phase noise, and $S_\nu(f)$ [$\mathrm{Hz}^2/\mathrm{Hz}$] the corresponding frequency power noise. The effective instantaneous linewidth $\Delta\nu_{\mathrm{instant}}$ is then given by the minimum of frequency noise multiplied by π [82]

$$\Delta\nu_{\mathrm{instant}} = \pi * \min^{\mathrm{m}}[S_\nu(f)] \tag{3.2}$$

To measure the phase noise, two packaged OFC units were used. We tuned them in a way that the combs were produced, then changed the frequencies of the lasers (by changing the frequencies of the resonators) so that the beat note of the lasers did not exceed a few GHz, and measured separately the phase noise of the RF signals produced by the units (by the combs) as well as RF signal produced by the two lasers emitted by the units. Assuming that the lasers are nearly identical, the laser beat phase noise should be reduced by 3 dB with respect to the shown noise to reflect the noise of the single laser. We also studied the spectral purity of the optical comb lines using the heterodyne-technique. The 3 dB linewidth of the RF beatnote created on a fast photodiode by beating a comb frequency harmonic, centered at 1553 nm, and a low noise local oscillator does not exceed 4 kHz, as shown in Fig. 3.16(c). Measurement with smaller RBW was hindered because of the jitter of the beat note frequency. This clearly suggests that comb lines can be considered as an ultra-narrow linewidth light source.

The comb output from the packaged and fiber-pigtailed OFC unit is optically amplified by an erbium-doped fiber amplifier (EDFA) and finally coupled into the photonic coherent receiver PIC using a tapered lensed fiber. The Y-branch laser output through front mirror was coupled out from the front side of the PIC using a similar lensed fiber for monitoring purposes. An optical isolator was used at the laser output to reduce back reflections. To measure the OPLL tone, the output from the laser was mixed with the comb in an off-chip 2×2 coupler, detected via an external high speed photodetector, and measured on the ESA, as shown in Fig. 3.17. The other output of this coupler was connected to the optical spectrum analyzer (OSA) to measure the optical spectra of Y-branch laser and the comb output. A signal with a frequency equal to the beat-note frequency as a frequency offset was applied from the RF synthesizer to the XOR gate within the EIC.

In order to achieve heterodyne-locking of tunable LO to the comb, the LO wavelength

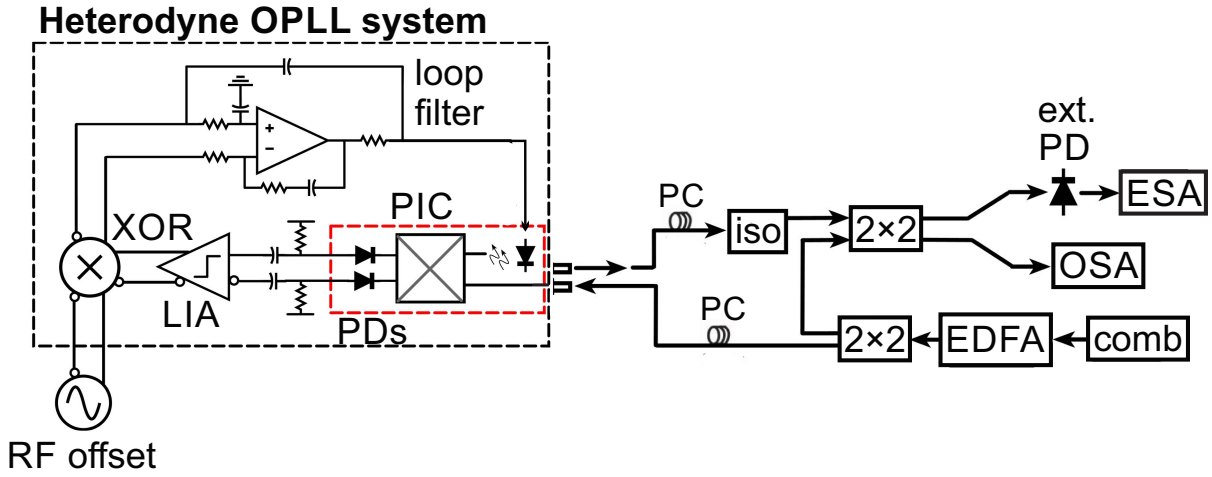

Figure 3.17: The test setup for the Gen-2 OFS system including the heterodyne OPLL, Y- branch laser and comb input. (ECL: external cavity laser, EDFA: erbium-doped fiber amplifier, ESA: electrical spectrum analyzer, ext. PD: external photodiode, iso: isolator, LIA: limiting amplifier, OSA: optical spectrum analyzer, PC: polarization controller, and PIC: photonic integrated circuit).

is tuned with respect to a comb line to get any random beat-note frequencies, i.e. $\leq$ half of the comb FSR as explained in the gen-1 OFS experiments. After differential PD signals are amplified by the LIA, the RF synthesizer then applies a signal close to the beat-note frequency to the XOR gate. With all feedback electronics is turned on, the XOR gate outputs a signal that becomes zero when the beat-note and RF signal have the same frequency and phase. In other words, the loop filter keeps tuning the LO's phase so that the beat-note signal with a constant offset frequency and phase matches the RF offset. This means that the LO and comb are at a constant phase and frequency offset, i.e. they are phase-locked to each other.

In the gen-2 OFS, heterodyne OPLL successfully phase locks the Y-branch laser to a comb line up to an offset frequency of 18 GHz with an RF synthesizer. Such maximum offset locking frequency is mainly limited by the operational frequency range of the XOR [49] and on-chip balanced PDs. Since the Y-laser has a tuning range of 60 nm, the whole frequency spectrum within the comb span with a FSR of 25.7 GHz can be utilized

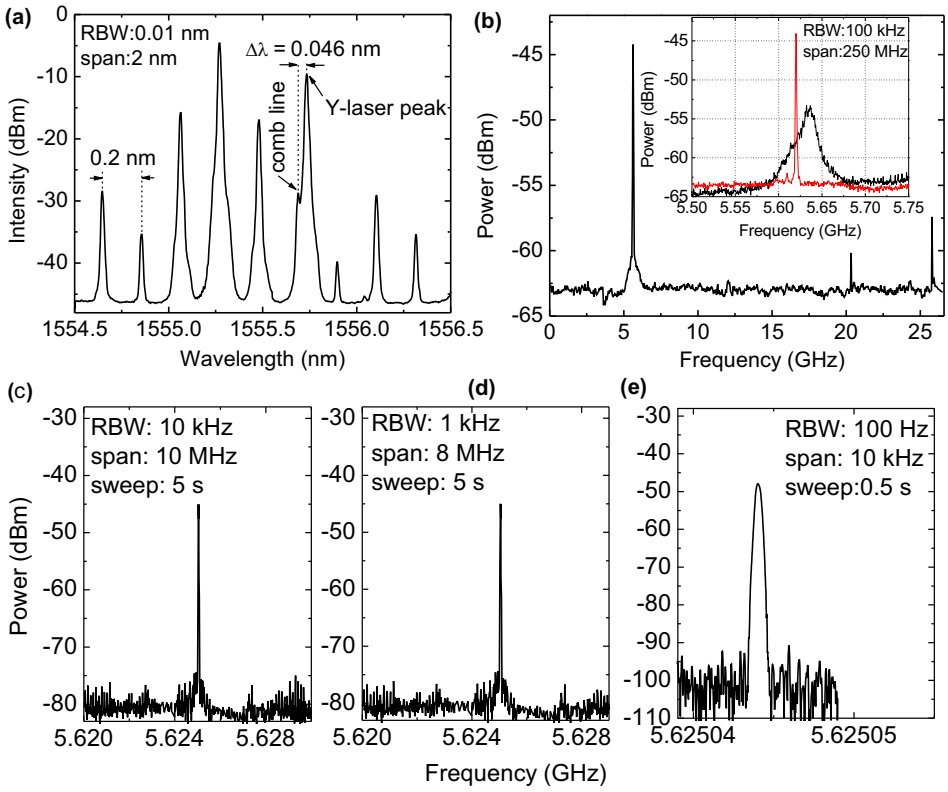

Figure 3.18: (a) Optical spectrum when Y-branch laser is offset-locked to the comb at 1555.69 nm with a wavelength difference of 0.046 nm, (b) RF spectrum of the locked beatnote between Y-branch laser and comb at 5.6 GHz is recorded. The beatnote generated between on-chip laser and adjacent comb line at 20.1 GHz and the beatnote produced between comb lines at 25.7 GHz are also visible. The resolution bandwidth is 3 MHz. The zoom-in spectra with a span of 250 MHz is shown as inset where the phase-locked (red) and free-running (black) cases can be seen, and (c)-(e) measured RF beatnotes at various RBWs.

for such offset locking. Fig. 3.18(a) shows the optical spectrum of the Y-branch laser with its emission wavelength 0.046 nm offset from the nearest comb line while the phase locking to this comb line is achieved. This is evidenced by the RF spectrum measured by the ESA at the resolution bandwidth (RBW) of 3 MHz, as shown in Fig. 3.18(b).

The RF beating tones show that the offset frequency is at 5.6 GHz, corresponding to the 0.046 nm. The beat tone generated between the locked Y-laser and the adjacent comb line is also seen at 20.1 GHz. This is expected, since comb lines are stable in phase with

respect to each other and the OPLL is phase-locked to one comb line, hence the OPLL is phase-locked to the adjacent comb line as well. Also, the RF beat tone produced between comb lines is observed at 25.7 GHz, as indicated in Fig. 3.18(b). Thus, the 23 nm wavelength span of optical comb source can be covered by tuning the wavelength of the tunable LO laser in the receiver. The free running laser has 12 MHz instantaneous linewidth, whereas the relative linewidth of the locked beat-note is less than 100 Hz, revealing excellent relative spectral coherence between the on-chip LO laser and comb. This narrowing of the heterodyne linewidth occurs when the LO laser is phase-locked to the reference comb line. Fig. 3.18(c)-(e) show the clear coherent peaks of the locked beat note at various RBWs. Sweeping time of each measurement is also shown.

To evaluate the performance of the OFS system, residual SSB phase noise of the OPLL locked to the comb source was measured from 10 Hz to 10 GHz using the setup shown in Fig. 3.17. The measurement was performed by directly connecting the locked beat-note to a Rohde & Schwarz FSU spectrum analyzer system and using its application firmware (R&S FS-K4). The locked beat-note at 3.1 GHz produced between the locked LO laser and the comb was used in this case. The measurement result is shown in Fig. 3.19. The phase noise variance from 10 Hz to 10 GHz is calculated to be 0.04 rad^2 corresponding to 11.4° standard deviation from the locking point.

In order to measure the linewidth of the locked on-chip laser, an out-of-loop measurement was performed by beating the locked LO with another ultra-narrow linewidth reference laser [2]. Fig. 3.20 shows the corresponding optical out-of-loop beat-note, showing the linewidth of the laser is approximately the same as the linewidth of the comb harmonic and is < 5 kHz. Measurement with smaller RBW was hindered because of the jitter of the beat note frequency, as observed earlier. In-loop measurement by mixing the LO laser back with the comb to which we are referencing cannot be used in this regard since a bound phase error which translates in zero frequency error between LO laser and

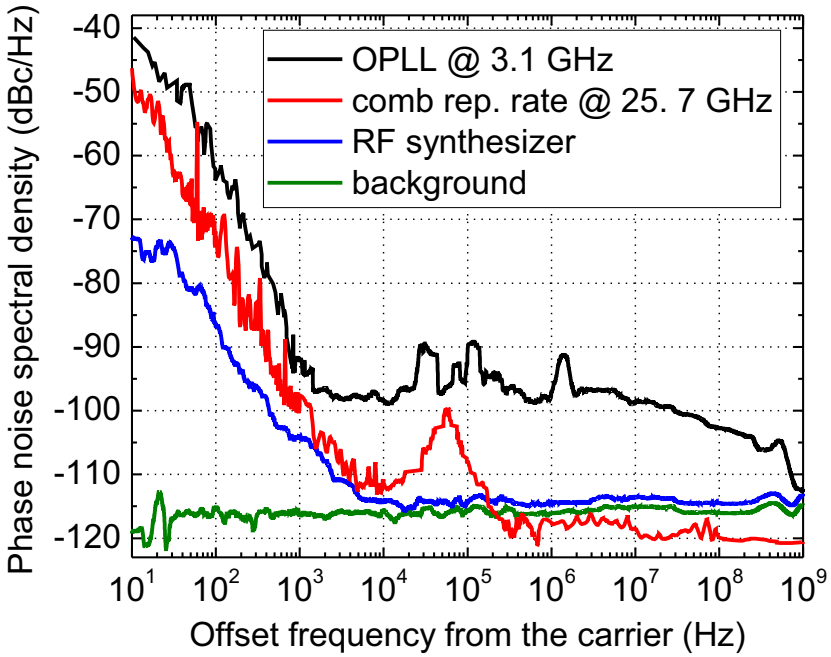

Figure 3.19: Single-sideband residual phase noise of the heterodyne OPLL locked to comb line at 3.1 GHz. Phase noise of the RF signal at 25.7 GHz generated by the comb repetition rate, RF synthesizer, and background is also shown here for comparison

the comb is obtained, once they are phase-locked. In other words, near zero linewidth can then be obtained in the RF spectrum analyzer with the LO offset phase-locked to the comb. Since the LO laser is being forced to instantaneously track the comb line (plus the RF offset) in order to be truly phase locked, common mode noise will not show up in the in-loop beat measurement.

As a result, on-chip tunable lasers are phase-locked to self-referenced and stable optical frequency comb lines using a highly integrated, low-power gen-2 heterodyne OPLL. However, further stabilization of comb sources is important for a range of scientific and technological applications, including frequency metrology at high precision, and high-purity optical as well as terahertz frequency synthesis. This stabilization is expected to be a key prerequisite for broadband and low-noise micro-comb generation for metrology applications, as well as for integrated micro and nanophotonic devices.

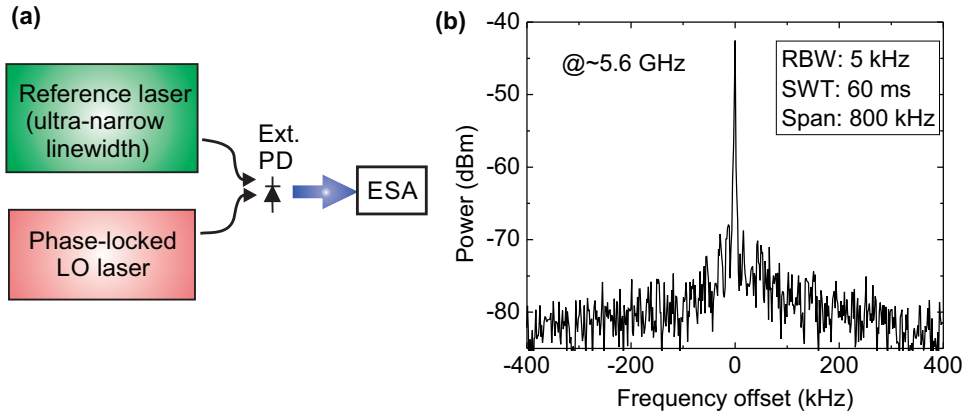

Figure 3.20: (a) Out-of-loop measurement setup, and (b) optical beat-note resulting from beating the phase-locked LO with another reference ultra-narrow linewidth lasers [2]

3.6 Conclusion and Future Work

In this chapter, we demonstrated two optical frequency synthesizers using the two OPLLs reported in the previous chapter. The second generation OPLL, therefore the OFS uses a compact, low-power consumption receiver PIC (designed and fabricated by the Freedom Photonics LLC). Therefore, the second generation OFS consumes record low power of only 1.7 W. The first generation OFS demonstrates sub-100 Hz tuning resolution with ± 5 Hz accuracy. Switching time between comb lines separated more than 25 nm was measured as less than 200 ns for the Gen-1 OFS. Both OFS can lock to the microresonator based, ultra-stable optical comb source designed and fabricated by OEWaves. Spacing of the comb lines is 25.7 GHz, which is less than the twice of the locking ranges of the heterodyne OPLLs. Therefore, continuous tuning between comb lines is possible.

Future work includes designing application-specific ICs, consuming only a few hundreds of mW of power for the heterodyne OPLLs. This will enable an OPLL with less than half a watt of power consumption. In addition, frequency locking can be introduced through the feedback electronics using Costas loop. This will allow system to know the

sign of the offset frequency, and further improve the lock-in range. Moreover, further stabilization of the optical comb generator with broader frequency coverage can be pursued. Lastly, the heterodyne OPLL and comb source can be integrated heterogeneously in a small carrier to further reduce the size, power consumption and thermal problems.

With all these improvements an octave spanning optical frequency synthesizer with a total volume of less than 1 cm^3 and a total power consumption of less than 1 W can be possible. Such a development is attractive for optical communication, sensing and imaging. All these developments will make the optical frequency synthesizers more practical to be used in optical communications in order to create broadband communications.

Part II

mm-Wave Transceiver Design for Broadband Wireless Communications

Chapter 4

Broadband Transceiver Design at D-Band using 22 nm CMOS FDSOI

4.1 Background and Motivation

High data rate wireless links are necessary due to the rapid increase in data demand. There is a large available spectrum at mm-Wave and sub-terahertz frequency bands, which can be utilized to provide broadband wireless communications. Low-cost CMOS technologies have experienced limitation in terms of their maximum frequency of operation for a long time. It was not possible to build low-cost mm-Wave transceivers at mm-Wave and sub-mm-Waves 10-20 years ago. Only high-cost, III-V based transceivers working above 100 GHz were reported during that time. Their applications are limited mostly to the defense industry, where cost is not a limiting factor [83, 84, 85]. During the last two decades, CMOS technologies have been developed tremendously. State of the art CMOS technologies now have power gain (f_{max}) and current gain (f_t) cut-off frequencies in 200-250 GHz range, referenced to the top metal layer [86]. Therefore, it is now possible to develop mm-Wave, sub-mm-Wave circuits, and transceivers using CMOS

at low-cost and high yield [27, 37, 87, 88, 89, 90].

D-Band is particularly attractive since there is a low atmospheric attenuation around the 120-140 GHz region, and there is still large available spectrum to be utilized. Moreover, the wavelength is small enough so that form factor is small, and massive number of antennas and ICs can be placed even in a small volume. This can allow us to build highly directive phased arrays with thousands of elements. These phased arrays can support single or multi-beam wireless communications with high data rate. Several designs [37, 91] were reported at this frequency band, but this work will provide a broadband mm-Wave front end designs that can support higher data rates.

This chapter starts with the transistor characterization for mm-Wave circuit design, which is the most critical part of mm-Wave IC design. Then D-Band amplifier, and multiplier designs will be explained in detail with the simulation results (due to export control issues, overall chip doesn't have the test structures to measure individual circuit blocks). Mixer design details and the simulation results are provided briefly, since they are designed by another lab member Ali Farid. Then, a broadband single channel transmitter and receiver at D-band is presented. A broadband amplifier is designed using cross coupled pair with capacitive neutralization, and the inter-stage matching is based on staggered tuning to enable a broadband design at the intended frequency band. A wideband pseudo-differential transimpedance amplifier (TIA) is used as a baseband amplifier in the receiver chain; with a 3-dB bandwidth of 20 GHz. Full receiver and transmitter channel characterization including the conversion gain, 3-dB bandwidth, 1-dB compression point and transmitter saturated output power is presented.

4.2 Technology and Transistor Characterization

We used 22 nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technology from Global Foundries in this work. Advertised (f_{max}) and (f_t) are 290/375 GHz respectively [92]. The process offers lower supply voltage, hence the possibility for lower power consumption of the circuit blocks. It provides mm-Wave supported metal stacks in order to design higher-Q, lower loss inductors, transmission lines and transformers. Back gate biasing capability provides additional freedom to optimize the performance and the power consumption. Low off-capacitance thanks to the fully depleted SOI provides high performance switches. Overall, with the high (f_{max}) and (f_t), and mm-Wave supported metal stacks this process provides a really good RF/mmWave performance. At the same time, low supply voltage and back gate biasing allows to design low power digital circuits. Therefore, it is overall a really good technology to provide system solutions, where RF/mmWave front ends needs to be integrated with baseband digital processors.

mm-Wave design always start with the transistor characterization and the layout effects on the main RF parameters including the f_{max}, f_t, maximum available gain (G_{max}) and minimum noise figure (NF_{min}). f_{max} and f_t are strong functions of the layout of a transistor, since they depend on the capacitor between gate and drain (C_{gd}), gate and source (C_{gs}), and gate access resistance (R_{gate}) (Eq. 4.1 and 4.2).

$$f_\tau \cong \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \tag{4.1}$$

$$f_{max} = \frac{f_\tau}{2\times\sqrt{(R_i+R_s+R_g)G_{ds}+2\pi f_\tau R_g C_{gd}}} \tag{4.2}$$

Given these, although, f_{max} and f_t are reported above 300 GHz, in reality once transistor is connected to the upper wiring stack through vias and metals, the reported

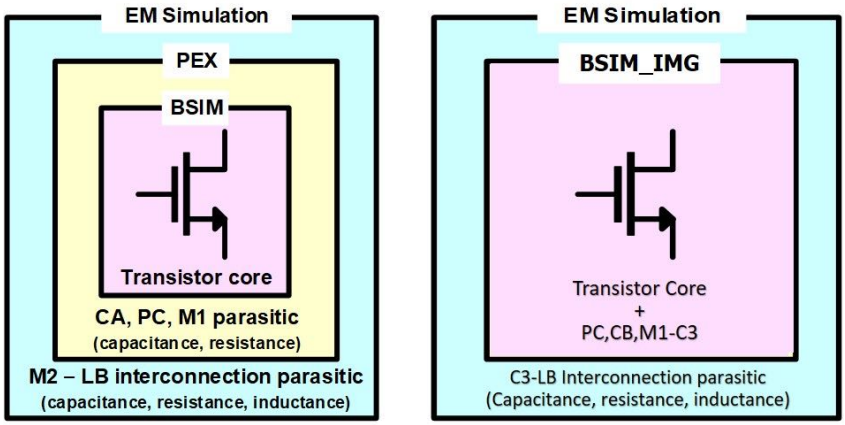

Figure 4.1: Two different transistor modeling strategy

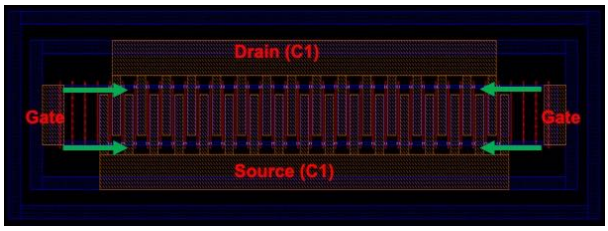

Figure 4.2: Transistor layout for $32 \times 0.5\,\mu\text{m} = 16\,\mu\text{m}$ device with 2xCpp gate to drain pitch up to 5^{th} metal layer

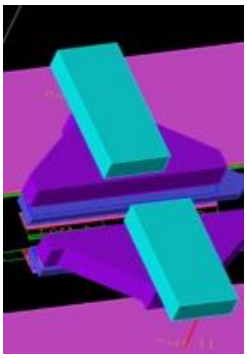

Figure 4.3: Transistor layout up to top metal layer in electromagnetic simulation environment

numbers for f_{max} and f_t drop significantly. Coupling capacitances between the metals running on gate, drain and source as well as the resistance of the connections through vias on gate and source degrade the f_{max} and f_t.

Therefore, modeling of the transistor starts with the foundry given model (up to Metal-1). Then parasitic extraction is done up to Metal-2 or Metal-3 layers. Lastly full electromagnetic simulation is run from Metal-2 or Metal-3 till the top most metal layer. In this work, since Global Foundries provided mm-Wave model up to intermediate metal layer (Metal-5), mm-Wave model is used. Full electromagnetic simulation is performed from this layer to the top most metal layer (Fig. 4.1).

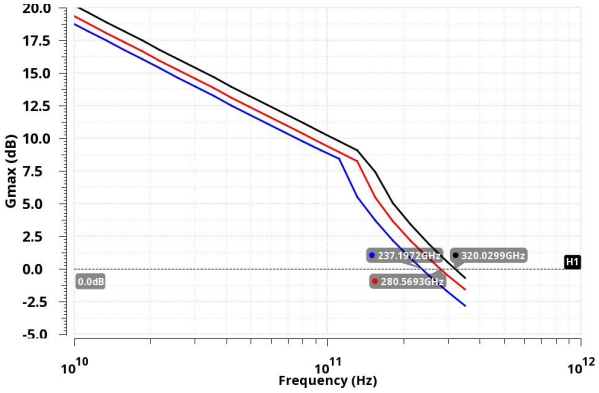

Figure 4.4: f_{max} referenced to the lowest metal layer, fourth metal layer and top metal layer with respect to frequency

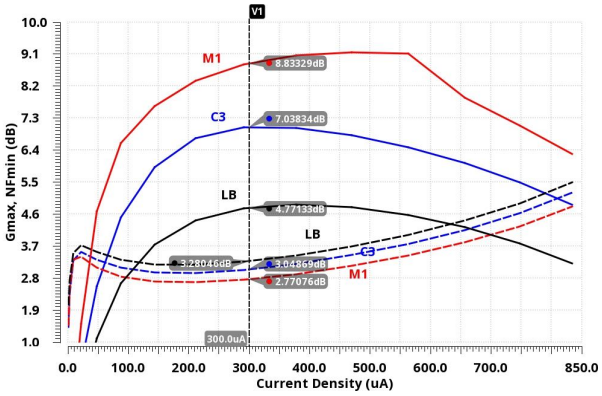

Figure 4.5: G_{max}, and NF_{min} at 140 GHz with respect to current density in μA/μm

Transistor layout in Fig. 4.2 is used and the connections to top most metal layers are designed from that middle layer. As can be seen in Fig. 4.2, gate connection is from double side to decrease the gate resistance. Double the gate pitch is used to satisfy the electro-migration rules later in the amplifier and multipliers. From this point everything is modeled with Keysight Momentum 2.5D electromagnetic simulation tool. The performance of the transistor model up to lowest metal layer, middle metal layer and the top most metal layer are compared and the degradation of the f_{max} is presented in Fig. 4.4. f_{max} is about 320 GHz when referenced to the lowest metal layer, and it drops to 280 GHz, and 237 GHz for the layouts shown in Fig. 4.2 and 4.3 respectively.

Another critical comparison is in terms of the maximum available gain (G_{max}), and the minimum noise figure (NF_{min}) of the device with respect to different wiring plane references, and the current densities. Fig. 4.5 shows the G_{max} and NF_{min} for three different cases with respect to the current densities at 140 GHz. 0.3-0.35 mA/μm provides the best G_{max} and 0.2-0.25 mA/μm provides the best NF_{min} performances. G_{max} at 140 GHz is 8.8 dB referenced to the lowest metal layer, whereas it is 4.8 dB referenced to the top metal layer. Similarly, NF_{min} increases from 2.7 dB to 3.3 dB.

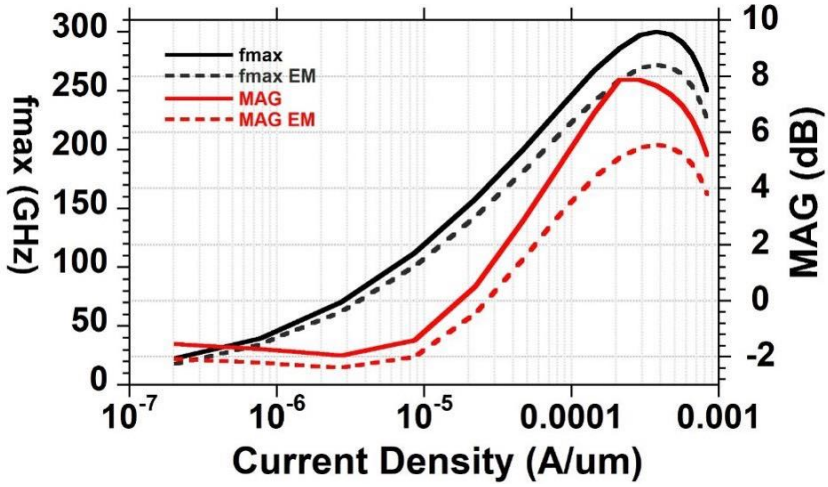

Figure 4.6: f_{max} and MAG with respect to current density in $A/\mu m$ using unileteral power gain definition

f_{max} comparison here utilized the maximum available gain curve from Cadence, but in reality it is not exactly correct. To do better job, also the actual formula for unilateral gain in Eq. 4.3 is used to find the f_{max}. Fig. 4.6 shows the f_{max} and MAG vs. current density by using this formula. This formula shows f_{max} is roughly 255 GHz referenced to the top metal layer, with roughly 5.5 dB gain at 135 GHz.

$$U = \frac{1}{4} \times \frac{|Y_{21} - Y_{12}|^2}{Re(Y_{11})Re(Y_{22}) - Re(Y_{12})Re(Y_{21})} \tag{4.3}$$

As can be seen in these simulation results and the arguments, transistor layout design is the critical part of a mm-Wave circuit design. Therefore, one needs to spend enough time to optimize the layout in order to minimize the parasitics. In other words, gate to drain, and gate to source capacitances, gate access resistance and source resistance needs to be minimized to minimize the performance degradation in the transistor performance due to the wiring stack.

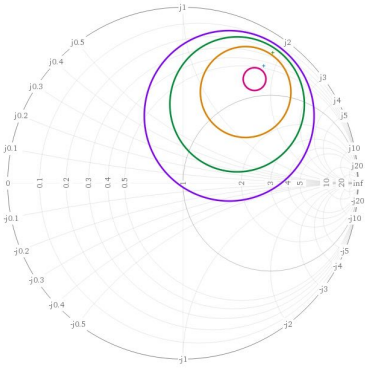

Figure 4.7: Noise circles for the LNA differential core

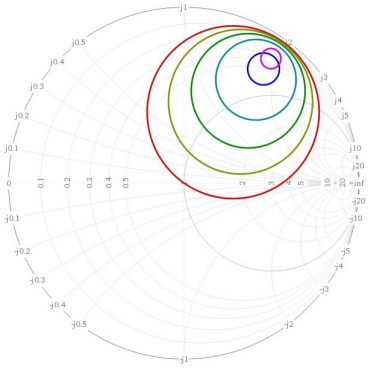

Figure 4.8: Available gain circles for the LNA differential core

4.3 Building Circuit Blocks for Transceiver

4.3.1 Amplifier Design at D-Band

After careful transistor characterization, a transistor footprint for $32 \times 500\,\text{nm}$ finger width device is designed (Fig. 4.3). This core is repeatedly used throughout the designs in this chapter, especially in amplifier and multiplier designs. However, this core has only 4.8 dB G_{max} at 140 GHz. With the significant losses of the passives at D-Band, to use this cell as a single common source amplifier stage we need to have a large number of stages to get enough gain. Then, the noise figure will be really high, because the noise contribution from the input matching and the first stage cannot be suppressed by the subsequent stages. Hence, we designed a differential core with C_{gd} neutralization using this core. Neutralization helps to increase the maximum available gain and improve the isolation between input and output. However, the maximum available gain and stability with respect to neutralization capacitor value should be evaluated carefully in order not to cause any instability for the amplifier. Fig. 4.9 demonstrates the MAG and K-factor vs. the frequency. When the k-factor is 1 or larger, C_{gd} needs to be less than 6.8 fF. Since the loss of the passives are high and can play a role as stabilization, we picked 7.5-8

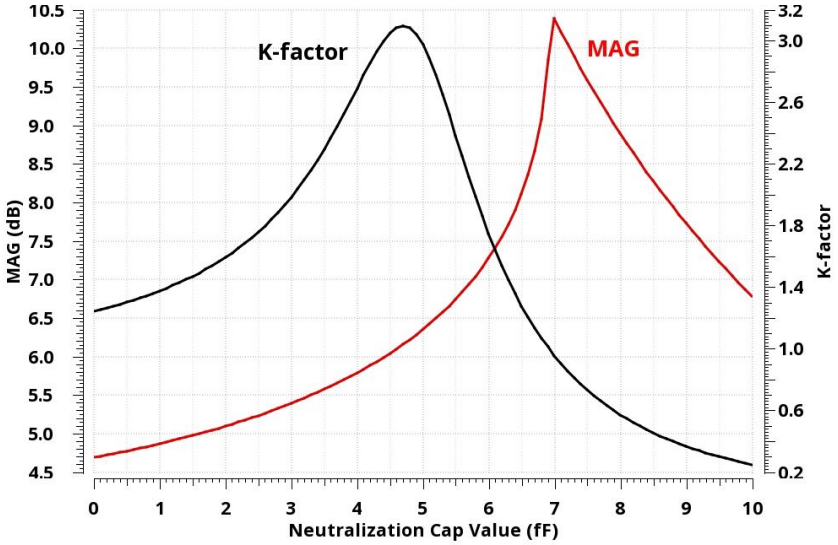

Figure 4.9: Maximum available gain (MAG) and k-factor with respect to neutralization cap value

fF as the neutralization cap for the amplifier design. At this neutralization value G_{max} is roughly equal to 10 dB.

Finally, a 4-stage fully differential common source amplifier (Fig. 4.10) is designed using a cross coupled pair with capacitive neutralization to boost the maximum available gain. The neutralization uses alternate polarity metal-oxide-metal (APMOM) capacitor. A center tapped transformer converts the single-ended input to a differential signal. Transformer center-taps provide DC voltages. For broad bandwidth, tuning of the inter-stage matching networks is staggered in frequency. The transformers use the top aluminum layer and the ultra-thick metal layer below the aluminum layer; they are simulated using Keysight Momentum. Available gain and noise circles of the differential core can be seen in Fig. 4.7 and 4.8. The device size of 16 μm is particularly chosen to have the circles close to 50 Ω impedance circle in the Smith Chart, so that simultaneous gain and noise matching can be done easily. This amplifier is designed to be used as a low noise amplifier (LNA) in the receiver chain and as a power amplifier (PA) in the transmitter chain. Therefore, the first stage device sizing was optimized for minimum

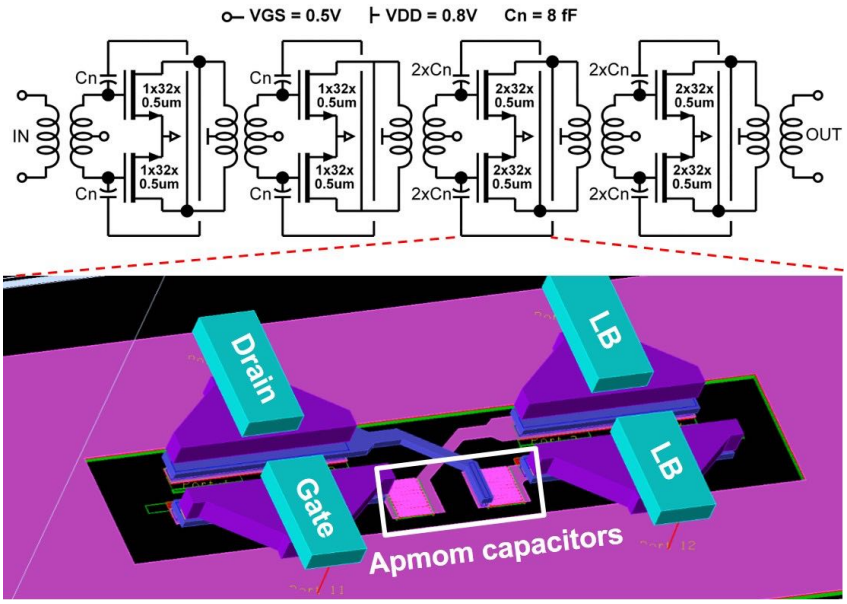

Figure 4.10: Schematic of the 4-stage amplifier and the layout view of the differential core with C_{gd} neutralization

noise figure and easy gain-noise matching. However, the last two stages device sizing is doubled to increase the saturated output power. This LNA/PA draws 55 mA from a 0.8 V supply, with a simulated gain of 16-dB and 40 GHz 3-dB bandwidth (Fig. 4.11). The simulated noise figure (NF) is 8.5 dB. Saturated output power is 4.5 dBm, while the 1-dB compression power is 1.8 dBm (Fig. 4.12).

4.3.2 Frequency Multiplier Design and D-Band Local Oscillator Generation

Both transmitter and receiver uses a 9:1 frequency multiplier to generate a 135 GHz LO signal from an external reference at 15 GHz. Multiplier design consists of an inverter-based single ended to differential (STD) converter, followed by two cascaded 3:1 frequency multipliers (Fig. 4.13). A fully differential structure reduces even harmonic generation and supply coupling. The x3 frequency multipliers use cross coupled pairs with capacitive

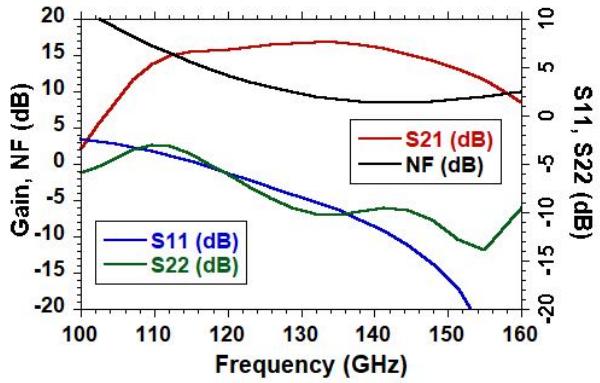

Figure 4.11: S-parameters of the amplifier

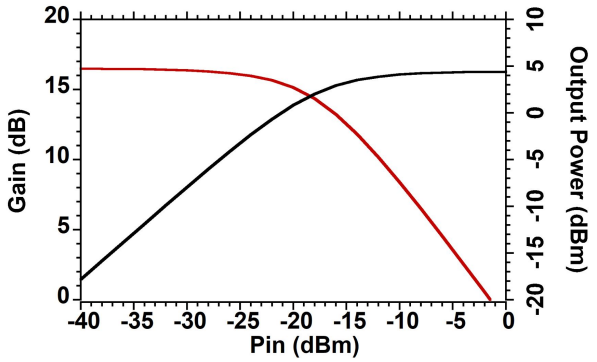

Figure 4.12: Output power and gain of the amplifier with respect to input power

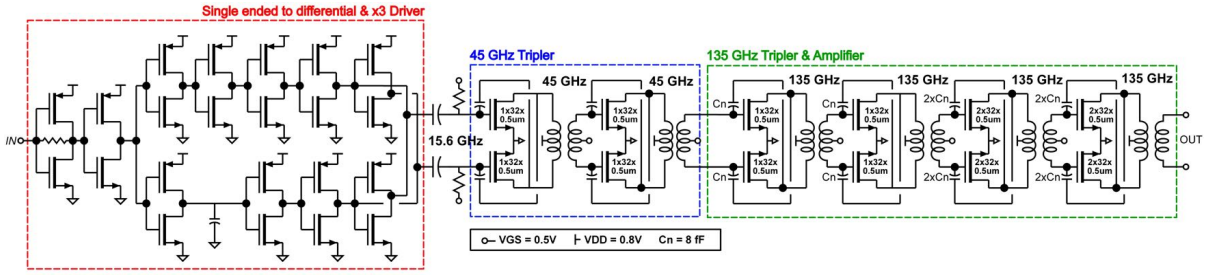

Figure 4.13: Schematic diagram of the multiplier including the single-ended to differential driver, x3 multiplier at 45 GHz, and x3 multiplier at 135 GHz

neutralization (same core used in amplifier). These are driven into saturation to generate the third harmonic. The output of the first x3 multiplier is tuned at 45 GHz (3rd harmonic of the input signal at 15 GHz), while the second x3 multiplier is tuned at 135 GHz. The topology and element values within the second 3:1 frequency multiplier are similar to those of the LNA/PA stages. The supply voltage of the entire chain is 0.8 V. The simulated output power is 3.5 dBm and the simulated 3-dB bandwidth is 25 GHz (Fig. 4.14). Fig. 4.15 shows that the simulated harmonic rejection is better than 25 dBc. The strongest harmonic power is generated through 7th harmonic.

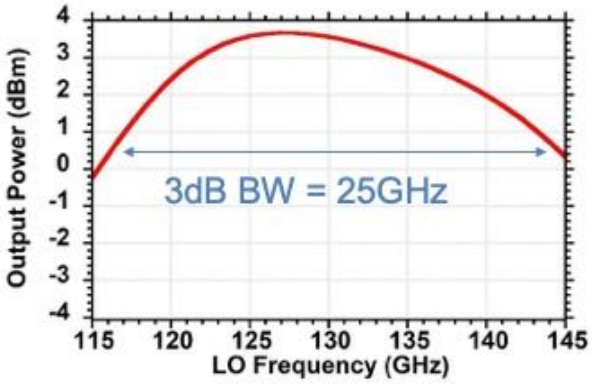

Figure 4.14: Simulated output power of the x9 multiplier with respect to LO input frequency

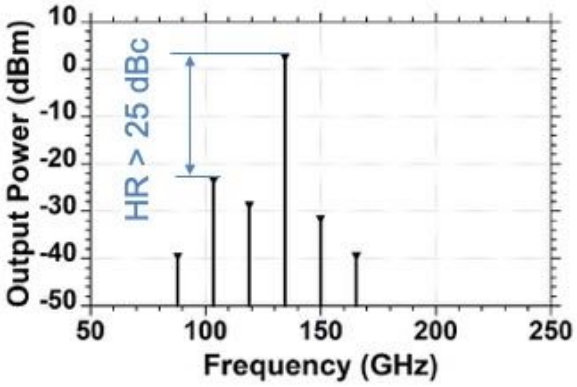

Figure 4.15: Simulated harmonic powers of the multiplier

4.3.3 Down-conversion Mixer and Transimpedance Amplifier

A pair of double balanced passive mixers (Fig. 4.16) down-convert the D-band signal to (I, Q) baseband. The differential output of the LNA drives both mixer inputs through a transformer. The quadrature (I, Q) LO signals are converted to differential form by transformers before driving the FET mixer gates. The baseband (I, Q) mixer outputs are DC-coupled to transimpedance amplifiers. To ensure sufficient LO drive power, the outputs of the LO multiplier are passed through a 4-stage post-amplifier before driving the mixer LO ports. This is not area efficient, but ensures that we get enough LO power at the mixer LO ports. Hence, the down-conversion mixer's conversion gain is not affected severely.

A pseudo-differential transimpedance amplifier provides the receivers' baseband gain. A three-stage voltage amplifier is first formed by an input g_m stage cascaded with two voltage-gain stages formed from g_m cells with local resistive feedback; adding global shunt resistive feedback forms a transimpedance amplifier (Fig. 4.16). A test structure for a single ended TIA was measured. Fig. 4.17 shows the simulated and measured (S_{21}), which shows agreement in gain between simulation and measurement. There is some

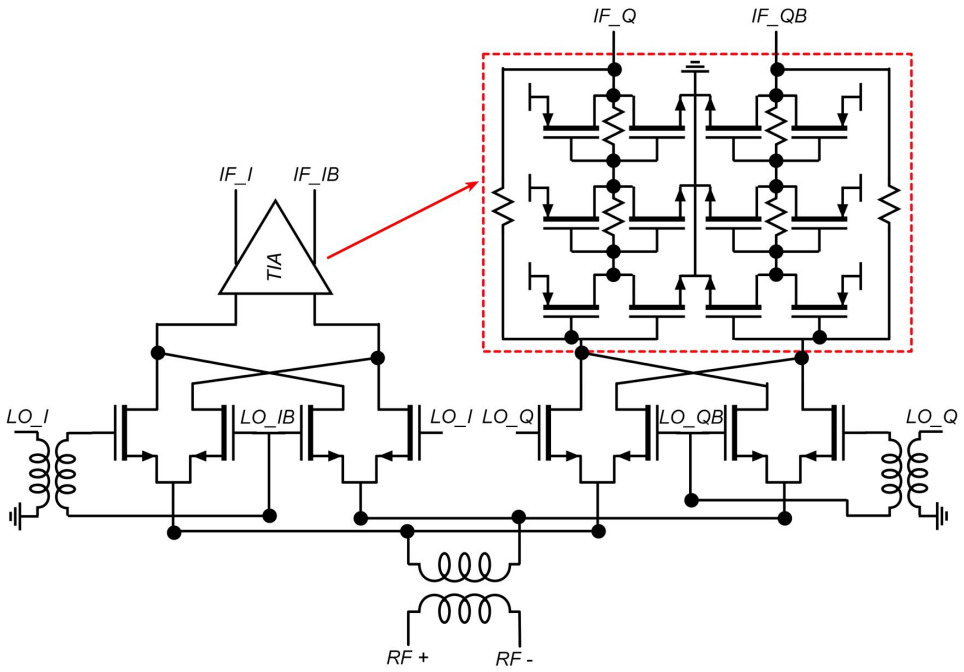

Figure 4.16: Schematic diagram of the down-conversion mixer with the trans-impedance amplifier schematic shown inset

discrepancy in the 3-dB bandwidth between simulation (22 GHz) and measurement (17 GHz), which is likely due to errors in parasitic extraction. The measured S-parameters shows a notch at DC, this is because the test structure is a single ended, and the supply capacitance in the test structure resonates with the DC supply probe inductance. In the receive chain, the design is less sensitive to supply inductance, as the design is pseudo-differential.

4.3.4 Up-conversion Mixer

In the direct conversion transmitter, a pair of double-balanced Gilbert-cell mixers upconverts the (I, Q) baseband signals to D-band. The (I, Q) signals are then summed and drive a broadband power amplifier. The LO multiplier is the same as that in the receiver except the interstage transformer to the amplifier. In the transmitter active Gilbert-cell based mixer is used since the conversion loss is low for the passive mixer,

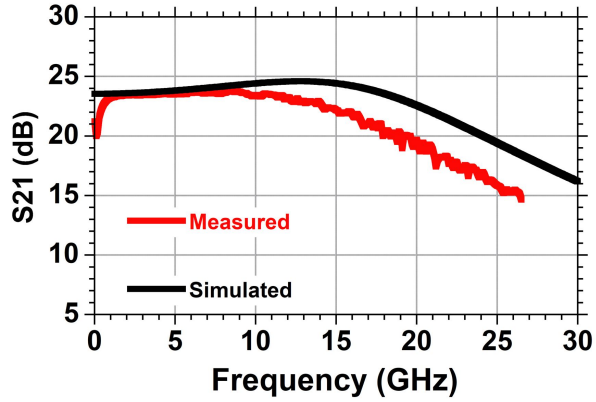

Figure 4.17: Simulated and measured TIA S-parameters

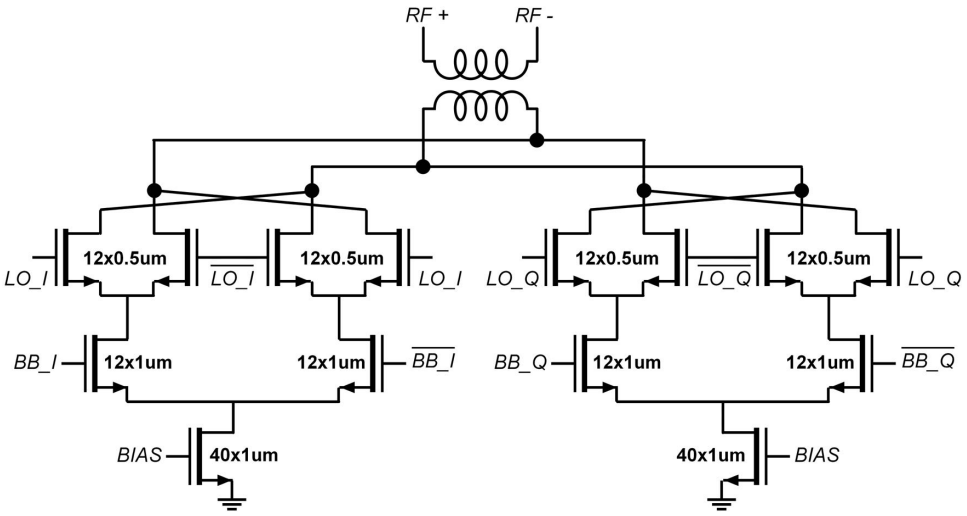

Figure 4.18: Schematic of the up-conversion mixer - Gilbert cell based IQ modulator

and can't drive the power amplifier. A pair of Gilbert cells serve as the IQ modulator (Fig. 4.18). The baseband inputs are DC coupled, while the LO and RF output ports are transformer-coupled. Despite being active, the mixer gain is low (2 dB in simulation) because of the 50 Ω RF port loading.

4.4 Design and Measurements of a Transmit and Receive Channel at D-Band

A direct conversion receiver (Fig. 4.19) consists of a 4-stage broadband LNA and a double balanced passive mixer, followed by a pseudo differential wideband transimpedance amplifier, for both in-phase (I) and quadrature phases (Q). The mixer is driven by an on-chip LO multiplier (x9), where the LO input signal is driven from external source at 15 GHz. The (I,Q) LO signals are generated by adding a ($\lambda/4$) delay line in the LO signal path, introducing a phase shift. This is done to eliminate the 90° hybrid loss at the end of the multiplier chain. In addition, we placed 4 stages post-amplifier at 135 GHz in order to make sure we saturate the output and drive the mixer LO input with enough power. However, this has a problem of frequency dependent phase shift, therefore it is not optimum design for the IQ balance.

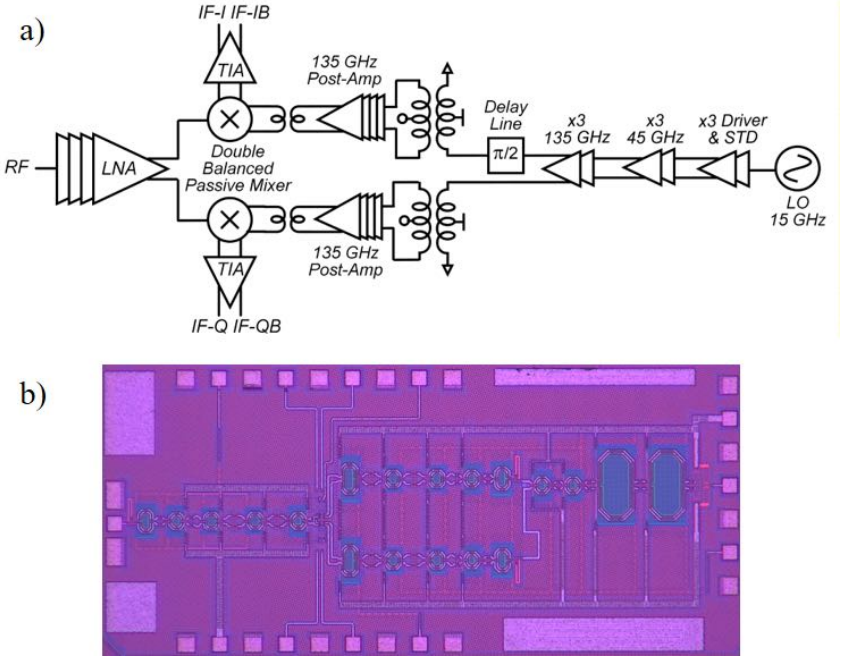

Figure 4.19: (a) Schematic and (b) layout of the receiver channel at D-Band

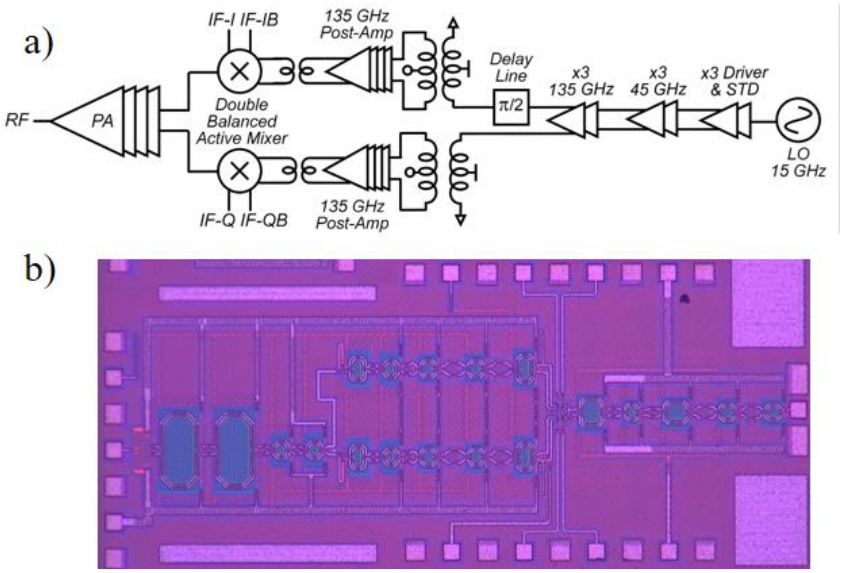

Figure 4.20: (a) Schematic and (b) layout of the transmitter channel at D-Band

In the direct conversion transmitter (Fig. 4.20), a pair of double-balanced Gilbert-cell mixers upconverts the (I, Q) baseband signals to D-band. The (I, Q) signals are then summed and drive a broadband power amplifier. The LO multiplier is the same as that in the receiver.

Transmitter and receiver channels are fully characterized using on wafer probing. The receiver conversion gain is measured using Virginia diodes AMC 333 as the input signal source, followed by GGB (90-140 GHz) probe to excite the receiver RF port. The two differential outputs are terminated by 50 Ω impedances during measurement.

Fig. 4.21 shows the measured conversion gain with LO signal fixed at 134 GHz and 135 GHz, while the input signal is swept from 122 GHz to 155 GHz. This measures the receiver modulation bandwidth. The measured gain is 27 dB, after de-embedding probe loses and correcting for single ended to differential conversion. The 3-dB bandwidth is 20 GHz. There is a good agreement between the measured and simulated gain. However, the simulated 3-dB BW is 1.5:1 larger than the measured. Fig. 4.22 shows the frequency dependent conversion gain, with a fixed baseband frequency, where the RF and LO

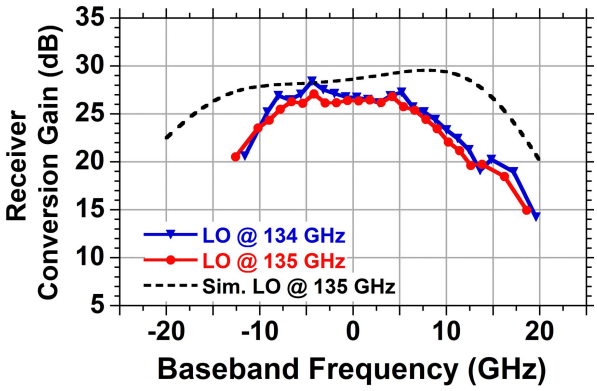

Figure 4.21: Receiver conversion gain vs. baseband frequency with a fixed LO frequency

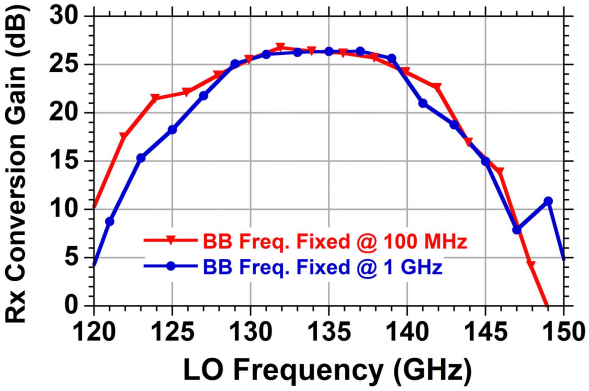

Figure 4.22: Receiver conversion gain vs. LO frequency with fixed baseband frequency

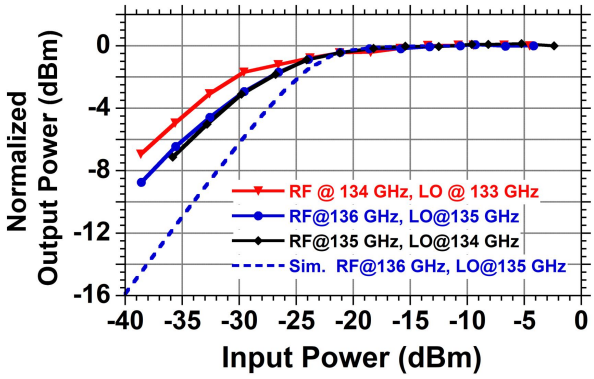

Figure 4.23: Receiver normalized output power vs. input power

signals are swept to keep the baseband frequency fixed at either 1 GHz or 100 MHz. This measures the receiver RF tuning range. The 3-dB bandwidth is here limited to 10 GHz. Smaller bandwidth than the prior measurement reflects the additional constraint coming from the LO tuning range. Receiver 1-dB compression point is measured (Fig. 4.23) at different LO frequencies. The measured input P_{1dB} is -30 dBm, which is slightly smaller than the simulated -26 dBm. The receiver compression point is limited by the TIA drive capability, as this stage drives 50 Ω

Transmitter saturated output power is measured using Erickson PM4 power meter,

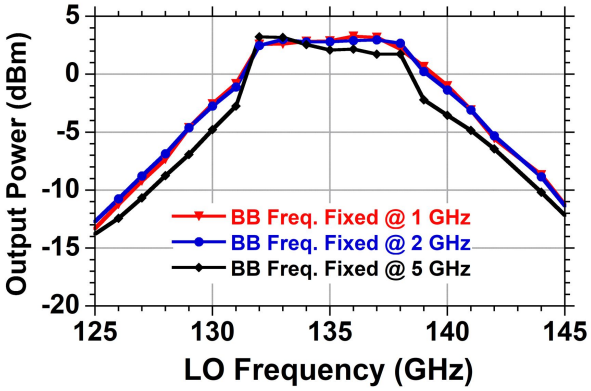

Figure 4.24: Saturated output power as a function of carrier frequency, with an 0 dBm baseband input signal, this showing an 8 GHz RF tuning range.

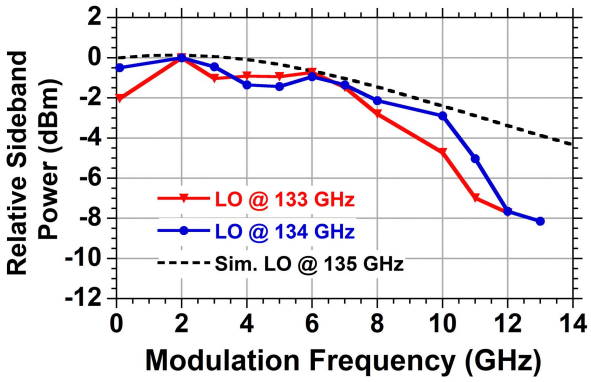

Figure 4.25: Modulation sideband power as a function of modulation frequency, this showing a ~ 8 GHz (SSB) modulation bandwidth.

where external signal generators drive the I and Q mixer inputs. To determine the transmitter saturated output power as a function of frequency, the transmitter was first driven by 0 dBm signals at 1, 2, or 5 GHz at the (I, Q) ports, and the LO was swept from 125 GHz to 145 GHz (Fig. 4.24). The saturated output power is 2.8 dBm with a 3-dB bandwidth of 8 GHz. This determines the transmitter frequency tuning range. Fig. 4.25 shows the normalized modulation sideband power with the baseband input frequency swept and the LO frequency held fixed. This measures the transmitter modulation response. The output spectrum was measured using an OML M05HWD harmonic mixer and a Rohde & Schwarz spectrum analyzer. There is a good agreement between the simulated and measured 3-dB bandwidth.

Fig. 4.26 shows the gain compression characteristics as a function of carrier frequency. The transmitter small signal gain is 18-dB. The compression in the gain curve at low input power is due to LO leakage.

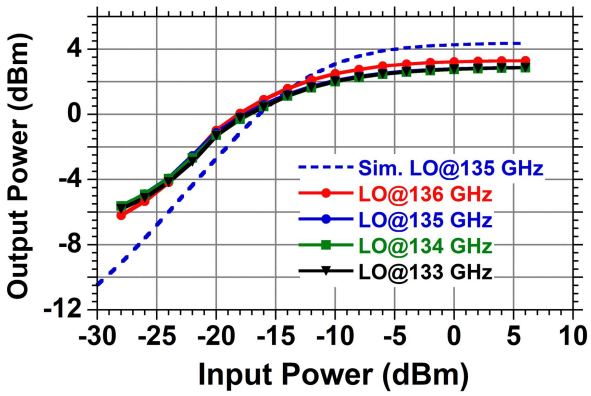

Figure 4.26: Transmitter output power as a function of input power, showing a typical 18 dB gain.

4.5 Conclusion

A broadband single-channel transmitter and receiver at D-band using the 22 nm CMOS FDSOI technology are demonstrated. Conversion gain of the entire receive channel is 27 dB with a 3-dB bandwidth of 20 GHz. The transmitter shows conversion gain of 18 dB with a saturated output power of 2.8 dBm. The transmitter and receiver consumes 196 mW and 198 mW respectively from a 0.8 V supply, both dominated by the 137 mW LO multiplier DC power consumption. The transmitter and receiver both have bandwidth sufficient for 10 GBaud transmission. There is no modulation limitation and these chips should be able to support 64, 128, 256 QAM modulations as well as the QPSK. This further increases the data rate that can be transmitted using these chips. If we can transmit 10 GBaud using 64-QAM, this means 80 Gb/s data transmission.

This transmitter and receiver channel can be used to implement single or multi-beam phased arrays by integrating them with off-chip antennas. Since these chips are direct conversion to I/Q baseband, full digital beamforming in the digital domain needs to be used for the baseband processing. The array size can be increased in a tiled approach. This way we can create arrays with 32, 64, 128 or even 1000s of elements. Moreover, we

can support multiple beams using these arrays. If each beam can support 10 GBaud or 20 Gb/s with QPSK, with 100 beams we can support 2 Tb/s data transmission. This can potentially create wireless communications at fiber speeds.

Chapter 5

Transceiver Measurements using 45 nm CMOS SOI at 140 GHz

5.1 Introduction

The increasing data consumption of mobile users demands high-data-rate wireless links. Millimeter waves (mm-Waves) provide wide unlicensed and unallocated frequency bands, creating an opportunity for wideband and high-speed applications. At these frequencies signal range is limited and attenuation can be severe; signal strength is recovered using phased arrays [90, 93]. The short wavelengths permit many simultaneous independent beams, massive MIMO, even from small antenna apertures. CMOS technologies are preferred for these applications due to their low cost and high integration capability. State of the art CMOS technologies now have power gain and current gain cut-off frequencies in 200-250 GHz range, referenced to the top metal layer [86]. It is now possible to develop mm-Wave transceivers and MIMO systems using CMOS [87, 88, 89].

In this chapter, we provide the measurement results and the one channel data transmission experiments of a previously designed 140 GHz 4-Channel MIMO transceivers in

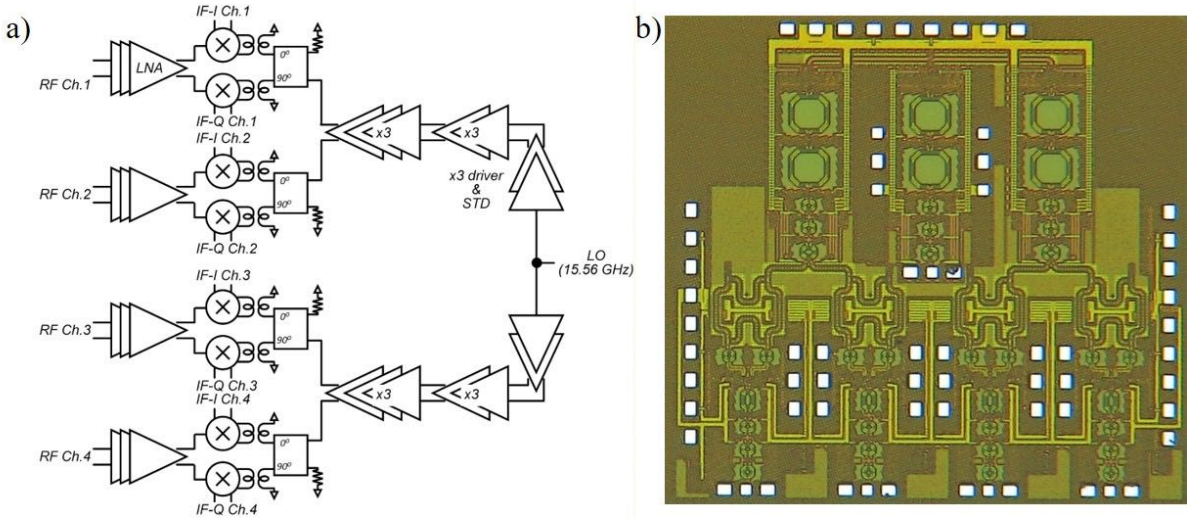

Figure 5.1: 140 GHz 4-channel MIMO receiver (a) circuit block diagram and (b) microscope image. Including pads, the die is 1.69 mm × 1.76 mm.

45 nm CMOS SOI technology from Global Foundries. Dr. Seong-Kyun Kim led the design efforts of these ICs. Chapter starts with the design summary and the measurements of the individual circuit blocks. Then, we provide one channel transmitter and receiver measurements. After, we present system impairment measurements including receiver noise figure and transmitter LO suppression. We then demonstrate the end to end data transmission using one channel of these transceivers with horn antennas over 25 cm air.

5.2 Receiver and Building Blocks

The four-channel receiver (Fig. 5.1) is direct conversion, with a three-stage LNA followed by double-balanced passive down-conversion mixers in the in-phase (I) and quadrature-phase (Q) signal paths. The I/Q baseband signals then pass through ∼ 20 dB gain on-wafer transimpedance amplifiers (not shown in Fig. 5.1). A 9:1 frequency multiplier chain and a 90° hybrid coupler generate the (I, Q) local oscillator signals. The 4-channel receiver is 1.69 mm × 1.76 mm.

The differential LNA shown in Fig. 5.2 uses capacitive cross-coupled neutralization of the gate-drain capacitance to boost the limited transistor maximum available gain at 140 GHz and to reduce interaction between the input and output tuning networks. Transformers match impedances between stages. The transistors use 24 double-contacted gate fingers of 1 μm length, and are biased at $\sim 0.3\,\mathrm{mA}/\mu\mathrm{m}$ with 1 V supply. The transistor footprint is simulated using the PEX parasitic extraction tool up to metal layer 3, with the remaining metal layers modeled using a 3D full-wave electromagnetic simulator (Ansys HFSS). Matching network elements are also modeled using HFSS.

In simulations (Fig. 5.3), the 3-stage LNA has 19.2 dB gain at 140 GHz, a peak 20 dB gain at 145 GHz, and 20 GHz bandwidth. The simulated noise figure is 5.2 dB, which is low [25, 89], but has yet to be measured. S-parameters of the LNA are measured using an Agilent PNA-X network analyzer, G-band (140-220 GHz) OML VNA extension modules, and GGB 140-220 GHz wafer probes. The measured peak gain is 19-20 dB, close to simulation, but the measured 3 dB bandwidth, at 10 GHz, is much smaller than measurement. We ascribe the difference between simulation and measurement to the device models, which, at the time of design, had not been confirmed by 140 GHz on-wafer measurements. LNA consumes 42.4 mW power from a 1 V supply.

The 4-channel receiver uses two 9:1 frequency multipliers to generate the 140 GHz

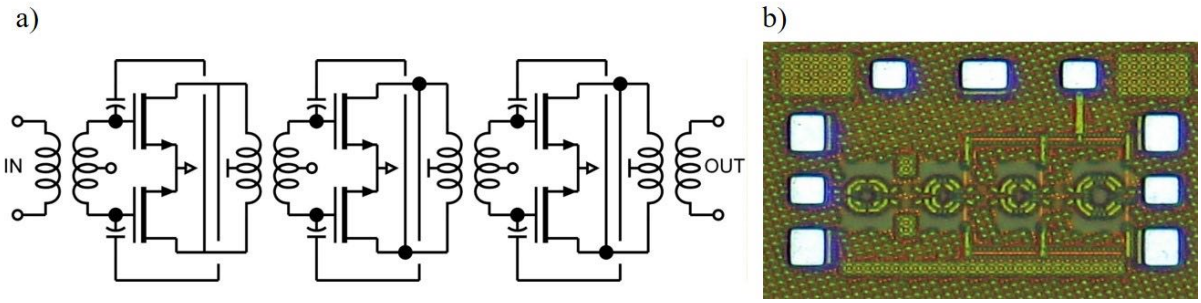

Figure 5.2: 140 GHz 3-stage LNA (a) circuit diagram and (b) microscope image. Excluding pads, the die is $0.32\,\mathrm{mm} \times 0.17\,\mathrm{mm}$.

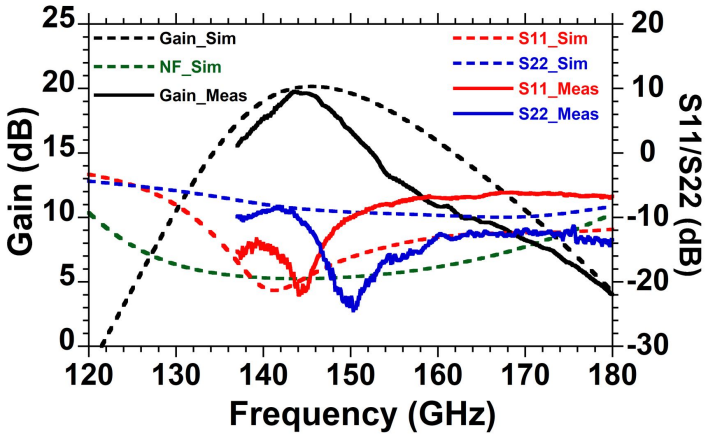

Figure 5.3: a) Simulated (dashed) and measured (solid) S-parameters of the LNA

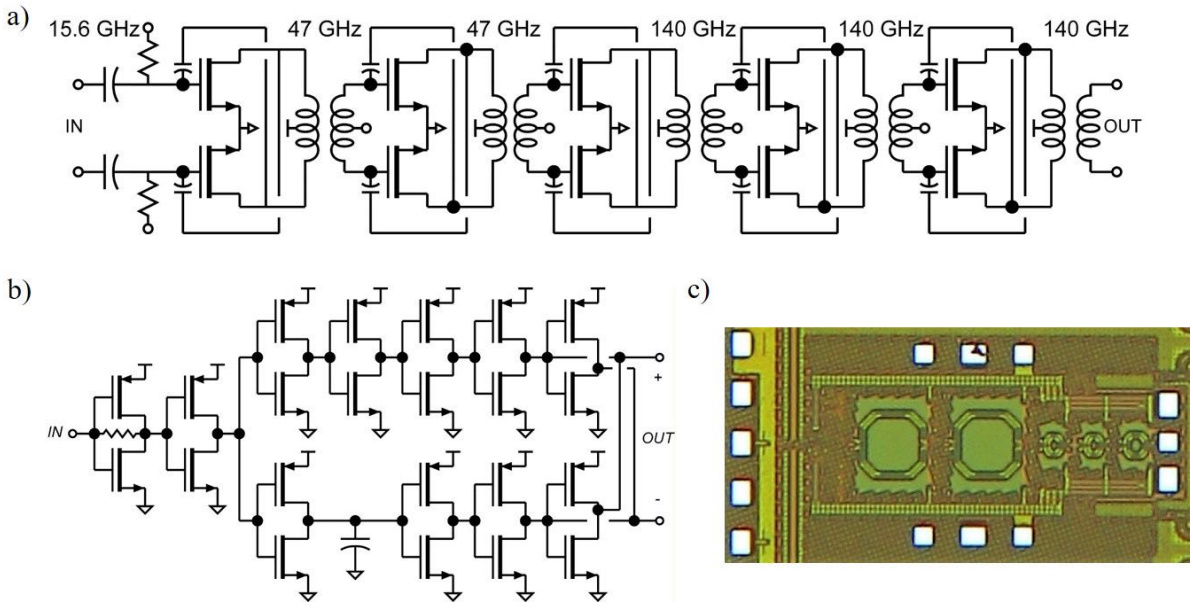

Figure 5.4: Circuit schematics of a) cascaded 3:1 multipliers and b) the single ended to differential conversion c) Microscope image of the multiplier. Excluding the pads, the die is 0.65 mm × 0.27 mm.

LO from an external 15.56 GHz reference, with each multiplier serving two channels (Fig. 5.1). Each 9:1 multiplier consists of a digital single-ended to differential converter (Fig. 5.4b) and cascaded 3:1 multipliers (Fig. 5.4a). The multipliers are similar in topology to the LNA (Fig. 5.2a), with transformer-coupling, cross-coupled capacitive neutralization,

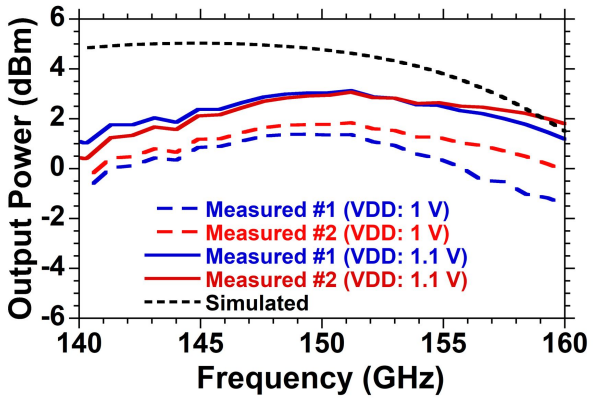

Figure 5.5: Simulated and measured output power vs. frequency curves for the LO multiplier breakout with 1 V and 1.1 V supply voltages.

and differential stages to reduce even harmonic generation. In the transformer-coupled chain (Fig. 5.4a) the first stage, driven into strong limiting, generates the 3rd harmonic of the 15.56 GHz input, and its output is tuned to 47 GHz. The second transformer-coupled stage operates as a 47 GHz amplifier. The third stage, with its output tuned to 140 GHz, operates as a multiplier, while the fourth and fifth stages operate as 140 GHz amplifiers. The multiplier's simulated output power is 5 dBm from 140 to 150 GHz, while the measured output power is 1-3 dBm from 140 to 160 GHz with a 1.1 V supply shown in Fig. 5.5. Multiplier consumes 98 mW from a 1 V supply and 108 mW from a 1.1 V supply.

For high dynamic range, the (I, Q) down-conversion mixer is passive (Fig. 5.6.a), using double-balanced CMOS switches. The mixers are followed by baseband pseudo-differential transimpedance amplifiers (TIAs, Fig. 5.6b). Fig. 5.6c shows the simulated and measured gain (S_{21}) of the TIA. In simulations, the overall receiver showed 31.5 dB conversion gain and 5.5 dB double sideband noise figure given a 140 GHz RF and a 1 GHz baseband output signal at 27°C. Fig. 5.7 demonstrates the simulated receiver performance at a fixed LO of 139 GHz.

Transmitter and receiver single-channel characteristics were measured with all four

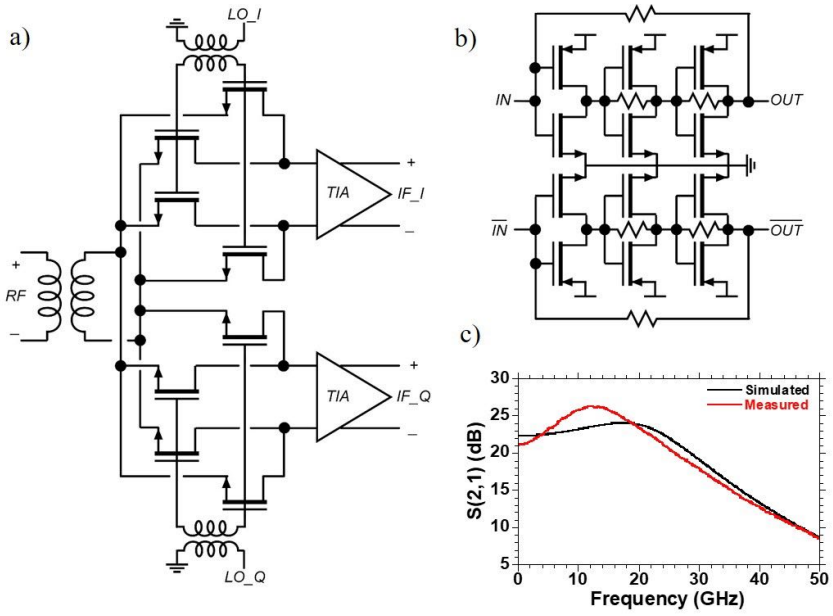

Figure 5.6: Circuit diagram of (a) the (I, Q) down-conversion mixer and (b) the baseband transimpedance amplifier. (c) Shows the simulated (black) and measured (red) gain S_{21} of the transimpedance amplifier.

channels biased. Linear S-parameter measurements used the equipment noted earlier; receiver gain characteristics are quoted with one of the two differential baseband outputs terminated in 50 Ω. Fig. 5.8a show the measured receiver frequency-dependent conversion gain with a fixed 145.9 GHz LO frequency, and with the baseband (and hence RF) frequencies swept. All data are corrected for probe losses and single ended to differential conversion. The measured conversion gain is 18 dB with 12 GHz 3-dB bandwidth. The difference ($\sim$ 30 vs $\sim$ 18 dB) in receiver's simulated and measured performance is likely a result of the reduced LO multiplier output power (Fig. 5.5). Fig. 5.8b shows the measured frequency-dependent gain with a fixed 100 MHz baseband frequency and with the RF (and hence LO) frequencies swept. The narrow-band 145 GHz zero in the transfer function, possibly the result of a power-supply resonance, will limit the transceiver data rate to 2-4 GBaud. It can possibly related with the early compression of the receiver channel due to the input power at this specific measurement. The 4-channel receiver

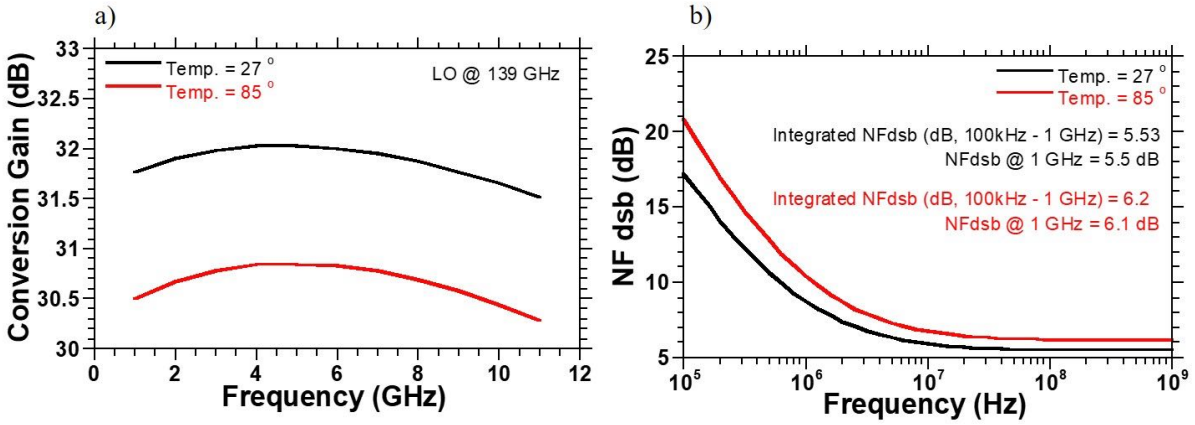

Figure 5.7: a) Simulated conversion gain and b) simulated double side band NF of the receive channel for two different temperatures

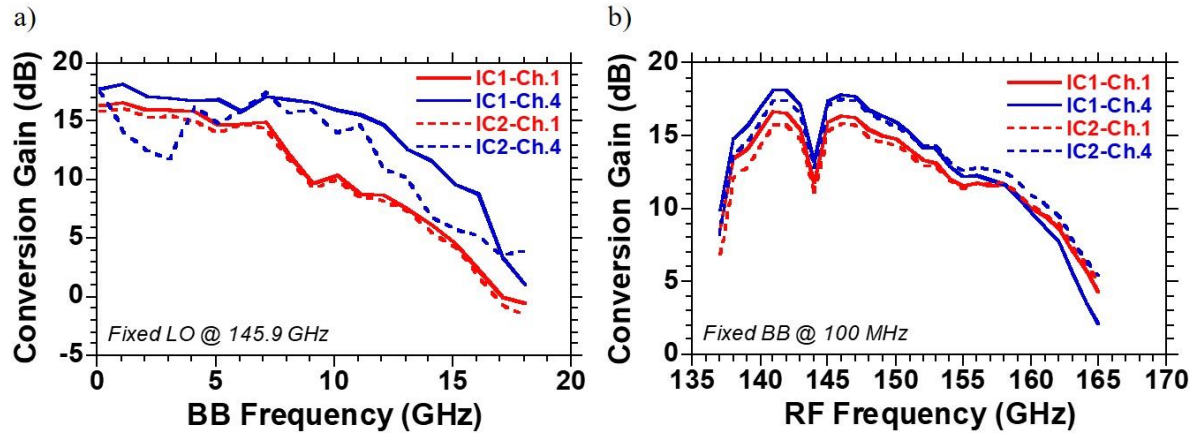

Figure 5.8: Measured conversion gain of two different receive channels of two different chips with (a) fixed LO at 145.9 GHz (b) fixed baseband at 100 MHz

operates with 1 V supplies for LNA, TIA and multiplier with 163 mA, 109 mA and 223 mA current consumption, hence 495 mW total power consumption for the 4-channel receiver.

5.3 Transmitter and Building Blocks

The transmitter design is similar to that of the receiver, except that the up-conversion mixers are active Gilbert cell designs (Fig. 5.9). The three-stage LNA of the receiver

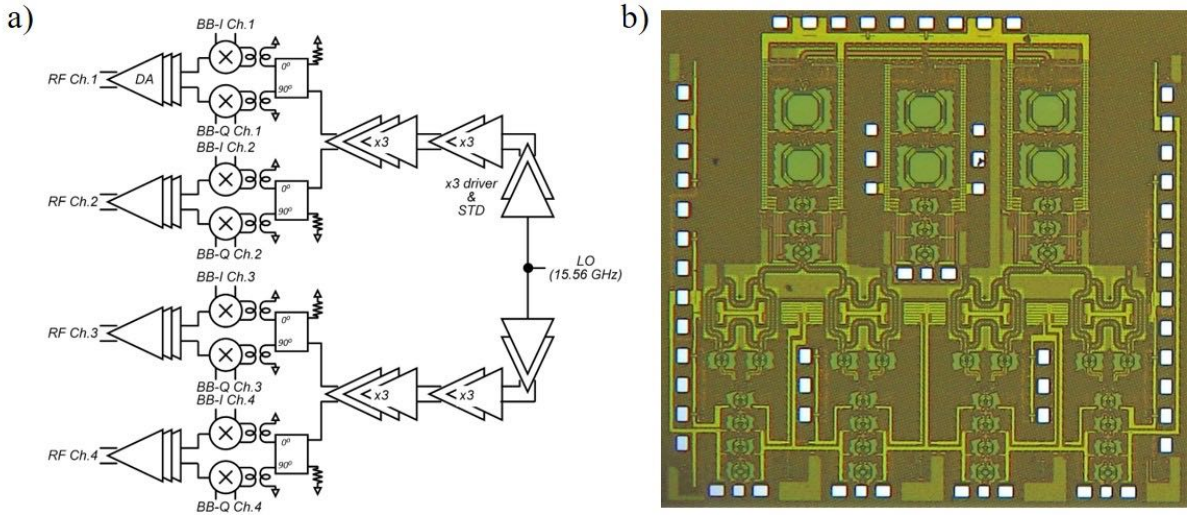

Figure 5.9: Circuit block diagram (a) and microscope image (b) of the 4-channel transmitter (Size = 1.67 mm × 1.76 mm).

was used, without modification, as the transmitter power amplifier. IQ modulator uses double-balanced (Gilbert cell) mixers (Fig. 5.10a). The baseband inputs are digital, with a digital single-end to differential converter (Fig. 5.10b). This eases testing, but restricts transmitter operation to simple QPSK, and, further, prevents transmitter spectral shaping with e.g. root-raised-cosine modulation waveforms. In simulations, the power amplifier showed 4.3 dBm output power at 1-dB gain compression (P_{1dB}) (Fig. 5.11) in single-tone operation. Similarly, simulated transmitter output power in QPSK operation is $\sim$ 4.2 dBm.

The transmitter was tested with modulation on the Q input, with the I input held at a logic zero. Spectral measurements were performed using a mm-Wave harmonic mixer and a microwave spectrum analyzer; measurements were corrected for probe losses. To measure the modulation bandwidth, the LO is held fixed at 146 GHz, the baseband input frequency is swept, and the power in the double side band (DSB) modulation sidebands is measured (Fig. 5.12a). From this measurement, the 3-dB modulation bandwidth is around 6 - 8 GHz. This is measured for one side only, possibly two-sided bandwidth is

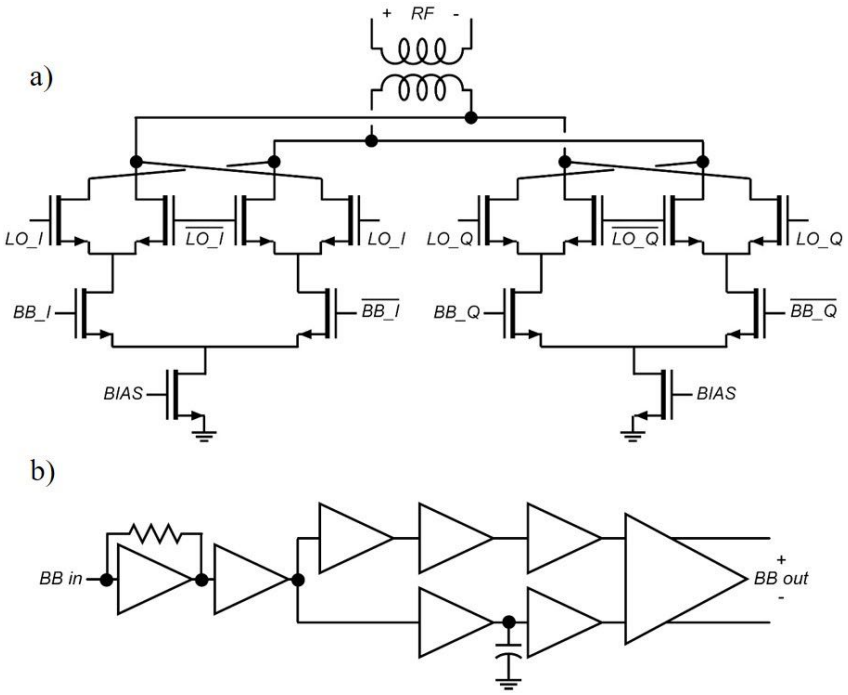

Figure 5.10: Circuit diagram of a) Gilbert cell based IQ vector modulator b) baseband input driver

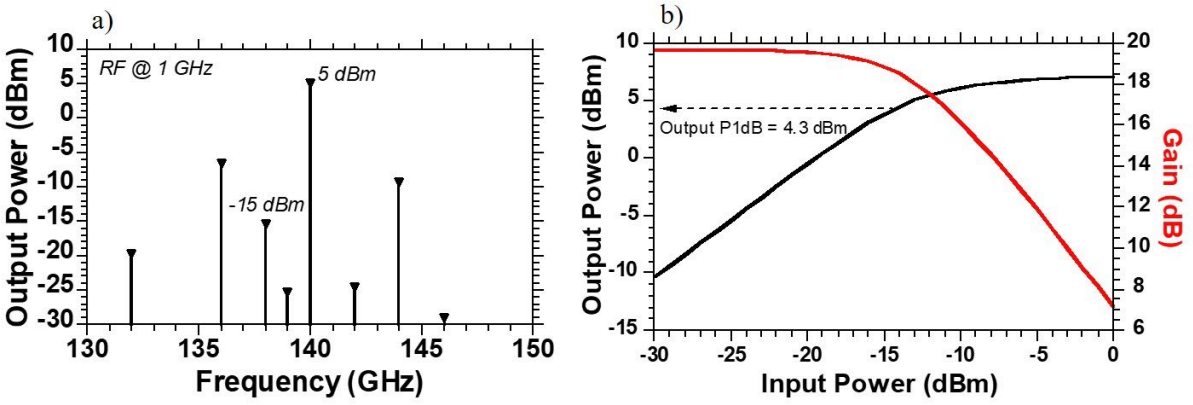

Figure 5.11: (a) Simulated output power spectrum in single-sideband operation (b) Simulated output power, and gain vs. input power of the power amplifier

higher. Then, logic 0/1 was applied to I and Q baseband inputs and the transmitter output power was measured using a power meter while sweeping the LO frequency (Fig. 5.12b). Total transmitter output power is -2 dBm with 1 V supply, and 3 dBm with 1.2 V supply at 145 GHz LO frequency.

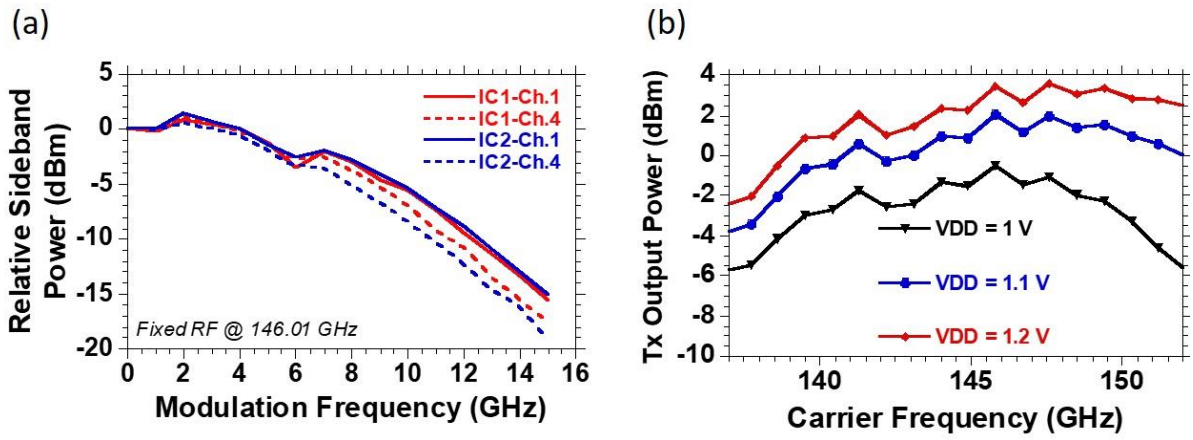

Figure 5.12: (a) Measured relative sideband power vs. modulation frequency with fixed RF frequency at 146.01 GHz for two different transmitter channels in two different ICs (b) Transmitter total output power vs. carrier (LO) frequency with baseband I and Q inputs (0/1) at 1, 1.1, and 1.2 V supply voltages

The 4-channel transmitter operates with 1 V power supplies for driver amplifier, mixer and multiplier chain, with 161 mA, 94 mA and 208 mA current consumption, hence 463 mW total power consumption of the 4-channel transmitter. Although these chips are designed to support 10 GBaud QPSK data transmission, due to the notch in RF frequency-gain curve, it is expected to support up to 5 GBaud QPSK data transmission. However, this notch can be due to the measurement error. One possibility is that receiver compressed with the applied input power at the measurement condition. If this is the case higher data rate transmission can be possible.

5.4 System Impairment Measurements

After the full characterization of the gain-frequency behavior of the receiver and transmitter channels, we measured the receiver noise figure and the transmitter IQ imbalance and LO suppression. In order to use these chips in a system, noise figure measurement is critical to evaluate the system dynamic range. Transmitter LO suppression and IQ

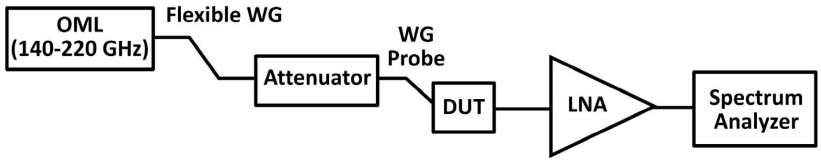

Figure 5.13: Noise figure measurement setup using gain method

imbalance is also important to know to evaluate how much correction is needed in the system side, and whether they are in the acceptable range.

Receiver noise figure is measured using the gain method, since 140 GHz noise source is missing in the lab. In this method, it is important to drive the receiver with really low power, so that receiver is in the linear region. In this method, OML frequency extension module (140-220 GHz) is used to input the receiver. OML output power is $\sim -22\,\text{dBm}$, therefore we added additional waveguide sections and attenuators to drive the receiver with $\sim -65\,\text{dBm}$ input power. Measurement is performed using wafer probe from GGB at 140-220 GHz band at the input. Output is connected to an external amplifier with $\sim 4.5\,\text{dB}$ noise figure, 22 dB gain and 5 GHz 3-dB bandwidth. Fig. 5.13 shows the experimental setup.

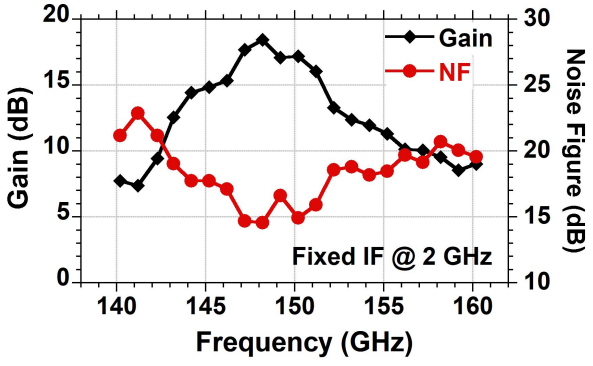

Figure 5.14: Gain and noise figure of the receive channel at fixed IF frequency of 2 GHz

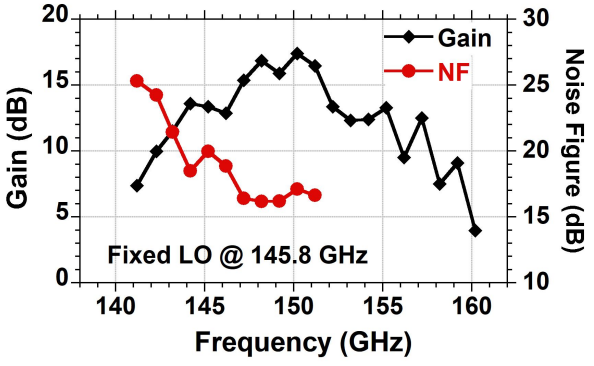

Figure 5.15: Gain and noise figure of the receive channel at fixed LO frequency of 145.8 GHz

In the gain method, we first measure the output power at the spectrum analyzer with

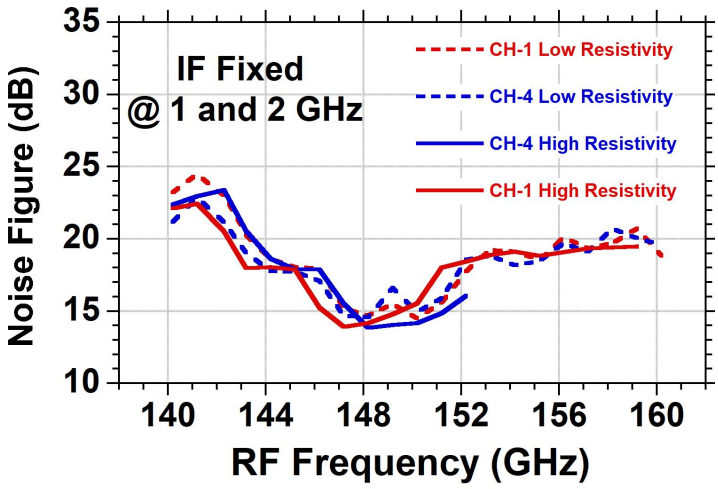

Figure 5.16: Noise figure when IF is fixed at 2 GHz for different channels and low vs. high resistivity substrates

input power on and find the system gain. Losses of the waveguide probe, cables and gain of the external amplifier is de-embedded. Then, measurement is repeated with the input terminated with 50 Ω to find the total output noise power ($P_{N,OUT}$). In this case since there is not available 50 Ω waveguide termination, we just turned the input off and assumed that with that low power and OML heads, input is roughly terminated with 50 Ω impedance. Using these results noise figure (NF) can be calculated as in eq. 5.1.

$$NF = P_{N,OUT} - (-174\,\text{dBm/Hz} + 10\log_{10}(\text{BW}) + \text{Gain}) \tag{5.1}$$

Noise figure (NF) is measured in two different cases. First, IF is fixed at 2 GHz, and RF and LO frequencies swept together. Fig. 5.14 shows the NF results in this case. Then, LO is fixed at 145.8 GHz, and RF is swept. For this case NF is measured as in Fig. 5.15. Moreover, NF with fixed LO frequency is measured for low resistivity and trap rich substrate for 2 different channels for each case. As can be seen in Fig. 5.16 all results are close to each other. High resistivity substrate shows only slightly less NF than the low resistivity substrate. In all cases, NF is about 15 dB, whereas simulations predict only

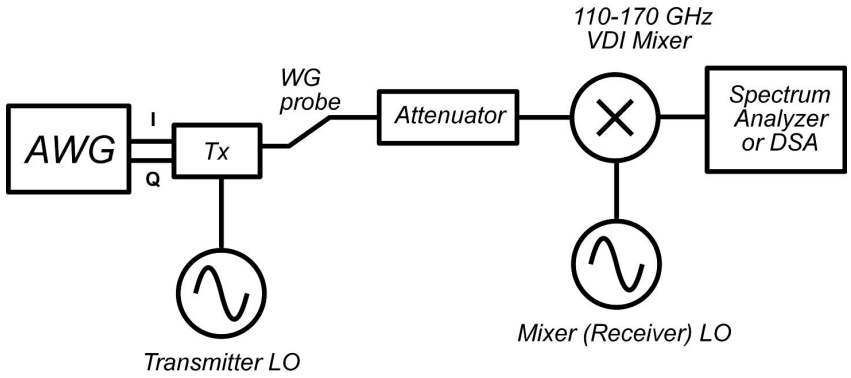

Figure 5.17: Schematic of the measurement setup for transmitter characterization

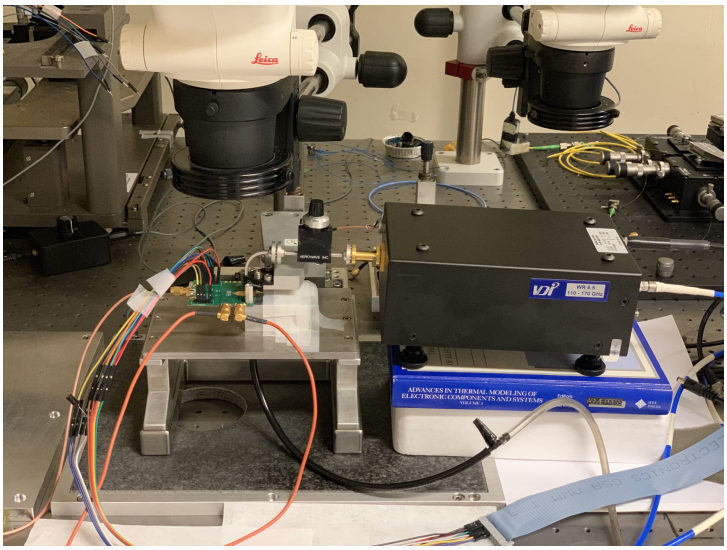

Figure 5.18: Image of the measurement setup for transmitter characterization

about 5.5 dB of NF. The main reason of this drop is likely due to the 12 dB drop in the overall gain of the receiver. This gain drop mainly happened in down-conversion mixer, hence the noise contribution of the TIA is not suppressed.

For the transmitter side, LO suppression and IQ imbalance are the important parameters in terms of the system performance. In order to measure this, experiment setup in Fig. 5.17 is used. Fig. 5.18 shows the actual setup built in the lab. To perform this experiment, printed circuit board for the transmitter chip is designed and fabricated. I/Q

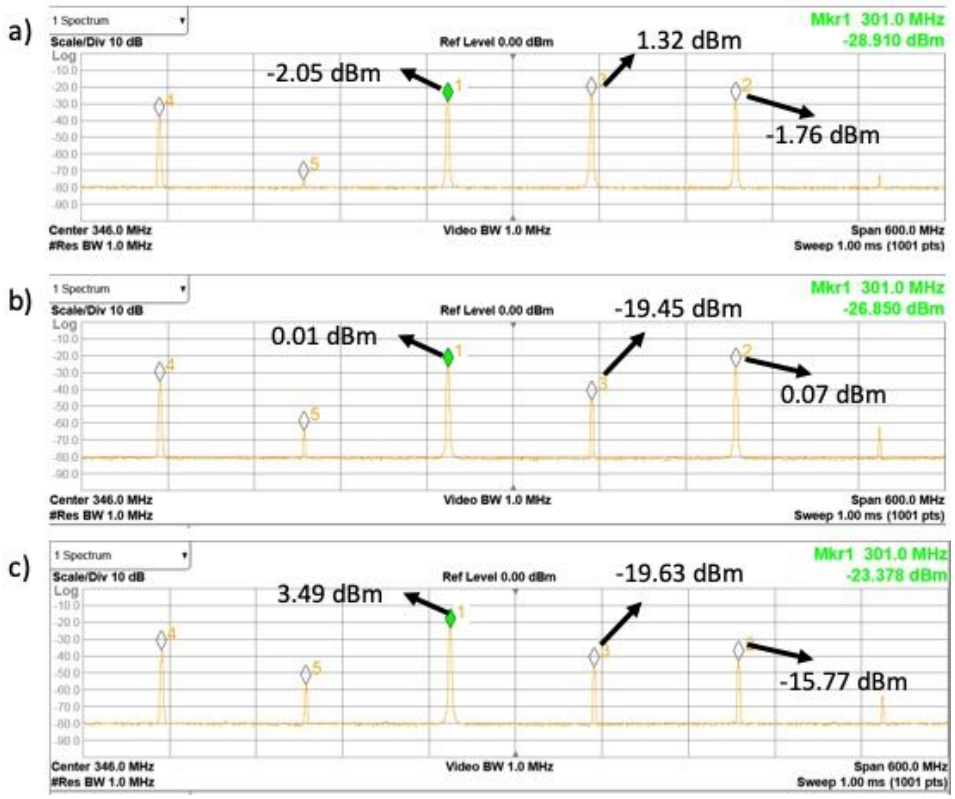

Figure 5.19: Transmitter output spectrum with single tone waveform (a) when only I channel is applied (b) same signal applied to I and Q (c) I-Q waveform with 90 degree phase difference is applied (Black bold numbers are corrected values)

signals, all bias pads and the LO signal are wire-bonded to the PCB and connected to the outside world via SMA cables and DC connectors. 140 GHz signal is not wirebonded, and it is wafer probed using GGB WR-05 waveguide probe. I/Q signals are applied to transmitter with an LO frequency of 144 GHz, and output spectrum is saved in the spectrum analyzer through waveguide probe, attenuator, and VDI harmonic mixer (110-170 GHz, WR-6). Losses of the waveguide probe, attenuator and VDI harmonic mixer are de-embedded. Fig. 5.19 shows the results for three different cases. Fig. 5.19 (a) shows the case where only I signal applied. In this case, LO is not suppressed and I-Q sidebands are approximately at the same power. In the Fig. 5.19 (b) same signals are applied to I and Q paths without the 90 degree phase delay. In this case, LO is suppressed and

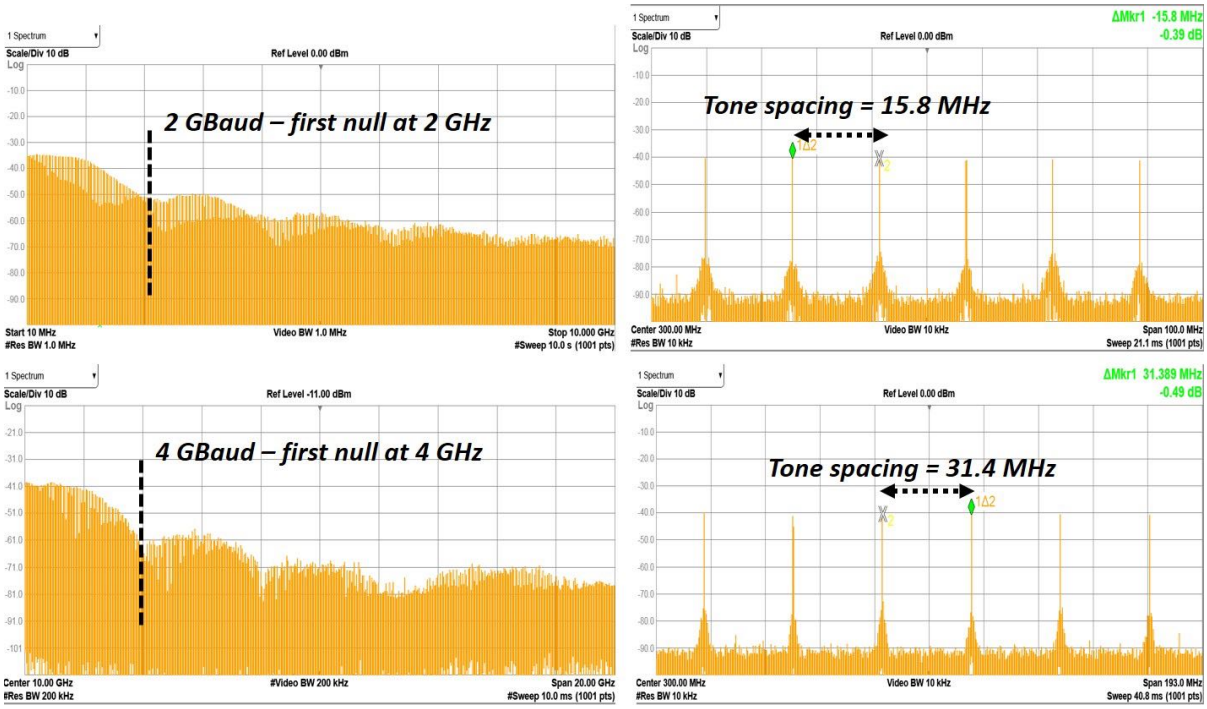

Figure 5.20: Transmitter output spectrum (sinc waveform) with PRBS data of length $(2^7 - 1)$ (a) with 2 GBaud data transmission, first null happens at 2 GHz with tone spacing of 15.8 MHz, which is equal to $2\,\text{GBaud}/(2^7 - 1)$ (b) with 4 GBaud data rate, first null happens at 4 GHz with tone spacing of 31.4 MHz, which is equal to $4\,\text{GBaud}/(2^7 - 1)$

I-Q sidebands are approximately at same power level. LO suppression is about 20 dB. I/Q signals with 90 degree phase delay are applied in Fig. 5.19 (c), where both upper sideband and LO is suppressed. This case is known as the single sideband modulation. In this case LO suppression is about 23 dB, and sideband suppression is about 20 dB. Main sideband power is about 3.5 dBm.

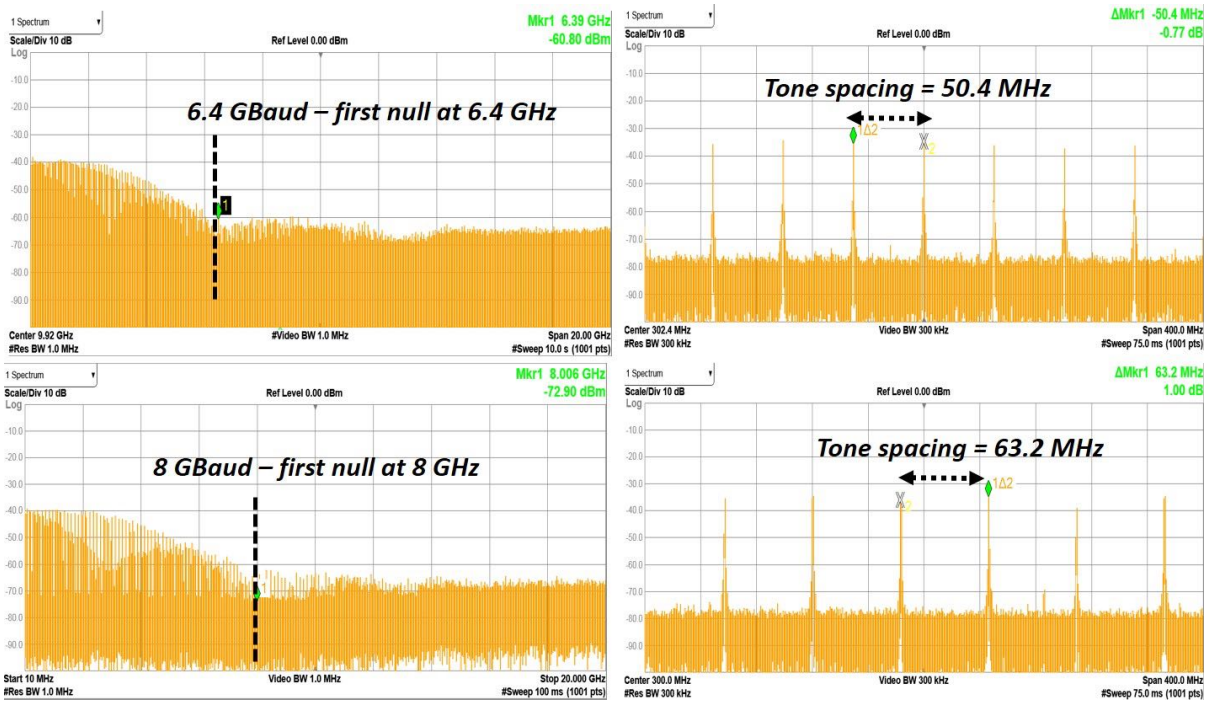

Figure 5.21: Transmitter output spectrum (sinc waveform) with PRBS data of length $(2^7 - 1)$ (a) with 6.4 GBaud data rate, first null happens at 6.4 GHz with tone spacing of 50.4 MHz, which is equal to 6.4 GBaud $/(2^7 - 1)$ (b) with 8 GBaud data rate, first null happens at 8 GHz with tone spacing of 63.2 MHz, which is equal to 8 GBaud $/(2^7 - 1)$

5.5 140 GHz Wireless Communication Link using Horn Antennas

As a final step the transmitter and receiver performances are evaluated through wireless data transmission experiment using one channel of the transmitter and receiver. First, only transmitter is used, again using the experiment setup in Fig. 5.17, independent pseudo-random bit sequence (PRBS) with $(2^7 - 1)$ length applied to I/Q channels and output is observed at the spectrum analyzer. In this experiment, one expects to see a sinc waveform (Fourier transform) with first null at the data rate with the tone spacing of data rate / sequence length $=$ data rate $/\,(2^7 - 1)$.

Fig. 5.20 demonstrates the results for 2 and 4 GBaud, where first nulls at the sinc

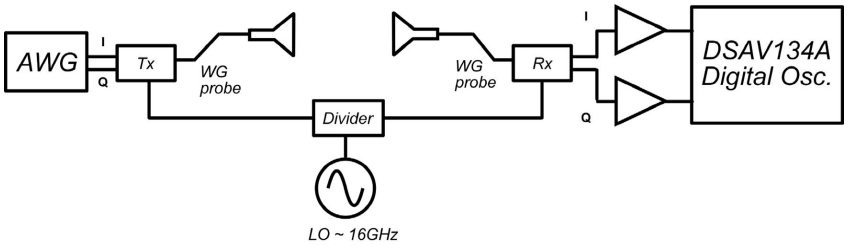

Figure 5.22: Schematic of the experimental setup for transceiver wireless data transmission experiment with horn antennas (20 cm link)

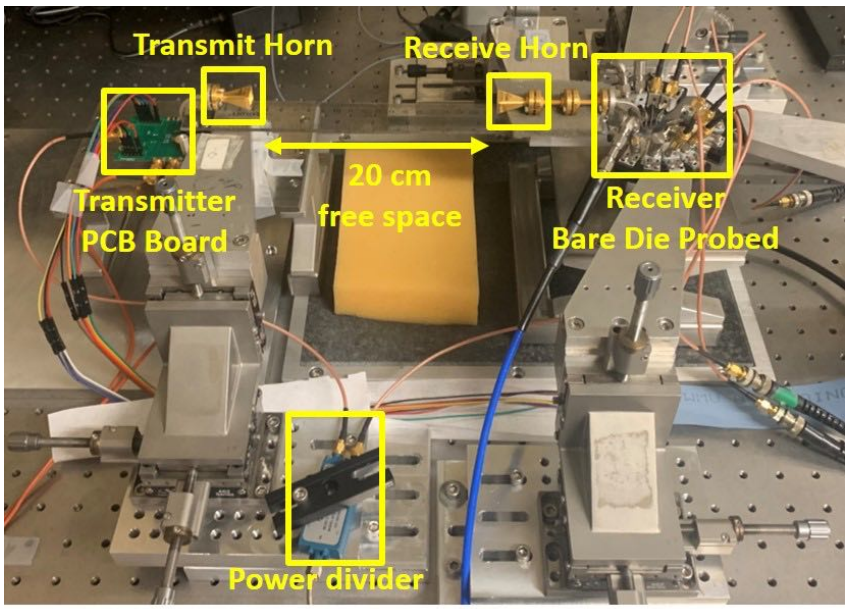

Figure 5.23: Image of the experimental setup for transceiver wireless data transmission experiment with horn antennas (20 cm link)

waveform happens at 2 GHz and 4 GHz respectively. Tone spacing of 15.8 MHz and 31.4 MHz matches with the expected value, given by $\text{data rate} / (2^7 - 1)$. Fig. 5.21 similarly shows the results for 6.4 and 8 GBaud, where first nulls at the sinc waveform happens at 6.4 GHz and 8 GHz. Tone spacing of 50.4 MHz and 63.2 MHz also matches with the expected values. However, as can be seen in the figures sinc waveforms are getting distorted with the higher data rates.

Finally, transmitter and receiver are placed 20 cm apart and both are wafer probed through GGB waveguide probes and connected to the WR-5 standard gain horn antennas

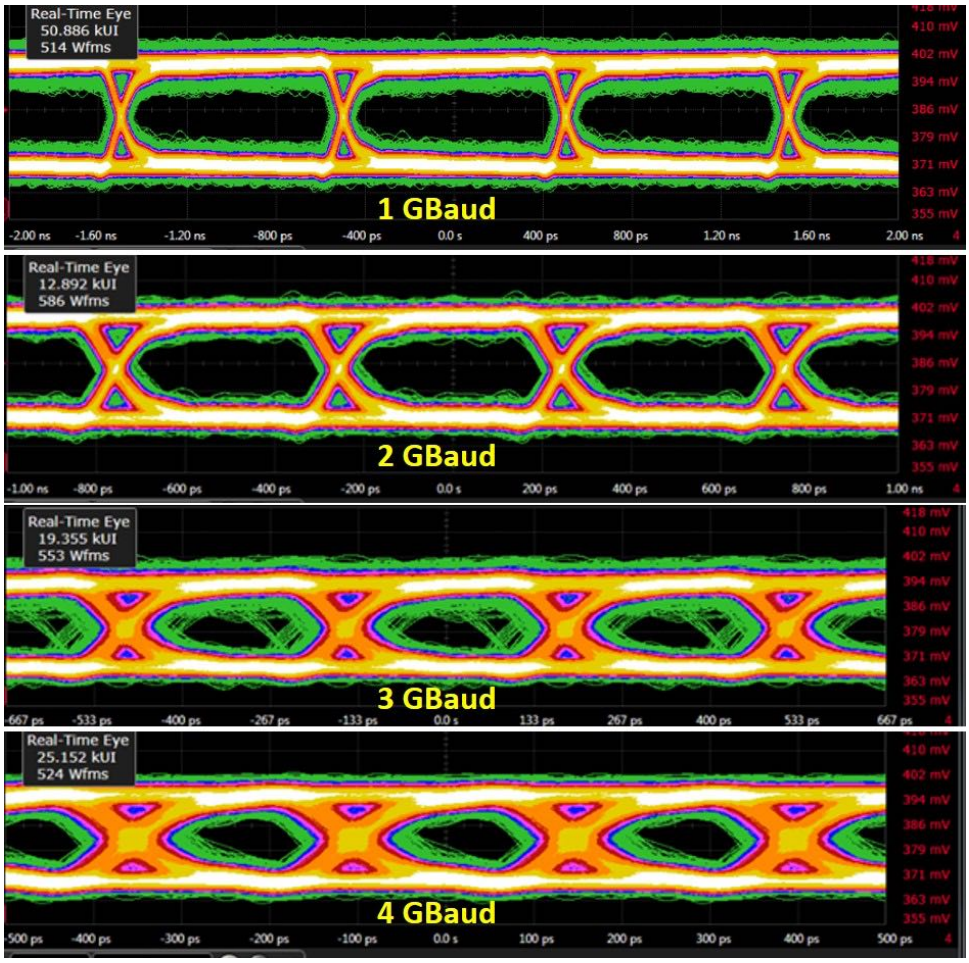

Figure 5.24: Eye diagrams at the receiver I channel for 1, 2, 3, and 4 GBaud BPSK wireless data transmission experiment

at their RF ports. We sent PRBS data sequence to I/Q channels of the transmitter, and we observed receiver I/Q baseband signals using DSAV134A digital oscilloscope from Keysight. Schematic and the image of the experimental setup can be seen in Fig. 5.22 and Fig. 5.23 respectively. In this data transmission experiment we used 145.8 GHz as the carrier frequency by applying 16.2 GHz external LO signal.

In this particular experiment, same data stream to I/Q channels are applied and I or Q channel of the transmitter is observed in the oscilloscope. Only I data is reported here. Open and clear eye patterns up to 8 GBaud data rate is demonstrated in this data

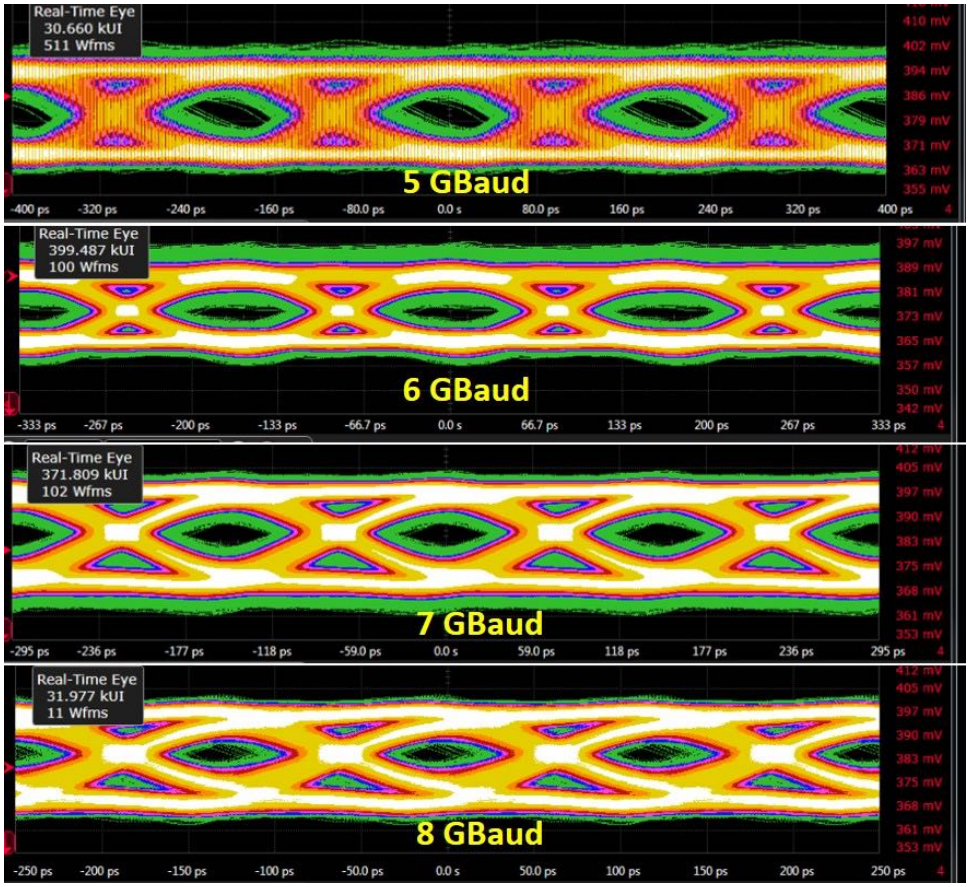

Figure 5.25: Eye diagrams at the receiver I channel for 5, 6, 7, and 8 GBaud BPSK wireless data transmission experiment

transmission experiment (Fig. 5.24 and 5.25). Since we didn't place any amplifiers after baseband I/Q data, output voltage swing is roughly 30-40 mV.

5.6 Conclusion

In this chapter we provided the design and measurements of the 140 GHz MIMO transceivers and building blocks. First the design and measurement results of the building blocks including amplifier, multiplier, mixers and baseband transimpedance amplifier were provided. Then, one channel gain-frequency measurements of the transmitter and receiver were presented for the fixed IF and fixed LO cases. In order to evaluate the

system, we further measured the system impairments in the receiver and transmitter channels by means of receiver noise figure and transmitter LO suppression and I/Q imbalance.

These chips showed 20 GHz of RF bandwidth with 30 dB receive conversion gain and 4.5 dBm transmit output power in simulations. However, measured performances were degraded possibly due the the multiplier performance degradation and the consequent LO drive power reduction of the passive down-conversion mixer. In measurements, receiver demonstrates 18 dB gain with $\sim$ 10 GHz 3-dB IF bandwidth. When IF is fixed, gain curve showed a notch which may possibly further prevents these chips to support higher than 5-6 GBaud data rates. Transmitter output power is -2 dBm with 1 V power supply, 1 dBm with 1.1 V and 3.5 dBm with 1.2 V supply. 4-channel receiver and transmitter consumes 495 mW and 463 mW of power from 1 V power supply respectively. In wireless data transmission experiments over 20 cm air, we observed clean and open eye patterns up to 8 GBaud with BPSK modulation.

After all of the successful transceiver measurements, off-chip antenna arrays are developed to integrate with these ICs. Our goal is to realize single and multi-beam phased array ICs using these transceivers. In the next chapter, we will explain the design of antenna arrays and IC-antenna transitions in detail. Fully packaged transmitter and fully packaged receiver phased arrays using off-chip antennas are going to be presented in the final chapter using these ICs.

Chapter 6

Antenna and Transition Designs at D-Band

6.1 Introduction

With the developments in low-cost CMOS technologies, now it is possible to realize low cost transceivers operating above 100 GHz. Two such examples are presented in Chapter-4 and Chapter-5 of this dissertation. However, there is still a need for low-cost, yet efficient antennas and low-cost assembly techniques at these frequencies. Many previous published mm-Wave systems have used either on-chip antennas [94, 95, 96] with limited gain and efficiency, or wafer probing [91, 97] to demonstrate data transmission. Importantly, recent work demonstrated low-loss Cu-stud flip-chip IC-antenna interconnection above 100 GHz [98]. Such assembly provides low IC-package interconnect losses, but requires tighter lithographic resolution in the package design. In addition, it is a costly integration for low volume applications. Lower cost C4 bump technology has only been demonstrated for the applications with frequencies lower than 100 GHz [99, 100].

In this chapter, we present low-cost and efficient antenna array designs using printed

circuit board (PCB) technology with Isola Astra MT77 material. These antennas will be integrated with the previously designed 45 nm CMOS SOI transceiver ICs reported in the previous chapter. These antenna arrays are intended to create phased arrays that can support single and multi-beam operation. From the system perspective, the ease and cost of the package design, we decided to implement series-fed patch arrays. Although, slot antenna arrays, and Vivaldi antennas can provide broader bandwidth, it is harder to integrate them in a system. Hence, in this study we designed series-fed patch antenna arrays, which can be integrated with the transceiver ICs at low-cost packaging techniques. Single row of the 8-element series-fed patch array test structure is measured and compared with the simulations. It shows 14 dB gain, 9° E-plane and 65° H-plane 3-dB beam-widths, and 7 GHz bandwidth (S_{21}), close to simulation. Subsequently, we propose a low-cost transition design from the transceiver ICs to antenna arrays with over 10 GHz 3-dB bandwidth and less than 2 dB loss using a wirebonding interface.

Finally, we conclude this chapter by proposing a future generation, more efficient packaging design, which can easily be tiled to create arrays with a massive number of elements. In addition, III-V based power amplifiers with higher output power can be integrated into the package to increase the system range. This generation proposes to use Cu-stud flip-chip interface between the CMOS ICs and the carrier, providing better and more robust transition performance than wirebonding.

6.2 Package Design, Antenna and Transition Options

In this chapter, we designed and measured antenna arrays to integrate with the 140 GHz MIMO transceivers reported in the previous chapter. At frequencies above 100 GHz, flip-chip integration is the desired method, but 45 nm MIMO transceiver ICs were initially designed for on-wafer measurement. Therefore, IC pads are small in dimensions and

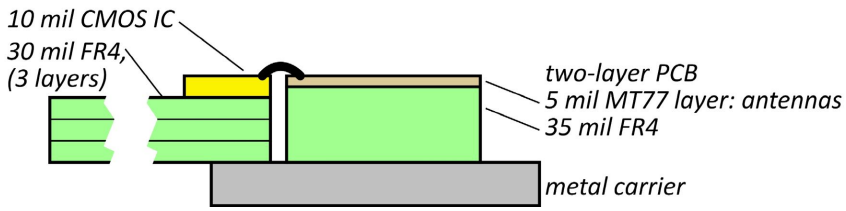

Figure 6.1: Design of the proposed package with separate antenna and CMOS carrier PCB with height alignment.

pitch, which prevents them to be flip-chip integrated either using C4 bumps or Cu-pillar. Therefore, only option remaining was wirebonding. In order to design a wirebonding interface at 140 GHz, the chip to antenna spacing and the height difference should be minimized and well-controlled . Wirebond lengths longer than 0.3-0.4 mm gives larger than 300 pH inductance, which prevents to have low loss, broadband interface. Hence, cavity based PCBs are the ways to realize wirebond interfaces at these frequencies. In this study we propose a low-cost packaging technique, which satisfies the length requirement similar to the cavity based PCB, but uses two separate PCBs one for the antenna design and the other for the CMOS carrier. These two PCB heights are adjusted within $\pm 50\,\mu$m (Fig. 6.1). In summary, for the transition, only viable solution was wirebonding using the existing transceivers, therefore we pursued this path to realize phased array transceivers. In order to achieve a good performance, we minimized the transition length and implemented a compensation network to absorb the inductance effect.

For the type of the antenna array, initial thoughts suggested three different options including the series-fed patch antenna arrays, series-fed slot antenna arrays and Vivaldi antenna arrays (Fig. 6.2). However, slot antenna arrays needs additional planes in the PCB for integration. In addition, they radiate towards the opposite side of the feeding plane, which makes the overall interface and the system design challenging. Vivaldi arrays are generally bigger and spaced more than $\lambda/2$ distance between antenna elements. This creates additional grating lobes and limit the steering range. They are good for the point

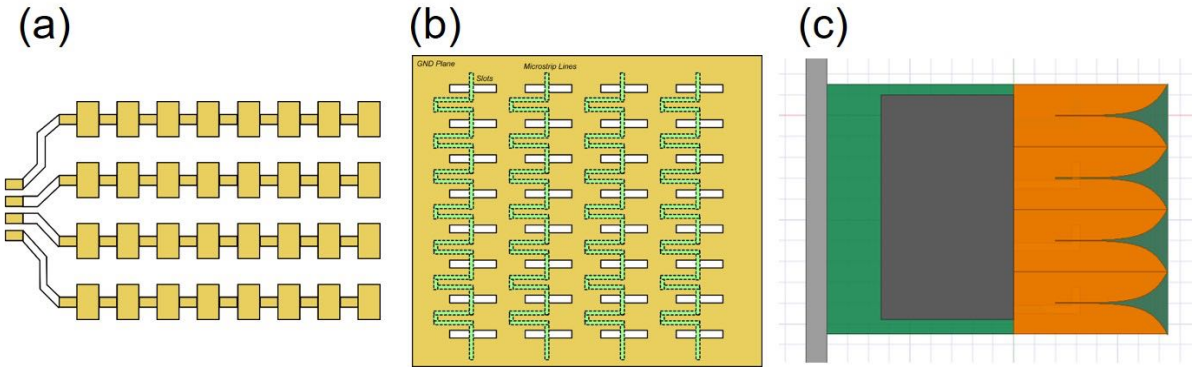

Figure 6.2: Proposed antenna options for the final package (a) series-fed patch array (b) series-fed slot array (c) Vivaldi array

to point MIMO applications, but not for the MIMO hub applications. On the other hand, series-fed patch antenna arrays are much easier to integrate in a system with well defined signal-ground paths and the radiation planes. They are low-cost and efficient designs. However, one major problem of them is their limited bandwidth due to the traveling wave structure and the frequency dependent phase characteristic. Since this is the first proof of concept design and we only expect to transmit 1-5 Gb/s data per channel, we decided to implement the series-fed patch arrays.

6.3 Antenna Designs and Measurements at D-Band

6.3.1 Design of a Series-Fed Patch Array

Series-fed patch arrays are well-known structures for a long time, hence the design and analysis methods are well-established. Detailed design procedures can be found in [101, 102]. The most critical part of the design of a series-fed array is the phase alignment of the patches along the array. The length of the individual patch is designed as $\lambda/2$, as well as the transmission line between the consecutive patches. This way the length difference between patch wavefronts are $\sim \lambda$, which gives 0° phase difference. The width

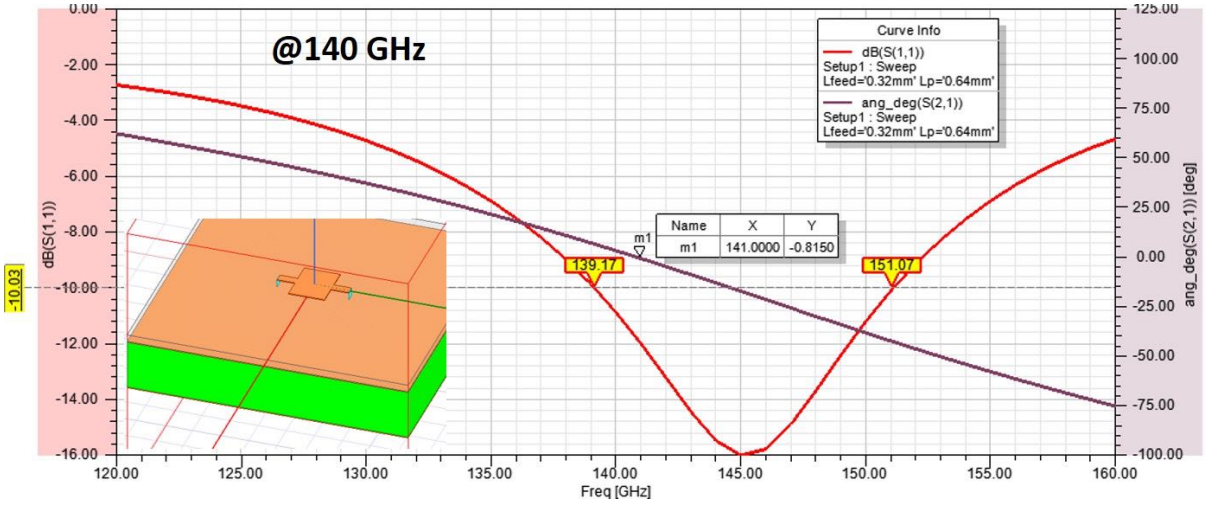

Figure 6.3: Unit cell design in HFSS. Figure shows the phase of S_{21} and amplitude of the return loss (S_{11}) of the unit cell given in the inset.

of the patches along the array can be arranged for impedance matching, and further tuning of the single patch resonant frequency. Therefore, the design starts with the single patch, preferably with two feeds from both sides having half of the total feed length ($\sim \lambda/4$) [103]. Two ports are defined at both ends, and length and width of the patch and the length of the feed line are adjusted to have 0° phase difference between the feed points. In addition, port impedances are arranged to have $\sim 50\,\Omega$ impedance at the design frequency (Fig. 6.3). All designs are performed using 3D electromagnetic simulation tool HFSS from Ansys.

After the unit cell design, this unit cell is copied multiple times and connected to build the series-fed array. Then, impedance of the input port is measured, it deviates from the 50 Ω due to the non 50 Ω termination at the end of the patch array. Additional quarter wavelength transformer with a proper impedance is used in the input to match 50 Ω impedance. All antennas are designed on 5 mil substrate using low-cost, high performance material Isola Astra MT77. This material has an $\epsilon_r = 3$, and $tan\delta = 0.0017$. Antenna PCB also uses additional 35 mil FR4 under the main antenna substrate of 5 mil Isola Astra MT77 in order to match the heights of the antennas and transceivers for

the wirebonding interface (Fig. 6.1).

6.3.2 Single Patches at 130, 140 and 148 GHz

Using the principles explained in the previous sub-section, we designed single patch test structures covering 130, 140, 148 GHz, and single row 8-element series-fed patch array test structures covering 136, 140, 144, and 148 GHz. Moreover, wirebonding and line loss characterization test cells, and 4-channel 8-element series-fed patch arrays with wirebonding transitions at 136, 140, 144, and 148 GHz were placed in the same design cycle. Fig. 6.4 (a) and (b) shows the fabricated test structures and one of the 4-channel antenna array designs including the transition (144 GHz MIMO board).

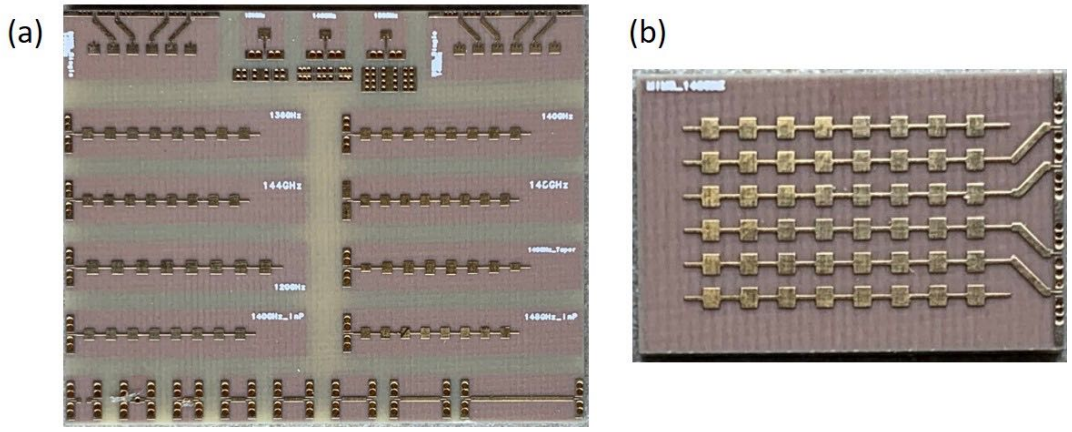

Figure 6.4: fabricated PCBs including (a) antenna test cells and thru-reflect-line calibration standards (b) MIMO board including the antenna array and transition at 144 GHz.

We characterized the single patch and single row 8-element series-fed patch test structures using the antenna measurement setup in Fig. 6.5. Setup is simple, but sufficient at mm-Wave and sub-mm-Wave frequencies since the wavelength is really short. Therefore, 15-20 cm from the test antenna is enough for the far field. In addition, no expensive absorbers are used, since there are no strong reflections within the setup due to short wavelengths.

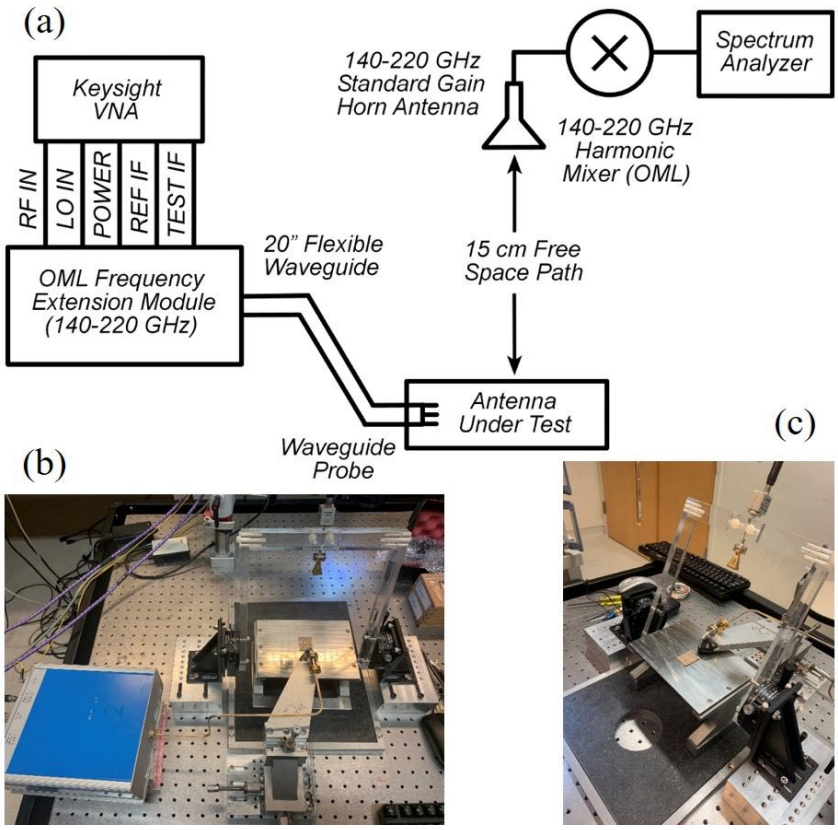

Figure 6.5: (a) schematic diagram (b)(c) images of the antenna measurement setup.

We tested single patches first in order to see how much shift in the resonant frequency happened in the designs. 130, 140 and 148 GHz single patch test structures are measured using the setup shown in Fig. 6.5. Fig. 6.6 shows the simulated vs. measured return losses for 3-different single patch test structures. Each curve shows three different measurement results, where each one represents different landing points at the input ports. Each probe landing space gives slightly different results. As can be seen in Fig. 6.6, there is $\sim 3-7$ GHz of frequency shift in the antenna resonant frequency depending on the landing point.

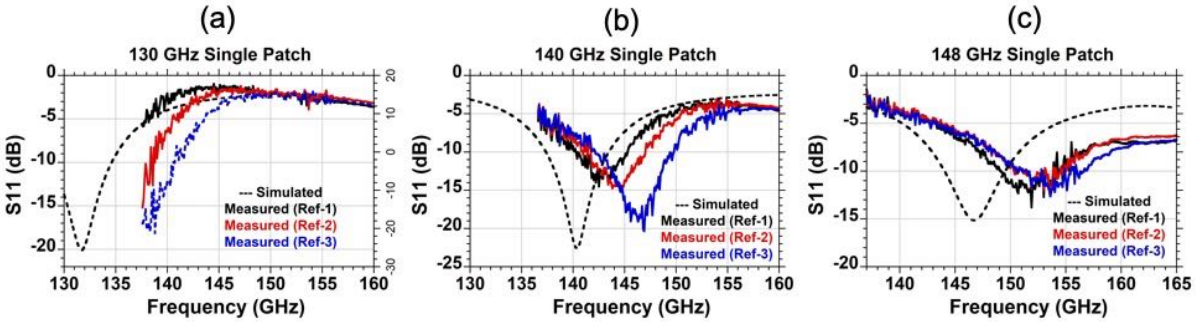

Figure 6.6: Simulated and measured return losses of single patch test structures at (a) 130 GHz (b) 140 GHz (c) 148 GHz

6.3.3 8-element Series-Fed Patch Arrays

Single row test structures for 8-element series-fed patch antenna arrays are designed and characterized, similarly using the design principles outlined in the beginning of the chapter. Overall PCB includes 136, 140, 144, and 148 GHz test structures, but 148 GHz test cell has missing ground vias due to the fabrication. Therefore, here we present the simulated vs. measured characteristics of the test structures designed for 136, 140 and 144 GHz. Fig. 6.7 shows the gain vs. frequency behavior of the 136 GHz test cell, where antenna resonant frequency is shifted $\sim$ 4 GHz. Fig. 6.8 shows the measured vs. simulated electric (E) and magnetic (H) field radiation patterns of the antenna. E-plane 3-dB beamwidth is about 9°, whereas H-plane 3-dB beamwidth is about 65°. Both are close to the simulations.

Fig. 6.9 shows the return loss simulation and measurement results of the 140 GHz series-fed path array test structure. Antenna resonant frequency is again shifted $\sim$ 4 GHz. This is also true for the gain vs. frequency behavior (Fig. 6.10). Measured gain is about 13.5-14 dB, close to simulations. Due to the frequency shift, radiation pattern is measured at 4 GHz above the simulated frequency. Fig. 6.11 shows the simulated vs. measured E and H field radiation patterns. Similarly, this antenna also shows $\sim$ 9° E-plane and $\sim$ 65° H-plane 3-dB beamwidths.

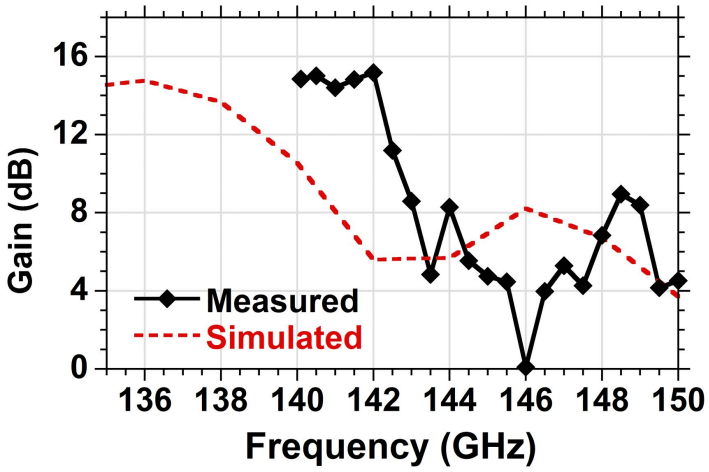

Figure 6.7: Simulated and measured gain vs. frequency curve of the 136 GHz series-fed patch array test structure.

We performed the same measurements for the 144 GHz test structure. Fig. 6.12 shows the return loss simulation and measurement results of the 144 GHz series-fed array. Similar $\sim$ 4 GHz antenna resonant frequency shift can be observed again. Gain vs. frequency curve also shifted $\sim$ 4 GHz (Fig. 6.13). Measured gain is about 13.5-14 dB. Measurements are again 1-2 dB lower than the simulations, which is likely caused by the inaccuracy in the surface roughness modeling in HFSS. Due to the frequency shift, radiation pattern is measured at 4 GHz above the simulated frequency. Fig. 6.14 shows the simulated vs. measured E and H field radiation patterns. This antenna also shows $\sim 9^\circ$ E-plane and $\sim 65^\circ$ H-plane 3-dB beamwidths.

In this section, we summarized the series-fed antenna array designs using electromagnetic simulator tools, then we provided the simulation and measurement results for single patch and series-fed patch antenna arrays designed for different frequencies. Since the precision of the PCB technology is not perfect (there may be $\pm 10\%$ under or over-etching), frequency can shift easily about 5-10 GHz. Therefore, we placed different frequency ranges as the test structures, and evaluated each of them. These antennas are designed using commercial low-cost PCB technology using Isola Astra MT77, which is

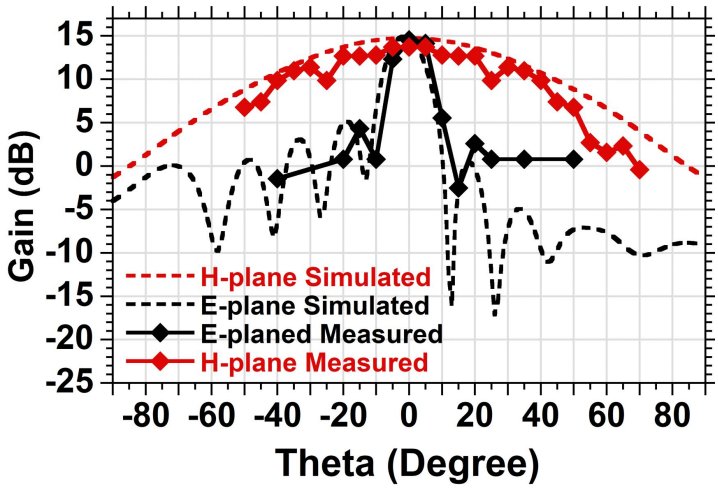

Figure 6.8: Simulated and measured E & H field radiation patterns of the 136 GHz series-fed patch array test structure. (Simulation at 136 GHz, measurement at 140 GHz)

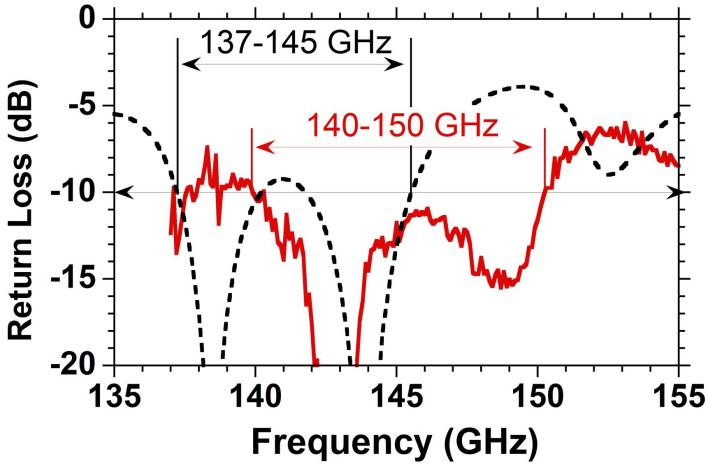

Figure 6.9: Simulated and measured return loss of the 140 GHz series-fed patch array test structure.

a new material. This material is created as an alternative for Rogers 4350, or 3003. In summary, we developed low-cost, yet efficient antenna arrays working above 140 GHz, which can be used to create scalable single or multi-beam phased arrays.

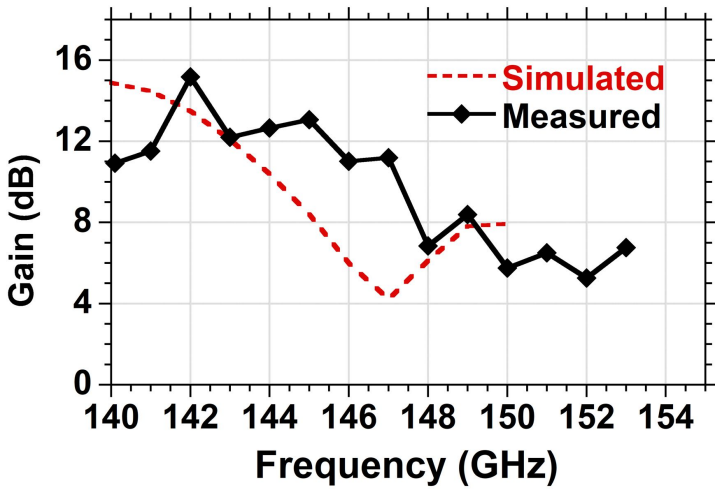

Figure 6.10: Simulated and measured gain vs. frequency curve of the 140 GHz series-fed patch array test structure.

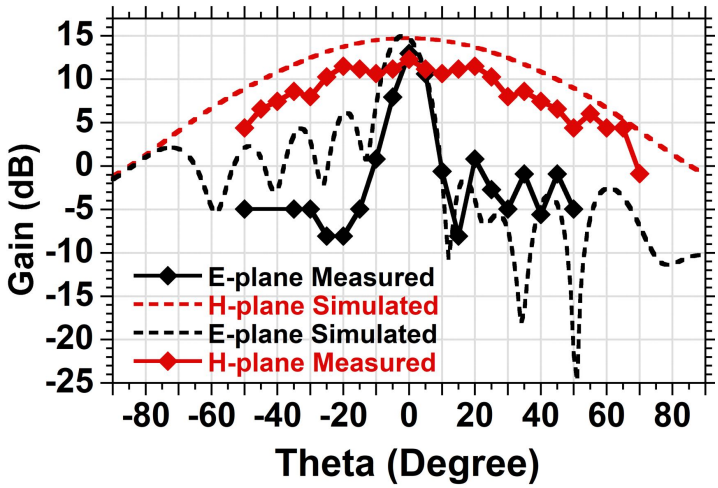

Figure 6.11: Simulated and measured E & H field radiation patterns of the 140 GHz series-fed patch array test structure. (Simulation at 140 GHz, measurement at 144 GHz)

6.4 Chip to Antenna Interface Design at 140 GHz

One of the main challenges at frequencies above 100 GHz is the interface between the chips and the antennas. IC technology has developed a lot recently, and it is now possible to build transceivers working above 100 GHz at low-cost and high yield. However,

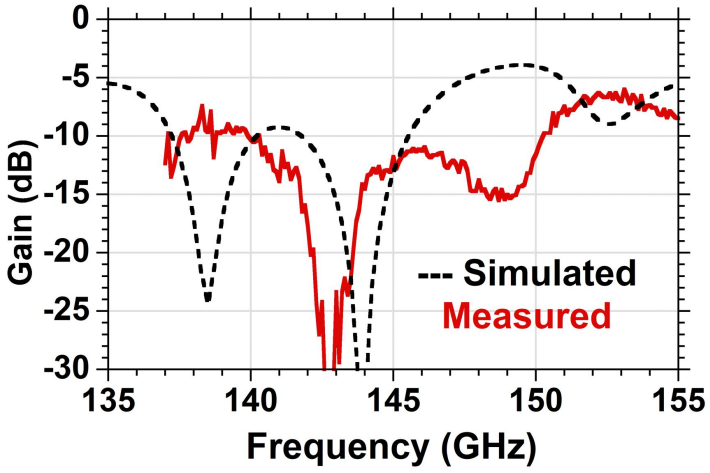

Figure 6.12: Simulated and measured return loss of the 144 GHz series-fed patch array test structure.

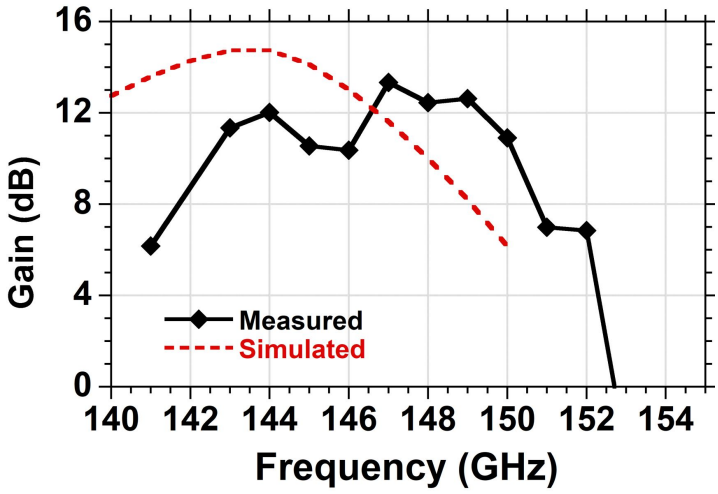

Figure 6.13: Simulated and measured gain vs. frequency curve of the 144 GHz series-fed patch array test structure.

antenna design and chip-antenna interfaces make system realization at these frequencies challenging. Therefore, many previous works either uses on-chip antennas or wafer probing for proof of concept demonstrations [91, 94, 95, 96, 97]. On-chip antennas have poor efficiency, and this leads to inefficient systems, even if the transceivers are really high performance. In this work, we propose a simple, low-cost, and moderate-performance transition designs through wirebonding from transceiver ground-signal-ground (GSG)

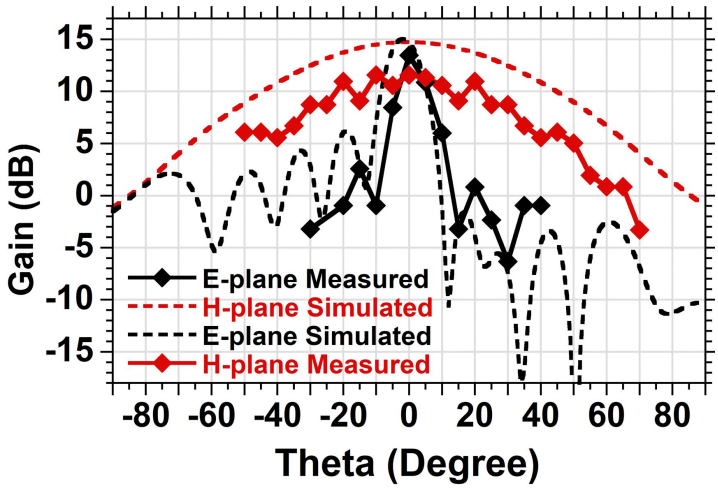

Figure 6.14: Simulated and measured E & H field radiation patterns of the 144 GHz series-fed patch array test structure. (Simulation at 144 GHz, measurement at 148 GHz)

pads to the microstrip transmission line. Then, this microstrip feeds the off-chip, high-efficient antennas explained in the previous section.

The wirebond transitions between the antenna and the 140 GHz CMOS transceiver RF input/outputs (I/Os) are designed using Ansys HFSS (Fig. 6.15). As noted, board thicknesses are selected such that the height of the antenna and the CMOS pads are aligned within $\pm 50\,\mu$m accuracy (Fig. 6.1). In assembly, the gap between the CMOS carrier PCB and the antenna PCB distance is kept below $50\,\mu$m (Fig. 6.16). This provides less than 0.3 mm wirebond length, giving less than 250-300 pH inductance.

The CMOS IC signal pads are ground-signal-ground, hence the antenna PCB substrate provides vias connecting the microstrip ground plane to ground pads, which are bonded to the CMOS IC ground pads (Fig. 6.15). The vias add additional series inductance. The IC-PCB transition (Fig. 6.15 (a)) contains a 430 μm length high-impedance ($\sim 90\,\Omega$) grounded coplanar waveguide (GCPW) transmission line as a series tuning element. The fringing capacitance between the end of the wider $50\,\Omega$ microstrip line and the CPW ground plane provides shunt tuning. The transition, designed in Ansys HFSS

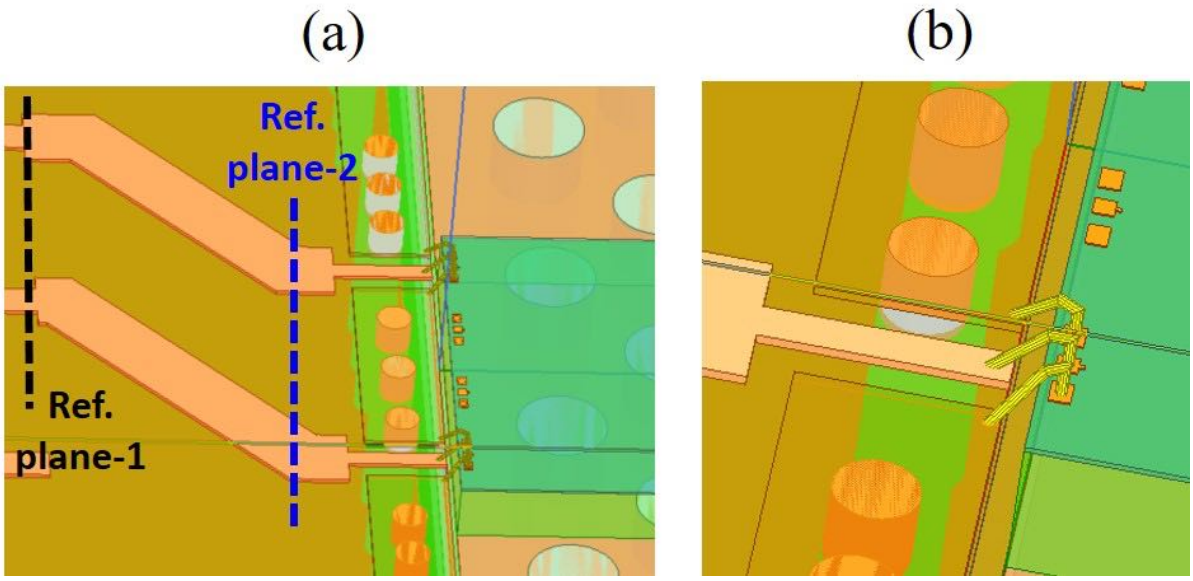

Figure 6.15: (a) HFSS simulation setup image (b) closer look at the wirebonding transition in HFSS

(Fig. 6.15), shows 1.8 dB loss at 140 GHz for the transition up to reference plane-2, and 2.5 dB up to reference plane-1 in Fig. 6.15 (a). Additional 0.7 dB simulated loss comes from the 50 Ω microstrip line between the IC-PCB transition and the antenna feed point. There is a small gain notch at 145-146 GHz, which is likely due to the ground return path and the minimum allowed via size in PCB fabrication. Using better resolution process with smaller vias, this problem can be solved. Isolation between adjacent antenna ports is better than 20 dB over most of the frequency band of interest. Fig. 6.17 shows the simulated S-parameters of the wirebond transition.

In this section, we designed a low-cost transition between ICs and antennas working above 140 GHz using wirebonding. The approach could be extended and utilized to realize arrays with a massive number of elements, ICs and antennas. However, wirebonding is not an easily reproducible method, and depends on outside factors. Thus it can create huge variation of performance in the actual implementation. Therefore, for more robust arrays and systems, more advanced flip-chip technologies including C4 bumps,

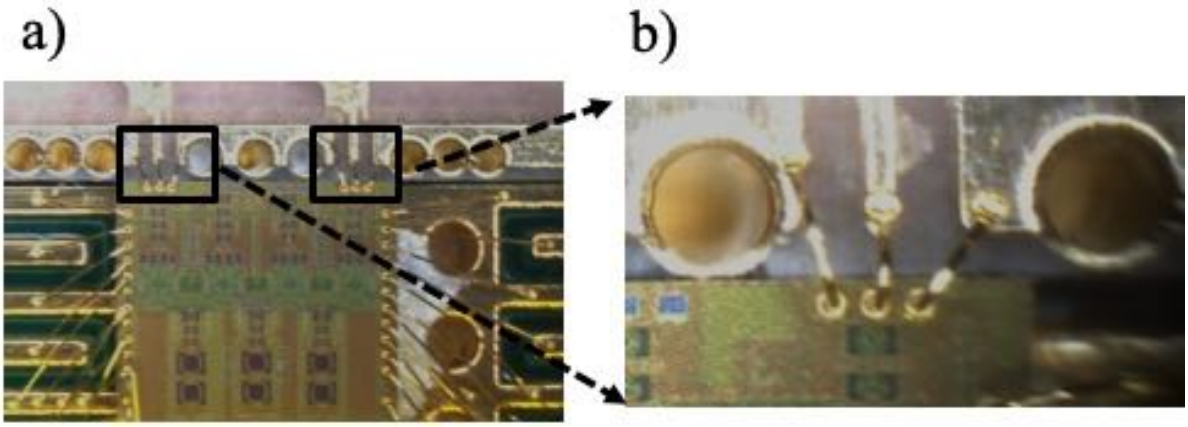

Figure 6.16: (a) Zoomed image showing the ICs and wire-bond interface. (b) Magnified image showing the wire-bonds

and Cu-stud bonds are preferable. Nevertheless, we proposed and designed a low-cost transition with simulated loss of 1.8 dB through wirebonding. Simulation results are experimentally validated in the 4-channel receive and 2-channel transmit array reported in the next chapter, and shows close performance with the measurements. Therefore, if we can maintain the repeatability of the wirebonding connections, this solution can be used in larger arrays at low-cost.

6.5 Future Generation Package Designs

Although wirebonding interface reported previously perform well with low-cost, it is not a well controlled and easily reproducible process. In addition, integration gets more complicated in a larger system. Therefore, we also propose and provide initial simulation results of a future generation packages. This package can easily be tiled in a larger array to realize MIMO array with a massive number of elements. This module can also accommodate III-V based power amplifiers or low noise amplifiers to further increase the system dynamic range.

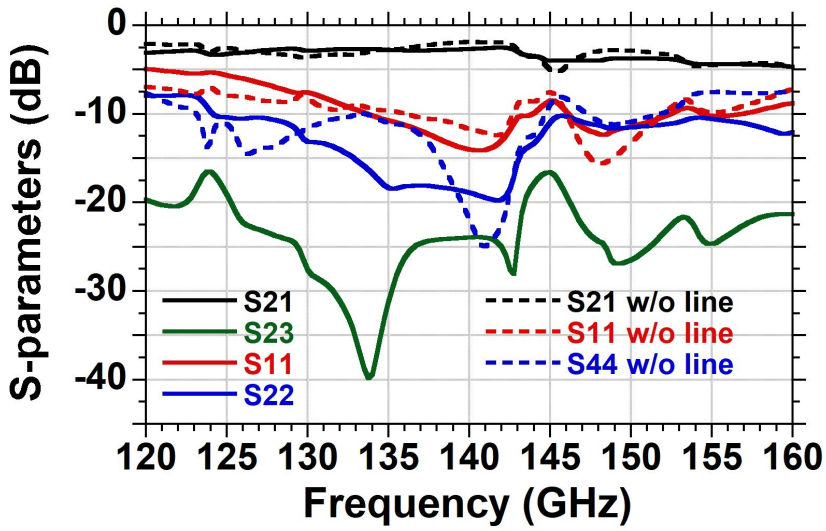

Figure 6.17: Simulated S-parameters of the transition including the feed line and without the feed line. Plot shows loss and return losses for both cases, and the isolation between 2 consequtive channels.

In this module (Fig. 6.18) Silicon beamformer ICs are flipped on to the low-temperature co-fired ceramic (LTCC) carrier via Cu-stud bumps. III-V amplifiers are placed in the cavity of 3 mil (same height with the chips). They are integrated with the LTCC carrier and antennas via wirebonding. Here we performed preliminary simulations for the flip-chip interface performance, wirebonding performance from amplifiers to antenna, and the series-fed patch antenna array performance on the LTCC material. LTCC material has $\epsilon_r = 5.2$ and $tan\delta = 0.0034$. Therefore, antenna performance is poorer in the LTCC material compared to the previously reported antennas. Fig. 6.19 demonstrates the design and performance of the Cu-stud interface. This transition has $\sim$ 1.5 dB loss, with $\sim$ 20 GHz -10 dB return loss bandwidth.

Second interface is between LTCC carrier and III-V amplifiers using wirebonding. Preliminary transition design using InP power amplifiers designed by Ahmed. S. H. Ahmed shows $\sim$ 0.5 dB insertion loss, with $\sim$ 30 GHz -10 dB return loss bandwidth (Fig. 6.20).

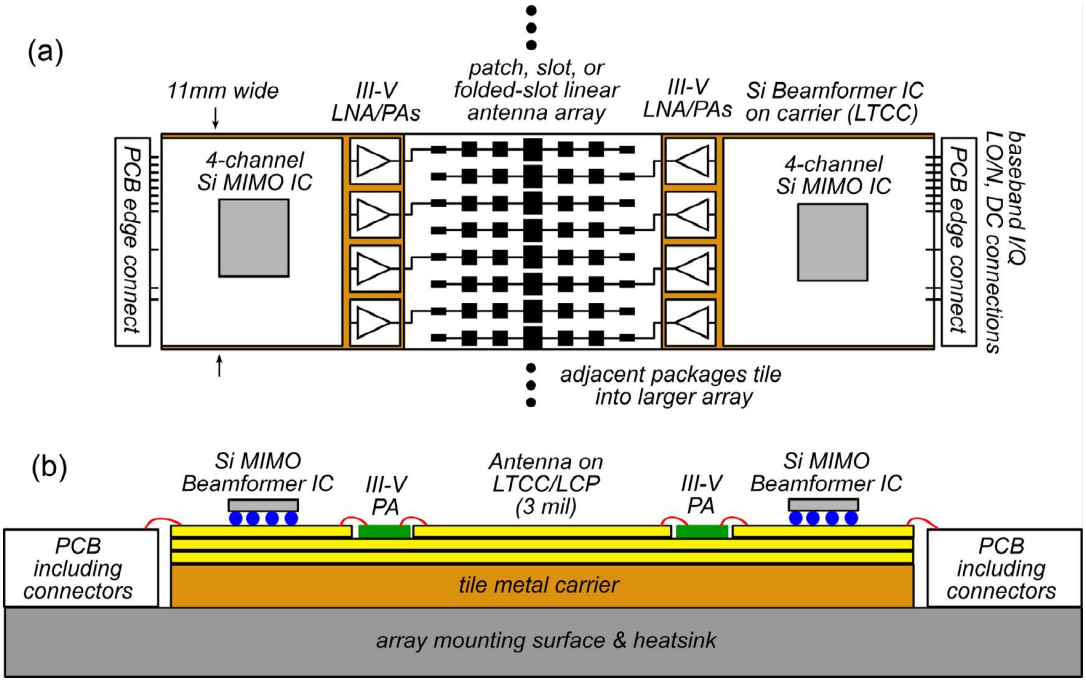

Figure 6.18: (a) Proposed next generation 8-element module, which can be tiled for the larger array realization. (b) LTCC carrier with 3 layers are to be used with thermal vias and cavity for the III-V power amplifiers.

Initial antenna simulations show that the efficiency of the single row 8-element series-fed patch array is roughly 68-72%, which is poorer than the antennas reported previously on Isola Astra MT77. The main reason is the high relative permittivity of the LTCC material, which creates more substrate modes and loss. Return loss bandwidth is about 7 GHz, again it is low since the structure is a traveling wave structure. Fig. 6.21 shows the simulation results of a single-row 8-element LTCC series-fed patch antenna array.

Here we proposed a module design for an 8 element array, which can accommodate high performance III-V amplifiers. This module can be tiled easily to realize arrays with a massive number of elements. The main application is base-stations. We can connect 32 modules via tiling to realize 256 elements array. This array can communicate with 128 users with 2:1 load factor. If we can support 1-10 Gb/s data rate per user, the total base-station can support 512 Gb/s to 5 Tb/s data rate. This can revolutionize the current

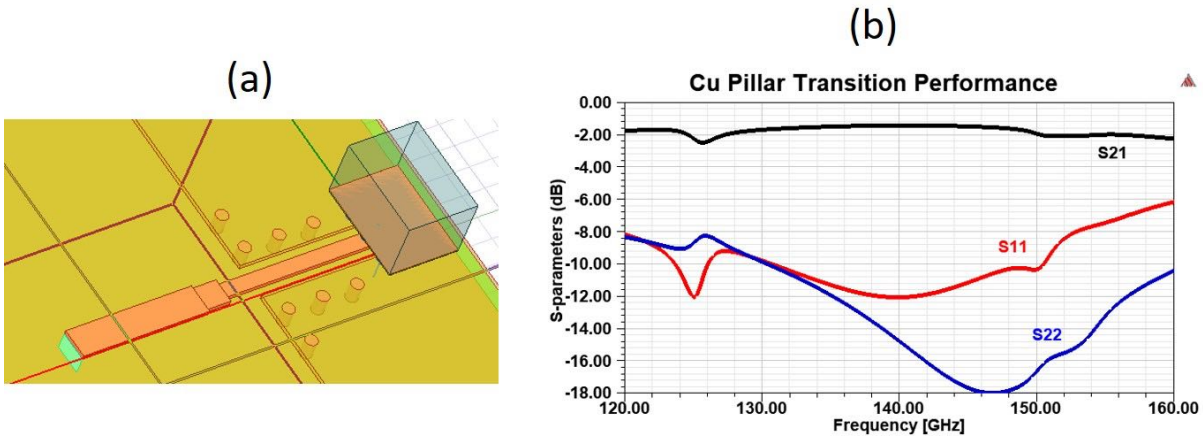

Figure 6.19: (a) Cu-stud flip-chip interface design in HFSS (b) simulated transition performance in HFSS

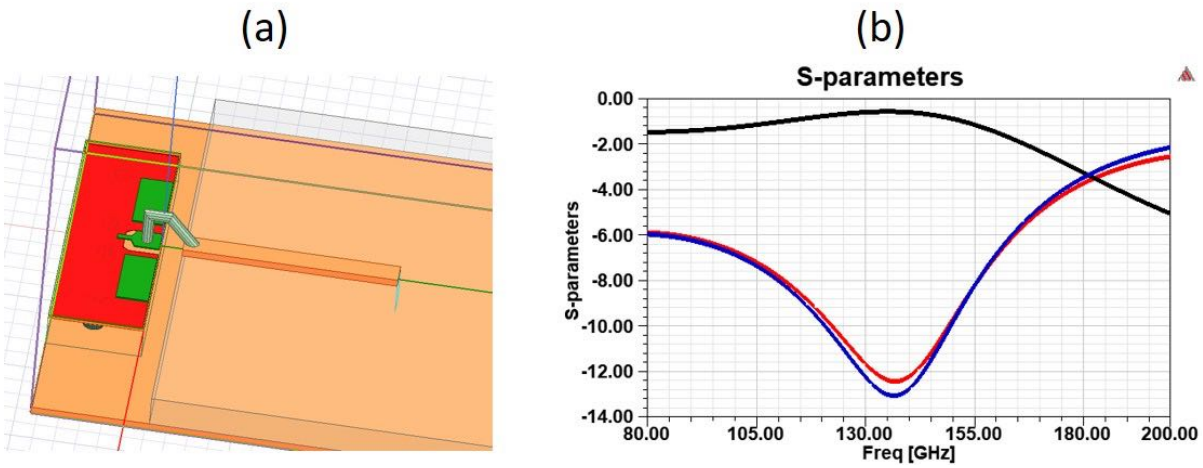

Figure 6.20: (a) InP-antenna interface design in HFSS (b) simulated transition performance in HFSS

communication systems and we can have wireless communications at fiber speeds.

6.6 Conclusion

In this chapter, we presented low-cost, yet efficient series-fed patch antenna arrays and wirebond transition designs. These will be utilized to build phased arrays using the 45 nm CMOS SOI transceivers. Although, the wirebonding interface has problem

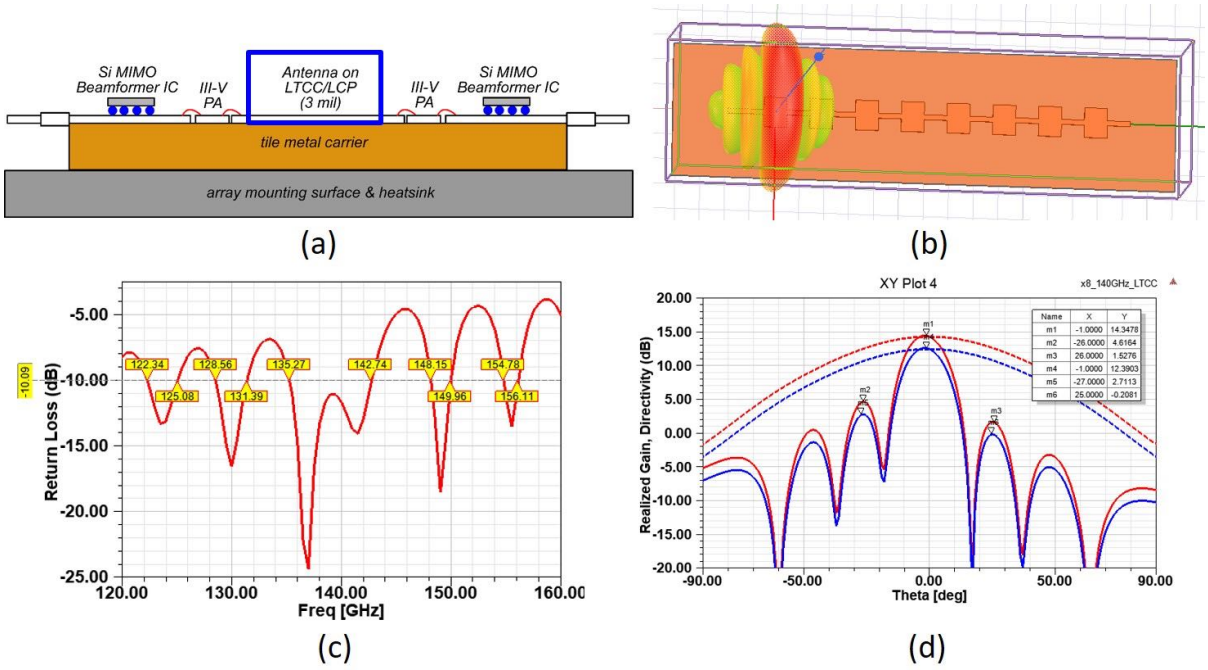

Figure 6.21: (a) System side view (b) single row 8-element series fed patch in HFSS together with the radiation pattern in 3D view (c) Simulated return loss (d) Simulated gain and directivity of the 8-element series-fed patch array in HFSS

of repeatability, with a careful assembly techniques it can give a really low loss. In addition, it has significantly lower cost then flip-chip technologies. Antennas designed here are off-chip antennas. They use high performance, low relative permittivity material. Therefore, they are efficient. Simulation and measurement results of the antenna test structures are closed, except the $\sim$ 4 GHz shift in the antenna resonant frequency. They show $\sim$ 14 dB gain, $\sim$ 7 GHz 3-dB gain bandwidth with $\sim$ 9° E-plane and $\sim$ 65° H-plane 3-dB beamwidths. The wirebonding transition shows 1.8 dB insertion loss and 10 GHz bandwidth. The wirebonding transition loss is not experimentally validated, but phased array modules in the next chapter proves that the transition loss is close to the simulations within the experimental errors.

Finally, we proposed a next generation packaging strategy, where 8-element module was presented using LTCC carrier. In this module, Si beamformer ICs are flip-chip

integrated using Cu-studs. III-V amplifiers are placed inside a 3 mil cavity and wire-bonded to the antenna and the LTCC carrier. This module can be tiled to realize arrays with a large number of elements to be used in the 140 GHz base-stations. LTCC based antennas are poorer in terms of efficiency due to the higher permittivity material. The flip-chip interface shows better transition losses than the wirebonding transition. In addition, it is easily reproducible. These modules can create arrays with 1000s of elements, and data rates can approach to 10s of Tb/s. This can be the next revolution in wireless communications.

Chapter 7

Fully Packaged Phased Array Transceivers at 140 GHz

7.1 Background and Motivation

Single beam phased array transceivers have already been reported up to 100 GHz previously [104, 105, 106]. In addition, there are previously reported one channel transceivers working up to 260 GHz frequencies [25, 27, 107], even up to 630 GHz using III-V technologies [83]. However, there is still need to build phased array ICs working above 100 GHz using low-cost techniques to support both single and multi-beam communications. At these frequencies ICs and antennas are small, and we can fit a massive number of elements into a small form factor. However, one of the main challenges at these frequencies is the design of antennas and high frequency interconnects. On-chip antennas have poor efficiency and they use too much silicon area, which is costly. On the other hand, low-loss interface design between ICs and off-chip antennas at these frequencies are challenging. If we can provide solutions to these problems, we can build arrays with a large number of antennas at low-cost and high-efficiency.

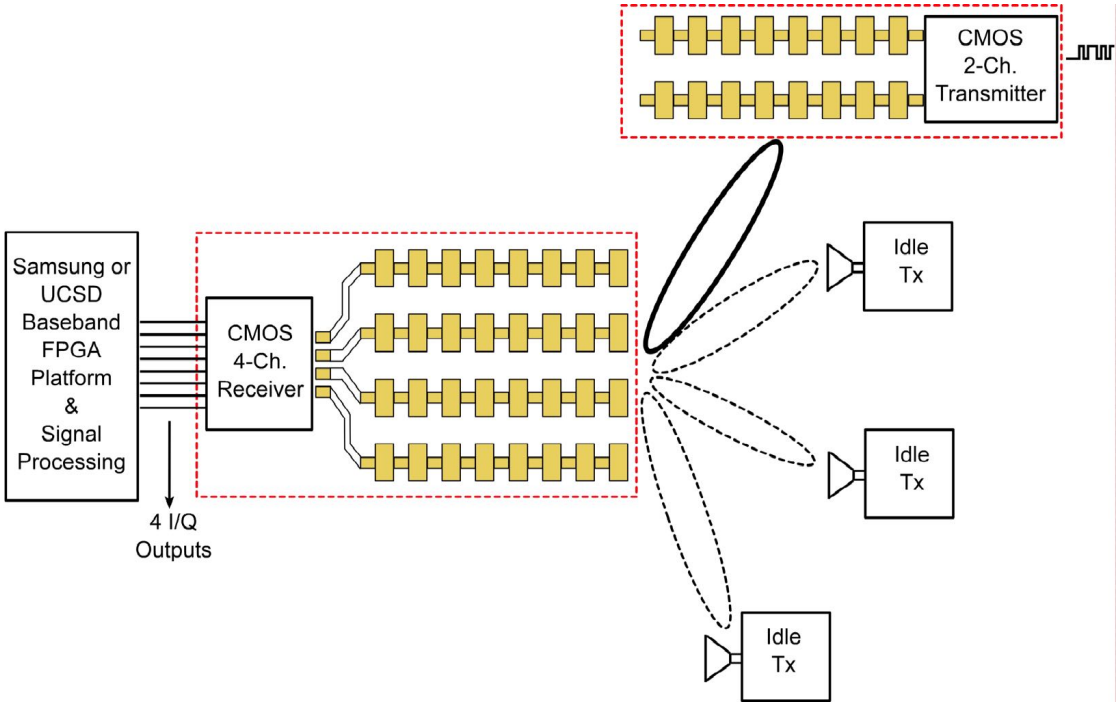

Figure 7.1: Multi-beam wireless communications experiment setup

In this chapter, we designed and experimentally validated 4-channel receiver and 2-channel transmitter using low-cost packaging techniques. These modules are first reported phased arrays working above 140 GHz to the best of author's knowledge. Antenna and interconnect designs are presented in the previous chapter. Using those designs, we realized the phased array transceivers working above 140 GHz at low-cost. These modules can support both single and multi-beam communications. Transmitter ICs have drivers before the I/Q inputs, therefore we cannot control the amplitudes. This prevents multi-beam operation in the transmit side, but two separate boards can be used to show the multi-beam capability. In this work, we mainly demonstrated the single beam communications and the beamforming capability of the transceivers. We performed data transmission experiments over 25 cm wireless distance using the one channel of these transmitter and receiver boards. In wireless transmission experiments up to 5 GBaud rate, the eye patterns of the received data were clean and open. Moreover, this exper-

iment showed less than 10^{-3} bit-error-rate (BER) up to 2.5 GBaud data transmission rates. However, further BER experiments using channel equalization and QPSK modulation are in progress.

After realizing a fully-packaged 4-channel receiver and a fully-packaged 2-channel transmitter with successful single beam operation, we have sent some boards to our collaborator Samsung Research America in order to further investigate the multi-beam operation using their baseband FPGA processor. Fig. 7.1 shows the experiment plan initially, later idle sources will be replaced by the second transmitter board to send two independent data streams as well. The knowledge and board transfer have been completed as the final goal of my Ph.D work. At the same time, we built the multi-beam setup at UCSB with 2 transmitter boards. We aim to demonstrate multi-beam communications using arbitrary waveform generators (AWG) and digital oscilloscopes. This is still in progress. This work is currently being pursued by Mohammed Abdelghany from Prof. Madhow's group. I transferred the boards and my knowledge on the hardware parts to him for the follow-up work.

7.2 MIMO Communications Overview

Higher carrier frequencies allow to place large number of antennas in a small volume thanks to the small antenna and transceiver sizes. Therefore, it is easier to create arrays with a massive number of elements, and hence the multiple independent beams. Multiple beams can be supported in the receiver, transmitter or both. Consequently, we can create single-input multi-output (SIMO), multi-input single-output (MISO), and multi-input multi-output (MIMO) communications. SIMO and MISO channel can provide signal to noise ratio (SNR) improvement, but not multiplexing. In order to send multiple data streams, we need to create multiple beams using MIMO channels. With MIMO we can

use the space as an additional degree of freedom to the time and frequency, and create unique spatial signatures to the transmit or receive beams. However, this can be utilized effectively if we have an adequate separation between the transmit or receive antennas, or multi-path channel. This will allow us to create unique spatial signatures, and ease the spatial multiplexing.

7.2.1 MIMO Channel

Consider a scenario where the transmitter and receiver antennas are separated by $\lambda/2$. Each transmitter antenna we want to send an independent symbol simultaneously given by: $\overrightarrow{x} = \begin{pmatrix} x_1 \\ x_2 \\ x_3 \end{pmatrix}$ as shown in Fig. 7.2. If we denote h_{kl} as the channel between the k^{th} receiver and l^{th} transmitter, we can express $\overrightarrow{y} = H\overrightarrow{x}$, where $\begin{bmatrix} h_{11} & h_{12} & h_{13} \\ h_{21} & h_{22} & h_{23} \\ h_{31} & h_{32} & h_{33} \end{bmatrix}$ as the MIMO channel matrix. Let d_{kl} be the distance between each transmit and receive antennas. If we suppose $d_{11} = d$, then:

$$d_{kl} = d + \frac{\lambda}{2}(k-1)cos\phi + \frac{\lambda}{2}(l-1)cos\theta \tag{7.1}$$

$$H = ae^{j2\pi d/\lambda} \begin{bmatrix} 1 & e^{j\pi cos\theta} & e^{j\pi 2cos\theta} \\ e^{j\pi cos\phi} & e^{j\pi(cos\phi+cos\theta)} & e^{j\pi(cos\phi+2cos\theta)} \\ e^{j2\pi cos\phi} & e^{j\pi(2cos\phi+cos\theta)} & e^{j\pi(2cos\phi+2cos\theta)} \end{bmatrix} \tag{7.2}$$

Using the channel matrix given in Eq. 7.2, we can write the spatial signature of the

first transmitter as:

$$\begin{bmatrix} h_{11} \\ h_{21} \\ h_{31} \end{bmatrix} = ae^{j2\pi(d/\lambda)} \begin{bmatrix} 1 \\ e^{j\pi cos\phi} \\ e^{j\pi 2cos\phi} \end{bmatrix} \tag{7.3}$$

This is equal for all three transmitters with just a phase difference. Hence all the three cases are likely dependent. The channel is of rank one. Therefore, we cannot get H^{-1} to solve $y = Hx$. Now lets move on to the cases where either transmitter and receiver antennas are geographically separated, or there is a multi-path environment we can benefit. In these following cases we can have a separate spatial signatures and utilize the spatial multiplexing, hence the capacity gain.

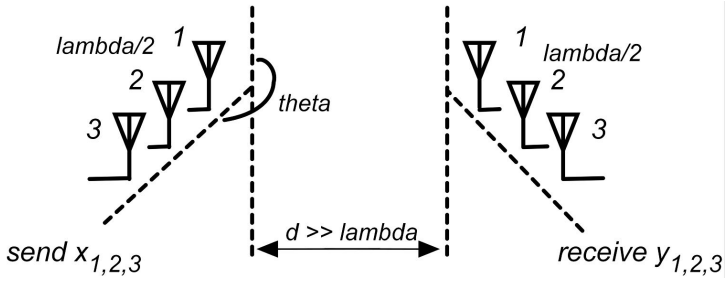

Figure 7.2: Line of sight MIMO with $\lambda/2$ spacing

7.2.1.1 Geographically Separated Transmit Antennas

If we have transmitters separated far from each other, we can have different spatial signatures (Fig. 7.3). This way we can increase the capacity by using the spatial dimension. In this case channel matrix can be written as Eq. 7.4.

$$H = ae^{j2\pi(d/\lambda)} \begin{bmatrix} 1 & 1 \\ e^{j\pi cos\phi_1} & e^{j\pi cos\phi_2} \end{bmatrix} \tag{7.4}$$

Eq. 7.4 shows that transmitter 1 and 2 has different spatial signatures, which is

equivalent to the series of phase differences. This scenario represents an up-link multi-user MIMO system.

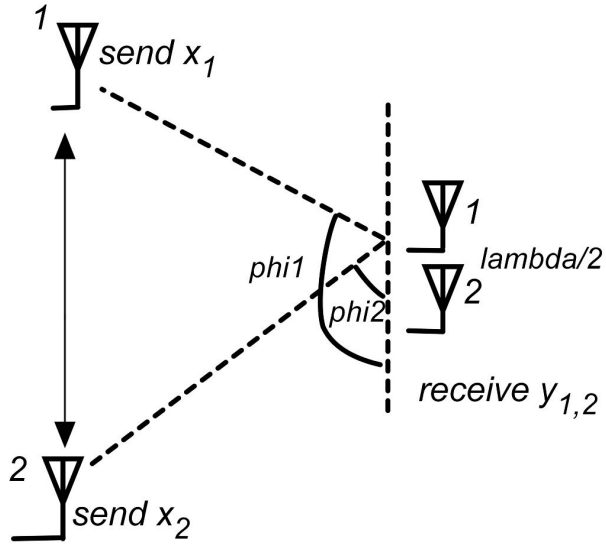

Figure 7.3: Geographically seperated transmit antennas

7.2.1.2 Geographically Separated Receive Antennas

Geographically separated receive antennas creates different spatial signatures for receivers. This scenario represents the down-link multi-user MIMO.

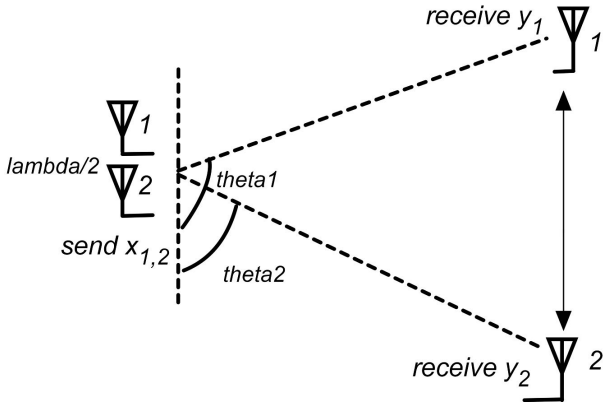

Figure 7.4: Geographically seperated receive antennas

7.2.1.3 MIMO in Multi-path

MIMO spatial dimension and capacity increase can be utilized effectively in a multi-path environment (Fig. 7.5). Multi-path creates unique spatial signatures for different beams, and creates an environment similar to the geographically separated receiver and transmitter antennas.

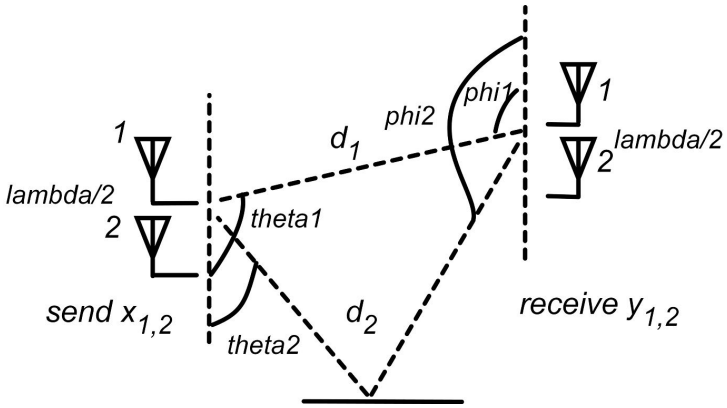

Figure 7.5: MIMO in multi-path environment

With multi-path environment channel matrix can be written as in Eq. 7.5. As can be seen in this matrix, there are unique spatial signatures, and using simple zero forcing, the receiver can separate the combined symbols. This increase the capacity by the number of the uniques spatial signatures. Further information related with the MIMO communications can be found in [108, 109]

$$H = \begin{pmatrix} a_1 e^{j2\pi d_1/\lambda} + a_2 e^{j2\pi d_2/\lambda} & a_1 e^{j2\pi(d_1/\lambda + cos\theta_1/2)} + a_2 e^{j2\pi(d_2/\lambda + cos\theta_2/2)} \\ a_1 e^{j2\pi(d_1/\lambda + cos\phi_1/2)} + a_2 e^{j2\pi(d_2/\lambda + cos\phi_2/2)} & a_1 e^{j2\pi(d_1/\lambda + cos\theta_1/2 + cos\phi_1/2)} + a_2 e^{j2\pi(d_2/\lambda + cos\theta_2/2 + cos\phi_2/2)} \end{pmatrix} \quad (7.5)$$

This brief introduction to MIMO communications shows that through multi-path or

geographical separation, unique spatial signatures can be created in MIMO channel. This can increase the number of streams sent. The maximum degree of freedom is equal to the minimum number of the receive or transmit antennas.

In this chapter, 4-channel receiver and 2-channel transmitter are built, tested and verified. These modules can be used to realize MIMO communications explained in this sub-section. Although modules support the MIMO communications, signal processing part needs high speed processors and large memory. Therefore, at that point collaboration with Samsung Research America and/or UCSD for the baseband processor will be critical. In this work, we focus on the module realizations and 1-channel measurements. In addition, we demonstrate the initial beamforming results for the single beam operation. However, next goal is to use multiple transmitter boards separated geographically and create spatially multiplexed MIMO communications. This will increase the capacity significantly.

Here we created the boards and the framework, and opened a path through the multi-beam communications. Knowledge and boards are transferred to our collaborator Samsung Research America in order to further explore the multi-beam communications using the modules designed in this dissertation. In addition, we started the multi-beam efforts with Mohammed Abdelghany from Prof. Madhow group just using the equipment including arbitrary waveform generator (AWG) and digital oscilloscope we have at UCSB.

7.3 2-Channel Transmitter

Two channels of the 4-channel transmitter IC and antenna array were wire-bonded together to form the 2-channel transmitter of Fig. 7.6. Only two active transmitter channels were connected due to the wirebond density concerns. The transmitter was

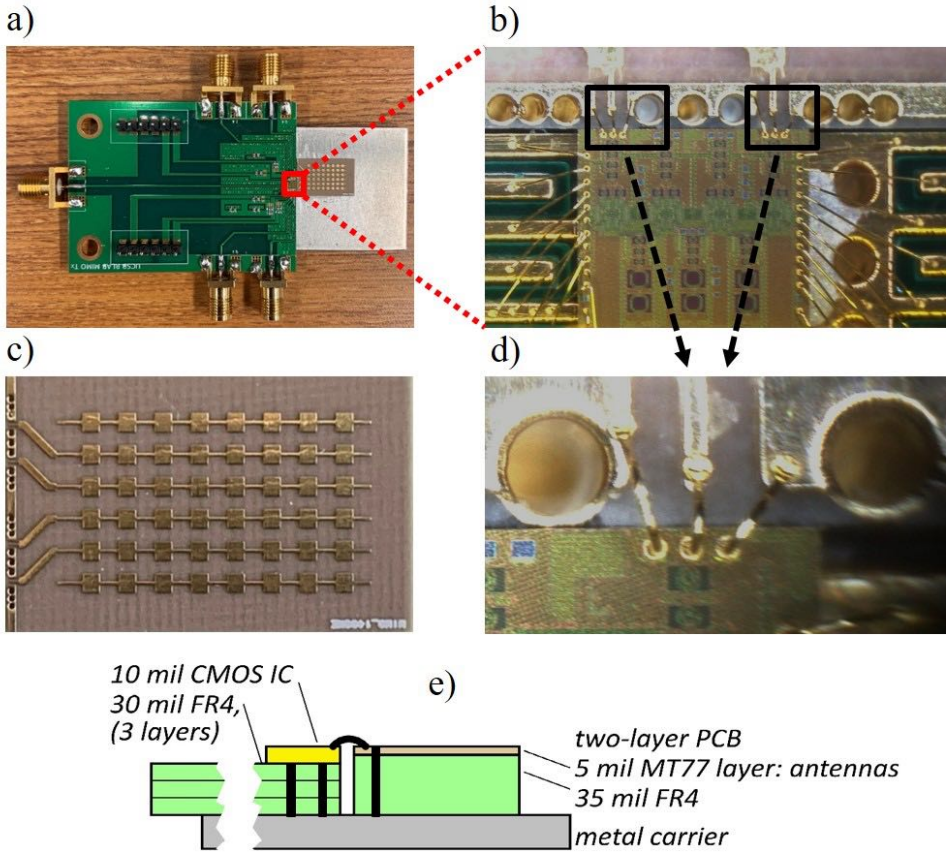

Figure 7.6: (a) Two-channel transmitter integrating a CMOS transceiver IC, a PCB carrying a microstrip patch antenna array, and a second PCB carrying low-frequency connections to the IC. (b) Zoomed image showing the ICs and wire-bond interface. (c) PCB 4-element antenna array, each of which is an 8-element series-fed linear microstrip patch antenna array. (d) Magnified image showing the wire-bonds. (e) Schematic cross-section of the assembly.

tested (Fig. 7.7) by driving its inputs by data from an arbitrary waveform generator (AWG), and by measuring the radiated power with a standard-gain horn coupled to a harmonic mixer and spectrum analyzer. The spectrum analyzer and harmonic mixer sensitivity was calibrated using a 140 GHz test signal source and a mm-Wave power meter. From the measured received power, the known gain of the standard-gain horn, and the transmitter-receiver separation distance, the transmitter effective isotropic radiated power (EIRP) can then be measured.

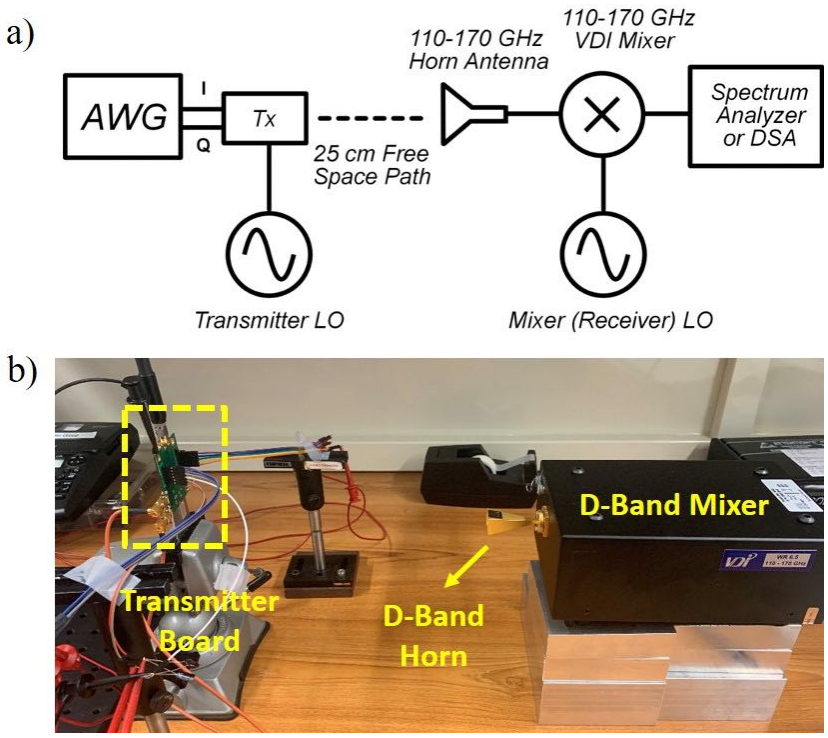

Figure 7.7: (a) Schematic diagram and (b) photograph of the apparatus for radiated power measurements and data transmission measurements.

If the AWG generates quadrature single-tone signals for (I, Q) inputs of one transmitter channel, then the transmitter will generate single-sideband modulation. If both transmitter channels are driven in this fashion, adjusting the relative phases of the transmitter inputs will adjust the relative phases of the transmitter outputs. Bringing the two transmitter outputs into phase (Fig. 7.8.a) results in spatial power-combining of the two transmitters. The EIRP is then 19.9 dBm. If, instead, the first transmitter is driven with such single-sideband modulation, and the second transmitter is driven with constant (DC) baseband inputs, then the two transmitters will radiate at different frequencies, without spatial power-combining. In this case (Fig. 7.8.b) the two transmitters have EIRP of 13.8 dBm and 14.13 dBm. 6 dB combining gain includes the 3 dB gain from the transmitter IC and 3 dB gain from the antenna gain.

The measurement is then repeated while sweeping the LO frequency. The result (Fig.

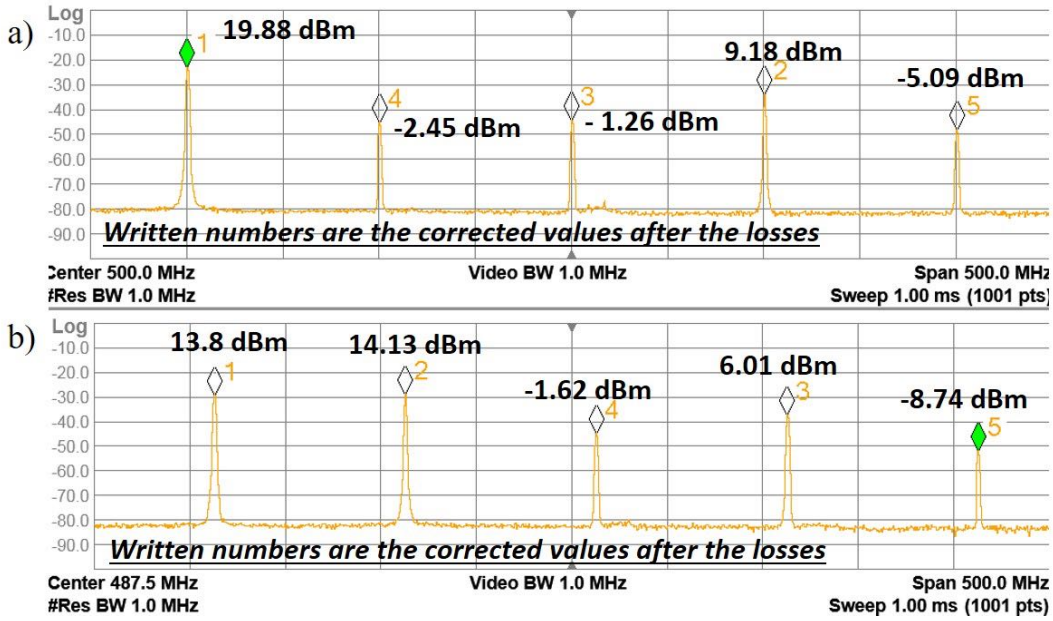

Figure 7.8: Received output spectra from the two-channel transmitter. In (a), both channels are driven with (I, Q) inputs corresponding single-sideband modulation with the two transmitters radiating in-phase. The measured EIRP is then 19.9 dBm. This demonstrates spatial power-combining. In (b) one channel is driven with (I, Q) inputs corresponding single-sideband modulation, while the other transmitter operates with DC (I, Q) inputs. The two transmitters then radiate at different frequencies, with measured EIRP for the two tones of 13.8 and 14.13 dBm.

7.9) shows transmitter power-combining as a function of frequency. The observed EIRP is consistent, within experimental error, with the measured transmitter IC output power, the measured antenna gain, and the simulated wire-bond insertion loss (shown in Fig. 6.17). Rough calculation from the measurements prove this as well within $\pm 1-2$ dB experimental errors (Eq. 7.8).

$$P_{out,chip} - Loss_{WB} + G_{ant} = P_{spectrum\,corrected} \tag{7.6}$$

$$2 - Loss_{WB} + 14 = 13.8 \tag{7.7}$$

$$Loss_{WB} = 2.2\,\mathrm{dB} \tag{7.8}$$

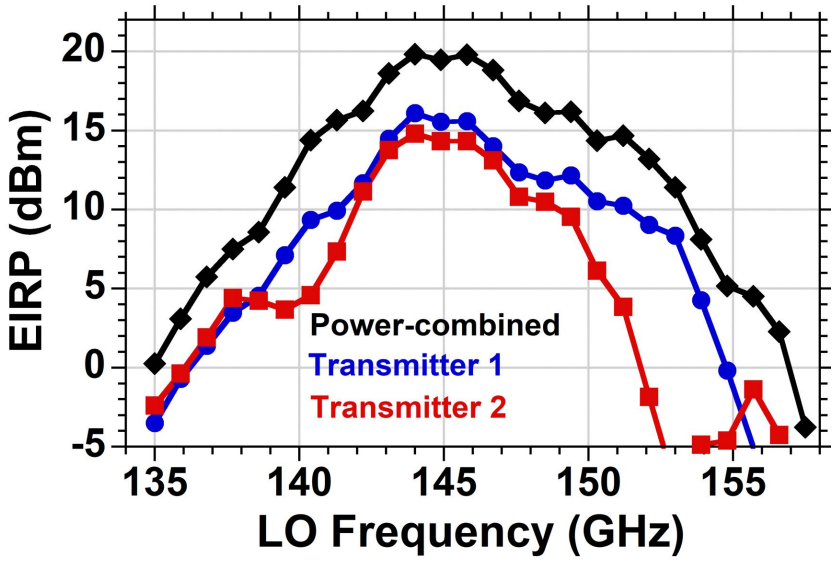

Figure 7.9: EIRP vs. frequency with the two transmitters power-combined and operating independently.

The data transmission experiment again uses the configuration of Fig. 7.7, with one transmitter channel inactive and the second transmitter channel driven by independent pseudo-random data sequences (PRBS) of different sequence lengths to its I and Q inputs. The output of the VDI harmonic mixer is connected to a digital oscilloscope (DSAV134A - Keysight) through an external amplifier having 24 dB gain. The oscilloscope displays the eye diagrams of the received I/Q waveforms. Without applying equalization within the digital oscilloscope, open eye patterns are observed with 10 Gb/s QPSK data transmission and 25 cm propagation distance (Fig. 7.10). Data rate higher than 10 Gb/s utilizes the feed-forward equalization for clock recovery and decision feedback equalization to further remove the inter-symbol interference (ISI) by correcting frequency response of the channel, cable, circuit and the test amplifier.

Results show that wirebond interface and antenna designs can support at least 7 GHz of bandwidth. By combining multiple transmitter channels with baseband beamforming one can support multiple independent beams, therefore multiple of 14 Gb/s data rate.

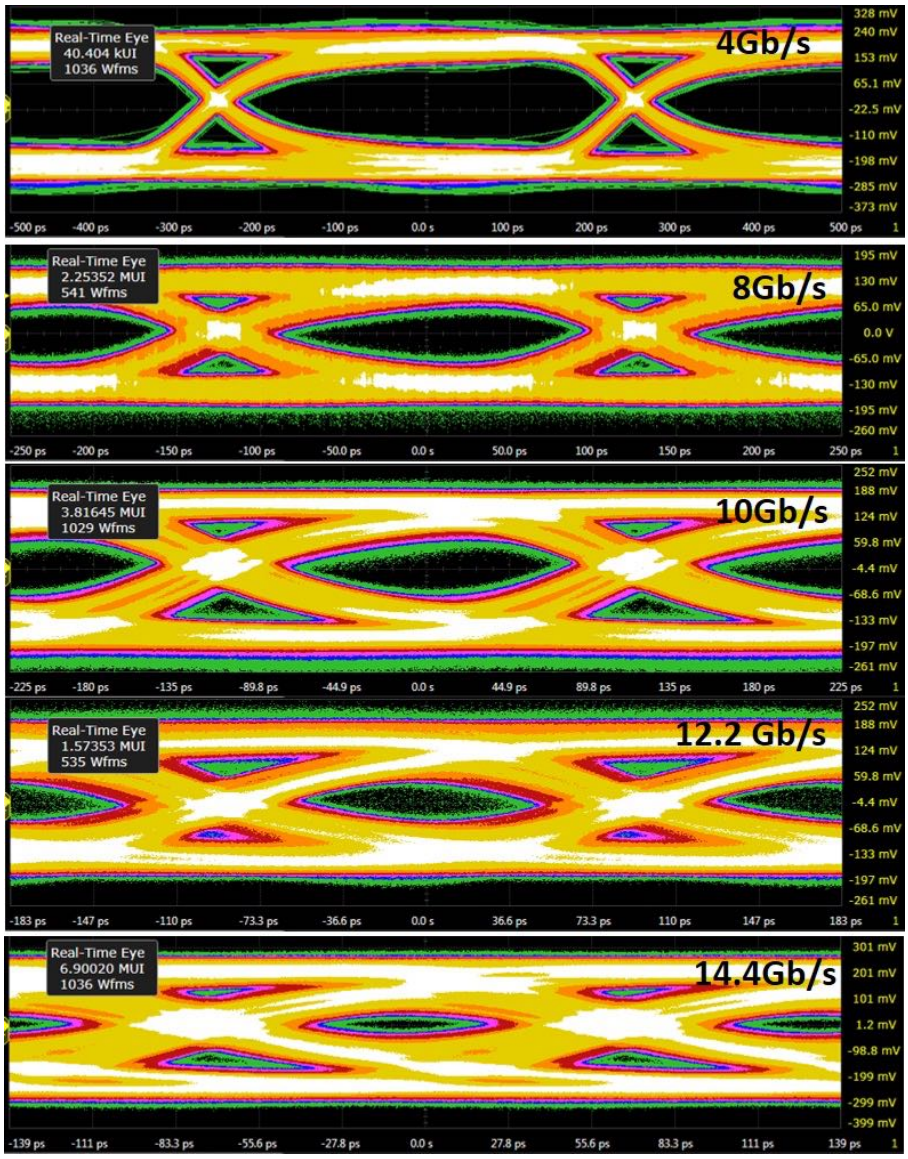

Figure 7.10: Eye diagrams captured in Keysight oscilloscope DSAV134A for 4 Gb/s, 8 Gb/s, 10 Gb/s, 12.2 Gb/s, and 14.4 Gb/s QPSK data transmission over 25 cm wireless link at 145.8 GHz carrier frequency.

However, in this transmitter chip there is a baseband interface, which makes the QPSK inputs square waveforms. This prevents the MIMO operation in the transmit side. In future, this interface can be removed to support multiple independent beams. ICs reported in Chapter-3 already removed this interface and they can support multi-beam operation in the transmit side as well. For multi-beam operation using these boards, two separate

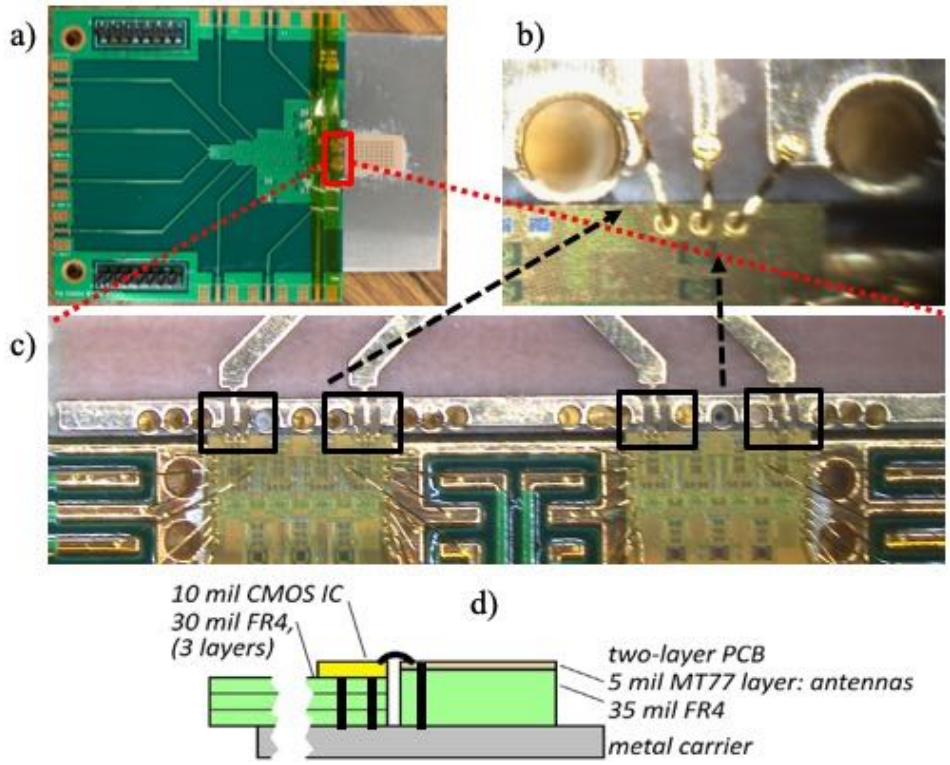

Figure 7.11: (a) Four-channel receiver integrating a two 4-channel CMOS transceiver IC, a PCB carrying a microstrip patch antenna array, and a second PCB carrying low-frequency connections to the IC. (b) Zoomed image showing high frequency wire-bond connections. (c) Zoomed view of the IC-wirebond interfaces (d) Schematic cross-section of the assembly.

transmitter boards need to be used.

7.4 4-Channel Receiver

4-channel receiver is again developed using the same integration principles with the transmitter board. Fig. 7.11 shows the 4-channel receiver board, and the close views of the wirebond interconnects. Using this board, receiver is characterized functionally with gain-frequency measurements using the measurement setup shown in Fig. 7.12. D-band up-converter (harmonic mixer) from VDI is used as the transmitter, followed by an amplifier and a standard gain horn antenna at D-band. Power of the VDI plus the amplifier

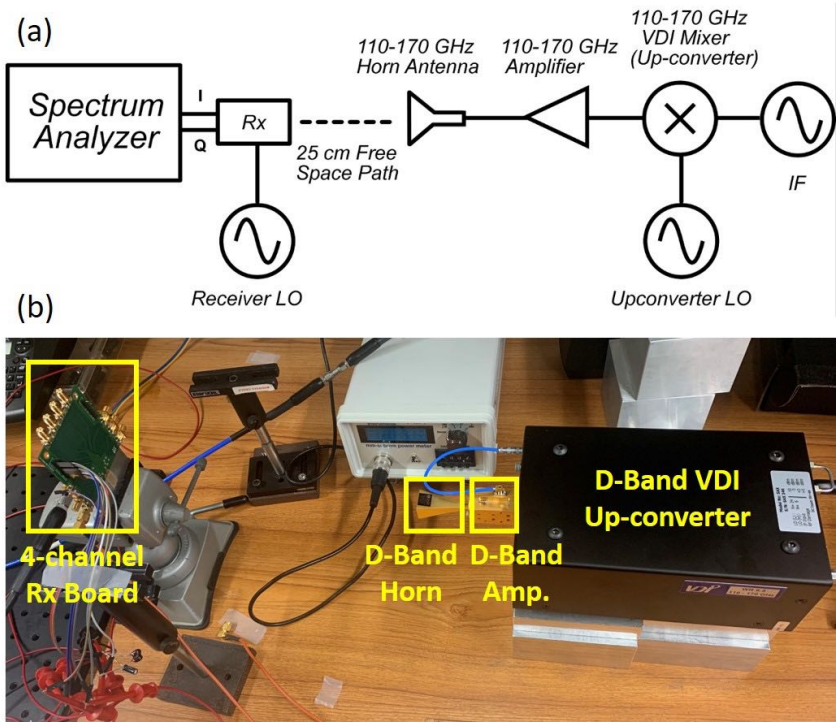

Figure 7.12: (a) Schematic diagram and (b) Image of the receiver board measurement setup.

are measured using Erickson PM4 power meter, and the measurements are corrected accordingly. Firstly, up-converter and receiver LOs are fixed at 145.8 GHz (actually we shifted the LOs 900 MHz to prevent the phase dependent amplitude variations during the measurement), and IF frequency is swept. Only one IC in the receive board was powered up and 2 channel I/Q measurements are recorded. The other IC, therefore the other 2-channels behave similarly. All cable losses, free space path loss, as well as the VDI mixer and amplifier losses are de-embedded.

Fig. 7.13 shows the receiver gain for the fixed LO case. I2 branch's gain is really low compared to the other channels, this is most probably due to the deformation on a wirebond or transmission lines or the edge connector at that branch. The other branches show about 20 dB gain, with single sideband 3-dB bandwidth of 2-3 GHz. Hence, the total expected 3-dB bandwidth is about 4-6 GHz. Receiver 3-dB bandwidth seems limited. Fig.

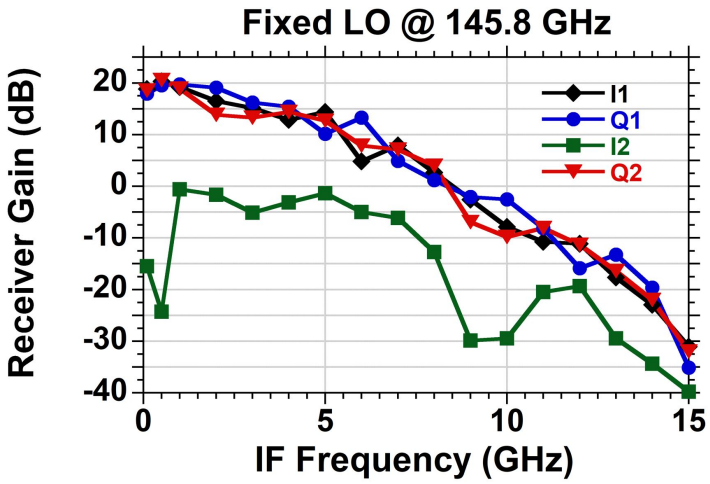

Figure 7.13: Gain of the two channel I/Q branches of the receiver board at fixed LO frequency of 145.8 GHz

7.14 demonstrates the receiver gain for the fixed IF frequency case. In this measurement IF is fixed at 1 GHz and LOs are swept. Similarly, I2 branch shows significantly lower gain as expected from the previous measurement. The other branches show 18 to 22 dB gain with about 5 GHz of 3-dB bandwidth. Calculations from the measured values show that wirebond loss is close to the simulation value within the experimental measurement errors (Fig. 7.11).

$$G_{Rx,IC} - Loss_{WB} + G_{ant} = G_{Rx,Board}\,(\text{Single ended}) \tag{7.9}$$

$$10 - Loss_{WB} + 14 = \sim 21 \tag{7.10}$$

$$Loss_{WB} = \sim 3\,\text{dB} \tag{7.11}$$

Receiver measurements show that the receiver board is also working functionally. With these measurements we directly moved on to the transceiver experiments, where we placed transmitter board and receiver board 25 cm apart, and tried to measure the gain vs. frequency curves. In addition, we did data transmission, and beamforming

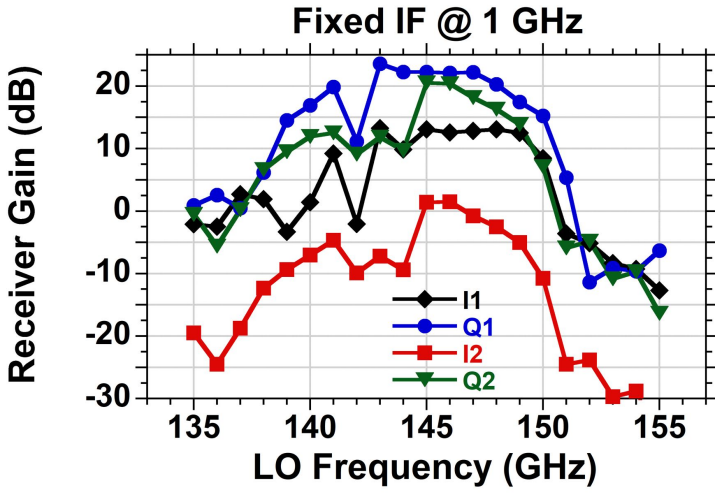

Figure 7.14: Gain of the two channel I/Q branches of the receiver board at fixed IF frequency of 1 GHz

experiments using the transmit and receive boards together. This brings us to the next section of the chapter.

7.5 Transceiver Experiments

In order to evaluate the transceiver performance, we performed one channel measurements using one transmitter and one receiver board. Frequency dependent gain behavior of the transceiver was measured by applying single tone I/Q signals to one channel of the transmitter board and recording the receiver output power for different I/Q channels. Data transmission experiments were performed by applying the pseudo-random bit sequence (PRBS) data through one I/Q channel of the transmitter board, and observing the data streams out of the receiver I/Q channels. Fig. 7.15 shows the experimental setup and the close look of the transmit and receive boards. Two different signal generators fed the local oscillator (LO) frequencies into the transmitter and receiver multipliers. These signal sources were locked to each other through external 10 MHz reference clock.

As an initial experiment, we measured gain-frequency characteristics over $\sim 25\,\text{cm}$

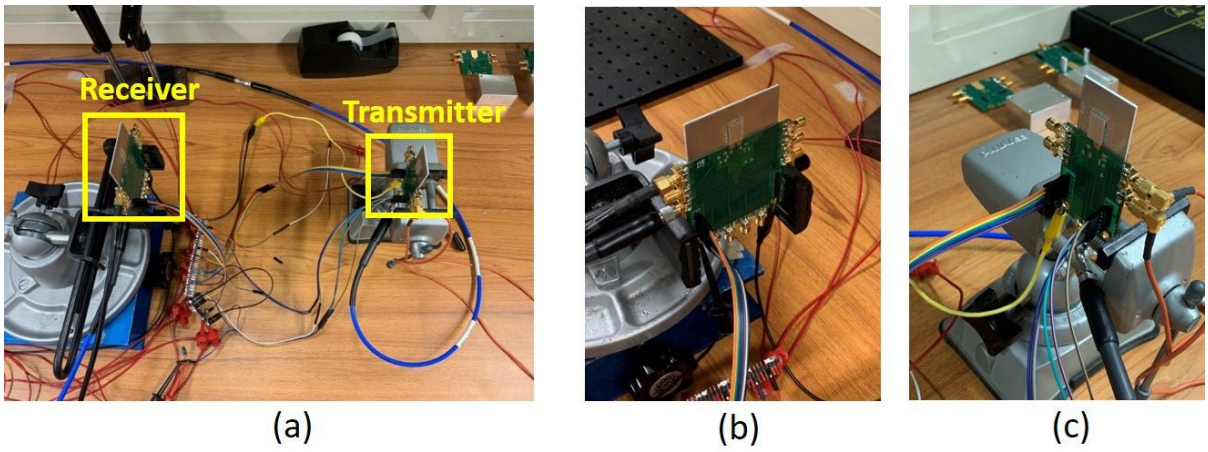

Figure 7.15: (a) Experiment setup for the transceiver measurements with 25 cm wireless link distance (b) Closer look of the 4-channel receiver board (c) Closer look of the 2-channel transmitter board

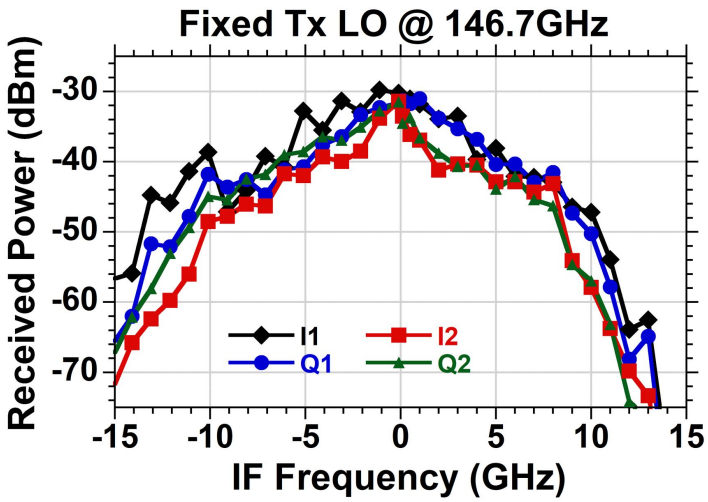

Figure 7.16: Measured gain vs. frequency curve for fixed LO at 146.7 GHz

air between the transmitter and receiver boards. Single tone I/Q signals were applied to one channel of the transmitter board, then the output from 2-channels of the receiver were recorded. Other channels are similar, and gives the similar results but detailed measurements are shown here only for the 2-channels for the simplicity in the plots. Firstly, LOs of the transmitter and receiver were kept constant at 146.7 GHz, and the IF frequency were swept. Received powers on the receiver after de-embedding the cable

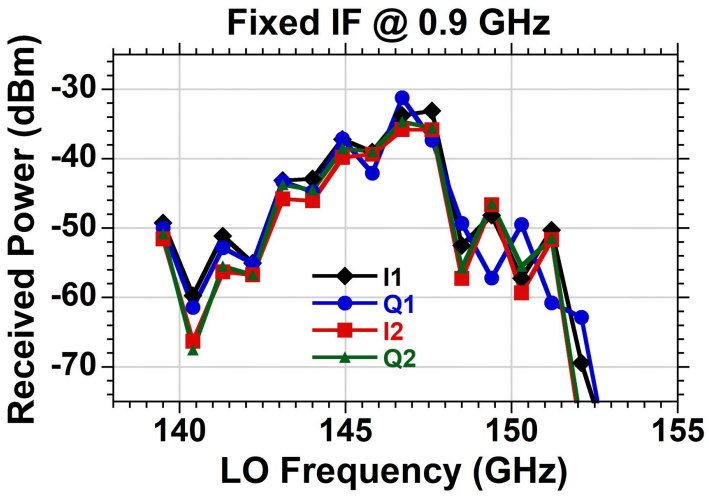

Figure 7.17: Measured gain vs. frequency curve for fixed IF at 0.9 GHz

losses were measured $\sim -30\,\text{dBm}$ for 2 channels I/Q outputs, with $\sim 5\,\text{GHz}$ of 3-dB bandwidth (Fig. 7.16). During these measurements I applied slight offsets to LOs of the transmitter and receiver, and I observed two sidebands at the receiver spectrum. When the LOs are at exactly same frequencies, due to phase fluctuations in time I observed an amplitude variation at the output spectrum. Using slightly different LO frequencies prevented this problem.

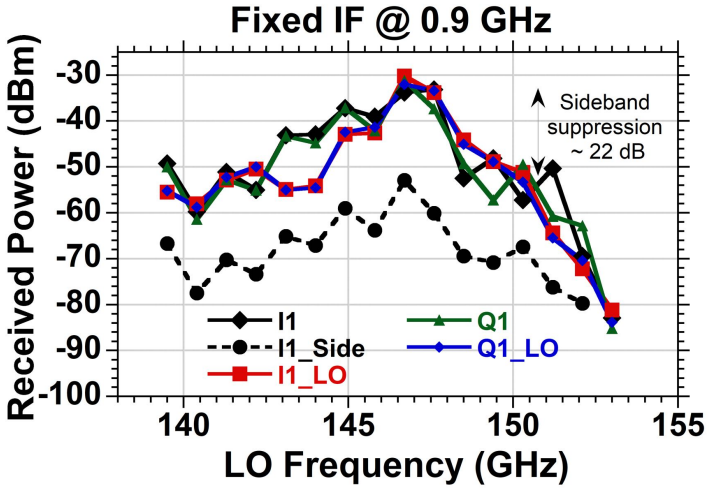

Figure 7.18: Measured gain vs. frequency curve for fixed IF at 0.9 GHz for one channel including the received sideband and LO powers

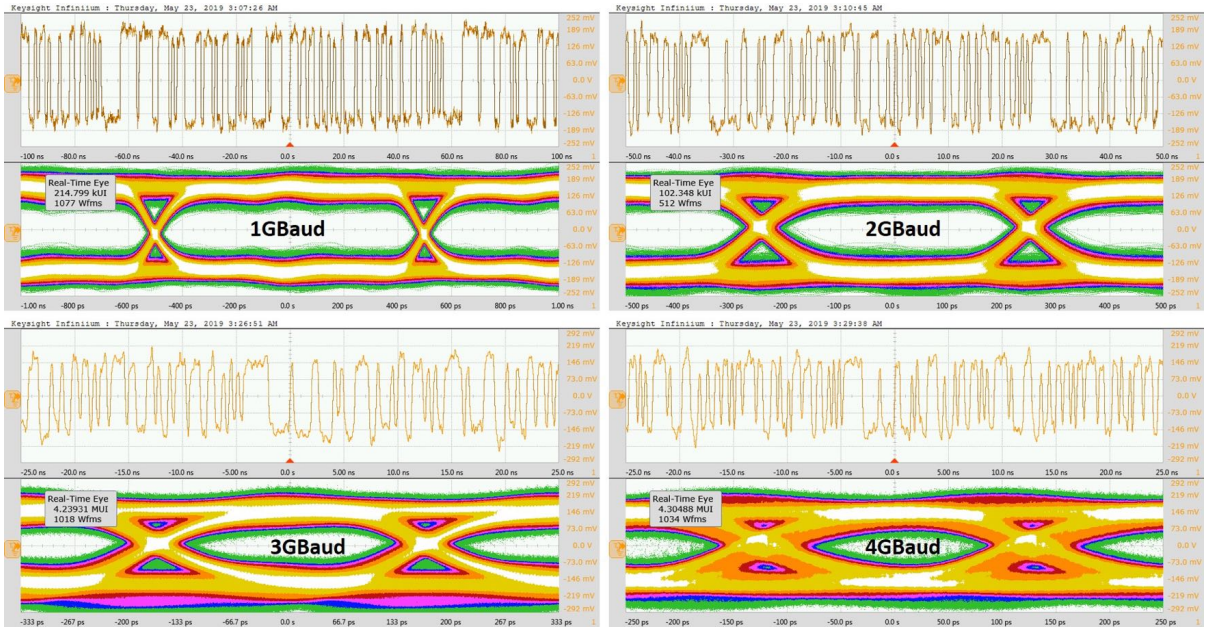

Figure 7.19: Eye patterns at the I output of one channel of the receiver, captured in Keysight oscilloscope DSAV134A for 1 GBaud (2 Gb/s), 2 GBaud (4 Gb/s), 3 GBaud (6 Gb/s), and 4 GBaud (8 Gb/s) QPSK data transmission over 25 cm wireless link at 146.7 GHz carrier frequency.

Then, we fixed the IF frequency at 0.9 GHz, and swept both the transmitter and receiver LO frequencies. After de-embedding the cable losses ~ -32 dBm power received at the receiver I/Q channels. (Fig. 7.17). In this case, bandwidth is severely limited due to the limitations both from the transmitter and receiver LO tuning ranges.

In these experiments, only 1-channel of the transmitter is active, the second channel's input is not applied. Therefore, this channel is not modulated, but since it is connected to the antenna, LO is radiated without the modulation. Since we applied I/Q waveform, the output is similar to the single sideband operation, and upper sideband is suppressed. Fig. 7.18 shows the channel-1 I branch main, sideband and LO powers as well as the Q branch main and LO powers. As can be seen, sideband suppression is about 22 dB, and LO is about the same power level with the main sideband. This is expected, and LO comes from the unmodulated second channel of the transmitter board.

After successful characterization of the gain-frequency curves of the transceiver, we performed wireless data transmission experiments over 25 cm air. Independent pseudo-random bit sequence (PRBS) data streams were applied to I and Q inputs of one channel of the transmitter, then the output of the receiver I/Q channels were recorded. Using the Keysight DSAV134A high speed digital oscilloscope, eye patterns out of the receiver I/Q channels were observed. In this case we only recorded the I of the channel-1. In wireless data transmission experiments, we observed clean and open eye patterns at the receiver I channel output up to 8 Gb/s without any equalization (Fig. 7.19). However, for data rates higher than 8 Gb/s we applied a feed-forward equalization for clock recovery and decision feedback equalization for the inter-symbol interference (ISI) suppression through the oscilloscope feature (Fig. 7.20). This corrects the frequency response of the channel, ICs and the test setup by applying an inverse finite impulse response (FIR) filter. In this data transmission experiments, external LOs were at 16.3 GHz which is equal to 146.7 GHz as the carrier frequency.

To further prove the eye diagram results, we first used the bathtub utility of the Keysight DSAV134A and created the bathtub curves (Fig. 7.21). This utility does not directly compare the transmitted vs. the received data streams, but it utilizes the jitter information from the received data stream. From the eye diagrams it calculates the timing jitters and approximately calculates the BER from these jitter data. It is still not as precise as comparing the data bit by bit, but it further proves the wireless data transmission using this transceiver.

As can be seen in Fig. 7.21, 1, 2 and 3 GBaud data rates (2, 4, and 6 Gb/s for QPSK) have wide openings at 10^{-6} BER, while 4 GBaud (8 Gb/s for QPSK) has marginal opening at 10^{-6} BER. In these curves, blues are the actual measured data, and the whites are the extrapolation points. For each measurement, I waited roughly 10-20 minutes to get enough data points. For all measurements random jitter RMS value is close and

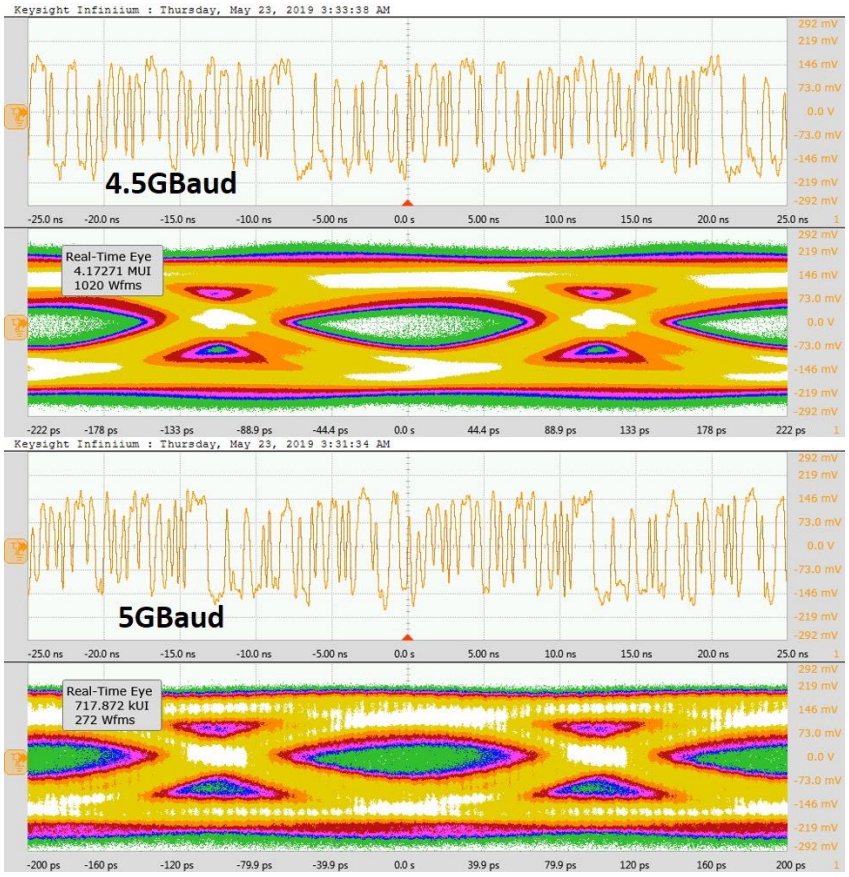

Figure 7.20: Eye patterns at the I output of one channel of the receiver, captured in Keysight oscilloscope DSAV134A for 4.5 GBaud (9 Gb/s), and 5 GBaud (10 Gb/s) QPSK data transmission over 25 cm wireless link at 146.7 GHz carrier frequency (Equalization applied through oscilloscope)

about 10-12 ps. These curves suggest that data transmission over 25 cm air up to 4 GBaud using QPSK modulation with these transceivers can be achieved.

In addition to these measurements, we also measured the actual bit-error-rate (BER) of the transceiver. Mohammed Abdelghany from Prof. Madhow's lab helped me on these measurements, where we sent a known PRBS data stream to I branch of the transmitter channel and saved the data received from the receiver I channel. Mohammed wrote a Matlab script, which applies a channel equalization as well and compares the sent and received data stream to calculate the BER. Fig. 7.22 shows the BER results for BPSK modulation. In wireless data transmission experiments over 25 cm air, this transceiver

Figure 7.21: Bathtub curves, and timing jitter data captured in Keysight oscilloscope DSAV134A for 1, 2, 3, and 4 GBaud data rate QPSK data transmission over 25 cm wireless link at 146.7 GHz carrier frequency.

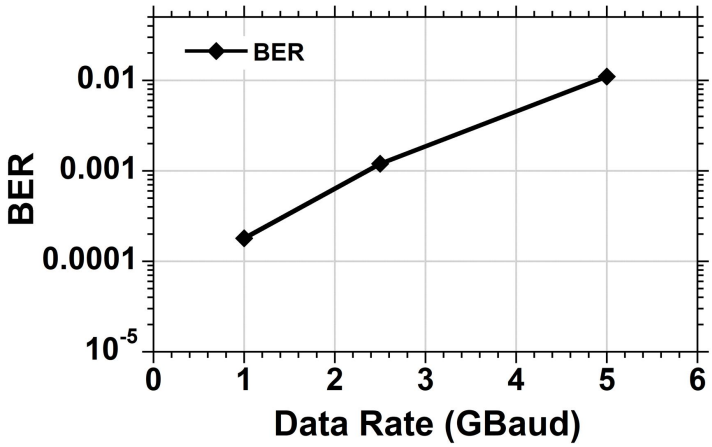

Figure 7.22: Measured bit-error-rate (BER) of the one channel transceiver at different data transmission rates over 25 cm wireless link at 146.7 GHz carrier frequency using BPSK modulation

achieves 10^{-3} BER up to 2.5 GBaud data rate. BER approaches to 10^{-2} around 5 GBaud data rate for the same data transmission experiment. The main limitations come from the limited transceiver bandwidth and high receiver noise figure. In addition, channel response is not good due to the reflections at certain distances.

Recently, Samsung Research America 5G&6G development team in Dallas has shown interest in these transceivers to create a path towards next generation communications,

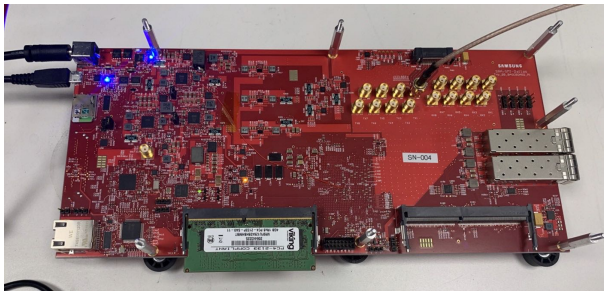

Figure 7.23: Baseband FPGA board of Samsung Research America to be used in beamforming experiments

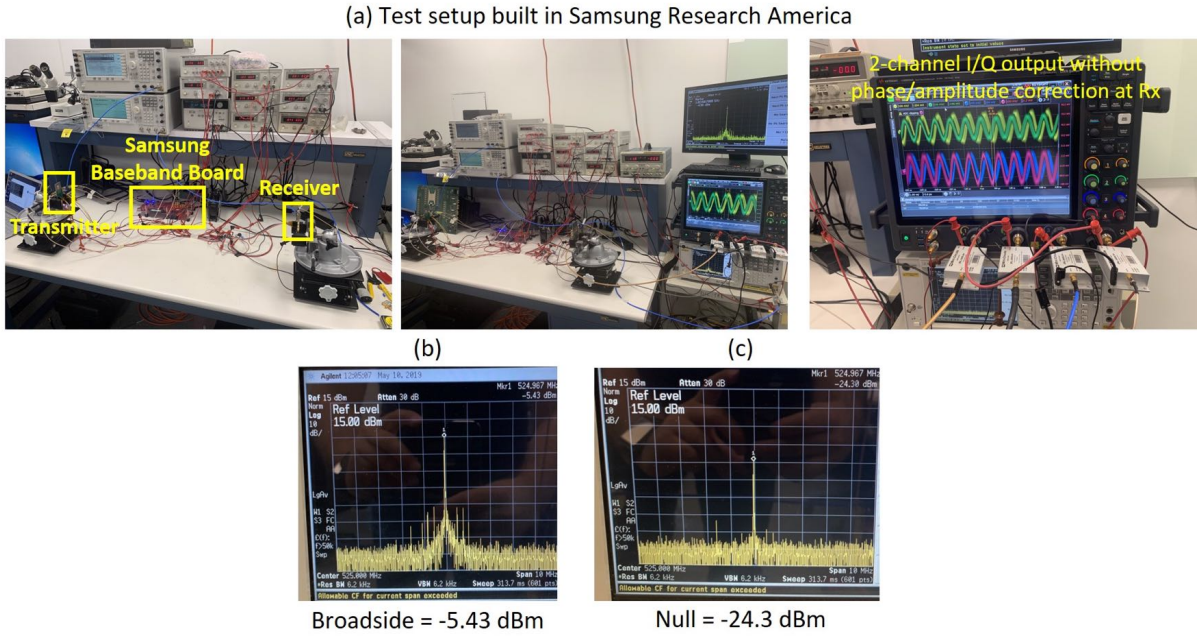

Figure 7.24: (a) Experiment setup using our transmitter, receiver modules and Samsung baseband board (b) Transmitter output power at broadside (c) Transmitter output power at null. Carrier frequency is at 145.8 GHz

6G. Therefore, I worked closely with them, and visited them for a week to transfer the technology and the knowledge. They have a custom built baseband processing board with 4 I/Q channels at transmit and receive side with high speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) (Fig. 7.23). This makes an effective collaboration for both sides to realize an end to end demonstration. During the visit, we integrated our transceivers with these baseband boards and we performed initial

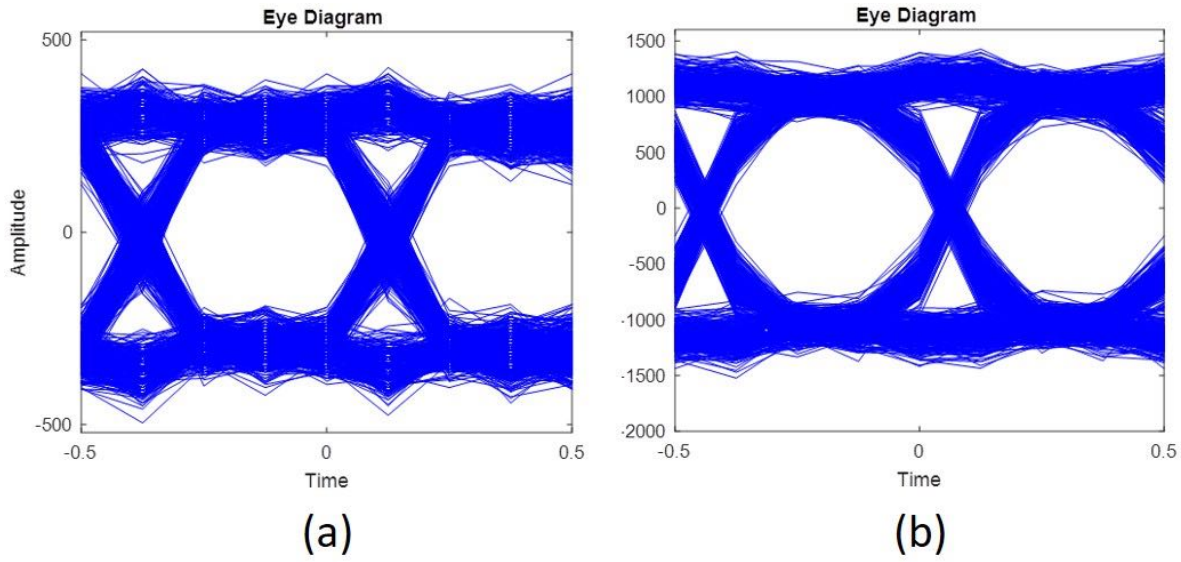

Figure 7.25: (a) Received data on 1-channel with 983.04 MSps data applied to transmitter channel-1 I-branch (b) Combined received data from 4-channels with the same data rate applied - receive beamforming. Carrier frequency is 145.8 GHz.

beamforming experiments at 1 meter link distance. Gary Xu, Nikalous Klemmer, Navneet Sharma, Shadi Abu-Surra, and Yu Liu programmed the baseband boards and helped me in these measurements. Firstly, in the transmitter side, we applied a single tone to 2-channels, and we adjusted the phase offset between 2-channels using the baseband board. Then we recorded the output at the electrical spectrum analyzer. For different phase offsets maximum (Fig. 7.24.b) and minimum (Fig. 7.24.c) power levels were recorded. They correspond the broadside and null in the antenna pattern. This proves the successful integration of baseband board and transmit beamforming operation with 2 channels.

Similar experiment was performed to show the receive beamforming. In this case we applied PRBS data stream with 983.04 MS/s from the baseband board through I-branch of the 1-channel of the transmitter. Then, we created the receive eye diagrams first using only 1-channel output (Fig. 7.25.a). Then, we combined the 4-channel outputs together (Fig. 7.25.b) using Matlab to show the beamforming gain. 4-times beamforming

gain is demonstrated. 1-channel data output shows $\sim$ 600 mV peak-to-peak voltage swing, whereas 4-channel combined version shows $\sim$ 2.4 V peak-to-peak voltage swing. It corresponds to the 6-dB beamforming gain as expected. In addition, eye is further opened through beamforming and phased array operation due to the SNR improvement.

7.6 Conclusion

Using the antenna and transition designs explained in the previous chapter, we developed a fully packaged 4-channel receiver and a fully packaged 2-channel transmitter boards at low-cost. These phased array transceivers work above 140 GHz carrier frequencies. They are the first demonstrated phased arrays at these frequencies to the best of author's knowledge. They can support both single and multi-beam communications. The structure can be extended to larger arrays via tiling.

In this chapter, we first demonstrated a two-channel transmitter module with 20 dBm EIRP, consistent to within measurement precision with the transmitter output power, simulated interface losses, and measured antenna gain. Transmitter boards show clean eye patterns up to 14.4 Gb/s data rate for the 25 cm wireless data transmission experiments. 4-channel receiver board has 20-22 dB gain per channel (single ended), and channels can be combined to realize higher gain (beamforming). Transceiver demonstrates $\sim$ 5 GHz 3-dB gain bandwidth for the fixed LO case. Wireless data transmission experiments are performed for one channel of the transceiver boards. Clean eye patterns up to 5 GBaud data rate at the output of the receiver channel were demonstrated in this wireless data transmission experiments over 25 cm. Measured bathtub curves prove that the transceivers can work up to 5 GBaud data rate as well with wide opening in the bathtub curves at $10^{-4} - 10^{-6}$ BER. Moreover, we measured the BER for the one channel transceiver again using the 25 cm wireless data transmission experiment. The

BER is less than 10^{-3} up to 2.5 GBaud data rate, and less than $\sim 10^{-2}$ for 5 GBaud data rate.

We further demonstrated the beamforming capability both in the transmitter and receiver boards. Transmitter 2-channel EIRP is ~ 20 dBm, which is ~ 6 dB higher than the one channel operation as expected. 3-dB comes from the output power of the ICs and another 3 dB comes from the antenna gain. 4-channel receiver beamforming gain is measured as 6-dB, or 4 times higher received power, again as expected. Hence, these boards are the first phased array transceivers working above 140 GHz with beamforming capability. Up to 5 GBaud data transmission can be achieved using these boards over 25 cm wireless link.

For the next step, these transceivers need to be further integrated with the baseband processors in order to fully make use of the beamforming gain. In addition, separate transmitters need to be used to send independent streams in order to demonstrate the multi-beam communications and the spatial multiplexing gain. More importantly, these structures can be extended, via tiling, to realize larger arrays. We now transferred the technology to our collaborator Samsung Research America and Prof. Madhow's system group here at UCSB in order to further pursue the both single and multi-beam experiments. With a better performance ICs reported in Chapter-5, these boards can be re-designed to support higher data rates. In addition, those ICs don't have the limiters at the transmitter inputs and they can be directly used for multi-beam operation using only one transmitter board.

Chapter 8

Conclusions and Future Work

8.1 Optical Frequency Synthesis using Heterodyne Optical Phase-Locked Loops

In this dissertation, we proposed and demonstrated chip scale optical frequency synthesis using highly integrated heterodyne optical phase-locked loops (OPLLs), in order to further develop optical communications and sensing. Through this, we have demonstrated the possibility of an optical revolution, similar to the microwave revolution that happened 40 years ago through the microwave frequency synthesizer design.

First, we demonstrated the two heterodyne OPLLs. Both OPLLs use commercial-off-the-shelf (COTS) integrated circuits (ICs) for the feedback electronics. Photonic integrated circuits (PICs) were designed and fabricated by Freedom Photonics LLC. The second generation PIC uses a compact cavity Y-branch laser, and eliminates some of the semiconductor optical amplifiers (SOAs). Therefore, it consumes significantly less power than the first generation PIC. The first generation PIC can tune over 40 nm, whereas the second generation PIC can tune over 60 nm. As a result, we realized a record low-power

heterodyne OPLL in the second generation with only 1.3 W, whereas the first generation OPLL consumes 1.8 W. Both OPLLs can lock up to at least 15 GHz offset frequencies, and provide less than 0.067 rad^2 phase error variance from the locking point.

Using these OPLLs, we then demonstrated two optical frequency synthesizers using a magnesium fluoride (MgF_2) microresonator-based optical comb generator, provided by the OEWaves. Frequency synthesis is achieved by offset-locking an on-chip widely tunable laser to an optical frequency comb with a 50-dB span of 25 nm ($\sim$ 3 THz) around 1550 nm with a 25.7 GHz repetition rate. The physical package of the comb source includes the pump laser, the optical coupling element, the high-Q microresonator, support electronics and thermal control with a volume of less than 0.2 cm^3 and a total electrical power consumption of 400 mW. Gen-1 OFS consumes 2 W of power, whereas gen-2 OFS consumes about 1.7 W. They both show a sub-100 Hz tuning resolution within $\pm$5 Hz accuracy, and gen-1 OFS also shows less than 200 ns switching time between two dozen comb lines ($\sim$ 5.6 nm). The phase noise variance from 1 kHz to 10 GHz is measured to be 0.08 rad^2 for the gen-1 OFS, corresponding to a 14° standard deviation from the locking point.

For a future extension of this work, application specific integrated circuits (ASICs) for the electronic feedback loop can be developed using sub-45 nm CMOS technologies, in order to further decrease the power consumption of the heterodyne OPLL. Using 0.8 V supply technology, heterodyne OPLL circuits with less than 200 mW can be designed and fabricated. In addition, the comb source can be further developed to span a wider range with self-referenced ultra-stable characteristics, as well as with a smaller size. Moreover, the comb source, widely tunable laser and electronics can be heterogeneously integrated in 1 cm^3 volume. With these improvements, we can create a true chip-scale, highly integrated optical frequency synthesizer consuming less than 1 W of power within 1 cm^3 of volume. Then, this unit can be used to realize broadband optical communications.

8.2 Broadband Wireless Communications at D-Band

In order to respond to the data demand for both the user-end point and the backhaul communication links, we proposed and presented mm-Wave transceivers using low-cost, high-yield CMOS technologies, low-cost yet efficient antennas, transitions, and fully packaged systems that can support broadband, high-speed data links.

We first demonstrated a broadband transmitter and a receiver channel using 22 nm CMOS FDSOI technology. The receiver channel shows a 27 dB conversion gain with a 3-dB bandwidth of 20 GHz. The transmitter's conversion gain is 18 dB with a saturated output power of 3 dBm. The transmitter and receiver consumes 196 mW and 198 mW respectively, from a 0.8 V supply. This transceiver can support a 10 GBaud data rate without modulation limitation. Therefore, the data rate can be as high as 80 Gbit/s with 64-QAM modulation. In addition, we also demonstrated transceiver link measurements, as well as the summary of the design and measurements of the previously designed 4-channel MIMO transceivers, using 45 nm CMOS SOI technology. In wireless data transmission experiments over 20 cm air, we demonstrated clear and open eye patterns at the receiver up to 8 GBaud data rate. In this data transmission experiment, we used horn antennas through wafer probing with a 145.8 GHz carrier frequency. These transceivers consume $\sim 450 - 500$ mW for the transmitter and receiver when all 4-channels are on. The receiver 3-dB IF bandwidth is about 10-12 GHz, with 18 dB differential gain. The transmitter output power is -2 dBm at 1V, and 1 dBm at 1.1 V supply with more than 10 GHz 3-dB bandwidth. The receiver noise figure is simulated as 5.5 dB, but measured as 15 dB due to the significant degradation of the conversion gain of the receiver channel. Transmitter LO suppression is more than 20 dB.

After the design, fabrication and measurements of the CMOS transceivers at D-Band, we also designed and demonstrated low-cost and efficient antenna and wirebond

transition designs using high performance Isola Astra MT77 material. Antennas show 13.5-14 dB measured gain, compared to the 15-15.5 dB gain in simulation. The 3-dB gain bandwidth is measured as 7 GHz, and it is closed to the simulations. The 3-dB E-plane and H-plane beamwidths are 9° and 65° respectively. They also align well with the simulations. The transition loss is simulated as 1.8 dB using the 3D electromagnetic simulator, Ansys HFSS. Simulated transition loss is close to the measurement results, within the accuracy of the fully packaged transceiver measurements. We also initiated and proposed simulations and designs of the more generic packaging, antenna and transition designs using low-temperature co-fired ceramic (LTCC) to create 8-element modules, which can easily be tiled to realize arrays with a massive number of elements. This module can also incorporate the III-V based high performance amplifiers to increase the system dynamic range. Using this combination of packaging techniques and designs, we finally realized the first fully packaged 4-channel receiver and fully-packaged 2-channel transmitter phased arrays. We performed wireless data transmission experiments over 25 cm air using one channel of these transceiver boards. We observed clean and open eye patterns up to 5 GBaud data rate in this data transmission experiment. In addition, a BER of less than 10^{-3} up to 2.5 GBaud data rate is achieved in the same data transmission experiment.

Moreover, beamforming capability both in the transmitter and receiver is presented through collaboration with Samsung Research America, utilizing their baseband board. Some working boards have been sent to Samsung Research America to further explore the single and multi-beam wireless communication capabilities with their baseband processor. These boards demonstrate the possibility of the low-cost phased array realization using printed circuit board technology. The concept can be extended to create arrays with more elements, and therefore systems at 140 GHz with a range of more than 100 meters can be developed. Moreover, using separate transmitters, multiple independent beams

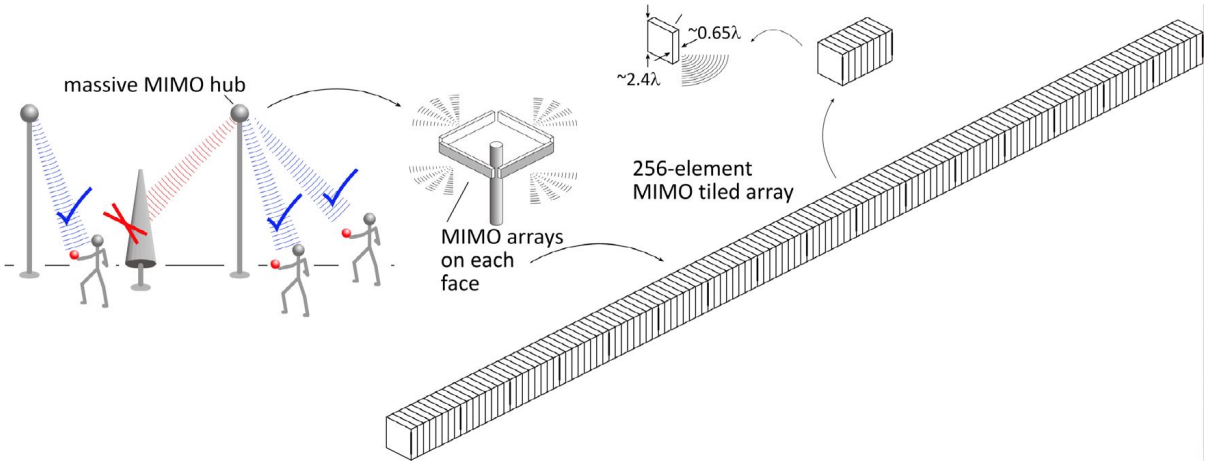

Figure 8.1: Massive MIMO Hub: Vision to realize bigger than 1 Tb/s wireless links using massive number of beams (*Courtesy of Prof. Mark J. W. Rodwell*)

can be transmitted using these boards, and true MIMO operation and capacity gain can be proven.

The work presented here has built the foundation of a larger goal to demonstrate multi-beam phased arrays with a massive number of independent beams. We demonstrated the first prototype with fully packaged phased array transceivers working above 140 GHz. This work should be followed by further experiments to demonstrate multi-beam operation using different transmitters as an initial step. Later, a new generation of 22 nm FDSOI transceivers should be integrated with antennas to further improve the system performance. New generation chips don't have limiters at the transmitter inputs, therefore they can support multi-beam operation in a phased array configuration. Using the proposed next generation packaging ideas, the first 8-element module including 22FDX transceivers, LTCC based antennas and high performance III-V amplifiers needs to be created. This module can then be easily tiled to realize arrays with a massive number of elements. In this way, we can create a system shown in the Fig. 8.1, where massive MIMO arrays on a light bulb can be realized with 256 elements per face, and 1024 elements in total. Using a 2:1 loading factor, this system can support 128 beams

per face, and 512 beams total. If each elements support only 1 Gb/s data rate, then we can create a MIMO hub supporting a total of 0.5 Tb/s data rate. If each element can support 10 Gb/s, then we can realize a total data rate of 5 Tb/s. This means we can have wireless links at fiber speeds. This will be the next era in wireless communications - perhaps the 6G.

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