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ABSTRACT

Presented is a design for a solid-state amplifier with the following characteristics:

- Voltage gain: 3 to 10, continuously adjustable.
- Rise time: 10 to 90%, 3 nsec.
- Output range: +1.5 to -1.5 volts, in a 50-ohm system.
- Impedance: 50-ohm matched input, emitter-follower output.

Broadband design techniques are used throughout so that no tuning is required.
A SOLID-STATE AMPLIFIER WITH A 3-NANOSECOND RISE TIME

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A solid-state amplifier has been developed at the Lawrence Radiation Laboratory for amplifying nanosecond pulses used in nuclear particle detection systems (see ref. 1). The amplifier has a 10-to-90% rise time of 3 nsec, an insertion voltage gain continuously adjustable from 3 to 10, and an output swing of +1.5 volts to -1.5 volts operating in a 50-ohm system. The overload characteristics are good, exhibiting no double pulsing and having a recovery time of a few nanoseconds. The linearity in gain over the maximum output swing is within 5%. The circuit is shown in Fig. 1. Front and side views of the instrument are shown in Figs. 2 and 3.

The first two transistors are common-base amplifiers, Q1 being used to provide a matched input to an arbitrary impedance Z0 of the input cable. A potentiometer in the collector circuit of Q1 provides a resistive division of the collector signal current between ground and the input of the second common-base stage. The ratio of current that enters the very-low-impedance common-base input of Q2 is continuously adjustable from a maximum of about 0.9 (≈ \frac{70}{70 + r_e}) to 0.3 (≈ \frac{20}{70 + r_e}), or a range of about 3 to 1. The emitter resistance is about 3 ohms maximum (r_e). The sizes of the potentiometer (50 ohms) and the resistor in series with it (20 ohms) are determined by the amount of loss at the high-gain position that can be tolerated, and by the degradation in rise time produced when the potentiometer is in midposition. When the potentiometer is set for one-half maximum gain, the resistance to ground on the collector of Q1 is at a maximum, \frac{(70 + r_e)}{4}, or about 20 ohms.
This resistance, along with the output capacity of $Q_1$, determines the minimum bandwidth of the gain-control stage, since the bandwidth decreases as resistance increases. Even though preceded by this gain-control stage, the 3-nsec rise time of the remainder of the circuit showed no appreciable degradation.

From the collector of $Q_2$ the signal is amplified by two cascaded feedback stages ($Q_3, Q_4$). The design of these stages follows the procedure of Ghausi and Pederson to obtain approximately a maximally flat magnitude response (see ref. 2).

The low-frequency gain, per stage, is given by:

$$A(0) = \frac{1}{R_b + \left( \frac{R_f + r_b'}{R_f} \right) \left( \frac{R_f + R_b}{R_f} \right) \frac{1}{\beta_0}}$$

or approximately $R_f/R_b$, when $\beta_0$ is large. The gain-bandwidth product is approximately the $f_i$ of the transistor (the frequency at which the common emitter current gain, with a short-circuit load, is equal to unity). $R_b$ is the resistance in the collector that is bypassed by the small trimmer capacitance. The optimum value of this resistance is between 100 and 300 ohms, according to ref. 2. $R_f$ is the feedback resistance from collector to base. $R_i + r_b'$ is the low-frequency input impedance of a common emitter stage, where $r_b'$ is the extrinsic base resistance. We then have

$$R_i = \beta_0 r_e = \beta_0 \frac{0.026}{I_e},$$

where $I_e$ is the emitter bias current, and $\beta_0$ is the low-frequency current gain of the common emitter circuit with a short-circuit load.

The value of the small capacitance bypassing $R_b$ is quickly found experimentally by observing the pulse response on an oscilloscope with a mercury-switch pulse generator for a source. The output rise time is minimized by varying the size of the capacitance while maintaining a reasonable amount of
pulse fidelity. This technique of broadband design has been compared with shunt-peaked interstage networks and with inductively coupled feedback networks, and found superior to both.

The dynamic range of the amplifier is determined by the second of these two stages for negative input pulses. The feedback is strong enough that with a 15-mA bias collector current only about 7 mA is switched into the load when the transistor is cut off. The remainder is used up in the feedback resistor to satisfy the voltage drop across it. This low economy of output swing requires excessively large bias currents in the second feedback stage \( Q_4 \) to obtain a normal limiting action in the output transistor \( Q_7 \). Germanium transistors (2N1143) were chosen for feedback stages \( Q_3 \) and \( Q_4 \) because of their good high-frequency characteristics. Limiting the junction temperature to a maximum of 75 °C, for an ambient of 50 °C, has ensured reasonable reliability. The dissipation is thus limited to about 75 milliwatts. This dissipation limit, in conjunction with the optimum biasing conditions for maximum gain-bandwidth figure \( f_v \), limits the dynamic range to an output of -1.5 volts. For symmetry, the positive excursion is also limited by diodes to this magnitude.

Another common-base amplifier, \( Q_5 \), follows the feedback stages. A common-base stage is preferred here to provide a low-impedance load to the feedback stage of \( Q_4 \). This stage then acts as a voltage amplifier driving the relatively high-input impedance of a shunt-compensated Darlington pair; \( Q_6 \) (N709) and \( Q_7 \) (MM487 or 2N2218). The common-base stage gives voltage gain by raising the impedance level of the signal while maintaining the current level. The Darlington pair maintains that voltage level while lowering the circuit impedance level to a load value of 50 ohms; thus a current gain is realized. Because of the emitter-follower output, the output impedance of the amplifier is quite low (about 30 ohms at 100 Mc). The use of the small shunt inductance on the collector of \( Q_5 \) improves the rise time of the output by approximately 1 nsec.
To obtain a good overload characteristic, series-diode-current clamping was used between $Q_2$ and $Q_3$. The diodes are QUTRONIC's Q6-100, fast-switching low-impedance germanium diodes. This point in the circuit was used because of the low-input impedance of the feedback state $Q_3$; thus the added shunt capacitance effects were minimal. A diode clamp was also employed at input $Q_1$, to avoid the reflections that occur when $Q_1$ is cut off by excessively large positive signals at the input, thus losing input termination.

To obtain the best performance as a pulse amplifier, the output is adjusted for approximately 10% overshoot for a step input. (A maximally flat magnitude adjustment would result in a 4% overshoot.) With this amount of overshoot for an ideal step-function input, approximated by a mercury pulser input, the output with an input-signal rise time of a few nanoseconds will have an optimum response (fast, with no overshoot). This results because the input time constant is included with the time constants of the amplifier circuitry, when computing the time response of the output signal.

The amplifier has relatively good stability despite changes in $\beta_0$ of the transistors resulting from aging, temperature changes, or the initial variation of parameters within a manufactured lot. The common-base and common-collector circuits have good inherent stability with changes in $\beta_0$ or temperature. The feedback around stages $Q_3$ and $Q_4$ tends to reduce gain drifts in these stages, the feedback factor given by the ratio of the open-loop gain to the closed-loop gain being about 10 to 1.
FOOTNOTES AND REFERENCES

*This work was done under the auspices of the U. S. Atomic Energy Commission.

1. Lawrence Radiation Laboratory, Pulse Amplifier Model 10-03NS
   (dwg. 4X9062).

2. M. S. Ghausi and D. O. Pederson, "A New Feedback Broadbanding
   Technique for Transistor Amplifiers," University of California ERL
FIGURE LEGENDS

Fig. 1. Schematic diagram: Model 10-03NS pulse amplifier. All capacitors are 6.8 μF/30 V dry tantalum. At all points where supply voltages are shown, additional capacitors have been provided as needed for accurate bypassing. All leads are kept as short as possible. Q7 is mounted in a low-capacitance heat sink. All resistors are 1/2 W, unless noted otherwise.

Fig. 2. Panel view of the 10-03NS pulse amplifier.

Fig. 3. Side view of the 10-03NS pulse amplifier, showing details of construction.

Fig. 4. Waveforms.
Fig. 1
Fig. 2
Fig. 4