Title

Interpreting Kelvin probe force microscopy under an applied electric field: local electronic behavior of vapor—liquid—solid Si nanowires

Journal

Nanotechnology, 24(20)

ISSN

0957-4484

Authors

Quitoriano, Nathaniel J

Sanderson, Robert N

Bae, Sung-Soo

et al.

Publication Date

2013-05-24

DOI

10.1088/0957-4484/24/20/205704

Nanotechnology **24** (2013) 205704 (8pp) doi:10.1088/0957-4484/24/20/205704

Interpreting Kelvin probe force microscopy under an applied electric field: local electronic behavior of vapor–liquid–solid Si nanowires

Nathaniel J Quitoriano[1], Robert N Sanderson[2,3], Sung-Soo Bae[3] and Regina Ragan[3]

[1] Department of Mining and Materials Engineering, McGill University, Montreal, H3A 2B2, Canada
[2] Department of Physics and Astronomy, University of California, Irvine, Irvine, CA 92697, USA
[3] Department of Chemical Engineering and Materials Science, University of California, Irvine, Irvine, CA 92697, USA

E-mail: rragan@uci.edu

Received 30 December 2012, in final form 26 March 2013
Published 23 April 2013
Online at stacks.iop.org/Nano/24/205704

Abstract
Kelvin probe force microscopy (KPFM) is used to characterize the electrical characteristics of vapor–liquid–solid (VLS) Si nanowires (NWs) that are grown in-place between two predefined electrodes. KPFM measurements are performed under an applied bias. Besides contact potential differences due to differing materials, the two other primary contributions to measured variations on Si NWs between electrodes are: trapped charges at interfaces, and the parallel and serial capacitance, which are accounted for with voltage normalization and oxide normalization. These two normalization processes alongside finite-element-method simulations are necessary to characterize the bias-dependent response of Si NWs. After applying both normalization methods on open-circuit NWs, which results in a baseline of zero, we conclude that we have accounted for all the major contributions to CPDs and we can isolate effects due to applied bias such as impurity states and charged carrier flow, as well as find open connections when NWs are connected in parallel. These characterization and normalization methods can also be used to determine that the specific contact resistance of electrodes to the NWs is on the order of $\mu\Omega$ cm^2. Thus, the VLS growth method between predefined electrodes overcomes the challenge of making low-resistance contacts to nanoscale systems. Thereby, the experiments and analysis presented outline a systematic method for characterizing nanowires in parallel arrays under device operation conditions.

(Some figures may appear in colour only in the online journal)

1. Introduction

Semiconductor nanowires (NWs), since the first demonstration of vapor–liquid–solid (VLS) growth almost 50 years ago [1], have shown remarkable progress in the control of their growth parameters and have received much attention in applications, for example as specialty, field-effect transistors [2]. In addition, self-assembled parallel arrays of nanowires have applications in thermoelectric devices [3], complementary inverters [4] and interdigitated electrodes for electrochemical based detection in sensors [5]. Improved metrology is needed to guide the synthesis of emerging research materials in the semiconductor roadmap [2] and for the many emerging low-cost applications [3–5]. Here we utilize a directed self-assembly process that allows the control of horizontal, planar growth of VLS Si NWs. The

current–voltage response of these Si NWs has previously been characterized in top-gated, metal-oxide–semiconductor field-effect transistors (MOSFETs) [6], and here we examine the nanoscale electronic environment.

Kelvin probe force microscopy (KPFM) measures the local electronic properties of nanoscale systems and is particularly useful for investigating the local electronic behavior of nanoscale systems connected in parallel, since current–voltage measurements only probe collective behavior. KPFM is a scanning probe characterization method that measures the contact potential difference (CPD) between a sample and a probe tip and is typically conducted alongside atomic force microscopy (AFM) measurements in order to facilitate the understanding between surface structure and measured CPD. CPD is the difference between the work function of the probe tip and a conductive sample surface and is defined as:

$$\mathrm{CPD} = \frac{\varphi_{\mathrm{tip}} - \varphi_{\mathrm{sample}}}{-e} = -\delta v \tag{1}$$

where e is the elementary charge, ϕ_{tip} and ϕ_{sample} are the work functions of the tip and sample, respectively, and δv is the applied external voltage. KPFM measures the electrostatic force between the probe tip and the surface to characterize the CPD. The force due to the separation-dependent capacitance and potential between the tip and the sample [7] is given by:

$$F = -\frac{V^2}{2}\frac{\partial C}{\partial z} \tag{2}$$

where the potential, capacitance and distance between the probe tip and sample surface are V, C, and z, respectively. On the first trace, a non-contact AFM topography is acquired in our ambient system. On the retrace, acquired at constant tip–sample distance, KPFM maps the CPD between the sample surface and the probe tip by applying a small signal voltage (δv) on top of a time-varying bias (δV) at frequency ω on the tip. During KPFM, the small signal δv is varied to minimize the force between the probe tip and sample surface, and sampled at a frequency ω. The voltage, δv, at which the minimum force is measured is equal to the CPD between the substrate and probe tip, which is measured using a lock-in technique.

The CPD can be understood by considering two materials that are electrically isolated from one another, where their vacuum levels match but their Fermi energies typically do not (i.e. when the materials' work functions differ). When one electrically connects these two materials, electrons will flow from the material with a higher Fermi energy to the lower Fermi-energy material until an electric field is established to create a constant Fermi level across the two materials, thus reaching equilibrium. The CPD between the sample and the probe tip can be viewed in a number of ways. Practically, it is the potential difference required to prevent the flow of electrons between the probe tip and the sample surface to maintain equilibrium when the probe and sample are electrically connected. However, it can also be viewed as the difference between the Fermi energies of the two materials, which is affected by the intrinsic Fermi energy, impurities and local surface charges [8, 9]. In the case of non-conductive surfaces and samples in ambient conditions, KPFM will also measure the surface charge between the tip and the underlying, conductive substrate [10].

The analysis may appear straightforward, yet parallel capacitance between the sample background and local surface structure, a so-called averaging or weighting effect [11, 12], and serial capacitance [8] due to induced surface charge and/or passivating layers on semiconductor surfaces in device structures influence KPFM measurements, particularly on nanoscale features. These effects make the interpretation of raw KPFM images difficult. While KPFM has been used to characterize surface defects in semiconductors [9, 13], the surface electronic structure of model bimetallic nanocatalysts [14], and semiconductor nanowires (NWs) [15, 16], measurements are typically performed in ultrahigh vacuum and/or controlled environments. Few measurements are performed in conditions of device operation and/or on passivated material device structures [17–20].

Moreover, few papers discuss KPFM measurements with an applied voltage across the material to be characterized (other than the voltage between the sample and probe), see for example [19–22]. Recently, we have applied this technique to characterize local defect states in Si NWs fabricated by etching the top, Si (device) layer of a silicon-on-insulator (SOI) substrate and compared the results with Si NWs produced using the vapor–liquid–solid (VLS), catalyzed-growth process to understand the relationship between processing conditions and surface electronic structure in device architectures [20]. Here, we use KPFM to characterize VLS semiconductor NWs that were grown, in-place, against a silicon dioxide surface, between two Si electrodes with different applied voltages across them. We find that two normalization procedures are needed for data interpretation: (1) normalizing the measured CPD data across biased NWs with respect to CPD data across NWs with no bias and (2) normalizing the measured CPD data across NWs under an applied bias with respect to CPD data acquired adjacent to the NW at the same bias. We refer to the former as voltage-normalized surface potential and to the latter as oxide-normalized surface potential. We describe these normalization procedures and use them to estimate the contact resistance of the NWs as well as determine if the NW has made good contact with both electrodes.

2. Experimental procedures

The semiconductor NW devices were made using a combination of top-down and bottom-up procedures. The Si contact electrodes were defined and fabricated using a top-down procedure on a (001)-oriented, SOI substrate. The 100 nm-thick, n-type ($\sim 10^{19}$ cm^{-3} phosphorus), Si electrodes were isolated from one another by etching through the top (device layer) Si and stopping at the underlying SiO_2. Nominally undoped Si NWs were grown between these two electrodes by guiding the NW growth against the SiO_2 using a bottom-up approach. Au colloids were deposited somewhat selectively onto the exposed Si surfaces, the underside of the

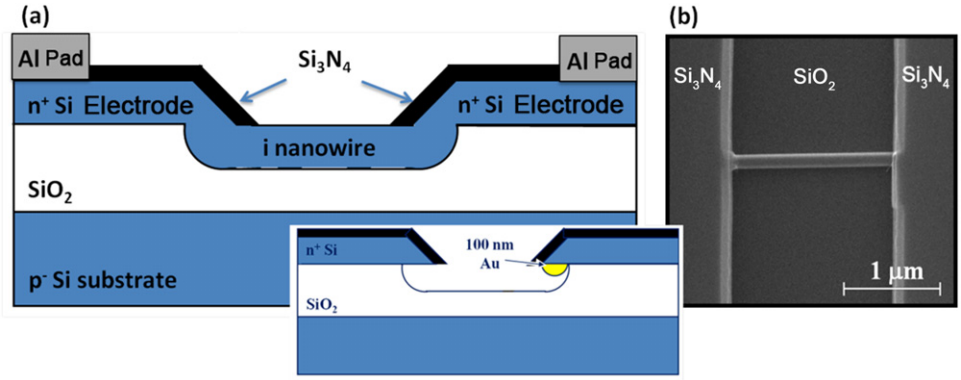

Figure 1. (a) Schematic cross-section of a VLS NW grown between two electrodes taken through the NW which connects the two electrodes. (Inset) Schematic of the NW fabrication process, using Au particles to catalyze NW growth. (b) Plan-view SEM image of the two electrodes passivated with Si_3N_4 connected by a NW that was grown in between and electrically connects the two pads.

Si device layer (see the inset in figure 1(a)). These Au particles acted as catalysts for Si NW growth and the NWs grew between the two Si contact electrodes to electrically connect them. Figure 1 shows a schematic cross-section taken through the NW and a plan-view scanning-electron-microscope (SEM) image. The details of the NW fabrication procedure are published elsewhere [6, 23] and these devices were essentially the same as those described in [6], though without the top metal gate deposited on the NW and with a ∼3 nm, dry thermal oxidation process, SiO_2.

The samples were then scanned using AFM and KPFM to gather both the height and CPD information using the described two-pass technique. The samples had varying voltages across the electrodes from 0 to 1 V in 0.25 V intervals. AFM and KPFM measurements were performed using an Asylum Research AFM system, MFP-3D. The measurements were obtained in an air ambient at room temperature with a scan rate of 0.3 Hz to allow for adequate controller response time [24]. Commercial Si AFM tips (Olympus AC-160TS) were coated with approximately 3 nm of Cr using an Ar sputtering system (IBS, Southbay Technology) to obtain a conducting tip for KPFM analysis. The resonance frequency of the AFM tips was measured to be in the range 310–320 kHz and their spring constant was listed as 42 N m^{-1}. KPFM data was acquired in amplitude modulation mode. An AC voltage, δV, of 3 V is applied to the tip at the first resonance of the cantilever. A lock-in technique is used to measure the applied DC voltage, δv, needed to minimize the electrostatic force between probe tip and sample surfaces, which is monitored at the first resonance frequency of the cantilever oscillation.

The NW systems were modeled using finite-element-method (FEM) simulations to lend an understanding to the KPFM studies. The geometry of figure 1 was modeled with accepted values for the conductivity and permittivity being used for Si, SiO_2, and Si_3N_4. The SPM tip was modeled as a conical frustum with a semi-angle of 15° capped with a spherical tip of radius 9 nm. The simulations solved Laplace's equation $\nabla^2\varphi = 0$ and gave the electric potential distribution in three dimensions. The electric field was calculated using $E = -\nabla\varphi$, and the electrostatic force on the SPM tip was calculated by integrating the Maxwell stress tensor over the tip's surface area. CPD measurements were simulated by iterating for a number of tip biases and fitting the results to find the tip bias that minimizes the z-component of the force on the SPM tip, as is done in KPFM experiments to determine the CPD.

3. Results and discussion

Figure 2 shows AFM (figure 2(a)) and CPD (figures 2(b) and (c) with $V_{AB} = 0$ V and 1 V, respectively) images, scanned at an approximate 45° angle to capture all abrupt topographic variations, for Si NWs fabricated as depicted in figure 1. In figure 2(c), electrode B in the upper left has a lower potential than electrode A in the lower right, this is because there is an applied bias ($V_{AB} = V_A - V_B = 1$ V) between the electrodes. As illustrated in figure 1, when the NW bridges the gap between the two electrodes and a bias is placed across those two electrodes, then current will flow. From figures 2(a) and (b), NW1 is observed to have grown over the side of electrode A.

Line profiles were taken across the NWs between electrode A and electrode B at different voltages, V_{AB}, along the black lines indicated in figure 2(c). Figure 3(a) shows the resulting CPD line profiles for voltages, V_{AB}, from 0 to 1 V in 0.25 V intervals for NW2. The regions on the line profiles corresponding to the NW are highlighted with arrows. As can be seen in figure 3(a), all of the CPD line profiles have a similar shape. For example, in figure 3(a), the curve corresponding to $V_{AB} = 0$ V has significant CPD variations as a function of position, related to surface charges, differing materials, etc, which are not related to an applied voltage across the NW.

One of the dominant features of all these CPD profiles is the increase in CPD values near the interfaces between the NW and the electrodes. These features are also observed in the line profile of NW1, shown in figure 3(c), with some slight variations where NW1 climbs over the side of electrode A. This CPD increase seen in the line profiles of figures 3(a) and (c) near the NW2/electrode A–B and NW1/electrode A interfaces could occur due to differing doping densities [25],

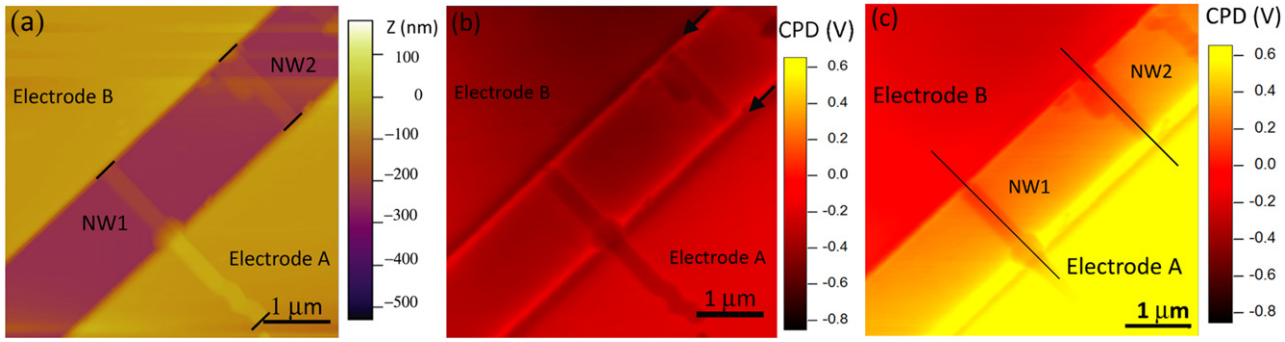

Figure 2. (a) AFM and (b) CPD images at $V_{AB} = 0$ and (c) at $V_{AB} = 1$ V of bridging NWs between electrodes A, lower right, and B, upper left. Lines in (a) highlight the ends of the NWs. Arrows in (b) point to the edge of the electrode. Electrode A is at a higher potential than electrode B in (c). The CPD voltage key for both (b) and (c) is shown on the right of (c).

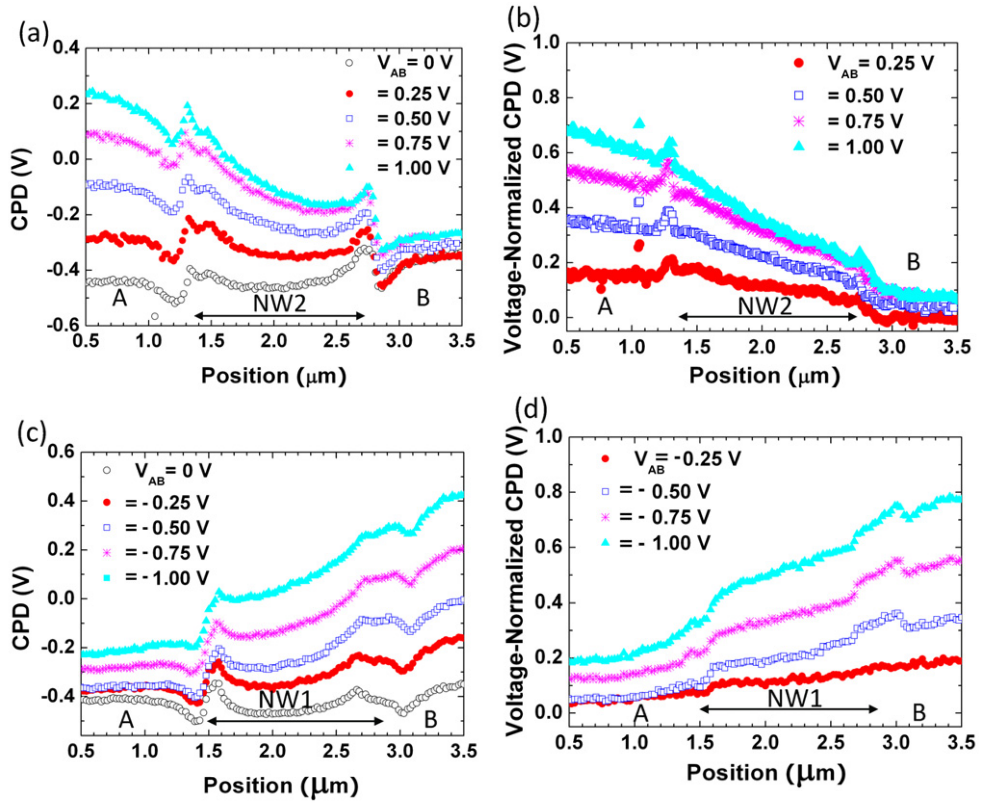

Figure 3. CPD line profiles at different applied voltages across (a) NW2 and (c) NW1, as labeled in figure 2(a). Electrode B corresponds to the electrical contact in the upper left corner of figure 2(a). (b) and (d) Voltage-normalized CPD line profiles obtained by subtracting the $V_{AB} = 0$ V line profile from the others in (a): profile for NW2 in (b) and NW1 in (d).

occupied surface states [26], and height variations between the NW and the electrodes.

To isolate and better understand the effect of the applied voltage on the CPD profiles, the line scan corresponding to $V_{AB} = 0$ V was subtracted from the other line scans [22, 27, 28], ($V_{AB} = \pm 0.25, \pm 0.50, \pm 0.75$ and ± 1 V), and the resulting data are shown in figures 3(b) and (d); we refer to this process as voltage normalization. The line profiles are quite smooth, except for some jumps in the CPD for one or two data points near the interfaces, corresponding to small misalignments in the line scan data taken across multiple scans. (Since the normalization process requires taking scans and subtracting them, anomalies can result from subtracting one from another when they are not exactly aligned.) Besides these anomalies, the voltage-normalized CPD increases nearly linearly with increasing V_{AB}, with a small change in slope between NW2 and electrode B near the 2.8 μm position, and a CPD increase at the 1.3 μm position. Both of these features exhibit a small bias dependence and have several data points associated with them, thus they do not represent normalization artifacts due to misalignment of data subtraction.

First we consider the linear current–voltage response along the NWs in the data of figures 3(b) and (d). The linear potential drop across the NWs is 70%–80% of the

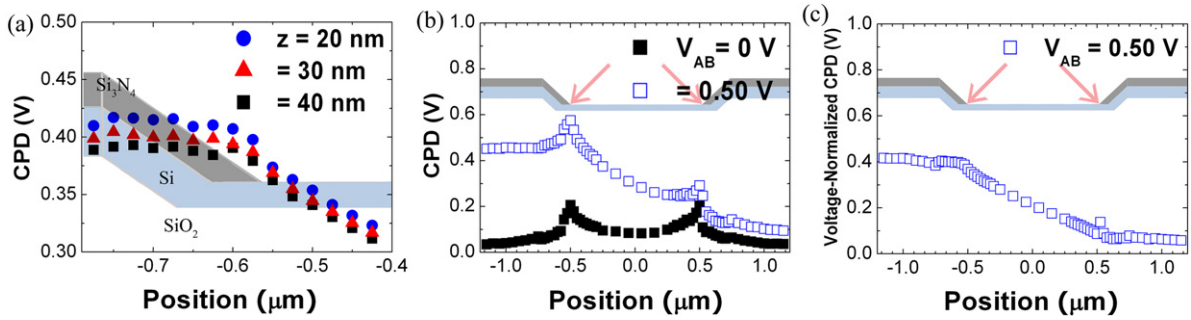

Figure 4. (a) Simulated CPD line profiles near the positive electrode, held at +0.50 V above the grounded electrode ($V_{AB} = 0.50$ V), for various tip–sample separations, where z is taken to be the vertical distance between the lowest point of the SPM tip and the sample. (b) Simulated CPD line profiles across a NW with positive interface charges inserted at the lowest point of the Si_3N_4 ramp (indicated with arrows). (c) Voltage-normalized CPD line profile, obtained by taking the difference between the two data sets in (b) point-by-point.

applied bias; this behavior was reproducibly observed in the many measured NWs. Parallel capacitance contributions from the neighboring positive electrode are known to increase the CPD measured at the grounded electrode, leading to a smaller potential drop in the applied bias [11, 12]. The linear, current–voltage (Ohmic) response that was measured, in spite of the large differences in doping between the NW and electrodes, can be understood when considering the NW surface states. Though the Si NWs have not been intentionally doped, a positive surface charge density between the NW and the 3 nm thermal SiO_2, on the order of 10^{12} cm^{-2}, leads to an accumulation of electrons in the NW [29]. For a similar device [6] in a metal-oxide–semiconductor, field-effect transistor configuration, an appreciable current was measured with a zero gate voltage, indicating that the NW is lightly n-type due to its surface states. Therefore, the near linear CPD response with applied V_{AB} is reasonable since the NW acts as a resistor with a decreased cross-section and a decreased (effective) doping density.

We now examine the CPD increases at the NW–electrode interfaces, e.g. at the 1.3 μm position in figure 3(a) and the 1.5 μm position in figure 3(c). An increase in CPD would be consistent with the accumulation of positive charge at the interface, which could be due to interface states at SiO_2 and Si_3N_4 junctions. It is also possible that positively-charged surface states on Si NWs 29 would not be compensated by electrons in the undoped NWs near the depletion region; yet it would not be expected that such features would be symmetric as observed in the experimental data. The CPD increase, on the other hand, may also be associated with the tip–electrode separation. FEM simulations were utilized to lend further understanding to the results shown in figure 3. The CPD increases seen near the NW2/electrode A–B and NW1/electrode A interfaces might be interpreted as measurement anomalies caused by the steep geometry of the nanowire trench ramp. AFM does not track the surface topography of a sample perfectly, and at steep topographical features the measured surface topography is distorted, causing downward slopes to become less pronounced [30]. It is thus possible that in figure 3 the probe tip was not properly tracking the sample surface at both ends of the SiO_2 trench, and was in fact further from the sample surface at this point relative to others. To investigate the plausibility of this explanation, FEM simulations were conducted for various tip–sample separations. The FEM simulations used in this work modeled the KPFM tip (Olympus AC-160TS) as a sphere of radius 9 nm joined to the end of a right conical frustum, 11 μm tall, with an opening angle of 15°. Figure 4(a) shows simulated CPD line profiles near the higher potential electrode, which is held 0.50 V above the drain, which is held at ground. It is seen that an increased tip–sample separation causes a decrease in the detected CPD, rather than the increase seen in the experimental data. Figure 4(a) is the result of a series of FEM simulations for varying tip–sample separations and generally shows that decreasing the separation does lead to a CPD increase. Yet it was found in the FEM simulations that even if the tip–sample separation is halved, the corresponding CPD increase is ~30 mV; much less than the ~150 mV CPD increases seen in the experimental data. These results thereby show that the CPD increase near the edge of the electrodes is not primarily due to the sample geometry.

In order to examine if interface states give rise to the CPD increase, FEM simulations were also performed with a positive charge along the NW–electrode (SiO_2/Si_3N_4) interface, as indicated with arrows in the cross-sectional diagram inlaid in figure 4(b). It is seen in figure 4(b) that the CPD increases in FEM simulations are present at the same location and are of equal magnitude to those in the experimental results in figure 3. Thus, FEM simulations indicate that it is not the sample geometry but rather the SiO_2/Si_3N_4 interface states that lead to the CPD increase. Moreover, when the CPD line profile taken with an applied voltage $V_{AB} = 0$ V is subtracted from the line profile for $V_{AB} = 0.50$ V, shown in figure 4(c), we obtain a normalized CPD line profile with a linear drop along the NW. The large increase in CPD at NW–electrode interfaces is not observed in the voltage-normalized simulated curves, similar to the experimental voltage-normalized data. Also in agreement with experimental results, the voltage-normalized simulated data has a smaller potential drop than the applied bias across electrodes. The parallel capacitance between the probe and the neighboring high potential electrode raises the measured CPD at the grounded electrode. Voltage normalization is thus demonstrated to be valid in-principle for understanding the

CPD response due to an applied bias and the resulting charge transport.

A CPD drop is observed in figure 3(b), near 2.8 μm, at the NW2–electrode B junction that is not observed in the simulated voltage-normalized curves. This change in the CPD at NW–electrode interface increases with increased applied bias, indicating that it is correlated with contact resistance, since FEM simulations do not include contact resistance. Using the voltage-normalized data and the measured current as a function of applied bias, the contact resistance, $R = \Delta\text{CPD}(V)/I$, was estimated between the NW and the electrodes from this feature at 2.8 μm. Note that there are several NWs between electrodes A and B; consequently, current can pass through multiple NWs. Thus-extracted contact resistances from the potential drops at the NW2–electrode interfaces can only provide minimum values for contact resistances; the actual contact resistance is somewhat higher since the current through NW2 is somewhat lower than the total current. Due to a CPD spike in the voltage-normalized data near the high-potential electrode (e.g. electrode A in figures 2(c) and 3(b)), the contact resistance was thus only determined at the NW–low-potential contact. For example, when the bias was reversed, we observed a similar CPD peak at the NW1–electrode B interface (the opposite electrode from figure 3(b) due to reversal of the bias). Thus in order to evaluate the contact resistance at both NW interfaces, the bias across the NW was reversed, thus reversing the location of the CPD spike and enabling the determination of the contact resistance on both sides of the NW. The measured potential drops, 'ΔCPD: $V_{AB} > 0$ V' and 'ΔCPD: $V_{AB} < 0$ V', at the NW2–electrode B and NW2–electrode A interface, respectively, are listed in table 1 as a function of applied bias, V_{AB}. Each value in the table corresponds to a single representative measurement. The applied bias is listed in the first row and the measured current across the electrodes in response to the listed V_{AB} is listed in the second row. The contact resistance ($\Delta\text{CPD}(V)/I$) is estimated as 3.7 kΩ at the NW2–electrode B interface when $V_{AB} > 0$ V and 3.5 kΩ at the NW2–electrode A interface when $V_{AB} < 0$ V. These values are basically the same within experimental error. Assuming the NW diameter of 240 nm, as determined from the full-width at half-maximum in topography line profiles, the specific resistance is estimated as 1.6 ± 0.3 ($1\sigma, n = 8$) $\mu\Omega$ cm^2. Note that there are eight independent measurements in table 1 to estimate the contact resistance, and the 19% standard deviation is consistent with some electrostatic screening of the surface potential due to the thin SiO_2 layer on the surface. Nevertheless, this determined specific resistance is consistent with that reported for a single VLS NW, 4.4 ± 0.6 $\mu\Omega$ cm^2, grown in a similar manner to span two electrodes [31]. Furthermore, SEM images typically show less than 8 NWs across the electrodes. Thus the contact resistance is still estimated to be very low ($\leq$10 $\mu\Omega$ cm^2) even when considering there are other NWs in parallel. In comparison, the contact resistance for Ti/Au contacts to p-type Si NWs was reported as 500 $\mu\Omega$ cm^2 [32]. The low contact resistance in the VLS Si NWs studied here is in agreement with a previously measured, nearly ideal, current response (low contact resistance) as a function of applied gate voltage for devices fabricated using the same fabrication protocol [6, 23].

Table 1. Current–voltage response and associated CPD variation at NW2–electrode interfaces.

$\lvert V_{AB}\rvert$ (V):	0.25	0.50	0.75	1.00
Current (μA):	11	25	41	55
ΔCPD (mV): ($V_{AB} < 0$ V)	50	80	120	180
ΔCPD (mV): ($V_{AB} > 0$ V)	70	95	125	135

Figure 3 shows a clear trend between the CPD responses across the NW as a function of different applied voltages after voltage normalization. When examining similar data across a Si NW that is not connected to both electrodes there is a similar CPD response before normalization, as can be seen in figure 5(a). Figure 5(b) shows the voltage-normalized CPD line profiles for this NW; the corresponding 3 μm $\times$ 3 μm KPFM image acquired at $V_{AB} = 1$ V is shown in figure 5(d). Surprisingly, the line profiles do not exhibit significant differences from those depicted in figure 3(b); the CPD across the disconnected NW versus voltage is slightly nonlinear after voltage normalization, whereas the CPD across the connected NWs of figures 3(b) and (d) are not. However, the differences are not obvious. In figure 5(e), the CPD response of the SiO_2 trench under an applied bias is shown. The CPD increases seen on both sides of the NW trench are still present here, where there is no NW. First, this data shows that the interface states that are responsible for this behavior are therefore not dependent on the NW–electrode interface, but rather on the SiO_2 trench-Si_3N_4 covered electrode interface. This can be explained as trapped charge at the Si_3N_4–SiO_2 interfaces, which have been studied in depth for their charge storage properties [33]. Upon voltage normalization, there is a similar nonlinear response of the SiO_2 trench as observed for the disconnected NW. Voltage-normalized data for the SiO_2 trench is shown in figure 5(f). It has been observed previously, when examining CPD data across NWs that are not electrically connected [20], that unconnected NWs also have a similar CPD response after voltage normalization to that of the SiO_2 trench.

The differences in physical connections of the NWs of figure 3 versus figure 5 suggest there should be a way to clearly differentiate the two NWs and their surface potential responses when there is an applied bias across them. We find that only when the CPD line profiles are normalized by subtracting the voltage-normalized SiO_2 CPD, e.g. at $V_{AB} = 1$ V, across the neighboring oxide trench from the voltage-normalized CPD taken across the NW at the same voltage, e.g. at $V_{AB} = 1$ V, can we distinguish between the connected and disconnected NWs. This procedure is referred to as oxide normalization. (The oxide-normalized CPD thus has two normalization procedures—first voltage normalization followed by oxide normalization.) The oxide-normalized, CPD line profiles for the disconnected NW are shown in figure 5(c). After oxide normalization the CPD response versus voltage is approximately zero across the NW. The only exception is the decrease in CPD associated

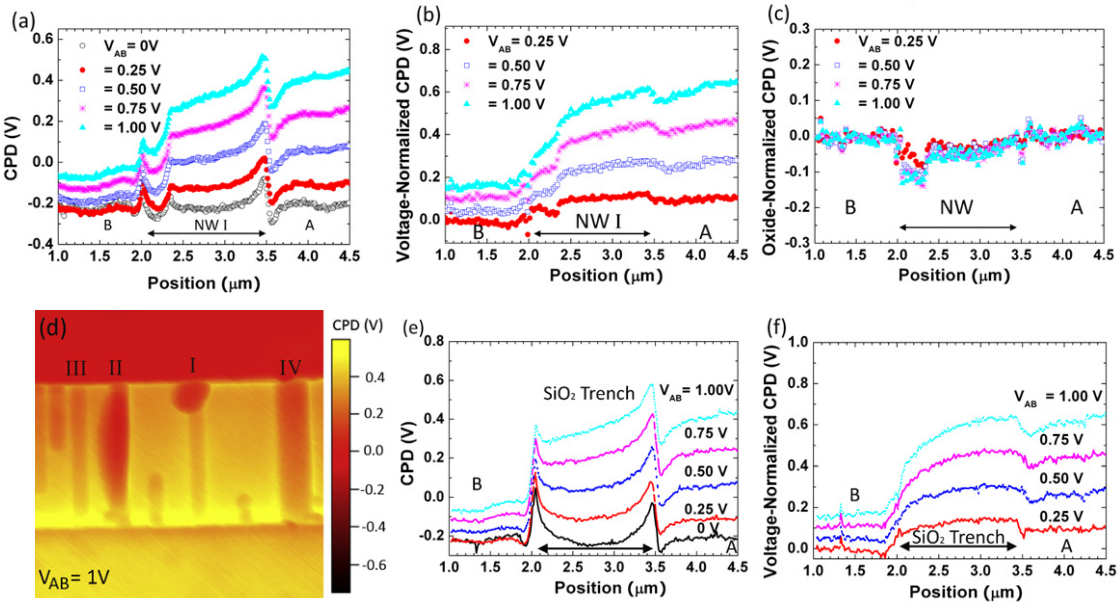

Figure 5. CPD line profiles at different applied voltages across (a) an unconnected Si NW. (b) Voltage-normalized CPD line profile and (c) oxide-normalized CPD data for the same NW labeled I in the 3 μm $\times$ 3 μm KPFM image acquired at $V_{AB} = 1$ V shown in (d). (e) CPD line profiles at different applied voltages across the SiO_2 trench adjacent to NW. (f) Voltage-normalized CPD line profiles for the SiO_2 trench.

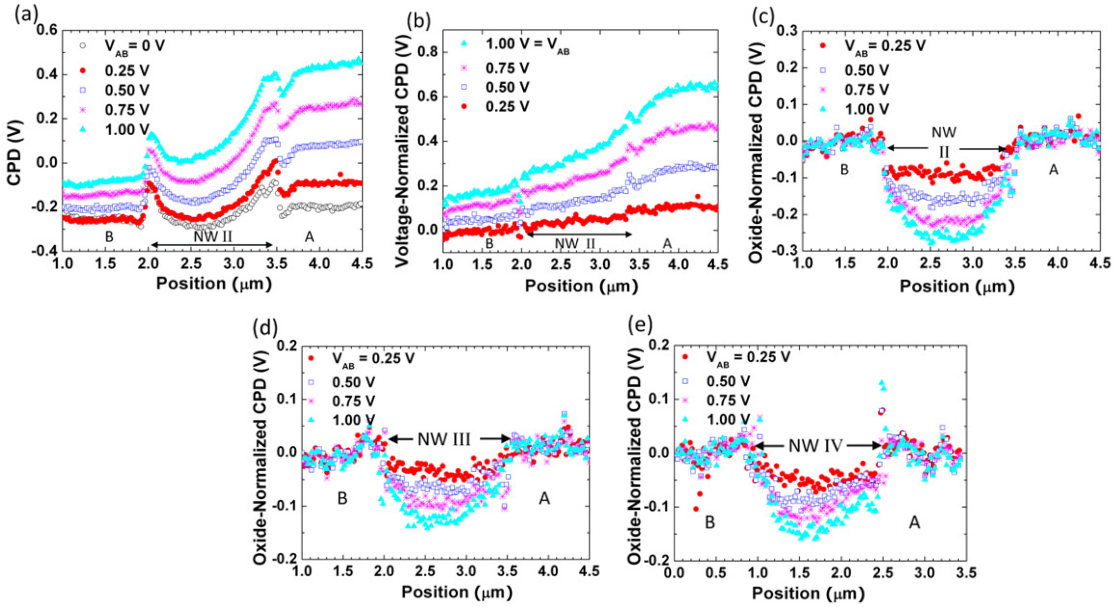

Figure 6. CPD line profiles at different applied voltages across (a) connected Si NW (labeled II in figure 5(d)). (b) Voltage-normalized and (c) oxide-normalized CPD line profile for the same Si NW. Oxide-normalized CPD data for Si NW labeled (d) III and (e) IV in the KPFM image of figure 5(d).

with residual Au from the growth process that remains at the 2.2 μm position after oxide normalization. Au can induce acceptor defects in Si NWs, which then exhibit a bias-dependent response [15, 20] that would remain after voltage normalization. The impurity state is clearly observed in the oxide-normalized data. Overall, this analysis suggests that the surface potential of the disconnected NW does not significantly differ from the SiO_2 trench under an applied bias and the changes observed in the raw KPFM data of the disconnected NW in figure 5(a) are attributable to the SiO_2 capacitive response to V_{AB} and are not related to current flow in the NW.

We investigated the bias-dependent behavior of several NWs in relationship to the bias-dependent response of the SiO_2 trench to gain a further understanding of the response of Si NWs. For comparison an example of raw CPD data and voltage-normalized CPD data for a connected NW, labeled II in figure 5(d), is shown in figures 6(a) and (b), respectively. The oxide-normalized, CPD line profiles for the connected NW II, figure 6(c), shows a monotonic decrease in surface

potential as V_{AB} increases from 0.25 to 1 V, when compared to that acquired at $V_{AB} = 0$. In figure 6(c), the gradual reduction in the CPD as one decreases the applied bias from 1 to 0 V is associated with the accumulation of electrons in the NWs, leading to an increase in Fermi energy [15]. In figures 6(d) and (e), oxide-normalized CPD data is shown for two other NWs, labeled III and IV in figure 5(d), connected to the same electrodes. The increase in Fermi energy is larger with applied bias for NW II when compared with NW III and NW IV. The oxide-normalized data of figures 6(c)–(e) thus provides information of the relative amount of current flowing across the NWs.

4. Conclusion

We have characterized VLS-grown Si NWs using KPFM with an applied bias across the NWs and found that proper normalization alongside FEM simulations is necessary to analyze the data. We have performed two types of normalization, voltage- and oxide-normalization procedures, as detailed above. The results show that voltage normalization mitigated contact potential differences due to localized charge and material work function variations, while oxide normalization mainly removed contact potential differences due to the structure's capacitance. These procedures have enabled us to estimate the NW contact resistance and locate poor NW connections to the electrodes. We estimated the contact resistance between the NW and the electrodes as a few $\mu\Omega$ cm^2. This is quite low and this KPFM method gives researchers a way to characterize the contact resistance to semiconductor NWs; contact resistance has often been a problem when fabricating NW devices, especially when one deposits metal directly onto the semiconductor NW to make a device.

By correcting for contributions from the oxide capacitance, NWs with poor electrical connections have a significantly different surface potential response to an applied bias than NWs connected to both electrodes. The CPD of the oxide-normalized, disconnected NW is close to zero over all positions that do not have residual Au, suggesting that all major contributions to CPD variations have been accounted for by using these two normalization procedures and lending credence to the use of voltage and oxide normalization processes to understand the bias-dependent response associated with current flow and impurity states. Overall, the presented characterization method is particularly useful for measuring the uniformity of electronic behavior, such as local current flow when NWs are connected in parallel.

Acknowledgments

The authors acknowledge the National Science Foundation CHE-0748912 for funding this work. RR and NJQ thank T I Kamins (help with VLS NW growth), R M Penner, P G Collins and D R Mumm for useful scientific discussions. The authors also acknowledge the use of the facilities within The Laboratory for Electron and X-ray Instrumentation (LEXI) at the University of California, Irvine.

References

[1] Wagner R S and Ellis W C 1964 *Appl. Phys. Lett.* **4** 89
[2] *International Technology Roadmap for Semiconductors* www.itrs.net/reports.html
[3] Taggart D K *et al* 2011 *Nano Lett.* **11** 2192
[4] Briseno A L *et al* 2007 *Nano Lett.* **7** 2847
[5] Heo J I *et al* 2011 *J. Electrochem. Soc.* **158** J76
[6] Quitoriano N J and Kamins T I 2008 *Nano Lett.* **8** 4410
[7] Martin Y, Abraham D W and Wickramasinghe H K 1988 *Appl. Phys. Lett.* **52** 1103
[8] Hudlet S *et al* 1995 *J. Appl. Phys.* **77** 3308
[9] Rosenwaks Y *et al* 2004 *Phys. Rev.* B **70** 085320
[10] Luo G N *et al* 2003 *J. Alloys Compounds* **349** 211
[11] Jacobs H O *et al* 1998 *J. Appl. Phys.* **84** 1168
[12] Baier R *et al* 2012 *Phys. Rev.* B **85** 165436
[13] Glatzel T *et al* 2003 *Mater. Sci. Eng.* B **102** 138
[14] Ouyang W J *et al* 2011 *ACS Nano* **5** 477
[15] Koren E *et al* 2011 *Nano Lett.* **11** 2499
[16] Koren E *et al* 2011 *Nano Lett.* **11** 183
[17] Henning A K *et al* 1995 *J. Appl. Phys.* **77** 1888
[18] Robin F *et al* 2000 *Appl. Phys. Lett.* **76** 2907
[19] Mizutani T, Arakawa M and Kishimoto S 1997 *IEEE Electron Device Lett.* **18** 423
[20] Bae S S *et al* 2012 *Nanotechnology* **23** 405706
[21] Koren E *et al* 2009 *Appl. Phys. Lett.* **95** 092105
[22] Yan L *et al* 2011 *Nano Lett.* **11** 3543
[23] Quitoriano N J, Wu W and Kamins T I 2009 *Nanotechnology* **20** 145303
[24] Nony L and Baratoff A 2006 *Phys. Rev.* B **74** 235439
[25] Koren E, Berkovitch N and Rosenwaks Y 2010 *Nano Lett.* **10** 1163
[26] Saraf S, Molotskii M and Rosenwaks Y 2005 *Appl. Phys. Lett.* **86** 172104
[27] Leveque G *et al* 2000 *Appl. Surf. Sci.* **157** 251
[28] Katzer K D *et al* 2006 *Appl. Phys. Lett.* **89** 3
[29] Seo K I *et al* 2006 *Electrochem. Solid State* **9** G69
[30] Sadewasser S *et al* 2009 *Nanotechnology* **20** 10
[31] Chaudhry A *et al* 2007 *Nano Lett.* **7** 1536
[32] Mohney S E *et al* 2005 *Solid-State Electron.* **49** 227
[33] Leonov V *et al* 2012 *IEEE Trans. Dielectr. Electr. Insul.* **19** 1253