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High-Efficiency Millimeter-wave Single-ended and Differential Fundamental Oscillators in CMOS

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***Abstract*—This paper reports an approach to designing compact high efficiency millimeter-wave fundamental oscillators operating above the $f_{max}/2$ of the active device. The approach takes full consideration of the nonlinearity of the active device and the finite quality factor of the passive devices to provide an accurate and optimal oscillator design in terms of the output power and efficiency. The 213-GHz single-ended and differential fundamental oscillators in 65-nm CMOS technology are presented to demonstrate the effectiveness of the proposed method. Using a compact capacitive transformer design, the single-ended oscillator achieves 0.79-mW output power per transistor (16 μm) at 1.0-V supply and a peak dc-to-RF efficiency of 8.02% (V_{DD}=0.80 V) within a core area of 0.0101 mm^2, and the measured phase noise is -93.4 dBc/Hz at 1-MHz offset. The differential oscillator exhibits approximately the same performance. A 213-GHz fundamental voltage-controlled oscillator (VCO) with bulk tuning method is also developed in this work. The measured peak efficiency of the VCO is 6.02% with a tuning rang of 2.3% at 0.6-V supply.**

***Index Terms*—CMOS, oscillators, VCO, signal generation, transformers, terahertz, millimeter-wave, sub-millimeter-wave.**

I. Introduction

THE millimeter-wave (mmW) and the terahertz (THz) frequency bands have great promise in enabling high-performance communication [1], [2] and sensing [3], [4] systems. The wide bandwidth available at these bands gives higher data rates and greater sensing/imaging precision. In addition, these bands encompass the rotational and vibrational frequencies of many molecules and hold great potential in realizing spectroscopy systems [5], [6].

The small wavelength at mmW/THz frequencies ensures that the antennas could be made very small. Together with the scaling of modern semiconductor technologies, much research has been devoted to designing highly integrated circuits and systems working at these frequencies [7]–[15]. However, the design of a solid-state mmW/THz signal sources with adequate output power and efficiency still remains a challenge due to the limited maximum frequency of oscillation f_{max}.

The f_{max} of the compound semiconductor devices, such as indium phosphide (InP) based heterojuction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs), has approached or exceeded 1 THz [16], [17]. A fundamental oscillator of 330 GHz is reported in an 35-nm InP HEMT process with 0.27 mW output power [18]. Fundamental oscillators fabricated in 0.25-μm InP HBT with f_{max} greater than 800 GHz operate up to 570 GHz while generating -19.2 dBm output power [19]. In the CMOS technology, a fundamental oscillator of 300 GHz is achieved with f_{max} of 380 GHz for 65-nm NMOS device [20]. An output power of -7 dBm is realized for a fundamental 240 GHz oscillator in 32-nm CMOS process [21]. For SiGe HBT technology, a fundamental oscillator of 218-245 GHz is obtained with peak output power of -3.6 dBm and efficiency of 0.81% [9]. A clear trend is that high efficiency power generation becomes much more challenging as we get close to f_{max} due to a lower activity of the active device and a lower quality factor Q of the passives components.

In this paper, we present an accurate approach to designing compact high efficiency fundamental oscillators operating above the $f_{max}/2$ of the active device. Compared to many existing design methodologies, the proposed design approach takes full consideration of the nonlinearity of the active device and the finite Q of the passive devices to provide an accurate procedure for optimizing the output power of the oscillator. A design example of a 213-GHz single-ended fundamental oscillator in 65-nm CMOS technology is presented to demonstrate the effectiveness of the proposed method. With the use of a compact capacitive transformer, the oscillator achieves 0.79 mW output power per transistor (16 μm) at 1.0 V supply and a 8.02% peak dc-to-RF efficiency within a core area of 0.0101 mm^2. A differential oscillator is also presented with very similar performance. The measured peak efficiency of the VCO is 6.02% with a tuning rang of 2.3% at 0.6-V supply.

II. A Review of Existing Approaches to Maximizing Oscillator Output Power

A theory for maximizing the oscillation output power of an active device based on large-signal network analysis was first introduced in [22], [23] and developed in several subsequent works [12], [13], [24]–[28]. In this section, we provide a brief *review* of this theory and a discussion of its limitations.

Consider a two-port network as shown in Fig. 1. Let V_1 and V_2 be the complex voltages at port 1 and 2 of the network. A complex voltage gain A is defined as [22], [23]

$$A = A_R + jA_I = \frac{V_2}{V_1}, \tag{1}$$

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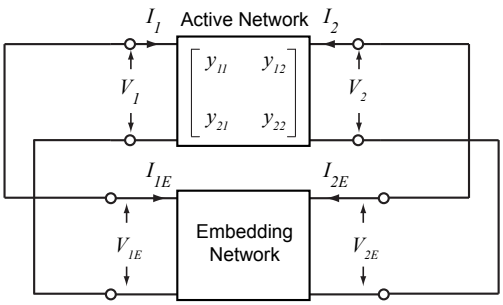

Figure 1. General two-port network described by its large-signal Y-parameters. A complex voltage gain can be defined as $A = V_2/V_1$.

where A_R and A_I are the real and imaginary parts of A, respectively. The net output power (or added power) of the two-port can be found by [22], [23]

$$P_R = -\frac{1}{2}\Re(V_1^* I_1 + V_2^* I_2).$$

The optimization of P_R can then be performed in terms of A. Since the absolute value of the port voltage and current cannot be analytically determined, several different expressions for the optimal voltage gain A_{opt} have been proposed. For example, (2) was derived under the assumption that $|V_1|$ is a constant with respect to A [22],

$$A_{opt} = -\frac{g_{21}+g_{12}}{2g_{22}} - j\frac{b_{21}-b_{12}}{2g_{22}} = -\frac{y_{21}+y_{12}^*}{2g_{22}}, \quad (2)$$

where g_{ij} and b_{ij} are real and imaginary parts of the large signal Y-parameters y_{ij} of the active network [23], respectively. Alternatively, (3) was derived assuming that $|V_1||V_2|$ is a constant [23],

$$\begin{aligned} |A_{opt}| &= \sqrt{\frac{g_{11}}{g_{22}}}, \\ \angle A_{opt} &= -\angle(y_{12}+y_{21}^*) + (2k+1)\pi, \end{aligned} \quad (3)$$

where k is an arbitrary integer. Both equations have been used recently to design high-efficiency millimeter-wave oscillators [12], [13], [15], [29].

Once A_{opt} is determined for a certain transistor and bias condition, the embedding network can be synthesized. By definition,

$$\begin{aligned} I_1 &= -I_{1E} = y_{11}V_1 + y_{12}V_2, \\ I_2 &= -I_{2E} = y_{21}V_1 + y_{22}V_2. \end{aligned} \quad (4)$$

Considering the real and imaginary parts, (4) contains 4 independent equations. To satisfy this set of equations, 3 reactive components are needed in addition to the load resistance which is the 4^{th} independent variable. The 3-component Π and T network typologies represent the most general and canonical solutions to this problem (Fig. 2). Herein, we use the lossless Π-network, more specifically Fig. 2(b), as an example to demonstrate how the embedding network is synthesized [24]–[26].

Here, the load G_L is connected between the gate and source of the active device. From Kirchhoff's current law, we have

$$\begin{aligned} I_{1E} &= Y_1 V_1 + Y_3(V_1 - V_2), \\ I_{2E} &= Y_2 V_2 + Y_3(V_2 - V_1). \end{aligned} \quad (5)$$

For lossless embedding networks, combining (1), (4) and (5), we arrive at the following matrix equation

$$\begin{bmatrix} 1 & 0 & 1-A_R & 0 & 0 & A_I \\ 0 & 0 & -A_I & 1 & 0 & 1-A_R \\ 0 & A_R & A_R-1 & 0 & -A_I & -A_I \\ 0 & A_I & A_I & 0 & A_R & A_R-1 \end{bmatrix} \begin{bmatrix} G_L \\ 0 \\ 0 \\ B_1 \\ B_2 \\ B_3 \end{bmatrix} = \begin{bmatrix} -g_{11} - \Re(Ay_{12}) \\ -b_{11} - \Im(Ay_{12}) \\ -g_{21} - \Re(Ay_{22}) \\ -b_{21} - \Im(Ay_{22}) \end{bmatrix}. \quad (6)$$

Solving the above equation will produce the desired admittance of the embedding network. The actual inductance/capacitance of the elements can be calculated from the admittance value at the desired oscillation frequency.

We note that the above approach is based on linear network analysis whereas oscillators are inherently nonlinear circuits. As such, it cannot accurately predict A_{opt}. For example, in deriving A_{opt}, there is no clear substantiation that either $|V_1|$ or $|V_1||V_2|$ must be a constant with respect to A. In reality, neither of these conditions is accurate. In addition, the Y-parameters of the active network are a nonlinear function of the voltage and current swing at the input and output terminals. This nonlinearity is influenced by the particular process technology as well as the layout, the bias condition, and the circuit topology of the active network. When the active device is operating above half of f_{max}, a linearization of this nonlinear problem may be appropriate because the amplitude of the harmonic waves are relatively small.

Several important works in high frequency oscillator designs have attempted to address the nonlinear design problem. Among them, [22]–[28] are based on quasi-linear network analysis to synthesize a proper embedding network from the large-signal parameters of the active device. Other works tackled the problem using nonlinear optimization [30], [31] of the terminal voltages and currents. When applied to the design of integrated oscillator operating close to f_{max}, existing methods have been found to produce incorrect (i.e. no oscillation) or sub-optimal designs. The primary reasons for this are an inaccurate extraction procedure of the device parameters and a negligence of the effect of the finite Q of the passive embedding network (more discussion in Section. III-C and Section. III-D). Building upon these existing works, we propose a design methodology that addresses these issues.

III. Proposed Design Approach to Maximizing Oscillator Output Power

A. Large Signal Y-parameters Extraction

Many researchers have recognized that there is a strong link between the designs of nonlinear power amplifiers and oscillators [25], [26], [28], [32], [33].

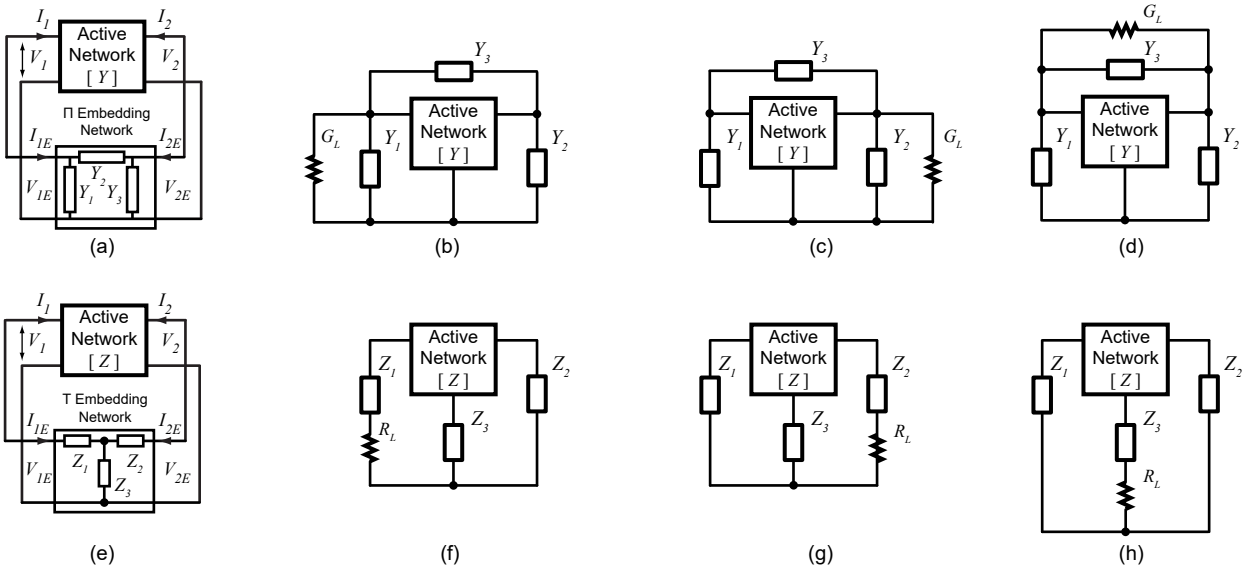

Figure 2. (a–d) Three Π (Y) embedding networks. The load is connected between gate and source, or drain and source, or drain and source, respectively. (e–h) Three T (Z) embedding networks. The load resistor is connected in series with the gate, drain, or source [24]–[26], respectively. Commonly used oscillator topologies such as the Colpitts and the Hartley belong to the Π embedding networks.

If we define *added power* P_{add} of the amplifier as

$$P_{add} = P_{out} - P_{in},$$

then it is well understood that the P_{add} reaches a peak value $P_{add,max}$ shortly after the output power starts to compress [32]. If $P_{add,max}$ is positive, then it is conceivable that a feedback network can be inserted at the output of the active device to route part of the output power back to the input to form an oscillator. As long as the feedback network provides the same impedance to the input and output of the active device, the device is independent of the external circuit. In this case, P_{add} is simply the output power of the oscillator. It can then be postulated that maximizing oscillator output power is equivalent to maximizing the amplifier $P_{add,max}$.

An iterative process based on source-pull and load-pull techniques can be used to maximize $P_{add,max}$, as shown in Fig. 3. The process starts with a set of initial values for the input power P_{in}, source impedance Z_S, and load impedance Z_L. The initial values for Z_S and Z_L may be set to $50\,\Omega$. The initial values of P_{in} may be set close to the compression point of the active device. A power sweep is first performed to identify the input power $P_{in,opt}$ at which $P_{add,max}$ is achieved under the current operating condition. Setting P_{in}=$P_{in,opt}$, several iterations of load-pull and source-pull sweeps may be used to identify the optimal source impedance $Z_{S,opt}$ and load-impedance $Z_{L,opt}$ that maximize P_{add}. A power sweep can then be performed at $Z_{S,opt}$ and $Z_{L,opt}$ for an updated $P_{in,opt}$. This process can be iterated until P_{in}, Z_S, and Z_L converge to a set of optimal values ($P_{in,opt}$, $Z_{S,opt}$, $Z_{L,opt}$) that maximize $P_{add,max}$.

Once the optimal condition is determined, the large signal Y-parameters can be extracted by the following procedures.

- Step 1: Extract the large-signal S-parameter with $Z_{S,opt}$ and $Z_{L,opt}$ at the optimum input power $P_{in,opt}$.
- Step 2: Re-normalize the large-signal S-parameters to a common system impedance Z_0.
- Step 3: Convert the re-normalized large-signal S-parameters to Y-parameters as in a linear network [34].

Because Y-parameters are sensitive to the terminal voltage and current swings, this procedure ensures that they are extracted at the exact operating condition for maximum oscillator output power. Theoretically, the Y-parameters may be directly extracted from a two-port measurement at the optimal condition. However, going through the large-signal S-parameter extraction is often easier, whether it's done through circuit simulations, as most high-frequency CAD programs come with built-in S-parameter and source/load-pull tools, or through measurement of an actual device, particularly at high frequencies. In contrast, directly obtaining the optimal terminal voltages and currents may be difficult in measurements [30], [31].

B. Optimal Voltage Gain A_{opt} with Lossless Embedding Networks

Once the large-signal Y-parameters, $Z_{S,opt}$, and $Z_{L,opt}$ are determined, A_{opt} can be calculated. Consider a terminated two-port network as shown in Fig. 4.

The port voltages and currents satisfy

$$\begin{aligned} I_1 &= y_{11}V_1 + y_{12}V_2, \\ I_2 &= y_{21}V_1 + y_{22}V_2, \\ I_2 &= -Y_L V_2. \end{aligned} \tag{7}$$

Solving (7) gives the complex voltage gain A

$$A = -\frac{y_{21}}{y_{22} + Y_L}.$$

Therefore,

$$A_{opt} = -\frac{y_{21}}{y_{22} + Y_{L,opt}}. \tag{8}$$

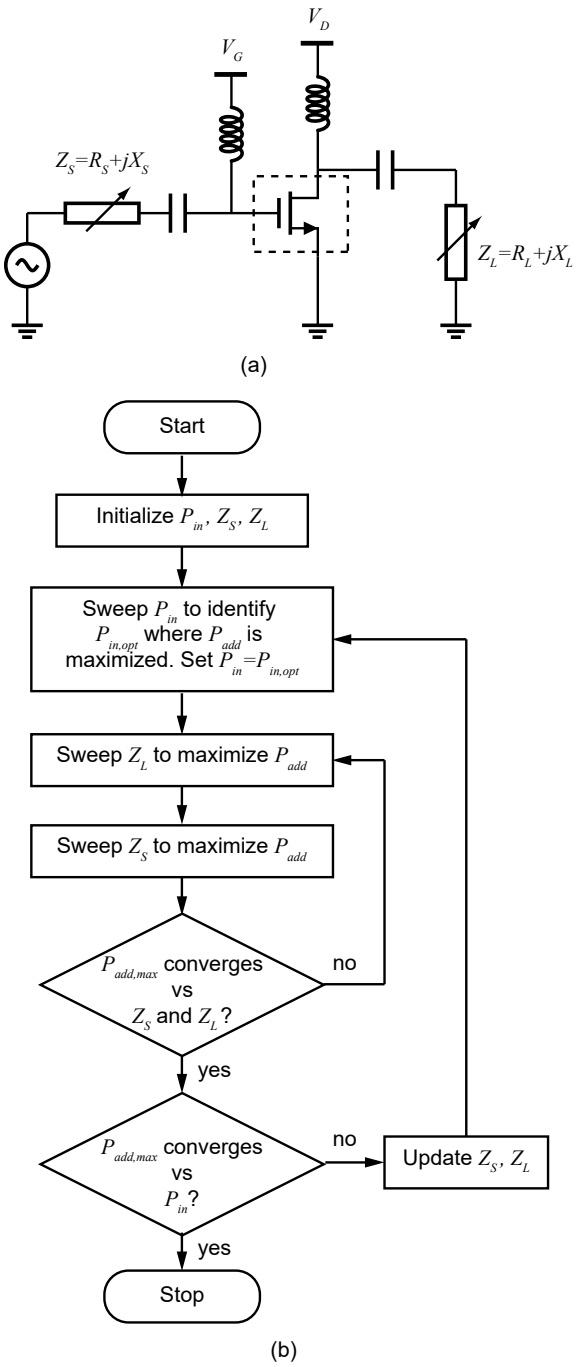

Figure 3. (a) Load-pull and source-pull setup and (b) an iterative process for maximizing $P_{add,max}$.

Alternatively, the input admittance of the two-port with Y_L as the load is given by

$$Y_{IN} = y_{11} + y_{12}A.$$

When maximum added power is achieved, $Y_{IN} = Y_S^*$. Solving for A gives

$$A = \frac{Y_S^* - y_{11}}{y_{12}}.$$

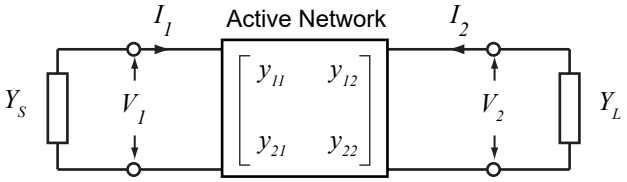

Figure 4. Two-port network with terminated loads.

Therefore, A_{opt} can also be obtained using

$$A_{opt} = \frac{Y_{S,opt}^* - y_{11}}{y_{12}}. \quad (9)$$

Furthermore, if the source/load-pull is performed in a circuit simulator, A_{opt} may be directly obtained from its definition, i.e. dividing V_2 by V_1.

(8) and (9) give practically identical value for A_{opt}. To illustrate this, we show the simulated and the calculated output power profile in Fig. 5(a). For each A, an automated script calculates the component values of the feedback network using (6), and constructs the netlist for the oscillator circuit. The script then runs a periodic steady state simulation on the netlist to find the output power of the oscillator. It can be seen that existing design equations deviate from the optimal solution, and that the A_{opt} calculated from our design method is almost identical to the optimal value produced by brute-force search. The plot is generated by circuit simulation. In these simulations, a lossless embedding network is assumed. Later we will see that practical lossy embedding network will introduce further design errors that existing design techniques do not take into account.

C. Synthesis of Embedding Networks with Finite Q

In integrated circuit processes, on-chip passive components typically have fairly low Q due to resistive loss of the metal interconnects and dielectric loss of the substrate. For practical designs, it is imperative that the Q of the feedback network components be taken into account in the design process. In this section, we use Π-embedding networks as an example to illustrate how component Q could affect the embedding network design.

For Π-embedding networks, the admittance parameters should be used. A lossy inductor or capacitor can be modeled as a lossless reactive component in parallel with a resistor and Q is defined as

$$Q_i = \frac{B_i}{G_{Qi}} \quad i = 1, 2, 3.$$

We first consider the case where load G_L is connected at the gate. G_L in (6) is then split into load conductance and the conductance of Y_1:

$$G_L = G + G_{Q1} = G + \frac{B_1}{Q_1}.$$

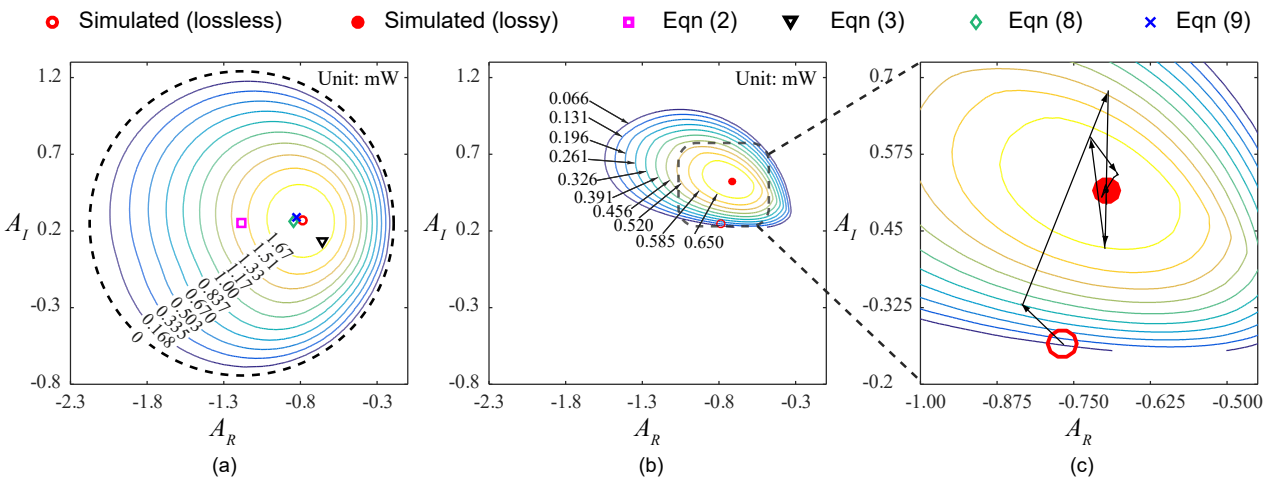

Figure 5. Constant power contours with respect to real and imaginary part of the complex voltage gain A, where $A = A_R + jA_I$ for (a) lossless Π-embedding network and (b) lossy Π-embedding network with quality factor for capacitor and inductor of 50 and 30, respectively. In (a), the dashed circuit represents the boundary between oscillation and no oscillation. In (b), it is observed that the oscillation region significantly shrinks and that the output power is much more sensitive to A_{opt} than in the lossless case. (c) plots the trajectory of A_{opt} of an example particle swarm optimization scheme to reach the true A_{opt} with finite Q.

The oscillation condition can then be expressed in the following matrix form:

$$D_i \cdot \begin{bmatrix} G \\ B_1 \\ B_2 \\ B_3 \end{bmatrix} = \begin{bmatrix} -g_{11} - \Re(Ay_{12}) \\ -b_{11} - \Im(Ay_{12}) \\ -g_{21} - \Re(Ay_{22}) \\ -b_{21} - \Im(Ay_{22}) \end{bmatrix}. \tag{10}$$

where

$$D_1 = \begin{bmatrix} 1 & \frac{1}{Q_1} & 0 & \frac{1-A_R}{Q_3} + A_I \\ 0 & 1 & 0 & -\frac{A_I}{Q_3} + 1 - A_R \\ 0 & 0 & \frac{A_R}{Q_2} - A_I & \frac{A_R - 1}{Q_3} - A_I \\ 0 & 0 & \frac{A_I}{Q_2} + A_R & \frac{A_I}{Q_3} + A_R - 1 \end{bmatrix}. \tag{11}$$

The subscript i denotes where the load is connected, with 1 representing the case when the load is between the gate and the source, 2 between the drain and source, and 3 between the gate and the drain. Following the same procedure, we can obtain the design equations when load is connected drain-source and gate-drain. The right hand side of (10) remains the same.

$$D_2 = \begin{bmatrix} 0 & \frac{1}{Q_1} & 0 & \frac{1-A_R}{Q_3} + A_I \\ 0 & 1 & 0 & -\frac{A_I}{Q_3} + 1 - A_R \\ A_R & 0 & \frac{A_R}{Q_2} - A_I & \frac{A_R - 1}{Q_3} - A_I \\ A_I & 0 & \frac{A_I}{Q_2} + A_R & \frac{A_I}{Q_3} + A_R - 1 \end{bmatrix}. \tag{12}$$

$$D_3 = \begin{bmatrix} 1 - A_R & \frac{1}{Q_1} & 0 & \frac{1-A_R}{Q_3} + A_I \\ -A_I & 1 & 0 & -\frac{A_I}{Q_3} + 1 - A_R \\ A_R - 1 & 0 & \frac{A_R}{Q_2} - A_I & \frac{A_R - 1}{Q_3} - A_I \\ A_I & 0 & \frac{A_I}{Q_2} + A_R & \frac{A_I}{Q_3} + A_R - 1 \end{bmatrix}. \tag{13}$$

The design equations are linear with respect to the unknowns which can be easily solved as is the case when embedding is lossless. G_{Qi} $(i = 1, 2, 3)$ should always be a positive value because it represents the conductance of reactive elements. Therefore, as the reactance of an inductor is negative, the associated Q should also be negative to make sure G_{Qi} $(i = 1, 2, 3)$ is positive.

However, the type of passive element cannot be predetermined without solving the equations. It is necessary to enumerate all eight possible combinations of the embedding: either capacitor or inductor for each of the three components. Each combination presets the sign of Q, and the solved susceptance should satisfy

$$B_i \cdot Q_i > 0 \quad i = 1, 2, 3.$$

to filter out networks with negative conductance components.

The impact of Q on oscillator output power is different for the three reactive components. Fig. 6 shows the simulated oscillator output power with respect to the component Q. Each curve represents one lossy component whose Q is swept from 10 to 100 while the others are kept ideal. It can be seen that the Q of Y_3 affects output power most significantly whereas Q of Y_1 and Y_2 have negligible influence on power when they are greater than 40. This is due to the larger voltage swing between

Table I
EFFECT OF HARMONIC IMPEDANCE ON FUNDAMENTAL POWER AND EFFICIENCY

Load-pull termination	$\max P_{add,max}$	$\min P_{add,max}$	$\max PAE_{max}$	$\min PAE_{max}$	Load and source impedance (Ω)
Optimal fundamental impedance, all harmonics open.	1.83 mW	1.83 mW	16.36%	16.36%	$Z_S(f_0) = 3.65 + j28.5$, $Z_L(f_0) = 12.6 + j28.1$.
Optimal fundamental impedance, sweep 2^{nd} harmonic, 3^{rd} harmonic open.	1.93 mW	1.68 mW	17.23%	14.95%	$Z_S(f_0) = 3.65 + j28.5$, $Z_L(f_0) = 12.6 + j28.1$.
Optimal fundamental impedance, optimal 2^{nd} harmonic impedance, sweep 3^{rd} harmonic.	1.93 mW	1.93 mW	17.30%	17.23%	$Z_S(f_0) = 3.65 + j28.5$, $Z_L(f_0) = 12.6 + j8.1$, $Z_L(2f_0) = 0.0 + j41.85$.

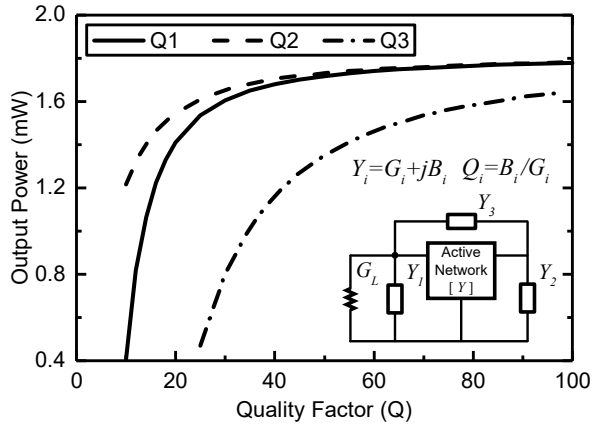

Figure 6. Simulated oscillator output power with respect to the component Q of the embedding network. An NMOS transistor (W/L = 16 µm/60 nm) is used as the active device in an oscillator topology given by the inset. Simulation is done at 215 GHz.

the gate and drain terminals. The difference in sensitivity to Q imposes a greater concern on the implementation of Y_3. It also affects the oscillator topology and physical realization which will be discussed in Section IV.

D. A_{opt} with Finite Q

It should be noted that A_{opt} will deviate from the ideal value given by (8) or (9) when the loss of the feedback network is considered because the lossy network elements consume a fraction of the output power from the active device and maximizing $P_{add,max}$ no longer ensures maximizing output power to the load. This is one of the reasons why existing design approaches fail for integrated devices working close to f_{max}. To illustrate this, we present in Fig. 5(a) and (b) a comparison between the simulated output power with respect to A for lossless and lossy embeddings. Fig. 5(b) is generated in a similar fashion as Fig. 5(a), except that (10) is used in place of (6). It can be observed that the oscillation region, defined as the range of A_I and A_R that produce a positive output power, significantly shrinks with decreasing Q and that the output power is much more sensitive to A than in the lossless case. In this particular example, it is evident that the "ideal" A_{opt} with lossless embedding is sitting at the boundary of the oscillation region. In an actual implementation, no output may be observed due to the loss of the output matching network.

In practical designs, the "true" A_{opt} with finite Q can be obtained by either searching around the original A_{opt} value or numerical optimization. We present here a possible optimization approach based on particle swarm optimization (PSO) [35], [36]. PSO solves an optimization problem by having a collection of possible solutions, referred to as "particles", and moving them in the search-space according to the their position and velocity. Because PSO does not require the gradient to operate, it is particularly suitable for circuit optimization problems involving a simulator in the loop.

In this example, two particles are used as our studies show that increasing the number of particles does not result in better solutions. The particles are initialized at the "ideal" A_{opt} value given by lossless embedding networks and given random initial velocities. In each iteration, the output power of the resulting oscillator is simulated for each particle and is used as the fitness function, based on which the individually best particle $pBest$ and the globally best particle $gBest$ are recorded. Each particle is then updated by moving towards $pBest$ and $gBest$. These steps are repeated until the fitness difference between two consecutive $pBest$ is less than a predefined error value. Fig. 5(c) shows the trajectory of the $gBest$ particle that leads to the global optimum. The convergence to the optimum point is very reliable.

Lastly, we should also note that when finite Q is considered, the voltage swing at the input and output port of the active device may change from the lossless embedding case, thus leading to a change in the device large signal Y-parameters. To resolve this issue, the Y-parameters may need to be re-extracted at a different input power and iterated through the design process.

E. Influence of Harmonic Impedance

Harmonic load impedance in general has an effect on fundamental output power and efficiency. However, when oscillation frequency approaches $f_{max}/2$ or even higher, the influence of harmonic termination becomes very small. To illustrate this, we simulated the $P_{add,max}$ and PAE of a 16-µm NMOS transistor under various harmonic terminations. The results are presented in Table I. We notice that optimal second harmonic termination has minimal effects on the fundamental output, with a 5.46% increase (1.93 mW vs. 1.83 mW) in

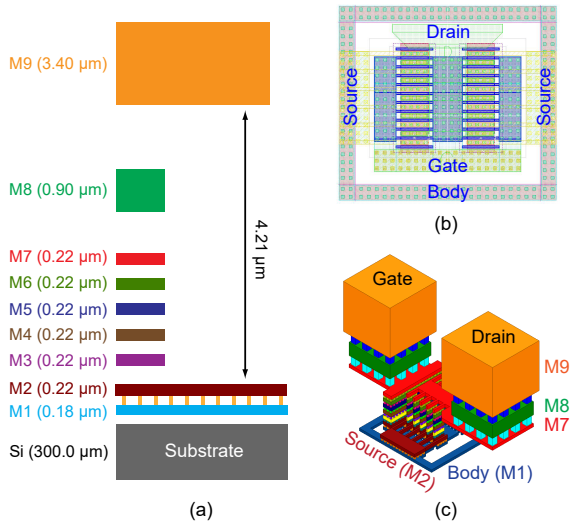

Figure 7. (a) Stack-up of the 65-nm CMOS technology. (b) Layout of the 16-µm NMOS transistor. (c) Interconnect setup used for connecting to the transistor.

maximum added power and 5.32% increase (17.23% vs. 16.36%) in maximum PAE. Third order harmonic has even less effect with less than 0.3% difference between optimum and worst termination impedance. These improvement in the fundamental power will be further negated by the loss of additional harmonic matching networks. As will be shown later in this paper, loss of passive components has a significant impact on the oscillation power. As such, we choose not to consider harmonic impedance terminations in this work.

IV. Design Examples

To demonstrate the validity and effectiveness of the above design approach, we present example designs for high-efficiency 215 GHz fundamental-mode single-ended and differential oscillators, and a fundamental-mode voltage controlled oscillator (VCO) in a 65-nm CMOS technology.

A. Process and Transistor

In this work, we realize our design in a 65-nm CMOS technology featuring 9 metal interconnect layers (Fig. 7(a)). To achieve a high f_{max}, we custom lay out a 16-µm NMOS transistor, as shown in Fig. 7(b). This transistor is constructed using two parallel 8-µm NMOS transistors. Double gate contacts are used to increase f_{max} by reducing the gate resistance. A 3-D rendition of the interconnects to the transistor is shown in Fig. 7(c). The parasitics of this 16-µm NMOS transistor are extracted up to M7 by Calibre and the simulated f_{max} is around 398 GHz.

For lossless embedding, through the source pull and load pull at 215 GHz, we can get the optimal input power of 3 dBm, optimal source impedance of $Z_{S,opt} = 5.15 + j28.95\,\Omega$ and optimal load impedance of $Z_{L,opt} = 17.25 + j29.5\,\Omega$. The extracted large signal Y-parameters are $y_{11} = 3.2915 + j27.7151$ mS, $y_{12} = -0.8609 - j7.10865$ mS, $y_{21} = 17.1224 - j10.5326$ mS, and $y_{22} = 6.8703 + 19.4183$ mS. The calculated A_{opt} is $-0.85 + j0.25$. The calculated component values for lossless Π-Networks are summarized in Table II.

Table II
Component Values for Lossless Π-Networks

Topology (Load location)	B_1	B_2	B_3	R_1
Gate-Source	39.78 fF	53.96 fF	15.69 pH	166.8 Ω
Drain-Source	6.94 fF	16.99 fF	31.90 pH	131.0 Ω
Gate-Drain	24.69 fF	36.21 fF	20.60 pH	581.4 Ω

Table III
Component Values for Lossy Embedding Π-Networks
(Capacitor Q=50 and Inductor Q=30)

Topology(Load location)	B_1	B_2	B_3	R_1
Gate-Source	5.75 fF	18.89 fF	32.46 pH	265.0 Ω
Drain-Source	151.9 pH	9.29 fF	47.34 pH	186.0 Ω
Gate-Drain	2.24 fF	14.11 fF	37.58 pH	779.8 Ω

For lossy embedding, using the proposed design approach with capacitor Q=50 and inductor Q=30, the optimal condition for maximizing output power is achieved at an input power of 0 dBm, a source impedance of $Z_{S,opt} = 3.65 + j28.45\,\Omega$, and a load impedance of $Z_{L,opt} = 12.60 + j28.09\,\Omega$. Under this condition, the extracted large signal Y-parameters are $y_{11} = 3.1869 + j27.6803$ mS, $y_{12} = -0.9383 - j7.1510$ mS, $y_{21} = 19.1174 - j12.0457$ mS, and $y_{22} = 6.9713 + 18.2182$ mS. The A_{opt} obtained from PSO algorithm for a lossy embedding network is $-0.744 + j0.584$ which is used in the oscillator design. Based on (10), (11), (12) and (13), the calculated component values for lossy Π-Networks are summarized in Table III. All calculations and optimization have been carried out at 215 GHz.

B. Oscillator Topology

1) Choice of Load Position: Theoretically, all six topologies, as shown in Fig. 2, should generate the same output power with lossless embedding components. In practice, however, not all topologies are equal, particularly in terms of the load impedance matching.

Take lossless Π-networks for example, the output power extracted from the three networks are:

$$\begin{aligned} P_1 &= \frac{1}{2} G_{L1} \cdot |V_1|^2, \\ P_2 &= \frac{1}{2} G_{L2} \cdot |V_2|^2, \\ P_3 &= \frac{1}{2} G_{L3} \cdot |V_1 - V_2|^2. \end{aligned} \tag{14}$$

Replacing V_2 as $A_{opt} \cdot V_1$, and recalling that power in (14) are identical, the ratio of loads are obtained:

$$\begin{aligned} G_{L1} &= |A_{opt}|^2 \cdot G_{L2}, \\ G_{L1} &= \left[|A_{opt}|^2 - 2\Re(A_{opt}) + 1\right] \cdot G_{L3}. \end{aligned} \tag{15}$$

From (15) we see that the ratio of G_{L1} over G_{L2} depends on the magnitude of A_{opt}. For the transistor size and biasing condition in this design, the magnitude of A_{opt} is 0.89, making G_{L1} and G_{L2} fairly close to each other. G_{L3}, however, is

almost always several times smaller than G_{L1} due to real part of A_{opt} being always less than zero. Too large a load resistance makes it difficult to match with low loss. The component values for the oscillator with lossless and lossy embedding networks are summarized in Table II and Table III for a more quantitative comparison.

Between the cases of gate-source connection and drain-source connection, we note that the drain-source connection results in a network with two large inductors and is therefore less preferable. Therefore, we choose to place the load at the gate of the active device in this design. The final values of the components (caption of Fig. 8) are slightly different from Table III to take into account the parasitics of the components.

2) Biasing Topology: The gate and drain terminals of the active device could be biased at either the same voltage or separately. The advantage of separate biasing is that oscillating power and efficiency can be optimized independently. However, as the calculated Y_3 (Fig. 6) is an inductor, a large capacitor is required in series to allow different gate-drain dc voltage. This capacitor degrades the overall Q of Y_3 in two ways: 1) the loss on the capacitor alone is considerable due to inability to build large high-Q capacitors (e.g. above 150 fF) at millimeter wave frequency; and 2) the series capacitor inevitably reduces the overall inductance so that to maintain the effective inductance unchanged, the inductor value has to be increased which in turn adds additional loss to the embedding network. Therefore, the biasing of the gate and the drain are shared in our design to achieve a compact die area.

The evolution of the circuit topology is captured in Fig. 8. Note that we take advantage of the parallel connection between R_1 and C_1, and utilize a capacitive transformer to match a typical system impedance of 50 Ω to the calculated optimum load, as shown in Fig. 8(b) [29].

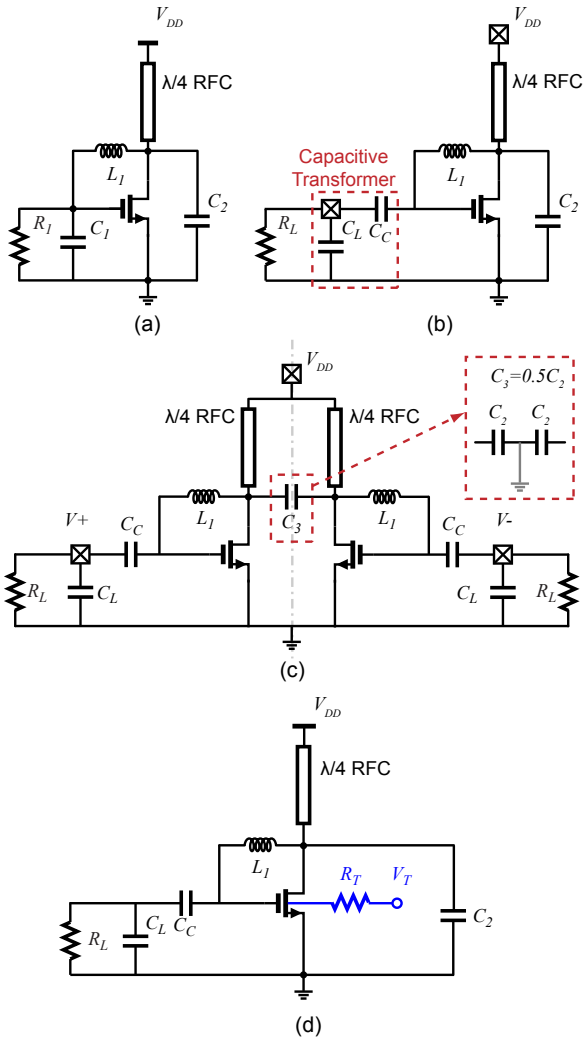

Figure 8. Evolution of the oscillator design and VCO. (a) Initial prototype topology. (b) Final schematic of the single-ended oscillator. (c) Schematic of the differential oscillator. (d) Schematic of the VCO. Critical component values are R_L=50 Ω, C_L=10.7 fF, C_C=11.2 fF, C_3=9.2 fF and L_1=33.6 pH. C_L is implemented as the parasitic capacitance of the RF pad.

C. Differential Oscillator

A differential oscillator is derived from the single-ended oscillator by locking two of them 180° out-of-phase through the drain capacitor C_3, as shown in Fig. 8(c). With $C_3 = 0.5C_2$, each half of the differential oscillator maintains the optimal oscillation condition. In the common mode half circuit, C_2 is left open and in this specific example, the remaining two reactive component (L_1 & C_1) do not provide an oscillation condition. Therefore, the two oscillator cores can only oscillate in the differential mode.

D. Voltage Controlled Oscillator (VCO)

Based on the proposed optimal design approach, we also present a voltage controlled oscillator design with high output power and dc-to-RF efficiency across the tuning range. Frequency tuning of integrated oscillators is commonly achieved by using varactors. At millimeter-wave and THz frequencies, the quality factor of a varactor in CMOS process is quite low, resulting in low output power and efficiency.

To overcome this limitation, we realize frequency tuning by varying the MOS transistor bulk voltage, as shown in Fig. 8(d). Here, the MOS transistor's bulk is isolated by a deep n-well. As the bulk voltage increases, the parasitic capacitance of the MOS transistor becomes large due to decrease in depletion region width. R_T is used to limit dc current when tuning voltage V_T is high (> 0.8 V) [37]. Compared with the varactor tuning method , bulk voltage tuning causes less degradation of the quality factor of the oscillating tank.

E. Passives

In order to achieve a better Q, the top metal layer (M9) is used to realize the inductor and ground metal beneath the inductor is removed. The spiral inductor with inner diameter 20 μm and width 4 μm is shown in Fig. 9 together with the corresponding effective inductance L and Q. At 215 GHz, the calculated inductance L is 33.6 pH and the qualify factor Q is 28.3.

Metal 6 and metal 7 layers are used to form parallel-plate capacitors for higher capacitance density and quality factor. The capacitance and Q of an example capacitor with size

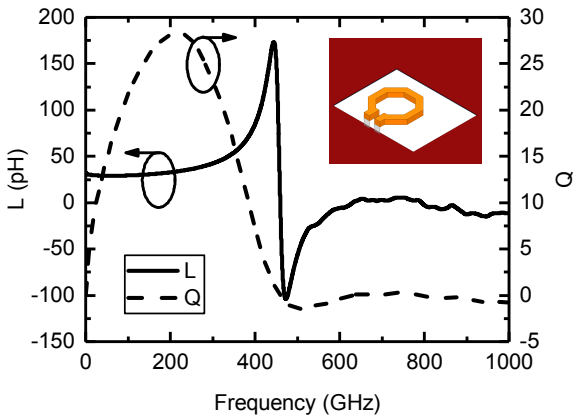

Figure 9. Effective inductance and Q of an inductor using M9 in the 65-nm process. The inset shows a 3D model of the inductor.

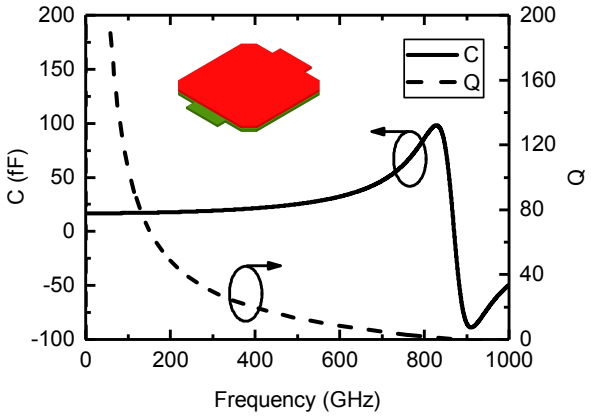

Figure 10. Effective capacitance and Q of a 10.0 µm × 10.0 µm parallel-plate capacitor using M6 and M7 in the 65-nm process. The inset shows a 3D model of the capacitor.

of 10.0 µm × 10.0 µm is shown in Fig. 10. At 215 GHz, the calculated capacitance is 17.9 fF and Q is 44.1.

F. Measurement Results

The measurement setups for measuring output spectrum, phase noise and output power are shown in Fig. 11. The output spectrum and phase noise of oscillators are measured using a signal analyzer (Agilent N9030A) with an external frequency extender (VDI WR-5.1 TX and RX mm-head module) (Fig. 11(a)). The LO signal which is generated from signal analyzer is fed into a tripler (PMP Ka3) through a diplexer (OML DPL313B) and then into the LO input port of the frequency extender. After multiplied by 18 times and amplified, the LO signal is mixed with the output signal of oscillator and the amplified IF signal is fed back to signal analyzer through the diplexer. A WR-5 bend is connected between the frequency extender and the G-band probe. The oscillators are biased through a dc probe. LDO regulators powered by batteries are used to provide the V_{DD} supply voltage to the oscillators. The combination of the battery supply and LDO ensures that minimal supply noise is upconverted to the carrier frequency.

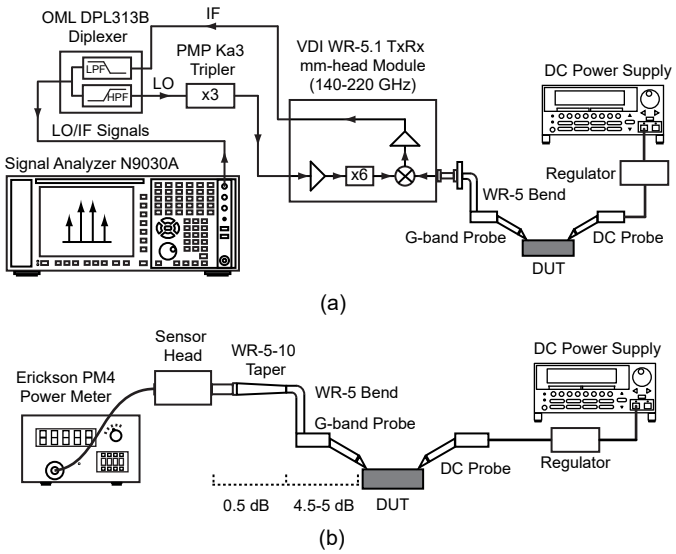

Figure 11. Measurement setup for (a) output spectrum and (b) output power.

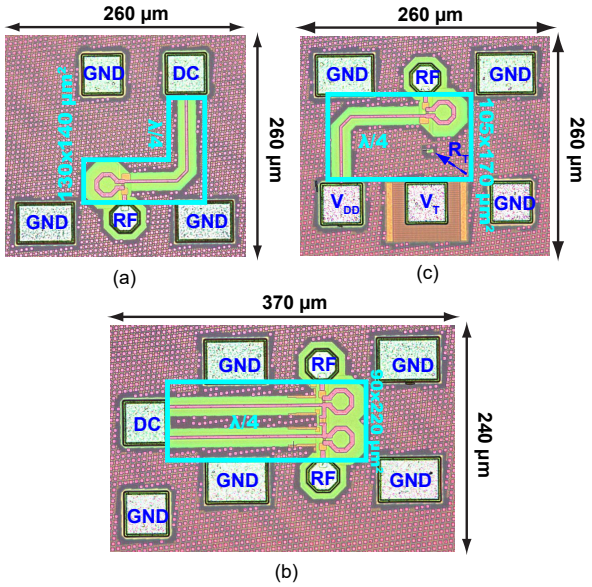

Figure 12. Chip photographs of the (a) single-ended oscillator, (b) differential oscillator and (c) VCO.

Pictures of the fabricated circuit dies are shown in Fig. 12. The die size is 0.26 mm×0.26 mm for the single-ended oscillator (Fig. 12(a)) and 0.37 mm×0.24 mm for the differential oscillator (Fig. 12(b)). Due to the use of the capacitive transformer, the core size of the single-ended oscillator is 0.0101 mm^2.

Fig. 13 shows the measured output power, dc-to-RF efficiency, and phase noise of the single-ended and differential oscillators. The output power of the single-ended oscillator is measured with an Erickson PM4 calorimeter, as shown in Fig. 11(b). With a dc current of 11.5 mA from a 1.0 V drain voltage, the oscillator achieves a 0.79 mW output power. For the single-ended oscillator, as shown in Fig. 13 (a–c), the measured output power increases monotonically with V_{DD} with a peak dc-to-RF efficiency of 8.02% at a V_{DD} of 0.80 V.

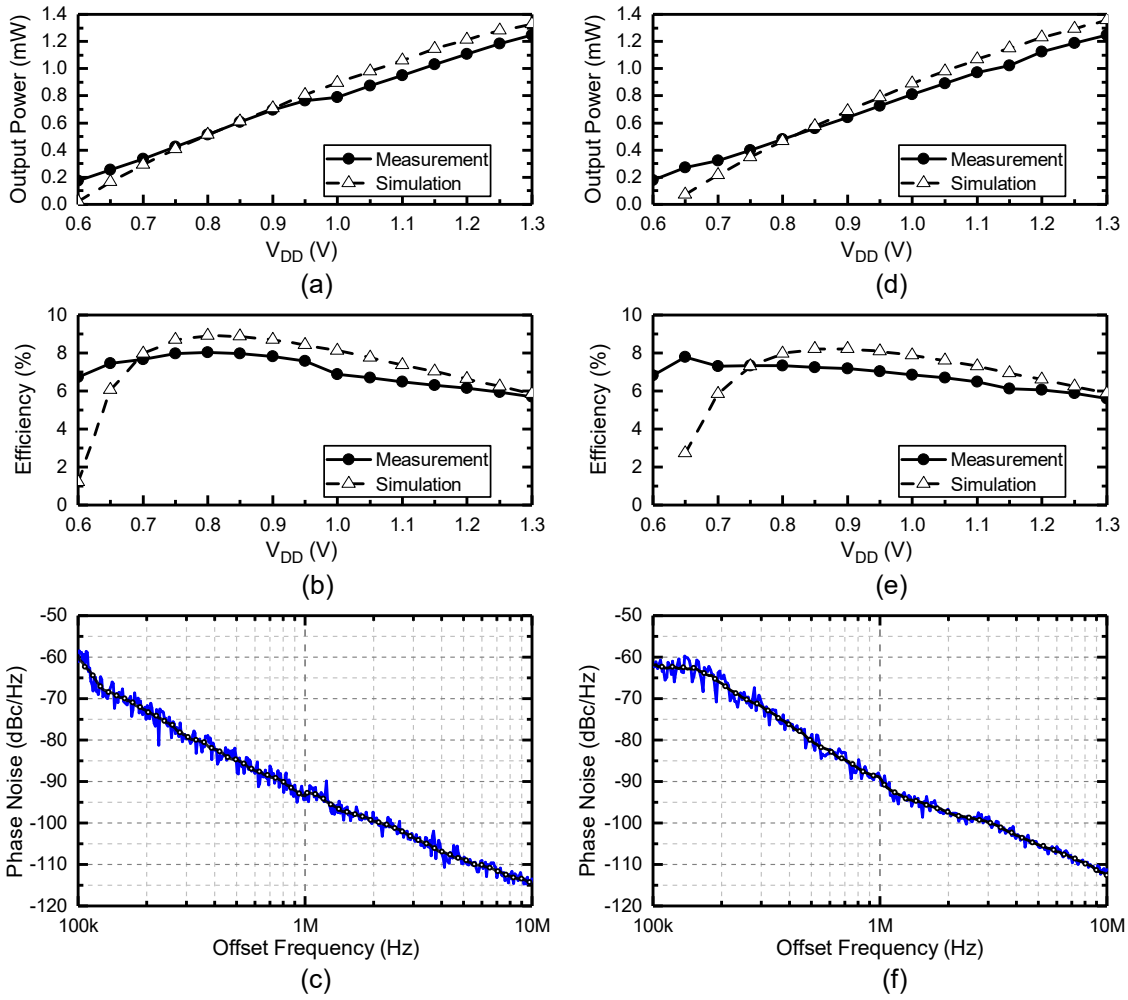

Figure 13. Measured performance of the single-ended and differential oscillators. The performance of the single-ended is shown in (a–c) and that of differential oscillator is shown in (d–f). Note: the simulation results are based on EM simulated SnP file of the entire structure of the oscillator.

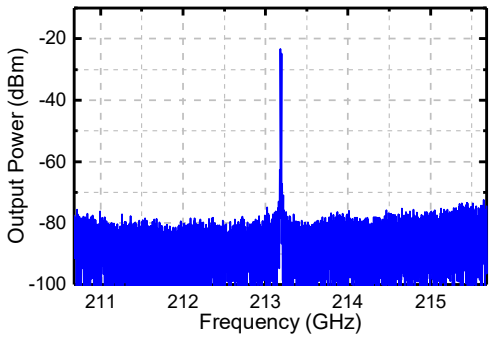

Figure 14. Measured IF spectrum of the single-ended oscillator.

At 1.0-V supply, the single-ended oscillator achieves a dc-to-RF efficiency of 6.87%. The measured phase noise is -93.4 dBc/Hz at 1 MHz offset and -114.9 dBc/Hz at 10 MHz offset, as shown in Fig. 13(c). Fig. 14 shows the measured IF spectrum of the single-ended oscillator. The measured oscillation frequency is 213.18 GHz and deviates from the design target (215 GHz) by approximately 1%.

To measure the differential oscillator, both the spectrum analyzer and the power meter are connected to provide 50-Ω terminations to both ports. The measured oscillation frequency of the differential oscillator is 213.32 GHz, which is also close to the design target (215 GHz). The measured output power, dc-to-RF efficiency, and phase noise of the differential oscillator are shown in Fig. 13 (d–f). The measured total output power is 1.618 mW and the measured efficiency is 6.86% at a V_{DD} of 1.0 V. The peak efficiency is 8.00% at a V_{DD} of 0.65 V. The measured power may potentially be lower than the actual power because of the impedance imbalance of the measurement setup. The measured phase noise of the differential oscillator is -90.9 dBc/Hz at 1 MHz offset and -112.6 dBc/Hz at 10 MHz offset.

The measured output frequency, output power, dc-to-RF efficieny, and phase noise of the 213 GHz fundamental VCO are shown in Fig. 15. The tuning profile of the VCO is shown in Fig. 15(a). At a V_{DD} of 0.6 V, its oscillation frequency is tuned from 211.0 GHz to 215.9 GHz with bulk voltage swept from 0 V to 1.0 V. The measured output power varies from

-0.83 dBm to -7.9 dBm and -6.8 dBm to -14.5 dBm at a drain voltage of 1.0 V and 0.6 V, respectively, as shown in Fig. 15(b). Although the output power is much lower than the highest output power possible, we note that the VCO maintains high power efficiency of better than 6% over the tuning range (Fig. 15(c)). We also note that for bulk voltage less than 0.8 V, the variation in output power is less than 1.2 dB for V_{DD}= 1.0 V and less than 2.1 dB for V_{DD}= 0.6 V. The measured phase noise is -93.7 dBc/Hz at 1 MHz offset and -114.5 dBc/Hz at 10 MHz offset, as shown in Fig. 15(d).

The discrepancy between the design target, simulation, and measurement may be due to a number of factors, including inaccurate device modeling provided by the foundry, fabrication tolerances, and small errors introduced in the electromagnetic simulation of the passive structures (e.g. the slopes of the sidewalls of the interconnect traces modeled as perfectly vertical sidewalls, and groups of vias simplified to a slab of metallic connection).

Table IV compares the designed oscillators with the state-of-the-art and shows clearly the advantages of our proposed design in terms of efficiency and area.

V. Conclusion

In this paper, we have presented an accurate design approach that maximizes the output power and dc-to-RF efficiency of integrated fundamental oscillators working above the $f_{max}/2$ of the active device. The approach uses source-pull and load-pull simulations/measurements to determine the optimal source impedance, load impedance, and input power presented to the active device such that maximum oscillator output power is achieved. Compared with existing works, the proposed approach takes into account the inherent nonlinear characteristics of the active device as well as the finite Q of the external components, and provides an accurate prediction of the oscillation condition, frequency, and power. To demonstrate the effectiveness of this approach, we have presented a 213 GHz single-ended fundamental oscillator, a 213 GHz differential fundamental oscillator, and a 213 GHz fundamental VCO, all implemented in 65-nm CMOS technology. With the use of compact capacitive transformers, these oscillators achieve smaller area compared to other oscillators.

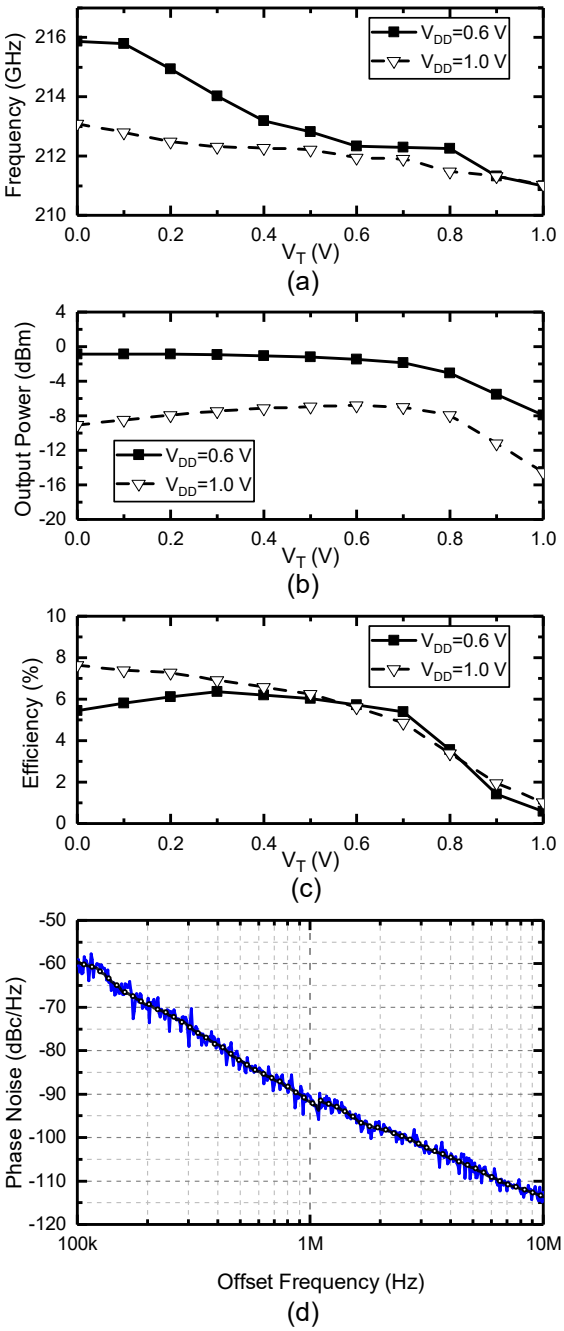

Figure 15. Measured output frequency (a), output power (b) and dc-to-RF efficiency (c) of the 213 GHz fundamental VCO with respect to the bulk tuning voltage (V_T), and measured phase noise with respect to offset frequency (d).

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Table IV
COMPARISON WITH OTHER STATE-OF-THE-ART INTEGRATED OSCILLATORS AND VCOS

Reference	Type	Frequency (GHz)	RF Power (dBm)	Tuning Range (%)	Phase Noise (dBc/Hz)	dc Power (mW)	dc-to-RF Efficiency (%)	Area (mm^2) (Chip/Core)	Technology
[38]	Push-push	212	-7.1	2.8	-92 @1 MHz	30	0.65	0.0725/ NA	130-nm SiGe
[39]	Push-push	256	4.1	6.5	-94 @1 MHz	227	1.14	0.4355/NA	65-nm CMOS
[40]	Push-push	239	-4.8	12.5	-98.43 to -110.9 @10 MHz	18.5	1.47	0.18/ NA	65-nm CMOS
[41]	Push-push	210	1.4	10.6	-87.5 @1 MHz	26–61	2.4	0.08 / 0.027	130-nm SiGe
[42]	Push-push	215	5.6	0.65	-94.6 @1 MHz	79	4.6	0.08 / NA	65-nm CMOS LP
[15]	Fundamental + Multiplier	225	3	5.33	-94 @1 MHz	68	2.95	0.525 / NA	65-nm CMOS
[9]	Fundamental	245	-3.6	11.66	-98.0 @10 MHz	54	0.81	NA /NA	120-nm SiGe
[21]	Fundamental	240	-7	4.58	-93.0 @10 MHz	13	1.5	0.0552 / 0.004	32-nm CMOS
[43]	Fundamental	210	-13.5	3.85	-81.0 @1 MHz	42	0.1	NA / 0.04	32-nm CMOS SOI
[44]	Fundamental	219	-3	NA	-77.4 @1 MHz	24	2.08	0.105 / 0.014	65-nm CMOS
[45]	Fundamental	195	6.5	1.1	-98.6 @1 MHz	28.69	15.3	0.1517 / NA	55-nm SiGe
[7]	Fundamental	175.6	4.8	0.34	-101.7 @1 MHz	25.8	11.7	0.193 / NA	130-nm SiGe
[29]	Fundamental	213	-2.5	NA	-87 @1 MHz	14.35	3.9	0.067 / 0.0028	65-nm CMOS
This work	Fundamental Oscillator	213	-1.0	NA	-93.4 @1 MHz	11.5	6.87	0.0675 / 0.0101	65-nm CMOS
This work	Fundamental Diff. Oscillator	213	-0.92†	NA	-90.9 @1 MHz	11.8 ‡	6.86	0.0888 / 0.0198	65-nm CMOS
This work	Fundamental VCO§	213	-0.83	0.98	-93.7 @1 MHz	10.82	7.6	0.0675 / 0.0179	65-nm CMOS
This work	Fundamental VCO *	213	-6.93	2.3	-93 @1 MHz	3.36	6.02	0.0675 / 0.0179	65-nm CMOS

† Single-ended calibrated output power of the differential oscillator.
‡ This differential oscillator draws 23.6 mA bias current from a 1.0 V supply. For one single transistor, the dc current is 11.8 mA.
§ V_{DD} = 1.0 V, V_T is from 0.0 V to 1.0 V.
* V_{DD} = 0.6 V, V_T is from 0.0 V to 1.0 V.

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