UNIVERSITY OF CALIFORNIA SAN DIEGO

Ku-Band Phased Arrays and K-Band Communication Circuits and Systems in Advanced SiGe and CMOS SOI Technologies for SATCOM On-the-Move Applications

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by

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2020

The dissertation of Abdurrahman H. Aljuhani is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2020

DEDICATION

To

my parents, Hamed and Hania

my wife, Jumana

my wonderful sons, Raed and Sami

my sisters, Wafaa and Wejdan

my brothers, Abdullah, Abdulhamid, and Sultan

my cousin, brother, and best friend, Essam

with love and gratitude for being the sources of motivation.

EPIGRAPH

"Whoever seeks a path in search of knowledge,

Allah (God) will facilitate his/her way to paradise."

— Prophet Mohammed (PBUH)

Tell me, and I forget,

Teach me, and I remember,

Involve me, and I learn.

— Xun Kuang

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Chapter 2, in full, has been submitted for publication of the material as it may appear in: A. H. Aljuhani, T. Kanar, S. Zihir, and G. M. Rebeiz, "A 256-Element Ku-band Polarization Agile SATCOM Receive Phased-Array with Wide-Angle Scanning and High Polarization Purity," in *IEEE Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and author of this paper.

Chapter 3, in full, has been submitted for publication of the material as it may appear in: A. H. Aljuhani, T. Kanar, S. Zihir, and G. M. Rebeiz, "A 256-Element Ku-band Polarization Agile SATCOM Transmit Phased-Array with Wide- Scan Angles, Low Cross-Polarization, Deep Nulls, and 36.5 dBW EIRP Per Polarization," in *IEEE Transactions on Microwave Theory and Techniques*. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in part, is a reprint of the material as it appears in: A. H. Aljuhani and G. M. Rebeiz, "A 12.5 mW Packaged K-Band CMOS SOI LNA with 1.5 dB NF," *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 156-159. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in part, is also a reprint of the material as it appears in: A. H. Aljuhani, T. Kanar, and G. M. Rebeiz, "A Packaged Single-Ended K-Band SiGe LNA with 2.14 dB Mean Noise

Figure," *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, San Diego, CA, 2018, pp. 198-201. The dissertation author was the primary investigator and author of this paper.

Chapter 5, in full, is currently being prepared for submission for publication of the material as it may appear in: Abdurrahman H. Aljuhani, and Gabriel. M. Rebeiz, "Ultra-Low-Power Low-Noise K-band Phased-Array Receive Beamformer Channel with a Novel High-Resolution Phase Shifter and Low Phase Imbalance Attenuators for K-band SATCOM Applications" in *IEEE Transactions on Microwave Theory and Techniques,* in preparation. The dissertation author is the primary investigator and author of this paper.

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PUBLICATIONS

A. H. Aljuhani, T. Kanar, S. Zihir, and G. M. Rebeiz, "A Scalable Dual-Polarized 256-Element Ku-Band Phased-Array SATCOM Receiver with ±70° Beam Scanning," *2018 IEEE/MTT-S International Microwave Symposium - IMS*, Philadelphia, PA, 2018, pp. 1203-1206.

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ABSTRACT OF THE DISSERTATION

Ku-Band Phased Arrays and K-Band Communication Circuits and Systems in Advanced SiGe and CMOS SOI Technologies for SATCOM On-the-Move Applications

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2020

Professor Gabriel M. Rebeiz, Chair

The use of electronically steerable antennas for Satellite Communication (SATCOM) applications has been limited for many years to mostly defense systems. Those planar phased antenna arrays were not able to penetrate the commercial SATCOM market due to their high cost, complex design, low yield, low production numbers, and time-consuming calibration needed for each antenna unit. This dissertation aims to make affordable SATCOM planar phased arrays with high yield and minimal calibration available for the commercial market. The low-cost phased arrays are not only useful for SATCOM on-the-move (SOTM) terminals, but similar phased-arrays can be built for point-to-point communications and low-power radars.

This dissertation presents two affordable Ku-band dual-polarized receive-only (Rx) and transmit-only (Tx) phased-arrays with 256-elements. The phased antenna arrays can receive or transmit linear, rotated-linear, and circular polarization. Both designs archive state-of-the-art performance with wide-scan angles and high polarization purity. The array designs are based on a low-cost approach where beamformer chips are assembled on a printed circuit board (PCB) with dual-polarized antennas and an integrated Wilkinson combiner/divider network. An affordable and reliable PCB stack-up is developed for both designs and achieves a 100% yield. The two tile designs are scalable to allow large-scale phased-arrays construction with 1024 elements or higher. Also, one phased array can be calibrated, and then, the same calibration coefficients can be applied to different arrays, thereby significantly reducing the calibration time and cost of large-volume commercial arrays. The phased-arrays' near-ideal performance, scalable compact size, low-profile, and ultra-lightweight make them ideal for affordable Ku-band SATCOM terminals.

Another critical parameter that determines the receive phased array size and, consequently, its cost is the required gain-to-noise-temperature (G/T). To maintain high G/T, a packaged low-noise amplifier (LNA) is needed near each antenna element. Therefore, this dissertation also demonstrates the designs of two stable packaged LNAs for a K-band SATCOM receive phased-array using two different technologies (SiGe and CMOS SOI). Both LNAs achieve state-of-the-art packaged performance in terms of gain, NF, and power consumption in both SiGe and CMOS processes. Additionally, a simplified simulation schematic is shown to provide an accurate representation of the packaging effects in a shorter time than the full 3D EM simulation model.

Finally, a K-band phased-array beamformer channel with a novel 8-bit phase shifter and low phase imbalance gain control using 45nm CMOS SOI technology is presented. The channel has a measured peak gain of 24.2 dB with 3-dB bandwidth of 16.4-19.8 GHz and 2.5 dB NF. The

phase shifter has a high resolution of 8-bit with the RMS phase and amplitude error of <1.4° and < 0.3 dB, respectively. Also, the K-band channel offers a 37.2 dB gain tuning range with a fine 0.25 dB step and low phase imbalance due to the added correction capacitors. The achieved performances make this beamformer channel ideal for affordable and high-performance SATCOM K-band receive phased-array systems.

Chapter 1

Introduction

1.1 Background and Motivation

The demands for higher data rates and persistent connectivity over a wide coverage area have been increasing rapidly due to the continuous growth of data traffic and usage. Satellites in the geostationary equatorial orbit (GEO), medium earth orbit (MEO), and low earth orbit (LEO) are potential solutions to meet these demands. They can provide communication and broadcast services to thousands of user terminals over a large geographical area. This primary advantage has encouraged the recent advancements in deploying small communication satellites as well as the massive investments in the satellite-based internet services. These satellite services are going to be essential for providing online access to many users in rural areas.

However, maintaining a high data rate link between the ground unit and the satellite requires the implementation of mechanically or electronically steerable antennas in the user terminal to track GEO satellites for mobile users, or MEO and LEO satellites for fixed and mobile users. Also, the electronically steerable antennas (phased arrays) are preferred over mechanically steerable antennas (reflectors or waveguide plates) because of their lower profile, lightweight, and the absence of maintenance due to non-moving parts. Still, the use of phased array for Satellite

Communication (SATCOM) applications has been limited for many years to mostly defense systems as they were not able to penetrate the commercial SATCOM market due to their high cost, complicated design, low yield, low production numbers, and time-consuming calibration needed for each antenna unit. This dissertation aims to make affordable SATCOM planar phased arrays with high yield and minimal calibration and high-performance communication circuits and systems available for the commercial SATCOM market.

1.2 Thesis Overview

This thesis presents two affordable Ku-band phased arrays with state-of-art performances and low power low noise K-band communication circuits and systems in advanced SiGe and CMOS SOI technologies for SATCOM on-the-move applications.

Chapter 2 presents a Ku-band phased-array receive tile with 256-elements. The 256-elements are spaced 0.52 λ apart at 12.7 GHz in the x-and y-directions. The measured patterns show near ideal patterns with a wide beam scanning range of ±70° (V-and H-pol) and high cross-polarization rejection of 27 dB. The array has a 3-dB instantaneous scanning bandwidth of 10.6-12.5 GHz. In circular polarization mode, the measured axial ratio (AR) is 0.5 dB at 11.75 GHz for both left-hand and right-hand circular polarization. The tile design is scalable to allow large-scale phased-arrays construction with 1024 elements or higher. Extensive measurements are presented, showing the versatility of this low-cost approach. Also, the dual-polarization feeds can be optimized to result in very low cross-polarization for circular and slanted-linear polarizations at all scan angles. The array performance, compact size, ultra-lightweight of 258 grams, and low-profile with 3.5 mm thickness make it suitable for affordable mobile Ku-band SATCOM on the move (SOTM) terminals.

In chapter 3, the thesis presents an ultra-low profile and lightweight Ku-band transmit phased-array with 256 dual-polarized antenna elements for satellite on-the-move (SOTM) terminals. The antennas are placed in a square grid with λ/2 spacing at 14 GHz. At normal incidence, the phased-array results in a measured EIRP of 64.5 dBm and 66.5 dBm at P1dB and Psat, respectively, per polarization. The measured patterns, in E-and H-planes, show almost ideal patterns with a wide scanning range of ±60°, a 3-dB instantaneous bandwidth of 13.0 – 14.6 GHz, and a cross-polarization isolation of 27 dB up to ±45° and 23 dB at ±60° scan angles. In circular polarization mode, the measured axial ratio (AR) is <1.1 dB at 14-14.5 GHz. The phased array is also capable of synthesizing deep nulls (-30 dB to -40 dB) over a wide range of angles, thereby reducing un-intended radiation to geostationary orbit (GEO) satellites. Transmit noise analysis is presented and shows that the array SNR is dominated by the block upconverter (BUC) and not by the beamformers. An EVM of 2.8-3.5% was achieved over a wide scan range for QPSK, 8-PSK, and 16-PSK waveforms with 100 MHz bandwidth. The array near-ideal performance, compact size, low-profile with 3.5 mm thickness, and ultra-lightweight of 212 grams make it ideal for affordable Ku-band SATCOM terminals.

Chapter 4 presents a packaged single-ended three-stage K-band low noise amplifier (LNA) using Jazz SBC18H3 SiGe process technology. The LNA consists of three common emitter (CE) stages to achieve a stable packaged amplifier with a low noise figure (NF) and high gain. The measured gain is 20.3 dB with a 3-dB bandwidth of 7 GHz (14.4 - 21.4 GHz). The measured noise figure (NF) is 2.14 dB at 18.4 GHz, and it is < 2.3 at (17.1– 19.7 GHz). At 18 GHz, the measured IP1dB, OP1dB, IIP3, and OIP3 are -23.7, -4.9, -15.3, and 5.1 dBm, respectively. This is achieved at a power consumption of 18-mW. This represents state-of-the-art packaged K-band LNAs in

terms of gain, NF, and power consumption in SiGe and CMOS processes at the time of publication of this work.

In chapter 4, the thesis also presents a packaged single-ended low-noise amplifier (LNA) for a K-band SATCOM phased-array receiver. The LNA is fabricated in a 45 nm Semiconductor-on-Insulator (SOI) CMOS process technology. It has a measured peak gain of 23.1 dB at 17.4 GHz with a 3-dB bandwidth (BW) of 8.1 GHz (13.9 - 22.0 GHz). The measured NF is 1.5 dB at (15.7 - 17.2 GHz) and it is <1.7 dB at (13.9 - 20.9 GHz). At 18 GHz, the measured IP1dB and IIP3 are -21.6 and -12 dBm, respectively. The CMOS LNA achieved this high gain and low NF with a power consumption of 12.5 mW. At 18 GHz, when the power consumption is increased to 21.6 mW, the measured gain is 24.4 dB, and the measured NF is 1.38 dB. This packaged single-ended CMOS LNA has the highest gain with the lowest NF and power consumption when compared to published packaged and non-packaged K-Band LNAs in SiGe and CMOS processes.

Chapter 5 presents a K-band low-power, low-noise phased-array beamformer channel with a novel 8-bit phase shifter and low phase imbalance gain control using GlobalFoundries 45-nm CMOS SOI. The receive channel has a realized peak gain of 24.2 dB with 3-dB bandwidth of 16.4-19.8 GHz and 2.5 dB NF. The phase shifter has a high resolution of 8-bit to realize the full 360° with the RMS phase and amplitude error of <1.4° and < 0.3 dB, respectively. Also, the channel offers a 37.2 dB gain tuning range with a fine 0.25 dB step and low phase imbalance due to the added correction capacitors. Comparing the single blocks and the channel to previously published work shows both achieved state-of-the-art performance. The lowest NF, high gain, high-resolution phase shifter with low RMS phase and amplitude errors, and large gain tuning range

with small gain step make this beamformer channel suitable for SATCOM K-band receive phased-array systems.

Finally, chapter 6 concludes the thesis with a summary of the presented projects and suggestions for future work.

Chapter 2

A 256-Element Ku-band Polarization Agile SATCOM Receive Phased-Array with Wide-Angle Scanning and High Polarization Purity

2.1 Introduction

The past decade has witnessed growing demands from defense and commercial sectors for higher data rates and connectivity over a wide coverage area. Satellites offer one of the best solutions to meet such demands and can provide communication and broadcast services to thousands of terminals over a large geographical area. In general, a mechanically-scanned or a phased-array user terminal is required to track geostationary equatorial orbit (GEO) satellites (for mobile users), or medium earth orbit (MEO) and low earth orbit (LEO) satellites (for fixed and mobile users). The tracking is needed to ensure an optimal link and high data rate between the satellite and the user.

Antenna systems in SATCOM on the move (SOTM) terminals can be divided into four main types. The first one employs lens or reflectors antennas for their high efficiency and relatively low cost [1-3]. Such terminals are bulky and have a large swept volume. The second type can achieve a lower profile using non-scanned (fixed) antenna arrays [4]. These systems still occupy a

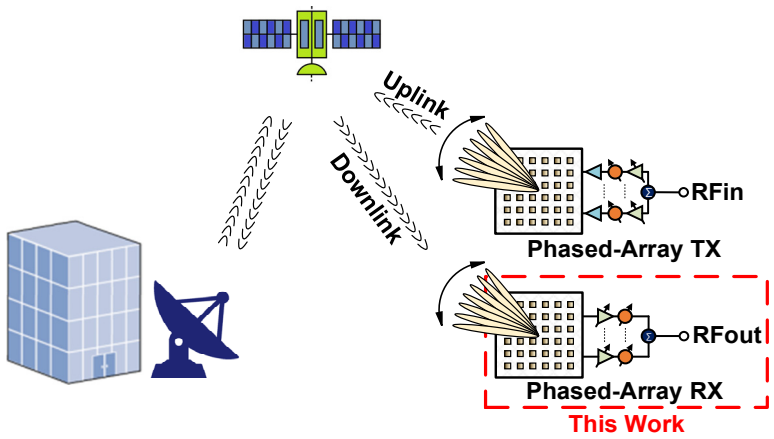

Figure 2.1: Low-cost Ku-band phased-array terminal (RF-front end).

large swept volume due to the need for a mechanical scan in both azimuth and elevation planes. Planar antenna array with a stair structure reduces the swept volume in [5] but still requires several motors for operation. Also, a variable inclination continuous transverse stub (VICTS) array can be used with two motors for scanning in all planes [6]. The third type combines electronic steering in the elevation plane and mechanical beam steering in the azimuth plane [7-9]. These arrays do result in a low profile but still require the use of a motor and thus have moving parts and added maintenance. The fourth type is based on phased-array antennas with full electronic beam steering (Figure 2.1). However, due to their high cost and low production numbers, SATCOM phased-arrays with full electronic beam steering have been generally used in defense systems but were not able to penetrate the commercial SATCOM market [10].

With silicon technology advancement in the past decade, silicon beamformer chips have become essential in the construction of large-scale phased-arrays for satellite communications [10-13], 5G phased-array systems [14-17], and 60 GHz systems [18-20]. With 8, 16, and even 64 phased-array channels on a single chip, they offer a high degree of integration along with biasing circuits and SPI control. Moreover, they can be packaged using quad-flat no-leads (QFN) or ball

grid array (BGA) packages at Ku-and Ka-band, leading to ease of assembly on a printed circuit board (PCB).

This chapter expands on [11] and presents detailed design and measurements of a dual-polarized scalable 256-element Ku-band SATCOM phased-array receiver. Section 2.2 discusses the phased-array design, including architecture and beamformer chips. Section 2.3 presents system analysis for the 256- and 1024-element phased-arrays. The PCB stack-up, stacked-microstrip antenna, and combiner network design are discussed in Section 2.4. Measurement of the Ku-band passive antenna and a 2x2-element phased array are presented in Section 2.5. The phased-array calibration is discussed in Section 2.6. An extensive set of measurements is presented in Section 2.7 to show the capabilities of such arrays in forming several different beams. The beam squint in large arrays is discussed in Section 2.8. Section 2.9 discusses cross-polarization mitigation and associated measurements. Section 2.10 presents the measurement of satellite signals, and section 2.11 concludes the chapter.

2.2 256-Element (16 x 16) Phased-Array Design

2.2.1 Dual-Polarized Phased-Array Architecture

The 256-element array is based on the all-RF architecture with 64-unit cells, with each unit cell consisting of four (2x2) dual-polarized antennas and a silicon beamformer chip. The antennas are implemented on one side of a 12-layer PCB, while the beamformer chips are assembled on the other side.

The beamformer chip has eight receive (Rx) channels, four channels assigned for vertical polarization (V-pol.), and four channels for horizontal polarization (H-pol.), with each channel having an independent phase and gain control. The beamformer chip has two RF outputs, one for

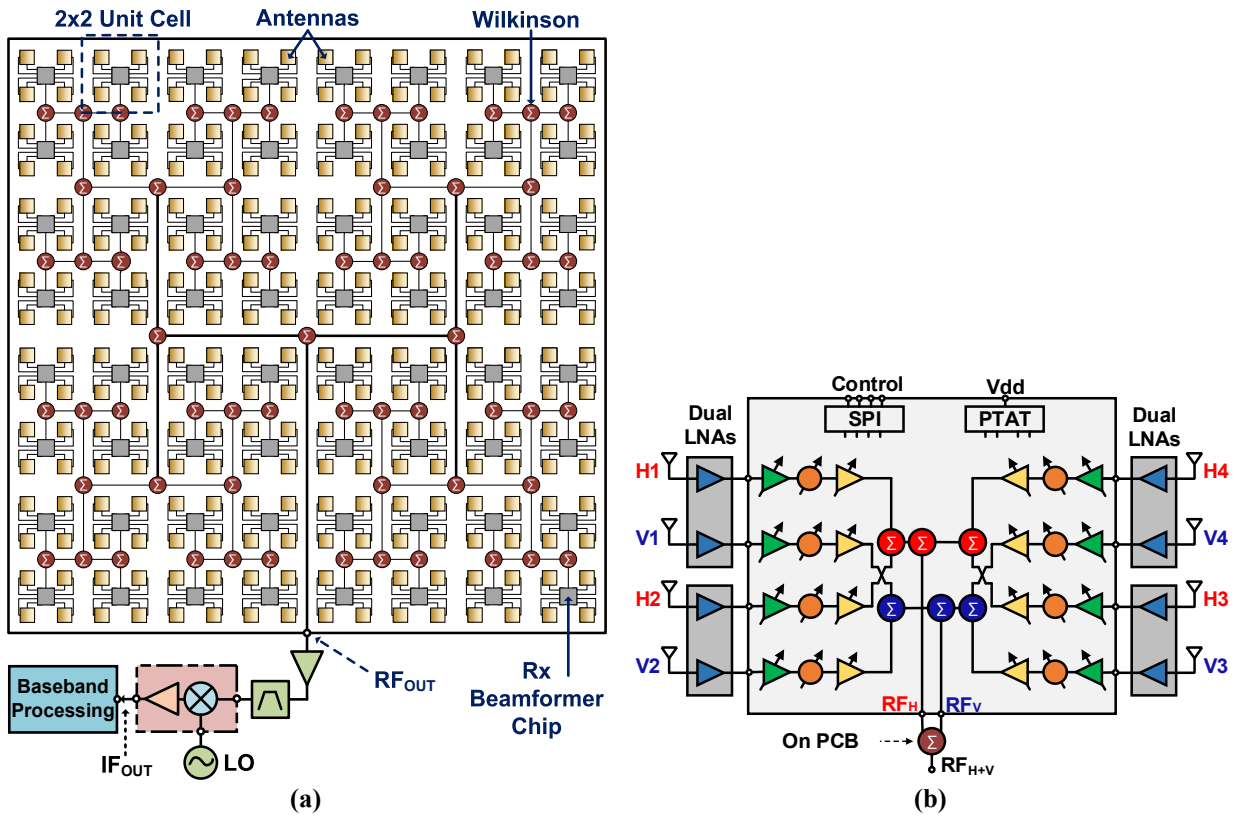

Figure 2.2: (a) A 256-element phased-array SATCOM receiver based on 64 quad beamformer chips. (b) Block diagram of the dual-polarized quad (2x2-elements) receive beamformer chip.

V-pol. and one for H-pol. This chip topology was adopted to allow for two independent beams if needed, each at a different polarization. However, in this implementation, the chip V and H outputs are combined using a Wilkinson network on the PCB just near the chip to result in a single beam with polarization agility. The resulting V+H signals from the 256-element array are then summed using a 64:1 Wilkinson network on the PCB.

An RF amplifier at the array output port is used to compensate for the Wilkinson network ohmic loss. Also, an external downconverter is used. The all-RF beamforming architecture allows for a sharp multi-pole filter before the down-converter to reduce the image response. The dual-polarized architecture with a single output beam allows for a polarization-agile architecture and the reception of linear, linearly rotated, and circular polarizations [Figure 2.2(a)].

2.2.2 Silicon Beamformer Chip

The 8-channel quad-core silicon beamformer chip is shown in Figure 2.2(b) and is based on a silicon-germanium (SiGe) BiCMOS process. Each channel consists of a variable gain amplifier (VGA_1, VGA_2) with 20 dB gain control and 0.5 dB gain steps and a phase shifter with 6-bit phase control with a step size of $5.6°$. The phase shifter RMS amplitude and phase errors are < 0.4 dB and < 2.5° at 11.75 GHz. The 8-channels are combined using two on-chip 4:1 Wilkinson combiner networks for the V- and H-polarization outputs. The Rx channel consumes 53 mW from a 2.3 V supply, and the total power consumption is 13.6 W per polarization (256 elements x 53 mW/element).

The chip receive electronic gain is defined as the measured S_{21} (port 1=antenna port, port 2 = RF output) + 6 dB, since only one channel is excited and the 4:1 on-chip Wilkinson combiner has 6 dB excess loss (this loss is not present if all channels are excited as is the case of a phased-array). The chip results in 14.6 dB electronic gain and 5.3 dB NF at 11.7 GHz, which is acceptable knowing that an external LNA with 17-20 dB gain is used. This LNA is placed next to the antenna port to reduce the loss between the antenna and the LNA.

The chip is controlled using a serial peripheral interface (SPI) and employs a built-in PTAT current source for biasing. With a 4-bit address, 16 chips can share the same SPI lines. The 8-channel chip is packaged in a 6x6 mm^2 40-lead QFN case.

2.3 System Analysis

Figure 2.3 presents the system calculations for the 256-element phased-array based on a 2×2 Ku-Band Rx beamformer core chip. The antenna directivity (D_{ANT}) is obtained using:

$$D_{ANT} = 10 \log_{10}\left(\frac{4\,\pi\,Area}{\lambda^2}\right) \tag{2.1}$$

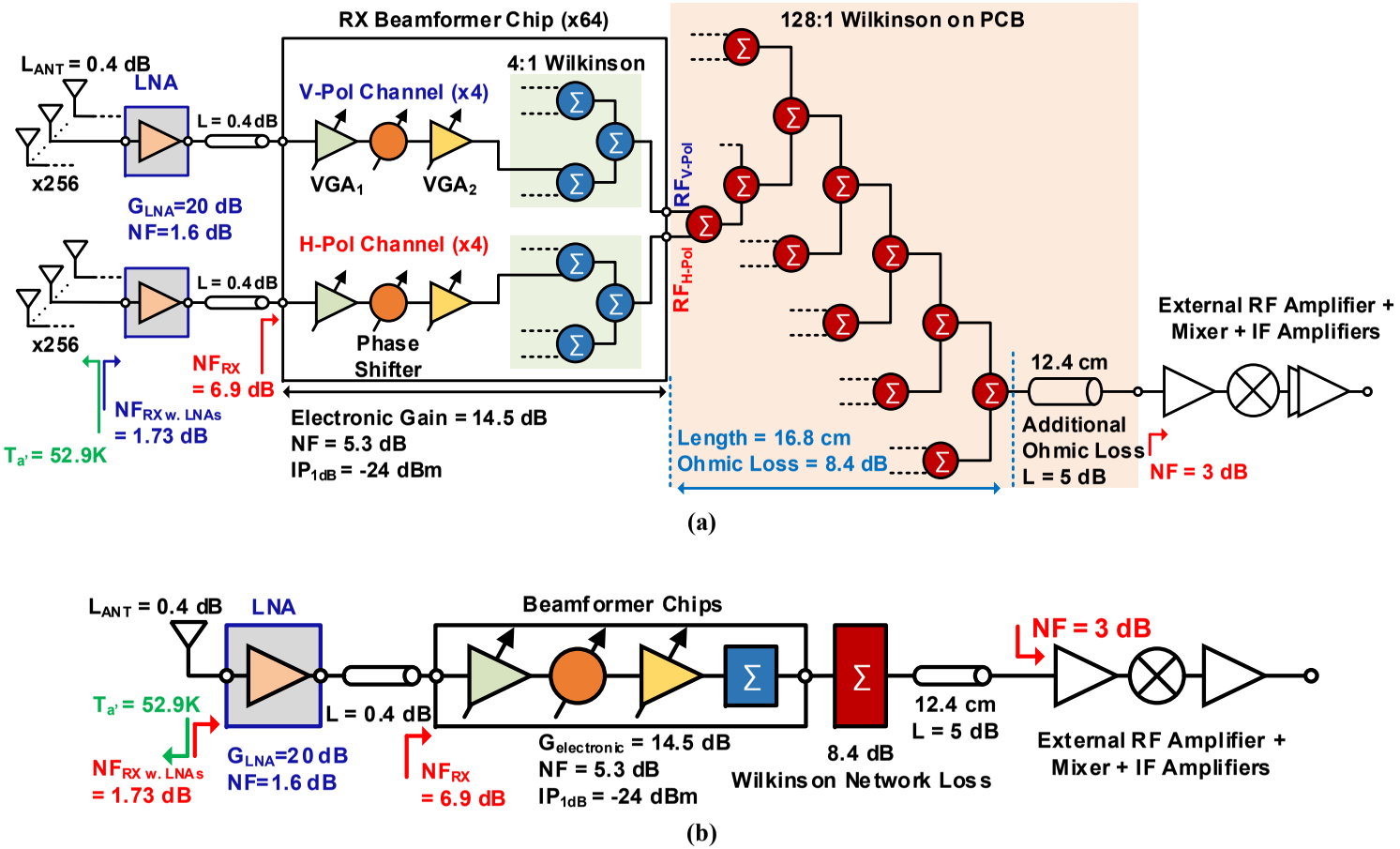

Figure 2.3: (a) System of the 256-element phased-array SATCOM receiver based on a dual-polarized quad (2x2-elements) Ku-Band Rx beamformer chip, and (b) simplified block diagram.

where $Area = (N_x d_x)\,(N_y d_y)$, N_x and N_y are the number of elements in the horizontal and vertical directions, d_x and d_y are the spacing between antenna elements, and λ is the wavelength. The antenna directivity can also be written as:

$$D_{ANT} = 10\ \log_{10}(N) + D_{el} \tag{2.2}$$

where D_{el} is the directivity of a single unit cell and is 4.6 dB at 11.7 GHz for a 0.48 λ x 0.48 λ unit cell, resulting in an antenna directivity of 27.9 - 29.4 dB at 10.7 - 12.7 GHz (28.7 dB at 11.7 GHz). The antenna gain (G_{ANT}) is 28.3 dB at 11.7 GHz given by:

$$G_{ANT} = D_{ANT} - L_{ANT} \tag{2.3}$$

where L_{ANT} is the antenna ohmic and dielectric loss and is simulated to be 0.4 dB at 11.7 GHz (Section 2.4).

The system gain and NF are calculated using the Friis equation and a simplified block diagram [Figure 2.3(b)]. Note that the 128:1 Wilkinson has an ohmic loss of 13.4 dB and has virtually no effect on the system NF as the LNA+beamformer gain is 34.5 dB. The calculated system electronic gain and NF are 20.7 dB and 1.73 dB, respectively, at 11.7 GHz.

The Rx system noise temperature is calculated using:

$$T_{System} = T_S + T_{a'} \tag{2.4}$$

where T_S is the noise temperature defined at the LNA input port, and $T_{a'}$ is the antenna noise temperature at the input of the LNA. T_S is determined using:

$$T_S = T_o\ (F_S - 1)\ =\ 141.9\text{K} \tag{2.5}$$

where T_o = 290K and F_S is the system noise figure. The antenna noise temperature $T_{a'}$ is calculated using:

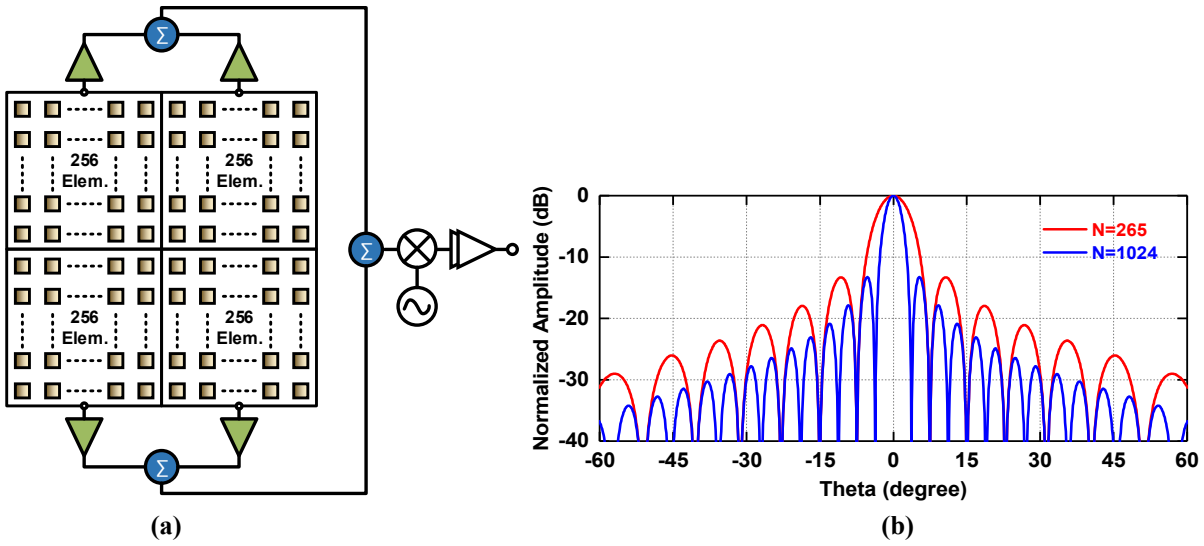

Figure 2.4: (a) Block diagram of how a 1024-element phased-array SATCOM receiver can be constructed using four tiles of scalable 256-element phased-array SATCOM receivers. (b) Simulated co-polarization patterns at broadside at 11.75 GHz with uniform illumination.

$$T_{a'} = \eta_{ANT}\, T_a + \, T_o \,(1 - \, \eta_{ANT}) = 52.9K \tag{2.6}$$

where T_a = 30K is the sky temperature, $\eta_{ANT} = 10^{\frac{-L_{ANT}}{10}}$, L_{ANT} is the antenna loss of 0.4 dB. The gain-to-noise-temperature (*G/T*) value with the external LNA is:

$$\frac{G}{T} = G_{ANT} - 10\ \log_{10}\left(T_{System}\right) = 5.4\ \text{dB/K} \tag{2.7}$$

The 256-element phased-array can also be used as a building block for a tile 1024-element phased-array [Figure 2.4(a)]. Figure 2.4(b) presents the simulated uniform illumination patterns at 11.75 GHz of the 256- and 1024-element phased-arrays. The directivity is 28.7 - 37.7 for a 256 - 1024 element array, respectively. Also, the *G/T* increases from 5.4 dB/K to 11.4 dB/K (Table 2.1). The G/T is expected to drop by 0.3-0.4 dB if mismatch loss between the antenna and the LNA is also taken into consideration.

At the time of this phased-array build, affordable dual-channel Ku-Band GaAs or CMOS LNAs were not available, and, therefore, the LNAs were not used. For the 256-element phased-

Table 2.1: System calculations of 256-and 1024-element phased-array SATCOM receivers

Parameter	Unit	Value	
Frequency	GHz	11.7	
Wavelength	cm	2.55	
Number of Elements		256	1024
Antenna Directivity	dB	28.7	34.7
Antenna Loss	dB	0.4	
Antenna Gain	dB	28.3	34.3
Rx noise Figure	dB	1.73	
Antenna Noise Temperature ($T_{a'}$)	K	52.9	
Rx Noise Temp (T_{system})	K	194.8	
G/T	dB/K	5.4	11.4

array, the system electronic gain reduces to 0.7 dB when both polarizations are active, and -2.3 dB when one polarization is active (due to a 3 dB excess loss in the first Wilkinson network), and the system noise figure, defined at the beamformer chip input port, increases to 6.9 dB. Still, the array performance shown in this chapter contains all the attributes of the complete array except for a higher NF and a lower *G/T*.

2.4 Microstrip Antenna and Combiner Network

2.4.1 PCB

The PCB stack-up is based on Panasonic Megtron-6 prepreg and core layers with $\varepsilon_r = 3.24 - 3.63$ and $tan\delta = 0.004$ at 12 GHz. It has 12 metal layers (M1-M12), two mechanical drilled vias (Via16 and Via1-12), and one laser-drilled via (Via12), as shown in Figure 2.5.

The beamformer chips are placed on M1, and grounded coplanar waveguide (GCPW) lines are used to connect the antenna ports to the RF ports. M1-M5 metal layers are used to distribute RF signals, digital routing, and DC supply. M10 and M12 are used for the antenna layers, and M6

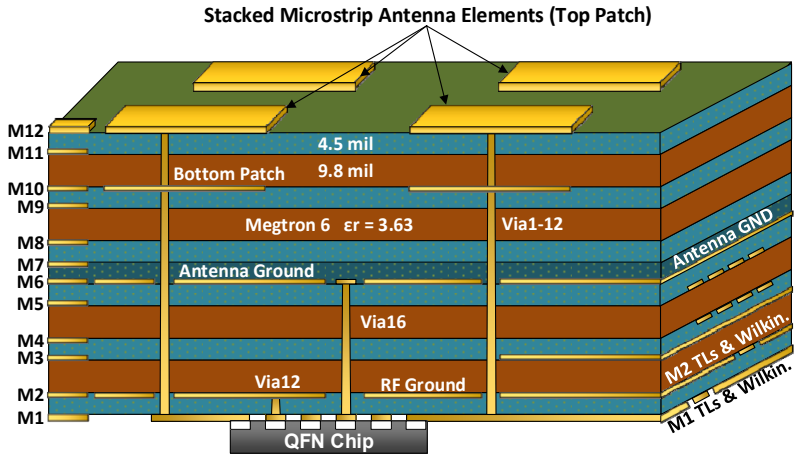

Figure 2.5: Printed circuit board stackup details

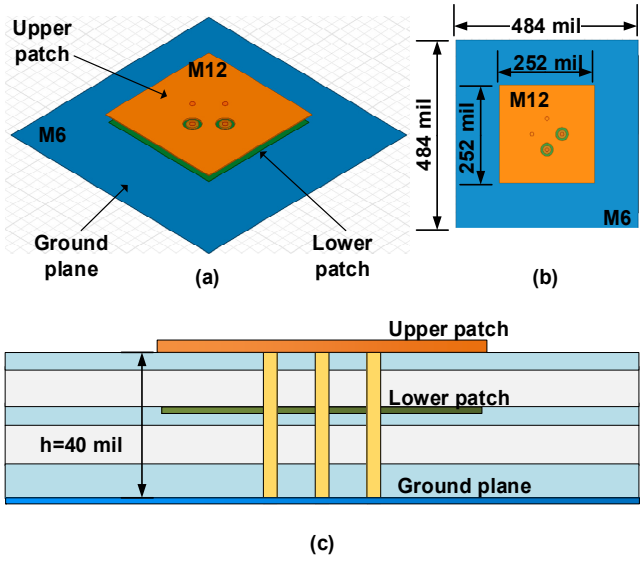

Figure 2.6: Dual polarized stacked microstrip patch antenna unit cell. (a) 3-D view. (b) Top view. (c) Side view.

is used for the antenna ground layer. M7-M9 and M11 layers are not used in this design, but they were included to improve the antenna bandwidth.

2.4.2 Dual-polarized Antenna

The dual-polarized antenna is a square microstrip stacked-patch antenna with dual-probe feeds for the V and H polarizations. A microstrip antenna is chosen due to its advantages, such as low-profile and ease of manufacturing [21]. Figure 2.6(a) presents the phased-array unit cell with

a 0.48 λ x 0.48 λ grid at 11.75 GHz. The lower patch (M10) is the probe fed patch, while the upper patch (M12) is the parasitic patch. The substrate thickness to the antenna ground on M6 is ~ λ_d/13 at 11.75 GHz. The coaxial transition (M1-M6) with grounded coaxial vias is simulated using ANSYS HFSS, and matching networks are used on M1 between the antenna and chip RF ports [Figure 2.7(a)].

The simulated antenna reflection coefficient at broadside referenced to the chip input port is < -10 dB at 11.2-13 GHz [Figure 2.7(b)]. The antenna impedance varies versus scan angles, as shown in Figure 2.7(c) for the V-pol. in the H-plane and Figure 2.7(d) for H-pol. in the E-plane. The antenna design is symmetric so that the other horizontal and vertical polarizations result in identical responses.

The 2x2 unit cell in Figure 2.7(a) is also used to simulate the port-to-port coupling, where P1 is the common output port, P2-3 are the chip output ports (V and H-pol.), P4-P11 are the eight input ports, and P12-P19 are the antenna ports. The highest coupling is < -46 dB at 10-12 GHz and is found for $S_{9,16}$ and $S_{8,17}$, where energy from antenna V-pol feed (or antenna H-pol feed) is fed to the adjacent channel input port [Figure 2.7(e)]. This is an insignificant amount of coupling, knowing that the coupling between the V and H-pol ports on the same antenna is -24 dB at 11.7 GHz (Section 2.5).

The simulated co-and cross-polarization frequency responses are shown in Figure 2.8. The 3-dB antenna bandwidth for both polarizations (V- and H-pol) is 10.8 – 12.9 GHz. The simulated ohmic loss at 11.75 GHz of the antenna, feed line, matching network, and matching loss $(1 - S_{11}^2)$ is 0.65 dB in the E- and H-planes. At 11.75 GHz, the simulated cross-polarization isolation is > 19 dB and > 15.5 dB for a $60°$ scan angle in the E and H-plane, respectively. A technique to improve the cross-polarization isolation to 27 dB over the whole scan range is presented in Section 2.9.

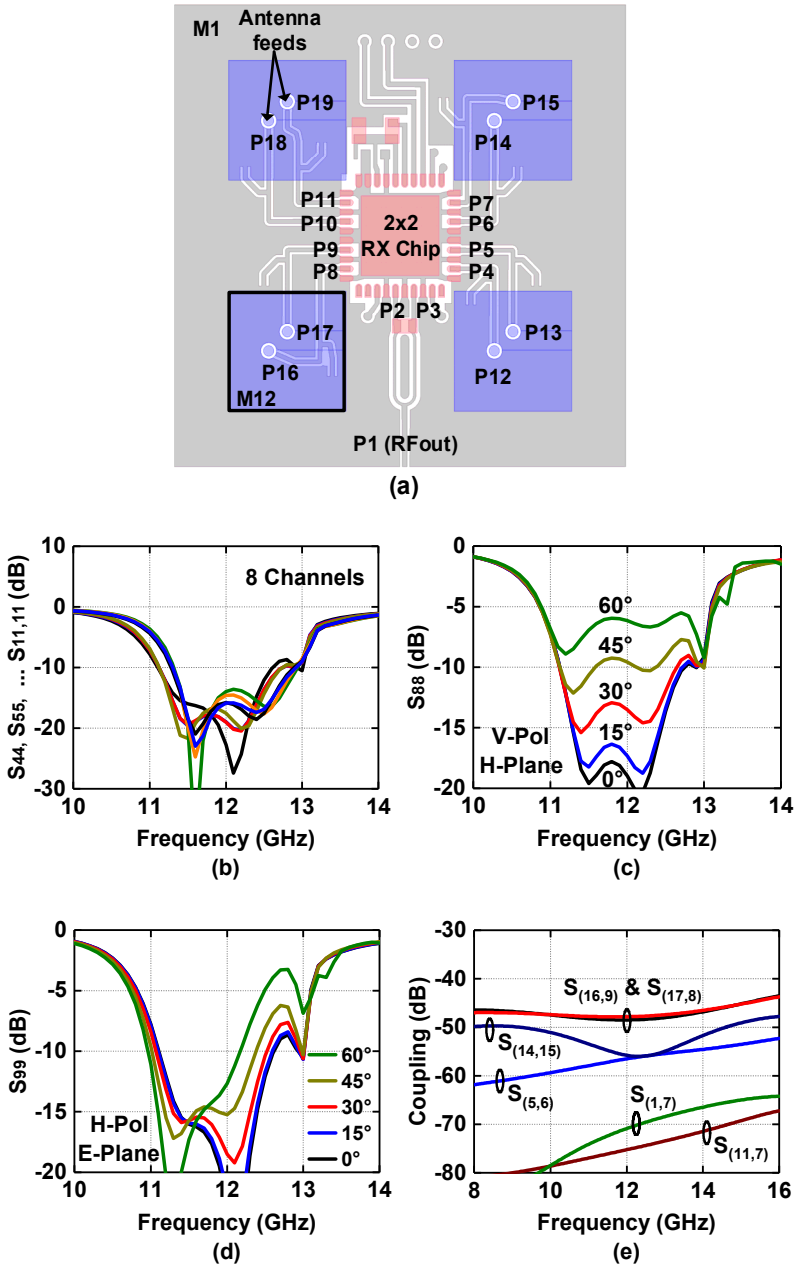

Figure 2.7: (a) 2x2 unit cell's PCB design (M1 and M12 are shown). Simulated antenna impedance at the input chip port of (b) all 8 channels at broadside, (c) vertical polarization (H-Plane), and (d) horizontal polarization (E-Plane) versus scan angles. (e) Simulated port-to-port coupling on the PCB.

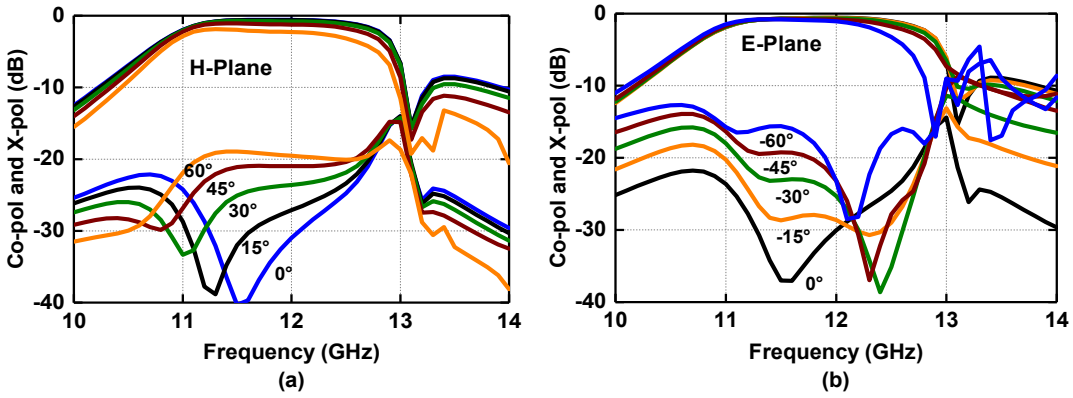

Figure 2.8: Co-and cross-polarized frequency response for different scan angles in, (a) H-Plane (V-pol.), and (b) E-Plane (H-pol.).

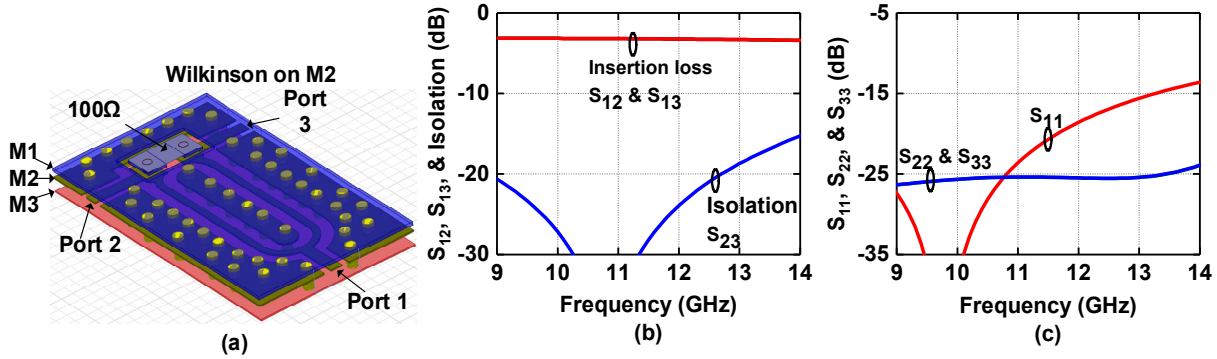

Figure 2.9: (a) Wilkinson combiner design on M2 (b) insertion loss and isolation, (c) matching. (Simulated in ANSYS HFSS and all port are 35 Ω).

2.4.3 Wilkinson Combiner Network

The 7-stage Wilkinson combiner network employs two different configurations for the Wilkinson combiners. The first realizes the Wilkinson combiner using M1/M2 in a grounded coplanar waveguide (GCPW) configuration. This Wilkinson is designed with a 50 Ω characteristic impedance and a lumped 100 Ω resistor for isolation and has a simulated loss of 0.2 - 3 dB at 10 – 13 GHz and an isolation of 20 dB.

To minimize any radiation or coupling to the antenna feed, a second Wilkinson configuration is used with the combiner built using (M1/M2/M3) in a stripline structure and with

ground planes on M2 and M3. The M2 Wilkinson is shown in Figure 2.9(a) with a 35Ω characteristic impedance. It has a simulated loss of 0.15-0.3 dB and > 20 dB isolation at 10-12.8 GHz [Figure 2.9 (b,c)].

2.5 Antenna and 2x2 Array Measurements

2.5.1 Passive Antenna

A passive array is first fabricated with four antennas connected to RF coaxial ports and surrounded by 12 dummy antennas terminated with 50 Ω resistors. Two passive arrays are placed in an antenna chamber, and the system S_{21} was measured using a Keysight network analyzer (Figure 2.10). The far-field Friis transmission equation contains (G_{ANT}^2), and therefore, one can easily deduce the antenna response versus frequency.

Figure 2.11 (a) presents the normalized V- and H-Pol frequency response of a single patch antenna. The measured 3-dB bandwidth is 10.7 – 12.7 GHz, and the antenna provides an image rejection of 21 – 27 dBc at 6.3 – 8.3 GHz, for an LO of 9.5 GHz. The measured S_{11} for both polarizations is <-10 dB at 10.7 – 12 GHz [Figure 2.11 (b)], and the measured coupling between the V and H-feeds in the same antenna is < -19 dB at 10.7 – 12.6 GHz [Figure 2.11 (c)]. Mutual coupling measurements between neighboring antennas show < -26 dB and < -19 dB coupling in the E and H-planes, respectively, at 10.7-12.7 GHz (not shown for brevity).

2.5.2 2x2 Phased-Array Measurements

A 2x2 phased-array with a single beamformer chip is also measured over-the-air to obtain the performance of a single unit cell. An S_{21} 3-dB bandwidth of 10.7-12.5 GHz is obtained, and as expected, the beamformer chip improves the image rejection to 43 – 34 dBc at 6.5 – 8.3 GHz for

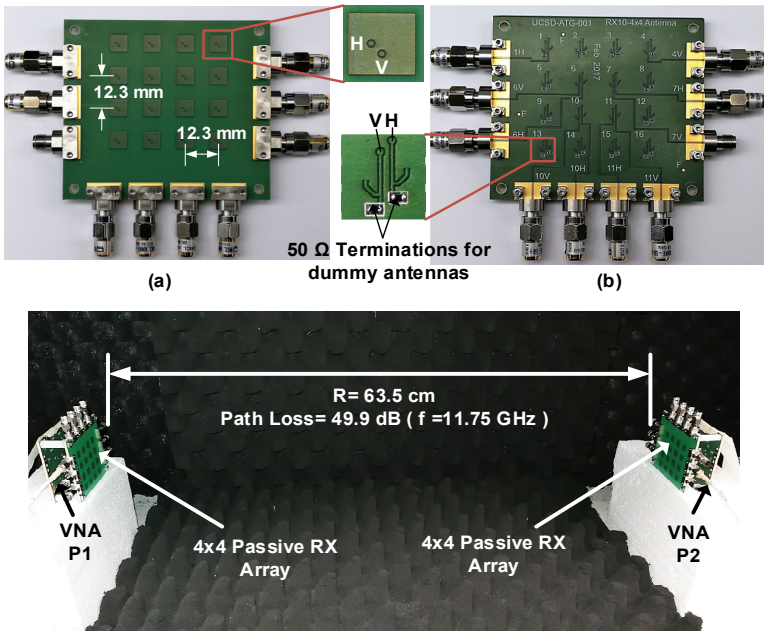

Figure 2.10: 4x4 elements antenna passive test board. (a) Antenna side. (b) Bottom side. (c) Measurement setup of the passive antenna element.

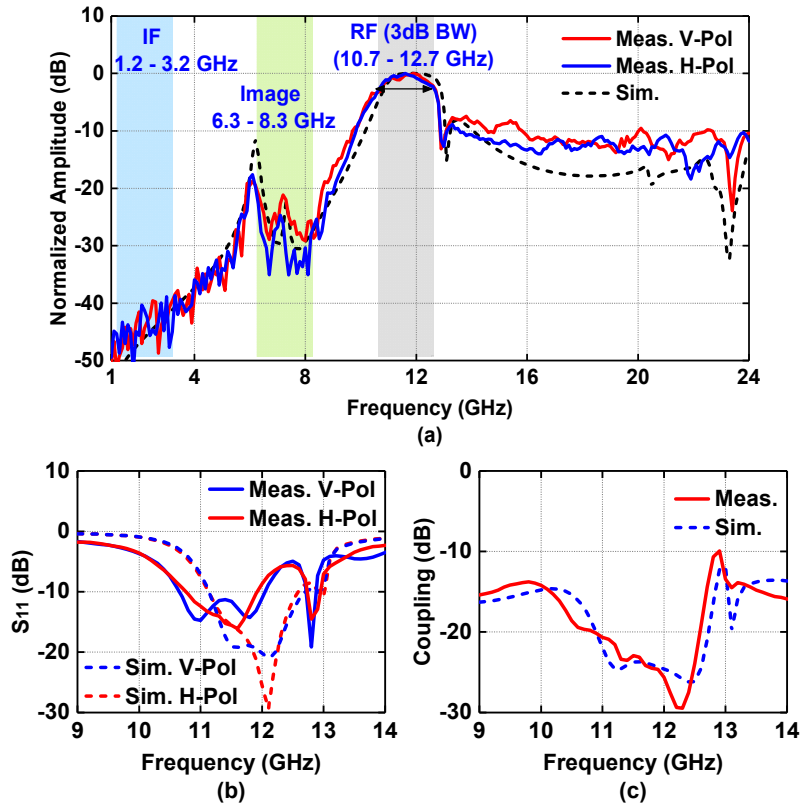

Figure 2.11: Simulated and measured single antenna (a) co-polarized frequency response, (b) input impedance (S11), and (c) coupling between V and H ports in the same antenna.

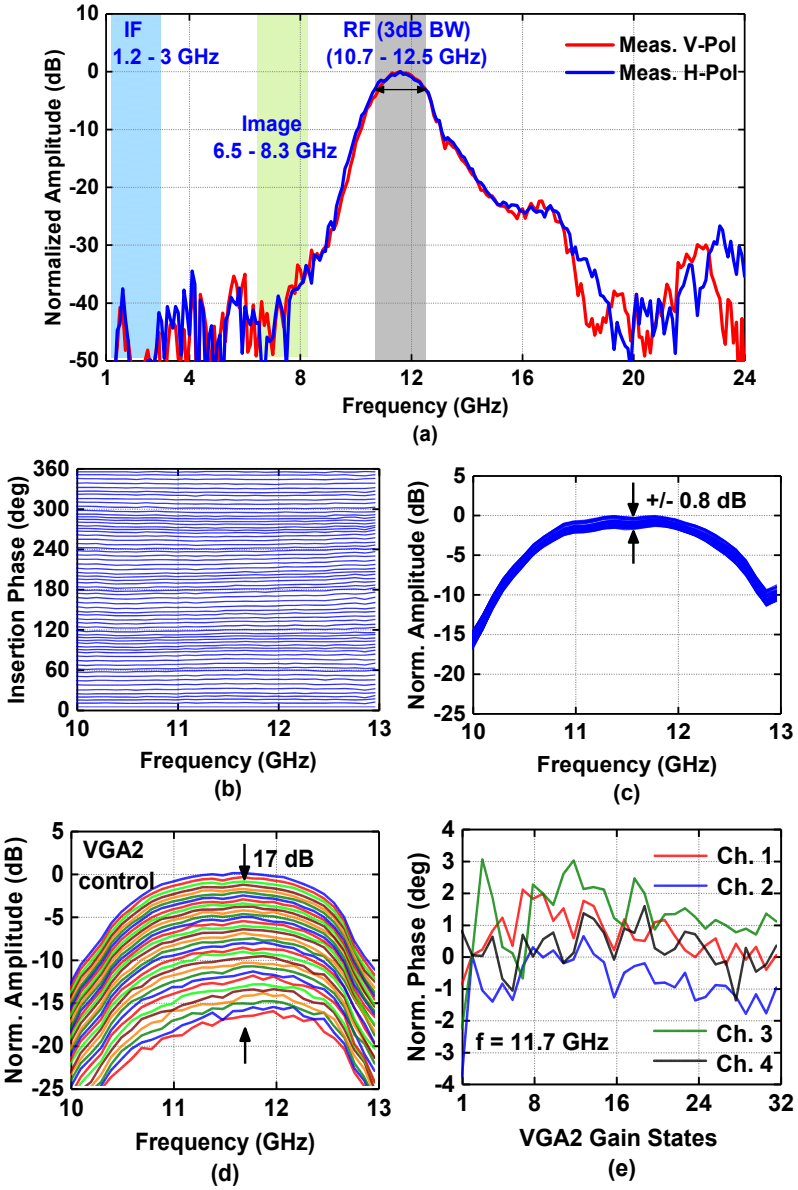

Figure 2.12: (a) Measured co-polarization active frequency response for vertical, and horizonal polarizations. Measured over-the-air (b) channel's phase states, (c) channel's gain changes with all phase states, (d) channel's 2nd VGA gain states, (e) phase change with 2nd VGA gain states for 4 channels (vertical polarization).

an LO of 9.5 GHz [Figure 2.12(a)].

Figure 2.12 (b) presents the insertion phase of a single channel in the 2x2 array. The 6-bit phase shifter is toggled, and the corresponding change in phase and gain is recorded. At 10-13 GHz, the measured RMS amplitude and phase errors are 0.5 dB and 3.2°, respectively. The

variable gain amplifier (VGA_2) gain states and the corresponding phase change at 11.75 GHz are shown in Figure 2.12 (d, e). Each channel results in 17 dB gain control using 5 bits of gain control (< 0.5 dB gain steps) and with ±2.5° phase change over the entire gain control range. Note that there is an additional 3.5 dB gain control in VGA_1. Therefore, the total gain control for each Rx channel is 20.5 dB. The phase and gain control are virtually orthogonal. That is, phase control does not change the gain, and gain control does not change the phase. This greatly simplifies the phased-array calibration.

2.6 Calibration

Figure 2.13 presents the scalable dual-polarized 256-element Ku-band phased-array tile with a size of 19.7 x 22.2 cm^2. The 64 Rx SiGe QFN packaged chips are clearly shown on the backside. The rectangular patches are the solder pads for small heat sinks to remove the heat in a 2-dimensional fashion from the board. These were not used due to the low power consumption of the chips. The tile design is scalable on three sides (top, left, and right), and only the lower PCB side is extended for the DC, SPI, and RF connections. This allows the construction of 1024-2048 element phased-arrays using 2xN tiles [Figure 2.4(a)].

The on-chip and the PCB Wilkinson networks are laid out symmetrically, thereby resulting in equal-distant feedlines from the array common-port to each channel. Therefore, the only electrical length variation is due to the feed lines between the antenna ports on M1 and the chip input ports, which are kept as short as possible to reduce the ohmic loss.

The phased array was measured at a range of R=1.85 m (between D^2/λ and $2D^2/\lambda$) using a VNA and a standard gain horn antenna [Figure 2.14]. Two motorized configurations were used for precise measurements: the first motor was to rotate the array and measure the scanned patterns, while the second motor was used to rotate the horn antenna for cross-polarization measurements.

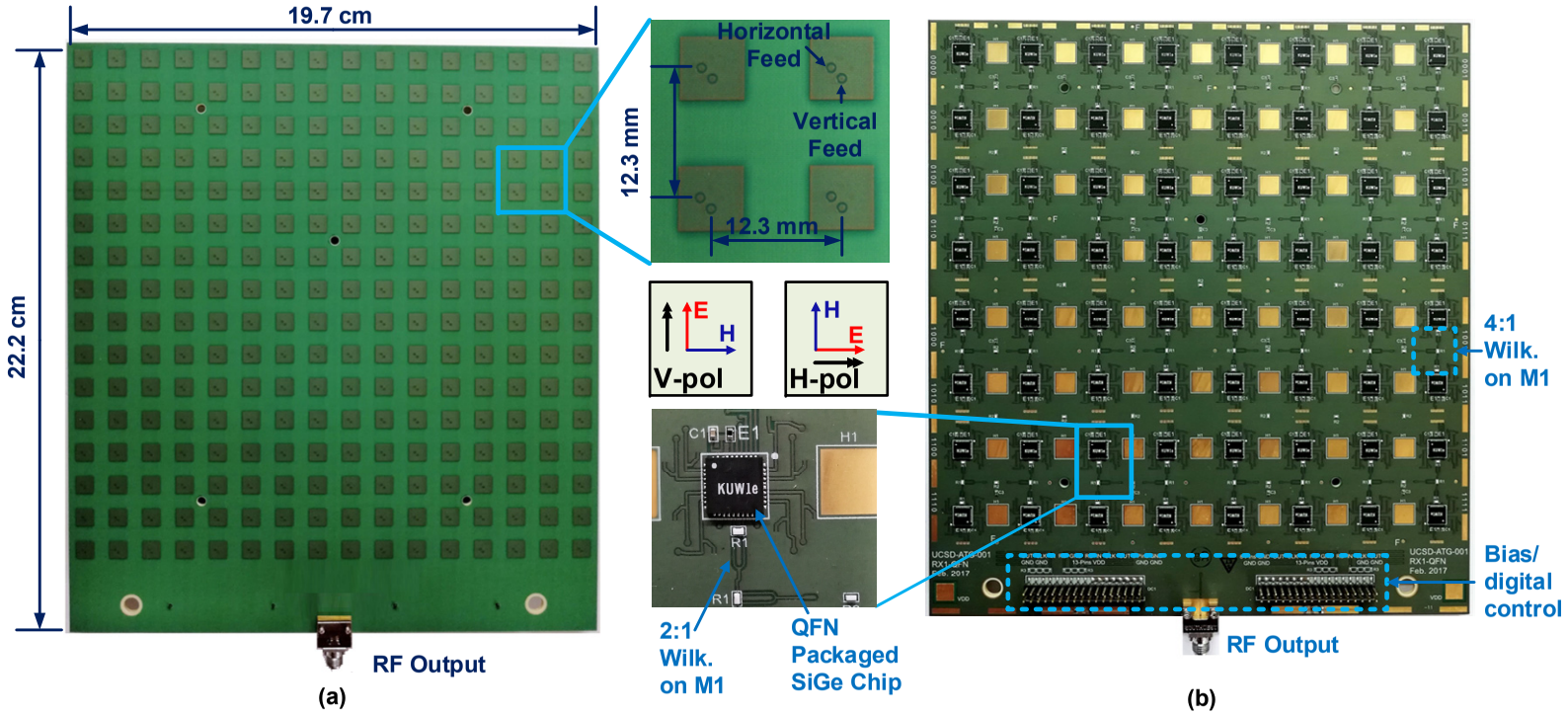

Figure 2.13: (a) Front view showing dual-polarized antennas. (b) Back view of a Ku-band 256-element phased-array showing 64 RX QFN packaged chips.

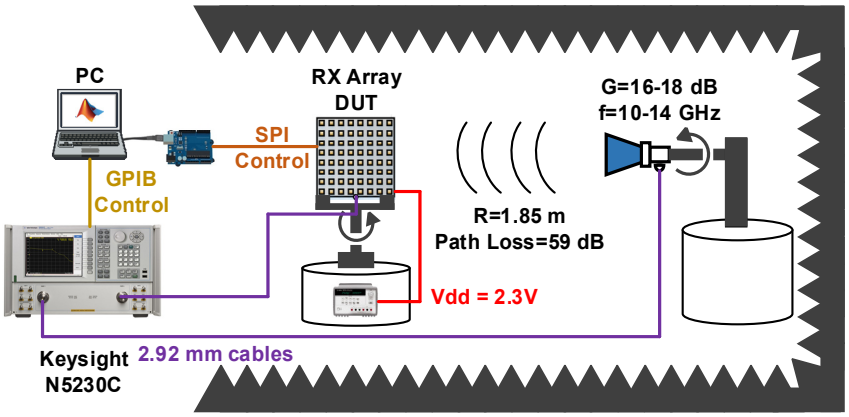

Figure 2.14: Array calibration and pattern measurement setup.

To calibrate the phased array, the antenna elements are turned-on individually, and the far-field S_{21} is measured in the nominal gain state and with the phase shifter set to 0°. After this is completed for 2x256 channels, one antenna channel phase is set at 0°, and the measured phases for all other antenna channels are used as calibration offsets. The final step is to remeasure S_{21} of the antenna elements individually after the calibration is applied to confirm that the calibration is acceptable. There was no need to measure all the 6-bit phase and 6-bit gain states for each channel due to the low RMS gain and phase errors in the phase shifter, and low phase variation in the VGAs. This significantly reduced the calibration time.

Figure 2.15 presents the measured far-field phase of the 256 V- and H-channels before and after phase calibration. The RMS phase error was reduced to 2.5°- 3.7° after phase calibration. The RMS amplitude error across the array is 1.4-1.5 dB for the V- and H-polarization and was not calibrated further (Figure 2.16).

This amplitude error is caused by the Wilkinson network power division mismatch, electronic channel gain variations, and the variability in the phase shifter gain versus phase settings (±0.8 dB). Using the gain control in each channel, the differences in amplitude can be easily corrected. However, for all the measured results, only phase calibration was performed.

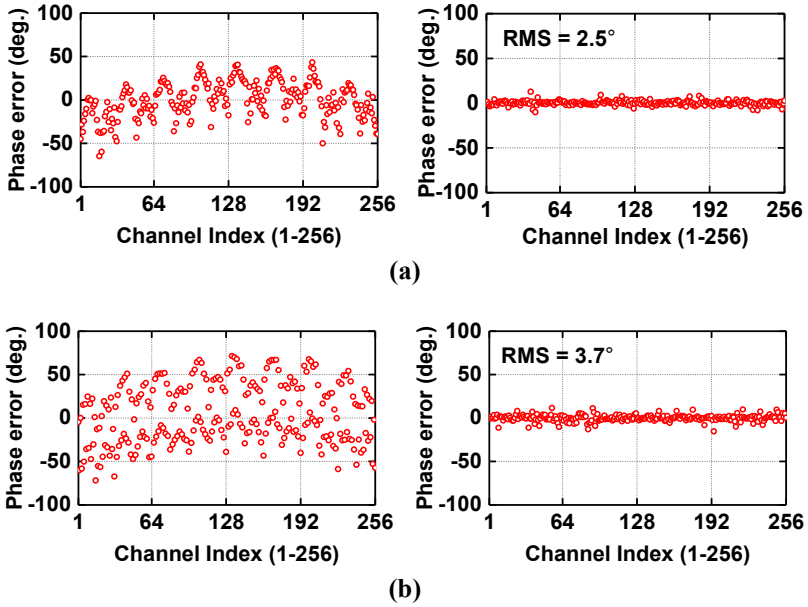

Figure 2.15: Measure far-field phase before and after phase calibration at 11.75 GHz: (a) vertical polarization, and (b) horizontal polarization.

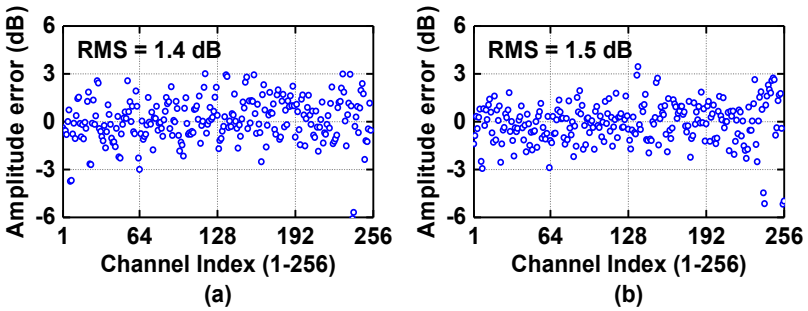

Figure 2.16: Measured far-field amplitudes without calibration at 11.75 GHz: (a) vertical polarization, and (b) horizontal polarization.

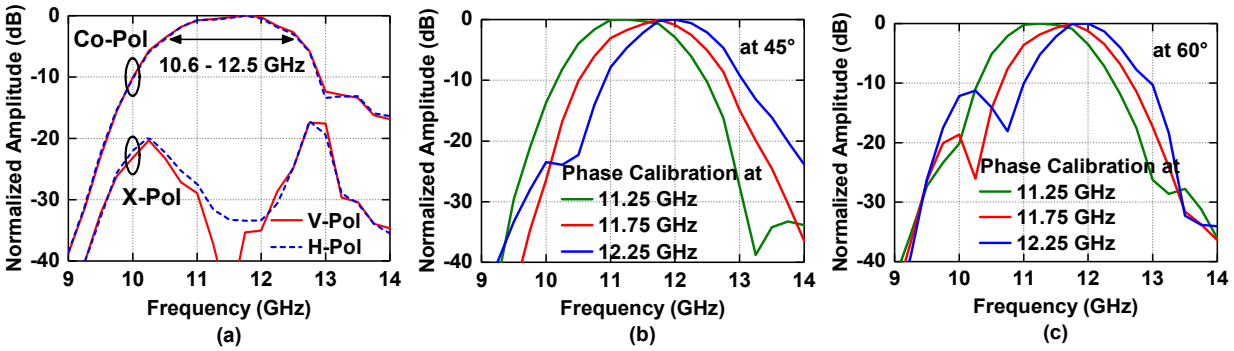

Figure 2.17: (a) Measured co-and cross-polarized frequency response at broadside for vertical and horizontal polarizations. Measured co-polarized frequency response for horizontal polarizations at (b) 45°, (c) 60° scan angles.

2.7 Measurements

2.7.1 Frequency Response

Figure 2.17(a) presents the measured normalized phased-array co- and cross-polarized frequency response for the vertical and horizontal polarization at broadside. The phased-array achieves a 3-dB instantaneous bandwidth of 10.6 - 12.5 GHz at broadside with < -27 dB cross-pol. levels. A nearly identical response is obtained if the phase calibration is done at 11.25 GHz or 12.25 GHz, showing that the frequency response is mostly due to the antenna and beamformer chip response.

The phased-array electronic gain, defined as the power at the common RF port divided by the power incident on the antenna aperture, can also be determined by re-writing the Friis transmission equation as:

$$\begin{aligned} P_{RX\ (at\ common\ port)} &= P_{inc} G_{RX(electronic)} \\ &= S\ Area\ G_{RX(electronic)} \\ &= \frac{P_t G_t}{4\pi R^2}\ Area\ G_{RX(electronic)} \end{aligned} \tag{2.8}$$

where $Area$ =Antenna aperture = 19.7 x 19.7 cm^2, S is the plane-wave power density at the aperture, P_t, G_t are the power and gain of the transmit horn, and $G_{RX(electronic)}$ is the phased-array electronic gain, also shown in Figure 2.33(b) (but without the LNA). The measured $G_{RX(electronic)}$ is -2.6 dB [0 dB normalized level in Figure 2.17(a)] and agrees well with Figure 2.4(b) when taking into account the antenna loss and an additional 3 dB Wilkinson loss since only one polarization is activated.

The frequency response at 45° and 60° scan angle for the H-pol (E-plane scan) are shown in Figure 2.17 (b, c). Note that when the beam is scanned, the 11.75 GHz calibration results in a

narrower bandwidth than the broadside setting, and this is due to beam squint, which limits the 3-dB bandwidth to 1200-1000 MHz at 45° and 60°scan angle (see Section 2.8). If the array is recalibrated in phase at 11.25 GHz or 12.25 GHz, then a much better response can be obtained at these center frequencies with similar 3-dB bandwidths.

2.7.2 Linear Polarization

Figure 2.18 presents the measured active element patterns at 11.5, 11.75, and 12.0 GHz for H-pol. (E-plane) and V-pol. (H-plane). The patterns are measured in the azimuth plane with one of the columns (1x16 elements) turned ON. In the E-plane, the active-element pattern fits a $\cos^{1.1}(\theta)$ roll-off with a 5.1 dB drop at ±70°, while the H-plane pattern fits a $\cos^{1.3}(\theta)$ roll-off with a 6 dB drop at ±70°. This is typical in microstrip antennas due to the far-field electric-field being parallel to the PCB ground plane in the H-plane.

Figure 2.19 presents the measured co-and cross-polarization patterns at broadside at 11.75 GHz with uniform illumination for the vertical polarization (H-plane) and the horizontal polarization (E-Plane), again using an azimuth scan. Both patterns are near-ideal and match simulations with cross-polarization levels of < -32 dB and sidelobe levels of < -13 dB. The theoretical scan patterns are determined using:

$$P\ (\theta) = \ AF\ (\theta)\cos^{n}(\theta) \tag{2.9}$$

where $\cos^{n}(\theta)$ is a simplified microstrip-antenna pattern ($n = 1.1 - 1.3$), and AF is the phased-array factor given by:

$$AF\ (\theta) = \sum_{n=1}^{N} I_n\, e^{jnkd_x\ \sin(\theta)} \tag{2.10}$$

and $I_n = e^{-jnkd_x\ \sin(\theta_s)}$ is the excitation phase for uniform illumination imposed on the nth element

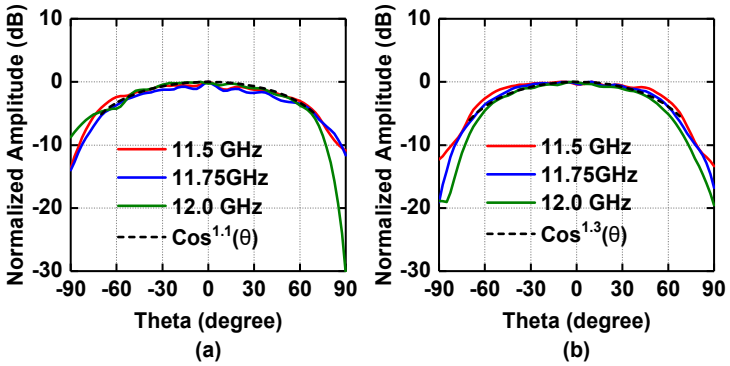

Figure 2.18: Measured co-polarization active patterns: (a) E-Plane (H-Pol). (b) H-Plane (V-Pol). Measurements done in the Azimuth plane for one array column with 1x16 elements active.

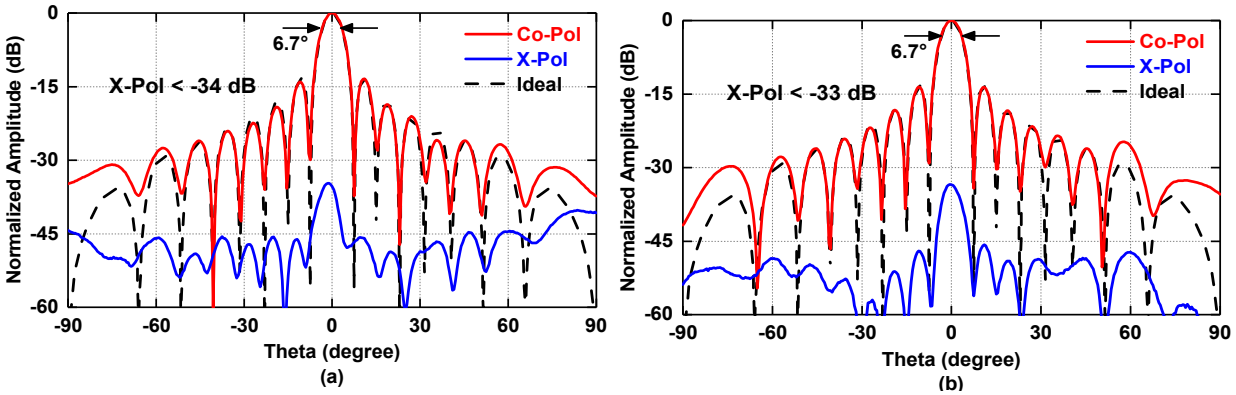

Figure 2.19: Measured co-and cross-polarization patterns at broadside at 11.75 GHz with uniform illumination. (a) Vertical polarization (H-Plane). (b) Horizontal polarization (E-Plane).

for a scan angle of θ_s, $k = {}^{2\pi}/_{\lambda}$ is the wavenumber, and d_x is the element spacing.

The dual-polarized phased-array has symmetric antenna elements placed in a symmetric x-y grid. Therefore, the patterns of the V-and H-polarizations in the E-plane are expected to be the same. Similarly, the H-plane patterns for the V-and H-pol are also expected to be the same. This is clearly shown in Figure 2.20 at different scan angles. In the E-and H-planes, the 3-dB beamwidth increases from 6.7° at boresight to 12.5°-16° at 60°-70° scan angle. The 3-dB beamwidth is determined using:

$$\theta_{3dB} = \frac{0.886\,\lambda}{L\,\cos(\theta_s)} \tag{2.11}$$

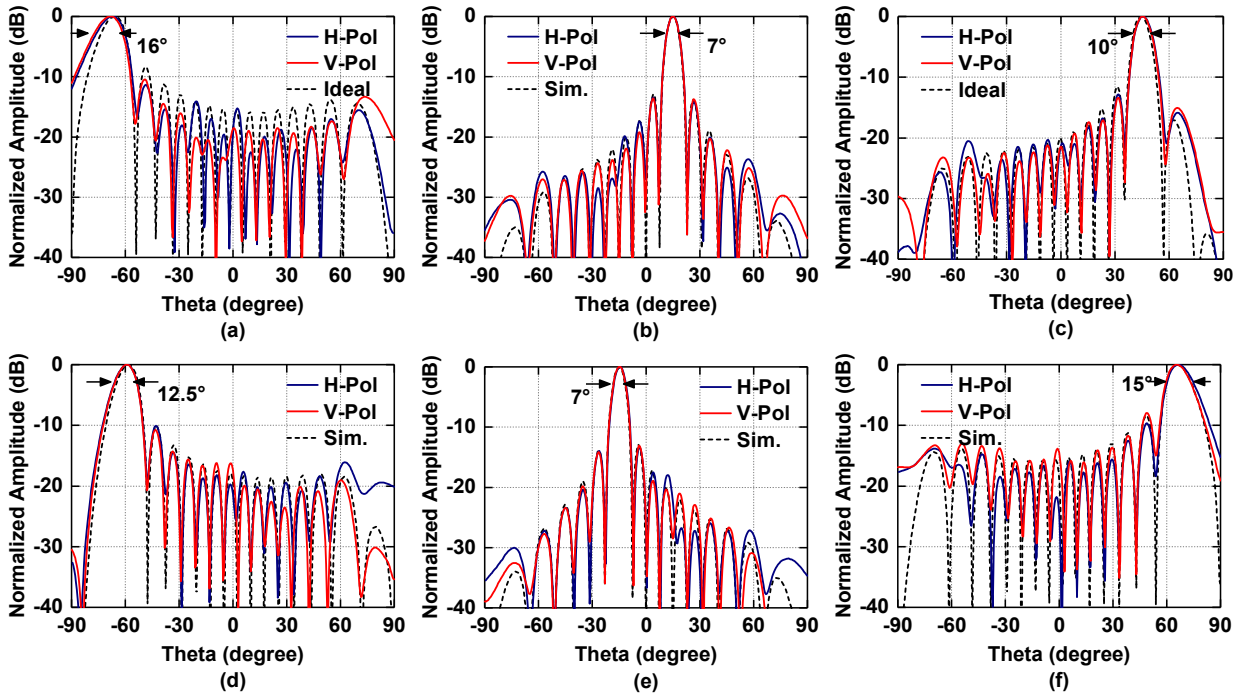

Figure 2.20: Measured co-polarized (E-plane) patterns at (a) -70°, (b) 15°, and (c) 45°. Measured co-polarized (H-plane) patterns at (d) -60°, (e) -15°, and (f) 70°. (shown for vertical and horizontal polarizations at 11.75 GHz with uniform illumination).

where $L = N_x d_x$ is the array length. The first sidelobe level increases from -13.3 dB at boresight to around -10 dB at ±70° scan angle, as expected, and is due to the drop in the element pattern gain at wide scan angles.

To reduce the sidelobes levels, an 8-dB raised-cosine taper illumination is applied on the antenna aperture using VGA2. The normalized amplitude of the elements is set by:

$$I_n = \alpha + (\alpha - 1)\cos\left(\frac{2\pi\,(n-1)}{N-1}\right) \tag{2.12}$$

where $\alpha = \frac{1+10^{-X/20}}{2}$ is a constant given by the edge taper X in dB ($X = 8$). The measured tapered patterns show a 3-dB beamwidth of 7.8° at broadside, together with a -22 dB sidelobes level (Figure 2.21). The lack of amplitude calibration is now seen in the measured patterns as some sidelobes are a bit higher or lower than simulations. Still, excellent patterns are achieved with

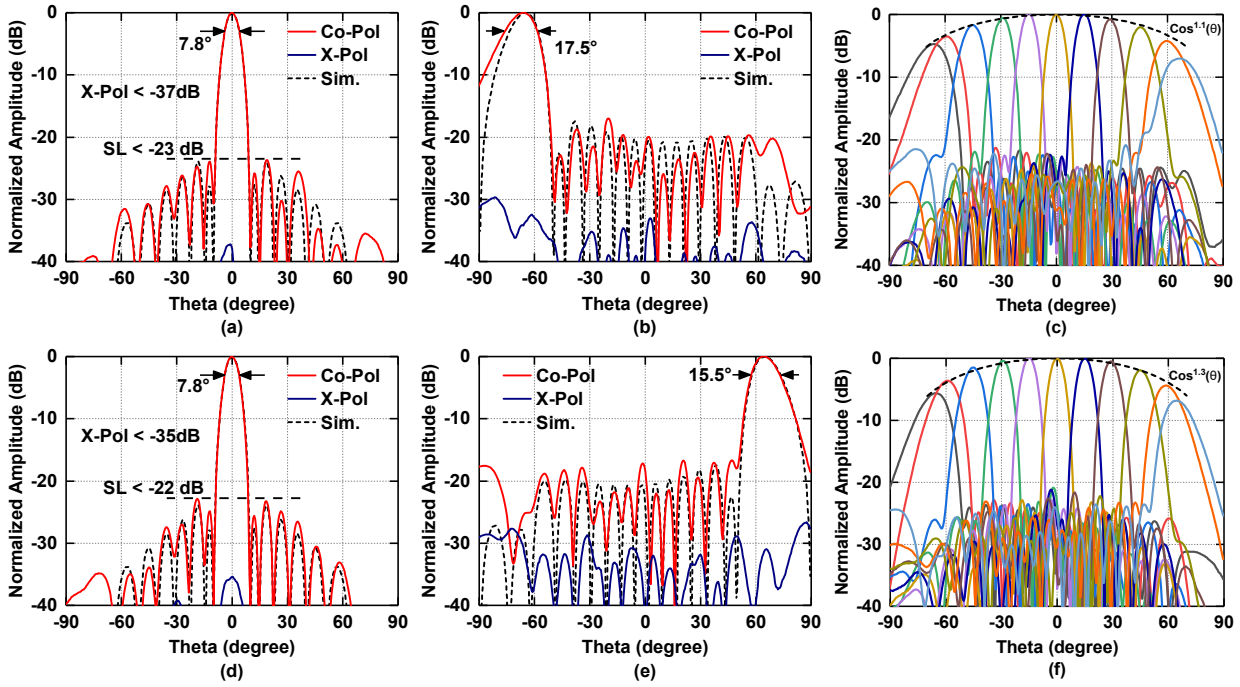

Figure 2.21: Measured E-Plane patterns (V-Pol) with at (a) 0°, (b) -70°, and (c) -70° to +70°. Measured H-Plane patterns (H-Pol) with 8-dB raised-cosine taper illuminations at (d) 0°, (e) 70°, and (f) -70° to +-70°. All patterns are at 11.75 GHz.

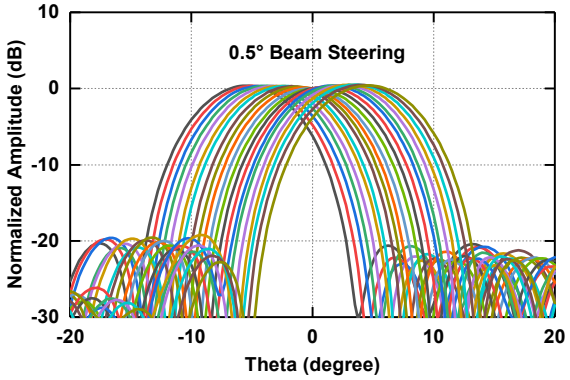

Figure 2.22: Measured co-polarized patterns with fine beam-steering resolution for E-plane with 8-dB cosine taper illumination. All patterns are at 11.75 GHz and from -5° to 5° with 0.5° step

sidelobe levels of < -17 dB even at ±70° scan angles and with cross-polarization levels < -27 dB. Figure 2.21 (c, f) presents the measured patterns from -70° to +70° for the E and H-planes. The patterns agree well with the roll-off given by active element patterns (see Figure 2.18).

As demonstrated in [22], the beam can be scanned in a finer resolution than the minimum phase step of 5.6° if the discretized phase gradient is applied across several elements. Using this

technique, the beam is steered in 0.5° steps (beamwidth/14) from -5° to 5° for the E-plane without degrading the sidelobe levels for the tapered illumination (Figure 2.22).

The AF at any observation angle (θ, ϕ) when the phased array is scanned to angle (θ_s, ϕ_s), is given by:

$$AF(\theta, \phi) = \sum_{n=1}^{N_x} \sum_{m=1}^{N_y} I_{n,m}\, e^{jk \sin\theta\, (nd_x \cos\phi + md_y \sin\phi)} \tag{2.13}$$

where $I_{n,m} = e^{-j\phi_{n,m}}$ is the excitation imposed on the nth, mth element, n is the antenna column number (n=0-15), m is the antenna row number (m=0-15), and $\phi_{n,m}$are the phases applied according to:

$$\phi_{n,m} = k \sin(\theta_s)\ (nd_x \cos(\phi_s) + md_y \sin(\phi_s)) \tag{2.14}$$

where (θ_s, ϕ_s) is the scan angle. Figure 2.23 presents the measured V-pol patterns when scanned in the 45°plane using (12, 13) with uniform illumination. At boresight, the 3-dB beamwidth is 6.6°, and the sidelobes (SL) levels are <-26 dB. The measured 3-dB beamwidth increases to 12.8°, and the sidelobe level remains < -22 dB at the 60° scan angle. The low SLL is expected in this plane due to the square grid, which increases the sidelobe levels in the X and Y-planes and reduces them in the diagonal planes [23].

2.7.3 Rotated-Linear Polarization

The two orthogonal polarizations (V-and H-pol) can also be excited in phase and with the appropriate weights to form any desired rotated-linear polarization. This is necessary for polarization tracking between a mobile unit on the ground and a linearly polarized transmitter on the satellite. The Ku-band phased-array was set to receive three linearly rotated polarizations at 30°, 45°, and 60° with normalized weights (or gain settings) 0.5:1, 1:1, and 1:0.56 for the V and H

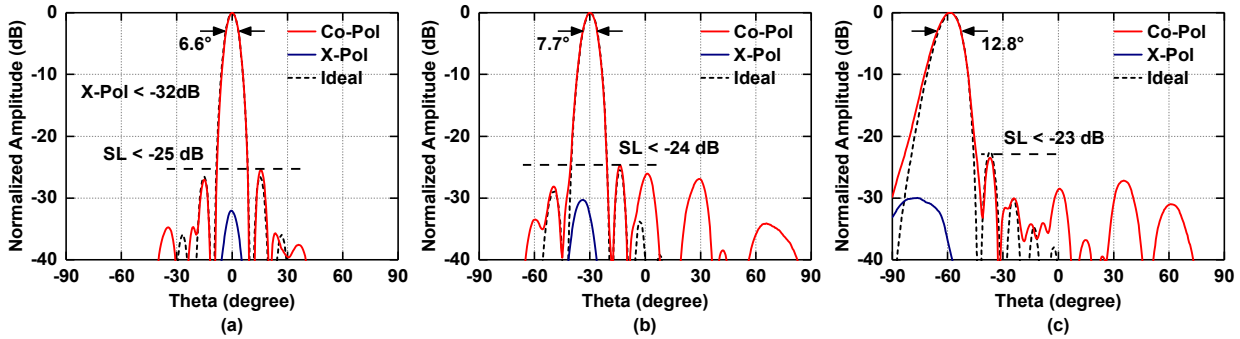

Figure 2.23: Measured vertical polarization patterns in the 45° plane with uniform illumination at (a) 0°, (b) -30°, and (c) -60°at 11.75 GHz.

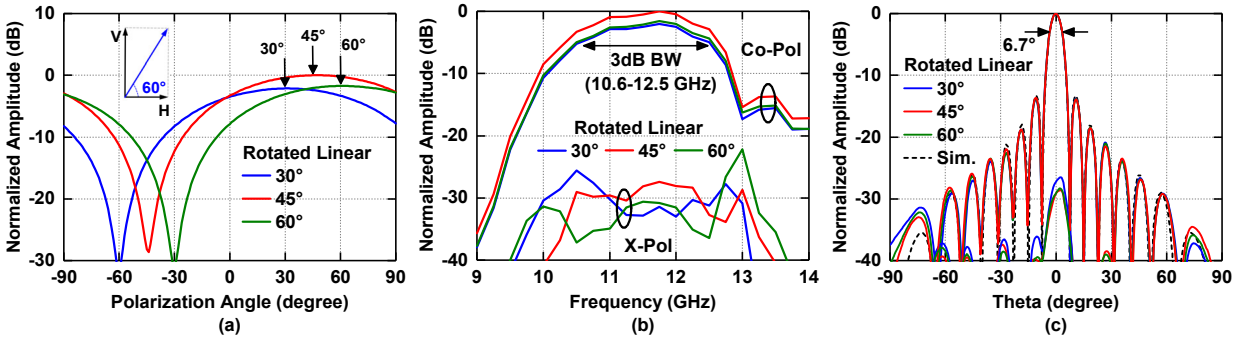

Figure 2.24: Measured (a) normalized amplitude versus rotation angle of the horn antenna, co-and cross-polarization (b) frequency responses, (c) patterns (elevation plane). Rotated-linear polarizations at 30°, 45°, and 60° at 11.75 GHz are displayed at boresight.

channels, respectively, on every antenna in the 256-element array. The frequency response of the three rotated-linear polarizations was first measured versus the polarization angle of the transmit horn antenna [Figure 2.24(a)]. Note that while it is hard to determine the peak due to its broad response, the null at 90° polarization off-set is visible and is -30 dB. The frequency response of the linearly-rotated polarizations has the same half-power bandwidth of 10.6 – 12.5 GHz, and high cross-polarization rejection of > 28 dB is achieved [Figure 2.24 (b)]. The measured patterns at boresight for the three different rotated-linear polarizations are shown in Figure 2.24 (c).

2.7.4 Circular Polarization

The dual-polarized Ku-band phased-array can also be configured to receive circular polarization. Both V-and H-pol channels are turned ON with a phase offset of ±90° for left-hand

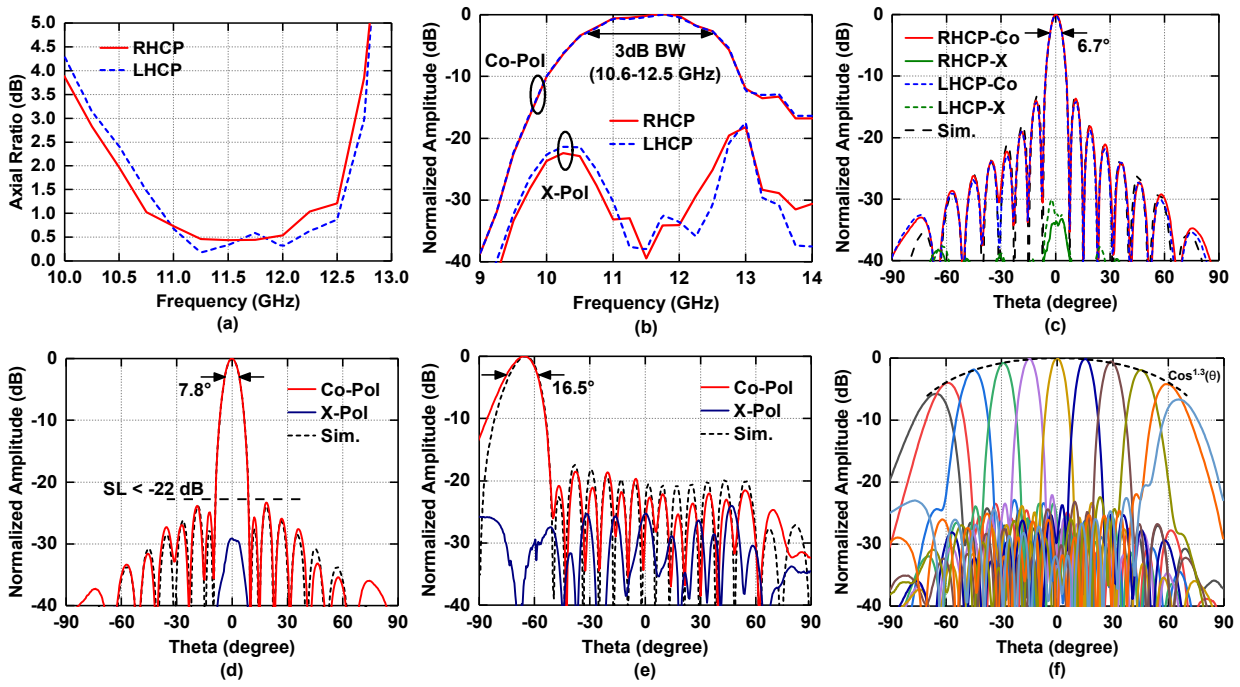

Figure 2.25: Measured LHCP and RHCP (a) axial ratio (AR) versus frequency (b) frequency response, and (c) patterns (elevation plane) at 11.75 GHz. Measured RHCP patterns at 11.75 GHz with 8-dB taper at (d) 0°, (e) -70°, (f) scanned patterns to ±70 in the elevation plane.

or right-hand circular polarization (LHCP, RHCP). At 11.75 GHz, the measured axial-ratio (AR, defined as the ratio of the major to minor axes of a polarization ellipse [24]) is 0.5 dB in the LHCP and RHCP modes [Figure 2.25(a)]. This translates to a cross-polarization level of -30.8 dB using:

$$XPD = 20 \log_{10}\left(\frac{r+1}{r-1}\right) \tag{2.15}$$

where $r = 10^{\frac{AR}{20}}$ is the magnitude of the axial ratio, and AR is the axial ratio in decibel. The 1-dB AR bandwidths are 10.8 – 12.2 GHz for the RHCP, and 10.9 – 12.5 GHz for the LHCP, using a single-point calibration at 11.75 GHz (AR=1 dB is a cross-pol. level of -24.8 dB). The frequency response of both circular polarization modes in Figure 2.25(b) agree with the linearly-polarized frequency response with a 3-dB bandwidth of 10.6 – 12.5 GHz. The measured LHCP and RHCP patterns at broadside are shown in Figure 2.25(c) and again with a 3-dB beamwidth of 6.7°. Also, the 8-dB raised-cosine taper illumination is applied across both V-and H-pol elements. The

measured tapered patterns show a 3-dB beamwidth of 7.8° at broadside, together with a -22 dB sidelobes level. The RHCP tapered patterns to ±70° were measured in the elevation plane and fit the $\cos^{1.3}(\theta)$ roll-off with sidelobe levels of < -17 dB even at ±70° scan angles and with cross-polarization levels < -25 dB (Figure 2.25).

2.7.5 Monopulse, Cosecant-Square, and Flat-Topped

A monopulse or difference pattern is used in tracking applications to identify the satellite location accurately. This is achieved by first setting the phases on the elements for a certain scan angle, and then adding a 180° phase shift to half of the array, thereby resulting in a null at the scan angle. In this work, it is also used to demonstrate the quality of the phased-array calibration. The measured monopulse patterns for uniform illumination are presented in Figure 2.26. At -70°, 0°, and 30°, the nulls depths are -37, -34, and -40 dB, respectively, without any additional amplitude calibration.

The Ku-band phased array can also be excited with the required current distribution to produce cosecant-square patterns with -22 dB sidelobe levels, as shown in Figure 2.27(a) [25]. These patterns are used in a high-altitude platform to result in constant energy on the ground versus range [26]. The measured patterns at 0° and -45° scan angle agreed with simulations and the measured cross-pol. levels are < -28 dB [Figure 2.27 (b, c)]. The scanned patterns are shown since they are used when the airplane banks at a steep angle, but the energy on the ground needs to remain constant.

Similarly, flat-topped patterns can also be synthesized using appropriate excitations [Figure 2.28(a)], and with -20 dB sidelobe levels. Such a pattern is required if the flying platform at low altitude and needs to result in a near-uniform illumination on the ground underneath the plane (these are sometimes called “flood beams”). The measured flat-topped patterns at 0° and

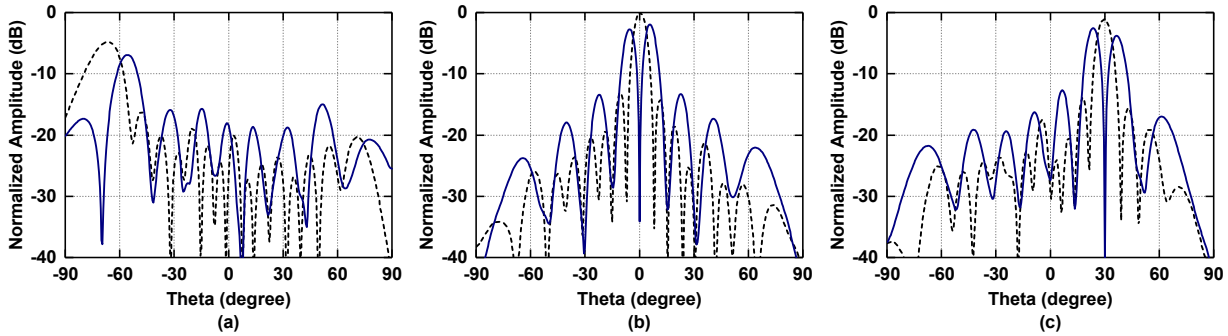

Figure 2.26: Measured monopulse patterns (solid) at (a) -70°, (b) 0°, and (c) 30° in the E-plane. All patterns are normalized to the 11.75 GHz pattern with uniform illumination at boresight. (Vertical polarization is displayed).

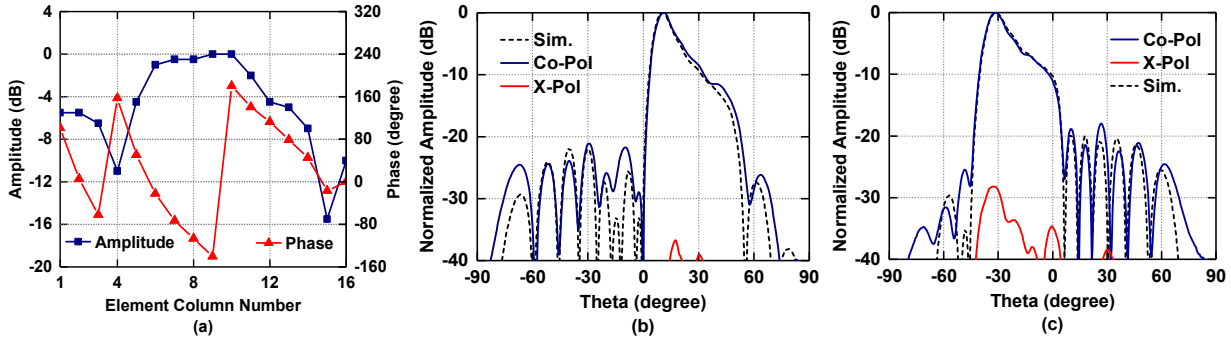

Figure 2.27: (a) Applied current distribution (amplitudes and phases). Measured patterns at (b) 0°, (c) -45° of cosecant-square patterns. All patterns are in the E-plane at 11.75 GHz for vertical polarization.

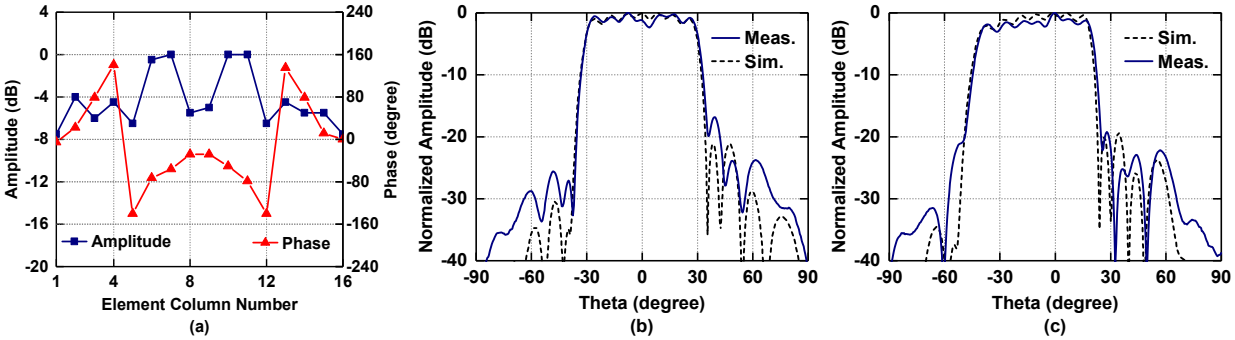

Figure 2.28: (a) Applied current distribution (amplitudes and phases). Measured patterns at (b) 0°, (c) -10° of flat-topped patterns. All patterns are in the E-plane at 11.75 GHz for vertical polarization.

at -10° scan angles agreed well with simulations [Figure 2.28 (d, c)]. All measurements are done without any amplitude calibration.

2.7.6 -30 dB Taylor Distribution

All previous measurements were achieved with only phased calibration and without amplitude calibration. Figure 2.29 presents the measured E-plane patterns at 11.75 GHz with 35-

dB Taylor taper [23]. This taper results in very low sidelobes. Due to the 1.5 dB RMS amplitude error on the aperture, the first sidelobe levels for a broadside pattern is -27 dB. Also, scan performance shows that the sidelobes are around -25 to -27 dB. In this case, the RMS amplitude error effects are seen, and further calibration is needed for lower sidelobe levels. Still, such an array can deliver < -25 dB SLL without any amplitude calibration.

2.7.7 Array to Array Comparison

A second phased array (PCB_2) was fabricated for comparison. This array employs the same stack-up and same chips as in PCB_1 discussed above. The second array was not calibrated individually, but rather, the same phase-calibration coefficients obtained from PCB_1 were applied to PCB_2. Also, the same cross-polarization cancellation coefficients (see Section 2.9) from PCB_1 were also applied to PCB_2. This was done to demonstrate the repeatability of the multi-layer PCB fabrication process and the silicon chips, and the robustness of the scalable 256-element phased-array.

The measured co-and cross-polarization frequency responses of both arrays are shown in Figure 2.30(a), with a near-identical response. Also, the measured scanned co- and cross-pol patterns at -30° of PCB_1 and PCB_2 arrays agree with each other with a high cross-pol rejection >35 dB [Figure 2.30 (b)]. The V-Pol. patterns in the E-plane from -70° to 70° are measured for the two arrays and again with excellent agreement [Figure 2.30 (c)]. The reason is two-fold: first, the phase errors are mostly determined by the transmission-line connections (between the chip and the antenna feeds) and not by the chips, so they translate well from PCB1 to PCB2. Second, the errors are relatively smalls, so small errors (from PCB1 to PCB2) have a negligible effect. This experiment shows that one-array can be calibrated, and then, the same calibration coefficients can

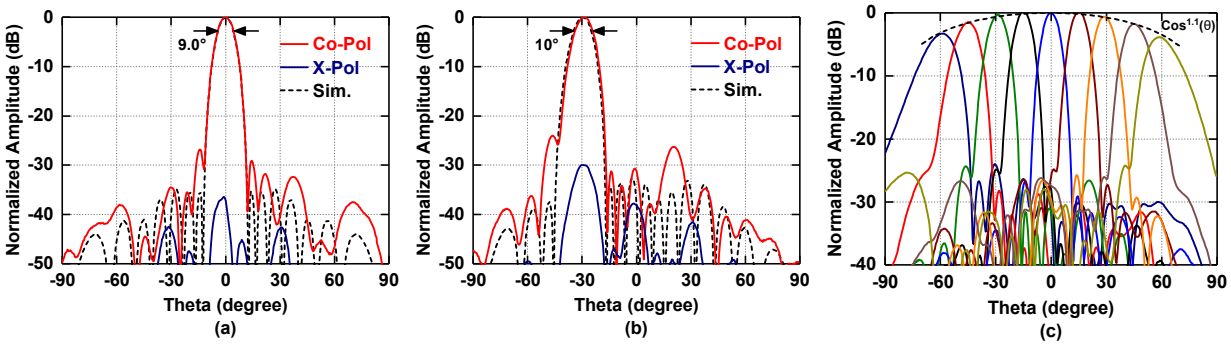

Figure 2.29: Measured E-Plane patterns at 11.75 GHz with 35-dB Taylor taper at (a) 0°, (b) -30°, and (c) ±60°. (Vertical polarization is displayed).

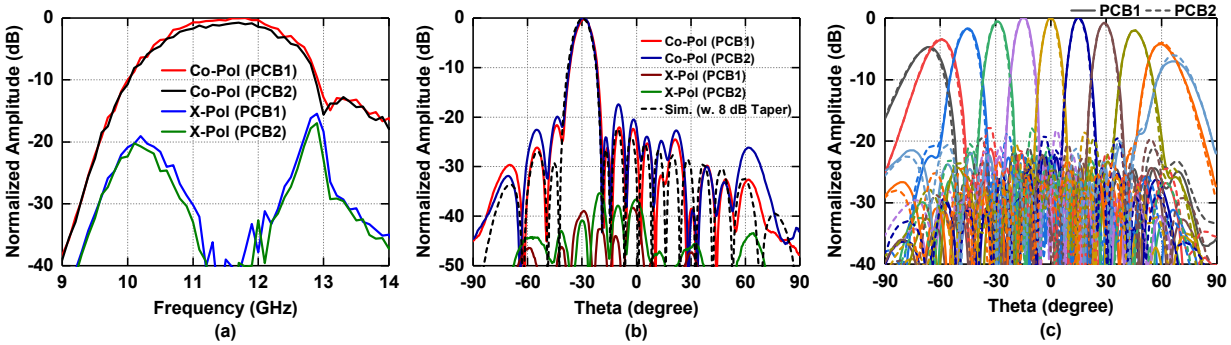

Figure 2.30: Measured PCB_1 vs. PCB_2 co-and cross-polarization (a) frequency responses, (b) patterns at 30°, (c) scanned patterns to ±70. E-Plane patterns (V-Pol) with 8-dB Cosine taper illuminations are shown. All patterns are at 11.75 GHz after phase calibration at 11.75 GHz.

be applied to different arrays, thereby significantly reducing the calibration time and cost of large-volume commercial arrays.

2.8 Beam Squint in Large Arrays

Figure 2.31(a) presents the measured patterns at 11.5 GHz, 11.75 GHz, and 12 GHz, with a phase setting at 11.75 GHz. This measurement is essential for wideband waveforms, such as a 300-500 MHz, used in LEO and MEO constellations. Any phased-array without true-time-delay correction at the element or sub-array levels suffers from beam squint, as the peak radiation angle changes with frequency. The squint angle θ_f at f due to the array factor is given by:

$$\sin(\theta_f) = \frac{f_0}{f}\sin(\theta_s) \tag{2.16}$$

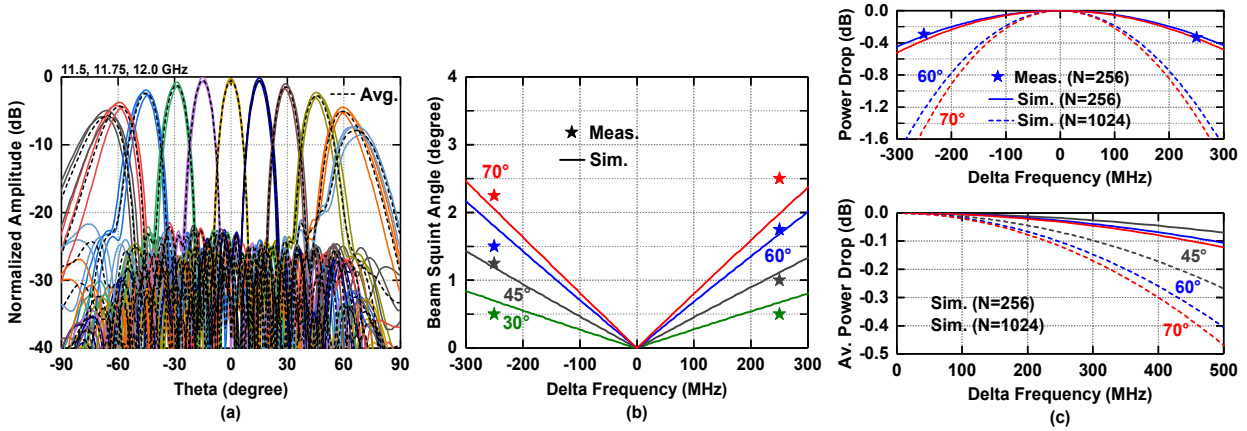

Figure 2.31: Measured beam squint for E-Plane (V-Pol) (a) patterns with 8-dB taper at 11.5, 11.75, 12.0 GHz. (b) Simulated and measured beam squint versus change in frequency. (c) Power drop versus change in frequency and average power drop versus instantaneous bandwidth.

where θ_s is the phased-array scan angle at f_0. Note that the actual pattern peak is not given by (2.16) for wide scan angles due to the element pattern, and a better equation to use is (2.9), which considers the AF and the element pattern. Measurements of the beam-squint angle agree with simulations done using (2.9), as shown in Figure 2.31 (b).

One of the essential questions in analog beamforming is when to include a true-time-delay (TTD) correction unit, and if it should be placed after 256-elements or 1024-elements. Figure 2.31(c)-Top presents the simulated and measured power drop at 60°-70° scan angles and is 0.35-1.6 dB for the 256-element and 1024-element array, respectively. The power drop versus frequency can be easily equalized in the modem, and thus has little effect on the waveform quality. A more critical simulation is the average power drop in the entire 500 MHz waveforms, shown in Figure 2.31(c)-bottom. For a 500 MHz waveform, a 256-element array results in a 0.05-0.1 dB drop in the total received power (or effective gain for the G/T calculation) at 45°-70° scan angle, while the 1024-element array results in a 0.25-0.5 dB drop. For 250 MHz waveforms, the average power drop is < 0.1 dB for both arrays at all scan angles. Since most LEO constellations require a scan-angle of ~45°-50°, TTD units should not be used for the 1000-element array, thereby

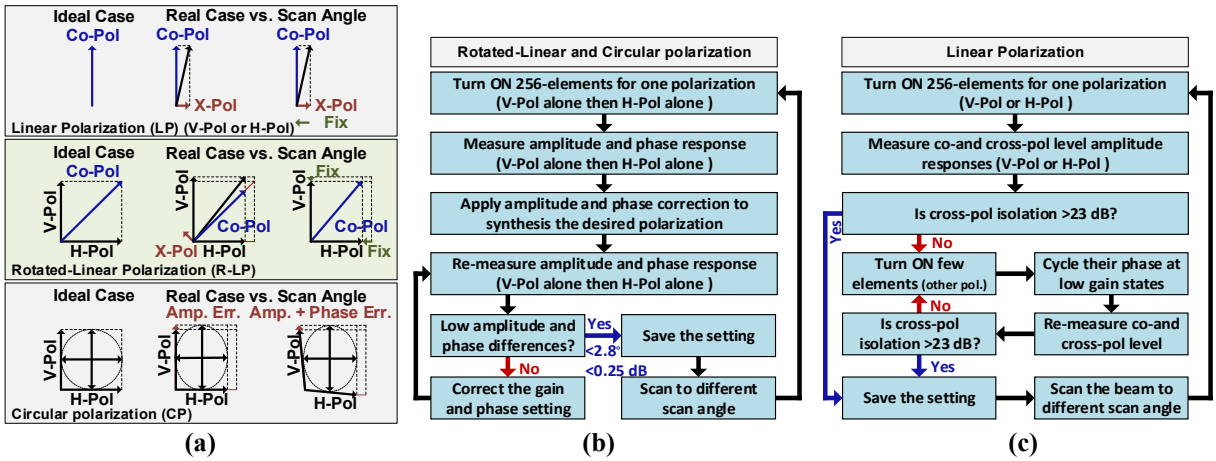

Figure 2.32: Cross-polarization (a) concept in linear, rotated-linear, and circular polarization. Cross-polarization optimization steps for (b) rotated-linear, and circular, and (c) linear polarizations.

significantly reducing the array cost.

2.9 Cross-Polarization Optimization

The dual-polarized array with 6-bit phase control and <0.5 dB gain-steps on every channel allows for near-ideal polarization correction. Thus, resulting in very low cross-pol components overall scan angles and for any polarization choice (linear, rotated linear, circular).

The cross-polarization is due to the microstrip antenna itself, the radome depolarization versus scan angle (if any), and imbalance in the electronic gain for the V and-H channels (on every antenna). The calibration technique is straightforward: After setting the amplitude and phase for a scan angle (θ_s, ϕ_s), the V-pol. and H-pol. far-field response (S_{21}) is measured individually, and any difference in amplitude and phase is corrected using the phase shifter and gain control on every V and H-channel of the 256-element array. Then, the desired amplitude and phase weighting between the V and H channels is implemented to synthesize the required polarization (rotated-linear or circular). For the case of circular polarization and due to the ±0.8 dB gain response variation in the phase shifter, which can degrade the axial ratio, the V- and H-pol response is

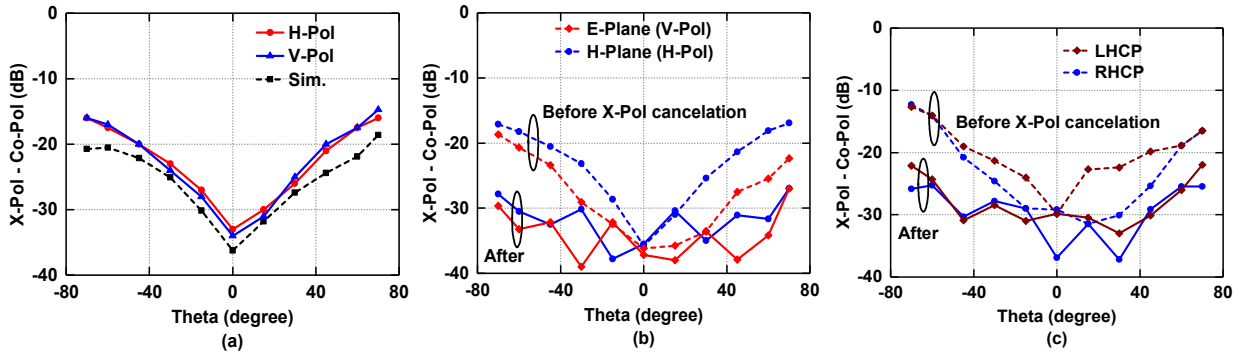

Figure 2.33: Measured cross-polarization rejection for (a) H-Plane scan with uniform illumination without cross-polarization optimization, (b) E-Plane and H-Plane with 8-dB cosine taper illumination before and after cross-polarization optimization using 4x16 elements, and (c) LHCP and RHCP before and after cross-polarization optimization.

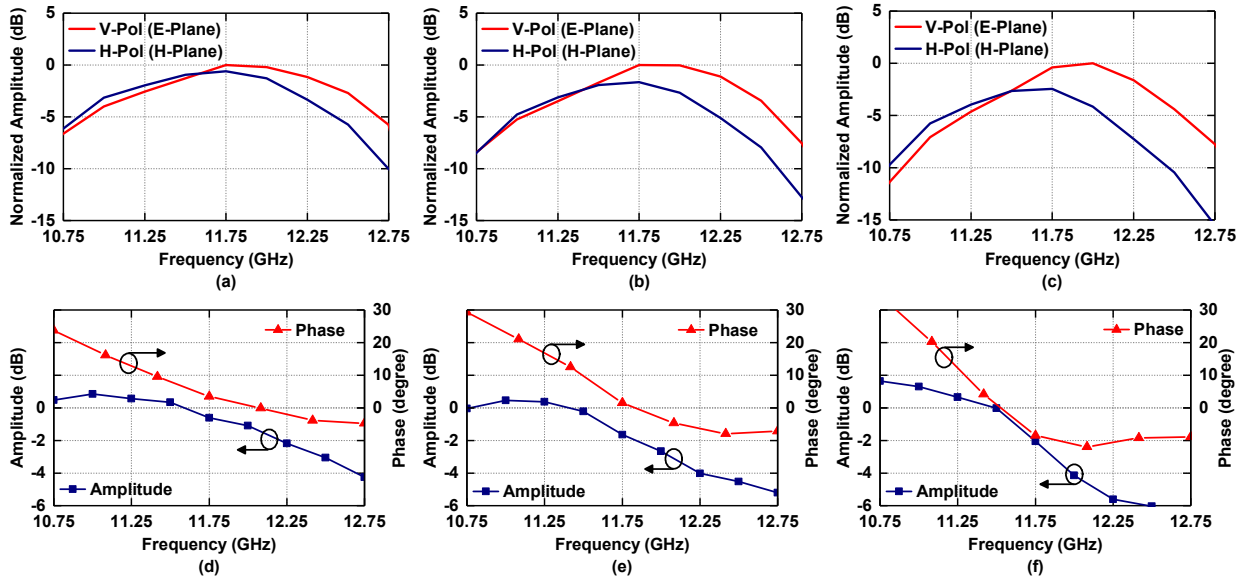

Figure 2.34: Measured V-Pol (E-Plane) and H-Pol (H-Plane) frequency response at (a) 45°, (b) 60°, and (c) 70° and measured amplitude and phase differences at (d) 45°, (e) 60°, and (f) 70°. All before corrections are done at 11.75 GHz.

measured again and corrected if needed using the VGA to result in very low cross-polarization levels. Note that this step is not required for rotated linear polarization as both channels have the same phase setting, and the VGA has only ±2.5° phase change versus gain setting.

A special case occurs when the array is linearly polarized (for example, V-pol. only). In this case, 2x16 or 4x16 H-pol. channels located at the center of the array are used for polarization correction, which saves DC power and still results in a very low cross-polarization level overall

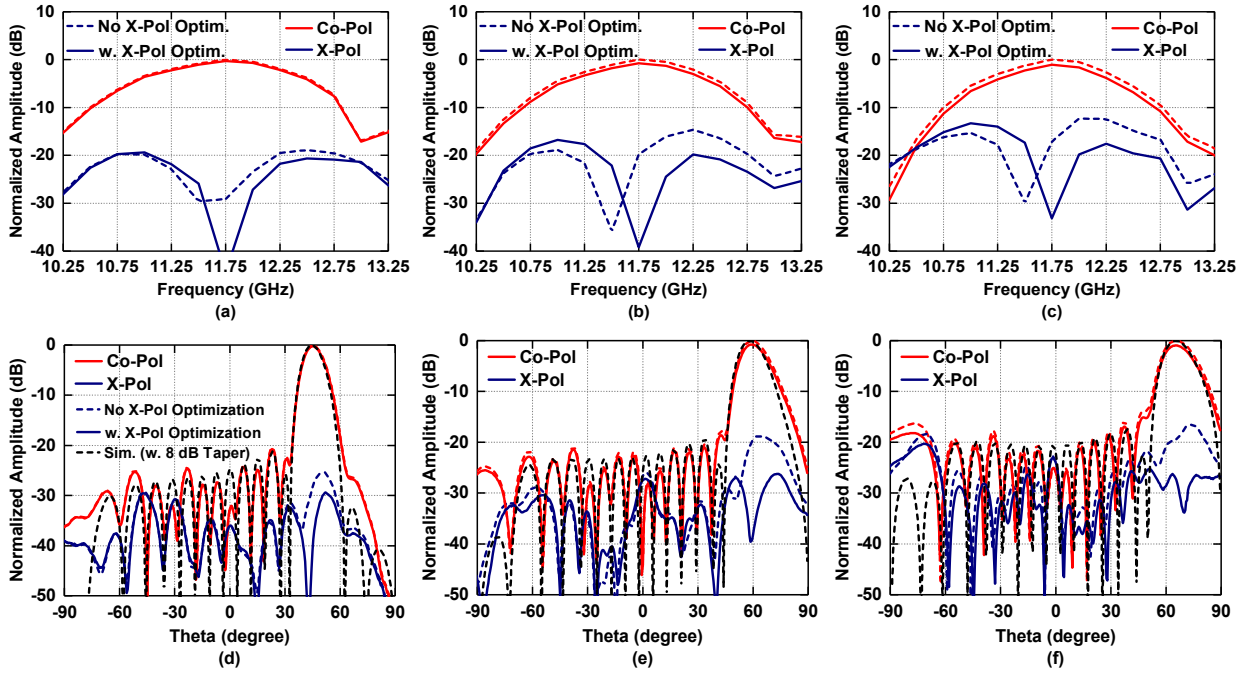

Figure 2.35: Measured RHCP frequency response at (a) 45°, (b) 60°, and (c) 70° before and after cross-polarization optimization. Measured RHCP patterns (elevation plane) at 11.75 GHz with 8-dB Cosine taper illuminations before and after cross-polarization optimization at (a) 45°, (b) 60°, and (c) 70°. Corrections are done at 11.75 GHz.

scan angle. The "correction sub-array" still must scan to the same angle as the primary array for best performance.

The calibration technique can be done at all scan angles, but we have found that the 256-element array naturally results in very low cross-polarization at 0° to 15° (<-25 dB), and no correction is effectively needed. Therefore, polarization correction is done every 15°, starting from 15° to 70°. Also, an instantaneous bandwidth of 500-350 MHz is achieved (after correction) for a cross-polarization level of <-20 dB at 60°-70° for circular polarization.

Fig. 2.32-2.35 details all the information discussed above. Figure 2.32 shows the cross-polarization optimization steps for rotated-linear, circular, and linear polarizations. Figure 2.33 presents the natural cross-polarization due to the microstrip antenna [Figure 2.33 (a)], achievable cross-pol. levels for linear polarization [Figure 2.33(b)] and circular polarization [Figure 2.33(c)]. Figure 2.34 presents the measured V and H-pol. responses at different scan angles, and the gain

and phase correction factors required. Figure 2.35 presents the co-pol. and cross-pol. frequency response before after cross-pol. correction at different scan angles, and finally, the measured pattern before and after cross-pol correction are shown in Figure 2.35. It is seen that this technique works well and results in a wide bandwidth for cross-polarization correction.

2.10 Satellite Reception

The array was taken outside and pointed to the southern sky using an App (Satbeams Finder), as shown in Figure 2.36(a, b, c). The output is connected to a spectrum analyzer with a resolution bandwidth of 5.6 kHz with a noise floor of -143 dBm/Hz, and a line amplifier is used to boost the signal. Several satellite transponders could be easily located with high SNR even with the low G/T. One transponder was clearly H-polarized (with 10 MHz bandwidth), and the other two were clearly V-polarized (with 30-40 MHz bandwidth), as shown in Figure 2.36 (d, e). The array was also mechanically pointed away from the satellite up to 70°, and the beam electronically steered back the satellite, and a signal reduction of 4.7 dB is seen due to the scan loss. Finally, all three transponders were received again when the array is set for circular polarization, and these are shown in Figure 2.36 (f). The measured noise floor of -135 dBm/Hz is due to the array effective NF (6.5 dB), electronic gain (0.7 dB), and the line amplifier at the common port (G=31.2 dB, NF=2.7 dB), resulting in a total simulated system gain and noise figure of (G=31.9 dB, NF=7.2 dB) and as a result a simulated output noise of -134.9 dBm/Hz.

A summary of the phased-array performance is shown in Table 2.2, which also compares this work with other large-scale state-of-the-art receive Ku-band phased arrays. This work demonstrates, without the need for any mechanical parts, the widest scan range of 140° with lowest roll-off at ±70° in both azimuth and elevation planes at the lowest power consumption of 67 mW per element. Moreover, this work showed low sidelobes <-22 at broadside high polarization purity.

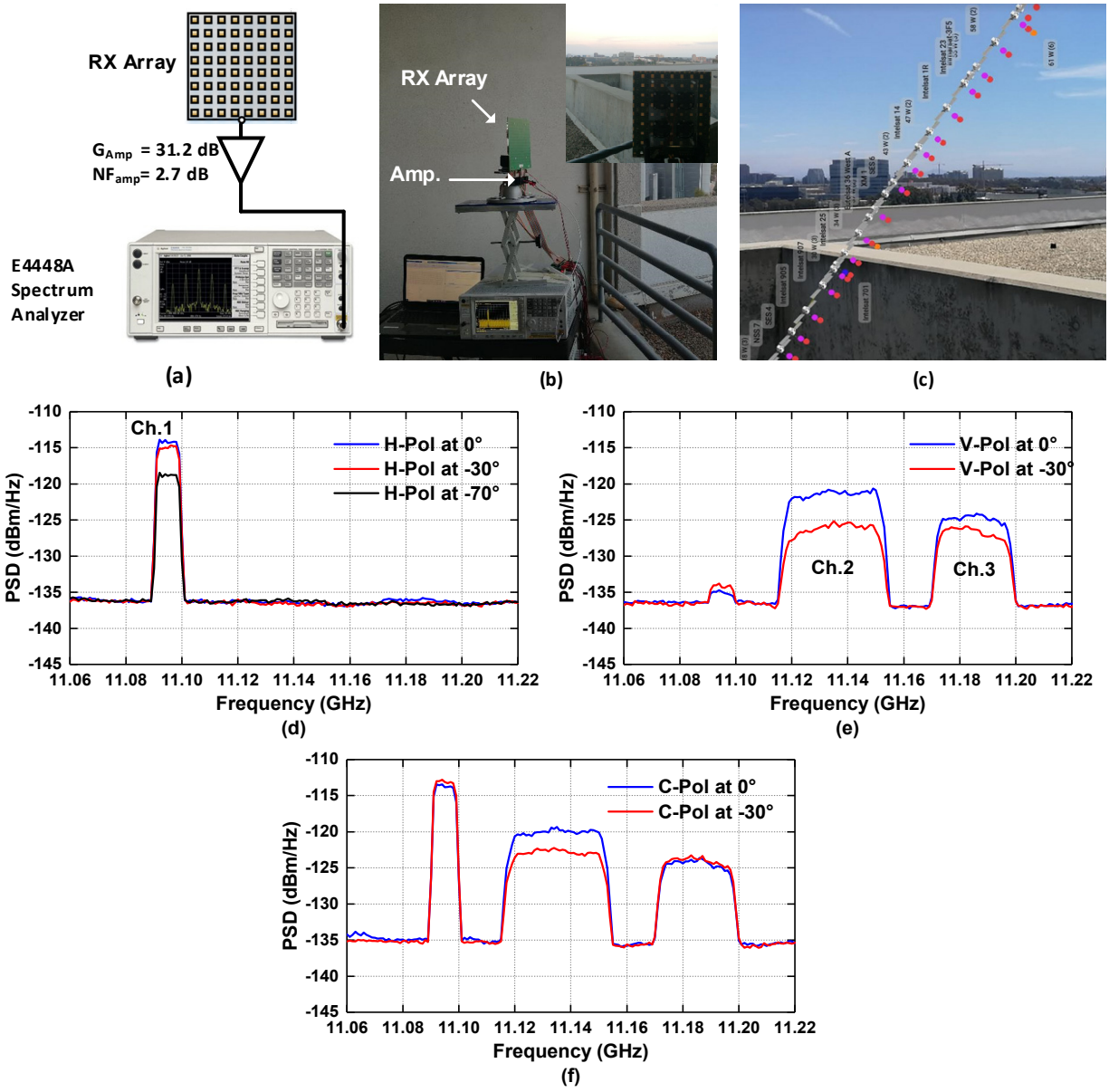

Figure 2.36: Measurement setup to test the possibility of receiving any satellite channels (a) block diagram, and (b) photo. (c) List of satellites in the array beam direction using an App "Satbeams Finder". Measured received power spectrum density for (d) horizontal, (e) vertical, and (f) circular polarization for three channels at different scan angles.

2.11 Conclusion

This chapter presented an ultra-low-profile dual-polarized 256-element Ku-band phased-array receive tile for SATCOM on-the-move applications, capable of receiving linear, rotated, and circular (or elliptic) polarizations. The design has a wide 3-dB instantaneous bandwidth of 10.6 – 12.5 GHz and ±70° scanning in all planes and with low scan loss. Besides, a beam-steering

resolution of 0.5° (beamwidth/14) was demonstrated. The work provided, for the first time, an extensive set of measurements to demonstrate that building low-cost planar phased-arrays is possible and that one can synthesize any pattern (sum, tapered, monopulse, cosecant, or flat-top) with accuracy and with minimal calibration. Also, a very low cross-polarization level and with wide bandwidth can be achieved at any scan angle. The patterns and results have been near-ideal and provide a high degree of confidence in this low-cost design approach. This was made possible using multi-channel silicon beamformer chips and multi-layer PCBs, all commercially available and at low cost. The planar phased-arrays are not only useful for SATCOM applications, but similar arrays can be built for point-to-point communications and low-power radars.

2.12 Acknowledgment

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Table 2.2: Comparison with state-of-the-art receive Ku-band phased arrays

Parameter		**This Work**	[27] 2017	[28] 2013	[7] 2010
Frequency (GHz)		**10.6 – 12.5**	10.7 – 12.7	11.725	10.7 – 12.75
Number of Elements		**256 (16x16)**	256 (16x16)	156	96 (8x12)
Polarization		**Dual** **Linear, Rotated, LHCP, RHCP**	Dual Linear	Dual Linear, Rotated	
Electronic Beam-Steering Range	Elevation	**140° (-70° to +70°)**	0° (Fixed at 23°)	140° (-70° to +70°)	70° (20° to 90°)
	Azimuth	**140° (-70° to +70°)**	40° (-20° to +20°)	140° (-70° to +70°)	0°
Sidelobes Level at Boresight (dB)		**< -13 (w. uniform illumination)** **<-22 (w. 8-dB taper illumination)**	< -10	< -15	< -13
Cross-Pol. Isolation (dB)		**> 33 (at 0°)** **> 23 (over scan range)**	> 20 (at 23° in Elev.) > 18 (at 0° in Az.)	> 20 (average) > 17 (worst case)	>15
Size (cm^2)		**22.2 x 19.7**	25 x 37	π x $(11)^2$	16x16
Directivity (dB) at 11.75 GHz		**28.7***	32.5*	28.6*	26.9*
Power Consumption		**53 mW per channel** **27.2 W (2*256*53mW)**	-	208 mW per channel 65 W (2*156*208mW)	-

* Calculated using $D=4\pi/\lambda^2 A_{phys}$ and $A_{phys}=radiating\ panel\ size$

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Scanning and 34.5 dBW EIRP," *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 1064-1067.

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Chapter 3

A 256-Element Ku-band Polarization Agile SATCOM Transmit Phased-Array with Wide-Scan Angles, Low Cross-Polarization, Deep Nulls, and 36.5 dBW EIRP Per Polarization

3.1 Introduction

This chapter is the second of two chapters on the design, analysis, and measurements of planar phased-arrays for low-cost Ku-band SATCOM on-the-move (SOTM) terminals (Figure 3.1). The chapter is based on [1] presented a dual-polarized 256-element receive Ku-band phased-array at 10.6 – 12.5 GHz capable of receiving linear, rotated-linear, and circular polarizations, discussed the beam squint in large arrays, cross-polarization mitigation over wide scan angles, and the measurement of satellite signals.

In this chapter, we expand on [2] and present detailed design and measurements of a 256-element Ku-band dual-polarized scalable transmit phased-array at 13.0 - 14.6 GHz. Section 3.2 discusses the phased-array design, including architecture and beamformer chips. Section 3.3 presents system analysis for the 256- and 1024-element transmit phased-arrays. The stacked

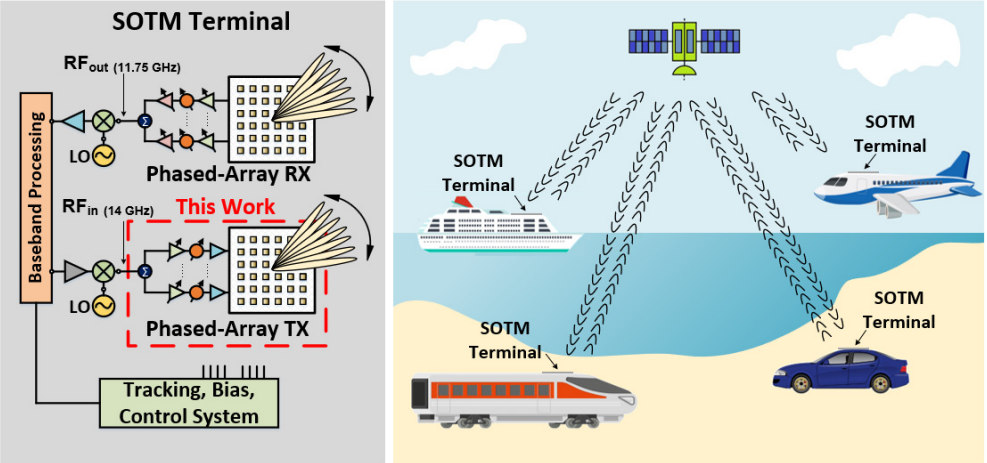


Figure 3.1: Low-cost Ku-band SATCOM on-the-move (SOTM) terminal based on planar phased-arrays.

microstrip transmit antenna is discussed in Section 3.4. Measurement of the Ku-band passive antenna and a 2x2-element transmit phased array are presented in Section 3.5. Section 3.6 presents the calibration and EIRP measurements, and section 3.7 presents extensive pattern measurements of the dual-polarized scalable 256-element phased-array. Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM) measurements for different waveforms are presented and discussed in Section 3.8. Section 3.9 is included to show the null tracking and null beamwidths capabilities of the 256-element phased-array, and section 3.9 concludes the chapter.

3.2 256-Element Transmit Phased-Array Design

3.2.1 Dual-Polarized Transmit Phased-Array Architecture

Figure 3.2 presents the RF beamforming transmit phased-array tile with 256 dual-polarized elements and 64 transmit (Tx) beamformer chips. The design consists of 64-unit cells, and each cell has one Tx chip and four dual-polarized antennas. The antenna elements are placed on one side of a multilayer printed circuit board (PCB), while the Tx chips are placed on the other side of the PCB. The design has a 7-stage of Wilkinson power divider to drive the two inputs of the Tx

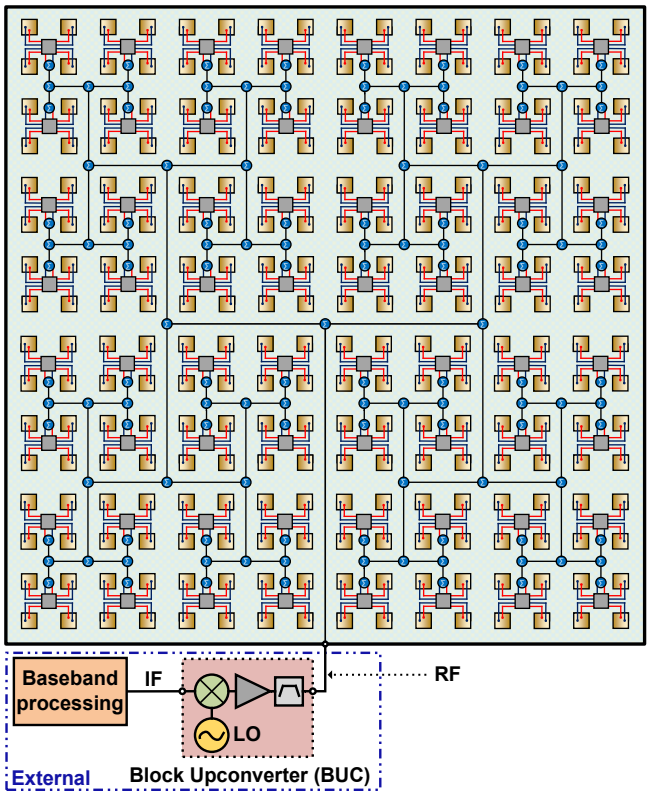


Figure 3.2: Architecture of the 256-element RF-beamforming transmit phased-array..

chip. The array is driven by an external block upconverter (BUC) to compensate for the division and ohmic losses of the Wilkinson network. The dual-polarized architecture allows the array to transmit linear, rotated-linear, and circular polarizations.

3.2.2 Silicon Beamformer Chip

The SiGe BiCMOS beamformer chip has eight channels, four for horizontal polarization (H-pol) and four for vertical polarization (V-pol). Each channel consists of a phase shifter, variable gain amplifier (VGA), and a power amplifier (PA), and each polarization has an independent Wilkinson divider network. This chip architecture allows for a dual-beam dual-polarization design but can also generate a single beam with polarization diversity if an external Wilkinson divider is used on the PCB. A VGA is used at the input of the chip on each polarization path for added gain (Figure 3.3).

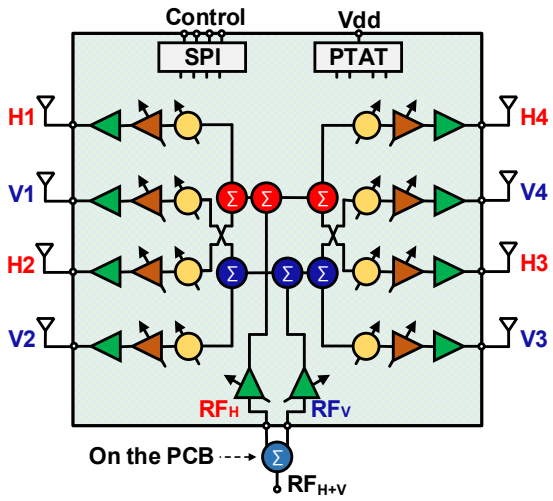


Figure 3.3: Dual-polarized transmit chip with eight beamforming channels.

Table 3.1 summarizes the chip performance. It has 16.2 dB gain control, a 6-bit phase shifter with RMS phase and amplitude errors of < 2.5° and < 0.4 dB, respectively, at 11-16 GHz. The PA OP1dB is 11-12 dBm at 12-16 GHz. The chip is controlled using a serial peripheral interface (SPI) and has a built-in PTAT current for biasing.

The measured chip electronic gain ($G_{Electronic,}$), defined as the power output per channel divided by the available power at the chip input port, is 35 dB at 14 GHz. This gain includes the VGA and the ohmic and division loss of the on-chip Wilkinson network. At an OP1dB of 12 dBm, the chip consumes 1.2 W from a 2.3 V supply, resulting in an overall PAE of 10.6% at 14 GHz. A chip-scale package (CSP) process is used for packaging with bumps spaced at a 0.4 mm pitch for both the RF ports (GSG) and the control ports (SPI, bias).

3.3 System Analysis

The Effective Isotropic Radiated Power (EIRP) per polarization is calculated using:

$$EIRP = P_T G_T = P_{EL} + G_{ANT} + 10 \log_{10}(N) \quad (3.1)$$

Table 3.1: Dual-polarized transmit SiGe beamformer chip

Parameter	Unit	Value
Frequency	GHz	12 – 16
Polarization	-	Dual (V-Pol and H-Pol)
Elements per chip	-	8
Output Power (OP1dB)	dBm	12
Input Power (IP1dB)	dBm	-22
Gain	dB	35
Phase shifter	bits	6
Phase step	degree	5.6
Gain control	dB	16.2
Gain control step	dB	0.25
Power dissipation/element	mW	150 at P1dB
Voltage Supply	V	2.3

where P_T is the transmitted power, G_T is the transmitted gain, N is the number of antenna elements, P_{EL} is element output power, and $G_{ANT} = 10\ \log_{10}(N) + G_{EL}$ is the array antenna gain, with $G_{EL} = D_{EL} - L_{ANT}$ is the antenna element gain. L_{ANT} is approximately 1 dB and represents the antenna and feed line loss, referenced to the chip output port. The antenna gain can also be calculated using:

$$G_{ANT} = 10\ \log_{10}\left(\frac{4\,\pi\,Area}{\lambda^2}\right) - L_{ANT} \tag{3.2}$$

where $Area = N_x N_y d_x d_y$ and N_x and N_y are the number of antenna elements in the horizontal and vertical directions, d_x and d_y are the element spacing, and λ is the wavelength. For $N = 256$, $d_x = d_y = 0.5\,\lambda\ at$ 14 GHz, and $P_{EL} = 12$ dBm, the $EIRP$ is 64 dBm per polarization.

The transmit electronic gain of the entire array ($G_{Electronic,array}$), defined as power per element divided by the input RF power, can be obtained from Figure 3.4:

$$\begin{aligned} G_{electronic,array} &= G_{\text{electronic}} - L_{Division} - L_{Ohmic} \\ &= 35 - 21 - 13.5 \\ &= 0.5\ \text{dB} \end{aligned} \tag{3.3}$$

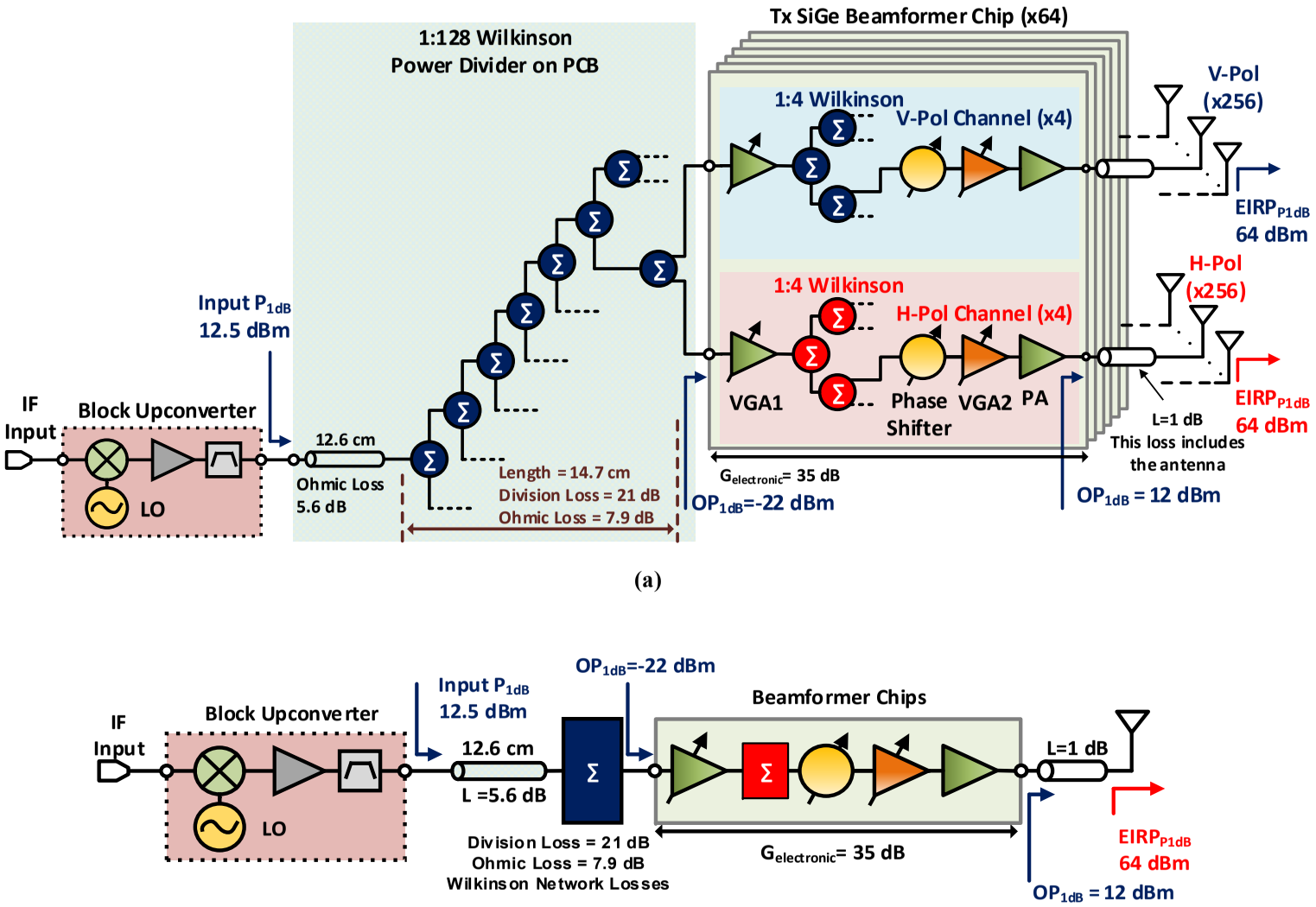


Figure 3.4: (a) The 256-element phased-array SATCOM transmitter tile system based on the dual-polarized (dual quad-core) transmit flip-chip with eight channels and (b) simplified block diagrams.

where $L_{Division}$ = 21 dB is division loss in the 7-stage Wilkinson divider network, and L_{Ohmic} = 7.9 + 5.6 = 13.5 dB is the ohmic losses of the transmission lines (0.44 dB/cm @ 14 GHz) and each Wilkinson stage (0.21 dB) (Figure 3.4). This means that the array requires an input power of 5 dBm to result in an output power of 5.5 dBm per element (assuming no compression). The required input P_{1dB} is 12.5 dBm and is calculated using:

$$IP_{1dB} = OP_{1dB} - (G_{\text{electronic}} - 1\text{dB}) + L_{Division} + L_{Ohmic} \tag{3.4}$$

where OP_{1dB} = 12 dBm and is element output power.

The 256-element array is scalable and cut on a $\lambda/2$ grid at three edges. Therefore, several tiles can be placed together to obtain a 1024-element array [Figure 3.5(a)]. The EIRP increases as N^2 and the beamwidth reduces by the linear dimension of the array it is given by:

$$BW_{Az} = 50.76^{\circ}\left(\frac{\lambda}{N_x d_x}\right) \tag{3.5}$$

for uniform illumination. Figure 3.5(b, c) present the EIRP and beamwidths versus the number of elements based on (3.1) and (3.5).

3.4 Dual-Polarized Stacked Patch Antenna

A square stacked patch-antenna is used with a dual-probe feed for the V and H polarization. The lower patch is implemented using a metal layer (M10) and is the fed patch, while the upper patch is implemented using the M12 layer, and it is the parasitic patch [3]. A probe feed via (Via 1-12) is used to connect M1 to M12 (Figure 3.6). ANSYS HFSS with a master/slave boundary is used to simulate the unit cell [4].

Figure 3.7 (a) presents the 2x2 unit cell design with a single-stub matching network between the antenna and the chip port. The simulated antenna impedance (S_{11}), referenced to the

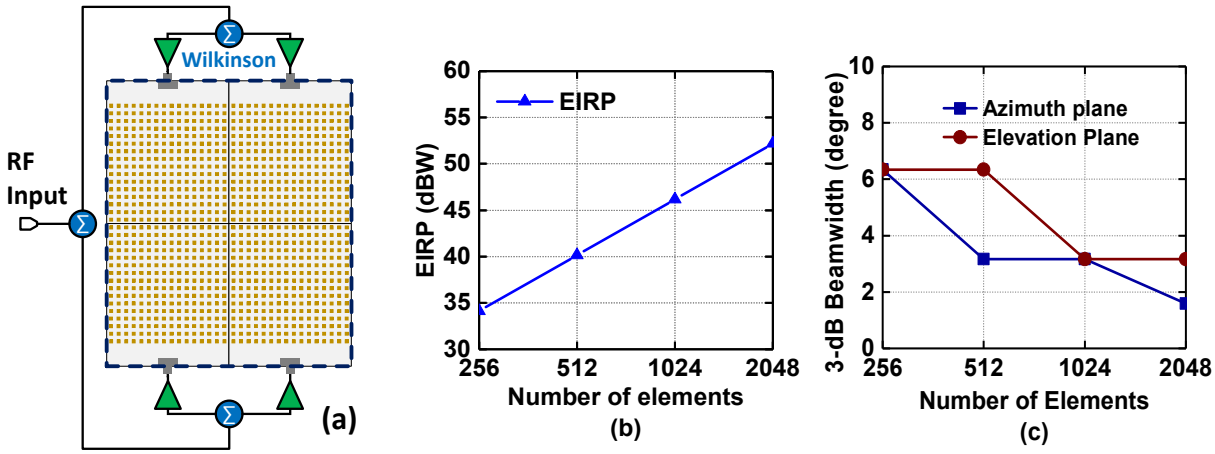


Figure 3.5: (a) Scalable phased-array tile design. Simulated (b) EIRP, and (b) 3-dB Beamwidth (in Az. and El. planes) versus number of elements, at normal incidence.

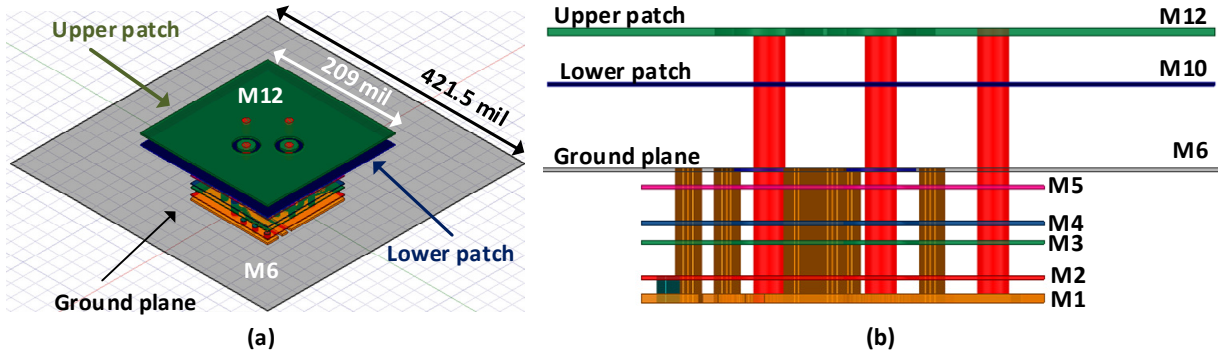


Figure 3.6: ANSYS HFSS simulated unit cell of the dual-polarized stacked microstrip patch antenna. (a) 3-D view, and (b) Side view.

chip port, are < -10 dB at 13 – 15.4 GHz [Figure 3.7(b)]. The antenna impedance changes versus scan angles in the E-and H-planes are also shown in Figure 3.7.

The simulated 3-dB bandwidth at broadside for the V-and H-polarization is 12.55 – 15.35 GHz, with a cross-polarization level <-40 dB at 14 – 14.5 GHz at broadside. The simulated ohmic losses at 14 GHz are 0.6 – 2.4 dB and 0.58 – 1.3 dB for 0°– 60° scan in the H-Plane and E-Plane, respectively (Figure 3.8). Most of the loss at the wide scan angle is due to mismatch loss. The cross-polarization level remains <-20 dB at 14 GHz for all scan angles.

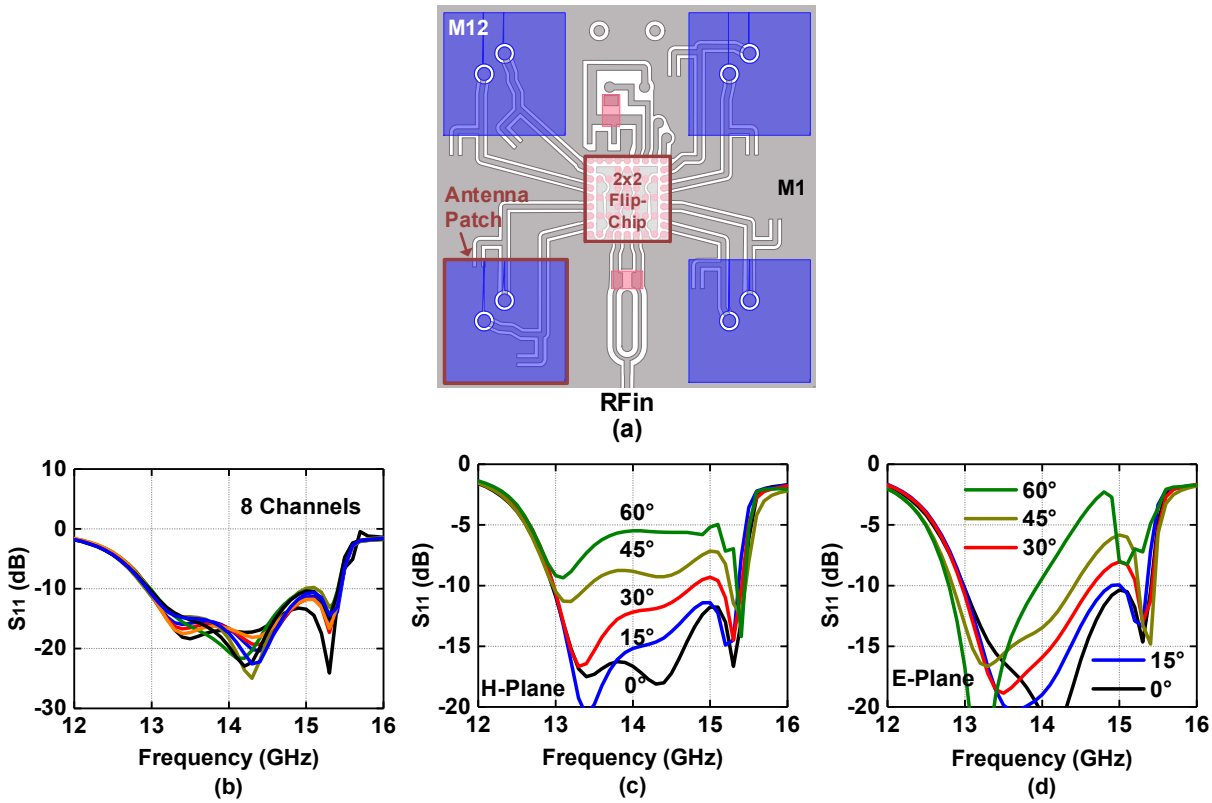


Figure 3.7: (a) 2x2 unit cell PCB design (M1 and M12 are shown). Simulated antenna impedance (S_{11}) at the output chip port of (b) all 8 channels at broadside, and versus scan angle in (c) H-Plane, and (d) E-Plane.

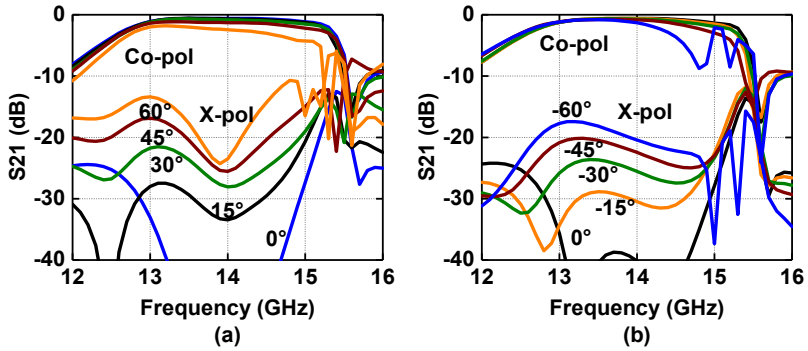


Figure 3.8: Simulated co-and cross-polarized frequency responses versus scan angle in, (a) H-Plane, and (b) E-Plane.

3.5 Antenna and 4-Element Tx Array Measurements

3.5.1 Passive Antenna

A 4-element passive antenna array surrounded by 12 terminated antennas is measured first. Two units are used, one for Tx and one for Rx, and this results in G_{ANT}^2 in the Friis transmission

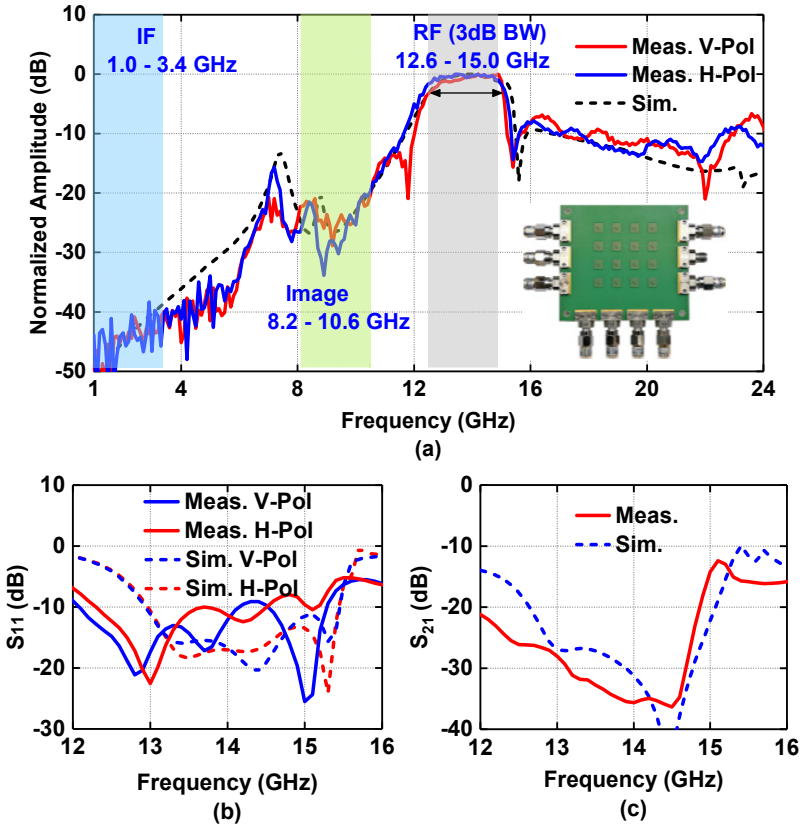


Figure 3.9: Measured and simulated single passive Tx patch antenna's (a) co-polarized frequency response, (b) antenna impedance (S_{11}), and (c) coupling between the antenna dual feeds.

equation. The measured frequency response shows a 3-dB bandwidth of 12.6 – 15.0 GHz [Figure 3.9(a)]. The antenna response provides an image rejection of 22 – 17.8 dBc at 8.2 – 10.6 GHz, for an LO at 10.6 GHz. The measured S_{11} for both polarizations are < -8 dB at 12.3 – 15.2 GHz [Figure 3.9(b)]. The measured coupling between the V and H-feeds is <-34 dB at 14 – 14.5 GHz [Figure 3.9(c)].

3.5.2 4-Element Phased-Array

A 2x2 (4-element) phased-array is used to measure the over-the-air performance of the transmit chip and antennas [Figure 3.10]. The 6-bit phase shifter is toggled, and the corresponding change in phase and gain is recorded [Figure 3.11 (a, b)]. The measured over-the-air RMS

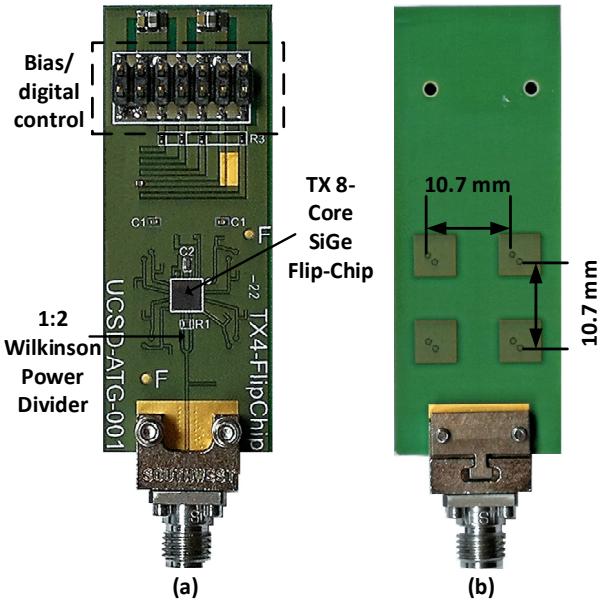


Figure 3.10: (a) Back view of a Ku-band 4-element phased-array showing the Tx 8-channel SiGe flip-chip and (b) front view showing 2x2 dual-polarized antennas.

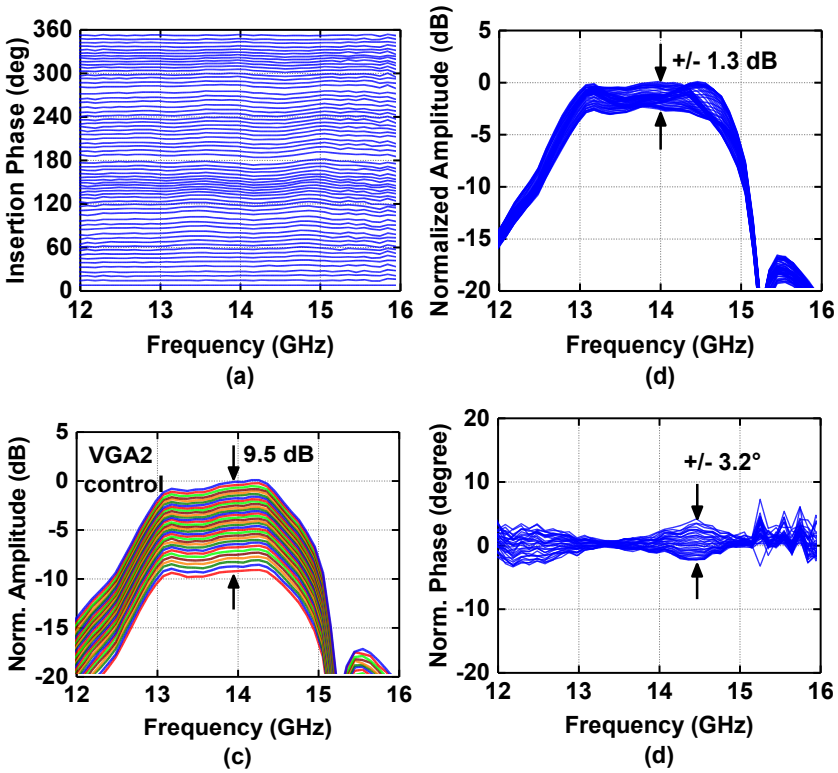


Figure 3.11: Measured over-the-air channel: (a) phase states, (b) gain change with phase states, (c) 2nd VGA gain states, (d) phase change with 2nd VGA gain states (vertical polarization).

amplitude and phase errors for the 6-bit phase shifter are 0.6 dB and 4.2° at 14 GHz. A VGA gain control of 9.5 dB is achieved with 0.25 dB steps, and < ±3.2° in phase change [Figure 3.11(c, b)]. Another VGA offers 6.7 dB of gain control with also ±3° of phase change (not shown), resulting in a total gain control of 16.2 dB.

3.6 Calibration and EIRP Measurements

The dual-polarized transmit phased-array is shown in Figure 3.12, with a size of 17.1 x 21.2 cm^2. The square metal openings are to attach small heat sinks to remove the heat from the PCB (38.4W per polarization).

3.6.1 Calibration

The phased array was calibrated at a range of R= 1.85 m (between D^2/λ and $2D^2/\lambda$) using a Keysight VNA (N5230C) and a receive standard gain horn antenna (Figure 3.13). Four steps were followed: First, each element is turned on individually after setting its nominal gain and zero phase states, and then its S_{21} phase and magnitude were measured. After that, one element is set at 0°, and other elements measured phases were used as calibration offsets for the 255 other antenna elements. Then, each element S_{21} was measured again after the phase calibration is applied. Finally, the measured phases were checked to make sure that the phase differences between elements are less than 5.6°.

Figure 3.14 presents the measured phase difference between the 256 elements before and after phase calibration for both V-and H-pol. The RMS phase error for the V and H-pol is 2.7 °-2.9° after phase calibration. The RMS amplitude error is 1.3-2 dB for the H-and V-Pol [Figure 3.15]. This amplitude error is caused by the Wilkinson power divider network mismatches, various electronic chip and channel gains, and the cyclic variability in the phase shifter gain versus phase

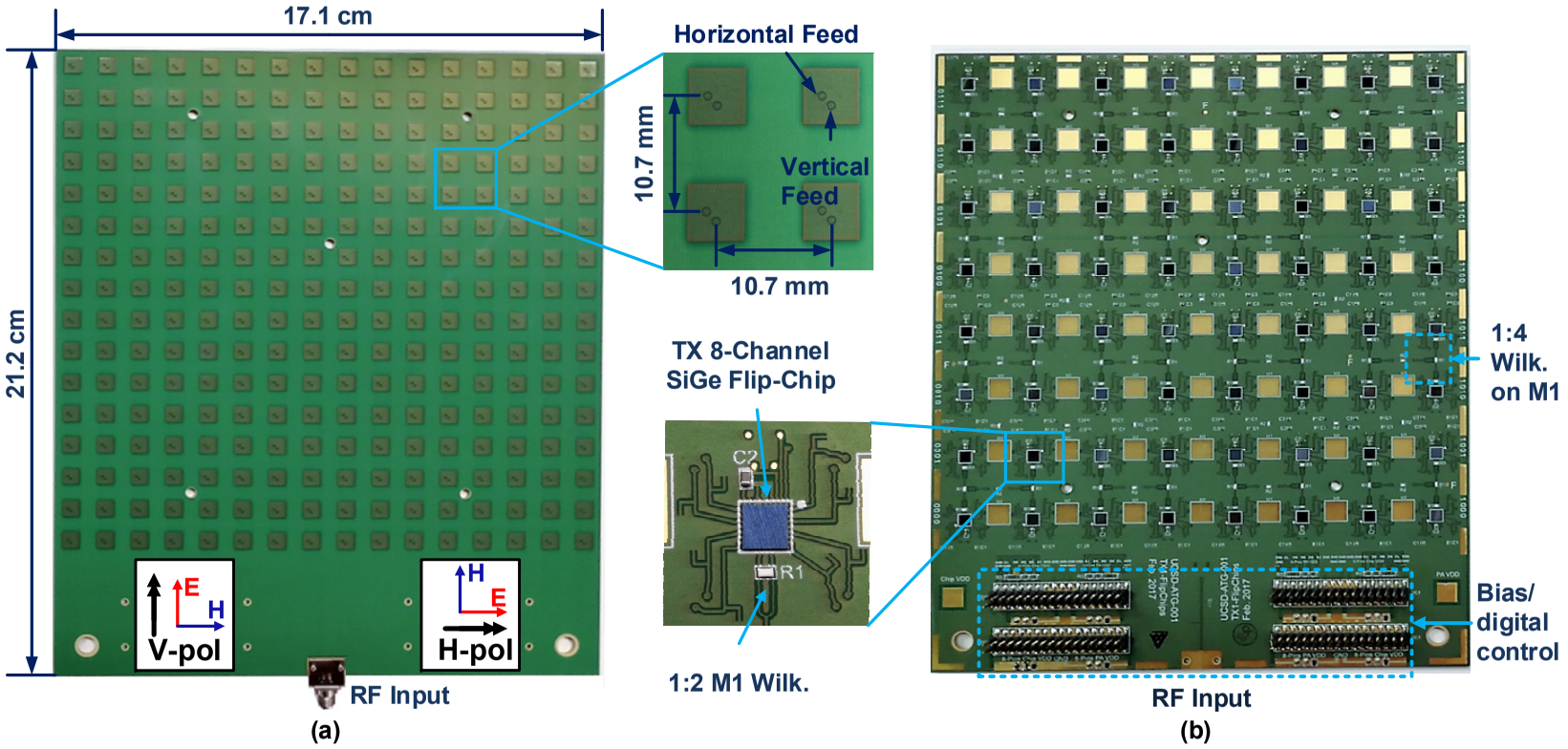
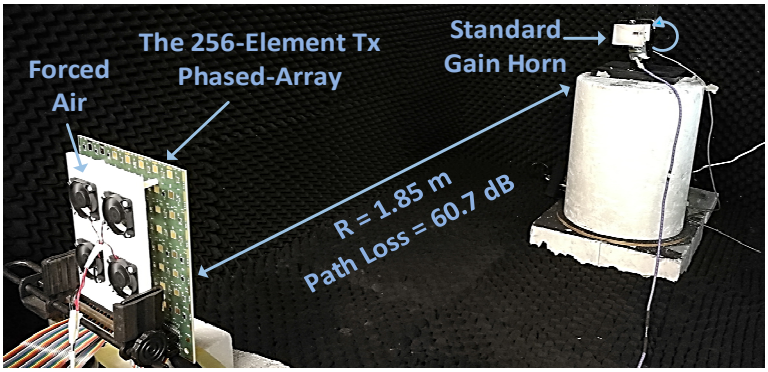
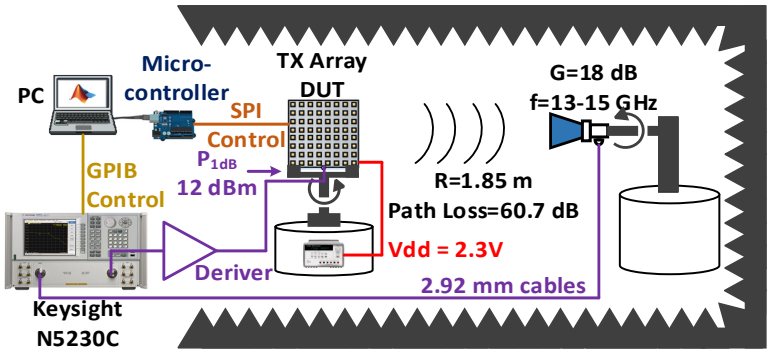


Figure 3.12: (a) Front view of a Ku-band transmitter phased-array tile showing 256 dual-polarized antennas (vertical and horizontal polarization). (b) Back view of the phased-array showing 64 Tx 8-channel SiGe flip-chips.



(a)



(b)

Figure 3.13: Array calibration and pattern measurement setup (a) photograph, and (b) block diagram.

settings (±1.3 dB). The differences in amplitude can be corrected using the VGA on each channel; however, for all the subsequent measured results, only phase calibration was performed. The RMS amplitude error of 1.2-3 dB causes 0.1-0.28 dB of antenna gain reduction, which is acceptable for test purposes [5].

3.6.2 Frequency Response

Figure 3.16 presents the measured co-and cross-polarization frequency response at broadside with uniform illumination at 6 dB backoff, P_{1dB}, $P_{SAT,}$ and each is normalized to its own peak. The 3-dB bandwidth is 13 – 14.6 GHz for V-and H-pol. At 14 GHz, the cross-polarization isolation is 28 - 32 dB.

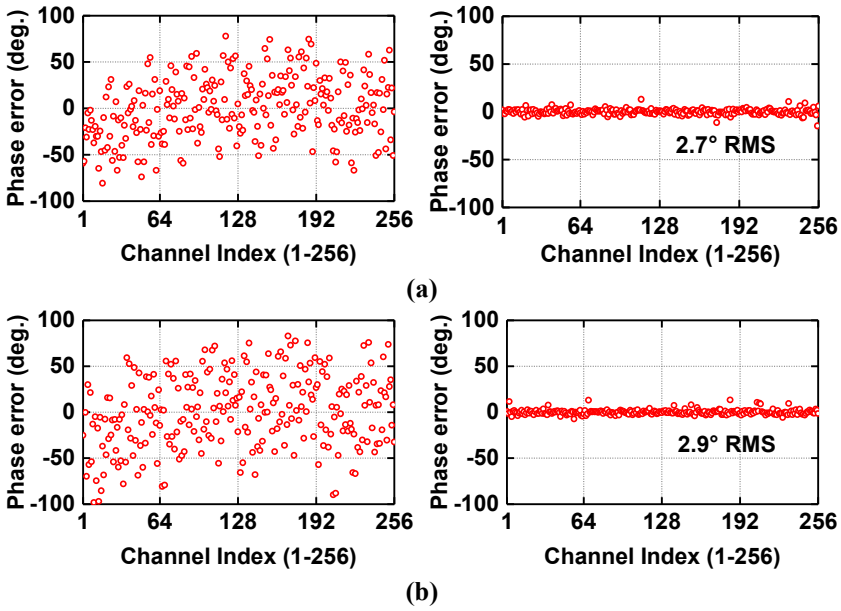


Figure 3.14: The phase errors of the 256 elements before and after phase calibration, (a) vertical polarization, and (b) horizontal polarization, at 14 GHz.

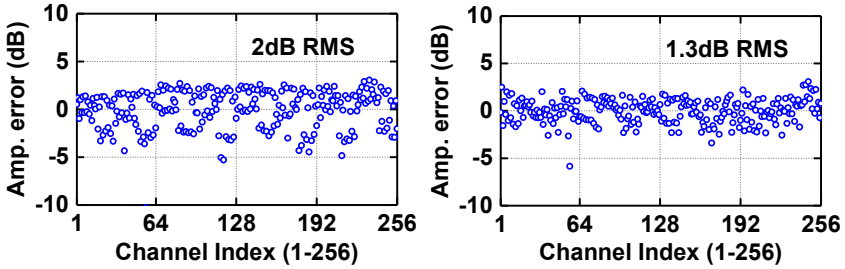


Figure 3.15: The 256 elements' amplitude errors without calibration, (a) vertical polarization, and (b) horizontal polarization, at 14 GHz.

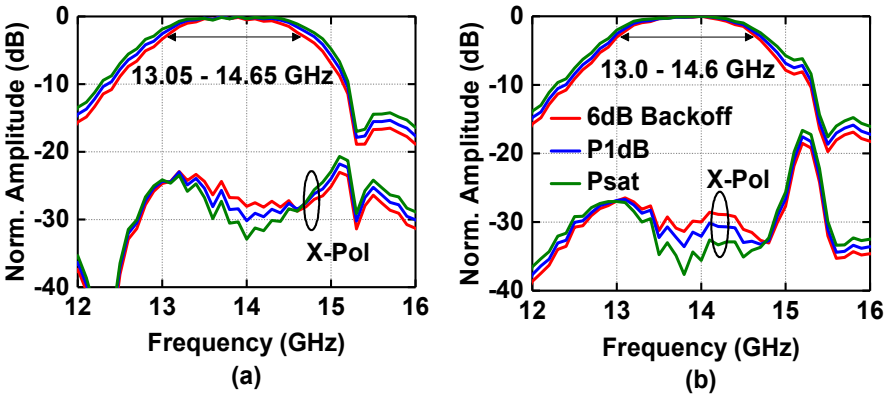


Figure 3.16: Measured co-and cross-polarized frequency responses at broadside with uniform illumination at 6 dB back-off, P_{1dB}, P_{SAT} for (a) vertical polarization, and (b) horizontal polarization.

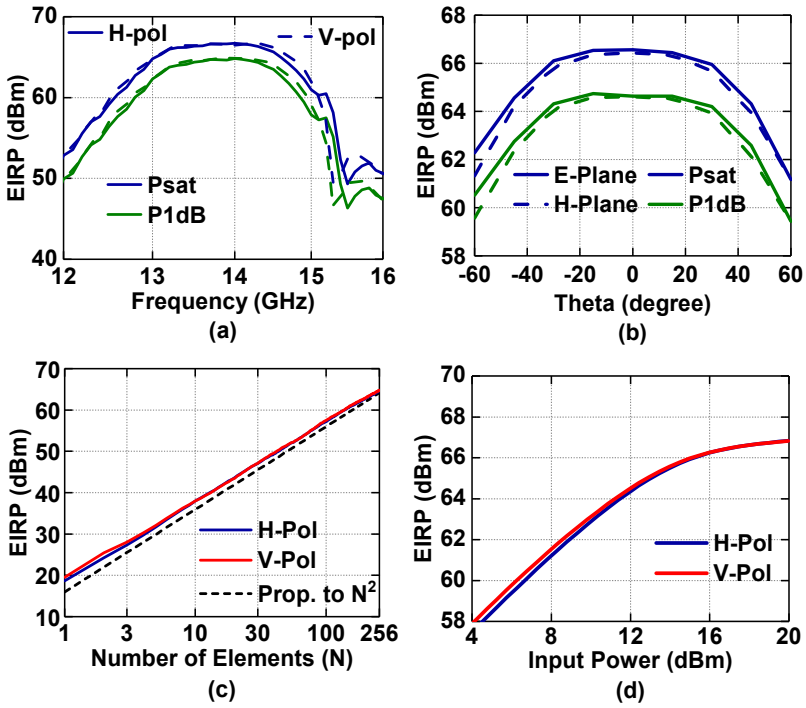


Figure 3.17: Measured EIRP with uniform illumination (a) frequency responses, and (b) versus scan angle at P_{1dB}, $P_{SAT.}$ Measured EIRP versus (c) number of elements at P_{1dB}, and (d) the phased-array input power.

3.6.3 EIRP

The measured EIRP at 14 GHz is 64.5 and 66.5 dBm at P_{1dB} and P_{SAT}, respectively, for uniform illumination and with a single polarization turned on (V-or H-pol) [Figure 3.17(a)]. This agrees with the simulated EIRP of 64 dBm. The measured EIRP versus scan angle at P_{1dB} and P_{SAT} is presented in Figure 3.17 (b), with a 4.1-5.2 dB drop at 60°scan angle in the E and H-plane, respectively. The drop in EIRP follows a $\cos^{1.3}(\theta)$ - $\cos^{1.5}(\theta)$ in the and E and H-plane, respectively. It is due to the $\cos(\theta)$ factor arising from the reduced aperture and to mismatch between the active antenna impedance and the power amplifier.

The measured $EIRP_{1dB}$ at 14 GHz versus the number of elements is presented in Figure 3.17 (c), and it is proportional N^2 for both V and H-polarizations, as expected. An input power of 12.5 dBm is required at the RF coaxial port to result in $EIRP_{1dB}$ and agrees well with simulations [Figure 3.17 (d)].

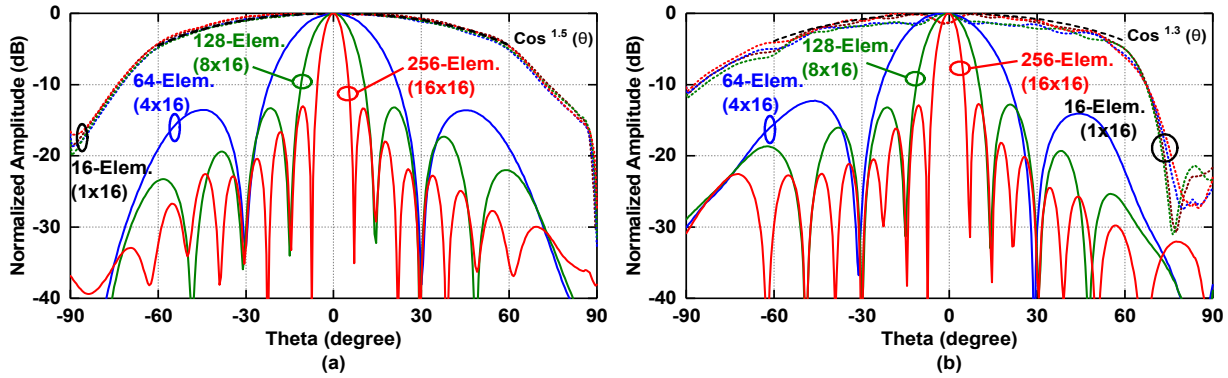


Figure 3.18: Measured co-polarized active patterns in (a) H-Plane (V-Pol), and (a) E-Plane (H-Pol). (Both are measured in the Azimuth plane for one, four, eight, and sixteen columns).

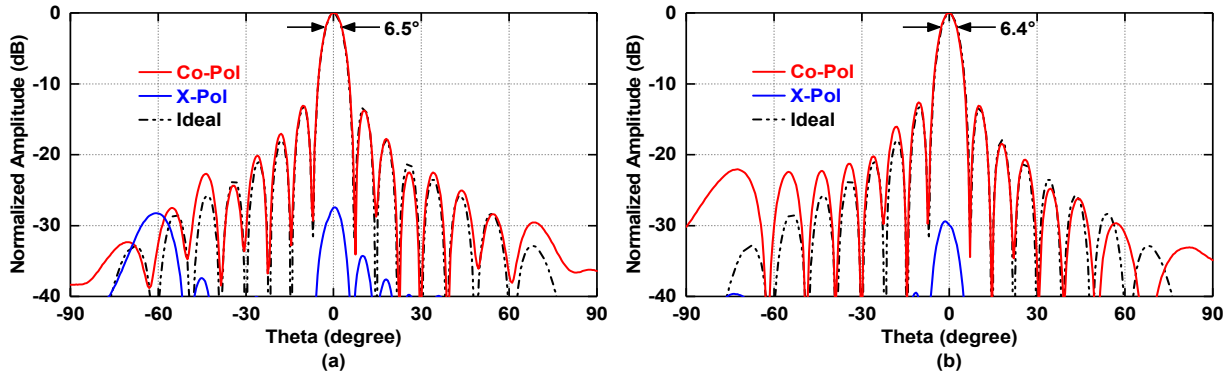


Figure 3.19: Measured co-and cross-polarized patterns at broadside at 14 GHz with uniform illumination for (a) vertical polarization (H-Plane), and (b) horizontal polarization (E-Plane).

3.7 Pattern Measurements

3.7.1 Linear Polarization

Figure 3.18 presents the measured co-polarized active element patterns for E-Plane (H-Pol) and H-Plane (V-Pol). This is done in the Azimuth plane with one, four, eight, and 16 columns turned ON. In the E-plane pattern at 14 GHz, the active patterns fit a $\cos^{1.3}(\theta)$ roll-off with a 4.0 dB drop at ±60°, while the H-plane pattern at the same frequency fit a $\cos^{1.5}(\theta)$ roll-off with a 4.5 dB drop at ±60°.

Figure 3.19 presents the measured co-and cross-polarization patterns at broadside with uniform illumination for the vertical polarization (H-plane) and the horizontal polarization

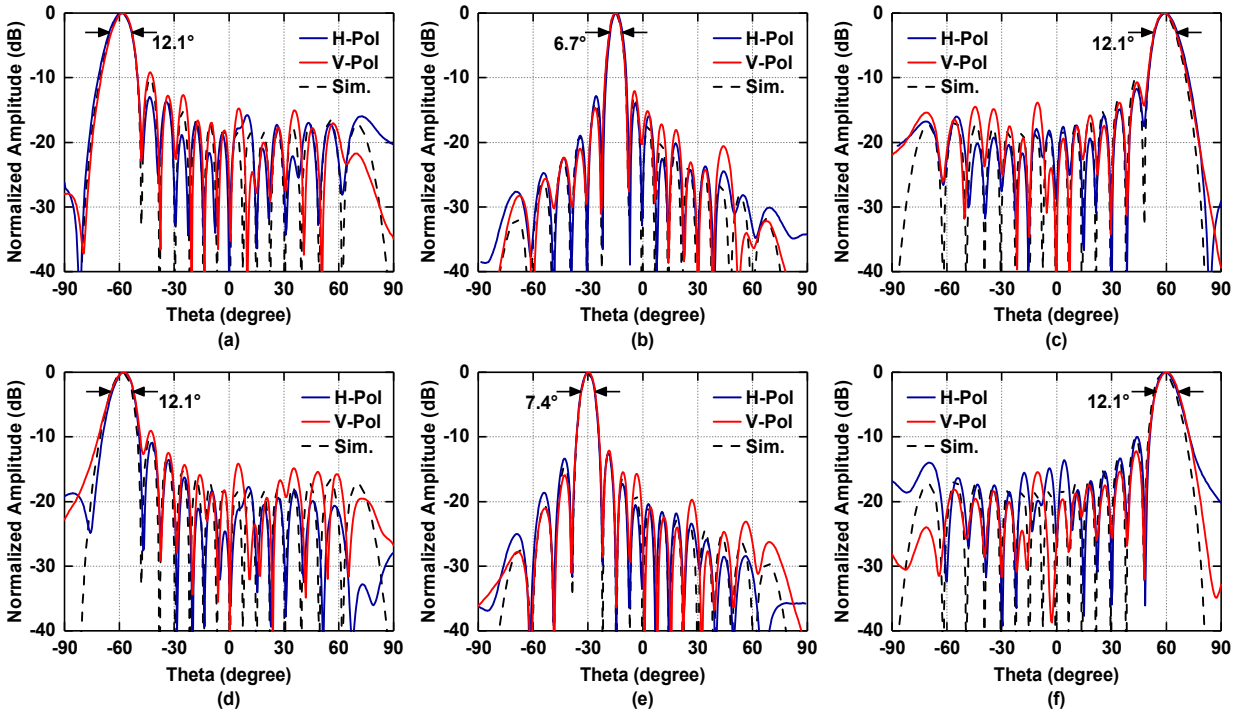


Figure 3.20: Measured co-polarized (H-plane) patterns at (a) -60°, (b) -15°, and (c) 60. Measured co-polarized (E-plane) patterns at (d) -60°, (e) -30°, and (f) 60°. (Vertical and horizontal polarization patterns are at 14 GHz with uniform illumination).

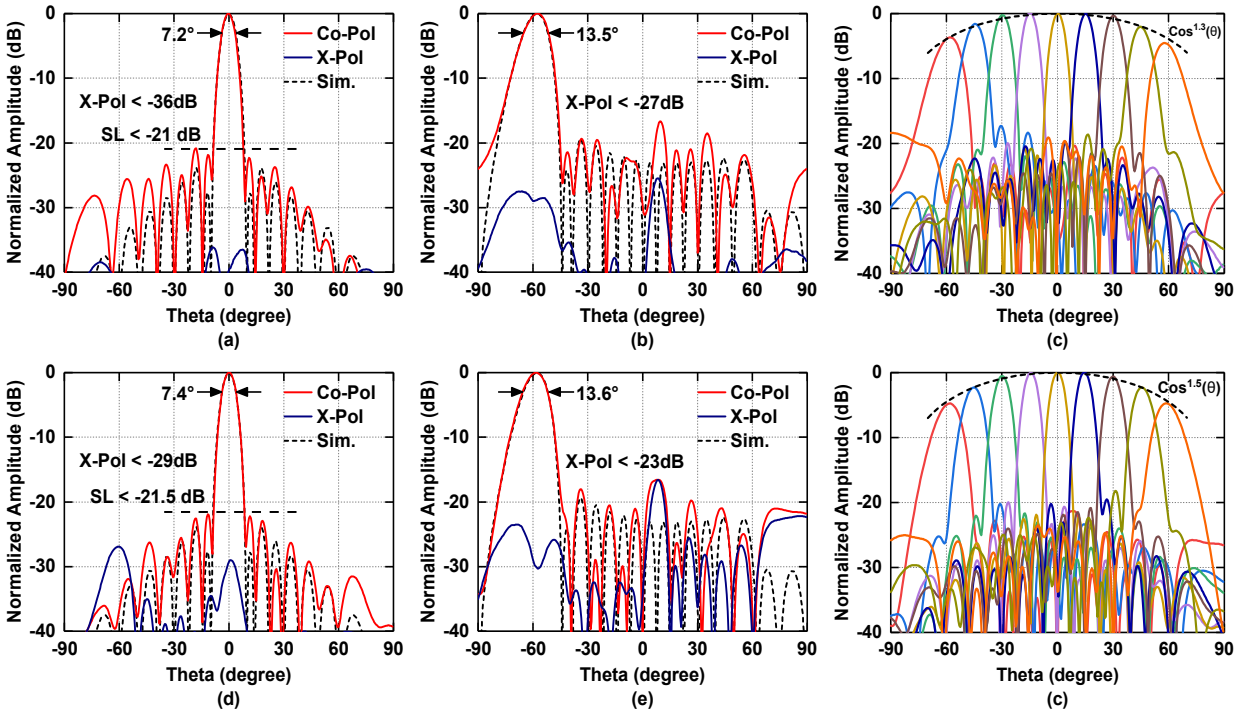


Figure 3.21: Measured E-Plane patterns (H-Pol) at (a) 0°, (b) -60°, and (c) -60° to +60°. Measured H-Plane patterns (V-Pol) with at (d) 0°, (e) -60°, and (f) -60° to +60°. (All patterns are at 14 GHz with 8-dB Raised-Cosine taper illumination and phase calibration at 14 GHz).

(E-Plane) at 14 GHz. All patterns are near-ideal and match simulations with cross-polarization levels of < -27 dB and sidelobe levels of < -12.7 dB for uniform illumination. The 3-dB beamwidth is 6.4° and agrees with (3.5).

The antenna element is placed in a symmetric gird and with symmetric dual-polarized feeds. Therefore, the co-polarization patterns in the E-plane of the V-and H-Pol antenna feeds are expected to be the same. Similarly, the H-plane patterns for the V-and H-pol antenna feeds will be similar. Figure 3.20 presents the measured E-plane and H-plane patterns for V-pol and H-Pol patterns at different scan angles, and they are nearly identical. The 3-dB beamwidth increases from 6.5° at broadside to 12.1° at ±60°scan angles. The difference in the sidelobe levels between measurements and simulations is due to the residual amplitude error on the array.

To reduce those sidelobes levels and meet a satellite communications mask in a larger phased array, an 8-dB raised-cosine taper is applied using VGA_2 in the Tx channels. At broadside, the 3-dB beamwidth increases to 7.2° ~ 7.4°, and the sidelobes levels are <-20 dB (Figure 3.21). Both the E-plane and H-plane patterns, with no amplitude calibration, have low sidelobes levels (< -17 dB) and high cross-polarization isolation of 27-23 dB up to ±45° and ±60° scan angles, respectively. The tapered E-and H-planes patterns at 14 GHz fit the roll-off of the active element patterns.

Figure 3.22 presents the measured patterns in the 45° plane for the vertical polarization with uniform illuminations and with sidelobe levels < -25 dB overall scan angles. As expected, the diagonal-plane patterns show very low sidelobe levels in a square grid [6].

3.7.2 Circular Polarization

Circular polarization can also be transmitted using the dual-polarized array. The V and H-pol antenna elements are both turned ON with a phase offset of ±90° for left-hand circular

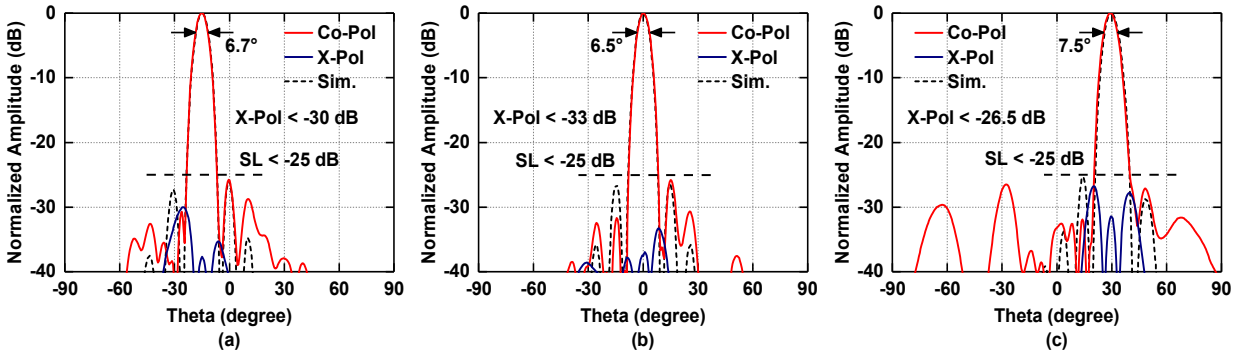


Figure 3.22: Measured vertical polarization patterns in the 45° plane with uniform illumination at (a) -15°, (b) 0°, and (c) 30° at 14 GHz.

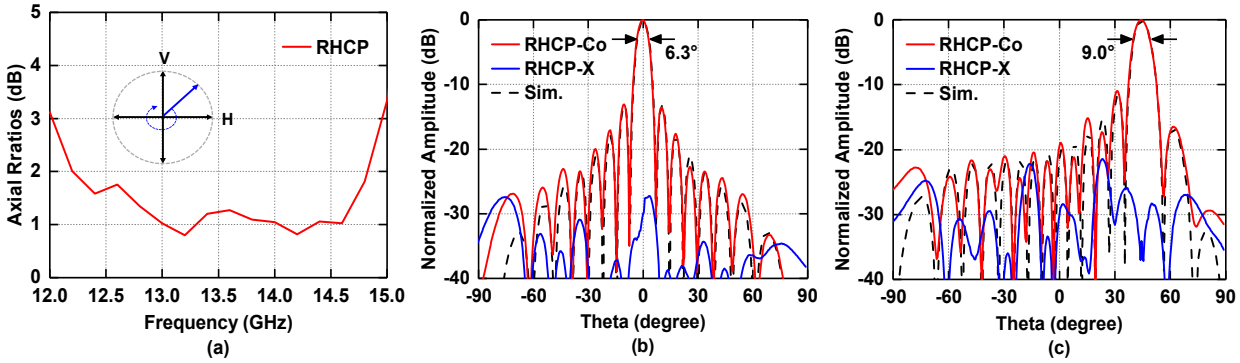


Figure 3.23: Measured (a) axial ratio (AR) versus rotation angle of the receive horn antenna, co-and cross-polarized patterns RHCP at (b) 0°, and (c) 45°. Patterns are at 14 GHz in elevation plane and cross-polarization optimization is applied with a single-point calibration at 14 GHz.

polarization (LHCP) or right-hand circular polarization (RHCP). The measured axial-ratio (AR, defined as the ratio of the major to minor axes of a polarization ellipse [7]) is <1.1 dB in the RHCP at 14-14.5 GHz, and <1.5 dB at 12.8 - 14.6 GHz, using a single-point calibration at 14 GHz (AR=1.1 dB is cross-pol level -24 dB [1]). The measured RHCP patterns with uniform illumination are similar to the linearly polarized patterns with near-ideal sidelobes levels (Figure 3.23). These results are achieved with cross-polarization optimization, which is detailed in [1].

3.7.3 Rotated-Linear Polarization

For Ku-band satellites with a linearly polarized receiver, it is essential for the transmitter in the SOTM terminal to form any desired rotated-linear polarization. This is done by exciting the

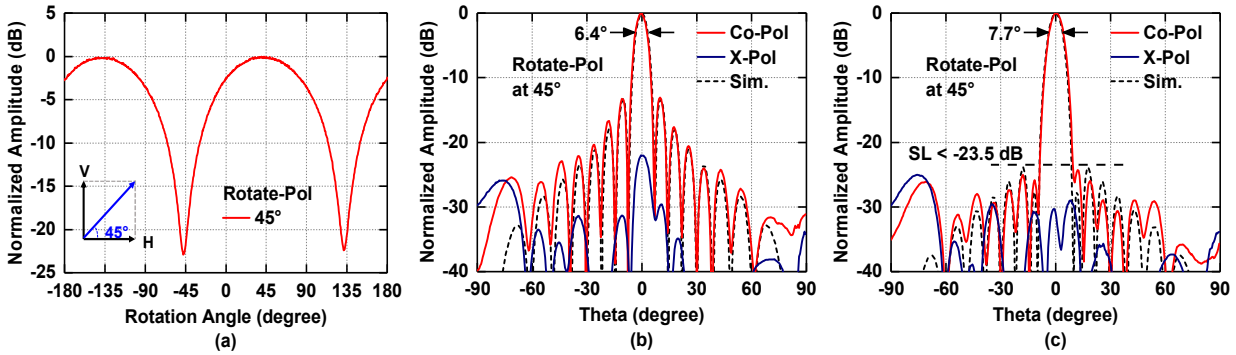


Figure 3.24: Measured (a) normalized amplitude versus rotation angle of the receive horn antenna, co-and cross-polarization patterns in the elevation plane at broadside (b) with uniform, and (c) 8-dB Raised-Cosine taper illuminations. All patterns are at 14 GHz.

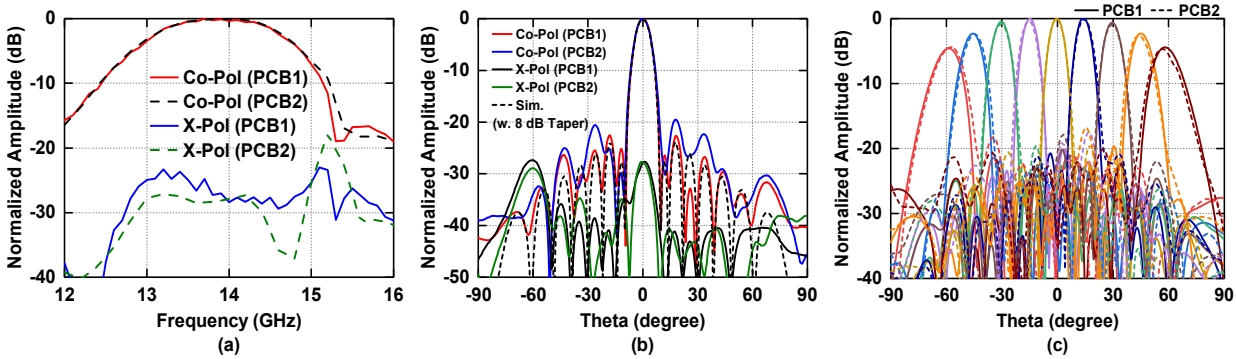


Figure 3.25: Measured PCB_1 vs. PCB_2 co-and cross-polarization (a) frequency responses, (b) patterns at 0°, (c) scanned patterns to ±60°. (H-Plane patterns (V-Pol) with 8-dB Raised-Cosine taper illumination are shown at 14 GHz).

two orthogonal polarizations (V-and H-pol) in-phase and with the appropriate weights. The Ku-band phased-array was set to transmit in 45°linearly rotated polarization mode with V-and H-pol excited with the equal amplitude and phase. The measured patterns with uniform and 8-dB raised-cosine taper illuminations at boresight agree well with simulations, as shown in Figure 3.24.

3.7.4 Array to Array Comparison

A second phased array (PCB2) was fabricated for comparison. This array employs the same stack-up and same chips as in PCB1 discussed above. The second array was not calibrated individually, but rather, the same phase-calibration coefficients obtained from PCB1 were applied to PCB2. This was done to demonstrate the repeatability of the multilayer PCB fabrication process

and the silicon chips, and the robustness of the scalable 256-element phased-array. The measured co-and cross-polarization frequency responses of both arrays are very similar, as shown in Figure 3.25(a). Moreover, the measured scanned co- and cross-pol patterns at 0° of the two arrays agree with each other and maintain a high cross-pol rejection > 28 dB [Figure 3.25(b)]. The scanned patterns of the V-Pol in the H-plane from -60° to 60° are measured for the two arrays and with good agreement [Figure 3.25(c)].

3.8 ACPR and EVM Measurements

A missing criterion in SATCOM phased arrays is a comprehensive data set on their ACPR and EVM performance versus modulation, bandwidth, and scan angle. Different QPSK, 8-PSK, and 16-PSK waveforms with up to 500 MHz bandwidths are generated at an IF of 1.15 GHz using an arbitrary waveform generator (AWG). The modulated data is up-converted to 14.2 GHz using a Ku-Band block upconverter (BUC) with a 13.05 GHz local oscillator (LO). The BUC has a conversion gain of 55 dB at 14.25 GHz with a 3-dB bandwidth of 14 – 14.5 GHz and is the limiting factor for the maximum allowable data rate. The BUC has an output P1dB of 33 dBm and is operated at 12.5 dBm (20 dB backoff) power levels to ensure that any ACPR is due to non-linear contributions of the array itself. One the Rx-side, a standard gain horn antenna is used, and the signal is fed to a Keysight spectrum analyzer or a DSO-Z series scope for waveform analysis using the Keysight 89600 VSA software module [Figure 3.26(a)].

The first order of analysis is to determine the radiated noise from the array. The AWG is operated at 1.15 GHz with a measured output power of -13.5 dBm and a measured wideband noise of -139 dBm/Hz, which results in a signal-to-noise ratio (SNR) of 45.5 dB for a 100-MHz waveform. This waveform is then attenuated by 33 dB to operate the BUC at 20 dB backoff. The measured noise at the BUC output is -107 dBm/Hz at an output signal of 8.5 dBm, resulting in an

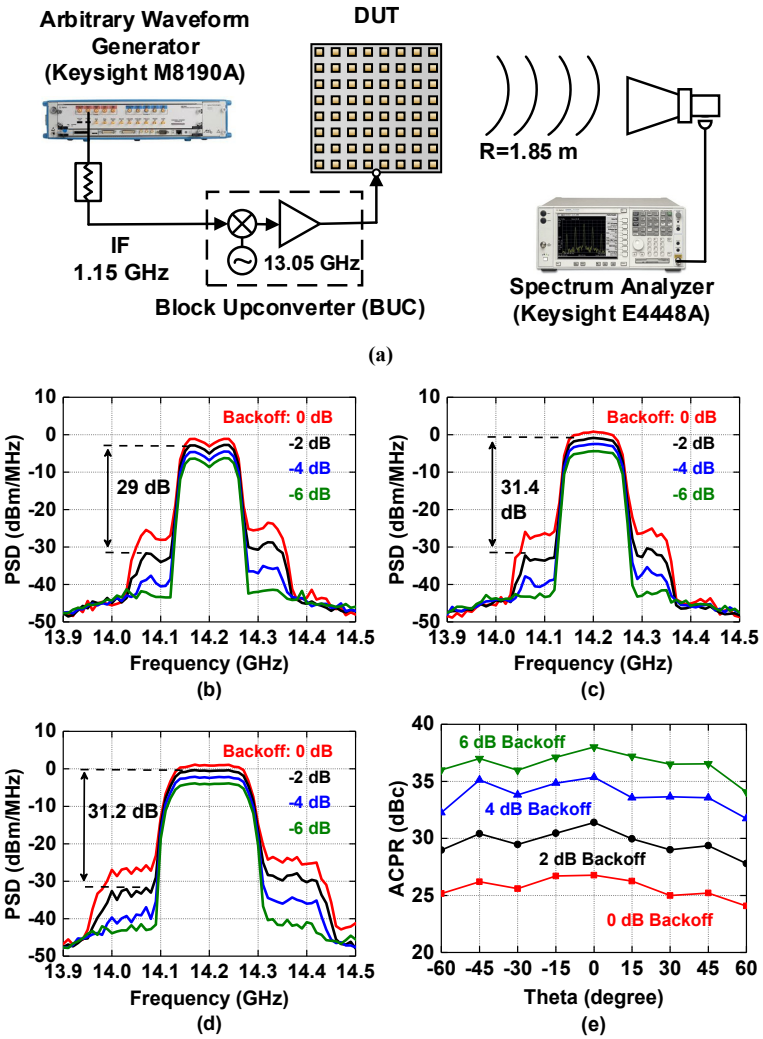


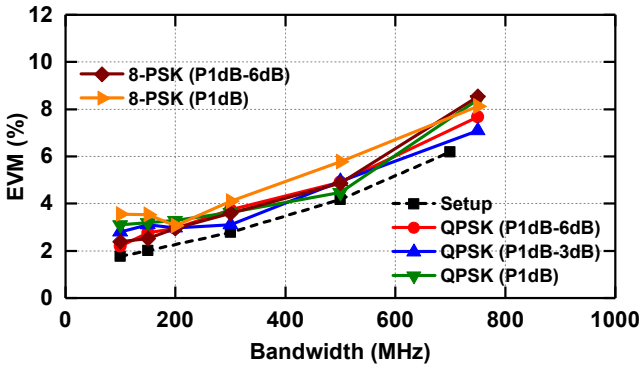
Figure 3.26: (a) ACPR measurement setup. Measured far-field ACPR for (b) QPSK (100 MBaud), (c) 8-PSK (100 MBaud), and (d) 8-PSK (150 MBaud) modulation. (e) Measured far-field ACPR versus scan angle for the E-plane (H-pol.) with 8-PSK modulation and 100 MBaud.

SNR = 35.5 dB. The AWG+BUC output noise is sent to all the beamformer chips and radiates coherently from the array. The available noise at the input of each beamformer chip is -107 dBm - 21 dB (division loss) – 13.5 dB (ohmic loss) = -141.5 dBm/Hz, which is much higher than the beamformer Tx NF of 8-9 dB (-165 dBm/Hz). Therefore, the AWG+BUC noise dominates the radiated noise (and SNR), and one can ignore the beamformer noise. Note also that the beamformer noise radiates incoherently from the 256-element array (different channels having different noise) and therefore increases as N and not as N^2 as the BUC noise, thereby contributing even less in the far-field.

Figure 3.26(b) presents the measured ACPR for different backoff power levels using a QPSK modulated waveform with 100 MHz bandwidth (MBaud) and a root-raised cosine pulse filter of ($\alpha = 0.35$), which results in a peak to average power ratio (PAPR) of 4 dB [8]. A 0 to -2 dB backoff from EIRP P1dB results in an ACPR of -24.3 dBc to -29 dBc.

The measured ACPR for an 8-PSK modulated waveform with 100 and 150 MBaud symbol rates are shown in Figure 3.26 (c, d). A 0 to -2 dB backoff from EIRP P1dB results in an ACPR around -27 dBc to -31 dBc for 100 and 150 MBaud symbol rates. Figure 3.26(e) presents the measured ACPR 8-PSK modulated waveform with a 100 MBaud symbol rate versus scan angle. The scan angle effect on the ACPR is negligible due to the small fractional bandwidth of the modulated signal.

Figure 3.27(a) presents the measured EVM versus bandwidth for QPSK, 8-PSK, and 16-PSK waveforms at various bandwidths for the vertical polarization at boresight. The measured EVM for the setup alone (QPSK waveforms) is 1.8% for 100 MHz bandwidth and increases to 6.2% for 700 MHz bandwidth, limited by the BUC bandwidth. For QPSK waveforms, the measured EVMs for 100 MHz bandwidth are 2.2% - 3.1% for -6 to 0 dB backoff, respectively.



(a)

Bandwidth	100MHz	200MHz	300MHz	500MHz
QPSK Constellation α = 0.35 0 dB Backoff PAPR=4dB				
EVM	3.1 %	3.3 %	3.6 %	4.5 %
8-PSK Constellation α = 0.35 0 dB Backoff PAPR=4dB				
EVM	3.5 %	3.1 %	4.1 %	5.8 %
16-PSK Constellation α = 0.35 0 dB Backoff PAPR=4dB				
EVM	4.0 %	5.9 %		

(b)

Constellation	16-QAM	32-QAM	64-QAM	128-QAM
100 MHz Bandwidth α = 0.35 3 dB Backoff				
EVM	2.9 %	2.6 %	2.6 %	2.2 %

(c)

Figure 3.27: (a) Measured EVM versus bandwidth using QPSK, 8-PSK, and 16-PSK waveforms at various backoffs, (b) measured constellations at 0 dB backoff for QPSK, 8-PSK, and 16-PSK waveforms and various bandwidths, (c) measured constellations at 3 dB backoff for 16-, 32-, 64-, and 128-QAMs and 100 MHz bandwidth. (Vertical polarization at broadside is shown)

When the bandwidth increases to 500 MHz, the EVM remains <5% for the same backoff levels, with 4% due to the source itself. Similar results to within ±1 % are obtained for 8-PSK waveforms.

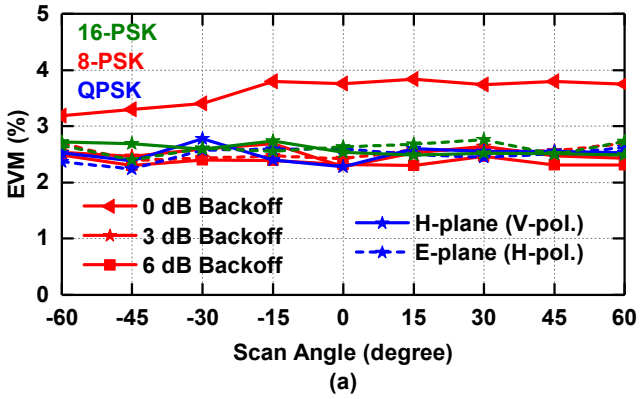
Figure 3.27(b) presents the measured constellations for the vertical polarization at broadside and 0 dB backoff for QPSK, 8-PSK, and 16-PSK waveforms and various bandwidths, and with excellent EVM. Similar results are obtained for the horizontal polarization and are not shown. The array can also handle 16-, 32-, 64-, and 128-QAMs constellations, as shown in Figure 3.27(c). This is important for the new generation of satellites that employ complex waveforms.

The EVM was also measured versus scan angle in the H-Plane (V-pol.) and E-plane (H-pol.) using 100-Mbaud QPSK, 8-PSK, and 16-PSK waveforms at various backoff levels [Figure 3.28(a)]. Over the entire scan range of ±60°, the EVM is < 3% for all waveforms with 3 or higher backoff power levels. Figure 3.28(b) presents the measured constellations for the vertical polarization at different scan angles and at 3 dB backoff for QPSK, 8-PSK, and 16-PSK 100 MHz waveforms. Excellent results are achieved. This extensive set of measurements shows that the phased arrays can handle complex waveforms and that the ACPR and EVM do not degrade versus scan angle.

3.9 Null Steering Patterns

For Low Earth Orbit (LEO) and Medium Earth orbit (MEO) satellite constellations, it is essential to communicate to the satellite without radiating energy into the GEO orbits. One way to achieve this is to synthesize deep nulls in the patterns. This can be done using mostly amplitude control (with a bit of phase change), mostly phase control (with a bit of amplitude change), or a combination of both.

Figure 3.29 presents results for a moving null with the scanned beam (fixed angle from the main beam), and Figure 3.30 presents results for a fixed null independent of the beam scan angle.



(a)

Scan Angle	-60°	-30°	0°	60°
QPSK Constellation α = 0.35 3 dB Backoff PAPR=4dB				
EVM	2.5 %	2.8 %	2.3 %	2.5 %
8-PSK Constellation α = 0.35 3 dB Backoff PAPR=4dB				
EVM	2.5 %	2.6 %	2.3 %	2.4 %
16-PSK Constellation α = 0.35 3 dB Backoff PAPR=4dB				
EVM	2.7 %	2.6 %	2.5 %	2.5 %

(b)

Figure 3.28: (a) Measured EVM versus scan angle in the H-Plane (V-pol.) and E-plane (H-pol.) using 100-Mbaud QPSK, 8-PSK, and 16-PSK waveforms at various backoffs, (b) measured constellations versus scan angle in the H-Plane (V-pol.) at 3 dB backoff.

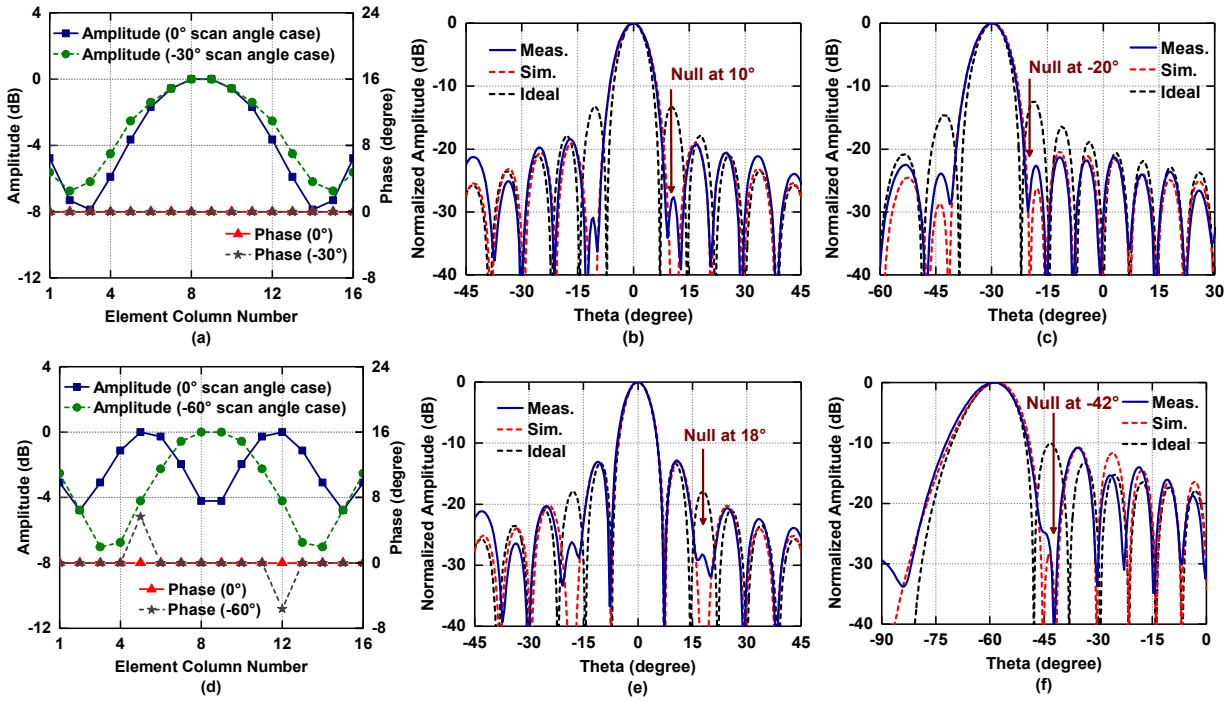


Figure 3.29: (a) Applied current distribution (amplitude and phase) for a moving null (10°). Measured scanned patterns at (b) 0°, (c) -30° with null located 10° from the main beam. (d) Applied current distribution (amplitudes and phases) for a moving null (18°). Measured scanned patterns at (e) 0°, (f) -60° with null located 18° from the main beam. (Patterns are at 14 GHz with phase calibration at 14 GHz).

The fixed-null case is critical for a ground terminal establishing a connection to a LEO or MEO satellite and avoiding a GEO satellite.

The results are based on amplitude control (mostly) with the excitations obtained using the MATLAB Phased Array System Toolbox[11]. The penalty in EIRP can be 2-3 dB, so phase control is a better solution. However, it was not implemented. Also, note that amplitude calibration is not done, and the deep nulls are achieved with a 2 dB RMS error across the aperture (see Figure 3.15).

Figure 3.31 presents the null bandwidth with phase and amplitude settings done at 14 GHz. A deep null can be maintained over the entire waveform bandwidth (100-250 MHz) even at wide scan angles. Also, the instantaneous patterns at f_o-200 MHz, f_o, and f_o+200 MHz are shown and remain nearly identical versus frequency, except for the expected beam squint at 60° scan angle.

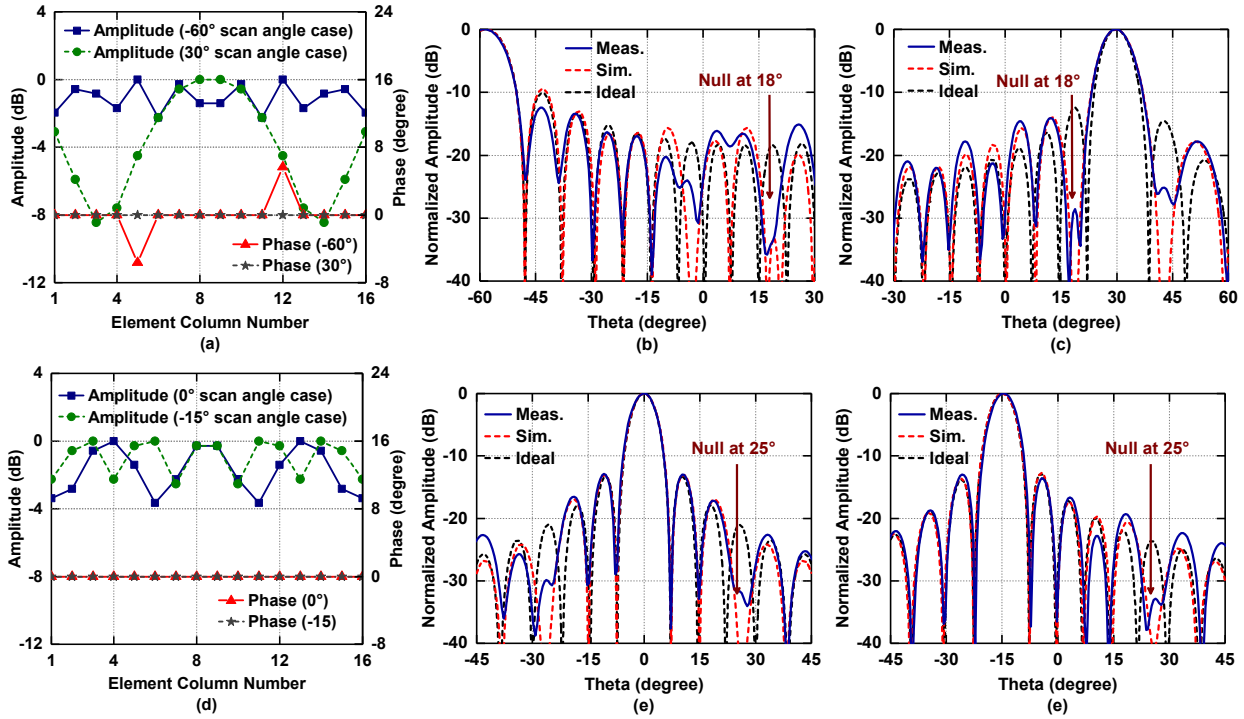


Figure 3.30: (a) Applied current distribution (amplitude and phase) for a fixed null at 18° for scanned patterns. Measured scanned patterns at (b) -60°, (c) 30° with null located at 18°. (d) Applied current distribution (amplitudes and phases) for a fixed null at 25°. Measured scanned patterns at (e) 0°, (f) -15° showing null located at 25°. (Patterns are at 14 GHz with phase calibration at 14 GHz).

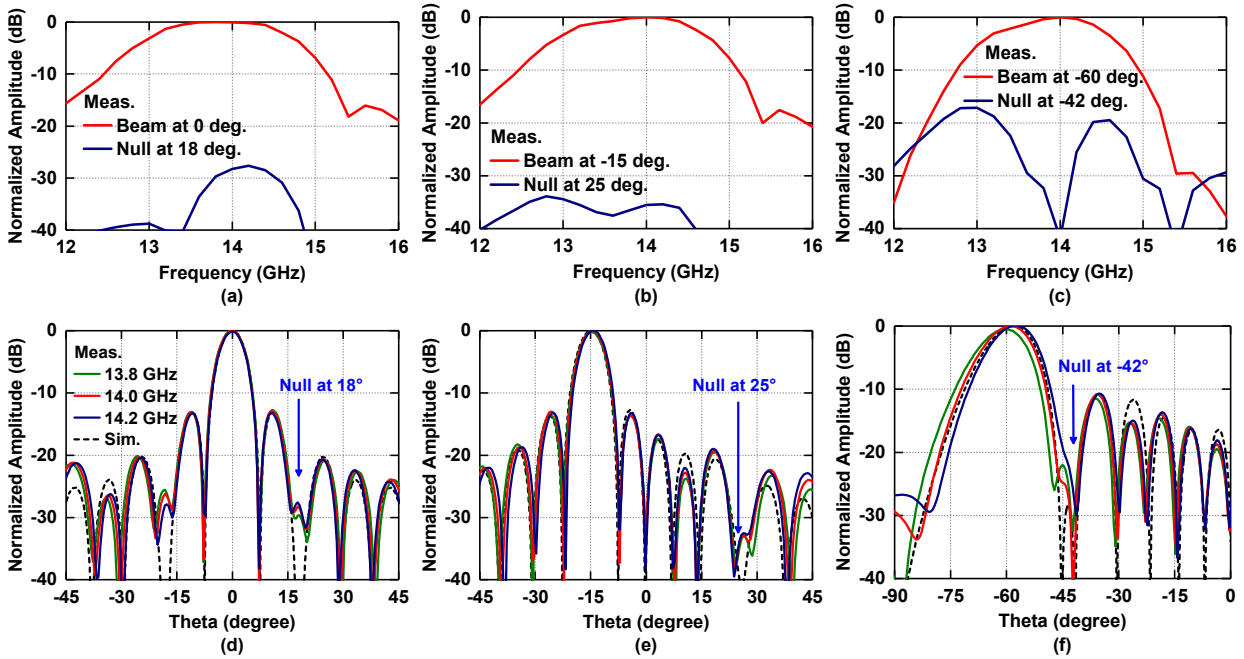


Figure 3.31: Measured co-polarized frequency response for (a) beam at 0° and null at 18°, (b) beam at -15° and fixed null at 25°, and (c) beam at -60° and null at -42°. Measured beam patterns at 13.8–14.2 GHz for (d) beam at 0° with null at 18°, (e) beam at -15° with fixed null at 25°, and (e) beam at -60° with null at -42°. (Phase calibration at 14 GHz). The beam squint versus frequency is clearly seen at -60° scan angle.

Detailed analysis of the beam squint effects versus bandwidth and scan angle are presented in chapter 1.

Table II summarizes the 256-element transmit phased-array and compares it with other large-scale state-of-the-art Ku-band phased arrays. This work demonstrates the highest measured EIRP per polarization and the widest bandwidth and a scan range of 120°, without the need for any mechanical parts, and with low roll-off at ±60° in both azimuth and elevation planes at a power consumption of 150 mW per element at P1dB. Moreover, this work showed <-17 dB sidelobes with 8-dB raised-cosine taper illumination and high polarization purity > 23 dB over the whole scan range.

3.10 Conclusion

This chapter presented an ultra-low-profile dual-polarized 256-element Ku-band phased-array transmit tile for SATCOM on-the-move applications. The design had a wide 3-dB instantaneous bandwidth of 13.0 – 14.6 GHz and a wide beam scanning range of 120° with low drop-off in the azimuth and elevation planes. The phased-array achieved a measured EIRP of 64.5-dBm and 66.5-dBm at P1dB and Psat, respectively, per polarization and high cross-polarization isolation of 27 dB up to ±45° and 23 dB at ±60° scan angle, in the azimuth and elevation planes. The measured EVM and ACPR were excellent at P_{1dB} values, showing that the array can be operated without backoff, thereby increasing the overall system efficiency of affordable mobile Ku-band SOTM terminals.

Table 3.2: Comparison with state-of-the-art transmit Ku-band phased arrays

Parameter		**This Work**	[9] EuCAP 2013	[10] TAP 2015
Frequency (GHz)		**13.0 – 14.6 (1.6 GHz BW)**	14.0 – 14.5 (0.5 GHz BW)	14.0 – 14.5 (0.5 GHz BW)
Number of Elements		**256 (16x16)**	128 (8x16)[#]	384 (32x12)
Polarization		**Dual Linear, Rotated, LHCP, RHCP**	Linear	Dual Linear
EIRP (dBW) @P1dB/Psat		**34.5/36.5**	31.5	-
Electronic Beam-Steering Range	Elevation	**120° (-60° to +60°)**	70° (20° to +90°)	60° (15° to +75°)
	Azimuth	**120° (-60° to +60°)**	0°	0°
Sidelobes Level at Boresight (dB)		**< -13 (w. uniform illumination) <-21 (w. 8-dB taper illumination)**	< -13* -	< -11* -
Cross-Polar Isolation (dB)		**> 29 (at 0° in Elev. & AZ) > 23 (over scan range)**	> 17* -	>30 >20
Power Consumption		**150 mW per element at P1dB 38.4 W (per polarization)**	-	-

*Estimated from plots #From the photograph

3.11 Acknowledgment

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Chapter 4

Packaged K-band SiGe and CMOS SOI LNAs for SATCOM Applications

4.1 Introduction

In recent years, there has been a growing demand for higher data rates and mobile connectivity over larger coverage areas. SATCOM on-the-move (SOTM) applications are intended to serve this purpose. To enable mobility, phased arrays (instead of mechanically steerable antennas) are considered for SOTM terminals. The feasibility of SATCOM phased arrays is aided by the significant progress in silicon-based semiconductor technologies, as demonstrated in the past few years [1, 2].

One key parameter that determines the phased array size (and consequently its cost) is the required gain-to-noise-temperature (G/T). In Ku- and K-band SATCOM phased-arrays, the overall system sensitivity and G/T are not only affected by LNAs' NF but LNAs' locations too. The space between antenna elements in such phased-arrays is larger than the size of a 4-element beamformer chip, as shown in Figure 4.1 (a & b). Therefore, integrating LNAs into the beamformer chip is not the optimal solution and will degrade the overall array sensitivity and G/T due to the ohmic loss of the transmission line between the beamformer chip and antenna feed, Figure 4.1 (c). To avoid

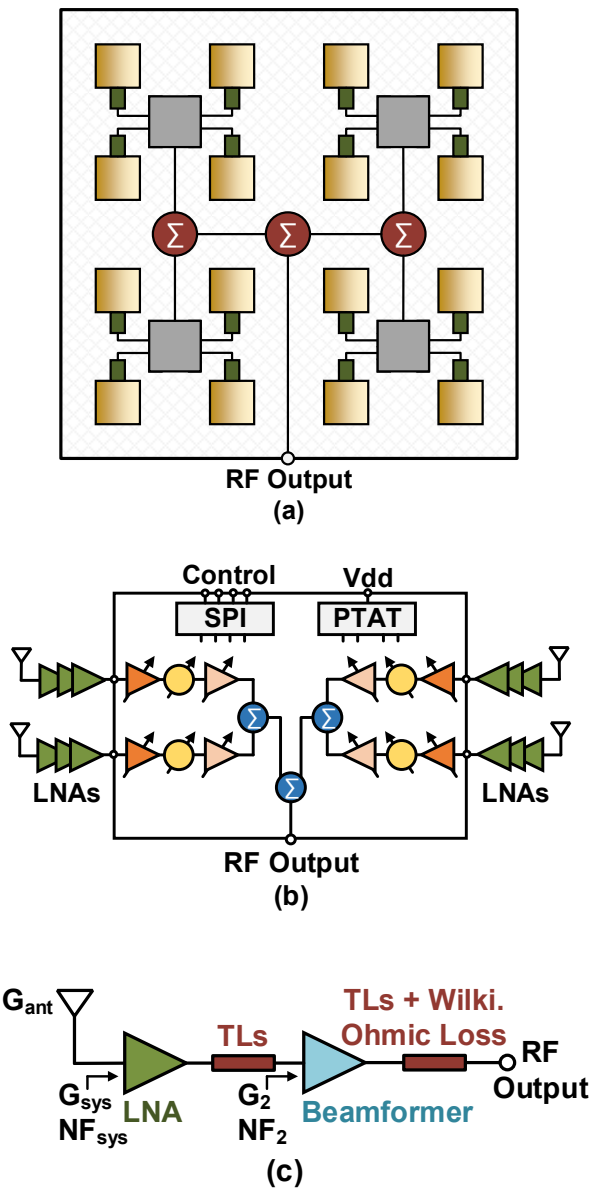


Figure 4.1: Block diagram of (a) 16-element phased-array SATCOM receiver with four quad (4-element) beamformer chips, (b) quad beamformer receiver chip. Both show the external packaged LNAs in green. (c) Array equivalent diagram for sensitivity and gain-to-noise-temperature calculations.

such degradation and to improve the G/T, a packaged LNA is required near each antenna element feed, as shown in Figure 4.1 (a & b).

This chapter aims to demonstrate the designs of packaged LNAs for a K-band SATCOM phased-array receiver using two different technologies: SiGe and CMOS SOI. The chapter is divided into two main sections: Section 4.2 presents a packaged single-ended K-band SiGe LNA with a 2.14 dB noise figure (NF), and section 4.3 presents a 12.5 mW packaged K-band CMOS SOI LNA with 1.5 dB NF before section 4.4 concludes the chapter.

4.2 A Packaged K-Band SiGe LNA with 2.14 dB Noise Figure

4.2.1 SiGe LNA Design

Figure 4.1 presents the proposed LNA. It is based on a three-stage common-emitter topology to achieve a stable packaged amplifier with low noise figure (NF) and high gain (>20 dB). A three-stage design is chosen to achieve noise optimization from the first stage and gain boosting from the second and third stages. The traditional simultaneous noise and power matching method, which is explained in [3], is implemented in the first stage by choosing the transistor size to achieve a real part of the optimum noise source impedance of 50 Ω. Then, a series inductor (L_b) and an emitter degeneration inductor (L_e) are employed so that the optimum noise source resistance and the input impedance coincides at 50 Ω.

4.2.2 SiGe Process Technology

The 14.4 - 21.4 GHz LNA is implemented in the 0.18-µm Jazz SBC18H3 SiGe process. The process provides six aluminum metal layers with a top metal (M6) thickness of 2.8-µm and high-density stacked metal–insulator–metal (MIM) capacitors, shown in Figure 4.3(a). Inductors

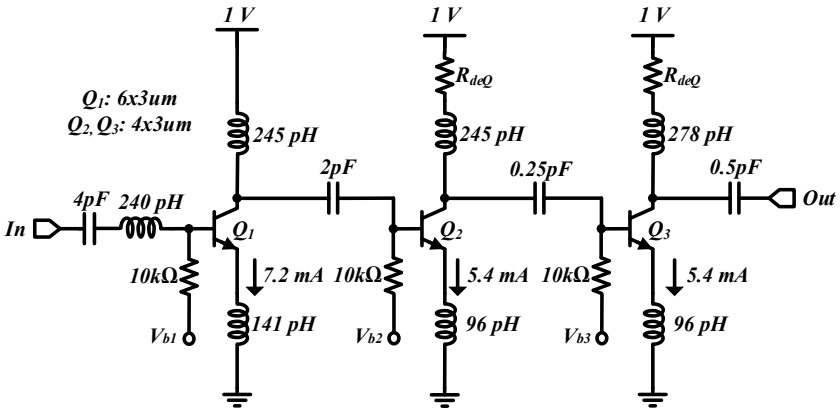


Figure 4.2: Schematic of the 3-stage K-band LNA.

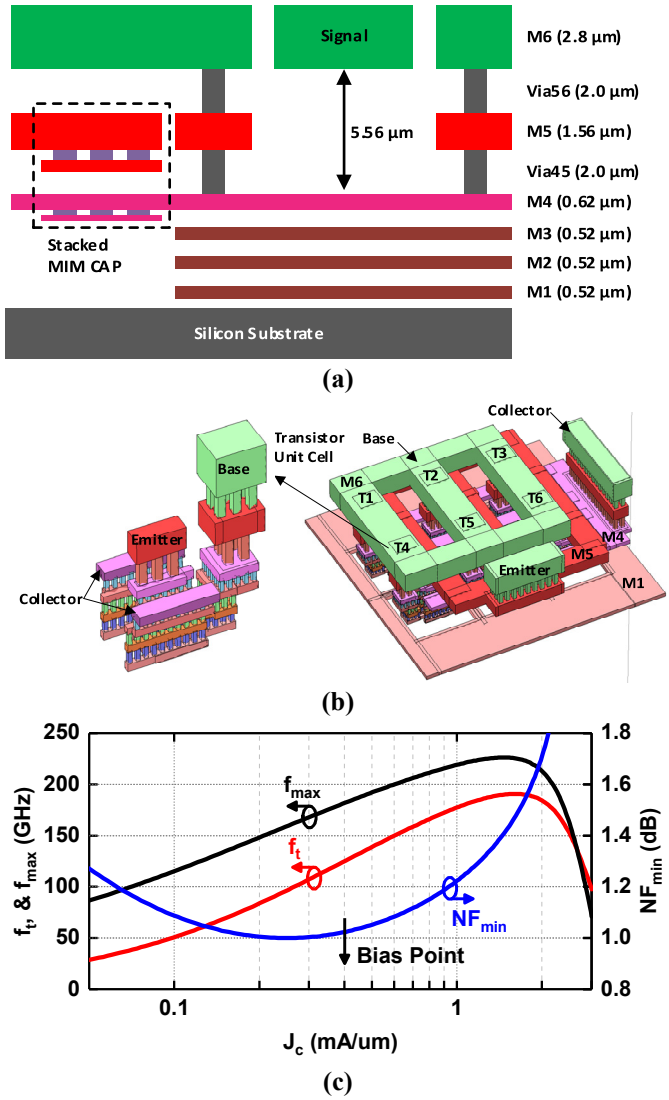


Figure 4.3: (a) Cross section of the Jazz 0.18 µm SBC18H3 SiGe process metal back-end, (b) Layout of a NPN transistor with emitter's width= 0.13 µm, length= 18 µm (6x3µm) up to M6 metal layer, (c) Simulated ft, fmax, and (NFmin at 18 GHz).

and transmission lines (TLs) are implemented using the M6 layer and are simulated using Sonnet (a full-wave EM solver). At 18 GHz, a quality factor of 20 is obtained for a 240-pH inductor that does not have any added ground plane in (M1-M6) layers.

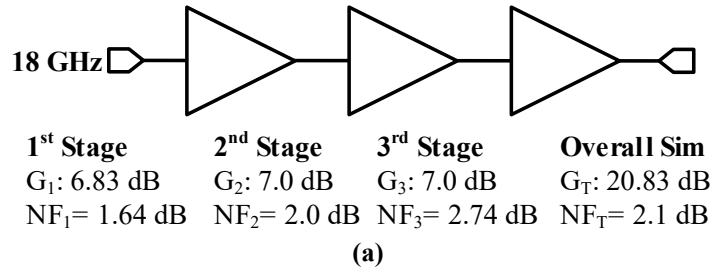
Figure 4.3(b) presents the 3-D layout of an NPN transistor with an emitter width of 0.13-μm and length of 18-μm (6 instances x single transistor length of 3-μm). In this multi-instance layout, M6, M5, and M4 layers are used to route the transistor base, emitter, and collector, respectively, to minimize the parasitic interconnect capacitances between transistors terminals, increase the isolation between the input and output nodes, and reduce the contact resistance in the base terminal.

Figure 4.3(c) presents the simulated f_t, f_{max}, and (NF_{min} at 18 GHz) versus current density (J). They are referenced to the top metal layer of the multi-instance transistor, shown in Figure 4.3(b). The simulated peak f_t and f_{max} are 190 and 225 GHz, respectively. At J = 0.25 mA/μm, the transistor has the lowest NF_{min} with f_t=100 GHz and f_{max}=160 GHz. However, the bias point of the first stage transistor is chosen to be at J=0.4 mA/μm to improve the first-stage gain without significant degradation in its NF.

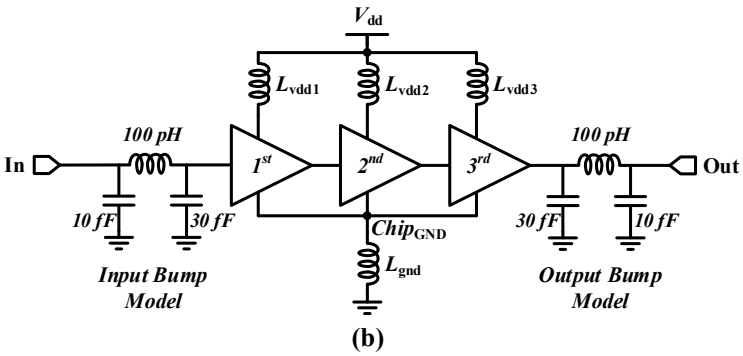
4.2.3 LNA Analysis

An analysis of the gain and noise-figure (at 18 GHz) for a three-stage common emitter design is shown in Figure 4.4(a). This analysis does not consider the RF input and output bump inductances. It shows that a 3-stage gain of 20.8 dB with an NF of 2.1 dB can be achieved.

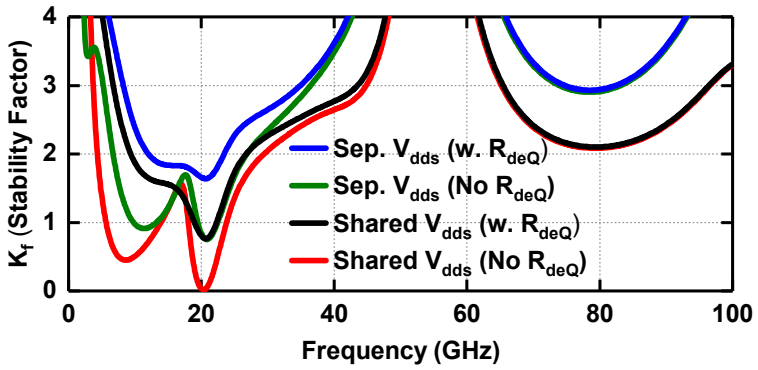
Figure 4.4(b) presents the simulation schematic, which is used to capture the packaging effects on the LNA stability and performance after it is assembled (flip-chip) on the printed circuit board (PCB). L_{vdd1}, L_{vdd2}, L_{vdd3}, and L_{gnd} represent the bump inductance of the V_{DD} and ground bumps, respectively.



(a)



(b)



(c)

Figure 4.4: (a) Simulated gain and noise-figure analysis for the three common emitter stages at 18 GHz, (b) Simulation schematic including the packaging effects on the LNA, (c) Simulated stability factor (K-factor).

The schematic in Figure 4.4(b) is also used to optimize the interstage matching circuits between the common-emitter stages. Due to large C_{bc} and packaging effects, the output load of the first CE stage affects the LNA input impedance and the optimum noise source impedance. Therefore, a simultaneous complex power match between the CE stages and noise figure match is done using optimization to provide an optimum input impedance.

Figure 4.4(c) presents the simulated stability factor (k-factor), which was introduced in [4], for different cases. It shows that the K-band LNA is unconditionally stable ($k > 1$) over the entire frequency range and up to ($L_{vdd1}=L_{vdd2}=L_{vdd3}=L_{gnd}$= 100 pH) when V_{DD} pads are separated on the chip level, and a series 8.6 Ω (R_{deQ} in Figure 4.2) is added to reduce the Q of the collector inductors in the second and third stage. In the other three cases, where V_{DD} pads are shared on the chip level or the added resistors R_{deQ} are removed, the LNA is conditionally stable ($0 < k < 1$).

4.2.4 Fabricated SiGe LNA and Test PCBs

The microphotograph of the K-band LNA is shown in Figure 4.5(a). The chip area is 700x350 μm2, excluding the pads, and 1110 x 610 μm2, including the pads. The chip package employs a CSP process (chip scale package) with bumps spaced at 0.25 mm pitch for both the RF ports (GSG) and the bias ports. The pitch is chosen to be 250-μm to allow the assembly of this LNA on a low-cost PCB of the LNA test board.

The packaged low-noise amplifier is tested using two different PCBs. PCB1, shown in Figure 4.5(b), is used to test the packaged LNA using RF probes (two 400-μm GSG RF probes) landed directly on the PCB. PCB2, shown in Figure 4.7, is used to test a connectorized LNA using two 2.4-mm edge RF female connectors. Both PCBs consist of a 6.6-mil Roger material (RO4350B) attached to a 32-mil FR4 for mechanical stability. The measured loss of the input and output RF transmission lines at 18-GHz is 0.6 dB/cm, while the edge connector has a measured

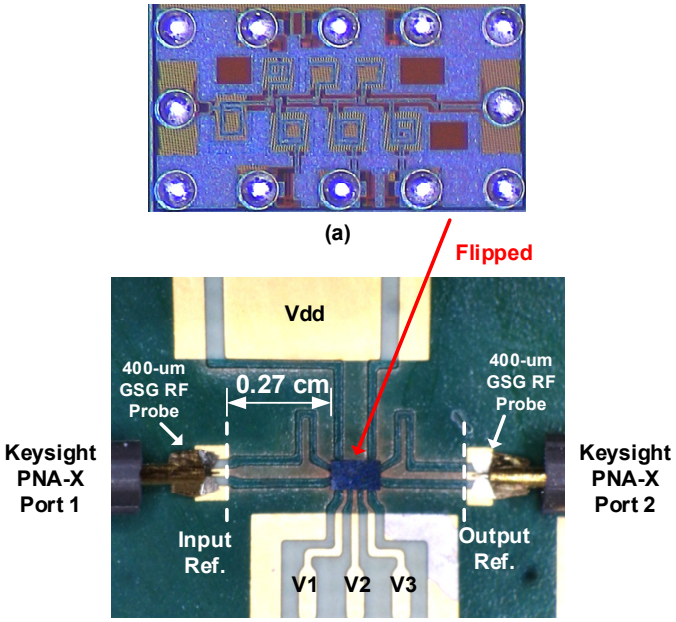


Figure 4.5: (a) Chip microphotograph of the LNA with solder bumps. (b) PCB1 with flip-chip packaging. The LNA is tested using RF probes on the PCB. The additional PCB matching network is used to compensate for the input and output bumps.

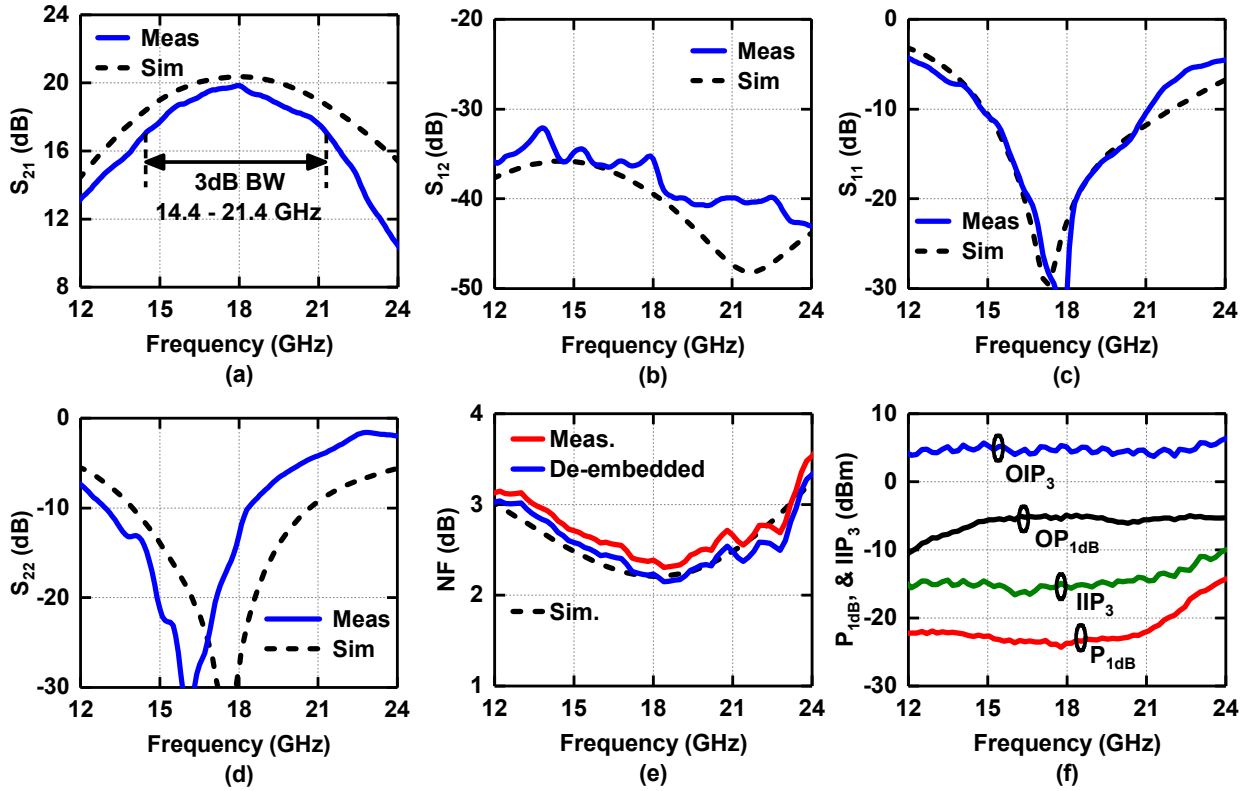


Figure 4.6: Measured and simulated S-parameters: (a) gain (S_{21}), (b) isolation (S_{12}), (c) input return loss (S_{11}), and (d) output return loss (S_{22}). (e) Measured and simulated NF for the 3-stage LNA. (f) Measured P_{1dB}, OP_{1dB}, IIP_3 and OIP_3 for the K-band LNA. All measured results include the ohmic loss of input and output 0.27 cm transmission-line up to the probe tips except the de-embedded results in (e).

insertion loss of 0.15 dB at 18 GHz.

4.2.5 Measurements

The measurement setup consists of a Keysight PNA-X network analyzer (N5247A) and a Keysight p-series power meter (N1912A). This equipment setup is used to measure S-parameters (S_{21}, S_{12}, S_{11}, S_{22}), noise figure (NF), gain compression (input P_{1dB} and O_{P1dB}), and intermodulation distortion (IIP_3 and OIP_3).

Calibration of PCB1 is done up to the probe tips on PCB using a PCB-based Thru, Reflect, Line (TRL) kit. The calibration of PCB2 (three samples) is done up to the two 2.4-mm RF cables using a Keysight electronic calibration module (N4694A). Calibration input and output reference planes for PCB1 and PCB2 are shown in Figure 4.5(b) and Figure 4.7, respectively.

Figure 4.6 (a, b, c, and d) presents the measured and simulated S-parameters of PCB1. The measured S_{21} has a peak gain of 20 dB at 18 GHz with a 3-dB bandwidth of 7 GHz (14.4 - 21.4 GHz). Also, when the input and output transmission-lines on the PCB are de-embedded, the measured peak S_{21} becomes 20.3 dB. The measured S_{11} is < -10 dB at 14.8-21.2 GHz and S_{22} is < -10 dB at 12.9-18.4 GHz. Also, the measured S_{12} is < -32 to -43 dB. The amplifier is unconditionally stable.

The measured and simulated NF of PCB1 LNA is shown in Figure 4.6(e). The measured mean NF is 2.14 dB (when the input 0.27-cm TLs insertion loss of 0.16 dB is de-embedded), and the NF is < 2.3 at (17.1 – 19.7 GHz).

Figure 4.6 (f) presents the 1-dB gain compression and linearity measurement results. The measured input P_{1dB} and OP_{1dB} at 18 GHz are -23.7 and -4.9 dBm, respectively. Also, the measured IIP_3 and OIP_3 at 18 GHz are -15.3 and 5.1 dBm, respectively. Measurements are done with a V_{DD} of 1.0 V and a bias current of 7.2, 5.4, and 5.4 mA, respectively, for the three stages. The total

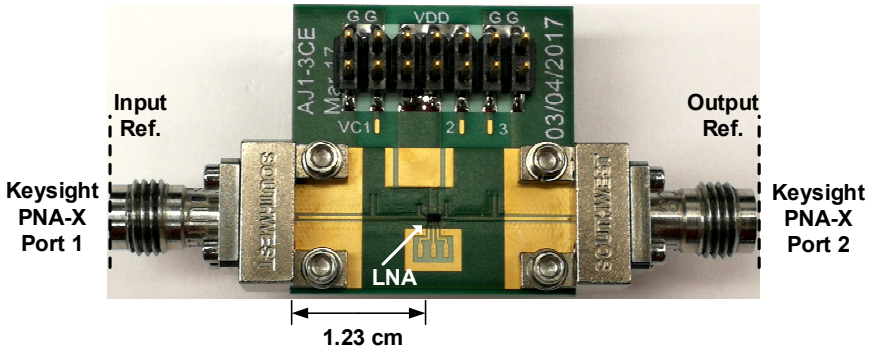


Figure 4.7: PCB2 connectorized three-stage K-band LNA.

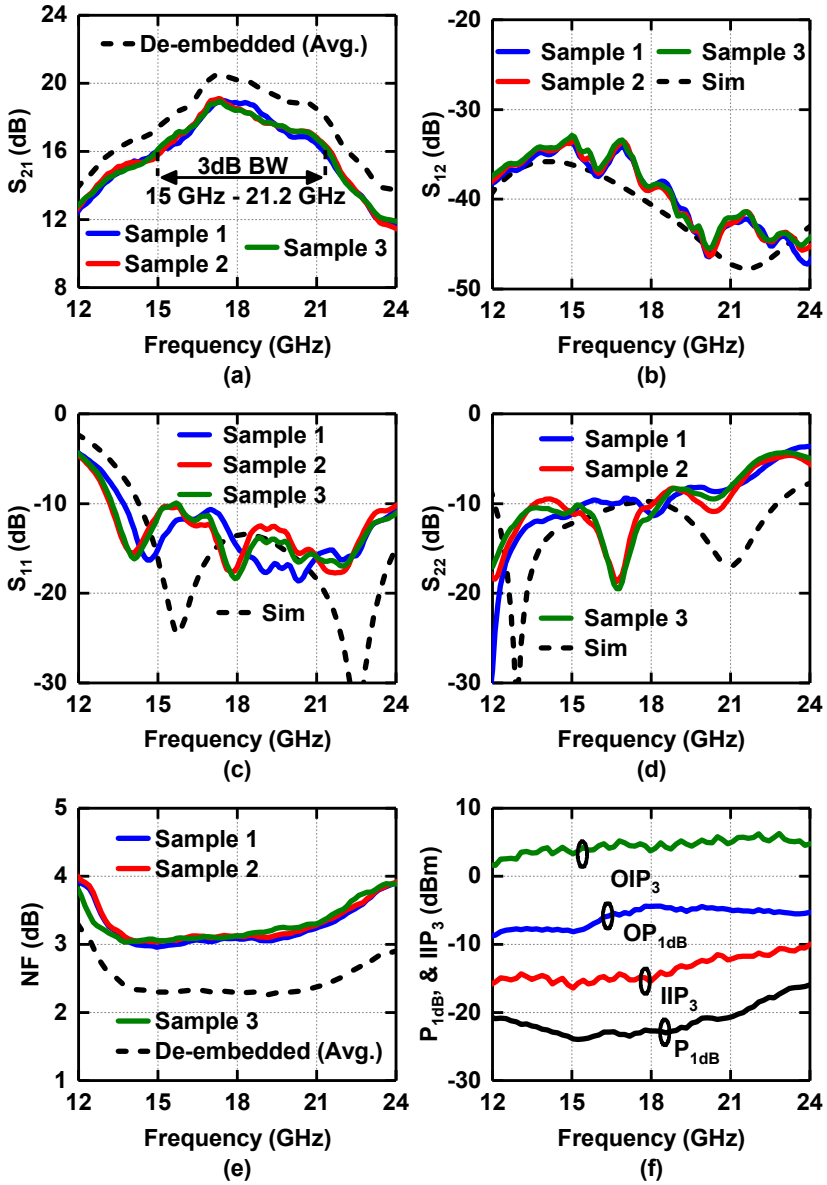


Figure 4.8: Measured and simulated S-parameters: (a) gain (S_{21}), (b) isolation (S_{12}), (c) input return loss (S_{11}), and (d) output return loss (S_{22}). Measured (e) NF, and (f) P_{1dB}, OP_{1dB}, IIP_3 and OIP_3 for the K-band LNA. All measured results include the insertion loss of input and output 1.23-cm TL and the edge RF connectors except for de-embedded results in (a) and (e).

power consumption is 18 mW.

Figure 4.8 presents the measured S-parameters, NF, input $P_{1dB,}$ OP_{1dB}, IIP_3, and OIP_3 for three samples of PCB2 LNA, shown in Figure 4.7. The measured peak S_{21} is 20.5 dB at 17.3 GHz (when TLs and connector losses are de-embedded) with a 3-dB bandwidth of 15-21.2 GHz. The measured NF is 2.3 dB after de-embedding. The small changes in gain and NF are due to the different PCB matching networks in PCB2. It has an additional short stub at the input and output of the LNA for additional ESD protection. The LNA has ESD protection diodes at its RF input and output as well as other bias pads.

4.2.6 Performance Summary and Comparison

Table 4.1 summarizes the measured performance of the packaged three-stage K-band SiGe LNA. The measured S_{21} is 20.3 dB with a 3-dB bandwidth of 7 GHz (14.4 - 21.4 GHz). The measured mean NF is 2.14 dB at 18.4 GHz, and it is < 2.3 at (17.1–19.7 GHz). At 18 GHz, the measured IP_{1dB}, OP_{1dB}, IIP_3, and OIP_3 are -23.7, -4.9, -15.3, and 5.1 dBm, respectively. This is achieved at a power consumption of 18-mW and after using two different PCBs to assemble the packaged LNAs and test their packaged performances.

Also, Table 4.1 compares the measured performance of the packaged three-stage K-band SiGe LNA with other non-packaged published LNAs at similar operating frequencies. It represents state-of-the-art packaged K-band LNAs in terms of gain, noise figure, and power consumption in SiGe and CMOS processes at the time of publication of this work.

Besides, this work demonstrates an unconditionally stable packaged K-band LNA while other published K-band LNAs present on-chip measurements using GSG probes and did not consider the packaging effects on the stability and the impedance matching networks of a multi-stage LNAs.

Table 4.1: Packaged SiGe LNA performance summary and comparison

Reference	Technology	Frequency (GHz)	Power (mW)	Gain (dB)	Mean NF (dB)	IP1dB (dBm)	IIP3 (dBm)	Area (mm2)
This Work	**0.18-µm SiGe process (Jazz SBC18H3)**	**14.4-21.4**	**18[#]**	**20.3**	**2.14**	**-23.7**	**-15.3**	**0.68 (0.25) ***
[5]	0.18-µm SiGe process (Jazz SBC18H3)	16-24	22.5	19	2.2	-16.0	-4.0	0.39
[6]	0.18-µm SiGe process	22.2-26	41	12	3.1	-8.7	-1.8	0.32
[7]	0.18-µm SiGe process	23-32	13	12	4.5	-	-4.5	0.25*
[8]	45 nm CMOS SOI	16-24	32.5	19.5	2.2	-18.5	-8	0.52 (0.15) *
[9]	0.1 µm GaAs pHEMT	18.5-30	27	29	2.1	-	-	2
[10]	0.15 µm InGaP/InGaAs HEMT	23-30	37.5	14.5	1.75	-	-	0.9

[*]Active area (pads are not included)

[#] Bias circuits power is not included

4.3 A 12.5 mW Packaged K-Band CMOS SOI LNA with 1.5 dB Noise Figure

4.3.1 CMOS SOI Process Technology

The 14-22 GHz packaged LNA chip is implemented in GlobalFoundries 45 nm CMOS SOI process. The stack option provides six copper (Cu) metal layers (M1-OB) in addition to a thick, 4.125 um, aluminum (Al) layer, shown in Figure 4.9(a). EMX® (a full-wave EM solver) is used to simulate the inductors and transmission lines (TLs). The simulation results, in Figure 4.10, show that the quality factor (Q) of a 677-pH inductor at 19 GHz is reduced from 25 to 19 when the top Al layer is used instead of the top Cu layer due to the Al higher resistivity. Therefore, the OB metal layer with 3 um thickness is used to implement all inductors and most of the transmission lines (TLs).

The 3-D layout of a first stage NFET transistor is presented in Figure 4.9(b). The transistor width is 100 um (5 instances x 25 fingers x 0.8 um finger width) and has a minimum length of 40 nm. This multi-instance, multi-finger transistor layout with the relaxed pitches and double gate contacts up to M3 is used to reduce the gate resistance and minimized the parasitic capacitances between its terminals. The extracted parasitic performance values of the 1st stage transistor are presented in Figure 4.9(c). The simulated peak f_t and f_{max} are 264 and 197 GHz, respectively. All the amplifier stages are operated at a current density of J = 0.1 mA/μm to achieve low NF and power consumption. At this operating point, f_t and f_{max} are 173 and 165 GHz, respectively.

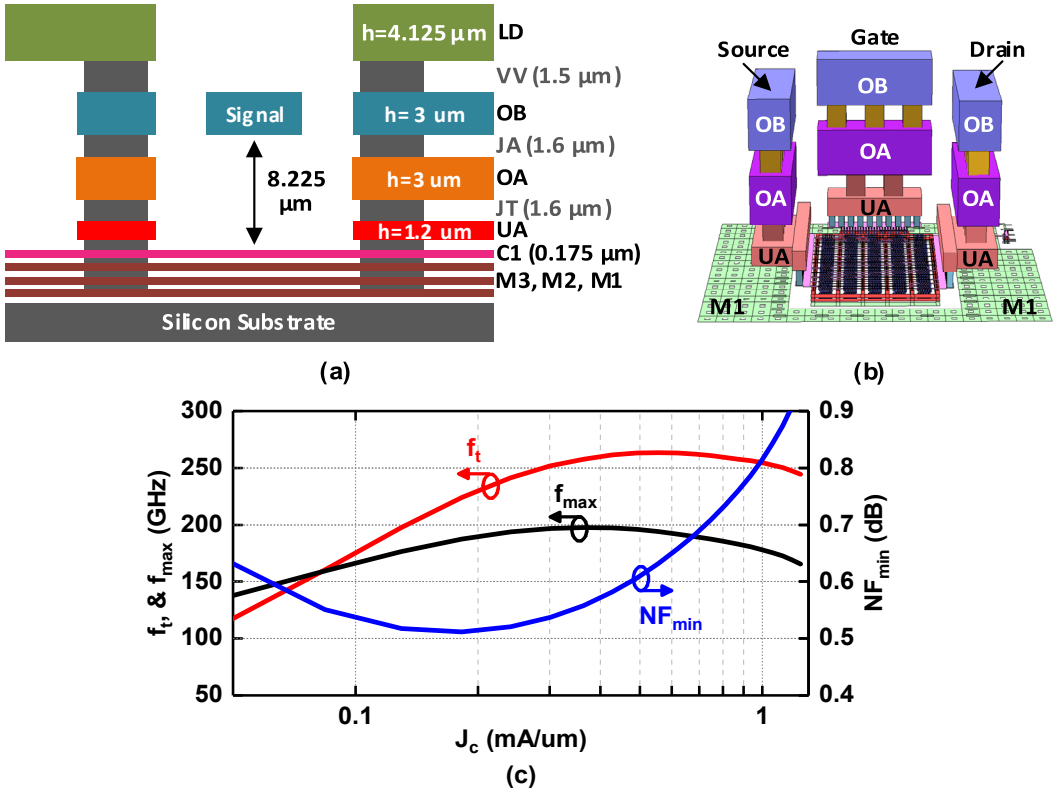


Figure 4.9: (a) Cross section of the GlobalFoundries 45nm CMOS SOI process metal back-end, (b) Layout of a first stage NFET transistor with width= 100 um (5x25x0.8um), and length= 40 nm, (c) Simulated first stage transistor ft, fmax, and (NFmin at 18 GHz) after the parasitic extraction.

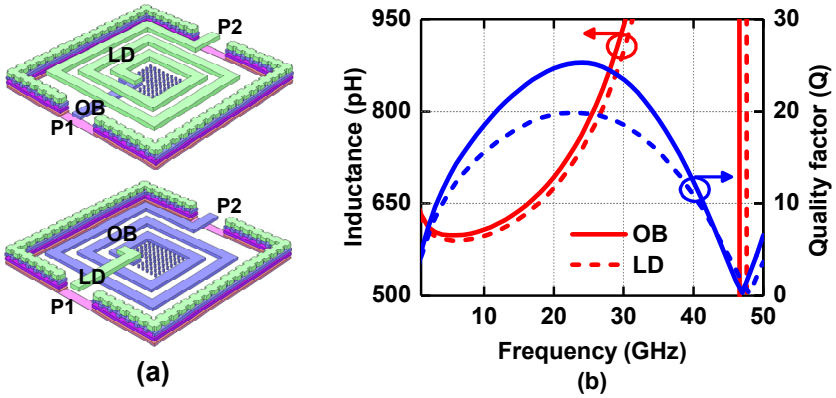


Figure 4.10: First stage gate inductor: (a) layouts, and (b) simulation results, when implemented on OB and LD metal layers.

4.3.2 LNA Design and Packaging Effects

Figure 4.11(a) presents the schematic of the proposed CMOS SOI LNA. A three-stage common-source LNA topology is chosen to provide high gain while preserving a low NF. The LNA is designed using the simultaneous noise and power matching method, discussed in [3]. The 1st stage transistor size is chosen to achieve a real part of the optimum noise source impedance of 50 Ω. Then, to make the optimum noise source resistance and the input impedance occurs simultaneously at 50 Ω, a series gate inductor (L_g) and a source degeneration inductor (L_s) are employed.

Figure 4.12 (a) shows the differences in the simulation schematic of the packaging effects on LNA when it is tested using probes or packaged. L_{input} and L_{output} represent the parasitic inductance of the input and output setup (RF probes and cables). They can be calibrated out and do not affect measurements in both cases. However, the parasitic inductances of bumps between the chip and PCB grounds (L_{gnd}) and Vdds (L_{vdd}) have no effects only when the LNA is tested using probes. If the LNA is packaged, then L_{gnd} is separating the chip and PCB grounds and has effects on the stability and the impedance matching networks of the multi-stage LNA. This is important to take into account when designing the LNA to avoid degrading its performance or even making it unstable when packaged.

Figure 4.12 (b)-Left presents a simple test circuit schematic to illustrate the effects of the ground inductance (L_{gnd}) on the isolation (S_{12}) between two ports. Ideally, the isolation should be infinite when L_{gnd}=0 H; however, Figure 4.12 (b)-Right shows that the S_{12} at 20 GHz can degrade to -32 – -18 dB for L_{gnd} of 10pH – 100 pH, respectively. It is clear that the feedback is higher at higher frequency as S21 at 50 GHz is increased to -25 – -12 dB for L_{gnd} of 10pH – 100 pH, respectively.

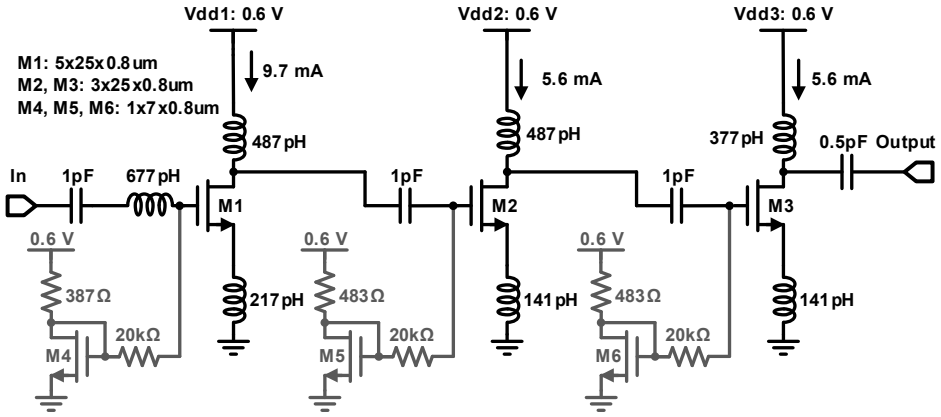


Figure 4.11: The 3-stage CMOS SOI LNA schematic.

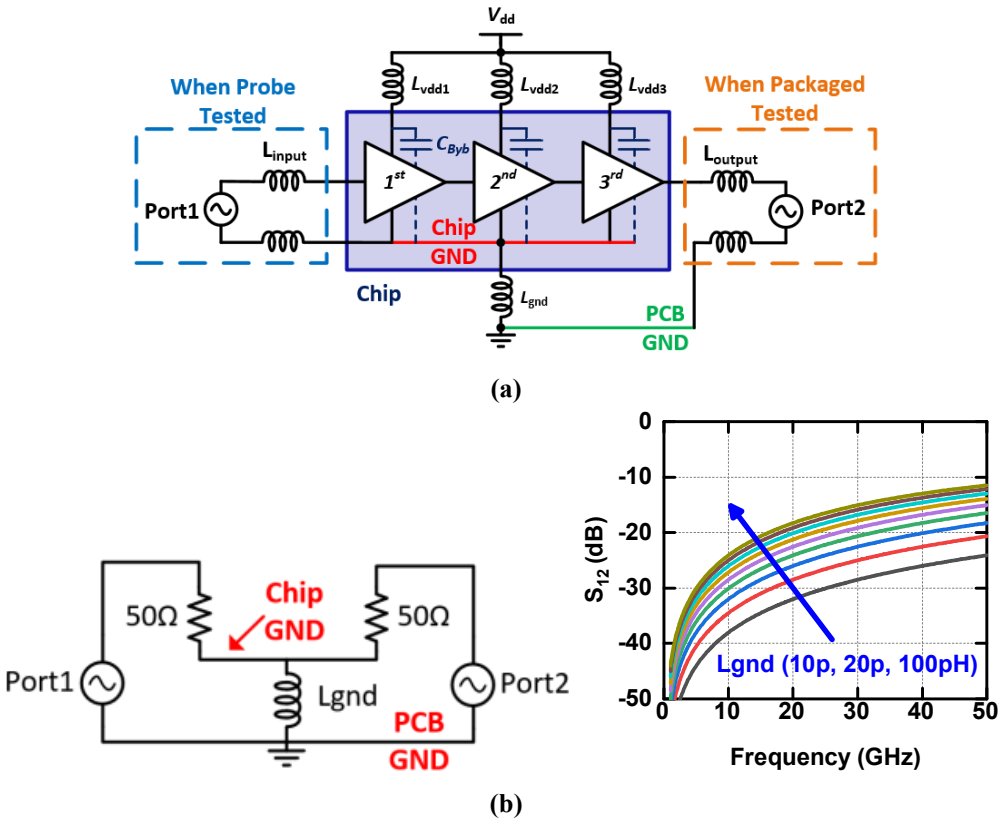


Figure 4.12: (a) The simulation schematic of the LNA showing the packaging effects on probe versus packaged testing. (b) Simulated S_{12} isolation schematic and simulation results versus ground inductance (L_{gnd}).

4.3.2.1 Flip-Chip and Test PCB Stackup

The LNA chips employ a chip-scale-package process (CSP) with C4 bumps spaced at 250 um, the minimum pitch that allows the assembly of those LNA chips on a low-cost phased-array PCB. The C4 bumps (SAC305) consist of 96.5 % tin, 3.0% silver, and 0.5% copper and has an electrical conductivity of 0.96x107 S/m. Figure 4.13 presents how the LNA chip will be flipped on a 12-layers PCB, typical for the phased array, but here only the top used three metal layers are shown. The metal layer (M1) is used to route RF signal and Vdds, M2 for ground, and M3 for bias voltage.

4.3.2.2 Full 3D EM Simulation Model

A full 3D EM simulation model is needed to capture the accurate packaging effects on the LNA performance and avoid any potential instability or detuning. However, this approach is not optimal for the initial design and design iterations because it takes a longer time to set and simulate and requires the complete layout of the chip and PCB.

Figure 4.14 shows the used Full 3D EM simulation model of the chip of the LNA and PCB. The layout of the chip was simplified for the HFSS model to work successfully. The simulated results of this HFSS model are compared with the measured results in section 4.3.4.

4.3.2.3 Simplified Simulation Schematic

Figure 4.15 presents a simplified simulation schematic to capture the packaging effects on the LNA performance after it is assembled on a printed circuit board (PCB). The inductors L_{vdd1}, L_{vdd2}, L_{vdd3}, and L_{gnd} represent the V_{DD} and ground C4 bumps, respectively. The LNA input and output C4 bumps model are extracted from an EM model and was included as part of the matching network at both ports such that there is no need for any additional matching network on the PCB. This simplified simulation schematic is optimal for the initial design and design iterations and its

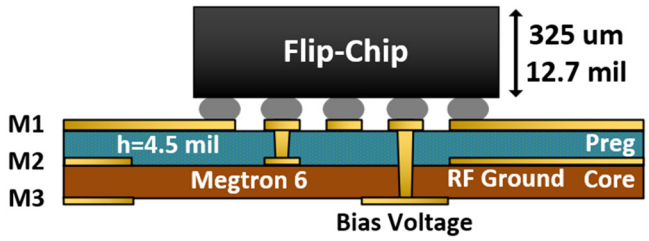
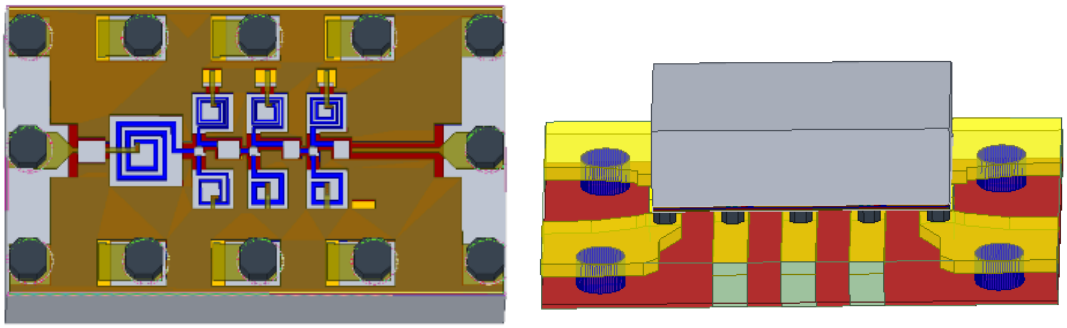


Figure 4.13: Flip-chip and test PCB stackup.



(a) **(b)**

Figure 4.14: Full 3D EM simulation models of (a) LNA, and (b) Flipped-LNA and PCB to capture the packaging effects.

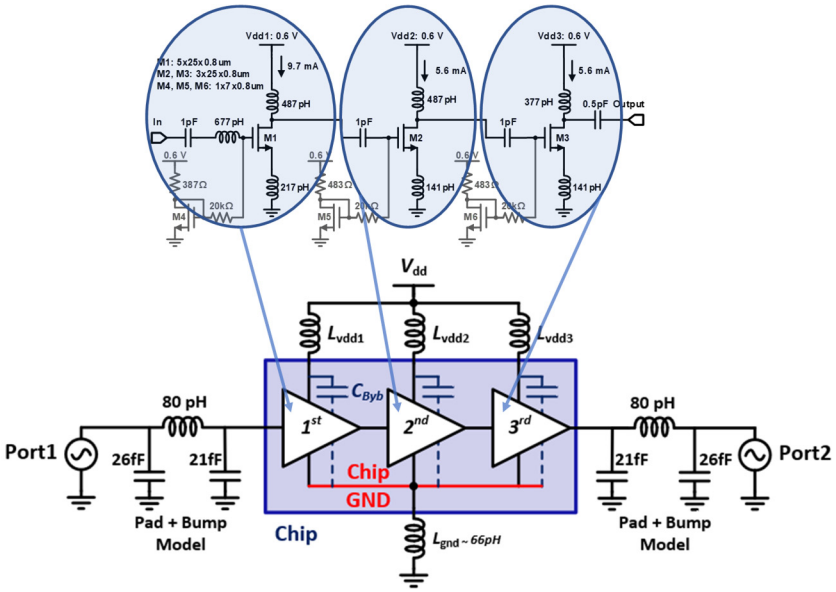


Figure 4.15: The simplified simulation schematic to capture the packaging effects on the LNA performance.

simulated results are compared with the HFSS model in addition to the measurements section.

4.3.3 Realization

The microphotograph of the CMOS SOI LNA with the C4 bumps is presented in Figure 4.16(a). The chip area is 1100 x 640 $um^{2,}$ including the pads, and 600 x 260 um^2, when the pads are excluded.

The LNA is tested using two different PCBs. The first PCB, Figure 4.17(a), tests the assembled LNAs using RF probes landed directly on the PCB. The second PCB, Figure 4.18, tests the packaged LNA with two 2.4-mm edge RF female connectors.

4.3.4 Measurements

A Keysight PNA-X network analyzer (N5247B) and a Keysight EPM series power meter (N1913A) are used to perform all the measurements of the S-parameters, noise figure, gain compression, and intermodulation distortion. The calibration reference planes in PCB1 and PCB2 are shown in Figure 4.17(a) and Figure 4.18, respectively. The calibration for PCB1 was done using a PCB-based Thru, Reflect, Line (TRL) kit, while the calibration of PCB2 used a Keysight electronic calibration module (N4694A).

The measured and simulated results of LNA on PCB1 are presented in Figure 4.17. The measured peak gain is 23.1 dB, and it occurs at 17.9 GHz with a 3-dB BW of 8.6 GHz (13.6 – 22.2 GHz), and %48 fractional BW. The measured S_{11} is < -10 dB at (16.8 – 22.0 GHz), and the S_{12} is < -30 dB. At 18 GHz, the measured NF is 1.6 dB, and the measured IP_{1dB}, and IIP_3, are -21.9, and -12 dBm, respectively.

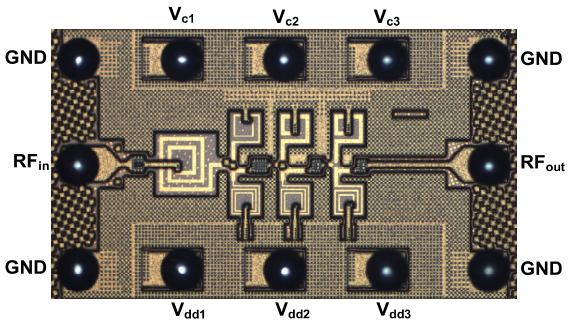


Figure 4.16: The 3-stage CMOS SOI LNA microphotograph with the C4 bumps.

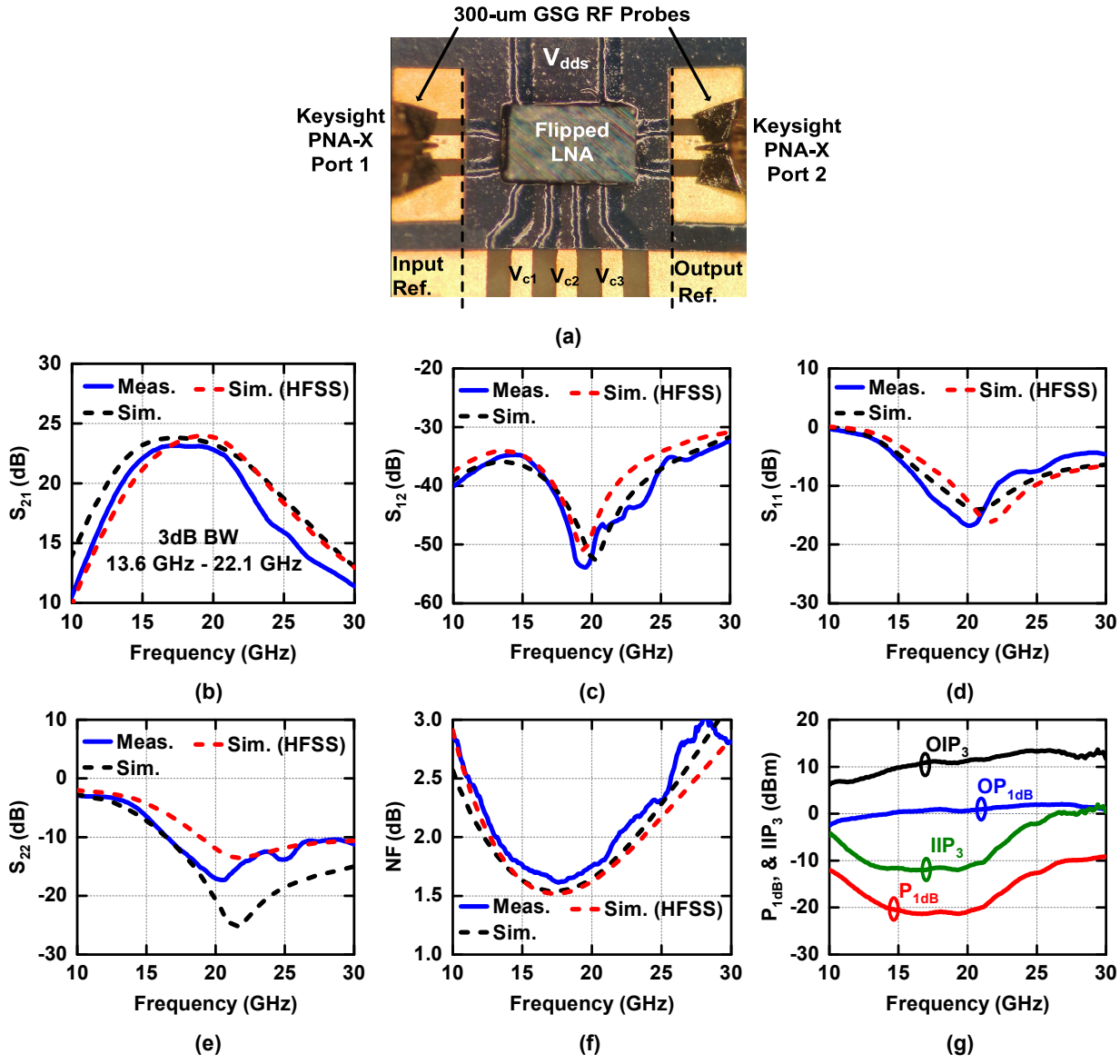


Figure 4.17: (a) Test PCB1 with a flip-chip assembled CMOS SOI LNA. Measured and simulated: (b) gain (S_{21}), (c) isolation (S_{12}), (d) S_{11}, (e) S_{22}, and (f) NF. (g) Measured IP_{1dB}, OP_{1dB}, IIP_3 and OIP_3. The ohmic loss of PCB1 input and output TLs are de-embedded from measured results in (b), and (f) up to the C4 bumps' pads.

Additionally, the measured and simulated results of the connectorized LNA on PCB2 are presented in Figure 4.19. The measured peak gain is 23.1 dB and occurs at 17.4 GHz with a 3-dB BW of 8.1 GHz (13.9 – 22.0 GHz). The measured S_{11} is < -10 dB at (16.2 – 24.0 GHz), and the S_{12} is < -30 dB. The measured NF is 1.5 dB at (15.7 – 17.2 GHz), and it is <1.7 dB at (13.9 – 20.9 GHz). At 18 GHz, the measured IP_{1dB}, OP_{1dB}, IIP_3, and OIP_3 are -21.6, 0.3, -12, and 10.9 dBm, respectively.

There is a small difference (~0.1 dB) between the measured NF of PCB1 and PCB2 after de-embedding the ohmic loss of the TLs. This difference is due to the different calibrations between PCB1 and PCB2.

All previous measurements are done with a voltage supply of 0.6 V and bias currents of 9.6, 5.6, and 5.6 mA, for the LNA three stages, respectively. So, the total power consumption is 12.5 mW. Figure 4.20 presents the measured LNA's power consumption when the applied voltage supply is changed from 0.2 V to 1.2V. At 18 GHz, when the power consumption is increased to 21.6 mW, the measured gain increases to 24.4 dB, and the measured NF reduces to 1.38 dB, while the OP_{1dB} increases to 3.3 dBm.

4.3.5 Performance Summary and Comparison

Table 4.2 summarizes the measured performance of the packaged three-stage K-band CMOS SOI LNA. The CMOS SOI LNA has a measured peak gain of 23.1 dB at 17.4 GHz with a 3-dB bandwidth (BW) of 8.1 GHz (13.9 – 22.0 GHz). The measured NF is 1.5 dB at (15.7 – 17.2 GHz) and it is < 1.7 dB at (13.9 – 20.9 GHz). At 18 GHz, the measured IP1dB and IIP3 are -21.6 and -12 dBm, respectively. The CMOS LNA achieved this high gain and low NF with a power consumption of 12.5 mW. At 18 GHz, when the power consumption is increased to 21.6 mW, the measured gain is 24.4 dB, and the measured NF is 1.38 dB.

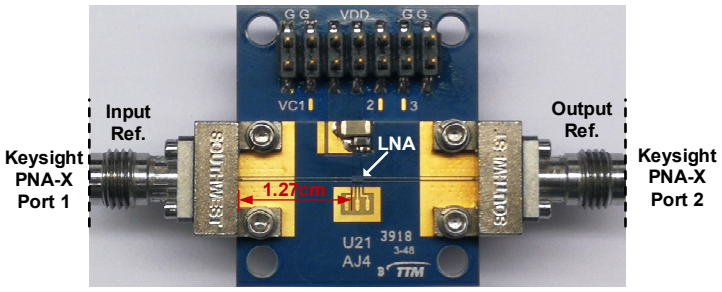


Figure 4.18: Test PCB2 with the assembled CMOS LNA. This connectorized LNA is tested using two 2.40 mm end launch connectors.

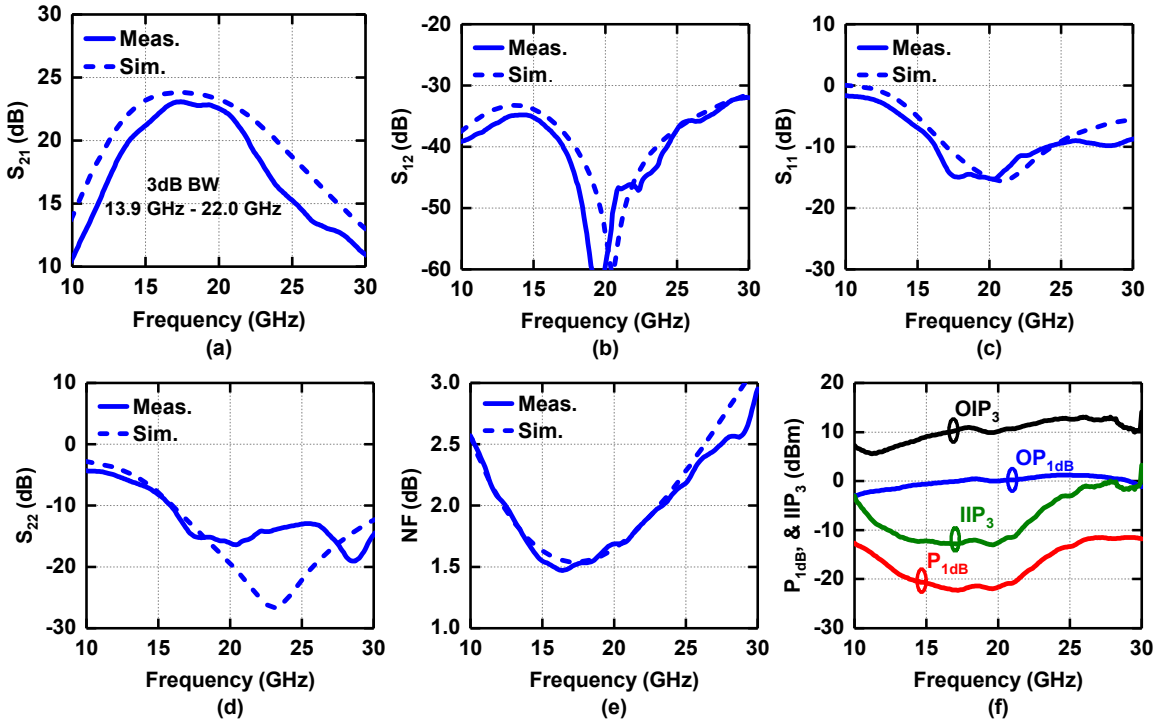


Figure 4.19: Measured and simulated: (a) gain (S_{21}), (b) isolation (S_{12}), (c) S_{11},(d) S_{22}, and (e) NF. (f) Measured IP_{1dB}, OP_{1dB}, IIP_3 and OIP_3. The ohmic loss of PCB2 input and output 1.27-cm TLs and the edge RF connectors are de-embedded from measured results in (a), (b), (e) and (f).

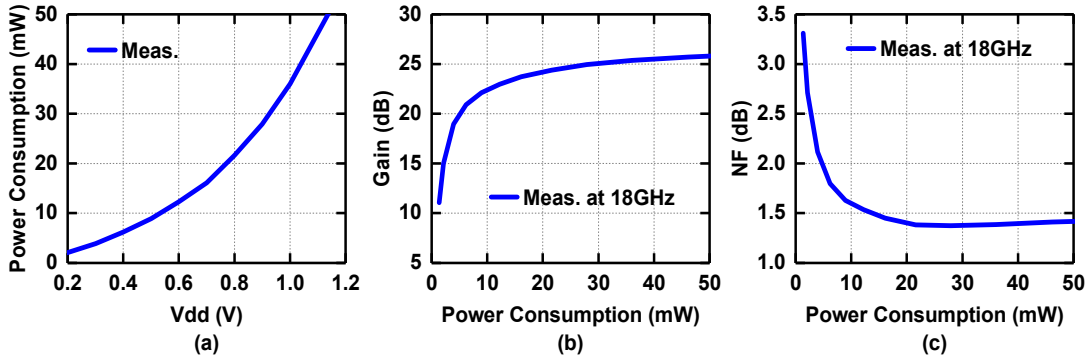


Figure 4.20: (a) Measured LNA's power consumptions versus applied voltage supply. Measured (b) gain, and (c) NF at 18 GHz versus LNA's power consumption. The ohmic loss of PCB2 input and output 1.27-cm TLs and the edge RF connectors on are de-embedded in (b), and (c).

Also, Table 4.2 compares this packaged CMOS SOI K-band LNA with other packaged and non-packaged recent works at similar operating frequencies. This work demonstrates the highest gain, with the lowest NF, and power consumption when compared to published packaged and non-packaged K-Band LNAs in SiGe and CMOS processes. Also, it demonstrates the highest fractional bandwidth (FBW) of 45% and is calculated using:

$$FBW = \left(\frac{BW}{f_c}\right) \times 100 \tag{4.1}$$

where BW is the 3-dB bandwidth in GHz, and f_c is the center of the 3-dB bandwidth in GHz too. Moreover, this CMOS SOI LNA demonstrates the highest figure of merit (FOM) of 27 dB and is calculated using:

$$FOM = 20 \times log_{10}\left(\frac{Gain_{lin} \times BW_{GHz}}{(F-1) \times P_{dc(mW)}}\right) \tag{4.2}$$

where $Gain_{lin}$ is the linear gain, BW_{GHz} is the 3-dB bandwidth in GHz, F is the linear noise figure, and $P_{dc(mW)}$ is the DC power consumption. The CMOS LNA NF is comparable to the latest GaAs LNA, in [17], which achieved an NF of 1.25 dB but with a power consumption of 212 mW (compared to 12.5 mW).

Besides, the other published K-band LNAs in Table 4.2, except the SiGe LNA from section 4.2 in [16], present on-chip measurements using GSG probes and did not consider the packaging effects on the stability and the impedance matching networks of a multi-stage LNAs.

4.4 Conclusion

This chapter presented a packaged single-ended K-band SiGe LNA that was demonstrated in a 0.18-µm SiGe BiCMOS process technology with a state-of-the-art NF value. The measured peak gain is 20.3 dB at 18 GHz with a mean NF of 2.14 dB, and power consumption of 18 mW.

Table 4.2: Packaged CMOS SOI LNA performance summary and comparison

Reference	Technology	Frequency [GHz]	FBW [%]	Power [mW]	Gain [dB]	NF [dB]	IP_{1dB} [dBm]	IIP_3 [dBm]	Area [mm^2]	FOM [dB]
This Work CMOS LNA	**45 nm CMOS SOI**	**13.9 - 22.0**	**45**	**12.5**	**23.1**	**1.5**	**-21.6**	**-12**	**0.70 (0.16) ***	**27.0**
[11] TMTT 2020	65 nm CMOS	24.4 – 32.3	28	22	24.4	4	-23	-	(0.12) *	11.9
[12] MWCL 2020	65 nm CMOS	21.2 – 24.0	11	0.99	19.1	3.6	-31	-	0.35	25.9
[13] JSSC 2020	65 nm CMOS	17.2 – 22.0	24	1.9	14.9	3.3	-	-	0.42	21.8
[14] RFIC 2019	65 nm CMOS	24.9 – 32.5	26	20.5	18.3	3.2	-24	-	0.38 (0.11) *	8.9
[15] IMS 2018	45 nm CMOS SOI	23.0 – 30.0	26	15	12.8	1.4	-	5	0.30	14.6
[8] CSICS 2013	45 nm CMOS SOI	16.0 – 24.0	40	32.5	19.5	2.0	-18.5	-8	0.52 (0.15) *	12.0
[16] SiGe LNA BCICTS 2018	**130 nm SiGe Bi-CMOS**	**14.4 – 21.4**	**39**	**18**	**20.3**	**2.14**	**-23.7**	**-15.3**	**0.68 (0.25) ***	**16.0**
[17] IMS 2017	150 nm E-Mode GaAs pHEMT	14.0 – 31.0	76	212	30	1.25	-11.5	-1.5	1.87	17.6

*Active area (pads are not included)

Two different PCBs were used to assemble the packaged LNAs and test their performances. It represents state-of-the-art packaged K-band LNAs in terms of gain, NF, and power consumption in SiGe and CMOS processes at the time of publication of this work.

Also, in this chapter, a packaged K-Band CMOS LNA was demonstrated in a 45 nm CMOS SOI process technology with state-of-the-art performance. At a power consumption of 12.5 mW, it achieved a gain of 23.1 dB at 17.3 GHz with a 45% fractional BW and NF of 1.5 dB at (15.7 – 17.2 GHz). This CMOS LNA achieved a comparable noise performance to the latest GaAs LNA at a small fraction of GaAs LNA's needed power and area. This work shows that CMOS SOI is an excellent alternative to other technologies as it can be used to build very low noise front ends. Additionally, this chapter also shows that a simplified simulation schematic can be used to provide an accurate representation of the packaging effects in a less short time than the full 3D EM simulation model.

4.5 Acknowledgment

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Chapter 4, in part, is a reprint of the material as it appears in: A. H. Aljuhani, T. Kanar, and G. M. Rebeiz, "A Packaged Single-Ended K-Band SiGe LNA with 2.14 dB Mean Noise Figure," *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, San Diego, CA, 2018, pp. 198-201. The dissertation author was the primary investigator and author of this paper.

Chapter 4, in part, is also a reprint of the material as it appears in: A. H. Aljuhani and G. M. Rebeiz, "A 12.5 mW Packaged K-Band CMOS SOI LNA with 1.5 dB NF," *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 156-159. The dissertation author was the primary investigator and author of this paper.

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Chapter 5

Ultra-Low-Power Low-Noise K-band Phased-Array Receive Beamformer Channel with a Novel High-Resolution Phase Shifter and Low Phase Imbalance Attenuators for K-band SATCOM Applications

5.1 Introduction

The increasing demands for higher data rates and persistent connectivity over large geographic areas, along with the endless growing amount of data usage, have encouraged the recent advancements in deploying small communication satellites and also the massive investments in the satellite-based internet services. Such services are essential to meet the data demands and provide online access to users in rural areas. Comparing to geostationary equatorial orbit (GEO) satellites, the medium earth orbit (MEO) and low earth orbit (LEO) satellites provide higher data transmission speed with lower latency. However, user (ground) terminals with tracking capabilities are needed to maintain the link with MEO and LEO satellites even for fixed-location users.

SATCOM phased arrays with full electronic beam steering are potential candidate for the ground terminals with tracking capabilities. They are preferred instead of mechanically-steerable antennas due to their advantages such as lower profile, lightweight, and the absence of maintenance due to non-moving parts. One of the essential components in the construction of large-scale phased-arrays for satellite communications is the silicon beamformer chip, as demonstrated in the past few years [1-7].

This chapter focuses on the development of an ultra-low-power low-noise K-band phased array receive beamformer channel using the 45 nm RF CMOS SOI process. Section 5.2 presents the design considerations, including the system of the phased-array beamformer chip, its targeted specifications, and process technology. Section 5.3 presents the channel's main building blocks, and section 5.4 presents the calibration and measurements of a novel passive VM. 5.5 discusses the design and measurements of the entire channel. Then, section 5.6 summarizes and compares the performance with prior work before section 5.7 concludes the chapter.

5.2 Design Considerations

5.2.1 System and Specifications

Figure 5.1 presents the block diagram of a K-band dual-polarized receive phased-array beamformer chip. It consists of eight channels (four for vertical polarization and four for horizontal polarization). This dual-polarized architecture with dual output ports is chosen to allow for two independent receive beams. The beamformer channel mainly consists of a low noise amplifier, followed by a passive vector modulator, then a variable gain amplifier. There are two added amplification stages to compensate for the insertion loss of the passive vector modulator and passive gain control using resistive attenuators.

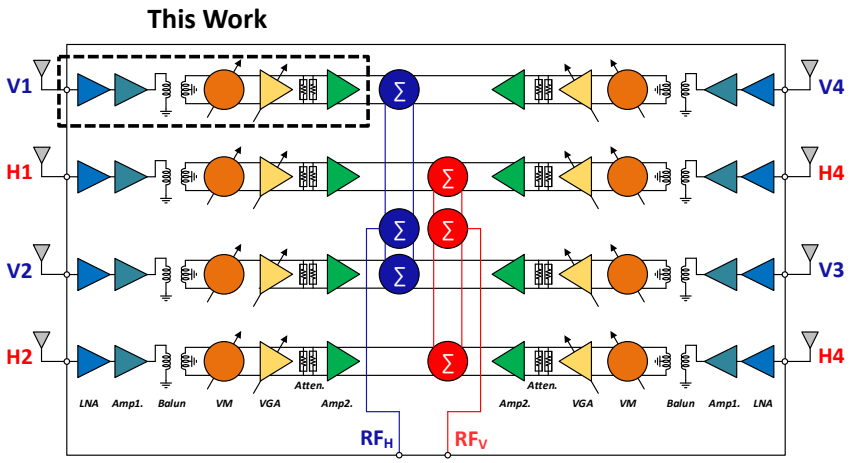


Figure 5.1: Block diagram of a K-band dual-polarized receive phased-array beamformer chip.

Table 5.1: Targeted specifications summary

Parameter	Unit	Value
Frequency	GHz	17.2 – 20.2
Polarization	-	Dual (V-Pol and H-Pol)
Elements per chip	-	8
Gain	dB	≥ 20
NF	dB	< 2.5
Gain Control Range	dB	≥ 30
Gain Step	dB	≤ 0.5
Phase shifter	bits	8
Phase step	degree	1.4
RMS phase/gain errors	°/dB	<1.4°/<0.2 dB
Power dissipation/element	mW	≤ 50 mW

Table 5.1 summarizes the targeted specification of the K-band beamformer channel. The channel gain should be higher than 20 dB to compensate for the ohmic loss of the Wilkinson combining network (on-chip and on the printed circuit board) and minimize the noise contribution of the successive downconverter stage. The phased array size (and consequently its cost) is determined the required gain-to-noise-temperature (G/T). Therefore, the noise figure of the channel should be less than 2.5 dB for the best performance. Also, high phase shifter and gain control resolution is needed to achieve low sidelobes levels and high cross-polarization purity.

5.2.2 Technology

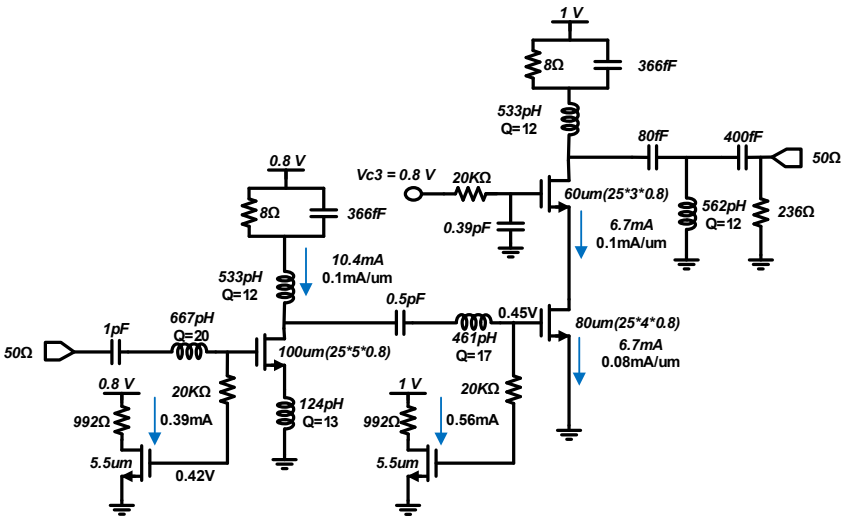
The K-band dual-polarized receive phased-array beamformer channel, and all the single blocks presented in this chapter are implemented in the GF 45 nm CMOS SOI process. The stack option provides six copper (Cu) metal layers (M1-OB) in addition to a thick, 4.125 um, aluminum (Al) layer. More information about this technology was shown in section 4.3.1.

5.3 Building Blocks

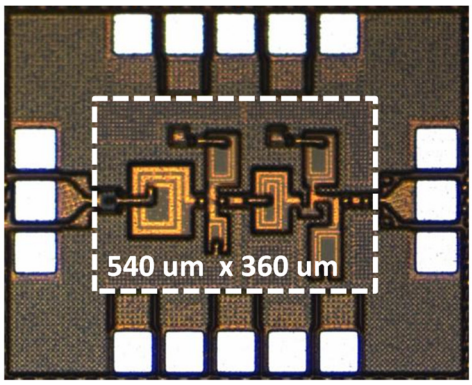
5.3.1 Low Noise Amplifier

Figure 5.2 (a) presents the proposed LNA for the K-band receive phased-array beamformer channel. It is was implemented using a two-stage topology, one common source (CS) stage followed by a cascode stage. This structure is used to achieve noise optimization from the first stage and gain boosting and gain control from the second stage. Both stages are biased at ~0.1 mA/μm to maintain low NF and low power consumption. Also, the traditional simultaneous noise and power matching method is implemented in both stages. The output matching network consists of a two-stage LC network to improve the output return loss (S_{22}) bandwidth. The microphotograph of the K-band two-stage LNA is shown in Figure 5.2 (b), and the chip area is 540 x 360 $\mu m^{2,}$ excluding the pads, and 880 x 700 μm^2 when the pads are included.

Figure 5.3 (a) presents the measured and simulated S-parameters of six stand-alone LNA samples. The measured S_{21} has a peak gain of 18.3 dB at 18.3 GHz with a 3-dB bandwidth of 9 GHz (14 – 23 GHz). The measured S_{11} is < -10 dB at 14.4 – 22.5 GHz, S_{22} is < -10 dB at 13.9 – 24.1 GHz, S_{12} is < -38 dB. Also, the measured and simulated NF is presented in Figure 5.3 (b), and it is 1.6 dB at 18 GHz and < 1.7 dB at 15 – 21.5 GHz. Moreover, Figure 5.3 (c) presents the 1-dB gain compression and linearity measurement results. At 18 GHz, the measured input



(a)



(b)

Figure 5.2: (a) Schematic and (b) microphotograph of a standalone LNA, the first block in the channel of the K-band dual-polarized receive phased-array beamformer chip.

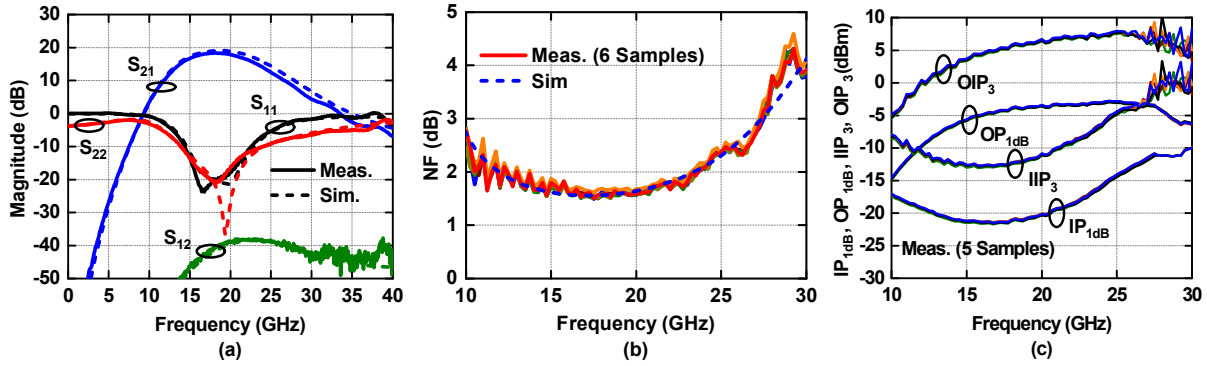


Figure 5.3: Measured and simulated (a) S-parameters, and (b) NF of 6 standalone LNA samples. (c) Measured P_{1dB}, OP_{1dB}, IIP_3 and OIP_3.

Table 5.2: Comparison of with published LNAs using 45 nm CMOS SOI technology

Reference	Frequency [GHz]	FBW [%]	Power [mW]	Gain [dB]	NF [dB]	IP1dB [dBm]	IIP3 [dBm]	FOM [dB]
This work Standalone LNA	**14.0 – 23.0**	**49**	**15.8**	**18.2**	**1.6**	**-21**	**-12.4**	**20.3**
[8] IMS 2019	13.9 - 22.0	45	12.5	23.1	1.5	-21.6	-12	27.0
[9] IMS 2018	23.0 – 30.0	26	15	12.8	1.4	-	5	14.6
[10] CSICS 2013	16.0 – 24.0	40	32.5	19.5	2.0	-18.5	-8	12.0

P1dB and OP1dB at 18 GHz are -21.2 and -4.0 dBm, respectively. Also, the measured IIP3 and OIP3 at 18 GHz are -12.7 and 5.2 dBm, respectively.

Table 5.1 compares the measured performance of the stand-alone LNA with other published LNAs using 45 nm CMOS SOI technology. It has the highest fractional bandwidth and the second-highest figure of merit. Over [8], this LNA has the advantage of adding gain control with minimum effect on the input and output return losses using current steering in the cascode stage.

5.3.2 K-band Wideband Balun

Two wideband baluns are needed for the K-band channel. The first one is used before the differential phase shifter, while the second one is added only for measurement purposes. Figure 5.4 presents the schematic and microphotograph of two back-to-back tuned transformer baluns. The core area of one balun is 230 x 360 um^2.

Figure 5.5 presents the measure and simulated of the stand-alone K-band wideband balun. At 19 GHz, the measured insertion loss is 2.5 dB with a 1 dB bandwidth of 13.1 GHz (11.8 – 24.9 GHz). The measured S_{11} is < -8 dB at 14.1 – 20.6 GHz, S_{22} is < -10 dB at 13.9 – 20.6 GHz

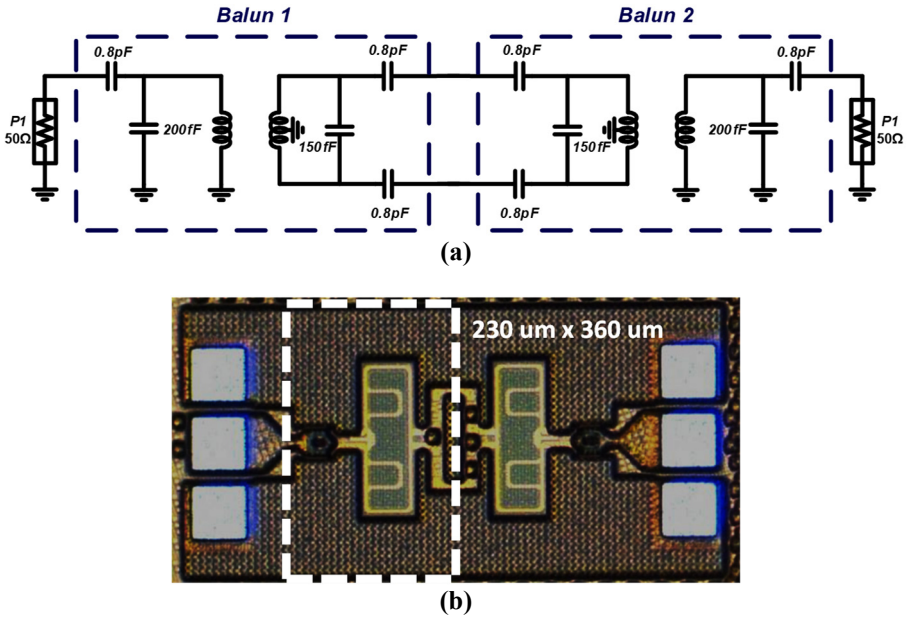


Figure 5.4: (a) Schematic and (b) microphotograph of a standalone K-band wideband balun.

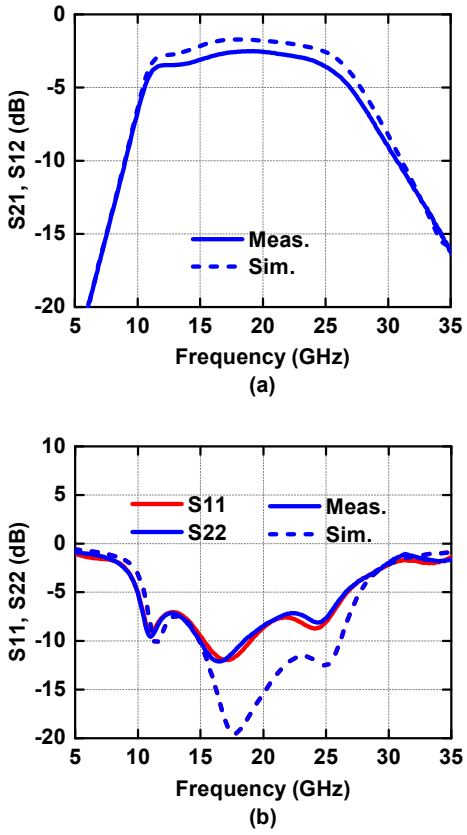


Figure 5.5: Measured and simulated (a) insertion loss (S_{12}, S_{21}), and (b) input and output return losses (S_{11},S_{22}) of the standalone K-band wideband balun.

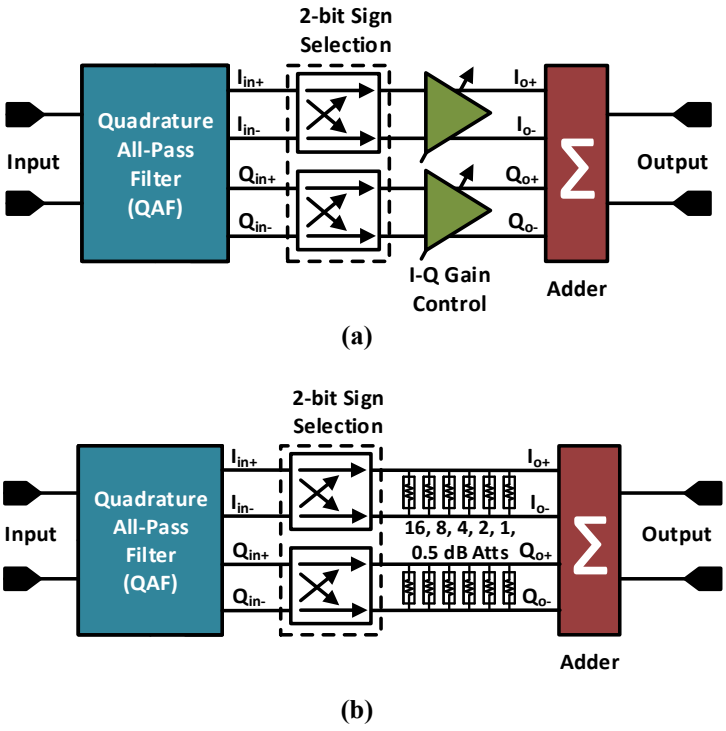


Figure 5.6: Block diagrams of (a) typical active and (b) proposed passive vector modulators.

5.3.3 K-Band 8-Bit Passive Phase Shifter

The phase shifter is based on I- and Q-vector signals modulator (VM). Figure 5.6 (a) presents a typical block diagram of the active VM. The first block is a quadrature all-pass filter (QAF), and it is used to generate quadrature phased I- and Q-vector signals from the input differential signal. Then, two switches are used to set the needed polarities of the I- and Q- signals before adding them with the required amplitude wight to give the interpolated differential output signal [11]. The phase and magnitude of the output signal are given by:

$$Phase = tan^{-1}\left(\frac{Q_{\pm}}{I_{\pm}}\right) \tag{5.1}$$

$$\text{Magnitude} = \sqrt{{Q_{\pm}}^2 + {I_{\pm}}^2} \tag{5.2}$$

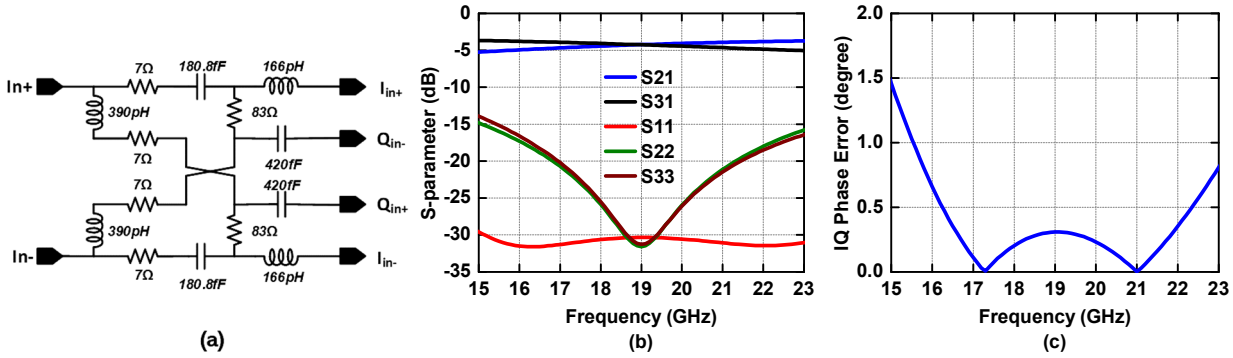


Figure 5.7: (a) Differential IQ generator schematic. Simulated (b) S-parameters and (c) IQ phase error. Port 1 (In_+, In_-), Port 2 (Q_{in+}, Q_{in-}), and Port 3 (I_{in+}, I_{in-}).

Smaller area, ease to reconfigure, wideband performance, better NF, and low insertion loss or gain are among the advantages of implementing the phase shifter using an active VM when compared to reflection or switched-line/filter phase shifters [12].

A novel phase shifter based on a passive VM is shown in Figure 5.6 (a). The two variable gain amplifiers and active differential adder are replaced by two differential switched π-type 8-bit attenuators followed by a differential transformer-based Wilkinson power combiner. The proposed structure maintains the advantages of a small area, wideband performance, ease of configuration, and tuning in addition to the advantage of high linearity and bidirectional functionally. The only drawbacks are higher insertion loss and NF. However, at the cost of less than half of the needed power for the two VGAs in the typical VM, an amplification stage can be added before the VM to reduce the insertion loss and improve the NF to a comparable level.

5.3.4 Differential IQ Generator

The differential IQ signals are generated using the QAF based on the L-C resonance developed in [11]. Figure 5.1 (a) presents the K-Band QAF schematic. It has a simulated insertion loss of 4.3 dB at 19 GHz, an amplitude error < 1 dB at 16.3 – 21.9 GHz, and a phase error <0.4°at 16.4 – 22.2 GHz.

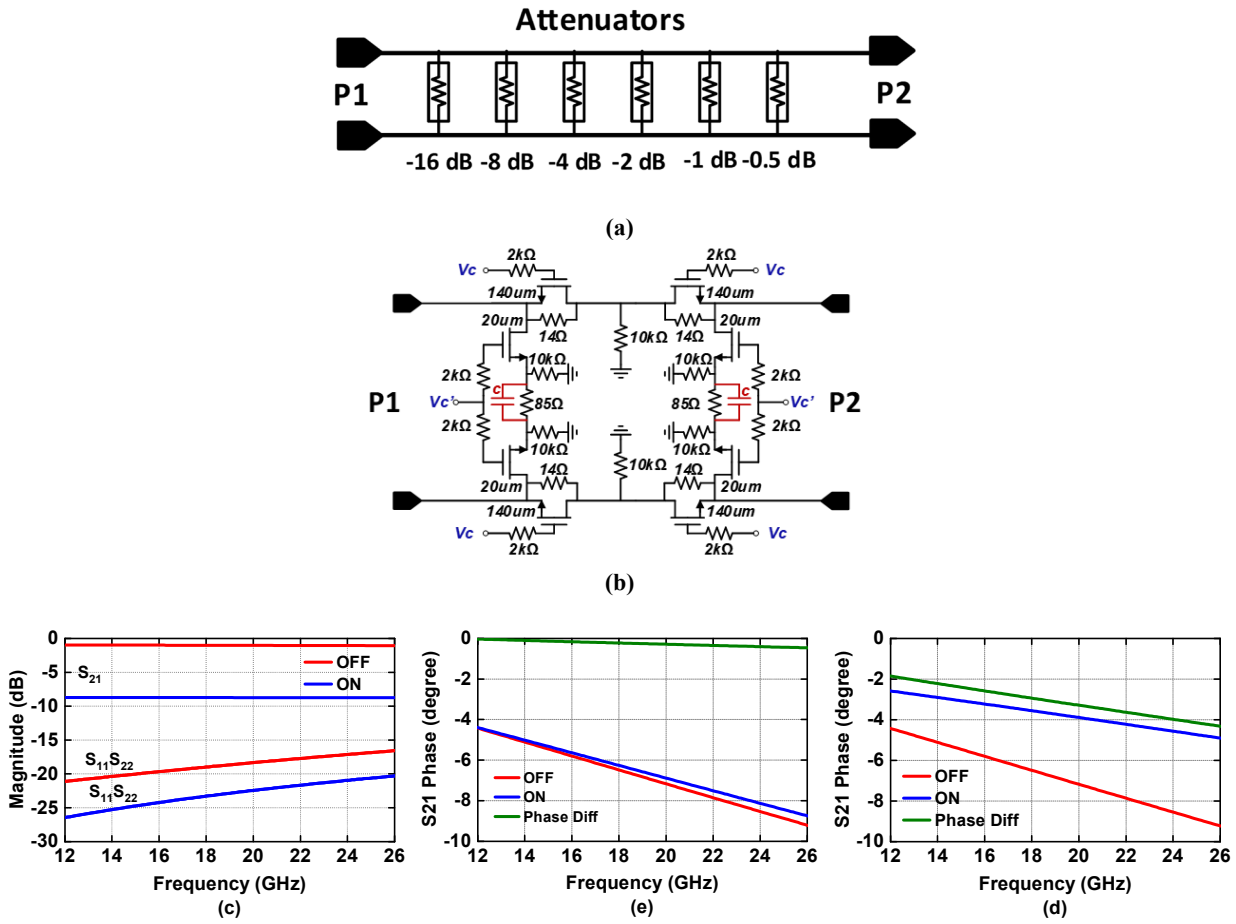


Figure 5.8: (a) Block diagram of differential switched π-type 6-bit attenuator. Differential switched π-type one-bit 8-dB attenuator (b) schematic and simulated (c) S-parameters. Simulated on and off state of S_{21} phase and phase difference (d) without, and (e) with the added parallel correction capacitors.

5.3.5 Differential Switched π-Type 6-Bit Attenuator

The gain control of I- and Q- signals is based on a switched π-type 6-bit attenuator with 32-dB gain control range and 0.5 dB step. Figure 5.8(a) presents the block diagram of differential switched π-type 6-bit attenuator showing the arrangement of the six attenuation stages to realize 32, 16, 8, 4, 2, 1, 0.5 dB attenuation levels. Figure 5.8(b) shows the schematic of the 8-dB attenuator with the added parallel correction capacitors to minimize the phase difference between the ON and OFF states. It has a simulated S_{21} of -0.9 dB (OFF state) and -8.8 dB (ON state), resulting in a 7.9 dB attenuation level. The simulated S_{11} and S_{22} are identical due to the symmetric

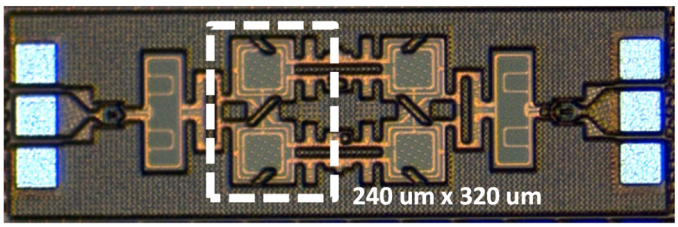


Figure 5.9: The microphotograph of the differential transformer-based Wilkinson power combiner used in the proposed passive vector modulator.

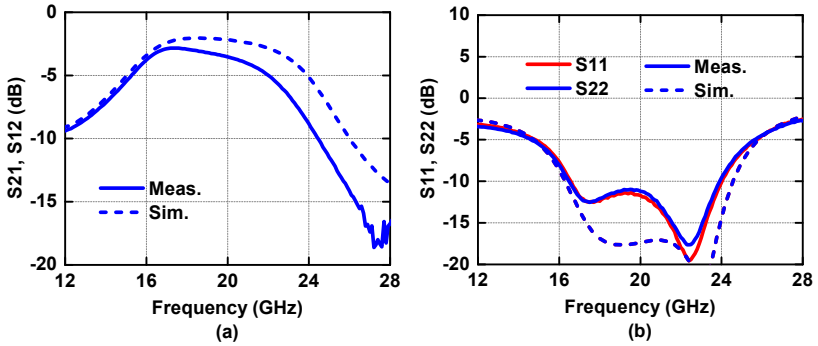


Figure 5.10: Measured and simulated (a) insertion loss (S_{12}, S_{21}), and (b) input and output return losses (S_{11},S_{22}) of the differential transformer-based Wilkinson power combiner.

design, and both return losses are <-18 dB at 16 – 22 GHz [Figure 5.8 (c)]. An added parallel correction capacitor of 17 fF is used and reduces the simulated phase difference between the ON/OFF states from 3° to 0.25° at 19 GHz, as shown in Figure 5.8 (d, e).

5.3.6 Differential Transformer-based Wilkinson Power Combiner

A Wilkinson power combiner is chosen to implement the needed adder in the passive VM. The design is based on the differential transformer-based Wilkinson power combiner and implements the schematic with two transformers proposed in [13]. It has the advantage of smaller area than the conventional Wilkinson using λ/4 transmission lines, and broader bandwidth than the ones based synthetizing λ/4 transmission lines using a lumped C-L-C π-network [13].

The K-Band Differential transformer-based Wilkinson power combiner design achieved a compact core area of 240 um x 320 um, as shown in Figure 5.1. It has a measured insertion loss of

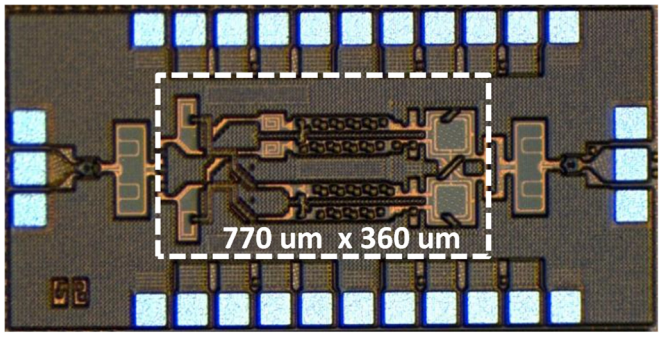


Figure 5.11: The microphotograph of a standalone passive vector modulator, the phased shifter implemented in the channel of the K-band dual-polarized receive phased-array beamformer chip.

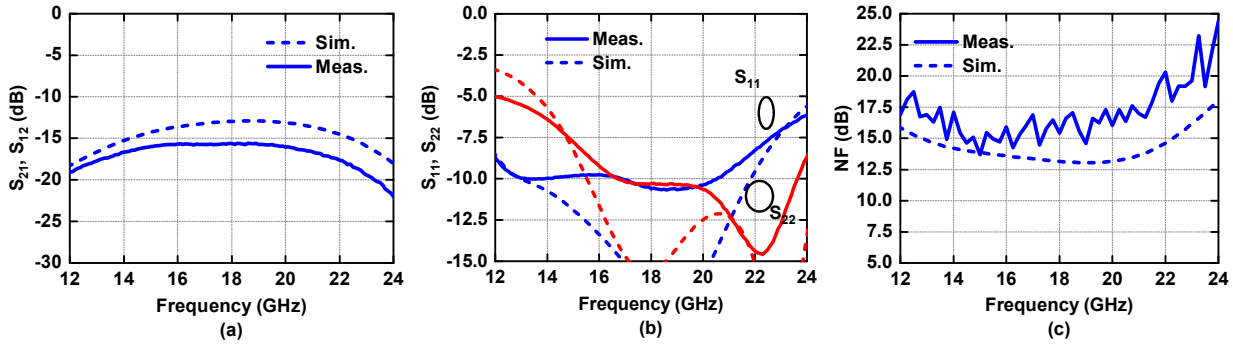


Figure 5.12: Measured and simulated (a) insertion loss (S12, S21), (b) input and output return losses (S11,S22), and (c) NF of the standalone passive vector modulator.

2.8 dB at 17.5 GHz with a measured 26% 1-dB fractional bandwidth from 15.9 GHz to 20.7 GHz. The simulated isolation is > 22 dB at 17.4 – 20.4 GHz.

5.4 Passive Vector Modulator Calibration and Measurements

A stand-alone passive vector modulator was fabricated after integrating the VM building blocks, and its microphotograph is presented in Figure 5.11. The design is based on the block diagram shown in Figure 5.6 (b). The added input and output baluns are de-embedded from the following measurement results as they were added to enable the single-ended testing of the differential VM.

Figure 5.12 presents the measured S-parameters and NF of the zero-power consumption vector modulator. The measured insertion loss is 15.7 dB, with a 3-dB bandwidth of

12.3 – 22.7 GHz. The measured S_{11} is -10 dB at 13.1 – 20.5 GHz, and S_{22} is <-10 dB at 16.7 – 23.6 GHz.

The needed amplitude and polarities of the IQ signals to set the phase states can be calculated using (5.1) and (5.2). However, to achieve the highest resolution of the VM with the lowest RMS amplitude and phase errors, a full simulation or measurements of phase states are needed to take into account any small IQ amplitude and phase differences, or any small phase change with attenuator states. However, it is a time-consuming task and was not done for this work.

Instead, the S_{21} magnitude and phase of the 64 attenuator states for one 6-bit attenuator is measured while the other 6-bit attenuator is at maximum amplitude attenuation. Then, the same is repeated for the second 6-bit attenuator. Then, both steps are repeated for each of the 4-states of the 2-bit sign selection switches, resulting in a measurement data of 512 states (only 3.1% of all available states). Using the measured data and (5.1) and (5.2), all the $2^{14\text{-bit}}$ states are predicted with high accuracy. The accurate prediction is essential to allow the selection of the needed phase states to minimize the RMS amplitude and phase error at any frequency of interest.

The 8-bit phase shifter is toggled, and the corresponding change in phase and gain are presented in Figure 5.13 (a, b). Also, the measured amplitude and phase errors are shown in Figure 5.13 (c, d). It is clear that the stand-alone passive vector modulator is optimized at 18 GHz. As a result, it has a measured RMS phase error of 0.65° at 18GHz, and < 2° at 16.3 – 19.6 GHz [Figure 5.13 (e)] and a measured RMS amplitude error is 0.1 dB at 18 GHz and < 0.3 dB at 16.2 – 20 GHz [Figure 5.13 (f)].

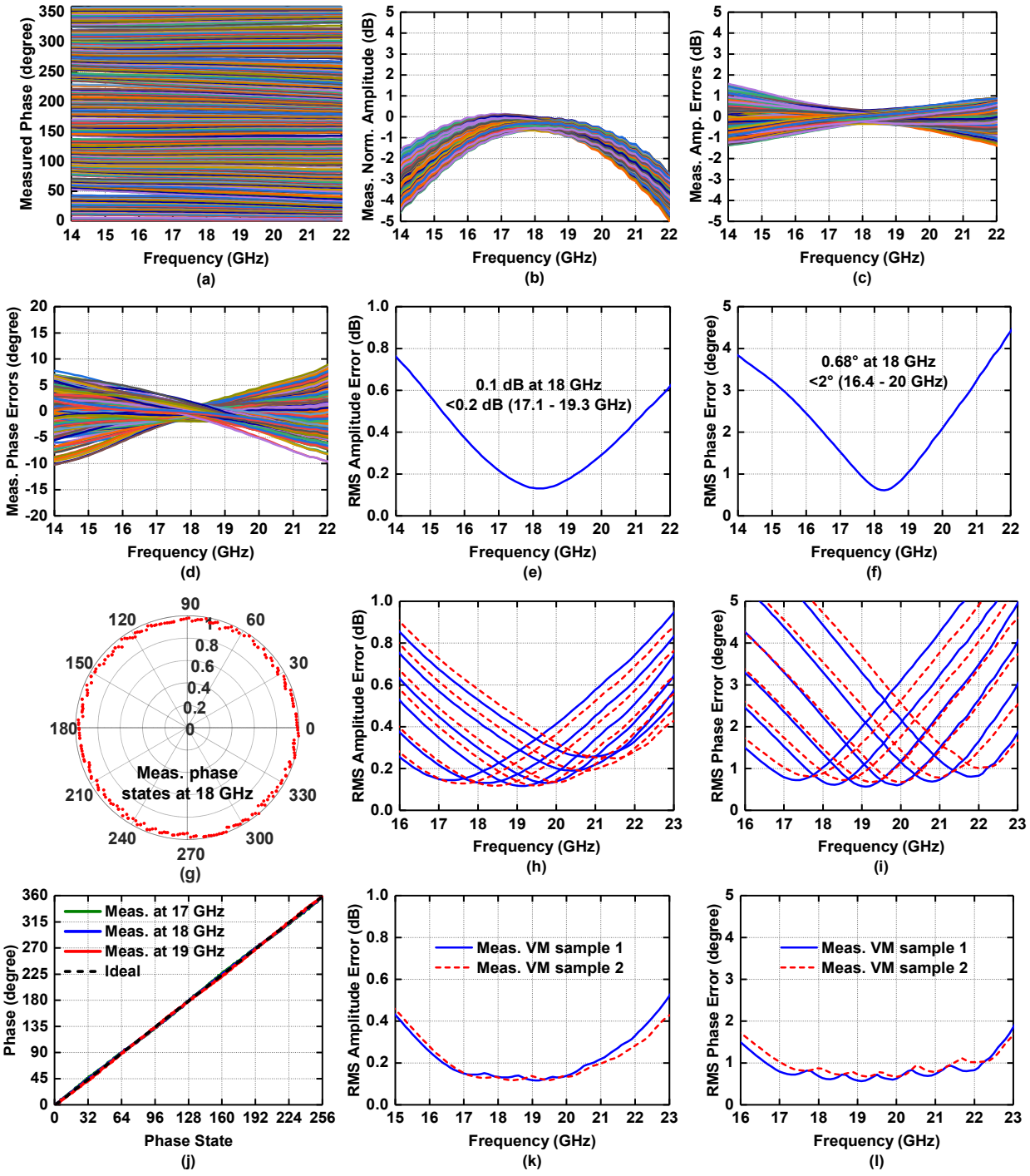


Figure 5.13: Measured (a) phase states, (b) amplitude change with phase states, (c) amplitude errors, and (d) phase errors of the standalone passive vector modulator. RMS (e) amplitude and (f) phase errors when the VM is optimized at 18 GHz, (g) measured phase states at 18 GHz, RMS (h) amplitude and (i) phase errors of two VM samples optimized at 17, 18, 19, 20, 21 and 22 GHz. (j) Measured phase states at 17, 18, and 19 GHz. Minimum RMS (h) amplitude and (i) phase errors of two VM samples showing the same optimization setting is applied to a second VM sample and it achieved the similar performance proving the design approach is reliable.

Table 5.3: Comparison of the VM with other published VMs using CMOS technologies

Reference	Process/ Number of Bits	Frequency [GHz]	FBW [%]	Insertion Loss [dB]	RMS Phase Error [°]	RMS Amp. Error [dB]	Power [mW]	Size [mm^2]
This work Standalone VM	**45 nm CMOS SOI 8-Bit**	**12.3 – 22.7**	**59.4**	**15.7**	**0.65**	**0.1**	**0**	**0.277**
[14] MWCL 2020	65 nm CMOS 5-Bit	27 - 42	43	13.4	0.7	0.8	0	0.395
[15] 2018	180 nm CMOS 5-Bit	26 - 30	14.3	16.5	1.6	0.68	0	0.840
[16] 2009	180 nm CMOS 3-Bit	21 -29	32	12.7	2.2	0.8	0	0.285

Additionally, the passive VM was optimized for each of the following frequencies (17, 18, 19, 20, 21, 22 GHz). Then, the same digital control setting obtained from the first VM sample is applied directly to a second VM sample on a different chip, and both achieved similar performances, as shown in Figure 5.13 (h, i). This shows that the measurement of the 512 states is a one-time calibration process and can be transferred from chip to chip. Without the need of re-calibration for the second VM sample, it achieved an RMS phase error of < 1° at 17 – 22 GHz, and RMS amplitude error of < 0.2 dB at 17– 21 GHz Figure 5.13 (k, l). Therefore, a digital assisted circuit can be added to the beamformer channel to maintain this excellent performance over the entire frequency range intended for K-Band SATCOM Rx applications.

Table 5.3 compares the stand-alone VM performance with other published passive VMs using CMOS technologies. It has the highest resolution of 8-bit with the minimum RMS phase and amplitude errors. Also, it has the broadest fractional bandwidth and the minimum core area.

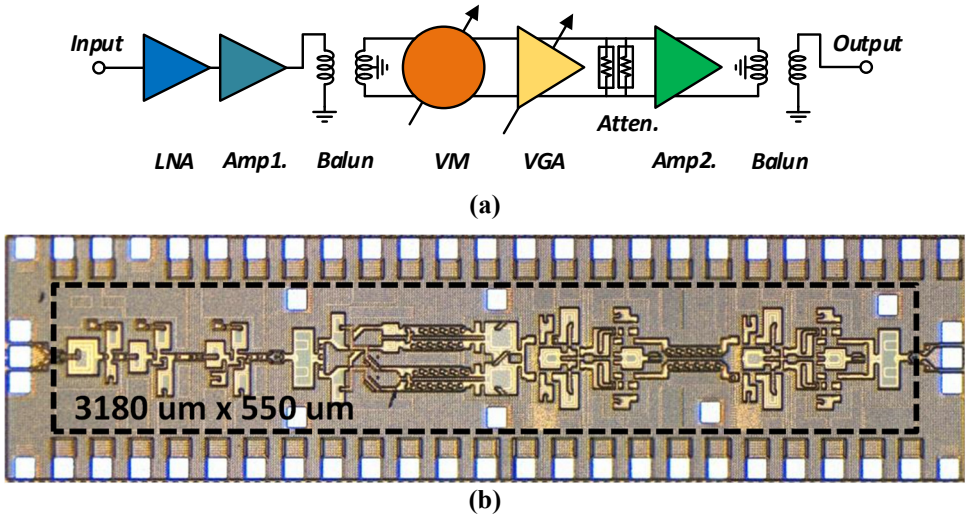


Figure 5.14: (a) Block diagram and (b) microphotograph of the channel of the K-band dual-polarized receive phased-array beamformer chip.

5.5 Entire K-band Phased-Array Receive Beamformer Channel

The block diagram of the K-band phased-array receive beamformer channel in 45 nm CMOS SOI is shown in Figure 5.14 (a). It consists of the LNA, followed by another by a one cascode stage amplifier to compensate for the insertion loss of the following balun and passive vector modulator. Also, it has a differential variable gain amplifier based on a cascode current-steering topology followed by the switched π-Type 6-Bit attenuator for gain control. There is an additional amplification stage for added gain. Finally, the output balun is added for testing purposes only. Figure 5.14 (b) shows the microphotograph of the fabricated K-band beamformer channel. It has a core area of 1.75 mm^2 (3.180 mm x 0.55 mm), excluding the pads and 3.17 mm^2 (3.370 mm x 0.94 mm), including the pads. The digital control pads limit the size of the chip. Once a serial peripheral interface (SPI) is implemented with a built-in PTAT current for biasing, the number of pads will be reduced, allowing the reduction of the channel core area.

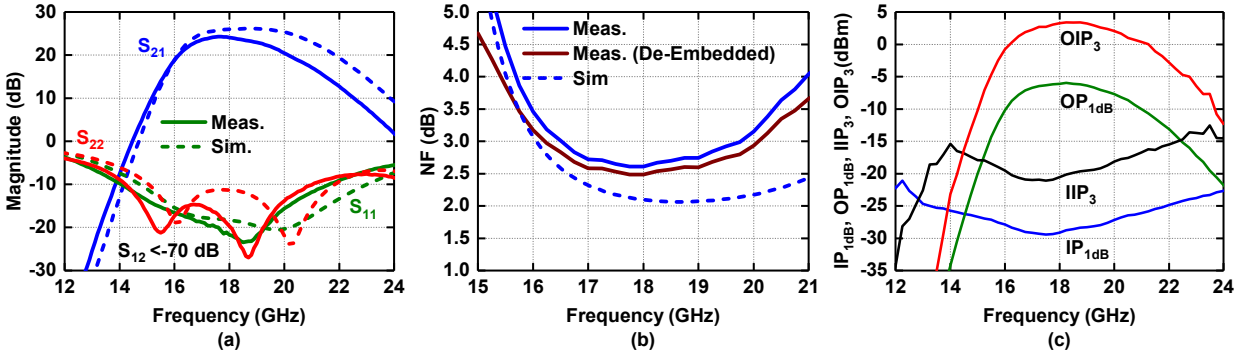


Figure 5.15: Measured and simulated (a) S-parameters, and (b) NF, and (c) measured P_{1dB}, OP_{1dB}, IIP_3 and OIP_3 of channel of the K-band dual-polarized receive phased-array beamformer chip.

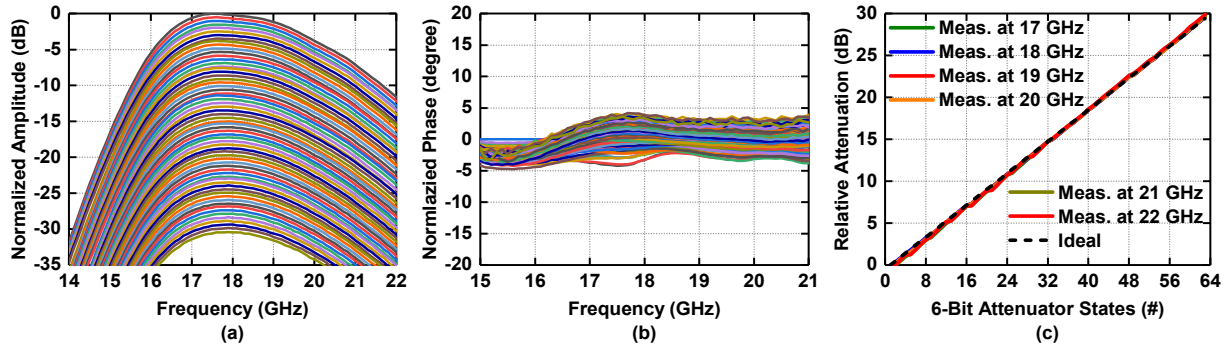


Figure 5.16: Measured of the 6-bit attenuator (a) relative attenuation, (b) relative insertion phase change with attenuation states, (c) relative attenuation at 17 – 21 GHz versus the number of the states. This was measured using the attenuator of channel of the K-band dual-polarized receive phased-array beamformer chip.

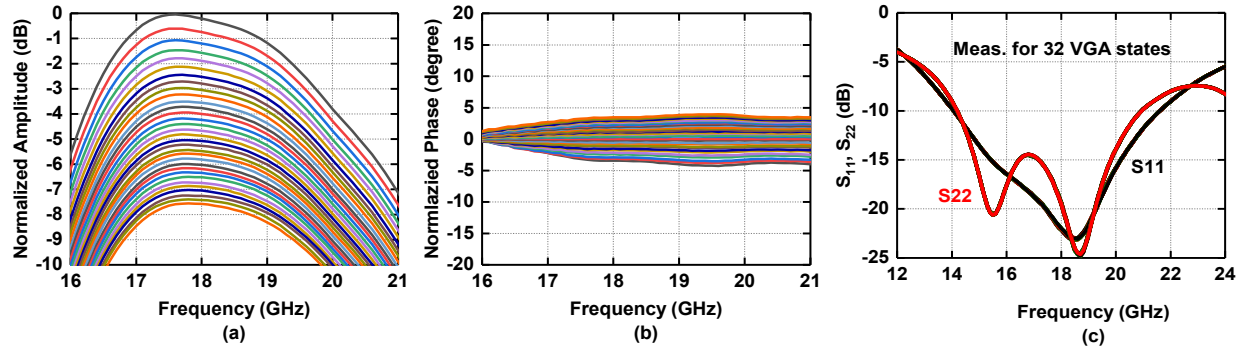


Figure 5.17: Measured of the 5-bit VGA (a) gain states, (b) relative insertion phase change with gain states. Measured (c) S_{11} and S_{22} of channel of for the all the 32 VGA gain states.

Figure 5.15 (a) presents the measured and simulated S-parameters of the phased-array beamformer channel at the highest gain state. The measured channel peak gain is 24.2 dB with 3 dB BW of 16.4-19.8 GHz, and the measured S_{11} is < -10 dB at 14.1 – 21.6 GHz, and S_{22} < -10 dB at14.3 – 21 GHz. The measured reverse isolation is <-70 dB (not shown), and the total power

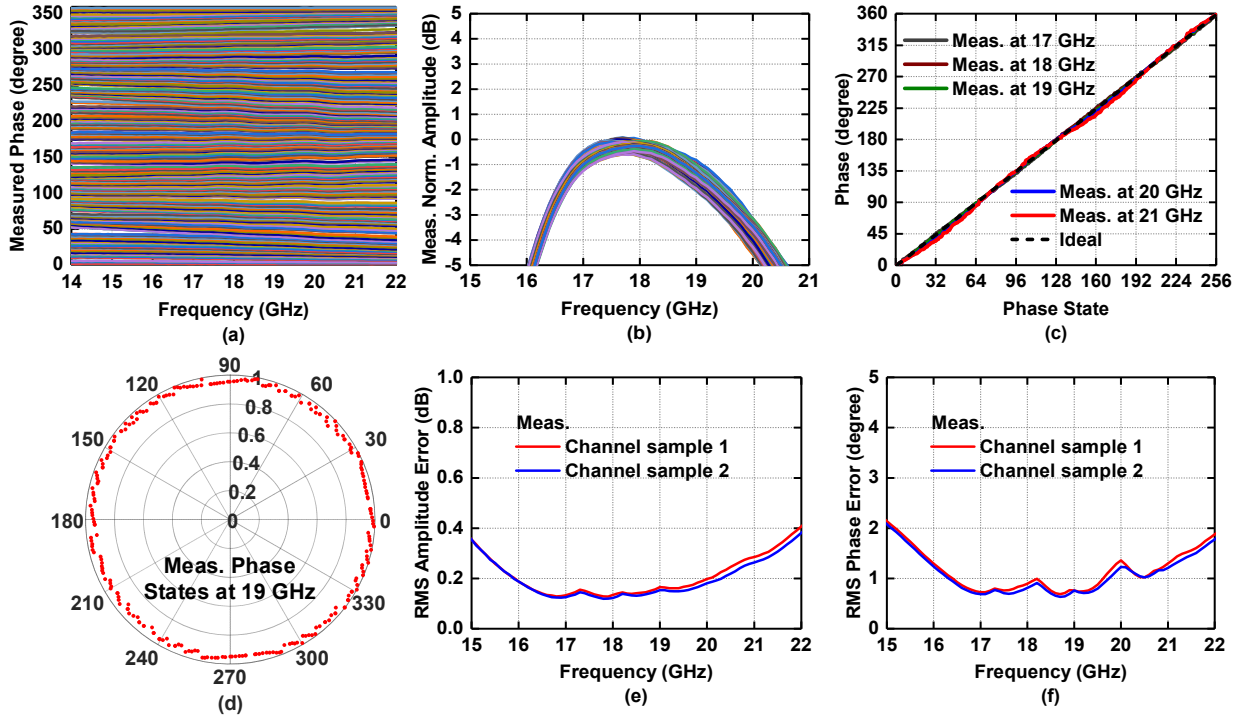


Figure 5.18: Measured (a) phase states, (b) amplitude change with phase states, (c) phase states at 17, 18, 19, 20, and 21 GHz, and (d) phase states at 18 GHz of the 6-bit VM in channel. RMS (e) amplitude and (f) phase errors of two channel samples optimized at 17, 18, 19, 20, 21 and 22 GHz.

consumption is 50 mW. The measured NF is 2.5 dB to 3.1 dB at 17.2 – 20.2 GHz [Figure 5.15(b)]. Also, the measured IP1dB is -29.32 dBm to -26.7 dBm at 17.2 – 20.2 GHz, and IIP3 is -21.0 dBm to -17.7 dBm at 17.2 – 20.2 GHz [Figure 5.15(c)].

The gain control is done mostly using the switched π-type 6-bit attenuator shown in Figure 5.8 [a]. The channel achieved a 30 dB gain control range with a 0.5 dB gain step and with a very low phase change of ±2.9°, as presented in Figure 5.16. For a finer tuning step, a VGA with current steering topology is used. It has a 7.2 dB gain control range with 0.25 dB gain step, as shown in Figure 5.17.

Figure 5.18 presents the measured relative phase and gain response of the VM in the K-band channel. Using the digital control setting obtained from the first VM sample, the measured

RMS phase error is < 1.4 ° at 16 – 21 GHz, and the measured RMS amplitude error is < 0.3 dB at 16 – 21 GHz [Figure 5.18 (e, f)].

5.6 Comparison to Prior Work

The performance of the K-Band phased-array beamformer channels is compared to previously state-of-the-art published beamformer channels, in Table 5.1, and shows the lowest noise figure, and with the highest phase shifter resolution of 8-bit than all other works. This channel demonstrates the lowest RMS amplitude and phase errors and the largest gain control with comparable gain and low power consumption.

5.7 Conclusion

This chapter presented a K-band low-power low-noise phased-array beamformer channel with a novel 8-bit phase shifter and low phase imbalance gain control using GlobalFoundries 45-nm CMOS SOI. The receive channel has a realized peak gain of 24.2 dB with 3-dB bandwidth of 16.4-19.8 GHz and 2.5 dB NF. The phase shifter has a high resolution of 8-bit to realize the full 360° with the RMS phase and amplitude error of <1.4° and < 0.3 dB, respectively. Also, the channel offers a 37.2 dB gain tuning range with a fine 0.25 dB step and low phase imbalance due to the added correction capacitors. The single blocks and the channel achieved state-of-the-art performance when compared to previous work. The lowest NF, high gain, high-resolution phase shifter with low RMS phase and amplitude errors, and wide gain tuning range with finer gain step make this beamformer channel suitable for SATCOM K-band receive phased-array systems. The dual-polarized receive phased-array beamformer chip based on this channel will achieve high performance with low power and can achieve low sidelobes levels and high cross-polarization purity.

Table 5.4: Comparison with the state-of-the-art beamformer channels and chips

Reference	Technology	Frequency (GHz)	FBW (%)	Gain (dB)	NF (dB)	Gain Tuning (dB)	Gain Step (dB)	Phase Shift Res. (°)	VM RMS Errors		IP1dB (dBm)	IIP_3 (dBm)	Core Area (mm^2)	Power (mW)
									Phase (°)	Gain (dB)				
This Work	**45 nm CMOS SOI**	**16.4 – 19.8**	**18.8**	**24.2**	**2.5**	**37.2**	**0.25**	**1.4**	**1**	**0.15**	**-29.3**	**-21.0**	**1.75**	**50**
[17] TMTT 2020	45 nm CMOS SOI	22.0 – 44.0	66.7	26.2	3.0 – 3.6	16	0.8	11.25	6	1.9	-25.4	-18	1.89	112
[18] TMTT 2019		24.0 – 30.0	22.2	16	3.7	7.5	0.5	11.25	4	0.8	-15	-7	2.96	54
[19] RFIC 2019	28 nm CMOS	37.0 – 40.0	7.8	42	6.0 – 7.6	27	1.5	11.25	-	2	-44	-	-	78.5
[20] APMC 2018	65 nm CMOS	36.0 – 40.0	10.5	40	6.0-9.0	20	1.0	22.5	5.5	2	-41	-	-	174
[12] TCAS II 2020	130 nm SiGe BiCMOS	22.0 – 27.0	20.4	28.5	3.3	6	0.4	5.6	0.2	1.0	-28	-	1.33	48
[21] RFIC 2018	180 nm SiGe BiCMOS	24.5 – 30.5	21.8	19	5.5	26	-	5.6	4	0.6	-19	-	1.42	160
[22] JSSC 2018		27.0 – 33.0	20.0	20	4.6	14	-	5.6	6	0.8	-22	-12	1.46	130

5.8 Acknowledgment

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Chapter 6

Conclusion

This thesis presented affordable Ku-band phased arrays and high-performance K-band communication circuits and systems in advanced SiGe and CMOS SOI technologies for SATCOM on-the-move applications. First, a Ku-band receive phased-array tile with 256-elements was presented in chapter 2. The Rx phased array could receive linear, rotated, and circular (or elliptic) polarizations. The design achieved a wide 3-dB instantaneous bandwidth, wide scanning in all planes, and with low scan loss. This Rx array demonstrated that building low-cost planar phased-arrays is possible, and they can synthesize any pattern (sum, tapered, monopulse, cosecant, or flat-top patterns) with accuracy and with minimal calibration. The patterns and results have been near-ideal and provide a high degree of confidence in this design approach.

Second, an ultra-low-profile dual-polarized 256-element Ku-band transmit phased-array tile was presented. The phased-array achieved a measured EIRP of 64.5-dBm and 66.5-dBm at P1dB and Psat, respectively, per polarization and high cross-polarization isolation in the azimuth and elevation planes. The measured EVM and ACPR were excellent at P1dB values, showing that the array can be operated without backoff, thereby increasing the overall system efficiency of affordable mobile Ku-band SOTM terminals.

Third, a packaged single-ended K-band SiGe LNA was demonstrated in a 0.18-μm SiGe BiCMOS process technology with a state-of-the-art performance. Also, a packaged K-Band CMOS LNA was demonstrated in a 45 nm CMOS SOI process technology with leading-edge performance. At a power consumption of 12.5 mW, it achieved a gain of 23.1 dB at 17.3 GHz with a 45% fractional BW and NF of 1.5 dB at (15.7 – 17.2 GHz). Additionally, it was shown that a simplified simulation schematic could be used to provide an accurate representation of the packaging effects in a shorter time than the full 3D EM simulation model.

Finally, a K-band phased-array beamformer channel with a novel 8-bit phase shifter and low phase imbalance gain control was presented. The low power with the lowest NF, high gain, high-resolution phase shifter with low RMS phase and amplitude errors, and wide gain tuning range with finer gain step make this beamformer channel suitable for affordable and high-performance SATCOM K-band receive phased-array systems.

6.1 Future Work

In chapter 5, a K-band phased-array beamformer channel has been presented. The promising performance of this channel suggests a K-band receive a phased-array beamformer chip with sixteen channels, and dual output ports can be implemented to receive two independent beams that can be linear, rotated, and circular (or elliptic) polarizations at the same time. Also, the leading-edge performance of the novel 8-bit passive vector modulator and low phase imbalance attenuator suggests that other applications, including 5G and advanced radars, may benefit from such phase shifting and gain control approaches.