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Front-end electronics and trigger systems – status and challenges

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Abstract

The past quarter century has brought about a revolution in front-end electronics for large-scale detector systems. Custom integrated circuits specifically tailored to the requirements of large detector systems have provided unprecedented performance and enabled systems that once were deemed impossible. The evolution of integrated circuit readouts in strip detectors is summarized, the present status described, and challenges posed by the sLHC and ILC are discussed. Performance requirements increase, but key considerations remain as in the past: power dissipation, material, and services. Smaller CMOS feature sizes will not provide the required electronic noise at lower power, but will improve digital power efficiency. Significant improvements appear to be practical in more efficient power distribution. Enhanced digital electronics have provided powerful trigger processors that greatly improve the trigger efficiency. In data readout systems they also improve data throughput, while reducing power requirements. Concurrently with new developments in high energy physics, detector systems for cosmology and astrophysics have made great strides. As an example, a large-scale readout for superconducting bolometer arrays is described.

keywords: electronics, integrated circuits, noise, power, trigger systems, bolometer arrays

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1. Introduction

The original title requested for this talk was “Modern Detector and Trigger Electronics”, but after giving it some thought, it wasn’t clear what constitutes “modern”. One definition can be derived from Marshall McLuhan’s statement:

If it works, it’s obsolete.

This could imply that modern electronics are characterized by not working. Indeed, there are numerous examples of “terminal cuteness”, where so many “modern” technologies were utilized that the cumulative challenges drove projects to failure. Although detectors for front-line science push the envelope, in high energy physics these are typically very large, complex, and expensive systems, so robustness, reliability, and cost are crucial. Another key requirement is fast turn-around in the prototype stage, which is often inhibited by special technologies that are only accessible at mass-production scales.

When custom integrated circuits were introduced into detector systems for high energy physics over two decades ago, there was a significant change in circuit design, as transistors could now be tailored to specific requirements and circuit topologies could be applied that were not practical with discrete components. These techniques have been extensively explored and today’s circuits apply these well-established circuit elements, albeit tailored to increasingly demanding requirements.

One of the hallmarks of progress in integrated circuit technology is the continual reduction in feature size and increased functionality. However, “modern electronics” can’t work miracles. As will be discussed below, under power constraints smaller feature sizes will not provide lower amplifier noise parameters, but reduction in sensor capacitance can reduce the equivalent noise charge. Smaller feature sizes reduce the size of some circuitry, although not necessarily in analog applications, but this does allow for additional circuitry to correct for shortcomings. For example, small feature sizes tend to increase threshold mismatches, but facilitate trim DACs to correct for this. Radiation damage shifts operating points, but digital control of bias circuitry can compensate. However, smaller feature sizes impose smaller supply voltages, which reduce dynamic range and place constraints on circuit topology. As a result, the major challenges are unchanged over the years: isolation of digital signals from the analog input, immunity to external pickup (e.g. power supply noise rejection), packaging (detector modules), power, and material, both in detector modules and in services. “Modern electronics” largely adapt existing techniques to incremental changes in technology.

2. Today’s electronics and their evolution

2.1 Electronics

Today’s front-end circuits have evolved along lines that originated in the 1980s, as illustrated for silicon strip detectors in Fig. 1. The first monolithic integrated circuit designed specifically for detector readout was the Microplex chip [1]. This was also the first chip designed with intimate involvement of high energy physicists, setting a

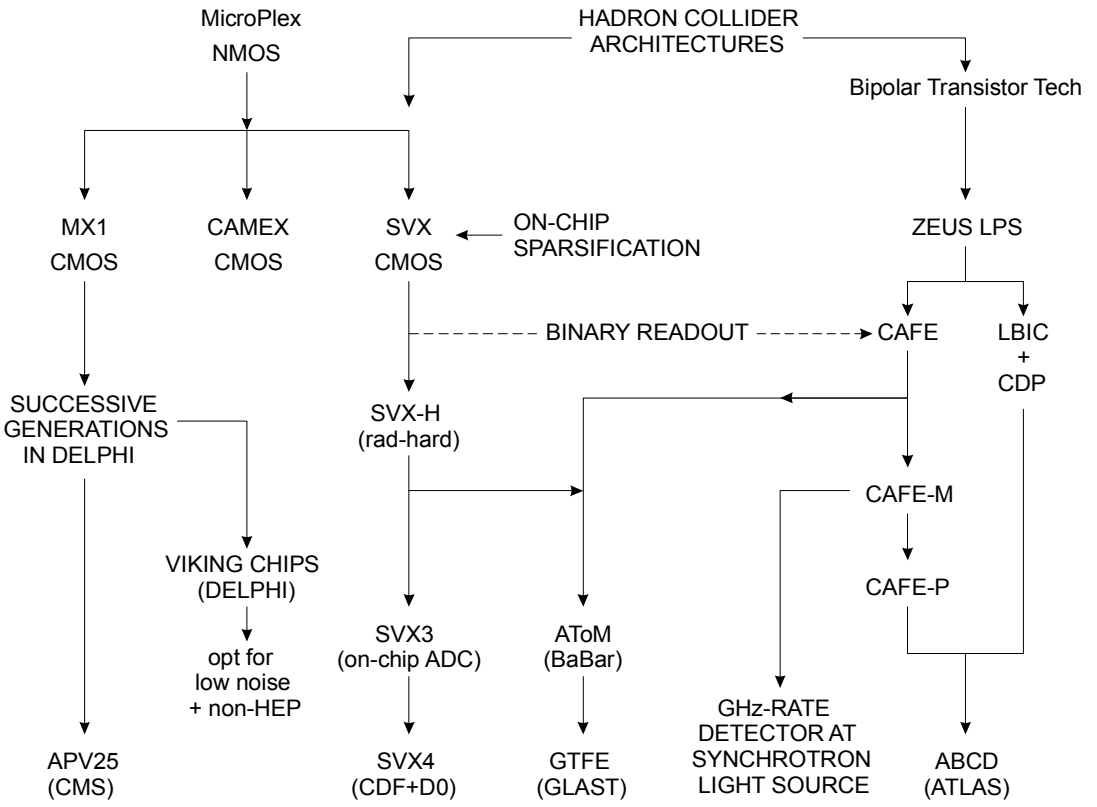

Fig. 1. Evolution over a quarter century of front-end ICs for silicon strip detectors.

precedent for subsequent designs at high energy physics laboratories. Parallel channels of charge-sensitive amplifiers and correlated double sampling pulse shapers were read out by a multiplexer that sequentially routed the analog output signals to the readout bus. These architectural elements were common to many subsequent designs, e.g. the MX [2] and CAMEX [3] chips used in e^+-e^- experiments at LEP. The SVX chip for CDF [4] extended this architecture to include threshold detection and on-chip zero suppression, so only channels with hits were read out to accommodate the higher occupancy at a hadron collider. Subsequent versions of the SVX chip were implemented in radiation-hard CMOS [5] and then incorporated on-chip analog-to-digital conversion, providing a fully digital readout [6]. The Viking chips originally designed for DELPHI [7] adopted time-invariant shaping, which – together with lower noise than its predecessors – opened its use in non-accelerator measurements that didn't provide a timing signal to synchronize the correlated double sampling. A direct descendent of the chips used at LEP is the APV chip [8], used to read out nearly 10 million channels in the 200 m^2 tracker in CMS.

The power dissipation of the Microplex was quite high (~ 10 mW per channel), so it had to operate with pulsed power, switching the supply voltages off between beam bunches. Today this is a recurring theme in designs for the International Linear Collider (ILC). Superficially, the reduction in power in the MX, CAMEX, and SVX has been attributed to the use of CMOS, rather than NMOS as in the Microplex . Although CMOS provides a significant power reduction in digital circuitry, the power dissipated in the input transistor is the same. The large power dissipation in the Microplex was determined by the input amplifier, which was designed with a much higher bandwidth than necessary. The

reasoning was that fast detectors need fast electronics, but this is not true, as the signal charge is initially integrated on the detector capacitance and then transferred into the amplifier as the charge-sensitive feedback loop becomes active [9]. The lesson is that one must consider design requirements very carefully, making sure that assumptions that lead to performance penalties are actually justified. It also illustrates that facile explanations are often accepted, even when they are not correct, so buzzwords frequently trump physics.

In the late 1980s a parallel development path emerged utilizing bipolar transistor technology. Initially, bipolar transistors were too large to accommodate circuitry on the 40 μm pitch needed for the 50 μm strip pitch in many detector designs. CMOS designs were also facilitated by the emergence of semiconductor foundry "brokerages" such as MOSIS, whose multi-project fabrication runs provide a low-cost prototyping path. The LBIC [10] and CAFE [11] chip designs initiated for the Superconducting SuperCollider and then continued for the LHC utilized more compact bipolar transistor processes that allowed circuitry on small pitches. Both the LBIC and CAFE chips utilized a binary readout that only registered the presence of a hit, which reduces dynamic range requirements in the front-end and simplifies the readout stream, both reducing power dissipation. There is an indirect cross-tie to the SVX chips. Although the SVX chip does provide analog information, in data analysis the binary data are used primarily, supporting the utility of a purely binary readout, which is still not generally accepted. The binary readout does allow analog measurements for diagnostic purposes by utilizing threshold scans.

These readouts faced a new challenge, as signal acquisition and data readout had to proceed simultaneously, unlike the situation at LEP or the Tevatron where the time between bunches was sufficiently large to read out the detector, so digital signal pickup to the analog front-end did not necessarily contaminate the signal, although this was still a problem in some designs. Both the LBIC and CAFE chips were operated in conjunction with a separate chip that included a digital pipeline and the readout circuitry. This allowed the optimum choice of technology for the analog circuitry, bipolar, and the digital portion, CMOS. The advent of BiCMOS processes allowed these to be combined in one chip, as implemented in the ABCD chip [12] used in ATLAS.

Experience from both the SVX designs and the bipolar front-end developments contributed to the AtoM chip used in BaBar [13], where the bunch structure is short enough to be equivalent to a DC beam, so readout and signal acquisition proceed simultaneously. In the BaBar silicon vertex tracker the readout does not degrade the electronic noise, unlike many other detectors where "common mode noise" was accepted as an inexorable fact of life. The experience from the AtoM chip led to a very low-power design in the GTFE chip [14] used in the GLAST satellite mission.

2.2 Radiation Effects

Currently, degradation of sensor properties is the primary limitation to detector lifetime under irradiation at the LHC. Use of "deep submicron" standard industry CMOS has extended electronics dose capability to beyond 100 Mrad [15, 16, 17]. The key is the use of thin gate oxides <100 nm, which accelerate the rate of electron tunneling from the

gate, so that the radiation-induced holes trapped at the silicon–oxide interface are neutralized. In analog circuitry the operating points can be adjusted to accommodate shifts in threshold voltage, but this is not possible in digital circuits, which tends to limit overall radiation resistance.

2.3 Pixel Systems

Pixel systems took a parallel path with substantial interaction with low-power designs for strip detectors. The small capacitance of pixels allows substantially lower noise than in strip detectors, so signal degradation due to radiation damage can be accommodated. Developments for high-luminosity colliders began in the early 1980s, but these systems are much more complex than strip detectors and together with increasing demands on radiation resistance and rate capability it has taken about two decades for them to come to fruition. Pixel detectors are essential at small radii in LHC experiments, both for pattern recognition and to sustain radiation damage. The enhanced radiation resistance of "deep submicron" CMOS has yielded pixel systems that operate beyond 100 Mrad.

The readout structure of the ATLAS pixel chip [18] (also see [9]) is shown in Fig. 2. The pixels are always active, but only transmit signals when they are struck, initiating a time stamp sent to a buffer at the base of each column. The signal amplitude, which is digitized by time over threshold, is stored in each pixel and only read out when a trigger is received with the corresponding time stamp.

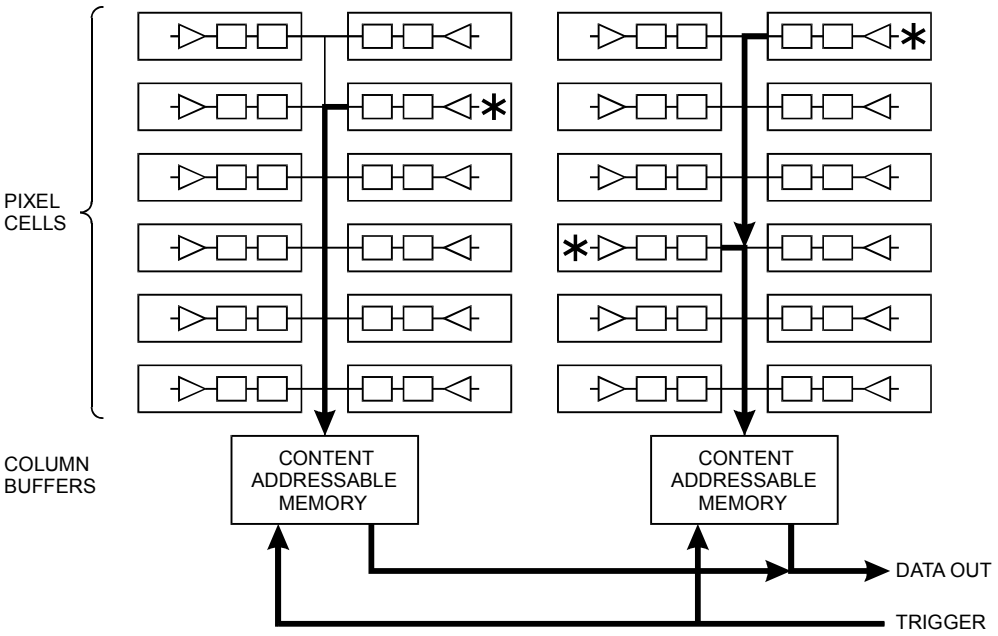

Fig. 2. Readout structure of the pixels in the ATLAS pixel chip. Signals are only transmitted when a pixel is truck. The time stamp is recorded at the chip periphery and the pixel is only read out upon receipt of a valid trigger.

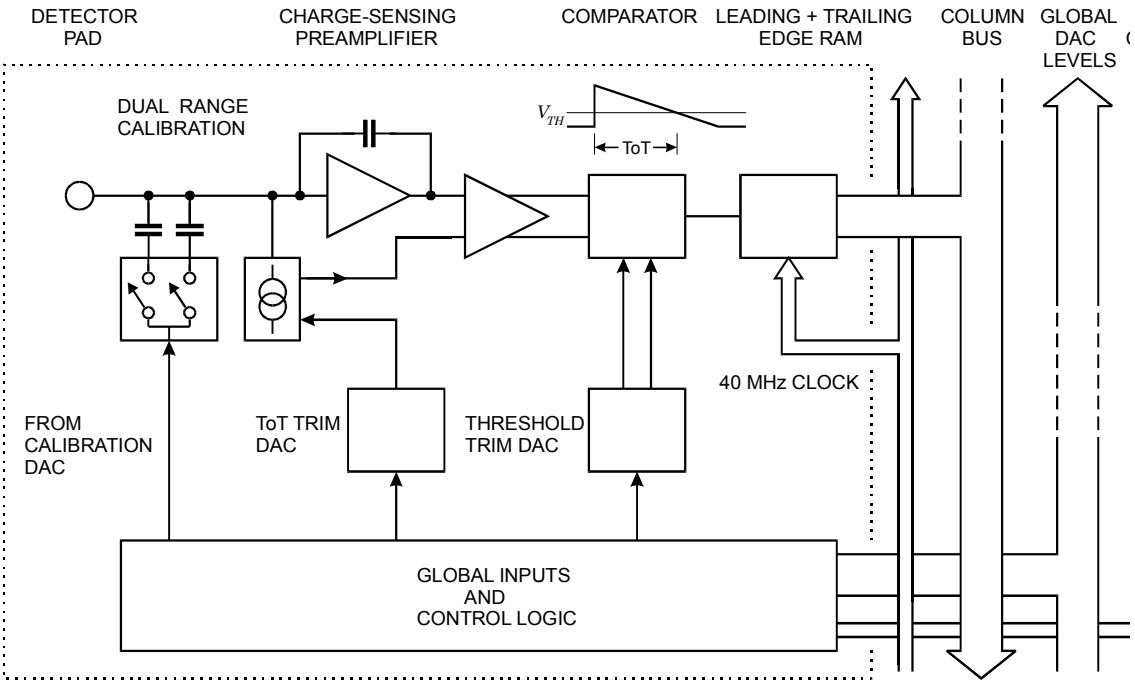

Fig. 3. Circuit blocks in the ATLAS pixel cell. Each cell contains a preamplifier, shaper, and threshold comparator. A buffer records time stamps of the leading and trailing edge of each pulse yielding time-over-threshold amplitude digitization.

Pixel systems for high levels of radiation damage require rather complex circuitry in each cell, as illustrated in Fig. 3. Additional complexity is introduced by the poor matching of small-geometry transistors, so the pixel-to-pixel threshold variations greatly exceed the electronic noise level. With a common threshold the spread sets the minimum signal threshold, negating the advantage of low noise. Adding a trim DAC to each pixel allows a fine adjustment so that threshold variations are well below the noise level of about 170 *e*.

The functionality in each pixel cell is driven by the requirements of radiation resistance, rate capability, and readout speed. New technologies will not reduce the required functionality. They can reduce the size of digital circuitry, but the size and power required for the transistors in the analog circuitry is set by the required noise and threshold matching.

2.4 Status summary

This discussion illustrates that the electronics that we use today, and are often taken for granted, have resulted from over two decades of parallel developments that together led to the wealth of experience and understanding that implicitly is incorporated in new designs. Although new designs are largely project-driven, they rely critically on the insights from a rich and varied history of previous parallel efforts. The importance of multiple parallel R&D efforts should not be underestimated, even in an age of decreasing funding.

3. Future Requirements

Two future operating environments characterize many of the challenges the future will pose. The ILC will relax requirements on radiation resistance and rate capability, but the vertex detectors require position resolution of order several μm to separate tracks in the cores of jets, so pixel sizes of about 20 μm close to the beam are needed. Minimizing material is critical, so power must be reduced to allow gas cooling and reduce material in power cabling. Tracking performance must be maintained in the forward regions, unlike previous collider detectors, where forward performance has been significantly worse than in the central region. This places severe constraints on cabling and support systems, that tend to concentrate material in the forward directions.

The Super LHC (sLHC) upgrade will increase luminosity ten-fold and probably reduce the bunch frequency, which will increase the number of interactions per crossing and hence the number of tracks to about 400. This increases requirements on pattern recognition throughout the detector and track separation close to the beam. Radiation damage in the sensors will reach levels where carrier lifetime due to trapping will significantly reduce signal charge, requiring a commensurate reduction in electronic noise. Constraints on the material budget are still stringent and a significant contribution is due to services. For example, in the ATLAS SCT the total material per layer is 3% X_0, of which half is for services, i.e. cooling, cabling, support. The total material in the three barrel layers of the ATLAS pixel system comes to 10.7% X_0, with 1.3% in the hybrids and cabling, and 6.9% in the support and cooling structures.

4. Novel structures

Current detectors are typically composed of separate sensors and readout ICs, either connected by wire bonds or a two-dimensional array of bump bonds in hybrid pixel devices. Some new developments, monolithic active pixel sensors (MAPS) and multi-tier electronics, are examples of structures that monolithically integrate sensors and complex readout electronics.

MAPS utilize commercial CMOS processes, where the epitaxial (epi) layer between the active devices and the substrate can be used as a sensor. The epi layer is thin, of order 10 μm, and the sensor bias voltage is limited, so charge collection proceeds primarily by diffusion. However, these structures allow very small pixel sizes of order 10 μm, so the small capacitance yields noise levels adequate to detect the small signal charge from minimum ionizing particles with good efficiency, although the typical signal-to-noise ratio of 10 does not provide much margin. Together with CCDs and DEPFET sensors these devices are among the prime candidates for vertex detectors at the ILC. However, the size of individual arrays is limited by chip reticle sizes (~ 20 mm), so many devices with the associated power and signal bussing must be integrated on the support structure to form the roughly 1 m^2 size detectors. The signal charge is very sensitive to minority carrier lifetime, as charge collection proceeds by diffusion and cannot be accelerated by application of bias voltages sufficient to form high fields throughout the sensitive region. This limits radiation resistance, although it appears to be adequate for the ILC.

Several papers at this conference describe recent developments [19-23]. Most MAPS utilize rather simple readout cells with correlated double sampling, similar to CCD output stages. This requires that all cells be read out to find hits. On-chip ADCs or threshold discriminators can be used to sparsify the external data readout, but the optimum architecture would resemble the pixel cell shown in Fig. 3. The small pixel size required at the ILC (~20 μm) imposes severe limits on the electronic circuitry, as the input transistor takes up a substantial fraction of the area to achieve the required noise level and the transistors in the threshold comparator must be rather large to control threshold matching. These circuits are subject to many of same design requirements as pixel designs for the LHC, but can't accommodate all of the circuitry, such as trim DACs. A prototype MAPS chip presented at this conference [21] accommodates a charge-sensitive amplifier, pulse shaper and threshold comparator in a 25 μm pixel, utilizing 130 nm CMOS. However, the simulated threshold dispersion is about equal to the electronic noise, which raises the usable threshold level. There are many applications for these devices and future developments will determine which applications are a good match for this technology.

A very interesting technology utilizes multi-tier structures to integrate a fully depleted sensor layer with multiple layers of electronics, as illustrated in Fig. 4. Designs for high energy physics were pioneered by Arai et al. [24, 25] and are also being pursued at FNAL [26]. These structures are often referred to as "SOI" or "3D". However, the common SOI (silicon on insulator) structures that have been available for decades include only a single layer of electronics and the term 3D is already used for a novel detector structure [27], so multi-tier is more appropriate.

350 μm thick substrate layers have been used, operating at full depletion and providing good charge collection efficiency and short collection times. The multiple layers

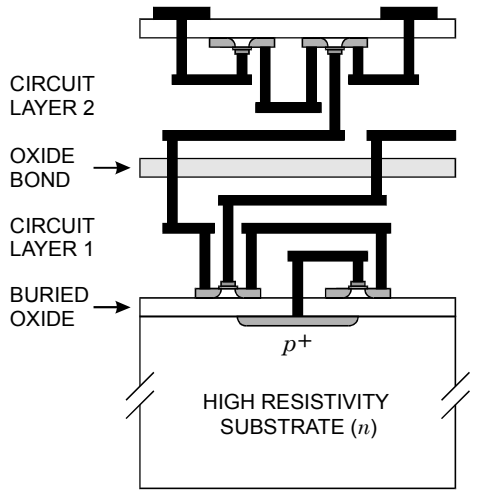

Fig. 4. Multi-tier ICs combine multiple layers of electronics isolated by intermediate oxide layers. A high-resistivity substrate is utilized as the sensor. Sensor layers of 350 μm thickness have been implemented. For fabrication steps see refs. [24] and [26].

available for electronic circuitry facilitate small cell sizes and can also provide shielding layers between analog and digital circuitry. Arai et al. are using a commercial process, but this is not yet a mainstream technology. However, many industrial applications are pushing developments in this direction. Further investigation of the radiation resistance of the sensor layer will be necessary to assess the scope of future applications. However, compared to current MAPS, these devices provide significantly superior sensor characteristics and offer a wider scope of applications.

5. Power efficiency

5.1 Electronics

In digital circuitry the power dissipation is determined by the total capacitance C associated with the switched nodes, the switching frequency f, and the voltage swing V,

$$P = fCV^2 . \tag{1}$$

Smaller CMOS feature sizes reduce both the voltage swing and capacitance, so for a given switching rate f the power decreases.

In the analog front end the equivalent noise charge

$$Q_n^2 \approx i_n^2 T_S + e_n^2 \left(C_d + C_i\right)^2 \frac{1}{T_S}, \tag{2}$$

where T_S is the shaping time, i_n the spectral noise current density, which increases with sensor bias current $i_n^2 = 2eI_{bias}$, C_d is the detector capacitance, C_i the open loop amplifier input capacitance, and e_n is the amplifier spectral noise voltage density. Both the detector bias current and capacitance are proportional to strip length. The noise voltage density depends on the input transistor's transconductance g_m, $e_n^2 \approx 4kT / g_m$.

In analog circuitry the current draw is driven by requirements of noise and speed. Both depend on transconductance, the ratio of the change in a transistor's output current vs. the change in input voltage. In a bipolar transistor the transconductance depends only on operating current I,

$$g_m = \frac{I}{kT/e} = 38.5I , \tag{3}$$

and is independent of geometry and technology, as it is determined by basic physics (see [9], for example). The transconductance of a field-effect transistor, however, is a non-linear function of current, as shown in Fig. 5. The power efficiency depends on the ratio of transconductance per unit current g_m / I_D, which is shown as a function of current in Fig. 6. At low currents the region of constant g_m / I_D denotes the weak inversion regime, where the transconductance is proportional to current, as shown in the second panel of Fig. 5. This is similar to a bipolar transistor, but due to interface states the transconductance is only about 60% of a bipolar transistor, a result borne out in many generations of MOS devices. Submicron devices provide adequate transconductance in or close to the weak inversion regime, where the transconductance depends only on current and not on geometry, so reduction in feature size does not improve power efficiency (see

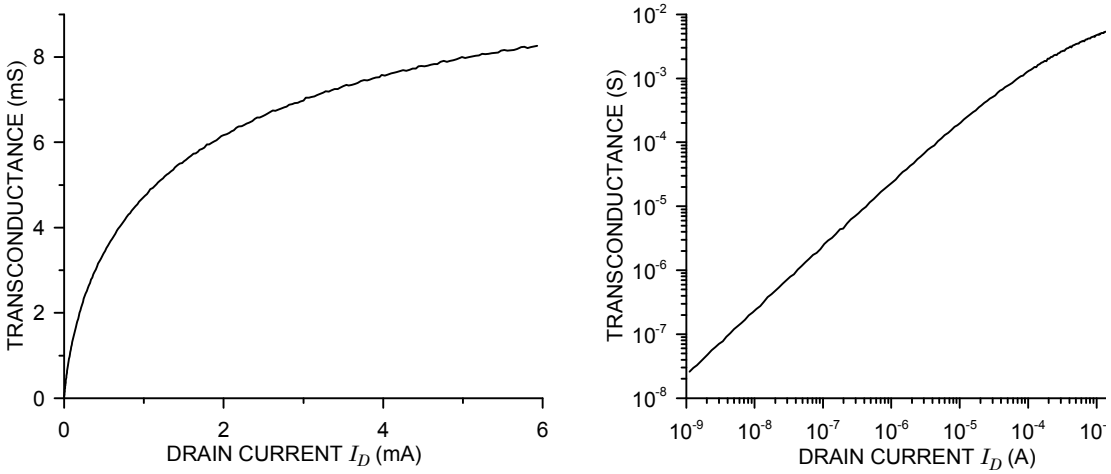

Fig. 5. MOSFET transconductance vs. current, shown for a device with a width of 100 μm and a channel length of 0.8 μm.

[9] for a more detailed discussion) . A smaller transistor can reduce the amplifier's input capacitance, but in systems optimized for power, the input capacitance is only a fraction of the sensor capacitance, so this is a minor effect.

The result of this discussion is that, given power constraints, the basic noise parameters of bipolar and field effect transistors will not improve with advances in technology.

In bipolar transistors the shot noise associated with the base current I_B adds additional

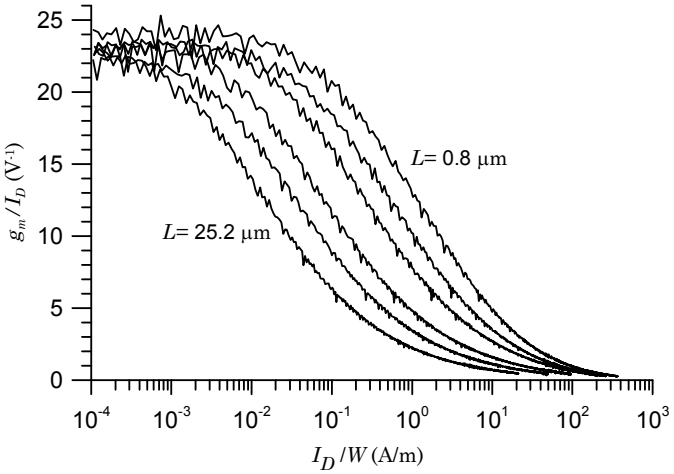

Fig. 6. Normalized transconductance g_m / I_D vs. normalized drain current I_D / W for channel lengths of 0.8, 1.2, 2.0, 5.2, 10.0, and 25.2 μm. All devices were fabricated on the same die in a 0.8 μm CMOS process. The transconductance is determined by differencing the raw measured I_D vs. V_{GS} data, so the irregularities in the curves are due to the differential non-linearity of the digitizer in the measurement system.

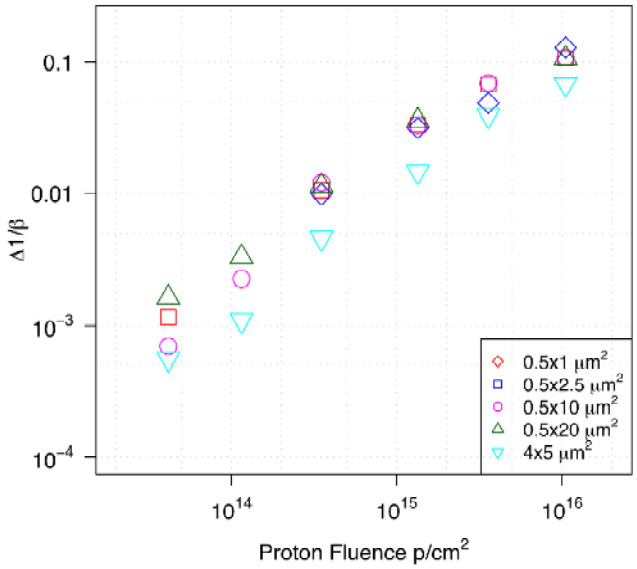

Fig. 7. DC gain degradation of SiGe bipolar transistors vs. fluence of 24 GeV protons.

noise, analogously to the detector bias current in eq. 2. Under irradiation displacement damage reduces the carrier lifetime in the base–emitter region, so the transistor's DC gain $\beta_{DC} = I_C / I_B$ degrades with particle fluence Φ, following the relationship

$$\frac{1}{\beta_{DC}} = \frac{1}{\beta_0} + K\Phi\,, \tag{4}$$

where β_0 is the pre-radiation DC gain and K depends on the particle type and energy. Generally, thinner base regions are less susceptible to radiation damage, so faster transistors tend to be better. BiCMOS processes combining SiGe heterojunction bipolar transistors with sub-micron CMOS are widely used in cell phones and other high-frequency communications systems and are readily accessible through foundry brokerages. Fig. 7 shows data taken by the Santa Cruz group on DC gain vs. fluence (24 GeV protons) on devices fabricated with the IBM 5AM process [28]. For small emitter areas the degradation remains acceptable up to fluences of 10^{16} cm^{-2} and shows promise for sLHC applications, as this would allow optimum usage of both bipolar and CMOS technology for minimum power dissipation.

5.2 Detector parameters

As noted above, a severe limitation at high fluences is the loss in signal charge due to recombination [29, 19]. After substantial displacement damage the lifetime is inversely proportional to fluence, $\tau \approx K / \Phi$, where $K \approx 2 \cdot 10^6$ s/cm^2 [30, 31]. For $\Phi = 10^{15}$ cm^{-2} this yields $\tau \approx 2$ ns, dropping to 0.2 ns at $\Phi = 10^{16}$, yielding a drift length of 20 μm at electron saturation velocity. For ideal charge collection a figure of merit for detector materials is Q_E / ε, the charge yield (signal charge per absorbed energy, inversely proportional to the

bandgap) divided by the dielectric constant, which reduces the capacitance and hence the equivalent noise charge. In the presence of trapping this must be modified to include the drift length, which is proportional to the mobility times the carrier lifetime, yielding the expression $\mu\tau Q_E / \varepsilon$. The reduced signal can be partially compensated by a smaller dielectric constant, as in diamond, for example.

In current detectors the main limitation from radiation damage is the buildup of space charge, which requires high operating voltages for full charge collection. Once carrier lifetime leads to drift lengths significantly smaller than the detector thickness, the detector can be thinned without a significant penalty in signal, since the largest contribution to the induced signal charge occurs as charges approach the pixel or strip electrodes at distances roughly equal to the electrode pitch [32]. The technologies developed for high voltage operation of strip detectors are still important, as high fields increase the drift length $\mu E\tau$. The "3D" detector configuration that alternates columnar *n*- and *p*-electrodes normal to the detector surface reduces the drift length required for full charge collection and allows thicker detectors, which increases the overall signal [27, 33].

Assume that the reduced signal charge due to trapping is S_{rad} / S_0. Under optimum scaling the power required to maintain the signal-to-noise ratio for the same detector capacitance and shaping time increases as $(S_0 / S_{rad})^2$ [34]. Alternatively, the signal-to-noise ratio in a strip detector can be maintained by reducing the strip length, so the capacitance and hence – to first order – the noise is reduced proportionally. Scaling the strip length by S_{rad} / S_0 increases the number of readout ICs and hence the total power by S_0 / S_{rad}, but this penalty is less than reducing noise by increasing the power in the input amplifier. This does increase material, so more efficient means of power distribution are important.

6. Power Distribution

Deep submicron processes operate at reduced supply voltages. A representative180 nm process, for example, has a maximum digital supply voltage of 1.8 V and a 130 nm process 1.2 V. Key circuit parameters such as noise and speed are set by transconductance, which in turn is set by device current. Thus, as discussed above, the current draw does not scale with feature size, but the supply voltage must be controlled more closely to avoid breakdown. To minimize material the cross-section of the power bussing is reduced, typically incurring a significant voltage drop. When many ICs or detector modules are fed by a common power bus, the dropout of one module can raise the voltage at the other modules to prohibitive levels, so the voltage drop in the cabling cannot be too aggressive.

6.1 Serial powering

Two mitigation approaches are being investigated. The first connects multiple modules in series, so the supply voltage increases proportionally allowing a greater tolerance in voltage drop. The power supply operates in constant current mode and the voltage at each module is controlled by local regulators, as shown in Fig. 8. Powering at constant current shifts the burden of voltage compliance (and additional power dissipation) to the external

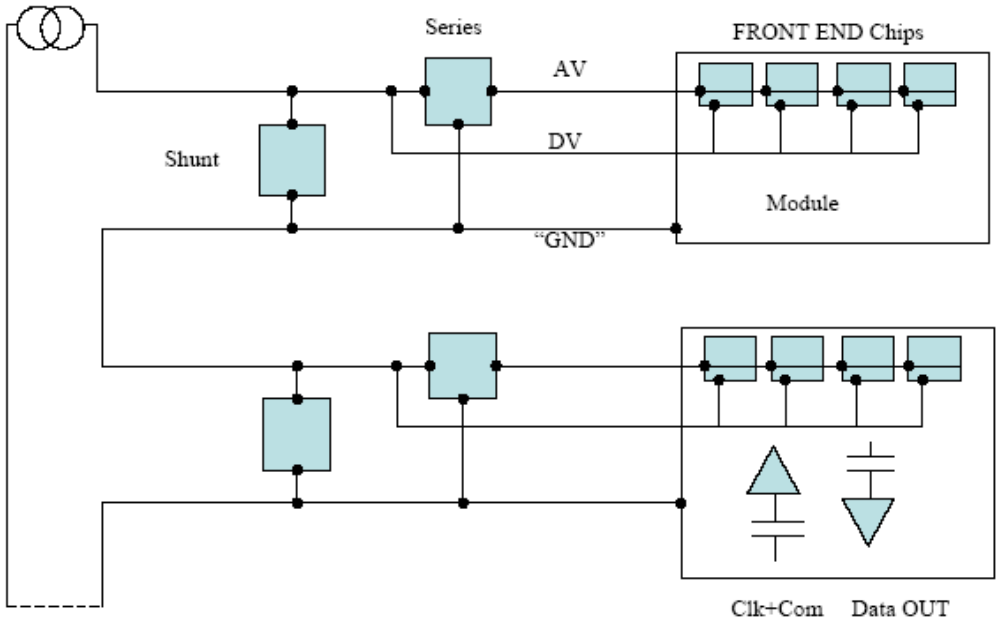

Fig. 8. Serial powering of silicon strip detector modules. (Figure courtesy of Carl Haber)

power supply. First implemented at the Univ. Bonn [35,36], this arrangement has also been tested at RAL [37] and LBNL [38], demonstrating full operation with little or no increase in noise. A stave design that integrates the detector module and support structure with the module services also contributes to material reduction [38].

6.2 Voltage conversion

The second approach to more efficient power distribution utilizes local power converters that transform a high supply voltage to the chip supply voltage, so the current in the primary supply lines is correspondingly smaller. This technique is commonly used in portable electronics, such as laptop computers. These systems typically utilize pulse width modulation to control the charge transferred to the regulator's output capacitor. Feedback controls the pulse width to set the desired output voltage. Fig. 9 shows a typical configuration. A representative commercial IC has a maximum input voltage of 5.5 V and provides 1.7 V with a current up to 7 A at an efficiency of 85%. The switching frequency is about 1.5 MHz, which allows use of a filter inductor L of about 200 nH, which can be implemented as an air core spiral inductor, compatible with a large static magnetic field as encountered in a typical tracking detector. The output noise is about 50 mV (see work by S. Dhawan, for example [39])

Another technique utilizes charge pumps, illustrated in Fig. 10. In the first phase, the primary supply voltage V_{in} charges n capacitances C in series, depositing the charge $Q = CV_{in}/n$ on each capacitor. In the next phase all capacitors are connected in parallel, yielding the voltage V_{in}/n and the charge $Q_o = CV_{in}$. When switching occurs at a

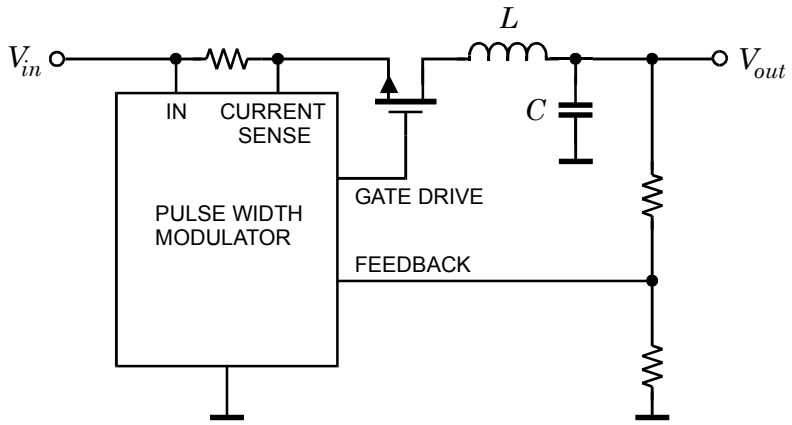

Fig. 9. Voltage conversion by pulse width modulation varies the duty cycle of the series transistor to maintain the charge on the output capacitor. The *LC* filter smoothes the pulsed output voltage.

frequency *f*, the available current is $fQ_o = fCV_{in}$. The switching frequency is limited by the charge and discharge time constants due to the on-resistance of the switching transistors and by the digital switching power C_iV^2 required to drive the transistors. Reducing the on-resistance by increasing the width of the MOS switching transistors also increases the transistors' input capacitance C_i, so the switching frequency cannot be increased arbitrarily. Although conceptually simple, the practical implementation is quite a bit more complicated, as shown in Fig. 11 [40]. Parasitic capacitances and resistances further reduce efficiency, so for an input voltage of 12.4 V and an output voltage of 2.23 V the simulations predict an efficiency of 65% with a 2 MHz clock and 57% with a 5 MHz clock.

The charge pump should have lower noise than a pulse width regulator, but both schemes will generate switching noise in a frequency band where the front-end electronics are sensitive. Since low-power input amplifiers typically are quite sensitive to power supply

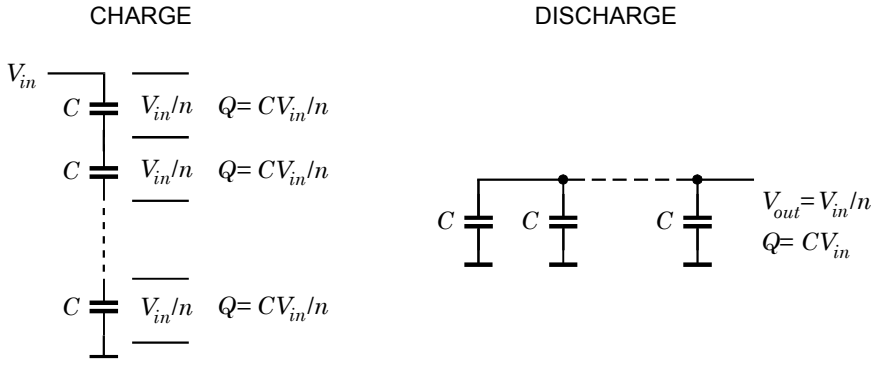

Fig. 10. Principle of charge pump voltage conversion. Initially capacitors are charged while connected in series. Then they are connected in parallel to provide a lower voltage at higher current.

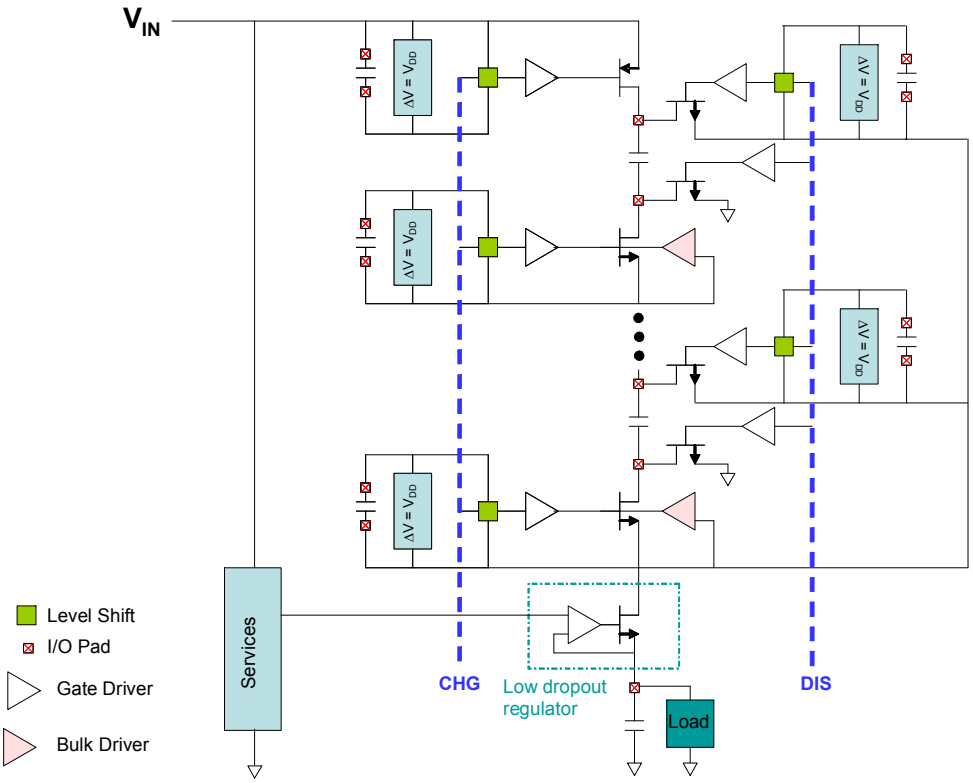

Fig. 11. Practical implementation of a charge pump circuit. (Figure courtesy of Peter Denes)

noise (they commonly exhibit a net gain for a signal injected at the power supply), alternative circuit designs and local filtering will be necessary. Voltage regulators typically are not effective at MHz frequencies.

6.3 Switched power

The proposed beam bunch structure at the ILC consists of a train of pulses with 337 ns spacing in a train of about 1 ms duration. About 200 ms elapse until the next bunch train, so the front-end electronics can be switched off to reduce the average power. This typically requires that the internal bias circuitry be specially designed to provide sufficiently fast response. Fig. 12 shows measured results on a low-noise strip detector IC with 1.2 μs shaping time, demonstrating a recovery time of 1 ms, so a roughly 100-fold reduction in power should be feasible [41].

7. Trigger Systems

The interaction rate in typical collider experiments does not allow all data to be read out, so trigger systems are used to apply filters that enhance the ratio of desired events to background events and reduce the readout rate to manageable levels. Fig. 13 shows the ATLAS trigger system as an example. Overall throughput is bounded at both the input, the data transmission bandwidth from the detector, which is limited by power

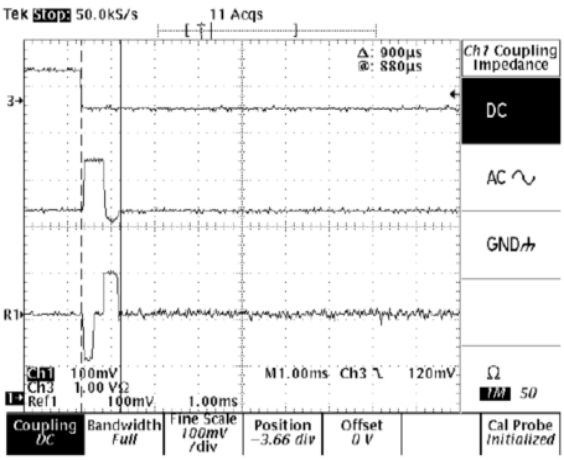

Fig. 12. Response (bottom trace) of a charge-sensitive amplifier and pulse shaper to power switching. The shaping time is 1.2 μs. (Figure courtesy of Bruce Schumm)

considerations, and the output, limited by the storage media. The intermediate rates are a compromise to match these two end conditions, which means that the efficiency for desired events can be severely compromised. Increasing the processing speed for complex events can substantially increase the yield. The second panel of Fig. 13 introduces a specialized hardware track finder, as implemented in CDF [42, 43]. The result of a lengthy design and optimization process, this unit increases the acquisition rate of events requiring B tagging or similar event topologies by roughly an order of magnitude. This has enabled physics analyses that in the conventional scheme would require a much higher integrated luminosity.

Field programmable gate arrays (FPGAs) are key components in this implementation. Currently, the processing power of FPGAs is increasing at a significantly faster rate than general purpose CPUs, so we should expect trigger and readout systems to be augmented by more powerful hardware processors in the future. For example, in the ATLAS pixel readout, the readout boards (RODs) that handle DAQ, trigger forwarding, and event building utilize 12 FPGAs and 5 DSPs. In a design study that includes the increased buffering required at sLHC, 5 new generation FPGAs replace the 12 FPGAs, 1 DSP, 5 FIFOs, and a significant amount of "glue" logic, while greatly simplifying the data path and providing a more than 4-fold increase in data rate. The circuit area can be reduced by about 75% with a significant reduction in power dissipation [44].

8. Superconducting bolometer arrays

Cosmology and high energy physics are becoming increasingly intertwined. The final example of advanced readout technology uses a different technology in a different application from the previous discussions, imaging the Cosmic Microwave Background (CMB) in experimental cosmology. The universe is permeated by background radiation from the Big Bang, today at 2.7 K. The CMB shows anisotropies at the 10^{-5} level, which

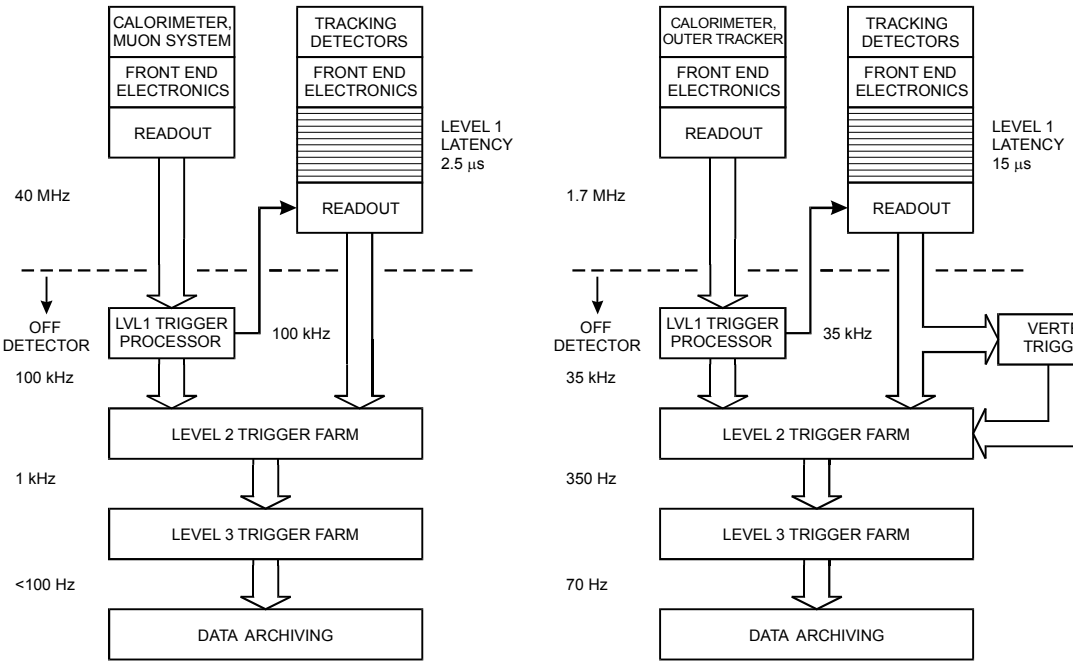

Fig. 13. ATLAS trigger layout (left) and the CDF trigger with a high-speed track-finding processor.

are the seeds of matter formation, in turn leading to stars and galaxies. The angular scale of the temperature distribution, the CMB power spectrum, shows multiple peaks, which provide information on the geometry of the universe (from the CMB we know that the universe is "flat"), the baryon density, and other fundamental cosmological parameters. A concise summary of modern cosmology and the CMB is given in the Review of Particle Physics [45].

The past two decades have greatly increased our understanding of the universe, but have also shown that dark matter and dark energy – neither of which we understand – comprise 95% of the universe. The first indications of dark energy came from supernova measurements, but only the combination of analyses of the CMB power spectrum and large scale structure, i.e. the spatial distribution of massive stellar objects vs. time, have narrowed the parameter space of matter and energy density. Today the CMB is very well understood and deviations from the "normal" distribution are used as a tool. One example is the Sunyaev-Zel'dovich (SZ) effect, where CMB photons traversing the hot gas in the core of galaxy clusters are shifted to higher energies through inverse Compton scattering. Thus, a measurement at the frequency of maximum power of the CMB (~ 200 GHz) will show a power deficit when viewing a galaxy cluster. Galaxy clusters are the most massive objects in the universe, so tracking their evolution constrains key cosmological parameters. This requires high sensitivity at large distances (redshift >1). Unlike optical or x-ray measurements, the SZ signal is independent of redshift, as the higher temperature of the CMB in the early universe compensates for the distance dependence.

The CMB power peaks at about 200 GHz. The signal can be detected either directly in sensors that convert the absorbed thermal power into an electrical signal (bolometers), or

via antennas coupled though transmission lines to load resistors, which in turn heat bolometers. Today, bolometers operating at sub-Kelvin temperatures are sufficiently sensitive that signal fluctuations are dominated by the shot noise of the CMB photons. However, future experiments require orders of magnitude improvements in sensitivity. Sensitivity can be increased by extending the measurement time and by performing many measurements simultaneously, which brings us to array technology.

In the past bolometers have been hand-crafted and difficult to operate. However, recent developments have changed this picture and brought large-scale bolometer arrays to the realm of practicality [46]. The bolometers used in the detectors discussed here are superconducting transition-edge sensors (TES), where a thin superconducting film is electrically biased, so its temperature is at the transition from the superconducting to normal state. This operating point provides a large change in resistance for a small change in temperature. Since the slope of the transition is finite, measuring the change in resistance yields the absorbed power.

The first key development is the insight that biasing the TES at constant voltage, rather than constant current, introduces electro-thermal negative feedback [47, 48]. Analogously to amplifiers, this speeds up the response, stabilizes the operating point, and provides a well-defined responsivity (output signal vs. absorbed power). Sufficiently strong electro-thermal negative feedback yields constant power vs. bias, so a change in incident power ΔP must be balanced by an equal change in bias power. For constant voltage bias V_b the change in bias current $\Delta I_b = \Delta P / V_b$. Stable operating points and well-defined response are both key ingredients for the practical operation of large arrays.

The second key development is that bolometers can be fabricated using photolithographic fabrication techniques for silicon ICs and micro-mechanics [49, 50]. This allows wafer-scale fabrication of bolometer arrays. Fig. 14 shows a comparison of the 16-bolometer array flown in the balloon experiment MAXIMA [51] and the 960-bolometer array

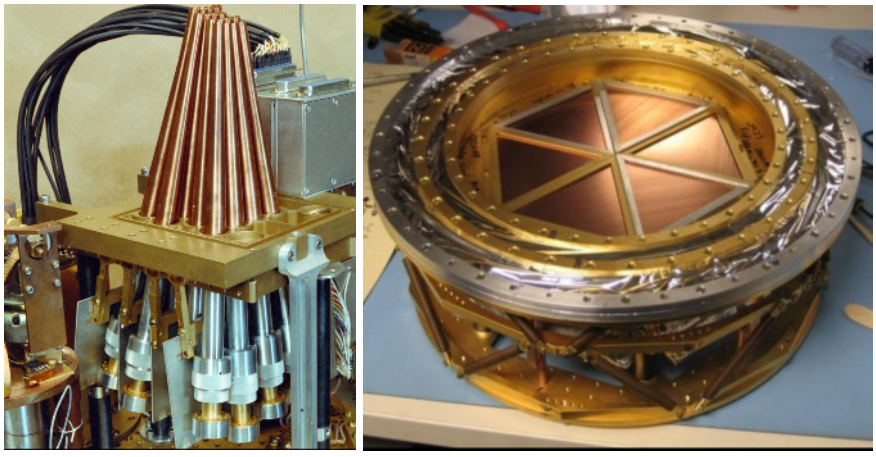

Fig. 14. Comparison between the 16-bolometer MAXIMA and the 960-bolometer SPT focal plane (the hexagonal object in the center) mounted in a part of the dewar. The SPT focal plane is about 15 cm in diameter.

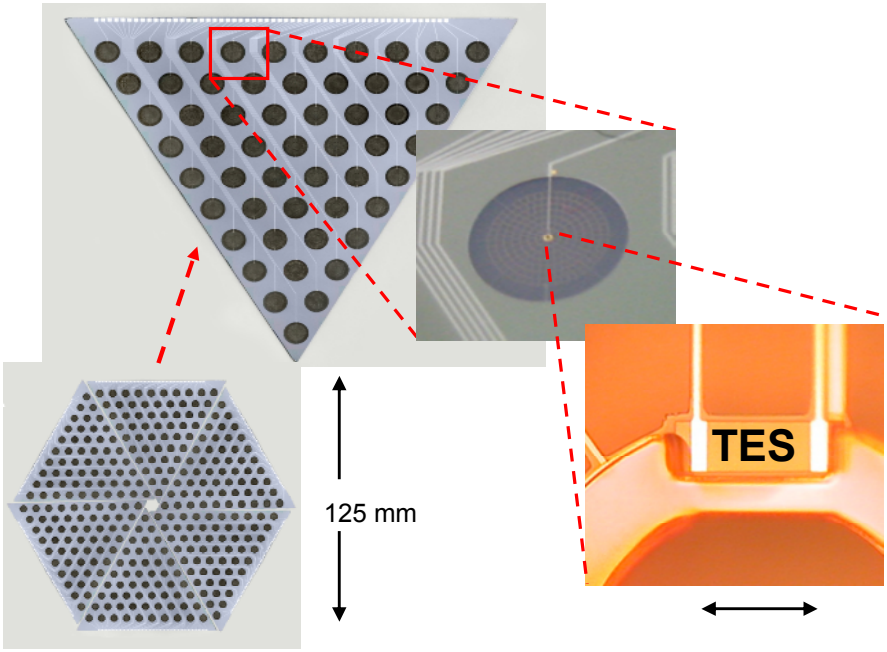

Fig. 15. A complete focal plane (lower left), wedge (upper left), individual pixel (intermediate), and a bolometer (lower right). The indicated width of the bolometer (TES) is 50 μm.

signal is uniquely placed in frequency space. Each bolometer is biased at a different frequency, so we can sum the currents from all bolometers and read them out through a single readout line. Frequency-selective demodulators separate the signals in the warm electronics. Fig. 16 shows the multiplexer circuit, which also shows how the bias frequencies can be fed through a single line. Tuned circuits associated with each

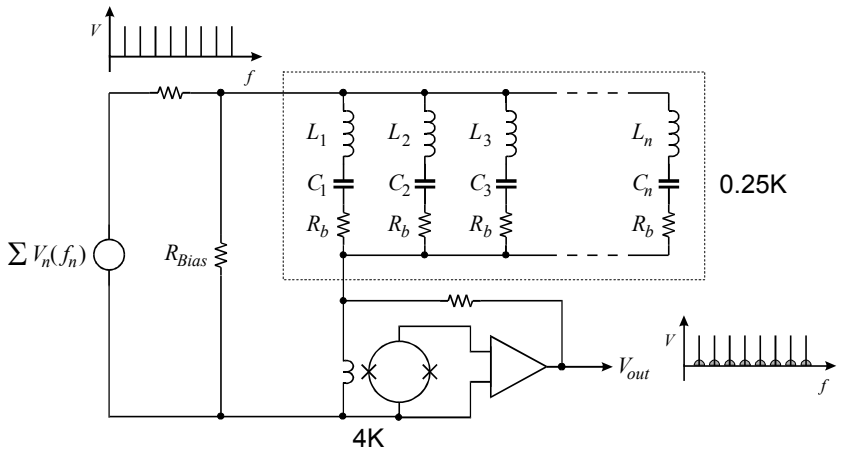

Fig. 16. In the cryogenic multiplexer the bolometers R_b are combined with series LC circuits and connected in parallel. The bias frequencies are applied as a "comb" and the series tuned circuits select the appropriate bias frequency. The currents from all bolometer legs are summed and sent through a single wire to the SQUID readout amplifier, whose output consists of the frequency comb with the signals from each bolometer uniquely associated with its bias frequency.

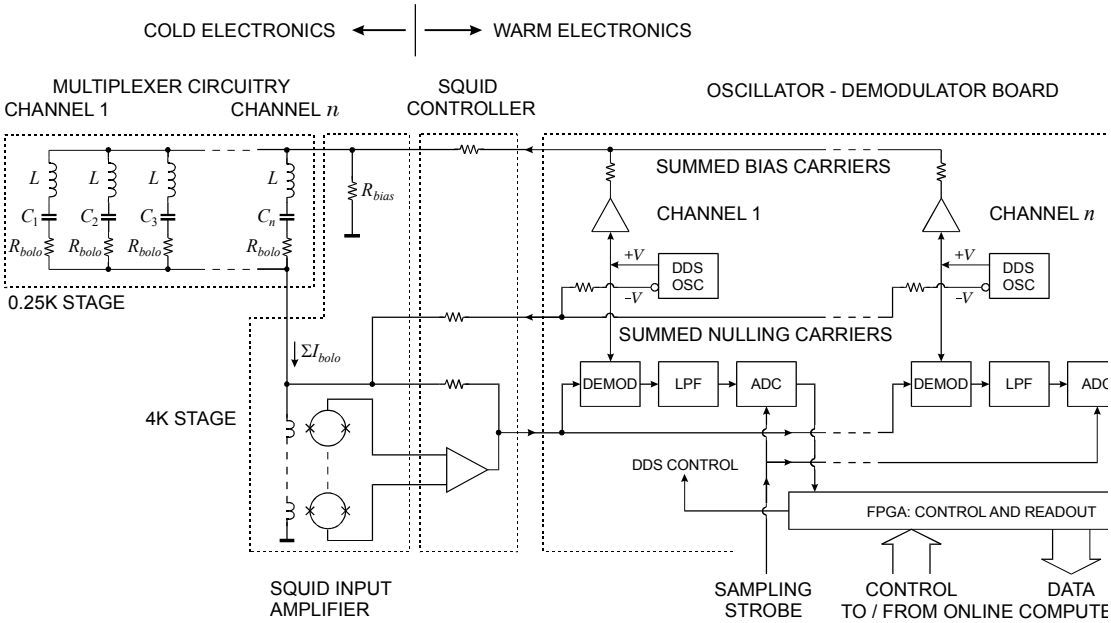

Fig. 17. The system block diagram shows the multiplexer circuitry on the 0.25K stage, the SQUID amplifier input at 4K, and the SQUID controller and readout-demodulator board at room temperature. Each channel of the oscillator-demodulator board serves one bolometer and includes a demodulator post-detection filter, and DDS that provides the bolometer bias and carrier nulling signal. The signals are digitized on board and transmitted to a PC for data storage.

bolometer "steer" each bias frequency to its designated bolometer. The bandwidth of the tuned circuits determines the cross-talk between channels and also limits the noise bandwidth to reduce the contribution of wideband Johnson noise from a given bolometer to the other channels. The summing amplifier utilizes a SQUID in the input stage at 4 K, operated with shunt feedback to provide a low input impedance of ~10 mΩ. Only two wires are needed per multiplexed array.

Fig. 17 shows the block diagram of the complete readout. The bias frequencies are generated by direct digital synthesis (DDS) ICs, which provide programmable precision frequency control, excellent amplitude stability, and very low sideband noise close to the carrier. Since the SQUID's output voltage is periodic in input current [56], the maximum signal is limited. The shunt feedback extends the dynamic range, but since the carrier levels are $10^5 - 10^6$ times the TES noise levels, additional techniques are necessary. In an amplitude modulated signal all of the information is in the sidebands, i.e. the carrier amplitude is constant, so the carrier can be suppressed without loss of information. This is performed by inverting the bias signal and applying it directly to the input of the SQUID summing amplifier. After demodulation the bandwidth of each individual channel is determined by a post-detection filter with a cutoff of 400 Hz. Signals are digitized to 14 bit resolution at 1 kHz intervals and data transferred to a PC. Current systems multiplex 8 bolometers, but extension to 32 bolometers appears to be practical, primarily limited by the bandwidth of the SQUID readout amplifier. Each readout board

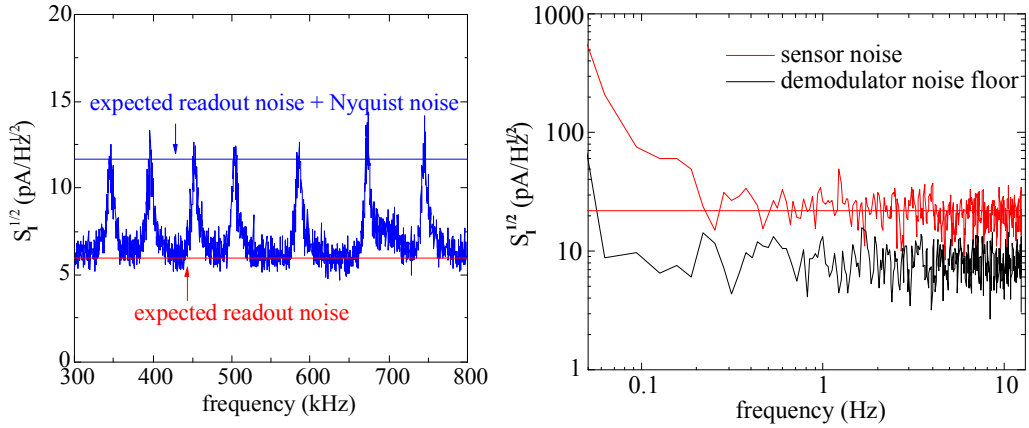

Fig. 18. Measured noise for multiple bolometer channels (left), in agreement with theoretical predictions. The "bump" at 700 kHz is from a low-Q resistor dummy channel. The electronic noise spectrum per channel (right) is flat down to 0.1 Hz.

serves 16 bolometers. All bolometer and SQUID operating parameters are computer controlled. Readout systems for over 2000 channels have been fabricated and are in use at SPT and APEX. A fully digital readout is now under development that uses an FPGA to process 40 channels with more than an order of magnitude reduction in power.

In scanning the telescope across a point source the signal amplitude changes very slowly, so the measured signal spectrum extends to well below 1 Hz. Thus low-frequency noise performance is critical down to about 0.1 Hz. Fig. 18 shows the output spectrum at the output of the multiplexer and the noise spectrum of an individual channel [57]. Noise levels are in good agreement with theoretical expectations and the electronic noise is flat down to 0.1 Hz.

TES frequency-domain multiplexing has also been applied to x-ray detection [58], providing an important ingredient for increasing detection efficiency and rate capability. By their very nature, high-resolution bolometers are small, so they are not very effective detectors. Even with electrothermal feedback their decay times are of order μs, so their rate capability is limited. However, as in silicon strip and pixel arrays at the LHC, distributing the rate over many detector channels reduces the rate per channel, so large TES arrays can increase both the detection area and rate capability. The system described above has been adapted to handle the 50 kHz sampling rates required for detector arrays now under development [59].

The technology of superconducting bolometer arrays has made tremendous strides and is still progressing. Arrays with several hundred to a thousand bolometers are now in operation and designs for the next generation with thousands of pixels are well underway. Mapping the polarization of the CMB is one of the next challenges, as it could yield signatures of gravity waves emitted during the Big Bang and measure the energy scale of inflation. Monolithic arrays providing dual polarization measurements per pixel have been demonstrated [60] and full system designs are underway for practical experiments.

9. Conclusion

New technology has enabled significant progress in detector electronics, both in high energy physics and in cosmology. However, one shouldn't take the "miracles of modern technology" for granted. Circuit topologies for monolithically integrated detector front-end electronics have been extensively explored. As in the past, the development of efficient readout architectures and work on systems integration is crucial. This is not as glamorous as IC design, but must be supported more systematically than in the past. Enhancements in digital electronics will allow more powerful trigger processing that yields more interesting physics events for a given integrated luminosity. Instrumentation R&D continues to provide tremendous leverage in physics capabilities and is one of the most effective and important investments the scientific community can make.

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References

1. J.T. Walker et al., Nucl. Instr. and Meth. **A 226** (1984) 200
2. P. Seller, P. Allport, M. Tyndel, IEEE Trans. Nucl. Sci. **NS-35** (1988) 176 –180
3. W. Buttler et al. Nucl. Instr. and Meth. **A273** (1988) 778-783
4. S.A. Kleinfelder et al., IEEE Trans. Nucl. Sci. **NS-35** (1988) 171
5. C. Haber, Nucl. Instr. and Meth. **A471** (2001) 12-17. The SVXH uses the architecture described by T. Zimmerman et al., IEEE Trans. Nucl. Sci. **NS-42/4** (1995) 803-807.
6. M. Garcia-Sciveres et al., Nucl. Instr. and Meth. **A435** (1999) 58-64
7. O. Toker et al., Nucl. Instr. and Meth. **A340** (1994) 572-579
8. M.J. French et al., Nucl. Instr. and Meth. **A466** (2001)359-365
9. H. Spieler, *Semiconductor Detector Systems*, Oxford university Press, Oxford (2005), 0-19-852784-5, TK9180 .S68 2005
10. E. Spencer et al., IEEE Trans. Nucl. Sci. **NS-42/4** (1995) 796-802
11. I. Kipnis, H. Spieler and T. Collins, IEEE Trans. Nucl. Sci. **NS-41/4** (1994) 1095-1103 (CAFE-M predecessor with very similar characteristics)
12. F. Campabadal et al., Nucl. Instr. and Meth. **A552** (2005) 292-328
13. I. Kipnis et al., IEEE Trans. Nucl. Sci. **NS-44/3** (1997) 289-297
14. L. Baldini et al., IEEE Trans. Nucl. Sci. **NS-53/2** (2006) 466
15. W.J. Snoeys, IEEE Trans. Nucl. Sci. **NS-49/4** (2002) 1829
16. M. Campbell et al., IEEE Trans. Nucl. Sci. **NS-46/3** (1999) 156-160
17. W. Snoeys et al., IEEE J. Solid State Circuits **35/12** (2000) 2018-2030
18. Grosse-Knetter et al., Nucl. Instr. and Meth. **A568** (2006) 252-257
19. P. Collins, Nucl. Instr. and Meth. **A581** (2007) 38-47
20. J. Baudot et al., Development of CMOS sensors for future high precision position sensitive detectors, http://vci.oeaw.ac.at/2007/program/Book_of_Abstracts.pdf, p. 40
21. G. Traversi et al., Nucl. Instr. and Meth. **A581** (2007) 291-294
22. A. Gabrielli, Nucl. Instr. and Meth. **A581** (2007) 303-305

23. L. Servoli et al., Nucl. Instr. and Meth. **A581** (2007) 335-338
24. Y. Arai et al., SNIC-2006-0016, SLAC-PUB-12079, http://www.slac.stanford.edu/econf/C0604032/papers/0016.PDF and H. Ikeda et al., Nucl. Instr. and Meth. **A579** (2007) 701-705, Y. Ikegami et al. Nucl. Instr. and Meth. **A579** (2007) 706-711
25. T. Tsuboyama et al., http://vci.oeaw.ac.at/2007/program/Book_of_Abstracts.pdf, p. 42
26. R. Yarema, Proceedings of the 12th Workshop on Electronics For LHC and Future Experiments LECC 2006, http://doc.cern.ch/yellowrep/2007/2007-001/p71.pdf and R. Lipton, Nucl. Instr. and Meth. **A579** (2007) 690-694
27. S. Parker et al., Nucl. Instr. and Meth. **A395** (1997) 328-343, C. Da Via et al. Nucl. Instr. and Meth. **A509** (2003) 86-91
28. J. Metcalf et al., Nucl. Instr. and Meth. **A579** (2007) 833-838
29. R. Bates, **A581** (2007) 314-317
30. G. Kramberger et al., Nucl. Instr. and Meth. **A481** (2002) 297-305
31. O. Krasel et al., IEEE Trans. Nucl. Sci. **NS-51/6** (2004) 3055-3062
32. H. Spieler, *Semiconductor Detector Systems*, Oxford university Press, Oxford (2005), pp. 71-82
33. S. Eckert et al., Nucl. Instr. and Meth. **A581** (2007) 322-325
34. H. Spieler, Nucl. Instr. and Meth. **A531** (2004) and H. Spieler, *Semiconductor Detector Systems*, Oxford university Press, Oxford (2005), pp. 266-275
35. T. Stockmanns et al., IEEE Trans. Nucl. Sci. **NS-52** (2005) 2721-2725
36. Duc Bao Ta et al., Nucl. Instr. and Meth. **A557** (2006) 445-459
37. M. Weber et al., Nucl. Instr. and Meth. **A579** (2007) 844-847
38. C. Haber, presentation at ATLAS Tracker Upgrade Workshop, Liverpool, Dec. 6-8, 2006, http://indico.cern.ch/conferenceDisplay.py?confId=a063014
39. S. Dhawan, presentation at ATLAS Tracker Upgrade Workshop, Liverpool, Dec. 6-8, 2006, http://indico.cern.ch/conferenceDisplay.py?confId=a063014
40. P. Denes, LBNL, private communication
41. B. Schumm, UCSC, private communication
42. B. Ashmanskas et al., Nucl. Instr. and Meth. A518 (2004) 532-536; originally proposed by M. Dell'Orso and L. Ristori, Nucl. Instr. and Meth. A78 (1989) 436-440
43. A. Abulencia et al. , Nucl. Instr. and Meth. **A581** (2007) 482-484
44. J. Joseph, LBNL, private communication
45. *Review of Particle Physics*, J. Phys. G : Nucl. Part. Phys. **33** (2006) 210-244
46. A.T. Lee et al., Voltage-Biased TES Bolometers for the Far-Infrared to Millimeter Wavelength Range, in Proceedings Far-IR, Sub-mm & mm Detector Technology Workshop, Wolf J., Farhoomand J. and McCreight C.R. (eds.), NASA/CP-211408, 2002 and at http://www.sofia.usra.edu/det_workshop/papers/manuscript_session5.html
47. K.D. Irwin, Appl. Phys. Lett. **66** (1995) 1998-2000
48. A.T. Lee et al., Appl. Phys. Lett. **69** (1996) 1801
49. J.M. Gildemeister, Adrian T. Lee, P.L. Richards, Appl. Phys. Lett. **74** (1999) 868
50. J.M. Gildemeister, Adrian T. Lee, P.L. Richards, Appl. Phys. Lett., **77** (2000) 4040
51. S. Hanany et al., Astrophysical Journal Letters. **545** (2000) L5-L9

52. J.E. Ruhl, et al., The South Pole Telescope. in *Millimeter and Submillimeter Detectors for Astronomy*. eds. J. Zmuidzinas, W. Holland, and S. Withington. Proc. SPIE **5498** (2004) 11-29
53. J.A. Chervenak et al., Appl. Phys. Lett. **74** (1999) 4043-4045
54. H. Spieler, Frequency Domain Multiplexing for Large-Scale Bolometer Arrays, in Proceedings Far-IR, Sub-mm & mm Detector Technology Workshop, Wolf J., Farhoomand J. and McCreight C.R. (eds.), NASA/CP-211408, 2002, LBNL-49993 and at http://www.sofia.usra.edu/det_workshop/papers/manuscript_session5.html
55. T.M. Lanting et al., IEEE Trans. Appl. Superconductivity **13/2** (2003) 626-629
56. J. Clarke and A.I. Braginski, The SQUID Handbook Vol 1, Wiley-VCH, Weinheim 2004, ISBN 3-527-40229-2
57. T.M. Lanting, et al. Appl. Phys. Lett. **86** (2005) 112511-1 ... 3
58. J. N. Ullom et al., IEEE Trans. Appl. Superconductivity **13/2** (2003) 643-648
59. J. Dreyer et al., IEEE Transactions on Applied Superconductivity **17** (2007) 633-636
60. M.J. Myers, et al., Appl. Phys. Lett. **86** (2005) 114103-1 ... 3