UNIVERSITY OF CALIFORNIA SAN DIEGO

Topologies, Modeling, and Control of Hybrid Switched-Capacitor Converters

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor Tse Nga Ng

2022

The Dissertation of Ratul Das is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2022

DEDICATION

This thesis is dedicated to my undergraduate thesis supervisor late Dr. Kazi Mujibur Rahman. He taught me how to think like an engineer.

EPIGRAPH

It doesn't matter how beautiful your theory is,
it doesn't matter how smart you are.
If it doesn't agree with the experiment,
it's wrong.

Richard Feynman

The saddest aspect of life right now is that
gathers knowledge faster than society gathers wisdom.

Isaac Asimov

The good thing about science is that
it's true whether or not you believe in it.

Neil deGrasse Tyson

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PREFACE

I tried to perform contemporary research works primarily from my curiosity and partly from the pressure of project delivery. Most of the works are already published. There are also some works I did not get chances to publish. This thesis contains both types of materials. I hope this thesis will help future power electronics enthusiasts in some parts of their research and work.

ACKNOWLEDGEMENTS

I acknowledge my supervisor and mentor, Professor Hanh-Phuc Le, for his immeasurable support throughout my Ph.D. journey. From answering my novice questions to guiding me in unfolding a very complex concept, he always had time for me. He patiently made me go through the steps of problem-solving. The occasions we spent on whiteboards and blank papers coming up with new topologies are my happiest memories of the last five and a half years. Whenever I asked for new instruments for even a tiny experiment, he never said no and always managed to provide me. Even when I asked for help at 2 am in the night to help me with experiments and writing papers, he was always there. I never said this to him, but he was always like an elder brother to me. I am grateful that I got Professor Le as my supervisor. He believed in me when nobody else did. He was with me in all my academic rejections and acceptances.

I also acknowledge Professor Dragan Maksimović of the University of Colorado Boulder. I had the luckiest opportunity to take his classes and occasionally directly learn from him. He was one of the motivations for my shooting for a Ph.D. degree.

I also want to thank Professor Khurram Afridi of Cornell University. His lessons on different topics of Power Electronics at CU Boulder were very helpful to me.

I had very little interaction with Professor Robert Ericson. However, it was an honor for me to be a member of the Colorado Power Electronics Center (CoPEC) at CU Boulder, which Professor Ericson and Maksimovic lead. 'Fundamentals of Power Electronics' has helped me and many other students and engineers to perform their work.

I had to leave CoPEC early as the situation demanded. I have always felt close to CoPEC from my heart. All my colleagues at CoPEC are also a significant part of my PhD journey. Fang Zhang, Ashish Kumar, Saad Parveiz, Prashanta Achanta, Jianglin Zhu, and Vivek Sangkaranarayan, were fantastic as my seniors. Whenever I reached out to them for the slightest help, they stepped in immediately. Ashish was my mentor during my internship at Texas Instruments Inc. where he guided me with his charismatic problem-solving skill and sharp humor.

Mausamjeet Khatua, Yucheng Gao, Kyle Goodrick and Danish Shehzad were my friends in CoPEC. The pressure of my first year of Ph.D. was relieved many times when we shared our happiness and sorrows. It was a pity that my path separated from others within two years. Their friendship was one of the most valuable things I achieved after coming to the USA.

I also learned much from Satyaki Mukherjee, Janko Cellikovic, and Branko Majnumovic. Talking, listening, and learning from them helped me solve many of my problems.

I also want to thank my internship manager at Texas Instruments Inc. (TI), Yogesh Ramadass, for his calm support and guidance. My colleagues at TI, Sombuddha Chakraborty, Ashish Kumar, Ujwal Radhakrishna, Maruthi Mukkannaiah, and Junmin Jiang, made my time at TI so eventful that I will always consider it one of my best times in life.

Throughout the move from Colorado to California and changing schools, the only constant people in my life were Casey Hardy and Tianshi Roger Xie. Without Casey's help in research and lessons about USA life, I couldn't survive in this foreign country. Whenever I asked for help from Casey, he not only advised me of the current problems, he advised me according to his projection on problems that I may face later. It was a blessing for me to get an experienced senior like Casey. I also got Roger's help in many projects, from software usage to FPGA programming.

Tirthasarathi Lodh joined our group later. As we are of the same mother tongue, my life at UCSD got many colors when I had him as my labmate. We spent hours talking about many life problems and studies in our language. Without Tirtha's help, I could not commute between Los Angeles and San Diego during the last year of my Ph.D. I gratefully thank him for that.

I am thankful to our other group members, Hieu Pham, Saket Jha, and Po-Han Chen. I enjoyed the occasional talks with Saket about various experiments. I also had mentees Ashwini Wankhede, Jacob Lopez, Ryan Tran, and Zhiheng Luo at different times in my Ph.D. Mentoring them was one of the significant achievements of my Ph.D.

I am forever grateful to all the group members of our iPower3Es. Discussions with them made me solve and understand many problems better. Whenever I could make these brilliant

people understand, I always felt confident about my research topics. Whenever I failed, I realized I needed to come up with either a new perspective or my understanding was incorrect. I loved to present in front of these people.

Rahat Ibn Rafiq, Romena Yasmin, Mohammad Al-Amin, and Ashrafunnahar Asha were so welcoming in Boulder that I never felt away from home. Having Rahat as my first roommate was a blessing. We had meals at Al-Amin Vai and Asha Apu's house countless times. All their help made my Colorado life fun, eventful, and lively.

Abu Raihan, Siam Umar Hussain, and Hasan Imam made my stay in San Diego more enjoyable. Thank them for their help, companionship, and family time.

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I see myself as an extended part of my family. Whatever achievements I had in my life, it is my family whose little and big sacrifices were behind. My parents supported me in every aspect of my life. They provided me with all the things within their reach. Their moral views and education are shaping my whole life. My brother had a significant impact on my character, my education, and my career path. I am grateful to my brother and sister-in-law for looking after my parents while I am busy with my academic ventures.

At last, I want to mention my former classmate and labmate, currently my wife, Baishakhi Rani Biswas. She was with me during my bad times. She is still with me, and I can only hope I will have the most incredible luck in the world to have her for the rest of my life. Not only could she calm me during my bad times, but it was also a blessing to get such a brilliant person as my life partner.

This dissertation includes quite a few published conference and journal papers. I am grateful to all the unknown reviewers and editors for their contributions.

Chapter 2, in full, is a reprint of the material as it appears in "Analysis of Dual-Inductor Hybrid Converters for Extreme Conversion Ratios," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 5, pp. 5249-5260, Oct. 2021 by the authors Das, Ratul; Seo, Gab-Su and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 3, in full, is a reprint of the material as it appears in "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 25-29 by the authors Das, Ratul; Seo, Gab-Su; Maksimovic, Dragan and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 4, in full, is a reprint of the material as it appears in "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 1997-2001 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 5, contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Chapter 6, in full, is a reprint of the material as it appears in "Gate Driver Circuits With Discrete Components for GaN-Based Multilevel Multi-Inductor Hybrid Converter," in IEEE Transactions on Industrial Electronics, vol. 70, no. 2, pp. 1105-1114, Feb. 2023 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 7, in partial, is a reprint of the material as it appears in "Demystifying Capacitor Voltages and Inductor Currents in Hybrid Converters," in 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8 by the authors Das, Ratul; Celikovic,

Janko; Abedinpour, Siamak; Mercer, Mark; Maksimovic, Dragan and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 8, in full, is a reprint of the material as it appears in "An Accurate Approach to Calculate and Measure Capacitor Voltage and Inductor Current Levels in Hybrid Converters," in 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021, pp. 1-5 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 9, in full, is a reprint of the material as it appears in "Analysis of Capacitor Voltage Imbalance in Hybrid Converters and Inherently Balanced Operation Using Symmetric Architecture," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 3, no. 4, pp. 1205-1209, Oct. 2022 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

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Chapter 11, in full, is a reprint of the archived unpublished materials in "Two-Stage Power Delivery Architecture Using Hybrid Converters for Data Centers and Telecommunication Systems," in TechRxiv.org by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 12, in full, is a reprint of the material as it appears in "Modular Hybrid Step-Down PFC Converter for Direct AC/DC Conversion with Differential Power Processing in Data Centers," in 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 2219-2223 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the

primary investigator and author of this paper.

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Chapter 14, in full, is a reprint of the accepted materials in "Multi-Inductor Multi-Output Hybrid (MiMoH) Converter for Large Conversion Ratio and Multiple Outputs," in 2023 Applied Power Electronics Conference and Exposition (APEC), 2023 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Appendix A contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix B contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix C contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

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Appendix E contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

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Appendix I contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix J contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

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PUBLICATIONS

1. R. Das and H. -P. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 1997-2001, doi: 10.1109/APEC.2019.8722246.

2. R. Das, G. -S. Seo and H. -P. Le, "A 120V-to-1.8V 91.5%-Efficient 36-W Dual-Inductor Hybrid Converter with Natural Soft-charging Operations for Direct Extreme Conversion Ratios," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 1266-1271, doi: 10.1109/ECCE.2018.8557854.

3. T. Xie, R. Das, G. -S. Seo, D. Maksimovic and H. -P. Le, "Multiphase Control for Robust and Complete Soft-charging Operation of Dual Inductor Hybrid Converter," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 1-5, doi: 10.1109/APEC.2019.8721951.

4. R. Das, G. -S. Seo, D. Maksimovic and H. -P. Le, "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 25-29, doi: 10.1109/APEC.2019.8721952.

5. R. Das, J. Celikovic, S. Abedinpour, M. Mercer, D. Maksimovic and H. -P. Le, "Demystifying Capacitor Voltages and Inductor Currents in Hybrid Converters," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8, doi: 10.1109/COMPEL.2019.8769722.

6. J. Celikovic, R. Das, H. -P. Le and D. Maksimovic, "Modeling of Capacitor Voltage Imbalance in Flying Capacitor Multilevel DC-DC Converters," 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8, doi: 10.1109/COMPEL.2019.8769615.

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9. R. Das and H. -P. Le, "Modular Isolated Vertically Symmetric Dual Inductor Hybrid Converter For Differential Power Processing," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 2439-2443, doi: 10.1109/ECCE47101.2021.9595908.

10. R. Das and H. -P. Le, "Modular Hybrid Step-Down PFC Converter for Direct AC/DC Conversion with Differential Power Processing in Data Centers," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 2219-2223, doi: 10.1109/ECCE47101.2021.9595934.

11. R. Das and H. -P. Le, "An Accurate Approach to Calculate and Measure Capacitor Voltage and Inductor Current Levels in Hybrid Converters," 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021, pp. 1-5, doi: 10.1109/COMPEL52922.2021.9645991.

12. R. Das and H. -P. Le, "Gate Driver Circuits With Discrete Components for GaN-Based Multilevel Multi-Inductor Hybrid Converter," in IEEE Transactions on Industrial Electronics, vol. 70, no. 2, pp. 1105-1114, Feb. 2023, doi: 10.1109/TIE.2022.3158014.

13. R. Das and H. -P. Le, "Analysis of Capacitor Voltage Imbalance in Hybrid Converters and Inherently Balanced Operation Using Symmetric Architecture," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, 2022, doi: 10.1109/JESTIE.2022.3189572.

14. R. Das and H. -P. Le, "Multi-Inductor Multi-Output Hybrid (MiMoH) Converter for Large Conversion Ratio and Multiple Outputs," accepted for publication in 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), 2023.

FIELDS OF STUDY

Major Field: Electrical Engineering (Electronic Circuits and Systems)

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ABSTRACT OF THE DISSERTATION

Topologies, Modeling, and Control of Hybrid Switched-Capacitor Converters

by

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Professor Hanh-Phuc Le, Chair

This dissertation explored the ideas and concepts for hybrid switched capacitor converter topologies and new power delivery architectures to provide viable solutions for high conversion ratio DC-DC and AC-DC applications.

A new Multi Inductor Hybrid (MIH) Converter family for high conversion ratio DC-DC applications has been synthesized and analyzed to provide non-isolated DC-DC conversions with large voltage conversion ratios efficiently. The highlight of this converter family is a 6-level 6-phase 6-inductor MPMIH converter, which achieved 90.7% peak efficiency with a load range of 0-220A at 1V and $>$1kA/in^3 density.

A new modeling method reveals that all odd-level Flying Capacitor Multi-Level convert-

ers become current sources with non-ideal timing while the even-level converters stay as voltage sources. A method for identifying unbalanced hybrid converters is also provided.

This dissertation demonstrates a two-stage power delivery architecture to bridge AC distribution voltages to core levels for computing loads in data centers. In combination, direct conversion from ~110 VAC to 1VDC achieves a peak efficiency of 84.1% while providing output currents up to 160A.

Partial power processing for AC/DC applications has been explored with a switched-capacitor (SC) based hybrid step-down converter and its new control techniques. The operation with multiple modules is verified with a 115VAC-to-48VDC conversion and 200VAC input to two 48VDC outputs.

A new modular isolated DC-DC converter is proposed and demonstrated for point-pf-load (POL) applications with partial power processing. A prototype of the modular architecture has been demonstrated for a 100V-to-3V point-of-load conversion with a maximum load of 60A. The peak efficiency of 91% is achieved at 57W/20A output.

A new multi-inductor multi-output hybrid converter is also proposed and demonstrated. The MiMoH converter prototype has been implemented to demonstrate conversion from a 24-48V input voltage to three individually regulated outputs ranging from 1.2V to 2.2V. The converter prototype achieves 40W peak power and 91.8% peak efficiency.

The topologies presented in this dissertation, corroborated with control and modeling techniques, demonstrated superior performance, natural balancing ability, and relatively easy controllability, making them excellent candidates for more compact and efficient system design.

Chapter 1

Introduction

Many industrial and household devices today receive power from AC power distribution lines, while most are DC loads by nature. These DC loads have increased quickly, and their power requirements have become increasingly stringent in recent years. Modern data centers and telecommunications systems also fall into this category.

Monthly global mobile data traffic is expected to surpass 350 ExaBytes (EB) in 2027 from around 100 EB today, and merely ~2 EB in 2013 [1–3]. This exponential growth has put critical pressure on the telecommunication infrastructure, particularly on the architecture of power supply and distribution for this massive need. The electricity consumption in data centers is estimated to reach 321 TWh by 2030 [4]. The same study also shows that if the semiconductor device technology following Moore's law saturates and the number of Internet-of-Things (IoT) connected devices continues to grow at the same rate, the power consumption can reach 752 TWh which will be about 2.13% of the total energy available globally. To meet the increasing demand for higher power requirements, replicating the architecture in the current data centers' delivery setup would require the space needed for these systems to grow exponentially. The time has come to bring new ideas and concepts to refurbish the traditional power delivery architectures in data centers and renovate them with more compact and energy-efficient power converters.

The problems related to data centers are also common in many other applications. Thus, although the dissertation is themed based on the power delivery of data centers, and related

solutions are provided; they have long-ranging effects on other applications. For example, the discussions in this dissertation are also relevant for mobile, laptop, or even smart home applications. The next section describes the power delivery of the data center and telecommunication systems with the traditional and new architectures.

1.1 Power Delivery Architectures

The final loads in data centers and telecom infrastructures are high-performance processors that need a group of power converters to interface with AC distribution lines [5]. With the demand for modern data processing power, computation, and storage requirements, these processors have become excessively power-hungry, which has ultimately translated into extremely high loading current at low supply voltages of ~1V.

Conventionally, high-performance computing rack servers in data centers are powered from an AC grid through an isolation transformer, followed by an online uninterruptible power supply (UPS), and typically four stages [5, 6]: 1) A power factor correction (PFC) rectifier from the AC line voltage to high-voltage DC link bus, 2) the second stage converts the DC link to intermediate DC bus at 48 V nominally, 3) a 48V-to-12V high-efficiency DC-DC conversion, and 4) the last stage converts 12 V to core voltages of 0.8 V to 3.3 V. This architecture is shown in Fig. 1.1. Generally, isolation is required in only one stage from the grid to the core levels, and a high-power isolation transformer is used either before or after the UPS. As voltage conversion techniques in AC-DC and DC-DC applications are many times dependent on the transformers, transformers are also used in the last four stages, but they do not provide the safety-rated isolation required. The series connection of multiple stages also results in overall low power efficiency and density, leading to excessive heat, which requires bulky and expensive cooling systems. We are experiencing fast growth in data management and processing in recent days [3, 7]. Coupled with the introduction of 5G communications, artificial intelligence, cryptocurrency, and cloud-dependent data processing and computations, this power demand trend will

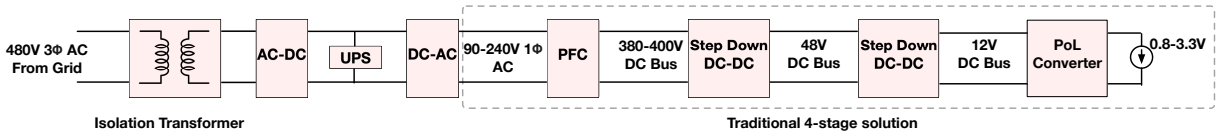
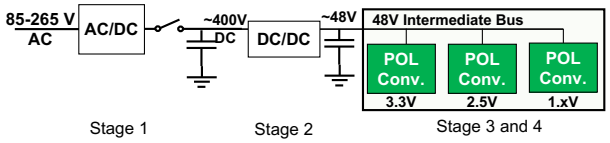
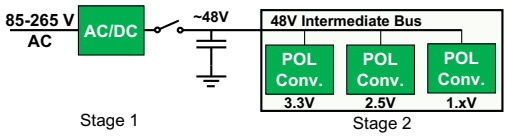


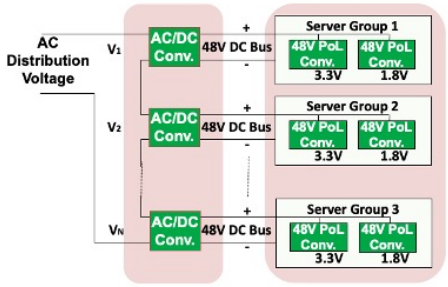
Figure 1.1. Traditional power delivery architecture



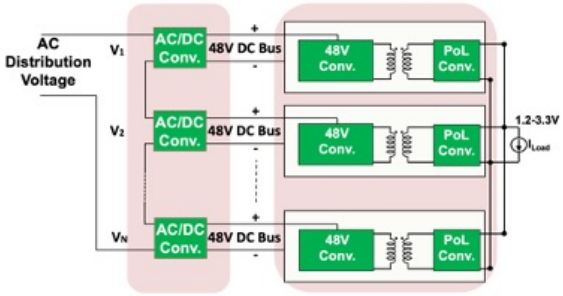
(a) Recent research trend merging last two stages



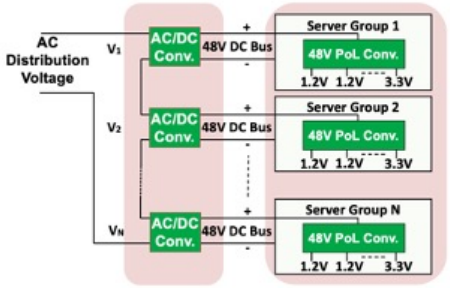
(b) Proposed power delivery architecture merging first two stages and last two stages



(c) Proposed power delivery architecture with distributed AC input voltage for differential power processing and distributed final loads using separate power converters



(d) Proposed power delivery architecture with distributed AC input voltage for differential power processing and common final load



(e) Proposed power delivery architecture with distributed AC input voltage for differential power processing and distributed groups of final loads using same power converter within the same group

Figure 1.2. Considered power delivery architectures in this dissertation

only get more challenging. As a result, the traditional multiple-stage power delivery architecture becomes a critical bottleneck of the system performance and cost and, thus, should be replaced with more advanced, optimized, and efficient ones.

This dissertation addresses the problem by proposing multiple power delivery architectures. In the conventional delivery architecture in Fig. 1.1, the 12V DC bus is the distribution bus. Assuming 400W as the final load, the power requirement of Intel Xeon Platinum 9282 Processor [8], even if the 12V PoL converter works at the theoretical no loss condition, it is required to deliver ~33A current from the 12V bus. This large amount of current from the distribution bus means a lot of conduction losses as well in the distribution path, even if there is a minimal equivalent series resistance (ESR) at the path. To overcome this, point-of-load (PoL) converters that can support large conversion ratios are desirable to reduce board-level distributions by lowering currents at a higher bus voltage. In recent research trends, 48V PoL converters are replacing conventional 2-stage 48V to 12V and 12V to PoL solutions [9] shown in Fig. 1.2a.

Last few years, there has been much research conducted on this last stage of power delivery, aka 48V PoL converters, and many solutions have been proposed. The other stages of the power delivery architecture were relatively less visited. However, the increasing requirement of the final loads is catching up even with the distribution currents from the 400V DC bus [10] and the AC bus preceding that. Projecting the future need in the future power delivery in the data centers, we propose the two-stage power delivery architecture combining AC to ~48V and 48V PoL stages. The proposed architecture is shown in Fig. 1.2b.

One very effective solution for the future data center is the partial power processing by distributing the 400V DC voltage in Fig. 1.1 over multiple PoL converters by connecting the inputs of the converters in series [10]. This solution can effectively improve the system design as individual PoL converters need to process smaller power; hence, they can be designed with higher power density and efficiency. However, this solution only comes after an AC-DC Power Factor Correction (PFC) stage. Differential power processing with the AC-DC PFC stage is

proposed and shown in Fig. 1.2c. The benefits of reduced voltage and superior system level operation like [10] can still be performed with a reduced number of stages in this architecture. With this architecture, each AC-DC converter connected in series generates separate ~48V buses. Each of these ~48V buses can be interfaced with separate PoL converters to serve a group of loads or, in this case, processors. Note that the separate loads in this architecture have separate ground nodes.

Iterating from the architecture shown in Fig. 1.2c, some implementations or applications may need just one big load to serve instead of separate distributed loads. However, the advantages of the reduced number of stages and AC-DC differential power processing may still be wanted for system-level optimization. Hence, isolated converters from each of the ~48V DC buses can be interfaced with isolated converters, and the secondary side of each can be paralleled together to serve the common load. Additionally, if necessary, the isolation barriers in these converters can be designed to provide safety-rated insulation. As these converters are at lower voltage levels, the overall transformers' design can be simplified to some extent to have a system-level compact design.

Modern processors have multiple cores for superior performance over broader computing needs. This is especially true for the processors in data centers. Each of these cores needs separate voltage rails for performing dynamic voltage, and frequency scaling [11]. Moreover, in a single motherboard of a server, multiple processors can work together along with many peripheral circuits that need separate voltage rails. Separate converter implementation for each voltage rail adds up and occupies a significant portion of the area and volume available for power management. Instead of using separate converters, single converters with multiple output voltage rails are can be area efficient and a superior system-level solution. From this motivation, the last architecture explored in this dissertation is shown in Fig. 1.2e. High conversion ratio multiple output ~48V PoL Converters can replace the necessity of separate converters.

Traditional power converters are not compatible with the proposed architectures. Therefore, new power converters are needed in the picture to accommodate the innovation of power

delivery. While the proposed power delivery architectures are indigenous and primarily relevant to the data centers and telecommunication systems, the proposed converters' ideas can be stretched to many other applications. Hence, this dissertation is focused on the topologies, control, and modeling of the new converters proposed. All the converters for different stages of each power delivery architecture are hybrid switched-capacitor converters. The following section will provide a brief description of the philosophy behind the used hybrid switched-capacitor converters.

1.2 Hybrid Switched-Capacitor Converters

Primarily, two types of energy storage elements can be used as power transfer components in power converters. Capacitors can store energy in terms of an electrostatic field. On the other hand, magnetic elements, i.e., inductors or transformers, can store energy in a magnetic field. Energy can be transferred from one voltage level to another using energy storage elements or passive components switching between the two levels. For high-frequency switching in electronic circuits, there are transistors, for example, MOSFETs, GaNFETs, etc., that can be turned off or on by electronic signals. While switches are common in almost all power converters, either capacitors or inductors are generally used as energy storage elements. If only capacitors are used as energy transfer elements, power converters are termed switched capacitor (SC) converters. Dickson, Ladder, Series-Parallel, and Flying Capacitor Multi-Level (FCML) converters are examples of SC converters. On the other hand, converters with inductors are termed switched inductor (SI) converters. Buck, Boost, Buck-Boost, Cuk, SEPIC, etc., traditional converters fall into this category. A brief distinction between SC and SI can be found in [12].

The explored converters are synthesized primarily from the SC converters by adding one or more inductors. These converters differ significantly from the parent converters regarding characteristics, advantages, and disadvantages. The customary name of the "hybrid switched-capacitor" converter originated in this way. While the ideas and concepts of hybrid

switched-capacitor converters are not new (some good examples can be found in [13, 14]), new hybrid topologies have been proposed and demonstrated in this dissertation. These topologies' characteristics, advantages, and disadvantages are separate from the parent SC converter and other hybrid converters. Thus, separate investigations were required to understand these converters to a greater extent. In some cases, the analysis conducted in this dissertation explained the characteristics of previously demonstrated hybrid converters and can even be projected to future converters yet to be invented. The next section describes the thesis organization based on the converter demonstrations and techniques for the design and analysis.

1.3 Thesis Organization

Considering recent research trends, industry necessities, and the author's projection of future needs, this dissertation focused on the power delivery architectures of Fig. 1.2 and the stages of these architectures. Because of the number of directions visited and the variation of the core ideas and concepts, the dissertation has been organized into several parts alongside the chapter divisions.

Chapters 2-4 are listed under Part I: Multi Inductor Hybrid Converter Family. Significant efforts have been put into the design of ~48V PoL converters of the last centimeter stage of Fig. 1.2a, 1.2b and 1.2c using the Multi Inductor Hybrid (MIH) converter family. Chapters 2-4 describe three members of the MIH converter family and their operation, and performance in length.

Chapters 5-6 describes the related techniques considered for synthesizing and implementing MIH converter and are listed under Part II: Techniques Related to Multi-Inductor Hybrid Converters. Chapter 5 discusses the synthesis and small signal analysis techniques. Chapter 6 compares the gate driving techniques used for different MIH converters and their advantages and disadvantages.

Chapters 7-10 are listed under Part III: General Analyses of Hybrid Switched-Capacitor

Converters. These chapters dealt with introducing new techniques for properly modeling MIH converters and FLying Capcitror Multi-Level (FCMl) converters, another popular hybris converter family. Chapters 7-10 explored the balancing issues and related considerations which can be projected to other hybrid SC converters for DC-DC applications.

Chapter 11 describes the complete power delivery architecture of Fig. 1.2b using a step-down PFC converter and a ~48V MIH point-of-load (POL) converter. The amount of work enlisted and the expected long-ranging effects of this demonstration warranted the chapter falling under Part IV: Full Power Delivery Architecture.

Chapters 12-13 in Part V:Partial Power Processing explore the topic using hybrid SC converters. Chapter 12 describes a potential solution that can be used for the AC-DC differential power processing shown in the first stages of architecture in Fig. 1.2c, 1.2d and 1.2e. Chapter 13 demonstrates a converter for the isolated stages of Fig. 1.2d.

In Part VI: Multi-Output DC-DC Converters, chapter 14 is listed describes a non-isolated converter capable of providing multiple outputs for the architecture shown in 1.2e. A brief description of the related papers and timeline can be found in the footnote [1].

[1]The chapters 2, 3, 4, 6, 7, 8, 9, 12 and 13 are published in [15], [16], [17], [18], [19], [20], [21], [22] and [23] respectively. Chapter 14 is scheduled to be published at a future conference. Chapter 11 is archived in [24]. Chapters 5 and 10, Appendices I and J contain unpublished materials at the time of organizing this dissertation.

Note that the works listed in this dissertation have been done over the course of five years. A brief timeline of the works is following:

The works in chapters 2, 3, 4, 6, 7 and 8 was mostly done from late 2017 to late 2019. The works on the balancing issues and small signal analysis of the MIH converters and other hybrid switched capacitors in chapters 5, 10 and 9 were done during the lock-down period in 2020. The works on the AC-DC converters in chapters 11 and 12 were accomplished between mid-2020 to mid-2021. The idea of the current control loopless control method in Appendix I was conceived in late 2022. The work on isolated DC-DC converters in chapter 13 was done in early 2021. From mid 2021 to late 2022, the author of this dissertation was working on multiple output power management IC, which has not been listed in this dissertation. The idea of the power converter has been demonstrated and listed in chapter 14. The idea of the multi-output converter was conceived in the first week of the author's Ph.D. journey. However, the control was the most critical part of this converter, and a valid solution was only discovered in late 2021 following the implementation of modular PFC controller in chapter 12. An updated version of this control was figured out after the application of the current control loopless controller in AC-DC modular implementations of Appendix I. The control methods for the multi-output converter are listed in Appendix J.

Part I

Multi Inductor Hybrid Converter Family

Chapter 2

Analysis of Dual-Inductor Hybrid Converters for Extreme Conversion Ratios

2.1 Introduction

For the advantages of simpler board-level input current distribution, large conversion ratios (i.e., 48V-to-1.8V) come with escalated challenges in designing converters to achieve high efficiency and power density. These challenges include (i) choosing optimal switches while satisfying high breakdown voltages and (ii) controlling the power switch driver and timing resolution. At large conversion ratios, the duty cycle of power switches is forced to be extremely small, comparable to the rise-time and fall-time of gate driver signals. To deal with the challenges, various converter architectures have been studied [25–32]. Several stages can categorize (multi-stage or single stage) and isolation (isolated or non-isolated solutions). Multi-stage solutions benefit from more straightforward implementations realized by common converter building blocks that are well established, e.g., 48V-to-12V and 12V-to-1V blocks, but they suffer from efficiency limit to $\sim$90%-92% because of their cascaded power conversion, which in effect reduces the overall system efficiency with the multiplication of efficiencies of separate converters connected in series [25–29]. A single-stage isolated converter reported in [30] uses a resonant impedance-controlled network (ICN) architecture to achieve high efficiency across a relatively wider range of voltage and load conditions whereas its efficiency is limited to $\sim$90% for a 48V-to-1.8V conversion. In the non-isolated category, 94.0% peak efficiency was reported by a

single-stage sigma converter stacking LLC converter-based dc transformer (LLC-DCX) over a Buck converter for a 48V-to-1V conversion [31, 33]. This converter, however, requires a complex startup control, and its efficiency degrades with input and output voltage variations [32]. To avoid relatively bulky, sophisticated custom-made transformers with expensive printed circuit boards (PCB) and control complexities in the isolated converters, this chapter focuses on non-isolated conversion utilizing a simple conventional duty-cycle control. In this category, hybrid converter topologies, such as flying capacitor multilevel (FCML) converter [34] and hybrid Dickson switched-capacitor (SC) converter [35, 36], have proved their unique advantages. In these non-isolated hybrid topologies, an SC network is employed to sustain high input voltages, and an inductor at the output provides a fine regulation like a Buck converter. More importantly, to achieve high efficiency and high power density, the inductor can be operated as a current source to soft-charge and soft-discharge the capacitors to avoid capacitor hard-charging loss. This loss is identified as a fundamental limitation of SC converters, the slow switching limit (SSL) loss, detailed in [37, 38]. As the SC network addresses the input voltage to its fraction, the voltage swing that the inductor and power switches process is significantly reduced.

The small voltage swing at a fraction of the input voltage applied at the inductors enables these hybrid converters to operate at manageable duty cycles avoiding the disadvantages of extremely small duty cycles. As a result, the converter controller can avoid requiring high-resolution pulse width modulation (PWM) and thus allow better utilization of power switches with less RMS current and less conduction loss. The FCML converter in [34] was demonstrated to obtain $\sim$85% efficiency for a 48V-to-2V conversion, while the hybrid Dickson converter in [36] achieved $\sim$95.2% maximum efficiency [36] for a voltage conversion from 130V to 12V at 2A load. Note that for the same output power and conversion ratio, achieving the same high power density at n times lower output voltage is approximately n^2 times (i.e., quadratically) harder even just considering conduction loss because of both n times higher output current and n times lower output voltage.

The dual-inductor hybrid (DIH) converter proposed in [39], shown in Fig. 2.1, shares

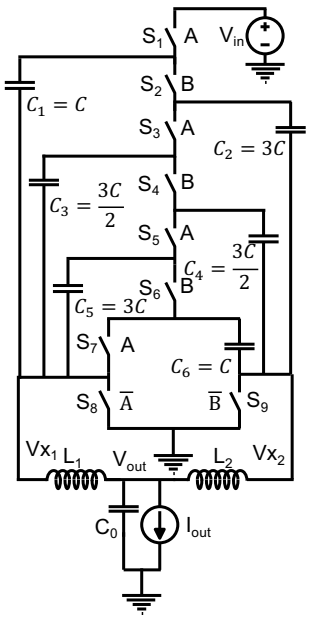


Figure 2.1. Schematic of a 7-to-1 dual inductor hybrid converter using optimal capacitor values described in Section 2.3.2.

the key benefits of the aforementioned hybrid converter topologies, including complete soft charging for flying capacitors by using inductors and low-voltage stress on switches and inductors by an SC network. In addition, the new hybrid converter overcomes their complexities and drawbacks, which include the complicated capacitor voltage balancing circuit in the FCML converter and the split-phase control required in the hybrid Dickson to mitigate capacitor partial hard charging [35, 40, 41]. The hybrid Dickson converter also suffers from duty cycle reduction by a factor of 2, $D = \frac{1}{2}\frac{NV_{out}}{V_{in}}$, from the native SC conversion ratio $\frac{NV_{out}}{V_{in}}$. The proposed DIH converter has two naturally interleaved inductors supporting relatively high output currents, similar to multi-phase interleaved Buck converters [42], and providing capacitors complete soft charging. Its simple Buck-like interleaved PWM operation yields an original, wider duty cycle of $D = \frac{NV_{out}}{V_{in}}$, allowing higher efficiency at larger conversion ratios.

Distinguished from even-level DIH converters analyzed in [40, 41], the odd-level DIH converter has its unique operating principles and resultant merits that allow it to overcome the drawbacks present in the counterpart while keeping the benefits of SC-derived hybrid converters,

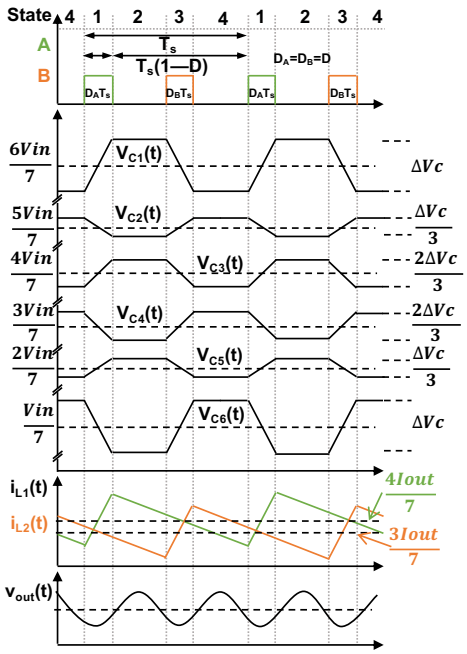


Figure 2.2. Timing diagrams and ideal operational waveforms of 7-to-1 division DIH converter.

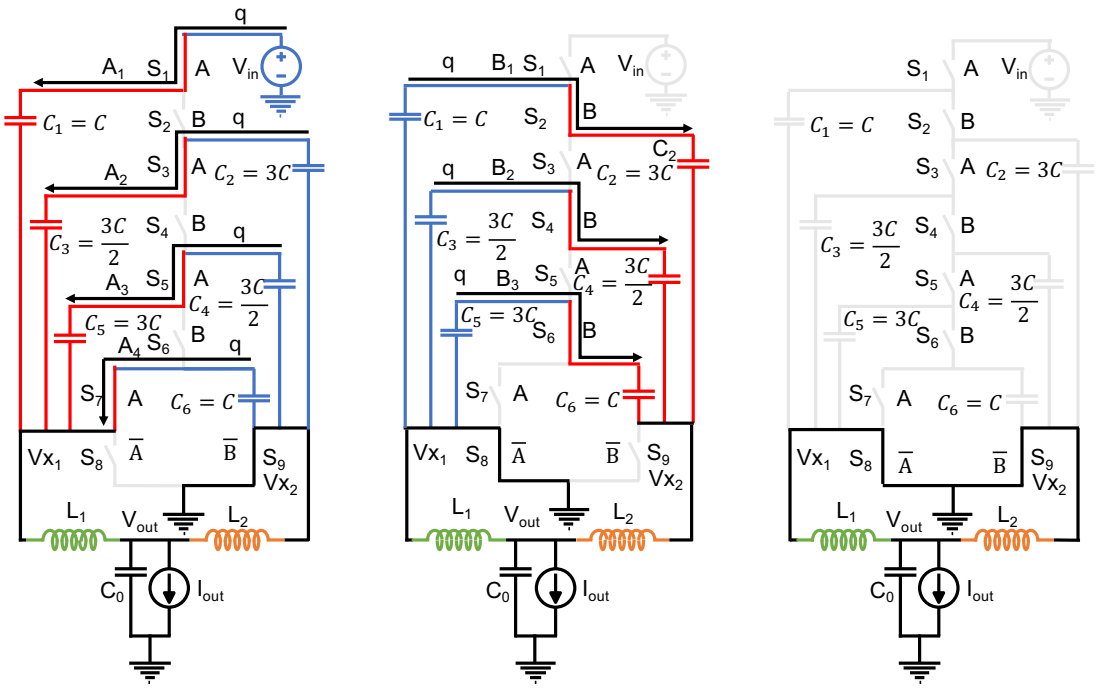
including low voltage stress devices, soft-charging operation, and seamless output regulation. Aiming to provide a comprehensive description of the new converter, this chapter provides a detailed analysis, inductor current balancing method and its experimental validation, residual hard-charging in the switched capacitors, and new experimental results of operations at moderate to very extreme conversion ratios. Particularly, The rest of the chapter is organized as follows.

Section 2.2 discusses the converter structure and operations details. Section 2.3 explains the hard-charging phenomenon of the converter because of voltage ripples of the flying capacitors and introduces the capacitor sizing strategy to achieve complete soft charging. Section 2.4 provides interesting characteristics of the inductor currents in magnitudes and ripples and a simple modulation method to achieve balanced currents. Key loss analysis and experimental results of a DIH converter prototype are provided in Sections 2.5 and 2.6, respectively. Section 2.7 summarizes and concludes this chapter.

2.2 Operation of DIH Converter

A 7-to-1 DIH converter is illustrated in Fig. 2.1. The converter employs nine switches S_{1-9}, six capacitors C_{1-6}, and two inductors L_{1-2}. The converter configuration provides the same voltage division of 7 from the input at the switching nodes, V_{x1} and V_{x2} while using only 9 switches compared to 11 switches in a hybrid Dickson converter counterpart. As described in [41], this difference leads to significant improvements of 2X better switch utilization and loss reduction. The topology has two halves operated in an interleaving manner. The left half includes three capacitors $C_{1,3,5}$, inductor L_1, and switch S_8. The right half includes three capacitors $C_{2,4,6}$, inductor L_2, and switch S_9. Illustrated in Fig. 2.3, these two halves operate in two interleaved phases A and B which typically have the same duty cycles and are 180°out of phase, i.e., shifted by $\frac{1}{2}$ of the switching period, T_s. In this figure, the capacitors in blue are discharging and the ones in red are charging. The operation of the converter can be described together with the timing diagram and ideal waveforms of the converter in Fig. 2.2. In phase A, also state 1 of the operation, illustrated in Fig. 2.3a, the odd-numbered switches $S_{1,3,5,7,9}$ are turned ON, connecting V_{x1} to $\frac{V_{in}}{7}$ to charge inductor L_1. This inductor L_1 current soft-charges $C_{1,3,5}$ and soft-discharges $C_{2,4,6}$. Similarly, during state 3 (Fig. 2.3b), the even-numbered switches $S_{2,4,6,8}$ in phase B are ON to charge L_2 whose current soft-charges $C_{2,4,6}$ and soft-discharges $C_{1,3,5}$. During states 2 and 4 depicted in Fig. 2.3c, switches S_{1-7} stay off letting the flying capacitors idle, while the inductors L_1 and L_2 freewheel via switches S_8 and S_9, respectively.

The two inductors, L_1 and L_2 form two interleaved filters with the common output capacitor C_0. Therefore, the output voltage is just the average voltage of the swings at nodes, V_{x1} and V_{x2}, similar to a two-phase interleaved Buck converter supplied by $\frac{1}{7}V_{in}$. As phases, A and B have the same duty cycles, represented by D, steady-state voltages of the flying capacitors V_{Ci} and the conversion ratio can be calculated. During phase A, analyzing switching node voltage V_{x1} and capacitor branches A_{1-4} denoted in Fig. 2.3a gives:



(a) State 1 (Phase A) **(b)** State 3 (Phase B) **(c)** State 2, 4 (freewheeling)

Figure 2.3. DIH converter circuit operation.

$$V_{x1} = V_{in} - V_{C1} = V_{C2} - V_{C3} = V_{C4} - V_{C5} = V_{C6} = \frac{V_{out}}{D} \tag{2.1}$$

where V_{Ci} is the average voltage of capacitor C_i. Similarly, during phase B in Fig. 2.3b, analyzing switching node voltage V_{x2} and capacitor branches B_{1-3} yields:

$$V_{x2} = V_{C1} - V_{C2} = V_{C3} - V_{C4} = V_{C5} - V_{C6} = \frac{V_{out}}{D} \tag{2.2}$$

Solving (2.1) and (2.2), the steady-state voltages of the flying capacitors and the output voltage can be found as:

$$\begin{aligned} V_{C1} = \frac{6V_{in}}{7},\ V_{C2} = \frac{5V_{in}}{7},\ V_{C3} = \frac{4V_{in}}{7},\ V_{C4} = \frac{3V_{in}}{7}, \\ V_{C5} = \frac{2V_{in}}{7},\ V_{C6} = \frac{V_{in}}{7},\ \text{and } V_{out} = \frac{DV_{in}}{7} \end{aligned} \tag{2.3}$$

Therefore, the switching node voltages in phases A and B converge to be:

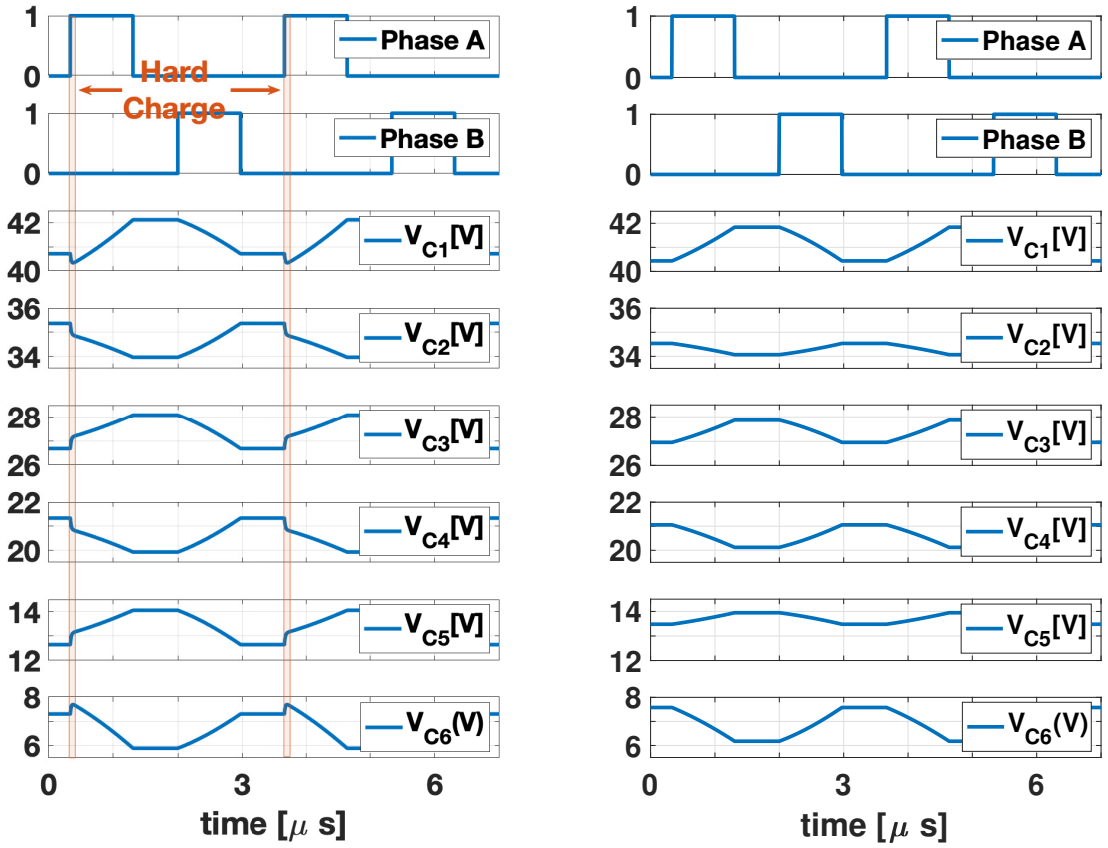
$$V_{x1} = V_{x2} = \frac{V_{in}}{7}. \tag{2.4}$$

As seen in (2.3), the average capacitor voltages are the same as a Dickson-star SC converter [43], and thus the DIH has the same advantages of a Dickson SC converter with a similar structure - having 7 or $7/2$ times less switch voltage stresses compared with a traditional Buck converter. Specifically, switches S_{2-6} experience a voltage stress of $\frac{2V_{in}}{7}$, while $S_{1,7-9}$, on the other hand, endure $\frac{V_{in}}{7}$. This SC-like feature results in better switch utilization with better switch V-A product, [44]. Particularly, it enables the selection of switches with potentially lower voltage breakdown, smaller on-resistance, and smaller parasitic capacitance that can switch faster to reduce passive component sizes.

As will be described in more detail in Section 2.3 and Section 2.4, the capacitors can be designed for the inductor currents to split equally into the capacitor branches to soft-charge and soft-discharge all flying capacitors in phases A and B. In addition, as the inductors, when charged, are connected to different numbers of capacitor branches, they share different fractions of the output current, $\frac{4}{7}I_{out}$ for L_1 and $\frac{3}{7}I_{out}$ for L_2.

As shown in (2.4), the voltage swing applied to the switching nodes is only $\frac{V_{in}}{7}$ which is seven times lower than V_{in} in case of a Buck converter with a large conversation ratio from V_{in} to V_{out}. This voltage reduction allows a significantly relaxed inductor design with much less required inductance, leading to the use of lower equivalent series resistance (ESR) inductor and thus lower associated losses in the DIH converter.

One can think of extending this DIH converter topology to optimize for different operating conditions. For example, an N-to-1 DIH converter has $N-1$ capacitors and $N+2$ switches, feeding a voltage swing of $\frac{V_{in}}{N}$ to the output inductors. The output and capacitor voltages can be found as:



(a) Equal capacitor sizing (C_{1-6}=1 µF)

(b) Optimal capacitor sizing ($C_{1,6}$=1 µF, $C_{2,5}$=3 µF and $C_{3,4}$=1.5 µF)

Figure 2.4. Simulated operations of the 7-to-1 DIH converter. Operating condition: L_{1-2}=2 µ H, V_{in}=48 V, V_{out}=2 V, I_{out}=10 A.

$$V_{out} = \frac{DV_{in}}{N} \text{ and } V_{C_k} = \frac{(N-k)V_{in}}{N}, \quad \text{where, } k = 1,2,...,N-1. \tag{2.5}$$

Since the SC network works as a step-down DC transformer in a DIH converter, the output voltage can be simply regulated to any particular value less than $\frac{V_{in}}{2N}$ by controlling duty-cycle D. Compared with the hybrid Dickson converter counterpart in [36] having $V_{out} = \frac{2DV_{in}}{N}$, the proposed DIH converter is capable of reaching half the output voltage for the same input

voltage and duty cycle, implying benefits in extreme step-down conversion with reasonable switch on-times.

Note that, because of the constraint of non-overlapping operation between the two phases A and B, assuming equal duty cycle D for both phases A and B, the value of duty cycle D is limited to 50%. This is the origin for the factor of 2 in the maximum output voltage limit at $\frac{V_{in}}{2N}$. For example, in case of the 7-to-1 converter in this chapter, V_{out} is limited to $\frac{V_{in}}{14}$. However, while the non-overlapping operation still needs to be maintained for phases A and B, the DIH converter supports an interesting flexibility where the maximum duty cycle limit for a particular phase can be greater (less) than 50% if one chooses to change the phase shift between the phases and/or to reduce (increase) the maximum duty-cycle limit of the other phase. In a similar scenario of operation, the duty cycles of the two phases A and B can actually be different for another specific reason, for example, to balance the DC currents in the two inductors. Details about the specific relation of duty-cycles and inductor currents of this converter will be provided in section 2.4.

2.3 Impacts of Flying Capacitor Values on Their Voltage Ripples and Soft-Charging Capability

This section provides a detailed analysis of the converter operation in terms of flying capacitor voltage ripples in order to explain how capacitor values can be optimized to achieve inherent capacitor soft charging.

In the operation of the 7-to-1 DIH converter in Fig. 2.1, in every switching cycle, T_S, a capacitor receives a charge portion, equivalent to the input charge, from the input (for C_1) or from a higher capacitor and transfer it to the next lower capacitor or inductor (for C_6). For example, C_3 receives a charge from C_2 in phase A and transfers it to C_4 in phase B. This operation ensures charge balance in flying capacitors and their steady-state voltages. The charge flow through a capacitor C_i, can be calculated in two ways: (i) $C_i \triangle V_{Ci}$ where $\triangle V_{Ci}$ is the voltage ripple of the capacitor C_i, or, (ii) integrating the current flowing through the capacitor over its charging

Table 2.1. Flying capacitor voltages for equally sized capacitors

Phase	Capacitor Voltage	Initial	Final
A	V_{C1}	$\frac{6V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{6V_{in}}{7} + \frac{\triangle V_C}{2}$
	V_{C2}	$\frac{5V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{5V_{in}}{7} - \frac{\triangle V_C}{2}$
	V_{C3}	$\frac{4V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{4V_{in}}{7} + \frac{\triangle V_C}{2}$
	V_{C4}	$\frac{3V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{3V_{in}}{7} - \frac{\triangle V_C}{2}$
	V_{C5}	$\frac{2V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{2V_{in}}{7} + \frac{\triangle V_C}{2}$
	V_{C6}	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
B	V_{C1}	$\frac{6V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{6V_{in}}{7} - \frac{\triangle V_C}{2}$
	V_{C2}	$\frac{5V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{5V_{in}}{7} + \frac{\triangle V_C}{2}$
	V_{C3}	$\frac{4V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{4V_{in}}{7} - \frac{\triangle V_C}{2}$
	V_{C4}	$\frac{3V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{3V_{in}}{7} + \frac{\triangle V_C}{2}$
	V_{C5}	$\frac{2V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{2V_{in}}{7} - \frac{\triangle V_C}{2}$
	V_{C6}	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$

Table 2.2. Switching node voltages by different branches for equally sized capacitors

Phase	Switching Node Voltage	Relation with Capacitor Voltage	Initial	Final
A	$Vx_1(A_1)$	$V_{in} - V_{C1}$	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
	$Vx_1(A_2)$	$V_{C2} - V_{C3}$	$\frac{V_{in}}{7} + \triangle V_C$	$\frac{V_{in}}{7} - \triangle V_C$
	$Vx_1(A_3)$	$V_{C4} - V_{C5}$	$\frac{V_{in}}{7} + \triangle V_C$	$\frac{V_{in}}{7} - \triangle V_C$
	$Vx_1(A_4)$	V_{C6}	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
B	$Vx_2(B_1)$	$V_{C1} - V_{C2}$	$\frac{V_{in}}{7} + \triangle V_C$	$\frac{V_{in}}{7} - \triangle V_C$
	$Vx_2(B_2)$	$V_{C3} - V_{C4}$	$\frac{V_{in}}{7} + \triangle V_C$	$\frac{V_{in}}{7} - \triangle V_C$
	$Vx_3(B_3)$	$V_{C5} - V_{C6}$	$\frac{V_{in}}{7} + \triangle V_C$	$\frac{V_{in}}{7} - \triangle V_C$

or discharging phase. In order to ensure complete soft charging, there must not be an impulse current flowing through the capacitor. In other words, the capacitor should be charged and discharged only by an inductor current (and not through a low-impedance path with another capacitor). In a typical operation of the converter where phases A and B have the same duty cycle D, this condition and the charge balance condition for flying capacitors (i.e., $q = I_{C_i} D T_S$) require that the same amount of currents flow through every capacitor in both charge and discharge time, i.e., in phases A and B. This means the currents flowing through all the capacitor branches A_{1-4} and B_{1-3} in phases A and B, respectively, are the same. It turns out that this is not automatically

achieved, but rather affected by choices of capacitor values. The next subsection analyzes two scenarios of capacitor selection: the use of (i) the same values for all flying capacitors, and (ii) optimal values for individual flying capacitors.

2.3.1 Flying Capacitors of the Same Value

In SC converters, it is a common design choice to choose flying capacitors, whose capacitance is proportional to the amount of charge that they process [37, 38]. In the SC network used in this hybrid converter, all flying capacitors process the same amount of charge every cycle. Therefore, one may follow SC converter design wisdom to size all capacitors of the same capacitance C (ideally) or the same effective capacitance (if taking different voltage bias conditions and capacitance degradation into account). However, this capacitance selection method will incur additional losses due to capacitor hard charging.

The key to an optimal capacitor selection is to recognize that charge balance for all the flying capacitors needs to be achieved with soft charging operations using the inductor currents. The charge capacitor C_i processes can be expressed in terms of voltage ripple on the capacitor and the current following through the capacitor over the charging and discharging times, as follows:

$$Q_{C_i} = C_i \triangle V_{c,chrg} = C_i \triangle V_{c,dischrg} = \int_0^{t_{chrg}} i_{chrg} dt = \int_0^{t_{dischrg}} i_{dischrg} dt \tag{2.6}$$

In typical operation, the charging and discharging time, t_{chrg} and $t_{dischrg}$, are the same as DT_S. In steady-state operation, charge balance ensures the voltage ripples when charged $\triangle V_{c,chrg}$ and when discharged $\triangle V_{c,dischrg}$ to be the same, $\triangle V_{c,chrg} = \triangle V_{c,dischrg}$. To achieve complete soft charging for the capacitor, the charging current i_{chrg} and discharging current $i_{dischrg}$ should be a portion of an inductor current and have no impulse. Let us analyze the capacitor voltages and currents in two charging phases, A and B, to check this condition. The simulated waveforms in Fig. 2.4a are used for illustration.

Table 2.3. Capacitor voltages for optimally sized capacitors

Phase	Capacitor Voltage	Initial	Final
A	V_{C1}	$\frac{6V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{6V_{in}}{7} + \frac{\triangle V_C}{2}$
	V_{C2}	$\frac{5V_{in}}{7} + \frac{\triangle V_C}{6}$	$\frac{5V_{in}}{7} - \frac{\triangle V_C}{6}$
	V_{C3}	$\frac{4V_{in}}{7} - \frac{\triangle V_C}{3}$	$\frac{4V_{in}}{7} + \frac{\triangle V_C}{3}$
	V_{C4}	$\frac{3V_{in}}{7} + \frac{\triangle V_C}{3}$	$\frac{3V_{in}}{7} - \frac{\triangle V_C}{3}$
	V_{C5}	$\frac{2V_{in}}{7} - \frac{\triangle V_C}{6}$	$\frac{2V_{in}}{7} + \frac{\triangle V_C}{6}$
	V_{C6}	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
B	V_{C1}	$\frac{6V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{6V_{in}}{7} - \frac{\triangle V_C}{2}$
	V_{C2}	$\frac{5V_{in}}{7} - \frac{\triangle V_C}{6}$	$\frac{5V_{in}}{7} + \frac{\triangle V_C}{6}$
	V_{C3}	$\frac{4V_{in}}{7} + \frac{\triangle V_C}{3}$	$\frac{4V_{in}}{7} - \frac{\triangle V_C}{3}$
	V_{C4}	$\frac{3V_{in}}{7} - \frac{\triangle V_C}{3}$	$\frac{3V_{in}}{7} + \frac{\triangle V_C}{3}$
	V_{C5}	$\frac{2V_{in}}{7} + \frac{\triangle V_C}{6}$	$\frac{2V_{in}}{7} - \frac{\triangle V_C}{6}$
	V_{C6}	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$

Table 2.4. Switching node voltages by different branches for optimally sized capacitors

Phase	Switching Node Voltage	Relation with Capacitor Voltage	Initial	Final
A	$Vx_1(A_1)$	$V_{in} - V_{C1}$	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
	$Vx_1(A_2)$	$V_{C2} - V_{C3}$	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
	$Vx_1(A_3)$	$V_{C4} - V_{C5}$	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
	$Vx_1(A_4)$	V_{C6}	$\frac{V_{in}}{7} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{7} - \frac{\triangle V_C}{2}$
B	$Vx_2(B_1)$	$V_{C1} - V_{C2}$	$\frac{V_{in}}{7} + \frac{2\triangle V_C}{3}$	$\frac{V_{in}}{7} - \frac{2\triangle V_C}{3}$
	$Vx_2(B_2)$	$V_{C3} - V_{C4}$	$\frac{V_{in}}{7} + \frac{2\triangle V_C}{3}$	$\frac{V_{in}}{7} - \frac{2\triangle V_C}{3}$
	$Vx_3(B_3)$	$V_{C5} - V_{C6}$	$\frac{V_{in}}{7} + \frac{2\triangle V_C}{3}$	$\frac{V_{in}}{7} - \frac{3\triangle V_C}{3}$

In phase B illustrated in Fig. 2.4a. with all the capacitors of the same values, charge balance ensures that all capacitors have the same $\triangle V_c$ regardless of their bias voltage V_{Ci}. Three branches B_1, B_2, and B_3 each have two capacitors of the same values, making the same equivalent capacitance and thus the same impedance per branch. This leads to equal distributions of the inductor L_2 current : $\frac{I_{L2}}{3}$ for each branch. Equal voltage ripples $\triangle V_C$ and equal current flows $\frac{I_{L2}}{3}$ over the same duty cycle D in phase B ensure that all the capacitors be soft-charged by the inductor L_2 current, as illustrated on Fig. 2.4a.

In phase A, on the other hand, there are four capacitor branches A_{1-4} connected to inductor L_1 and share its current I_{L1}. These branches have a different number of capacitors and

equivalent capacitance. Particularly, branches A_1 and A_4 have a single capacitor and an effective capacitance of C, while branches A_2 and A_3 have two equal capacitors connected in series and thus an equivalent capacitance of $\frac{C}{2}$. Using the capacitor voltages at the end of phase B in Table 2.1, the initial voltages of each branch A_i in phase A are calculated as shown in Table 2.2. The different numbers of capacitors in each branch lead to different V_{x1} if generated by separate branches A_i. That means as all these branches A_{1-4} are shorted to V_{x1} node, they hard-charge to each other to create a new uniform V_{x1}. This hard-charging phenomenon is illustrated in Fig. 2.4a.

Another way to explain the undesirable hard charge in the flying capacitors is to assess the impedance of capacitor branches and how the inductor currents are split to them. In phase A, the differences in equivalent capacitance lead to impedance differences and, thus, different current distributions in the capacitor branches. Particularly, since branches A_2 and A_3 have two capacitors in series and equivalent capacitance of $\frac{C}{2}$, each of them receives a portion of L_1 current, $\frac{I_{L1}}{6}$, while A_1 and A_4 with only one capacitor of capacitance C, each receive twice the current, $\frac{I_{L1}}{3}$. As a result, the rate of voltage change in V_{C1} and V_{C6} is twice that of V_{C2-C5} in phase A when the capacitors are linearly charged by L_1 current. Since all these branches conduct during the same duty cycle in phase A, charge balance is achieved by an initial hard charge at the beginning of phase A to compensate for the $\triangle V_C$ difference, as illustrated in Fig. 2.4a.

The capacitors' hard-charging is undesirable as it would degrade the converter efficiency. The next subsection derives a method to avoid it.

2.3.2 Flying Capacitors with the Optimal Values

To eliminate the hard-charging and achieve complete soft charging with the same duty cycle D in both phases A and B, a key is to make sure all the charging and discharging currents, I_{chrg} and $I_{dischrg}$, through all the branches are the same. This can be done with an optimal capacitor sizing strategy [39]. In this proposed capacitor optimization method, to balance the currents, it is necessary to match the equivalent capacitance of all branches connected to the

same switching nodes, V_{x1} or V_{x2}. In this 7-to-1 DIH converter, the equivalent capacitance of respective branches are

$$C_{A_1} = C_1,\ C_{A_2} = C_2||C_3,\ C_{A_3} = C_4||C_5,\ and\ C_{A_4} = C_6\ in\ phase\ A \tag{2.7}$$

$$C_{B_1} = C_1||C_2,\ C_{B_2} = C_3||C_4,\ and\ C_{B_3} = C_5||C_6\ in\ phase\ B \tag{2.8}$$

where the operator || is used to express the equivalent capacitance of two series-connected capacitors C_a and C_b - $C_a||C_b = C_a * C_b/(C_a + C_b)$.

For hard-charging elimination, according to the proposed strategy, the equivalent capacitance of all the branches needs to be equal:

$$C_A = C_{A_1} = C_{A_2} = C_{A_3} = C_{A_4} \tag{2.9}$$

$$C_B = C_{B_1} = C_{B_2} = C_{B3} \tag{2.10}$$

Solving (2.7)-(2.10) in terms of a unit capacitance C yields the required values of capacitance for all the flying capacitors as:

$$C_1 = C,\ C_2 = 3C, C_3 = \frac{3C}{2}, C_4 = \frac{3C}{2},\ C_5 = 3C,\ C_6 = C,\ C_A = C,\ and\ C_B = \frac{3C}{4} \tag{2.11}$$

An optimal selection of flying capacitors following (2.11) will ensure equal equivalent capacitance in branches connected to a common switching node, either in phase A or B. In this case, the capacitor voltages and switching node voltages are listed in Table 2.3 and Table 2.4, respectively. The same voltages seen in all the branches in each phase in Table 2.4 are the evidence of no hard-charging in the circuit. This result is also illustrated in a simulation shown in Fig. 2.4b.

2.3.3 Generalization to N-to-1 DIH Converter

The general capacitor optimization for any N-to-1 DIH converter where N is an odd integer can be found as:

$$\begin{gathered} C_k = \frac{N-1}{N-k}C, \textit{ when k is an odd number}, \\ C_k = \frac{N-1}{k}C, \textit{ when k is an even number}, \\ C_n = C_{N-n},\ C_A = C,\ C_B = \frac{N-1}{N+1}C, \\ \textit{where},\ n = 1,2,...,\ \tfrac{N-1}{2}\ \textit{and}\ k = 1,2,...,\ \tfrac{N-1}{2} \end{gathered} \tag{2.12}$$

Note that there is no such solution for optimal capacitance, and thus no complete soft charging, when N is an even integer number larger than 2. A 2-to-1 DIH converter with only one flying capacitor does not require this optimization method. Hard-charging in even-level DIH converters can only be minimized by selecting even-numbered capacitors as big as possible compared to odd-numbered capacitors or a more complex split-phase operation is needed [35, 36, 40, 41]. However, split-phase operation as in [35] is not favorable for large-ratio conversions as it needs even smaller duty cycles for some of the switches than the actual duty-cycle of the converter, as also discussed in section 2.1. Moreover, ideal split-phase timing still depends on the load current, inductor values, and capacitor values, requiring a much more complicated control method for efficient converter operations at multiple operating points [13]. In this consideration, an odd N would be preferred to achieve efficient soft charging using the proposed capacitor selection method.

2.4 Inductor Currents and a Balancing Method

In the presented DIH converter, the two inductors are operated in two interleaved phases having similar current ripples but different DC current levels. This phenomenon has been briefly mentioned in Section 2.2. This section specifically discusses the origin of the unequal inductor currents and proposes a method to make the DC current levels equal. Equal distribution of output

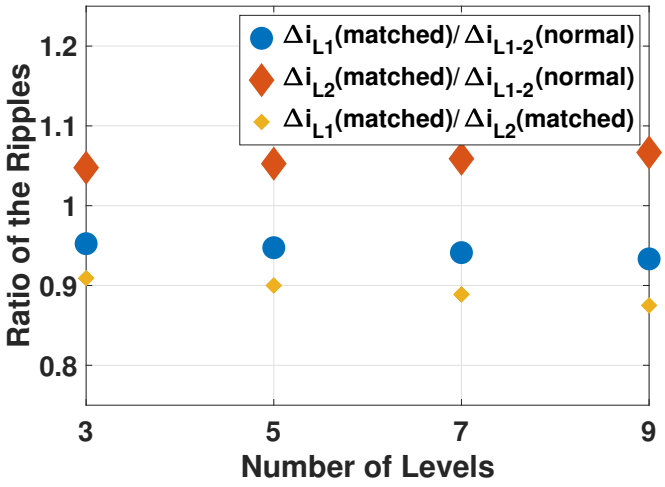


Figure 2.5. Inductor current ripple variation at 48V-to-2V operation.

currents in the two inductors is important as it can significantly reduce the DC conduction loss of the inductors.

In steady-state operation of the DIH converter, charge balance with complete soft-charging ensures that all the capacitor branch currents are the same and summed up to the related inductors. In this way, an inductor current equals n times of the current of an individual capacitor branch, where n is the number of branches connected to that inductor. In this 7-to-1 DIH converter, L_1 is connected to four capacitor branches in phase A, including A_1 with C_1, A_2 with C_{2-3}, A_3 with C_{4-5}, and A_4 with C_6, while L_2 connected to three capacitor branches in phase B, including B_1 with C_{1-2}, B_2 with C_{3-4}, and B_3 with C_{5-6}. Therefore, L_1 carries $\frac{4}{7}$ of the load current I_{out} while L_2 carries $\frac{3}{7}I_{out}$, and their ratio is $\frac{I_{L_1}}{I_{L_2}} = \frac{4}{3}$.

This interesting phenomenon of unequal, yet fixed-ratio inductor currents is present in any N-to-1 DIH converter, where N is an odd number. As L_1 is connected to $\frac{N+1}{2}$ branches and L_2 to $\frac{N-1}{2}$ branches, I_{L1} is $\frac{N+1}{N-1}$ times of I_{L2}. Although the two inductors have different DC current levels, their current ripples are the same since their associated switching nodes, V_{x1} and

Table 2.5. Key components used for converter prototype

Component	Parts for 48V operation	Parts for 150V operation	Part number for capacitors and inductors
S_{1-7}	EPC2014C	EPC2007C	0.68μF 100V TDK-C4532X7R2A684K230KA 1.0μF 100V TDK-CGA8N2X7RA105K230KA 1.5μF 100V TDK-C4532X7R2A155K230KA 3.3μF 100V TDK-CGA8M3X7S2A335K200KB 0.68μF 450V TDK-CGA9M4X7T2W684K200KA 1.0μF 450V TDK-C5750X7T2W105K250KA 2.2μF 450V TDK-C5750X6S2W225K250KA 2.2μH Vishay-IHLP5050EZER2R2M01
S_{8-9}	EPC2023	EPC2020	
C_1	2x0.68μF 100V TDK	2x0.68μF 450V TDK	
C_2	3.3μF+1.0μF 100V TDK	2.2μF+2x1.0μF 450V TDK	
C_3	1μF+0.68μF 100V TDK	2.2μF 450V TDK	
C_4	1.5μF 100V TDK	1.0μF+0.68μF 450V TDK	
C_5	3.3μF 100V TDK	2.2μF+1.0μF 450V TDK	
C_6	1μF 100V TDK	1μF 450V TDK	
L_{1-2}	2.2μH Vishay		
Anti-parallel Diodes with S_{8-9}	CRS08		
Isolated Gate Drivers	Si8275-GBD IS1		

V_{x2}, have the same swing of $\frac{V_{in}}{N}$ during with same DT_s. This current ripple is:

$$\triangle I_L = \frac{\frac{V_{in}}{N} - V_{out}}{2L} DT_s. \tag{2.13}$$

It is of interest to emphasize that the inductor currents are dictated by the charge in the capacitor branches. As a result, although operated similarly to Buck converter and different from each other, these interleaved inductor currents are constrained with fixed ratios to the output current, and thus free from possible thermal runaway issues as in multi-phase Buck converter. However, the nature of unequal inductor currents in odd-level DIH converters may impose unbalanced inductor losses or require different inductors in the same design, which can be undesirable in some applications. Therefore, it is sensible to explore a method to balance the inductor currents in an odd-level DIH converter while still achieving soft charging for all the capacitors.

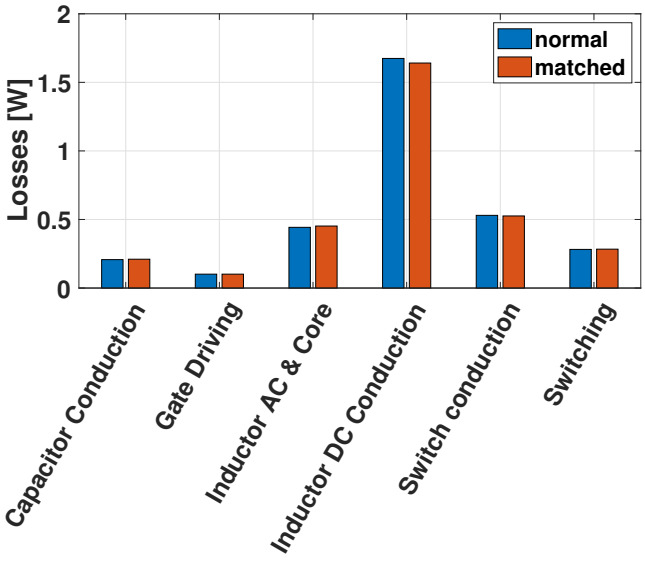


Figure 2.6. Analytical Loss Analysis for 48V-to-2V/20A (300kHz operation).

Considering capacitor charge balance, to maintain a fixed charge processed by a capacitor every cycle, the current through the capacitor can be modulated when changing the activation time of its capacitor branch. For example, increasing the duty cycle of the related phase will cause the current through the capacitor to reduce to sustain the same charge. Since each inductor conducts the summation of the branch currents when activated, when the branch currents are changed, inductor currents will also be altered. Understanding this principle, it is possible to match the DC inductor currents with different duty cycles of phase A and phase B while still sustaining soft charging for all capacitors. Assuming duty cycles D_A and D_B respectively for Phase A and B, (2.1) and (2.2) become:

$$\begin{aligned} V_{x1} &= V_{in} - V_{C1} = V_{C2} - V_{C3} \\ &= V_{C4} - V_{C5} = V_{C6} = \frac{V_{out}}{D_A} \end{aligned} \tag{2.14}$$

$$\begin{aligned} V_{x2} &= V_{C1} - V_{C2} = V_{C3} - V_{C4} \\ &= V_{C5} - V_{C6} = \frac{V_{out}}{D_B}. \end{aligned} \tag{2.15}$$

If Q is the charge processed in each charging or discharging incident, the inductor currents

can be calculated as:

$$I_{L1} = \frac{4Q}{D_A T_s} \; and \; I_{L2} = \frac{3Q}{D_B T s} \tag{2.16}$$

Solving (2.14)-(2.16) with $I_{L1} = I_{L2}$ gives the steady-state input-to-output voltage and duty-cycles relationship as:

$$V_{out} = \frac{V_{in}}{\frac{4}{D_A} + \frac{3}{D_B}} \; and \; \frac{D_A}{D_B} = \frac{4}{3} \tag{2.17}$$

The steady-state capacitor voltages can also be calculated from (2.14)-(2.17). Because of different duty cycles, the converter obtains new steady-state average values for the capacitor voltages.

This calculation can be extended for any DIH converter with an odd-number N of levels as:

$$V_{out} = \frac{V_{in}}{\frac{N+1}{2D_A} + \frac{N-1}{2D_B}} \; and \; \frac{D_A}{D_B} = \frac{N+1}{N-1}. \tag{2.18}$$

For the same output voltage, duty cycles of matched inductor current operation can be written in terms of the duty cycle D of unmatched inductor current operation as:

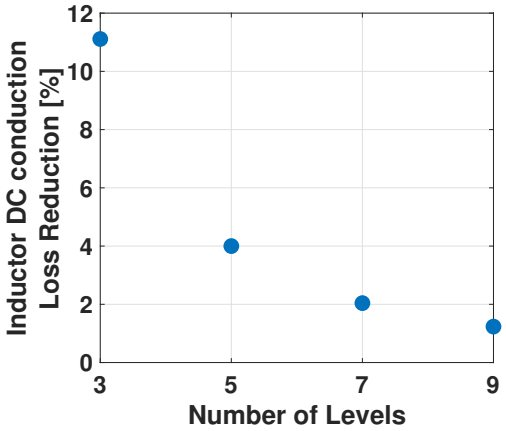


Figure 2.7. Inductor DC conduction loss reduction with matched current operation

$$D_A = \frac{N+1}{N} D \;\; D_B = \frac{N-1}{N} D. \tag{2.19}$$

Switching nodes V_{x_1} and V_{x_2} also swing with different voltage of $\frac{V_{in}}{N+1}$ and $\frac{V_{in}}{N-1}$, respectively. That means, in this case, where, two inductors have the same DC currents, they have different current ripples. New current ripples can also be calculated as,

$$\begin{aligned} \triangle I_{L_1} &= \frac{\frac{V_{in}}{N} - \frac{N+1}{N} V_{out}}{2L} DT_s, \\ \triangle I_{L_2} &= \frac{\frac{V_{in}}{N} - \frac{N-1}{N} V_{out}}{2L} DT_s \end{aligned} \tag{2.20}$$

Fig. 2.5 illustrates the relationship between current ripples of the inductors after modulation for the same average current, noted as *matched*, and the inductor current ripple when operated with equal duty cycle $D_A = D_B = D$, noted as *normal* or *unmatched*, and the relationship between the two inductors' current ripples in the matched case. The decrease of current ripple in L_1, $\Delta I_L - \Delta I_{L1}$, and the increase of current ripple in L_2, $\Delta I_{L2} - \Delta I_L$, are equal and can be calculated as $\frac{V_{out}}{N} \frac{DT_S}{2L}$. Their deviations are symmetric in the current matched operation compared to their nominal values in the normal operation. It can be seen that the values of the current ripples do not deviate much from the nominal value. This is because as duty cycles change, respective switching node voltages also change and in an effectively opposite way, keeping the ripple from departing away from the nominal value. This phenomenon implies that there will be an insignificant difference in inductor AC and core losses between the matched and normal cases.

As long as the condition of $(D_A + D_B < 1)$ is satisfied, equations (2.14)-(2.20) are valid. In practical implementation, values of D_A and D_B can be calculated in a microcontroller to obtain a desirable operation and conversion ratio. This will be demonstrated in experiments presented in Section 2.6.

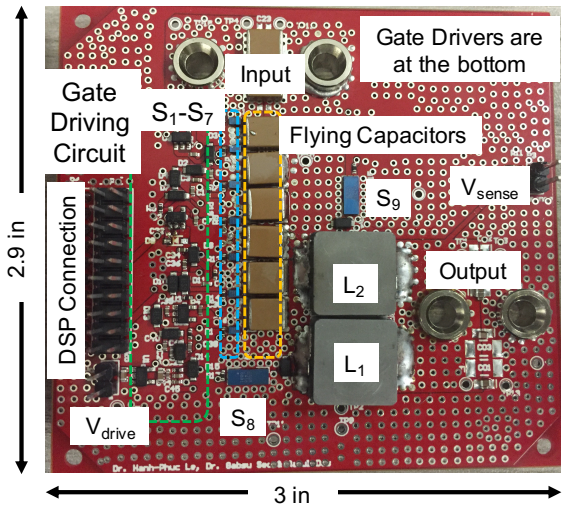
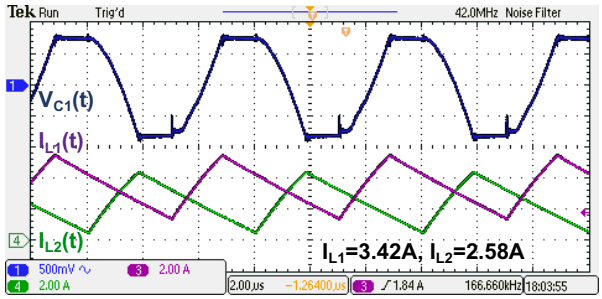


Figure 2.8. 7-to-1 DIH converter prototype on a 3 in x 2.9 in demonstration board

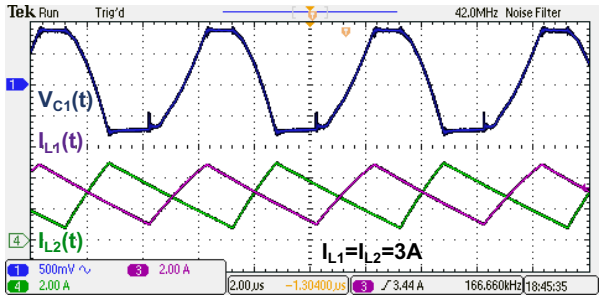
2.5 Loss Analysis

This section covers loss analysis to understand loss contributions in a practical design as well as identify the impact of equalizing the inductor currents with different duty-cycles. In the presented 7-to-1 DIH converter (Fig. 2.1), S_{1-7} serve similar functions as the high-side switch while S_{8-9} emulates the operation of the low-side switch of a synchronous Buck converter. Considering the operation described in Section 2.2, two different types of devices are required for the implementation of the high-side switches and low-side switches. Losses in the converter circuit have been analyzed according to the synchronous Buck converter analysis from [45]. Inductor AC and core losses have been determined following [46]. Capacitor voltage ripples are assumed insignificant and ignored for the analysis.

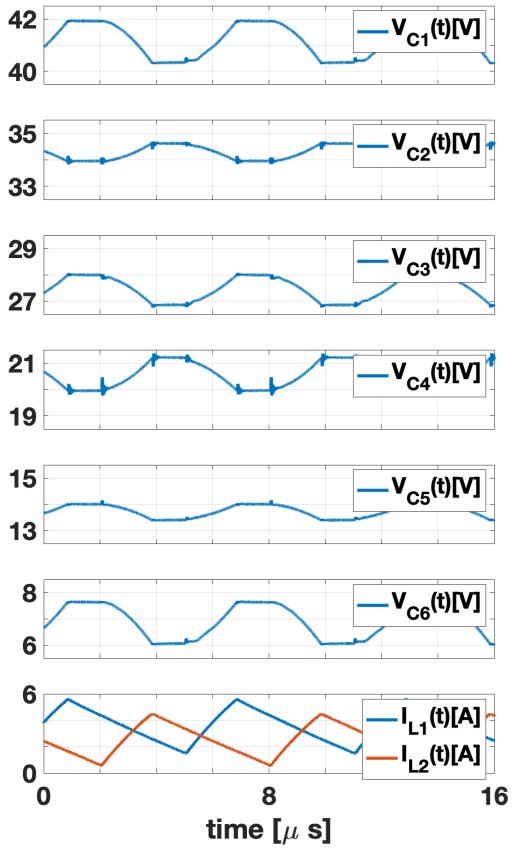
Fig. 2.6 shows the converter loss breakdown when operated at a 48V-to-2V conversion at 20A load with a switching frequency of 300 kHz. From Fig. 2.6, it can be observed that at this particular operating point, the normal unmatched and matched inductor current implementations have insignificant loss difference, although the latter have slightly lower inductor DC conduction loss. Considering R_L as the inductor DC resistance (DCR) we can calculate the DC conduction



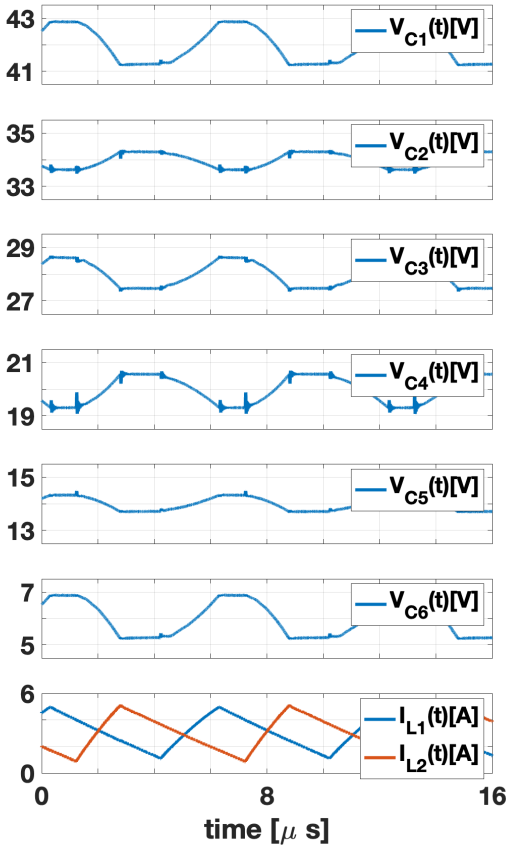
(a) at 48V-to-2V/6A in normal operation



(b) at 48V-to-2V/6A in matched current operation



(c) at 48V-to-2V/6A, normal

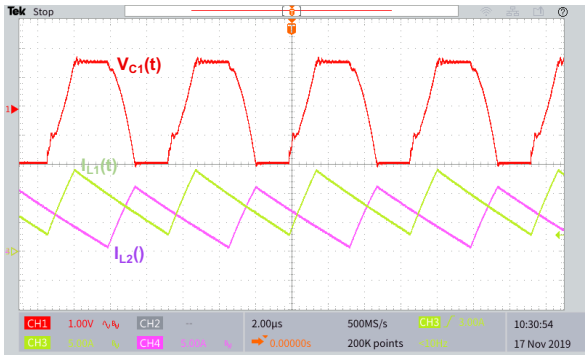


(d) at 48V-to-2V/6A, matched current operation

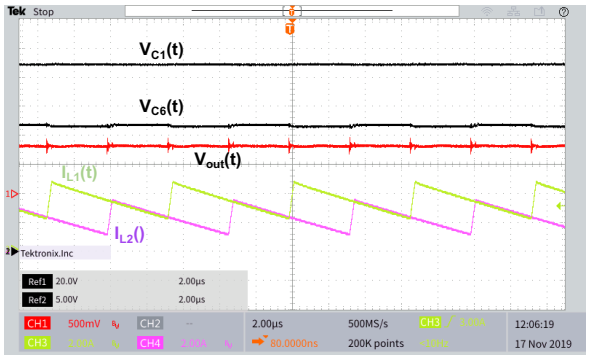
Figure 2.9. Key experimental waveforms of capacitor voltages and inductor currents with $V_{in} = 48V$ and f_s = 167kHz

loss in the inductor in normal and matched operations as:

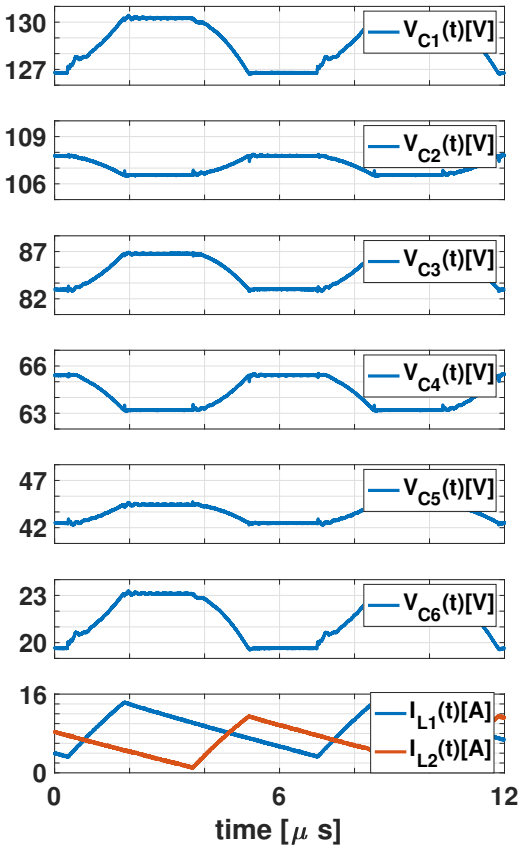
$$\begin{aligned} P_{inductor,normal} &= [(\frac{N+1}{2N})^2 + (\frac{N-1}{2N})^2] I_{out}^2 R_L \\ &= [\frac{1}{2} + \frac{1}{2N^2}] I_{out}^2 R_L \end{aligned} \tag{2.21}$$



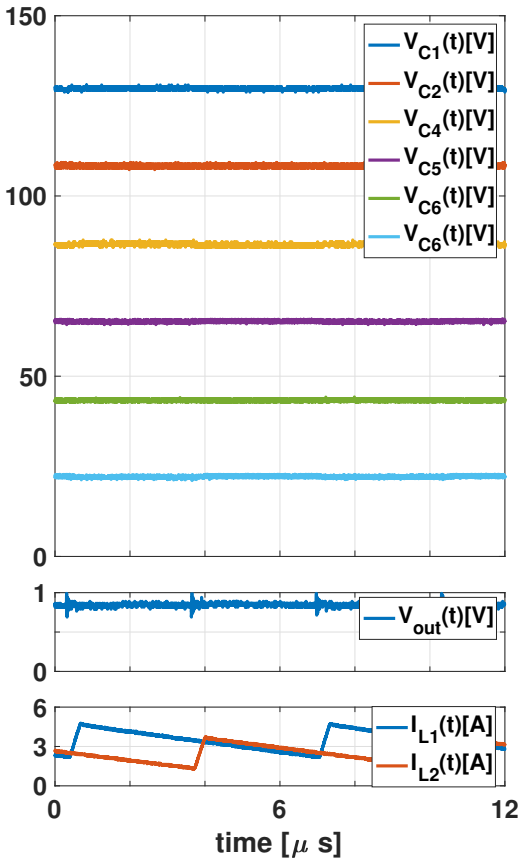
(a) at 150V-to-5V/15A



(b) at 150V-to-0.85V/5A



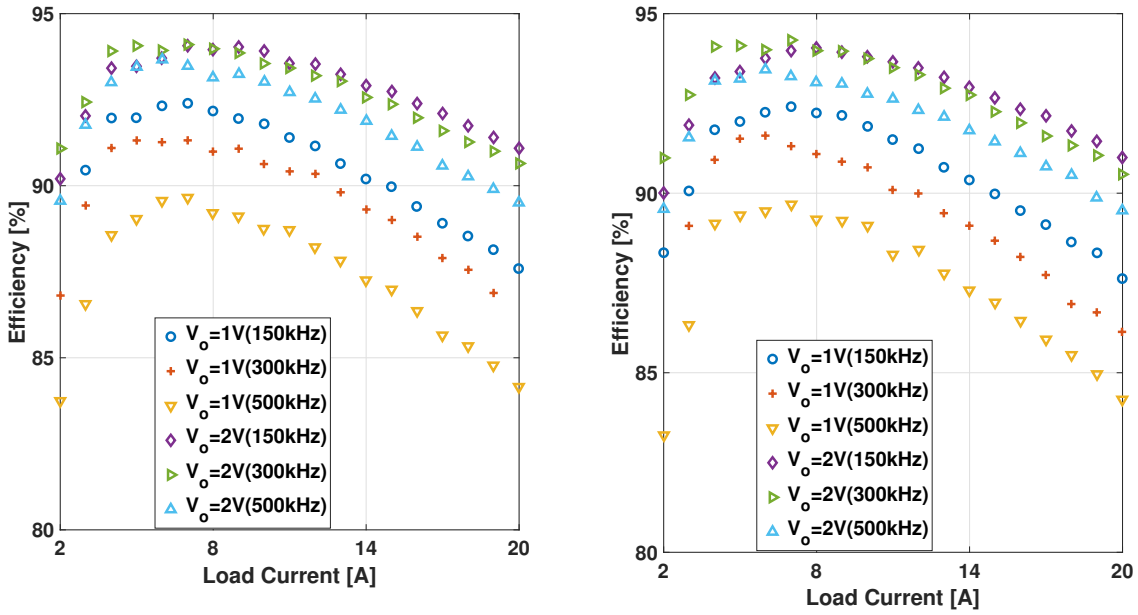
(c) at 150V-to-5V/15A



(d) at 150V-to-0.85V/5A

Figure 2.10. Key experimental waveforms of capacitor voltages and inductor currents at V_{in} = 150V and f_s = 150 kHz in normal, unmatched operation

$$P_{inductor,matched} = \frac{1}{2} I_{out}^2 R_L \tag{2.22}$$



(a) Normal operation, $D_A = D_B = D$

(b) Matched inductor current operation

Figure 2.11. Measured efficiency at 48V input with normal operation and matched inductor currents

Comparing (2.21) and (2.22), it is possible to reduce $\frac{1}{N^2}$ portion of the DC conduction loss from the inductors with the matched inductor current operation. However, the reduction is small with $N = 7$ in the implemented 7-to-1 DIH converter. In a converter with a smaller number of levels, e.g. N=3, the average current difference and thus the inductor DC conduction loss reduction can be significant, as illustrated in Fig. 2.7.

From Fig. 2.6, it is evident that although the voltage swings for the inductors have been reduced significantly by the switched-capacitor network to reduce AC and core losses in the inductors, their DC conduction loss still dominates the total loss of the converter. In this analysis, commercial inductors have been used for loss analysis and implementation, which have relatively high DCRs. Nevertheless, high DC conduction loss for the inductor is the common most challenging problem in designing step-down converters with an inductor at the output that needs to support large output currents [47, 48].

2.6 Hardware Implementation and Experimental Results

To verify the feasibility of the new converter topology and design methods, a 7-to-1 DIH converter prototype was implemented and demonstrated for 48V to 1-2V/20A and 150V to 1-5V/20A conversions. The prototype's PCB is displayed in Fig. 2.8. A list of key components is tabulated in Table 2.5. PWM signals required to drive the converter were generated from a TMS320F28377S microcontroller. A converter average model was employed to design switches and capacitors with the proposed capacitor size optimization strategy in Section 2.3.2. As capacitance values are highly dependent on the voltages they experience (in steady state), capacitance degradation occurs differently for capacitors at different levels. To address this, the capacitor values were selected according to the data sheets so that after degradation their effective capacitance satisfies the optimal ratio calculated in (2.11).

Fig. 2.9 and 2.10 show operational waveforms of the converter in steady-state operation from 48V and 150V inputs, respectively. Measured capacitor voltages' ripples along with inductor currents are shown in Figs. 2.9c, 2.9d and 2.10c, verifying the capacitors' soft-charging and soft-discharging operations for a wide range of input voltage and conversion ratios. Figs. 2.9c and 2.9d demonstrate operations of the normal and matched current operations for the same input and output conditions, validating the discussion and methods described in Section 2.4. Note that while duty cycles were modulated to achieve balanced inductor currents, all flying capacitors still have soft charging operations.

Fig. 2.11 shows measured efficiencies of the converter at 48V input and when operated in normal operation or in matched inductor current operation. These experimental results verify that the two operations do not have significant efficiency and loss difference, as predicted in the loss analysis in Section 2.5. The converter exhibited peak efficiencies of 94.3% and 92.6% for 2V and 1V, respectively, from a 48V input.

Fig. 2.10d illustrates the DC voltage levels of the capacitors in normal operation at an extreme conversion of 150V input to 0.85V output, or 176:1 conversion. The converter

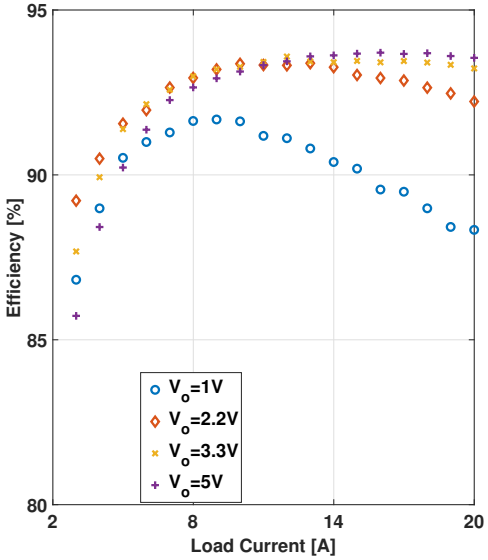


Figure 2.12. Measured efficiency at $V_{in} = 150V$ and f_s = 150 kHz

performance at 150V input providing a wide range of regulated output voltages from 1V to 5V is shown in Fig. 2.12. The converter achieves 91.3% peak efficiency at a 150:1 conversion ratio from 150V to 1V and 93.7% peak efficiency at a 30:1 conversion ratio from 150 to 5V, validating its feasibility in applications where a high conversion ratio with high efficiency is required.

2.7 Chapter Summary

This chapter has presented a hybrid converter using two interleaved inductors, that is verified to be able to support extreme conversion ratios with promising efficiency. The converter works with two interleaving phases sharing the same front-end switched-capacitor network and achieves soft charging and balance for all flying capacitors. Residual hard-charging that can come from non-optimal capacitor values has been addressed properly with an intuitive capacitor voltage ripple analysis and sizing. The two output inductors of the odd-level DIH converter analyzed in this chapter have an inherent interesting characteristic: they have unequal, yet fixed-ratio currents. These inductor currents can be equalized using a relatively simple duty-cycle modulation technique. The trade-offs in loss and design between normal (unmatched) and

matched current operations have also been discussed. A converter prototype was implemented and verified in the experiments at up to 20A and 100W operations. It can also support extremely wide input and output voltage ranges, tested at 48V-150V and 1V-5V. The DIH converter prototype achieved desirable operations and characteristics and demonstrated 92.4% peak efficiency at 48V-to-1V operation and 91.3% peak efficiency at 150V-to-1V operation. The converter would be a promising candidate for power conversion with extreme conversion ratios that can push the limit of point-of-load applications, reducing complexity and cost for bus voltage distributions, as well as enabling reduction in conversion stages and thus higher efficiency in overall power delivery for data centers and high-performance digital systems.

Chapter 2, in full, is a reprint of the material as it appears in "Analysis of Dual-Inductor Hybrid Converters for Extreme Conversion Ratios," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 5, pp. 5249-5260, Oct. 2021 by the authors Das, Ratul; Seo, Gab-Su and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 3

An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter

3.1 Introduction

Recently, leveraging the intrinsic dual phase operation of the Dickson SC converter, Dual Inductor Hybrid (DIH) converter topologies has been proposed [39, 40]. The DIH converter with an odd number of levels excluding the zero level in [39] employs a capacitor sizing strategy to effectively achieve soft-charging and over 91% efficiency for an extreme conversion ratio of 120V to 1.8V. The even-level DIH converter in [40] utilizes a split-phase operation similar to the Hybrid Dickson SC converter in [36] to minimize hard-charging in flying capacitors and achieves ∼95% efficiency for a 48V-to-1.8V conversion.

It is of interest to note that the intrinsic phase duality of a Dickson SC converter can be extended to a larger number of phases to further optimize soft-charging operation [49]. Based on this realization, a Multi-phase multi-inductor hybrid (MPMIH) Converter topology is proposed in this chapter for PoL applications. Compared with the odd-level DIH converter, the MPMIH converter can achieve complete capacitor soft-charging with a simpler capacitor sizing strategy and does not require any complexity such as split-phase control. In addition, for the same ripple at the output, the proposed converter can significantly reduce the inductor size because of its native interleaving operation and small inductor voltage swing, i.e. $\frac{V_{IN}}{N}$ for an N-level MPMIH converter. In order to explore the capabilities and characteristics of this new converter, we discuss

details of the converter operation, capacitor sizing strategy, and its advantageous characteristics in Sections 3.2 and 3.3. Section 3.4 presents experimental results of an MPMIH converter prototype supporting 48V-to-1V/2V conversion at up to 40A loads. Conclusions are presented in Section 3.5.

3.2 Operation of the Multi-Phase Multi-inductor Hybrid Converter

A three-phase version of the proposed MPMIH converter having one inductor for each phase, as shown in Fig. 3.1, is used to discuss the converter operation principles. The converter consists of five flying capacitors C_{1-5} and eight switches S_{1-8} to form a switched-capacitor network followed by three inductors L_{1-3} and output capacitor C_0. Different from SC converters where flying capacitors are directly connected to the output, the switched capacitor network delivers charges from the input to the output through the three inductors. This configuration enables the hybrid converter to avoid capacitor hard-charging, which is a fundamental loss limitation in SC converters. The converter has three groups of passive components associated with three inductors, L_1 directly connected to C_1 and C_4, L_1 to C_2 and C_5, and L_3 to C_3. As

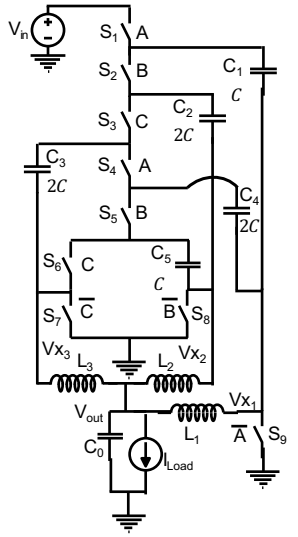


Figure 3.1. Multi-phase multi inductor hybrid converter topology

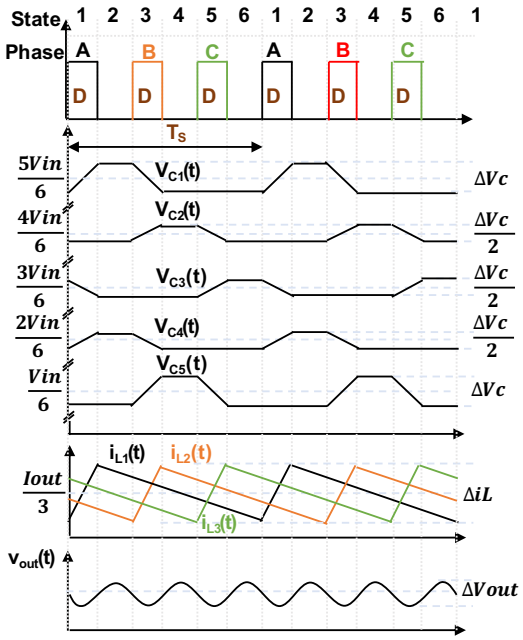
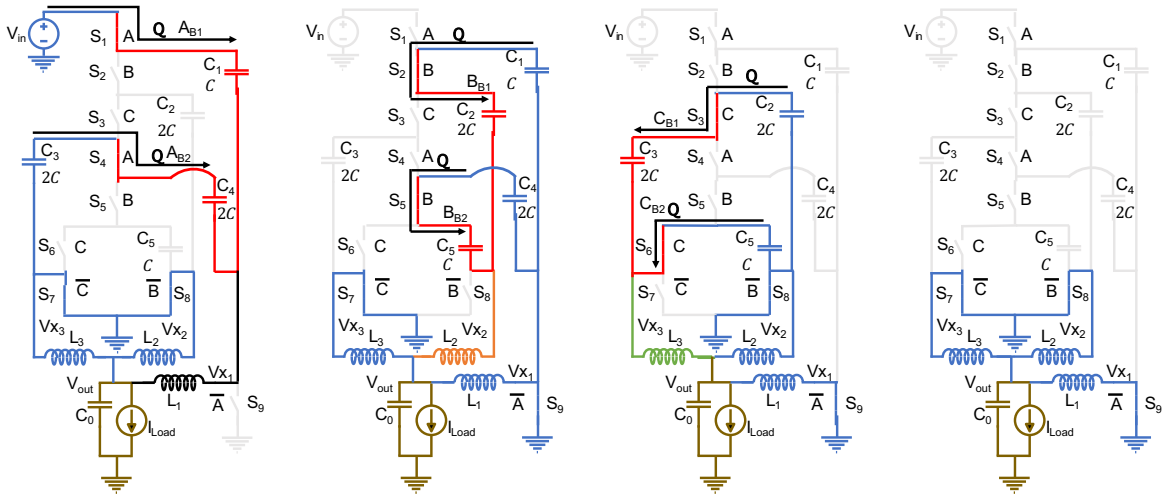


Figure 3.2. Operational waveforms

illustrated in Fig. 3.2 and Fig. 3.3, the converter has six states with three inductor charging phases in one operating cycle T_S. In States 1, 3, and 5 (Phases A, B, and C), inductors L_1, L_2, and L_3, respectively, get charged. Over a cycle, one inductor charges in one state and discharges (freewheels) to the output in all other states when its associated bottom switch is activated. For example, L_1 gets charged in State 1 (also referred to as Phase A) and discharges in States 2-6. When L_1 gets charged, the capacitors C_1 and C_4 in its group also get charged by the inductor's current in a lossless manner. The charge is then transferred to the next group, L_2 with C_2 and C_5, and finally to L_3 with C_3. In States 2, 4, and 6, all inductors freewheel, while all flying capacitors are open-circuited and inactive.

Assuming small ripples on the flying capacitor voltages, the steady state capacitor voltages V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5} are found to be $\frac{5V_{in}}{6}$, $\frac{4V_{in}}{6}$, $\frac{3V_{in}}{6}$, $\frac{2V_{in}}{6}$, and $\frac{V_{in}}{6}$, respectively, similar to a standard 6-to-1 Dickson switched-capacitor converter [50]. With duty cycle D defined as the ratio between the ON time of one phase and the switching period T_SS, the ideal input to output voltage conversion ratio is $\frac{V_{out}}{V_{in}} = \frac{D}{6}$. The factor 6, enabling a large conversion



(a) State 1(ϕ A) **(b)** State 3 (ϕ B) **(c)** State 5 (ϕ C) **(d)** State 2,4 and 4(inactive phases)

Figure 3.3. Operating states of the proposed MPMIH converter

ratio, comes from the number of levels in the SC network.

As explained above and illustrated in Fig. 3.2, to maintain the intended operation of the converter Phases A, B, and C need to stay non-overlapped. This limits duty cycle D to $D_{max} = \frac{1}{3}$ and thus, the maximum output voltage to $V_{out,max} = \frac{V_{in}}{18}$. In a general implementation of an N-to-1 MPMIH converter with N SC levels, theoretical output voltage and capacitor voltages are given as:

$$V_{out} = \frac{DV_{in}}{N} \quad \text{and} \quad V_{C_k} = \frac{(N-k)V_{in}}{N} \quad , where, k = 1, 2, ..., N-1 \tag{3.1}$$

When this MPMIH converter topology is constructed to have N high-side switches, N-1 capacitors, N levels (ignoring the zero level), M inductors and M charging phases, its duty cycle is limited to $D_{max} = \frac{1}{M}$ and output voltage to $V_{out,max} = \frac{V_{in}}{N \cdot M}$. Note that these non-overlapped interleaving phases need to be equal, i.e. have the same duty cycle D, for the intended charge transfer operation and equal inductor current ripple in the inductors. However, they are not required to be evenly distributed over the period. In general, a uniform distribution is preferred since it ensures the smallest current and voltage ripple at the output, as similarly found in multi-phase Buck converters [42].

Table 3.1. Equivalent capacitance matrix

	Equivalent Capacitances		
Phases	A	B	C
B1 Branches	C_1	$C_1 \parallel C_2$	$C_2 \parallel C_3$
B2 Branches	$C_3 \parallel C_4$	$C_4 \parallel C_5$	C_6

3.3 Soft-Charging Operation and Strategy for Capacitor Sizing

In the MPMIH converter topology, the capacitor charge balance must be met in steady-state operation. When the same duty cycle D is applied to Phases A, B, and C, the inductors are activated for the same period of time and by the same voltage swing, and thus have the same current level. This results in an identical net charge supplied to each flying capacitor in an active state (State 1, 3, or 5), regardless of phase sequence or effective capacitance values. Note that in the operation of the MPMIH converter, one inductor is always charged through two capacitor branches in energizing phases A, B, or C. If these two capacitor branches, e.g. C_1 and C_2-C_3 in Phase A have different equivalent capacitances or $C_1 \neq \frac{C_2 \cdot C_3}{C_2+C_3}$, that leads to the different inductor current distribution through these branches. In other words, these capacitors will receive different charges distributed by the inductors. To maintain the fundamental steady-state operation of this topology, which assumes that all capacitors process the same net charge, hard charging may take place at the beginning of active phases to allow for charge redistribution.

Table 3.2. Switching node voltages for equal capacitor sizing

States	Switching Node Voltages	Start	End
1	$Vx_1(A_{B1})$	$\frac{V_{in}}{6} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{6} - \frac{\triangle V_C}{2}$
	$Vx_1(A_{B2})$	$\frac{V_{in}}{6} + \triangle V_C$	$\frac{V_{in}}{6} - \triangle V_C$
2	$Vx_2(B_{B1})$	$\frac{V_{in}}{6} + \triangle V_C$	$\frac{V_{in}}{6} - \triangle V_C$
	$Vx_2(B_{B2})$	$\frac{V_{in}}{6} + \triangle V_C$	$\frac{V_{in}}{6} - \triangle V_C$
3	$Vx_3(C_{B1})$	$\frac{V_{in}}{6} + \triangle V_C$	$\frac{V_{in}}{6} - \triangle V_C$
	$Vx_3(C_{B2})$	$\frac{V_{in}}{6} + \frac{\triangle V_C}{2}$	$\frac{V_{in}}{6} - \frac{\triangle V_C}{2}$

Table 3.3. Switching node voltages for optimal ratio capacitor sizing

States	Switching Node Voltages	Start	End
1	$Vx_1(A_{B1})$	$\frac{V_{in}}{6}+\frac{\triangle V_C}{2}$	$\frac{V_{in}}{6}-\frac{\triangle V_C}{2}$
	$Vx_1(A_{B2})$	$\frac{V_{in}}{6}+\frac{\triangle V_C}{2}$	$\frac{V_{in}}{6}-\frac{\triangle V_C}{2}$
2	$Vx_2(B_{B1})$	$\frac{V_{in}}{6}+\frac{3\triangle V_C}{4}$	$\frac{V_{in}}{6}-\frac{3\triangle V_C}{4}$
	$Vx_2(B_{B2})$	$\frac{V_{in}}{6}+\frac{3\triangle V_C}{4}$	$\frac{V_{in}}{6}-\frac{3\triangle V_C}{4}$
3	$Vx_3(C_{B1})$	$\frac{V_{in}}{6}+\frac{\triangle V_C}{2}$	$\frac{V_{in}}{6}-\frac{\triangle V_C}{2}$
	$Vx_3(C_{B2})$	$\frac{V_{in}}{6}+\frac{\triangle V_C}{2}$	$\frac{V_{in}}{6}-\frac{\triangle V_C}{2}$

Let us first consider a scenario where all the capacitors are sized equally for this converter in the same manner as a Dickson SC converter. In this case, the ripple voltage for each capacitor is $\triangle V_C$, and the switching node voltages generated by individual capacitor branches are listed in Table 3.2. It can be observed that during States 1 and 5, active capacitor branches do not have equal voltages, which results in hard charging. To remove this undesirable hard-charging, split-phase operations were employed in the Hybrid Dickson topology in [36] and the previous DIH converter topology in [40]. In the split-phase operation, activation of the first and last capacitor branches, having larger equivalent branch capacitance with only one capacitor of the same size, is made smaller to equalize the net charge delivery to avoid hard charge redistributions. Since the split-phase operation introduces more challenging timing, this may limit possible minimum duty cycles and thus achievable conversion ratios. It is therefore desirable to avoid this hard-charing without using split-phase operation.

In the MPMIHC topology, a simple capacitor sizing strategy can be applied to achieve soft charging for the capacitors without using any supplementary operation such as split-phase control. In every active state, there are two branches of capacitors connected with an individual inductor. Particularly, L_1 is connected to two branches of $C_1$and C_3-C_4 in State 1 (Phase A), L_2 to C_1-C_2 and C_4-C_5 in State 2 (Phase B), and $L_3$to C_2-C_4 and C_5 in State 3 (Phase C). Table 3.1 lists the equivalent capacitances for these active states. As explained above, to ensure soft charging, active branches in an active state should have the same equivalent capacitance.

Therefore, the equivalent capacitances in the two rows of each column in Table 3.1 should result in the same values. Applying this condition for all capacitor branches in all active states, the required capacitance values can be solved for in terms of a nominal capacitance C as:

$$C_1 = C,\ C_2 = 2C,\ C_3 = 2C,\ C_4 = 2C \text{ and } C_5 = C. \tag{3.2}$$

This capacitor sizing strategy bears similarity to the method used in [39]. Since, in the MPMIH converter topology of this chapter, one inductor only handles two capacitor branches instead of three or four branches in [39] the approach yields a simpler capacitor sizing calculation and strategy. Particularly, top capacitor C_1 and bottom-capacitor C_5 in the single capacitor, branches should be one-half of the other capacitors. Using these new capacitor sizes, the switching node voltages are recalculated and tabulated in Table 3.3, showing uniform capacitor

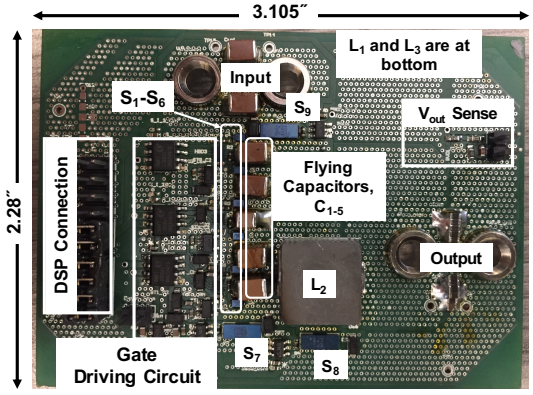


Figure 3.4. 6-level MPMIH converter prototype

Table 3.4. Major components

Component	Part info.
S_{1-6}	EPC2014c
S_{7-9}	EPC2023
C_1, C_2	2x2.2uF, 4x1.5uF 100V TDK
C_3, C_4, C_5	4x1.5uF, 4x1uF, 2x1uF 50V TDK
L_{1-3}	2.2uH Vishay
Isolators	Si8423
Gate Drivers	LM114BMF, LMG1205YFXR

voltages in the branches in each active state effectively eliminating hard-charging.

Although this sizing strategy theoretically ensures no hard charging, it should be noted that in practice small hard charging may exist because of engineering tolerances and bias voltage-dependent capacitance degradation. In addition, this capacitor sizing strategy does not guarantee valid solutions for all MPMIH converter versions with any number of phases and

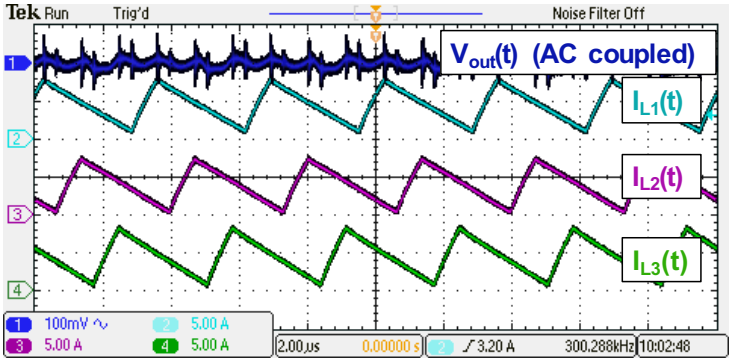
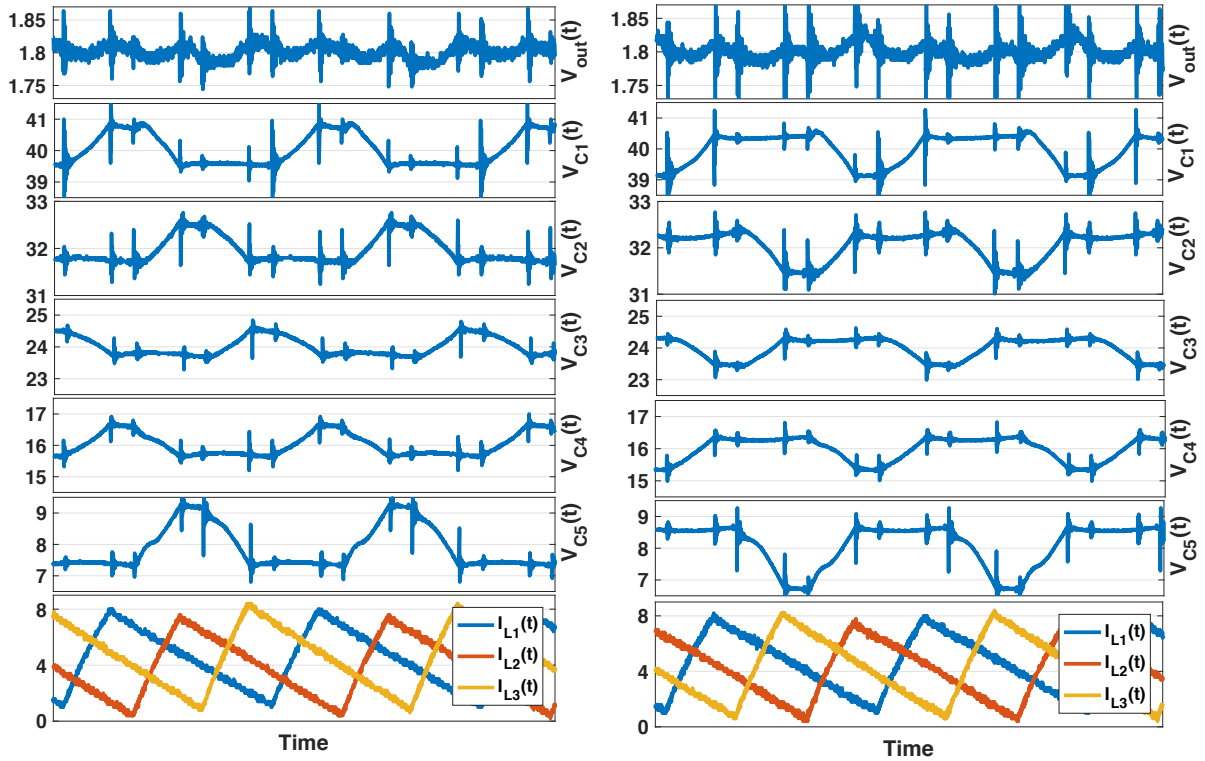


Figure 3.5. Steady-state waveforms with 13A load current



(a) ABC sequence **(b)** ACB sequence

Figure 3.6. Measure capacitor voltages at 13A loads

levels. For example, there is no valid solution with definite capacitor values for an eight-level four-phase four-inductor converter of this family, but the solution exists for a ten-level five-phase five-inductor version.

3.4 Experimental Results

The proposed topology and its operation are verified using the experimental prototype shown in Fig. 3.4 with the components listed in Table 3.4. Capacitor voltage and inductor current waveforms are shown in Figs. 3.5 and 3.6a. Fig. 3.6b illustrates the flexibility of this converter that it maintains its intended operation with different phase sequences. Particularly, the converter is operated with A-B-C sequence in Fig. 3.6a and with the A-C-B sequence in Fig. 3.6b while maintaining the intended characteristics of interleaved inductor phases and soft charging for flying capacitors. The converter has been tested for 48V input voltage and 1V-2V output for up to 40A of load currents, as shown in Fig. 3.7. It achieves a peak efficiency of 94.6% at 2V/8A output and maintains high efficiency (>90%) for a wide range of output loads up to beyond 30A for a 2V output. The converter has a power density of 425 W/in^3 considering key power conversion components.

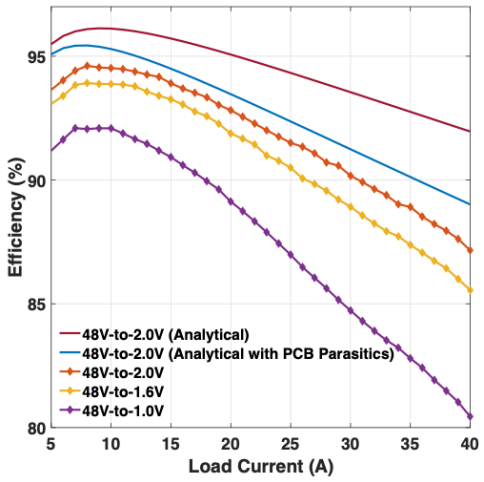


Figure 3.7. Measured converter efficiency

3.5 Chapter Summary

The chapter describes a Multi-Phase Multi-Inductor Hybrid converter that has significant benefits over state-of-the-art topologies, and shows how the SC network can be effectively soft-charged with inductors for high-efficiency conversions. The converter can achieve fine output voltage regulation with a simple pulse-width modulation scheme. In addition, the native interleaving structure and operation in this converter allows it to support high-current applications similar to multi-phase Buck converters. A 48V to 1-2V/40A prototype has been demonstrated to achieve 94.6% peak efficiency and 425 W/in^3, promising the MPMIH converter to be a good candidate for the PoL converter applications.

Chapter 3, in full, is a reprint of the material as it appears in "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 25-29 by the authors Das, Ratul; Seo, Gab-Su; Maksimovic, Dragan and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 4

A Regulated 48V-to-1V/100A 90.9% Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems

4.1 Introduction

Considering stringent space and load constraints, non-isolated hybrid DC-DC converter topologies have shown promising results. Notable examples include the 48V-to-1V converter reported in [40] aiming at high efficiency and high power density and the 120V-to-0.9V converter in [39] demonstrating extremely large direct conversion ratios. Employing a dual-inductor hybrid (DIH) converter architecture, both converters demonstrated high efficiencies in a moderate load range up to 20A. However, the need for a precise capacitor sizing strategy in [39] or a split phase operation in [40] creates undesirable design complexities that would in turn limit performance at heavier loads. Related works preceding these implementations include the Flying Capacitor Multi Level (FCML) converter reported in [34], the Hybrid Dickson converter in [35, 36], and the multiphase series capacitor Buck converter in [51, 52]. These interesting approaches for non-isolated POL converters still have various shortcomings. Particularly, the FCML converter needs a capacitor voltage balancing circuit, the Hybrid Dickson converter requires a split-phase control and published implementations of the series capacitor Buck converter exhibits efficiency

limited to ~90% for a conventional 12V-to-1V conversion. The need for higher efficiency is perhaps self-evident, but a larger conversion ratio, low output voltage, and extremely high output currents are also critical since they are directly related to the space overhead, and thermal management and hence cost of the input bus distribution, and to enable technology scaling of the load process.

In order to explore the boundaries of hybrid converter capabilities, in this chapter, we introduce, analyze and demonstrate a Dual-Phase Multi-Inductor Hybrid (DPMIH) converter), shown in Fig. 4.1. The DPMIH converter is derived as a continuation of work from the Dual Inductor Hybrid (DIH) converters [39, 40], and leverages similarities to the series capacitor Buck converter [53,54]. Section 4.2 describes the converter operation and key characteristics, including complete soft-charging operations of all flying capacitors without any specific capacitor sizing or split phase control, an inherent capability of providing less voltage stress across switches and inductors, and the benefits of natively balanced inductor currents. Section 4.4 presents experimental results that validate advantageous characteristics in enabling a DPMIH converter prototype to support large conversation ratios from a 48V input to 1V-5V output at a maximum the current of 100 A, and a maximum load of 500W. Section 4.5 concludes the chapter.

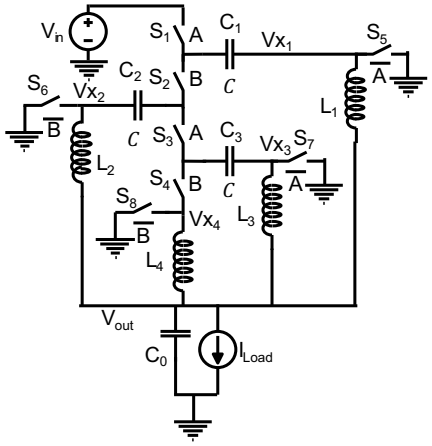
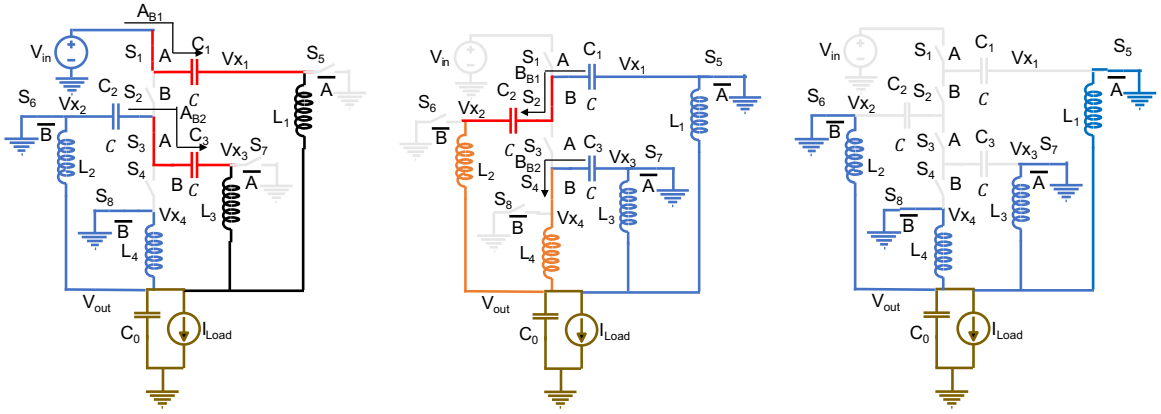


Figure 4.1. Dual-phase multi-inductor hybrid (DPMIH) converter



(a) State 1(Phase A) **(b)** State 3 (Phase B) **(c)** States 2 and 4

Figure 4.2. Operating states of the DPMIH converter

4.2 Operation of the DPMIH Converter

Theis chapter focuses on a four-level version of the DPMIH converter, ignoring the zero level. It is called a 4-to-1 DPMIH converter where four is the number of voltage divisions created by the switched capacitor network. The converter circuit is shown in Fig. 4.1. The converter employs three flying capacitors, four output inductors, and eight switches. As shown in Figs. 4.2 and 4.3, the converter is operated with 4 switching states within a switching cycle T_S where

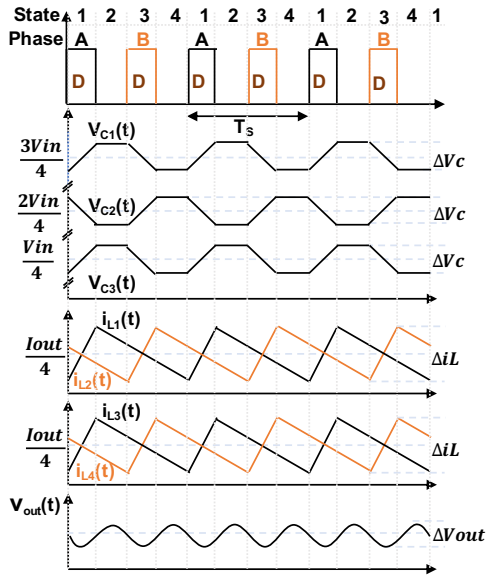


Figure 4.3. Operational waveforms of the DPMIH converter

States 1 and 3 are also named energizing phases A and B, respectively. In Fig. 4.2, the red color represents the capacitors getting charged while blue implies discharging. The charged inductors in Fig. 4.2 have the correspondingly matching color in the inductor current waveforms of Fig. 4.3.

The first three inductors and flying capacitors form three inductor-capacitor pairs where each capacitor C_i is directly connected to and soft-charged by inductor L_i in a charging phase, A or B. The last inductor L_4 only handles soft discharging for the capacitor C_3. The capacitors are open-circuited and inactive during States 2 and 4. Every inductor is charged in one energizing phase, A or B, and discharges to the output during the other energizing phase and in States 2 and 4. The converter operation converges to a steady state as each capacitor gets an equivalent charge and discharge once in every cycle, leading to native capacitor voltage balance and inductor current balance. Charge for each capacitor comes from either input voltage source for C_1 or from a capacitor at an immediate higher level in case of C_2 and C_3. In other words, flying capacitors discharge to their immediate lower-level capacitors and inductors except for C_3, which discharges directly to L_4.

Assuming small voltage ripples in the capacitors and inductor volt-second balance, the steady-state voltages for C_1, C_2, and C_3 are found as $\frac{3V_{in}}{4}$, $\frac{2V_{in}}{4}$, and $\frac{V_{in}}{4}$, respectively.As the result, the four inductors L_{1-4} are switched by the same voltage swing of $\frac{V_{in}}{4}$ at switching nodes V_{X1-X4}. Each inductor has a charging duty cycle D, i.e. in Phase A or B, making the output voltage $V_{out} = \frac{DV_{in}}{4}$. This intuitive conversion ratio result implies a straightforward duty cycle control, allowing for a simple and efficient output voltage regulation. General expressions for steady-state voltages at the output and across the flying capacitors for an N-to-1 DPMIH converter are given as:

$$V_{out} = \frac{DV_{in}}{N} \text{ and } V_{C_k} = \frac{(N-k)V_{in}}{N} \text{ , } where, k = 1, 2, ..., N-1 \tag{4.1}$$

For the intended operation of the converter, while Phases A and B need to stay non-overlapped,

Table 4.1. Switching node voltages in energizing states

Switching node voltages	State 1 (Phase A)		Switching node voltages	State 3 (Phase B)	
	Start	End		Start	End
$Vx_1(A_{B1})$	$\frac{V_{in}}{4}+\frac{\triangle V_C}{2}$	$\frac{V_{in}}{6}-\frac{\triangle V_C}{2}$	$Vx_2(B_{B1})$	$\frac{V_{in}}{4}+\triangle V_C$	$\frac{V_{in}}{4}-\triangle V_C$
$Vx_3(A_{B2})$	$\frac{V_{in}}{4}+\triangle V_C$	$\frac{V_{in}}{6}-\triangle V_C$	$Vx_4(B_{B2})$	$\frac{V_{in}}{4}+\frac{\triangle V_C}{2}$	$\frac{V_{in}}{4}-\frac{\triangle V_C}{2}$

they are not required to be evenly distributed in the switching cycle. In general, a uniform distribution of interleaving phases is preferred since it minimizes the output current and voltage ripples and enables load transient improvements as similarly found in multi-phase Buck converters.

4.3 Native Soft-Charging and Analysis of Switching Node Voltages

Native Soft-charging Feature

The key reason why this DPMIH converter can achieve complete soft charging for all flying capacitors is evident in its operation in which every capacitor is charged or discharged by an inductor in series. No capacitor is shorted in parallel with another capacitor or a low impedance source, and thus no capacitor hard charging. This beneficial soft charging is achieved natively without any complicated split-phase control [35, 40] or capacitor sizing strategy [39]. Native soft charging is also achieved regardless of variations and mismatches in flying capacitor values that are oftentimes unavoidable because of different bias voltages and manufacturing tolerance.

Analysis of the Switching Node Voltages

As described in the operation of the DPMIH converter in Section 4.2, all inductors experience an average voltage swing of $\frac{V_{in}}{4}$ and carries an equal average current of $\frac{I_{out}}{4}$. When charging and discharging the flying capacitors, this inductor current generates a voltage ripple of $\triangle V_C$ across each flying capacitor. In other words, the voltage across each flying capacitor has the same swing of $\frac{\triangle V_C}{2}$ in addition to its steady-state average voltage. However, in the operation

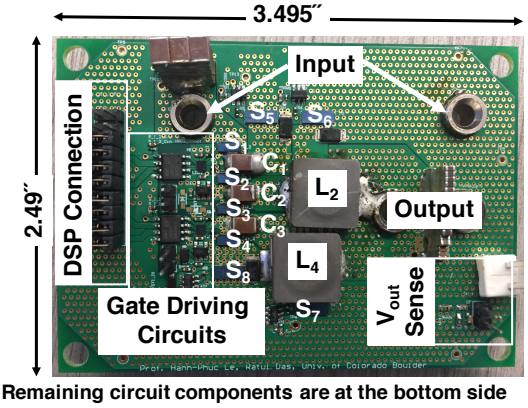


Figure 4.4. A 4-to-1 100-W DPMIH converter prototype

of the converter shown in Fig. 4.2, the charging branches, A_{B1}, A_{B2}, B_{B1}, and B_{B2} in the two phases, A and B have different numbers of capacitors, i.e. one or two capacitors. Therefore, the voltage swings at the switching nodes $V_{X1\text{-}X4}$ have different values, as detailed in Table 4.1. Specifically, during the charging phase V_{X2} and V_{X3} experience twice the voltage ripple of V_{X1} and V_{X4}, leading to larger variations in the current slope L_2 and L_3 compared with L_1 and L_4 during the energizing phase. However, note that if this $\triangle V_C$ is small compared with $\frac{V_{in}}{4}$, the difference in the inductor currents are insignificant. In addition, regardless of this small inductor current mismatch 1) each inductor still maintains a steady periodic waveforms every cycle, and 2) the feature of native soft-charging for all the flying capacitors described above is preserved.

Table 4.2. Major components

Components	Part information
$S_{1,2,3,4}$	2xEPC2015c
$S_{5,6,7,8}$	2xEPC2023
C_1	5.8uF 100V TDK
C_2	5uF 100V TDK
C_3	4.3uF 100V TDK
L_{1-4}	1uH Vishay
Isolators	Si8423
Gate Drivers	LM5114, LMG1205

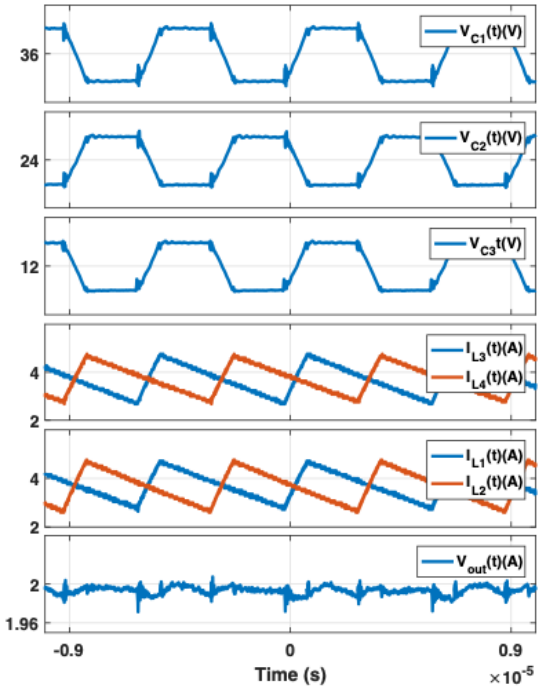


Figure 4.5. Measured waveforms of the DPMIH converter in a 48V-to-2V/15A conversion

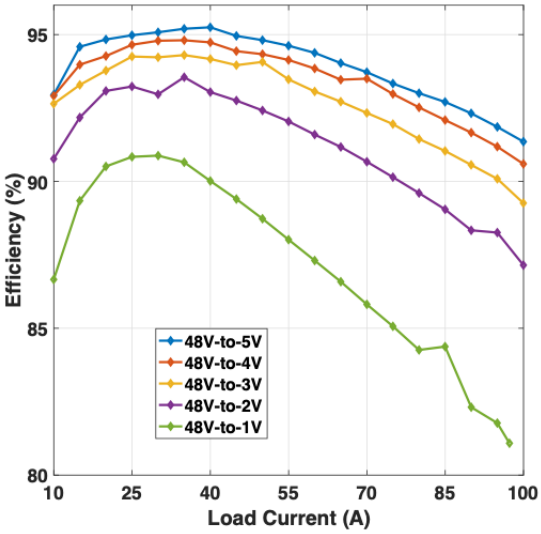


Figure 4.6. Measured efficiency of the DPMIH converter operated at 333 kHz.

Table 4.3. Comparison chart

Characteristics	DIHC [40]	Series Capacitor Buck [51]	DPMIH converter (This chapter)
Input voltage	40-54 V	12 V	48 V
Output voltage	1-2 V	0.6-1 V	1-5 V
Maximum load current	10 A	60 A	100 A
Maximum power	20 W	60 W	500 W
Number of levels	6	4	4
Capacitor sizing and split phase control	Required	Not required	Not required
Peak efficiency	93% @ 1V/4A	90.3% @ 1V/15A	90.9% @ 1V/30A

4.4 Experimental Results

In order to validate the converter operations and advantageous characteristics, a DPMIH converter prototype depicted in Fig. 4.4 was implemented. The key components used in the design are listed in Table 4.2. Steady-state waveforms of the four inductor currents, three flying capacitor voltages, and the output voltage are shown in Fig. 4.5, verifying the converter operation as described in section 4.2. In these experimental waveforms, the converter was operated at 167 kHz switching frequency, converting a 48V input to a 2V output and 15A load. This switching frequency was specifically chosen to create large ripples on the flying capacitor voltages and inductor currents for convenient measurements. The flying capacitor voltage waveforms in Figure 4.5 prove that soft charging is achieved for all flying capacitors while the inductor current waveforms demonstrate uniform current distribution for all inductors. To obtain the efficiency in Fig. 4.6, the converter was operated at an optimal switching frequency of 333 kHz for voltage conversions from a 48V input supply to an output regulated at 1V to 5V with a load current up to 100 A. The converter achieves peak efficiencies of 90.9% for a 1V/30A output, 93.6% for 2V/35A and 95.3% for 5V/40A. The efficiency measurements take into account all the powertrain components as well as gate driving losses. Considering key power conversion components, the converter achieves a power density of 440 W/in^3 at 1V and 2200 W/in^3 at 5V and a current

density of 440 A/in^3.

The DPMIH converter prototype is compared to previous works in Table 4.3. Compared with the series capacitor Buck converter [51], this DPMIH converter achieves a similar peak efficiency for 1-V output while supporting 4X conversion ratios, i.e. from 48V input instead of 12V, 1.6X maximum current capability, and 2X current at peak efficiency. Compared with the DIH converter in [40],it achieves 10X maximum output current and 25X output power.

4.5 Chapter Summary

In this chapter, a Dual-Phase Multi-Inductor Hybrid (DPMIH) converter was presented with operation analysis and experimental results. The converter exhibits a superior configuration and performance at higher loads compared with the state-of-the-art designs because of its unique hybrid topology configuration and operation that enables complete native soft charging in all flying capacitors without requiring any complex control or capacitor sizing method. A 500-W experimental prototype successfully demonstrates the intended operation and characteristics, achieving 90.9% peak efficiency for a 48V-to-1V conversion and regulating an output up to 5 V with loads up to 100A.

Chapter 4, in full, is a reprint of the material as it appears in "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 1997-2001 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Part II

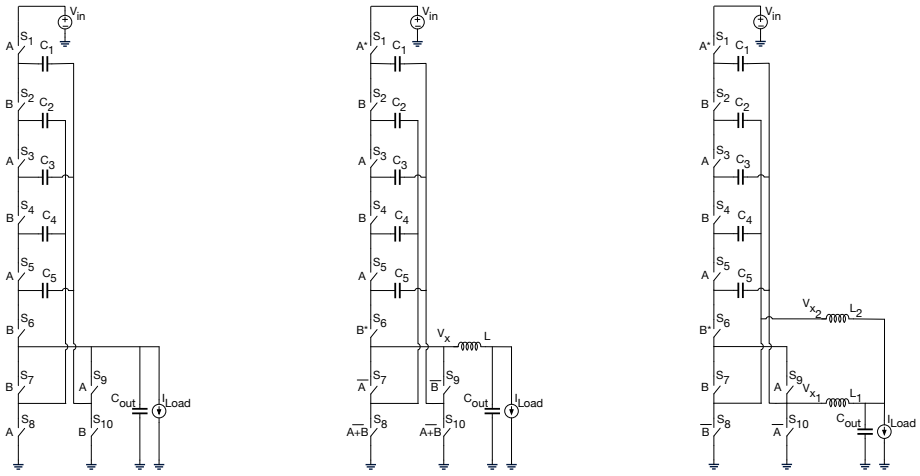
Techniques Related to Multi-Inductor Hybrid Converters

Chapter 5

Multi Inductor Hybrid Converter Family: Synthesis and Small Signal Analysis

5.1 Introduction

In the fast-moving field of power electronics, switched capacitor (SC) based multilevel hybrid converters have taken place in many applications. In this trend, a new family of hybrid converters, Multi Inductor Hybrid (MIH) converters, have proved their essence in high conversion ratio DC-DC applications, especially for data centers and telecommunications systems. With the progress of cloud-based computing, data storage, and the introduction of 5G in communication, there is a huge load on the existing architectures of power delivery in data centers and telecommunication systems. In these architectures, the most challenging loads are the high-performance processors, which require very small voltages of 1-3.3V but very huge currents to operate. The recent trend is to push the bus voltage of the last centimeter converter to 48V from 12V so that its distribution current is smaller. To perform the voltage conversion of 48V to 1-3.3V, recently, several Multi Inductor Hybrid (MIH) converters have been proposed [16, 17, 39, 40, 49, 55, 56]. These converters redefined state of the art, and several recent publications followed the structure of these converters to have high output currents for data center applications [57, 58]. Where previous publications focused on the performance and topology demonstration and, in some cases, details of individual converters [15, 41], we have included a more general perspective of this converter family here targeting the synthesis, techniques, and small signal analysis of the



(a) Dickson SC Converter

(b) Hybrid Dickson Converter

(c) Early Dual Inductor Hybrid Converter

Figure 5.1. Initial synthesis of dual inductor hybrid Converter

converters in this chapter.

The techniques for synthesizing these converters are equally important as the quantitative performance. As previous chapters listed some individual converters, their operation and techniques are only related to individual converters; here, in this chapter, the synthesis and control techniques for all the MIH converters are presented. We will present the synthesis of different converters in section 5.2. Section 5.3 includes small signal modeling of the member converters based on averaged circuit modeling. Section 5.4 concludes the chapter.

5.2 Multi-Inductor Hybrid Converter Family and Synthesis

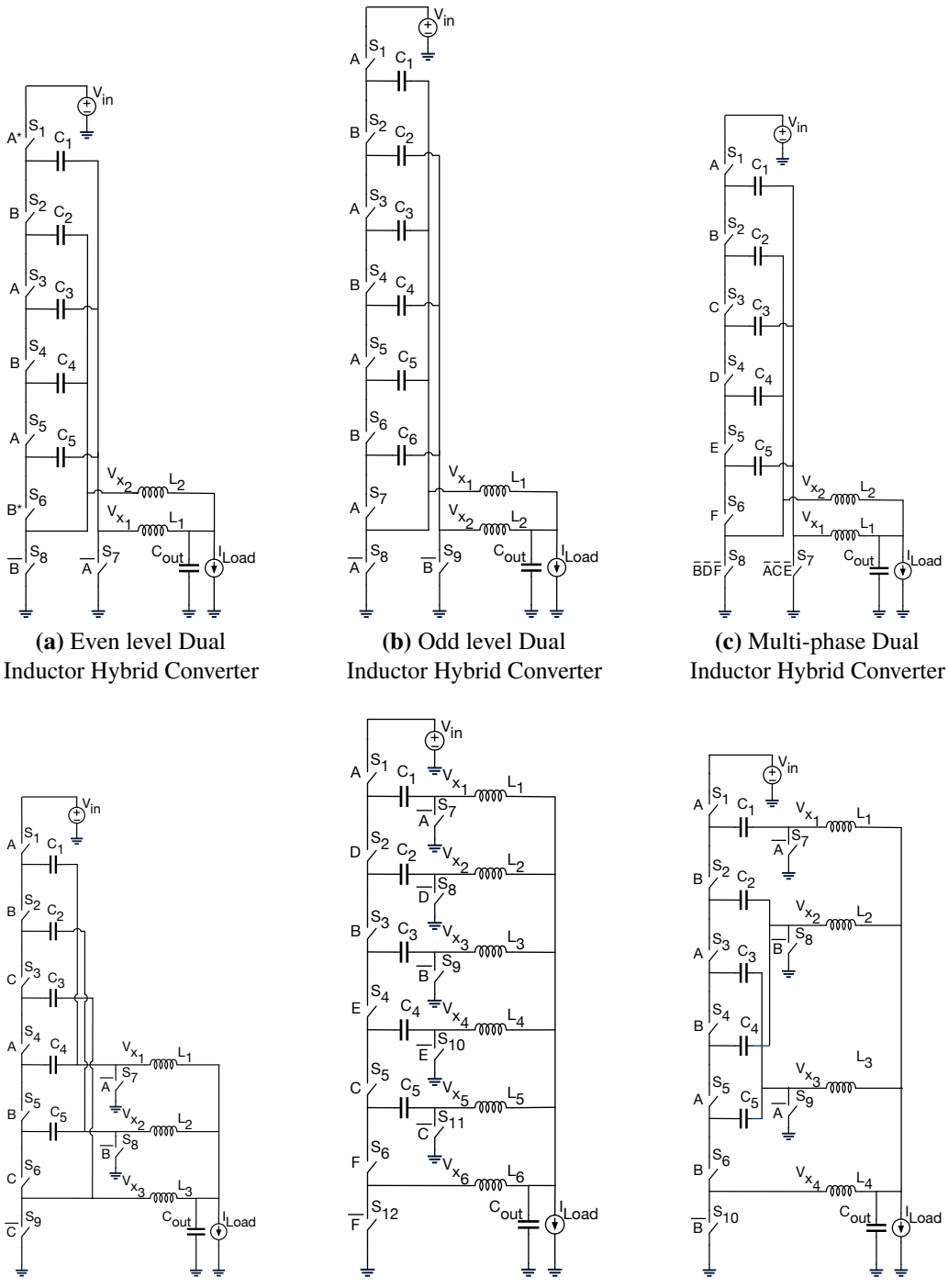
The expansion of research on hybrid converters started with merging a switched capacitor converter and a switched inductor converter to have the benefits of very fast regulation, and in the process, soft-charging was achieved on the switched capacitors, which resulted in more efficient and power-dense design was possible [59]. The research continued blooming while inductors were directly inserted into different traditional switched capacitor architectures to have similar benefits [26, 60, 61]. Flying Capacitor Multi-Level hybrid converters were already very

popular for a long time for inverter application [62, 63], which are essentially switched capacitor converters with inductors inserted for different reasons. Over the years, these converters also became popular in DC-DC applications because of their advantages resulting in low voltage stress on active and passive devices [34, 64]. Continuing this trend, an inductor was inserted in Dickson Star switched capacitor converter (Fig. 5.1a), and a hybrid Dickson converter (Fig. 5.1b) was demonstrated [36]. This converter achieved an average conversion ratio with very high efficiency. A significant innovation to achieve high efficiency in this converter was near soft-charging by split phase operation [35]. Although the conversion ratio of this converter can be increased by increasing the number of levels in the switched capacitor structure, it was not clear how to increase the output current of this converter which was limited mainly by the saturation current of the inductor.

On the other hand, modern applications require high output current and high conversion ratios. For high-output current converters, a significant limitation of performance emerges from the ESR of the inductor just before the output. To overcome this and achieve a very high current, it is common to use multiple inductors or converters sharing the very high current [65]. We have modified the traditional Dickson Star SC converter from this perspective and derived a family of MIH converters suitable for high conversion ratio high current applications. Our motivation was to achieve a high current at the output and understand the residual hard-charging and explore techniques to remove it. In subsequent discussions, we presented multiple MIH converters, each representing the uniqueness of its configurations and characteristics. However, it should also be noted that there can be numerous modifications of the topologies, and our goal is not to list all of them but rather to describe the logical flow of the synthesis and uniqueness resulting from each topological modification.

5.2.1 Dual Inductor Hybrid (DIH) Converter

A Hybrid Dickson converter was derived in [60] by adding one inductor in the traditional Dick Star switched-capacitor converter. Dickson Star switched capacitor converter, and Hybrid



(a) Even level Dual Inductor Hybrid Converter

(b) Odd level Dual Inductor Hybrid Converter

(c) Multi-phase Dual Inductor Hybrid Converter

(d) Multi-phase Multi-Inductor Hybrid Converter

(e) Series Capacitor Buck Converter

(f) Optimal inductor Hybrid Converter

Figure 5.2. Multi-inductor hybrid converter family

Dickson converter are depicted in Fig. 5.1a and 5.1b, respectively. However, we observed that in traditional Dickson Star switched-capacitor converter (Fig. 5.1a), switching nodes between S_7 and S_8, and between S_9 and S_{10} switches between V_{in}/N and 0 where N is the number of levels in the converter. So, it is possible to attach two inductors at those two nodes and get a two-inductor converter as in Fig. 5.1c to serve an output at a different location than the previous position. This converter is more suitable for high current operations than the Hybrid Dickson converter in Fig. 5.1b. However, this converter can be significantly modified by removing three switches from the architecture and finally deriving the final Dual Inductor Hybrid (DIH) converter in Fig. 5.2a and Fig. 5.2b. Compared with a Hybrid Dickson converter (Fig. 5.1b), a Dual Inductor Hybrid converter can have an odd or even number of levels. An N-level DIH converter has an N-1 number of capacitors and an N+2 number of switches. Among the switches, two switches are connected to the ground level. Other N switches are high-side switches. DIH converters are operated with two 180°phase-shifted signals for the switches. Depending on the odd or even number of levels, DIH converters significantly differ in their characteristics.

Even Level

Even level Dual inductor converters can not be fully soft-charging even if the converter architecture tries to route all the charging and discharging currents of the capacitors through the inductors. Impedance mismatches from the series and parallel combination of the flying capacitors result in the current flow between separate capacitor branches connected only through the switching nodes. [41] also discussed the adopted split-phase operation previously introduced for Hybrid Dickson in [35] to reduce the hard-charging in the converter.

Odd Level

Parent Dickson converter requires equal capacitance for each capacitor as they process the same charge. Odd-level DIH converters can be fully soft-charging if the capacitance is chosen with a specific ratio instead of equal capacitance [15]. This property also makes it a

better choice for extreme conversion ratio applications where duty cycles are relatively smaller, and split-phase operations are unsuitable. However, odd-level implementations also introduce uneven inductor current in the dual inductor. Using different duty cycles for the two phases can solve this issue [15].

5.2.2 Multi-Phase Dual-Inductor Hybrid (DIH) Converter

The subsequent modification in the converter architecture came from the realization that the operation in the converter is not limited to two phases anymore when there are two inductors in the structure. Multiple phases can be applied to the same inductor while increasing the number of inductor charging intervals. This principle also coincides with the FCML converters, for example, 3-level Buck converter [66], or 4-level Buck converter [64]. The same principle can be applied to the Dual inductor hybrid converters, leading to fully soft-charging operation. A 6-level 6-phase DIH converter was implemented in [49]. This converter provides a complete soft-charging operation without the use of split-phase [35], or capacitor sizing [39]. Each inductor in this converter experiences three charging intervals, so the required inductance can be significantly reduced.

5.2.3 Multi-Inductor Hybrid Converter

Many applications targets very high currents at the output, and their currents become limited by the number of inductors and their current capabilities. To sustain the high current operation, multi-phase Buck converters are well-adopted [67]. Therefore, multi-phase operation in the switched cap architecture motivates the idea of applying multiple phases to multiple inductors to support high currents. From this idea, another inductor was inserted into a regular dual inductor converter to make a 3-inductor hybrid converter [16]. This converter is depicted in Fig. 5.2d. In this converter, the same inductor shares multiple branches of capacitors to soft-charge and discharge each. However, when multiple branches are connected with the same inductors, capacitor sizing is required to achieve complete soft charging.

5.2.4 Series Capacitor Buck (SCB) Converter

From the other members of the MIH converter family, it can be seen that only inductors in the architectures do not guarantee a complete soft-charging operation. Split-phase operation or capacitor sizing has been adopted to make the converters complete soft charging. It can also be seen that residual hard-charging only happens between different capacitor branches connected with the same inductor. Hence, it is understood that if only one capacitor branch is allowed to connect with the same inductor simultaneously, no hard charging can happen. This leads to the converter in Fig. 5.2e. This converter can be operated with any number of phases between 2 and 6 if only one phase is allowed on one inductor. The 6-phase operation essentially reduces the output current ripple significantly. However, it also reduces the maximum amount of the duty cycles of the phases and, thereby, the range of output voltages the converter can regulate. Hence, in some applications, reduced phase operation may be necessary. One experimental validation of this converter with 4-level 4-inductor can be found in chapter 4. The 6-level 6-inductor version is implemented in chapter 11.

Although this converter has been derived from the Dickson SC converter through the DIH and MIH converters, converters with similar structures can be found in literature [53, 54]. Interestingly, similar converters can be derived from different perspectives separated by time, philosophy, and goals. This phenomenon is quite common, especially for power converters [68].

5.2.5 Optimal Inductor Hybrid Converter

As mentioned earlier, our investigation was motivated by both achieving high current at the output and eliminating the residual hard-charging in the converter. Although the Series capacitor Buck converter (Fig. 5.2e) can achieve both, not all applications require very high current at the output. Moreover, eliminating hard-charging by using an inductor for every branch requires the number of inductors equal to the number of levels, which is not acceptable in very high conversion ratios but low output current applications. Thus, a high number of inductors used

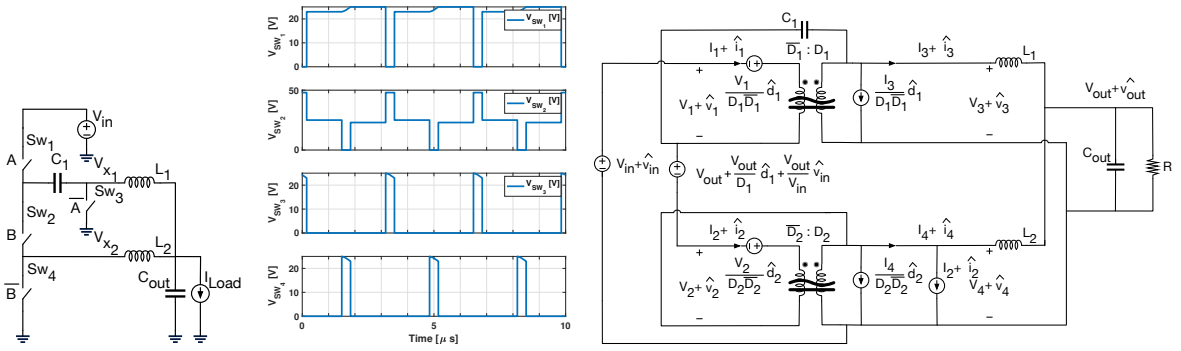
Table 5.2. Parameters for analytical verification with simulation

Parameters	2-level Series Capacitor Buck Converter	7-level Dual Inductor Hybrid Converter	6-level Series Capacitor Buck Converter
Input Voltage, V_{in}	48V	48V	48V
Duty Cycles, D	0.1	0.1	0.1
Frequency, F_S	300kHz	300kHz	300kHz
Inductor, L	560nH	560nH	560nH
Flying Capacitor, C_f	2μF	2μF*	2μF
Output Capacitor, C_{out}	40μF	40μF	40μF
Load Resistor, R_{load}	0.1Ω	0.05Ω	0.05Ω
*Minimum Capacitance, subject to capacitor sizing			

can not be allowed as they are the worst component in terms of power density in the converter. This perspective motivated the idea of an optimal inductor hybrid converter in Fig. 5.2f. Four inductors in this converter are enough to ensure all capacitors are always softly charged and discharged. Even if the number of levels increases, these four inductors can make the full converter soft charging. While implementing, only the top and bottom capacitor branches are required to be connected with separate inductors, while all other capacitor branches can be grouped into two categories, each category being connected with separate inductors. Note that this converter also leads to unequal inductor currents as in odd-level Dual inductor converter. Inductors $L_{1,4}$ can be selected with lower saturation current and thus smaller size compared to inductors $L_{2,3}$ to increase the effective power density.

5.3 Small Signal Model Based on Averaged Circuit Modeling

Depending on the number of levels, the number of inductors, the connection of the capacitors and the inductors, and the number of phases, there can be numerous MIH converters. Because of a significantly larger number of capacitors and inductors, small signal analysis of any member converter is extremely difficult. Moreover, there is no established rule for simplified small signal analysis for hybrid converters. Most research focused on complex mathematical

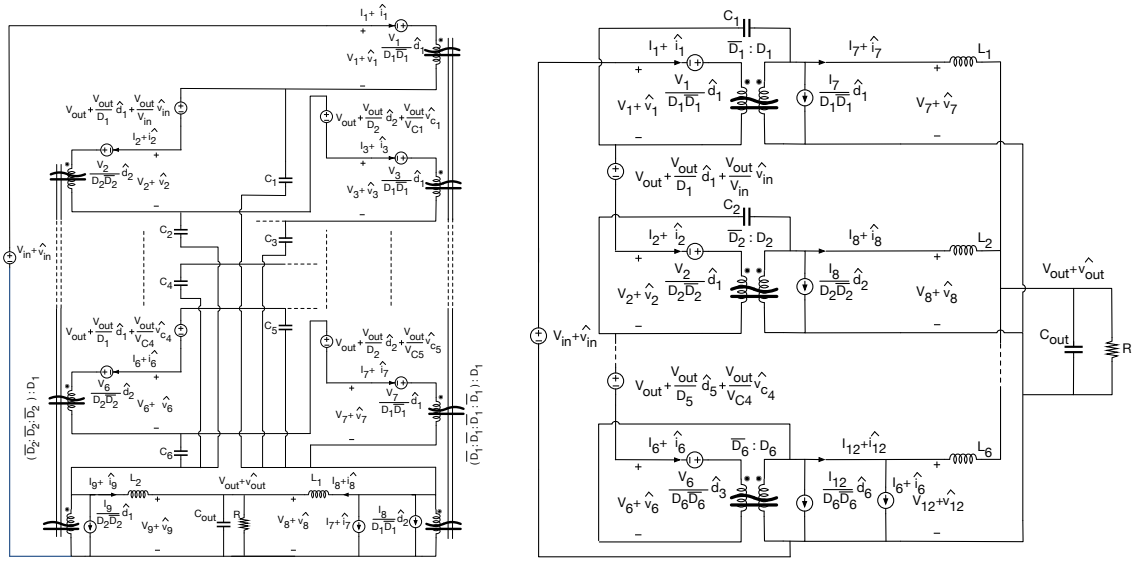


(a) 2-level series capacitor Buck converter

(b) Switch voltage stress of 2-level series capacitor Buck converter

(c) Small signal model of 2-level series capacitor Buck Converter

Figure 5.3. 2-level series capacitor Buck converter and its small signal model



(a) Small signal model of 7-level DIH converter (5.2b)

(b) Small signal model of 6-level series capacitor Buck converter (5.2e)

Figure 5.4. Small signal model of notable MIH converters

analysis. To analyze the MIH converters, a general method of analysis is required to be established to simplify the analysis. The averaged circuit modeling of simpler hybrid converters, for example, the Cuk and SEPIC converter where a flying capacitor works as an energy transfer element can be looked back in this case [69]. In this method, a pair of switches are identified with complementary ON and OFF time, and their voltage and current waveforms are averaged, perturbed, and linearized to determine an averaged circuit model. After that, complimentary

Table 5.1. Transfer functions of notable MIH converters

Converter	Transfer function	Expression	Simplified Expression ignoring pole-zero doublets
2-level SCBC	$G_{vg}(s)$	$\frac{\frac{D}{2}\frac{(2+D)}{2}\left(s^2+\frac{2D^2(2-D)}{LC_f(2+D)}\right)}{\left(s^2+\frac{D^2(2-D)}{LC_f}\right)\left(s^2\frac{L}{2}C_{out}+s\frac{\frac{L}{2}}{R}+1\right)}$	$\frac{\frac{D}{2}}{\left(s^2\frac{L}{2}C_{out}+s\frac{\frac{L}{2}}{R}+1\right)}$
	$G_{vd}(s)$	$\frac{\frac{V_{in}}{2}\left(s^2+\frac{D^2(2-D)}{LC_f}\right)}{\left(s^2+\frac{D^2(2-D)}{LC_f}\right)\left(s^2\frac{L}{2}C_{out}+s\frac{\frac{L}{2}}{R}+1\right)}$	$\frac{\frac{V_{in}}{2}}{\left(s^2\frac{L}{2}C_{out}+s\frac{\frac{L}{2}}{R}+1\right)}$
6-level SCBC	$G_{vg}(s)$	$\frac{\frac{D}{6}\begin{bmatrix} s^{10}\left(120L^5C_f^5\right)\left(6+5D+5D^2+5D^3+5D^4+5D^5\right) \\ +s^8L^4C_f^4\begin{pmatrix}7200D^2-624D^3+5262D^4-190D^5+4182D^6\\ -1916D^7+406D^8-1136D^9+666D^{10}-240D^{11}\end{pmatrix} \\ +s^6L^3C_f^3\begin{pmatrix}25920D^4-20976D^5+27572D^6-19187D^7+15281D^8\\ -14116D^9+5575D^{10}-1592D^{11}+40D^{12}\end{pmatrix} \\ +s^4L^2C_f^2\begin{pmatrix}40320D^6-51324D^7+51412D^8-41157D^9\\ +17271D^{10}-6147D^{11}+674D^{12}+40D^{13}\end{pmatrix} \\ +s^2LC_f\left(25200D^8-35604D^9+21452D^{10}-10619D^{11}+2040D^{12}\right) \\ +\left(4320D^{10}-6264D^{11}+2040D^{12}-90D^{13}\right)\end{bmatrix}}{6\left(s^2\frac{L}{6}C_{out}+s\frac{L/6}{R}+1\right)\begin{bmatrix} s^{10}\left(120L^5C_f^5\right) \\ +s^8L^4C_f^4\begin{pmatrix}1200D^2-1080D^3+806D^4-746D^5+626D^6\\ -546D^7+426D^8-336D^9+216D^{10}-120D^{11}\end{pmatrix} \\ +s^6L^3C_f^3\begin{pmatrix}4320D^4-6874D^5+6824D^6-6312D^7\\ +5093D^8-3692D^9+2114D^{10}-854D^{11}\end{pmatrix} \\ +s^4L^2C_f^2\begin{pmatrix}6720D^6-13430D^7+14148D^8-11340D^9\\ +6648D^{10}-2495D^{11}+130D^{12}\end{pmatrix} \\ +s^2LC_f\left(4200D^8-8434D^9+7177D^{10}-3294D^{11}+440D^{12}\right) \\ +\left(720D^{10}-1044D^{11}+340D^{12}-15D^{13}\right)\end{bmatrix}}$	$\frac{\frac{D}{6}}{\left(s^2\frac{L}{6}C_{out}+s\frac{\frac{L}{6}}{R}+1\right)}$
	$G_{vd}(s)$	$\frac{\frac{V_{in}}{6}\begin{bmatrix} s^{10}\left(120L^5C_f^5\right) \\ +s^8L^4C_f^4\begin{pmatrix}1200D^2-1080D^3+806D^4-746D^5+626D^6\\ -546D^7+426D^8-336D^9+216D^{10}-120D^{11}\end{pmatrix} \\ +s^6L^3C_f^3\begin{pmatrix}4320D^4-6874D^5+6824D^6-6312D^7\\ +5093D^8-3692D^9+2114D^{10}-854D^{11}\end{pmatrix} \\ +s^4L^2C_f^2\begin{pmatrix}6720D^6-13430D^7+14148D^8-11340D^9\\ +6648D^{10}-2495D^{11}+130D^{12}\end{pmatrix} \\ +s^2LC_f\left(4200D^8-8434D^9+7177D^{10}-3294D^{11}+440D^{12}\right) \\ +\left(720D^{10}-1044D^{11}+340D^{12}-15D^{13}\right)\end{bmatrix}}{\left(s^2\frac{L}{6}C_{out}+s\frac{L/6}{R}+1\right)\begin{bmatrix} s^{10}\left(120L^5C_f^5\right) \\ +s^8L^4C_f^4\begin{pmatrix}1200D^2-1080D^3+806D^4-746D^5+626D^6\\ -546D^7+426D^8-336D^9+216D^{10}-120D^{11}\end{pmatrix} \\ +s^6L^3C_f^3\begin{pmatrix}4320D^4-6874D^5+6824D^6-6312D^7\\ +5093D^8-3692D^9+2114D^{10}-854D^{11}\end{pmatrix} \\ +s^4L^2C_f^2\begin{pmatrix}6720D^6-13430D^7+14148D^8-11340D^9\\ +6648D^{10}-2495D^{11}+130D^{12}\end{pmatrix} \\ +s^2LC_f\left(4200D^8-8434D^9+7177D^{10}-3294D^{11}+440D^{12}\right) \\ +\left(720D^{10}-1044D^{11}+340D^{12}-15D^{13}\right)\end{bmatrix}}$	$\frac{\frac{V_{in}}{6}}{\left(s^6\frac{L}{6}C_{out}+s\frac{\frac{L}{6}}{R}+1\right)}$
7-level DIHC	$G_{vg}(s)$	$\frac{\frac{D}{7}R\begin{bmatrix}s^2C_fL\begin{pmatrix}45360+28404D-62772D^2-16415D^3\\ +28127D^4-4962D^5+334D^6-12D^7\end{pmatrix} \\ +\left(35280D^2-56196D^3+23128D^4R-2205D^5\right)\end{bmatrix}}{\begin{bmatrix}s^4C_fC_{out}L^2R\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +s^3C_fL^2\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +s^2 2C_fLR\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +s^2C_{out}LR\left(18000D^2-28428D^3+11866D^4-1170D^5\right) \\ +sL\left(18000D^2-28428D^3+11866D^4-1170D^5\right) \\ +R\left(35280D^2-56196D^3+23128D^4R-2205D^5\right)\end{bmatrix}}$	$\frac{\frac{D}{7}}{\left(s^2\frac{L}{2}C_{out}+s\frac{\frac{L}{2}}{R}+1\right)}$
	$G_{vd}(s)$	$\frac{\frac{V_{in}}{7}R\begin{bmatrix}s^2 2C_fL\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +\left(35280D^2-56196D^3+23128D^4R-2205D^5\right)\end{bmatrix}}{\begin{bmatrix}s^4C_fC_{out}L^2R\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +s^3C_fL^2\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +s^2 2C_fLR\begin{pmatrix}25920-2088D-16458D^2-19989CD^3\\ +16561D^4-2481D^5+167D^6-6D^7\end{pmatrix} \\ +s^2C_{out}LR\left(18000D^2-28428D^3+11866D^4-1170D^5\right) \\ +sL\left(18000D^2-28428D^3+11866D^4-1170D^5\right) \\ +R\left(35280D^2-56196D^3+23128D^4R-2205D^5\right)\end{bmatrix}}$	$\frac{\frac{V_{in}}{7}}{\left(s^2\frac{L}{2}C_{out}+s\frac{\frac{L}{2}}{R}+1\right)}$

operating switches are modeled with transformers with both DC and AC characteristics imposed on them. Then, the Extra-Element theorem is applied to determine the small signal model by comparing it with a Buck-Boost converter.

We analyzed MIH converters with a 2-level Series Capacitor Buck converter (2LSCBC) in Fig. 5.3a. A 2-level Series Capacitor Buck converter is a simple possible converter that can be extended and modified into other MIH converters. There are 4 switches $Sw_{1\text{-}4}$, and $Sw_{1,3}$ are one pair of switches with complementary ON and OFF time, and $Sw_{2,4}$ are the other pair with similar complementary ON and OFF times. If the current ripples are ignored, these pairs carry the same current when any switch is ON. But, when the switches are OFF, they block different magnitudes of voltages. The voltage stresses of the switches are shown in Fig 5.3b. If the ripples associated with the capacitor voltages are ignored, it can be seen that only switch Sw_2 experiences an extra blocking voltage during a portion of its OFF time.

The additional blocking voltage of Sw_2 can be calculated as,

$$V_{b_2} = V_{in} - V_{C_1} = V_{in} - \frac{V_{in}}{\left(\frac{1}{D_1} + \frac{1}{D_2}\right) D_2} = \frac{V_{in}}{\left(\frac{1}{D_1} + \frac{1}{D_2}\right) D_1}$$

To derive V_{b2}, V_{C1} has been used which can be calculated from the volt-second balance equations. This additional voltage appears for the $D_1 T_S$ interval of the switching period. With perturbation and linearization process, we get,

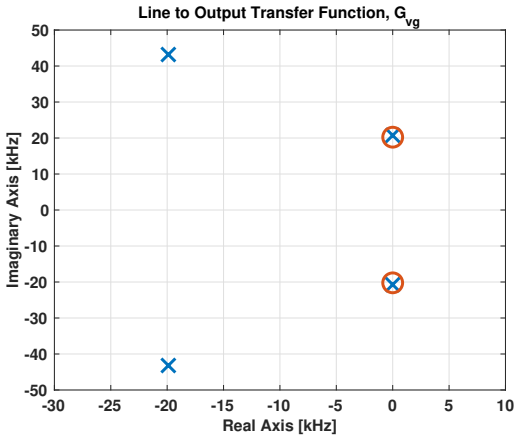
$$\left(V_{b_2} + \hat{V_{b_2}}\right)\left(D_1 + \hat{d_1}\right) = V_{out} + \frac{V_{out}}{D_1}\hat{d_1} + \frac{V_{out}}{V_{in}}\hat{v_{in}} \quad (5.1)$$

Hence, the additional blocking voltage after linearization can be modeled as a separate voltage source. Using standard procedures for averaging voltages and currents and considering the additional blocking voltage, the averaged circuit model can be drawn as in Fig. 5.3c. By analogizing with the 2-level Series Capacitor Buck Converter, the averaged circuit model of

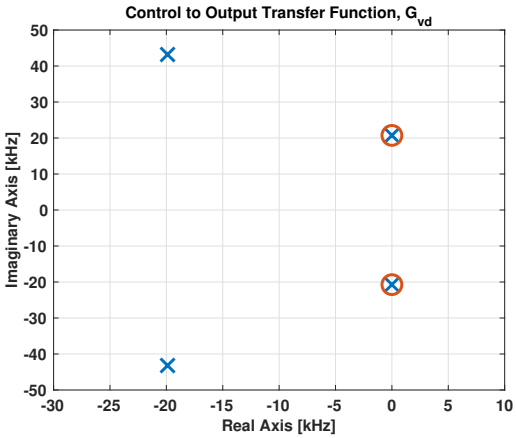
all other member converters can be drawn without further calculation. Example averaged circuit models of a 7-level DIH (7LDIH) converter and a 6-level series capacitor Buck converter (6LSCBC has been provided in Figs. 5.4a and 5.4b.

All these circuit models can be solved with circuit analysis. The Extra-Element theorem becomes exponentially complex to convey this analysis. Rather, we have used a symbolic solver to solve for the line-to-output and control-to-output transfer functions. These transfer functions are listed in Table 5.1. The orders of these transfer functions match the number of passive elements of the converters. As the number of passive elements is large in these converters, the determined transfer functions seem impractical to use for designing the control loop at first glance.

These transfer functions are plotted and compared with a simulation setup to verify the analysis in Figs. 5.8, 5.9 and 5.10. The numerical conditions of the simulation setup are listed in Table 5.2. The pole and zeroes of these transfer functions are mapped in Figs. 5.5, 5.6 and 5.7. From the frequency domain plots of the transfer functions in Figs. 5.8, 5.9 and 5.10 and the pole-zero mapping in Figs. 5.5, 5.6 and 5.7, it can be seen that all zeroes almost coincide with similar number poles or they make pole-zero doublets. Only two complimentary poles remain in all the transfer functions. This observation simplifies the complex transfer functions in Table 5.1.

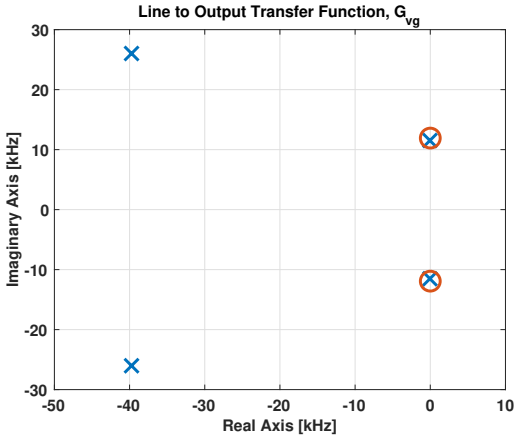


(a) Line to output

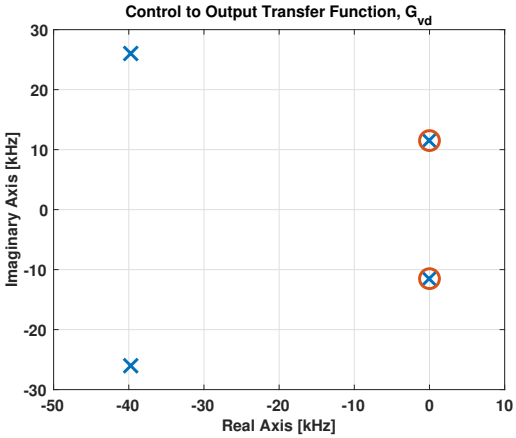


(b) Control to output

Figure 5.5. Pole-Zero mapping of the small signal transfer functions of 2LSCBC

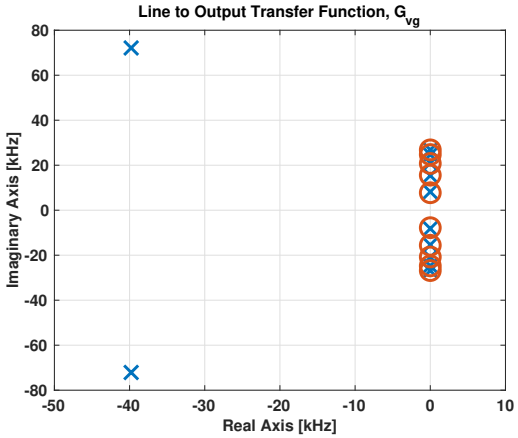


(a) Line to output

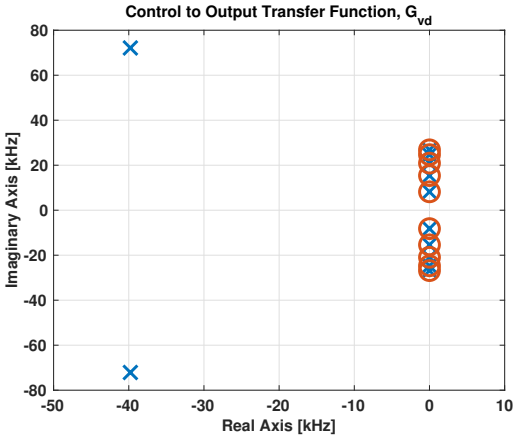


(b) Control to output

Figure 5.6. Pole-Zero mapping of the small signal transfer functions of 7LDIHC

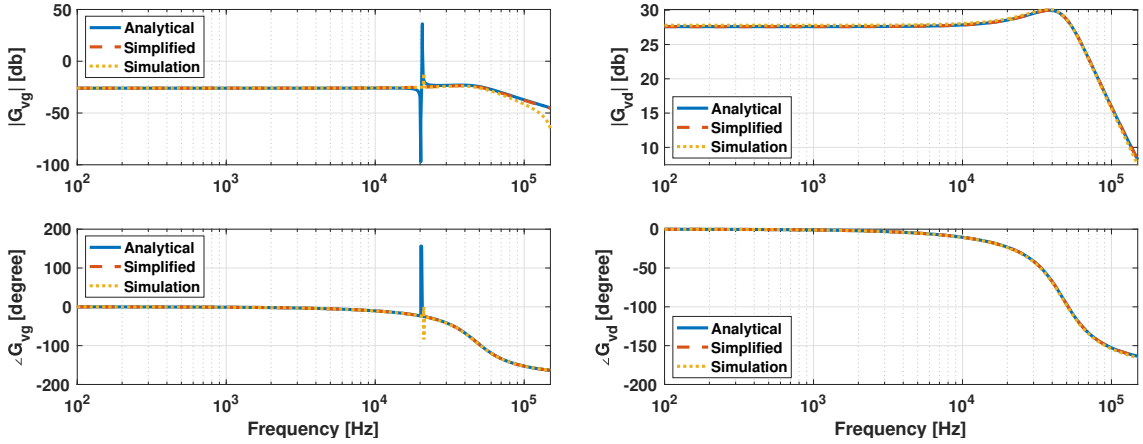


(a) Line to output



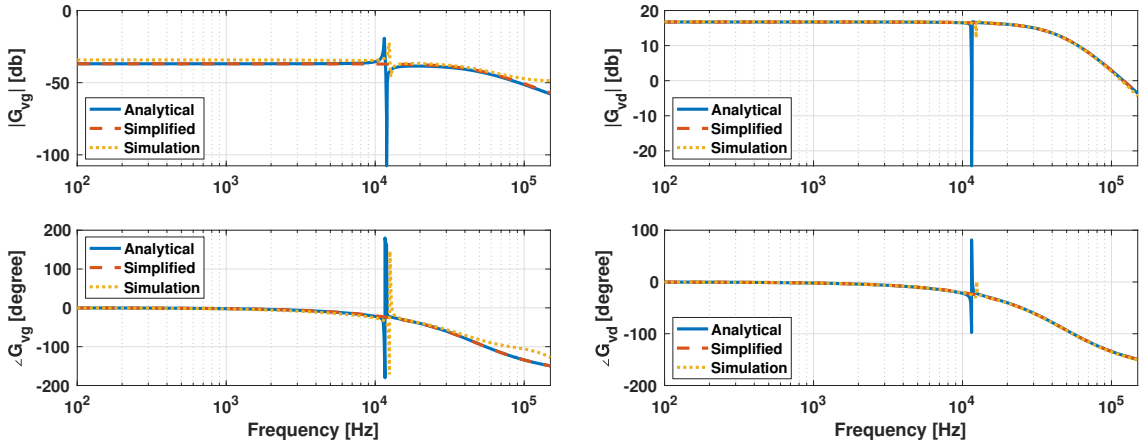
(b) Control to output

Figure 5.7. Pole-Zero mapping of the small signal transfer functions of 6LSCBC



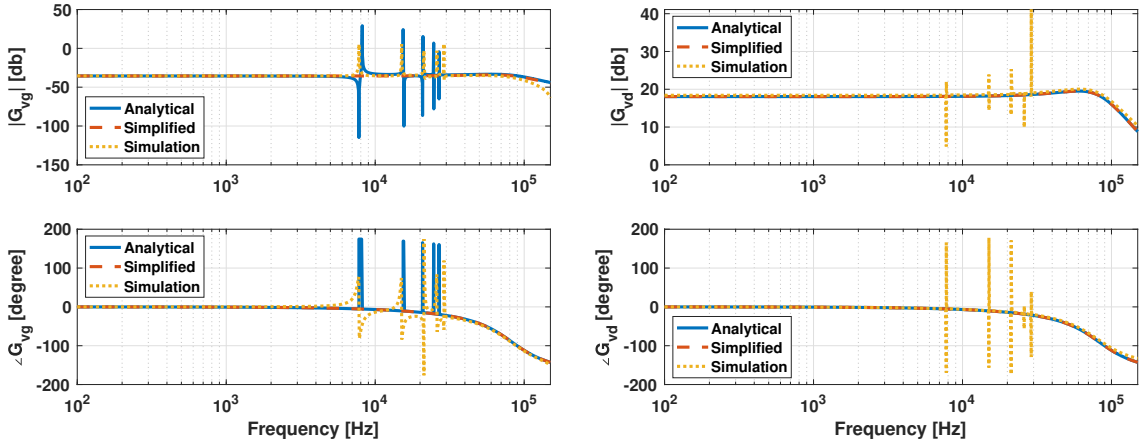
(a) Line to output transfer functions of 2LSCBC **(b)** Control to output transfer functions of 2LSCBC

Figure 5.8. Small signal transfer functions of 2LSCBC



(a) Line to output transfer functions of 7LDIHC **(b)** Control to output transfer functions of 7LDIHC

Figure 5.9. Small signal transfer functions of 7LDIHC



(a) Line to output transfer functions of 6LSCBC **(b)** Control to output transfer functions of 6lSCBC

Figure 5.10. Small signal transfer functions of 6LSCBC

The simplified transfer functions become exactly like Multi-Phase Buck converters [65]. The analytical transfer functions are also compared with the simplified expressions of multi-phase Buck converters ignoring all the pole-zero doublets in Figs. 5.8, 5.9 and 5.10, and it can be seen that they are good matches. The simplified expressions are also listed in Table 5.1. For any N-level MIH converter with m inductors, the transfer functions can be written as,

$$G_{vg} = \frac{\frac{D}{N}}{s^2 \frac{L}{m} C_{out} + s \frac{\frac{L}{m}}{R} + 1} \tag{5.2}$$

$$G_{vd} = \frac{\frac{V_{in}}{N}}{s^2 \frac{L}{m} C_{out} + s \frac{\frac{L}{m}}{R} + 1} \tag{5.3}$$

Eqns. 5.2 and 5.3 have similar lines and control to the output transfer functions of multi-phase Buck converters. If the pole-zero doublets are ignored, the control loops' design process should be similar to a Buck converter. These equations work for all the member converters of MIH converters except the MPDIH converter. Converters like MPDIH converters with multiple charging intervals of the inductors within the fundamental switching period need additional calculations for the current averaging.

5.4 Chapter Summary

This chapter has enclosed the step-by-step synthesis of the Multi Inductor Hybrid (MIH) converter family. The synthesis is followed by circuit manipulation for the complete elimination of hard-charging and, at the same time, supply of very high current at the output[1]. A general procedure for small signal modeling for these converters has also been included. The analysis

[1]For the converters where multiple capacitor branches are soft-charged with the same inductors, a general capacitor sizing strategy is proposed and listed in Appendix A.

For member converters that carry uneven inductor currents, a general current balancing strategy is proposed and listed in Appendix B.

The output resistances for notable member converters are calculated and listed in Appendix C.

is based on averaged circuit modeling, revealing that the frequency responses of most of the members of the MIH converter family resemble the multi-phase Buck converter.

Chapter 5, contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Chapter 6

Gate Driver Circuits With Discrete Components For GaN-based Multi-Level Multi-Inductor Hybrid Converter

6.1 Introduction

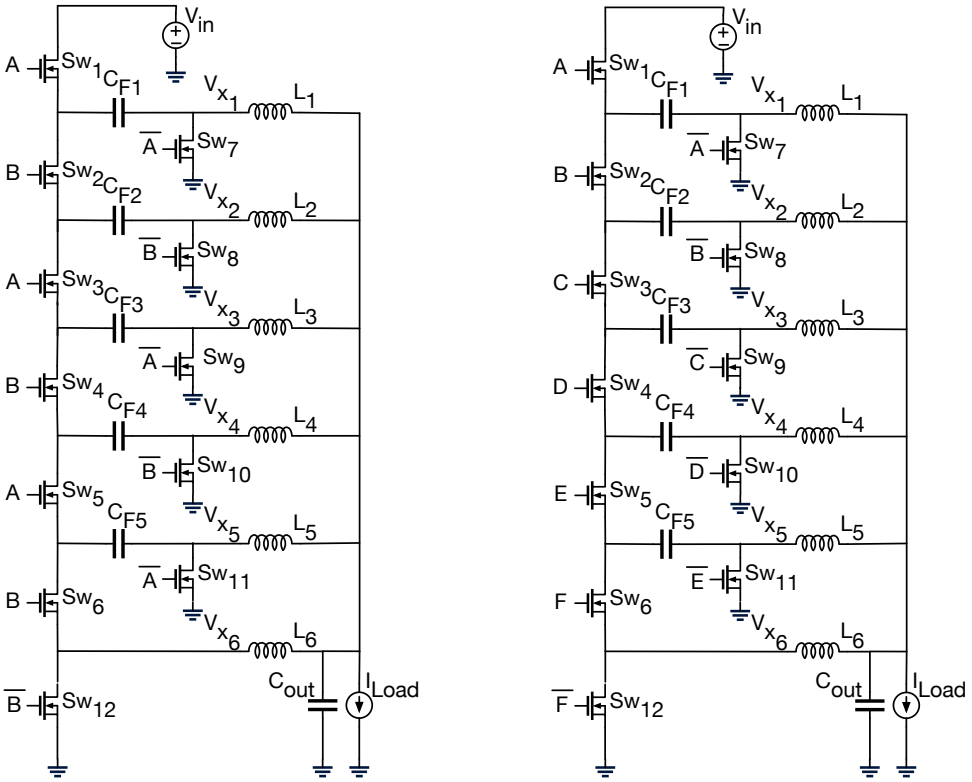
Multi-level hybrid DC-DC converters have significantly contributed to bolstering the recent rapid expansion of power electronics impact. Their successful integration in power supply for high-performance computing, automotive applications, space devices, domestic appliances, etc., has paved the path for a long-term strong establishment in the field. Remarkably, they emerge as the most appealing candidate for non-isolated Point-of-Load (PoL) converters in data centers and telecommunications systems. Recently, many different multi-level hybrid converters have been demonstrated for this application, where moderate to extreme step-up or step-down conversions are necessary, for example, 48V-to-12V [26, 28, 70, 71], and 48V-to-1.8V [16, 17, 30, 34, 41, 51, 72–75], etc. These converters have been demonstrated with resonant operations for highly-efficient fixed conversion ratios [26, 28, 30, 70, 72] or regulated output operations with pulse-width modulation (PWM) duty cycle control [17, 34, 41, 51, 71, 73–75]. With superior performance over conventional Buck converters, these hybrid converters promise significant improvement of the overall system efficiency and power density.

Despite their apparent advantages in power conversion, their market penetration is still

hindered by concerns over many design challenges, especially gate drivers for a relatively large number of stacked power switches. The designs of these hybrid DC-DC converters share a common characteristic: they utilize more switches and passive components to reduce voltage stress on them individually. The lower voltage stress enables the usage of devices with lower voltage ratings and higher density for higher system efficiency and smaller overall space. However, a large number of power switches means a challenge in the increased complexity of gate drivers. To make it worse, many power switches in these multi-level hybrid converters are operated at different voltage domains and shifted levels.

Figure 6.1 depicts a Multi inductor hybrid (MIH) converter [24, 54] as an example of multilevel hybrid converters, utilizing 12 switches, $Sw_{1\text{-}12}$. This converter can be operated in multiple ways with different operating numbers of inductor energizing phases. Fig. 6.1a and Fig. 6.1b show the configurations for 2 phases and 6 phases, respectively. In this converter, switches $Sw_{7\text{-}12}$ are operated at the ground level, i.e., their Source terminals are connected to the ground, while the other 6 switches, $Sw_{1\text{-}6}$ are stacked on top switch Sw_7. Although there are various types of multilevel converters, such as duty cycle controlled flying capacitor multi-level (FCML) hybrid converters [34, 76, 77], and multi-phase multi-inductor hybrid (MIH) converters [16,17,41,51,52,54,75], and a broad variety of resonant or hybrid switched converters [26,28,30,70,78,79], the stacked switch structure similar to $Sw_{1\text{-}7}$ in Fig. 6.1 is common in these converter families. The ground switches $Sw_{7\text{-}12}$ are relatively straightforward to drive, but it is challenging to drive the six stacked switches $Sw_{1\text{-}6}$ while satisfying reliability and performance across all operating points. The most fundamental stacked switch configuration is a half-bridge. Since gate driver integrated circuits (gate driver ICs) are often intended for only one single switch or two switches in a half-bridge, no single gate driver IC product can drive many stacked switches in multilevel converters.

This paper presents an optimal use of half-bridge drivers that takes advantage of built-in signal isolators in Section 6.2. In Section 6.3, a review of traditional and discussion of new schemes to generate power rails for the multi-level converter are provided. Section 6.4 presents



(a) 2-phase **(b)** 6-phase in ADBECF sequence

Figure 6.1. Multilevel hybrid converter example: 6-level MIH converter

experimental results and verifications of the circuits presented in Section 6.2 and 6.3. The paper is finally summarized and concluded in Section 6.5.

6.2 Optimal Use of Half-bridge Drivers

There are several techniques known for powering flying drivers, whose voltage domains are switched in regular operations of converters, some of which will be covered in Section 6.3. However, techniques to level-shift control signals from the ground level to appropriate flying voltage domains using discrete components can still benefit from further improvements for a smaller discrete component count and space. Commercial signal isolators rely on inductive or capacitive couplings to convey control signals to different voltage levels [80, 81]. Because of the relatively large passives required for isolated coupling and the nature of being discrete

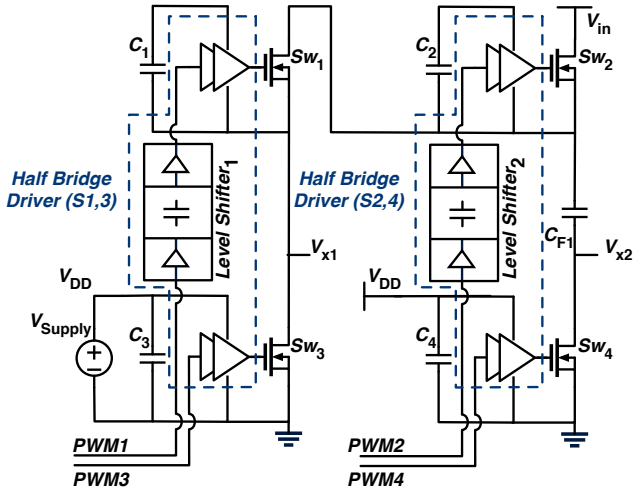
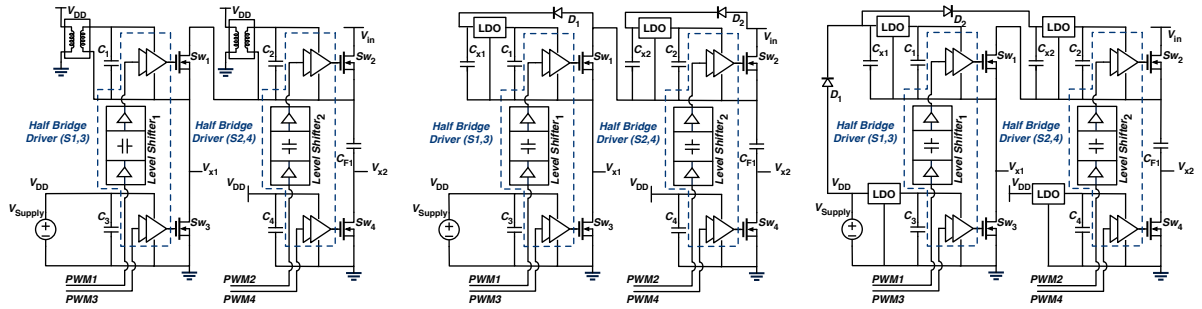


Figure 6.2. Optimal use of half bridge drivers with integrated signal isolators.

components, signal isolator ICs are often area-consuming and can be even larger than the switches that they are driving. This is a common problem in many power converters with multiple synchronous power switches, such as multi-level converters. In addition, these isolators can also add significant delays to the critical signal path, leading to more complex timing control. It is, therefore, desirable to minimize the number of signal isolator ICs required in converter design.

It is widely known that typical commercial half-bridge driver ICs have a built-in capacitive signal isolator. This half-bridge driver is usually used to drive a half-bridge switch pair where the top driver drives the switch that is stacked immediately on top of the one driven by the bottom driver [26, 77, 82, 83]. However, it is much less recognized that the built-in signal isolator in a half-bridge driver is capable of a large voltage difference and can be used in place of a signal isolator. Utilizing this built-in capability can optimize half-bridge gate driver functionality and eliminate the need for all discrete signal isolators in multilevel hybrid converters.

Figure 6.2 depicts the switched capacitor (SC) part of a Series Capacitor Buck Converter (SCBC) [52] as an example where half-bridge driver ICs and their built-in signal isolators are proposed to be used in a new configuration to remove the need for discrete signal isolators. The power converter architecture has 4 switches in Fig. 6.3a, two of them, Sw_1 and Sw_2 are



(a) Isolated modules **(b)** Regulated supplies from switch blocking voltages **(c)** Regulated supplies from cascaded bootstrap

Figure 6.3. Optimal use of half-bridge drivers in multilevel hybrid converter with different powering schemes

stacked on a ground-level switch Sw_3. Switch Sw_4 is at the ground level and operated in a complementary phase to Sw_2. Flying capacitor C_{F1} connects switch Sw_4 to Sw_1, Sw_2 and the rest of the circuit.

In this power converter, directly stacked switches Sw_1 and Sw_3 can be driven by a half-bridge driver IC. Sw Sw_2 and Sw_4 do not share a common switching node as in usual half-bridge switch pairs, so they may not immediately appear to be controllable by a single half-bridge driver IC. However, the power-transfer capacitor C_{F1} connecting them acts as a DC voltage source in operation transient, ensuring that their operation is logically complementary in the same manner of a half-bridge switch pair with a DC voltage separation equivalent to the voltage across C_{F1}, $V_{C_{F1}}$. Recognizing that the signal isolator built in a half-bridge driver IC is capable of this voltage separation, only one driver IC is utilized to drive Sw_2 and Sw_4 Particularly, the built-in signal isolator can bring the gate control signal up for Sw_2 while the high-side driver for Sw_2 can operate at a $V_{C_{F1}}$ from the ground. This proposed method results in more optimal utilization of gate driver IC and removes the need for an additional signal isolator that would have been needed for Sw_2 in the traditional solution [82].

It is worth noting that the example circuits in Fig. 6.2 represents the lowest 2 levels of the SC stage in an N-level SCBC, where N can be a number greater than 2 [17, 51, 54]. This optimal use of half-bridge drivers can be extended to drive all other high-side switches in the

stack in multi-level hybrid converters [16, 17, 41, 54, 84].

6.3 Power Rail Generation

Together with the new optimal half-bridge driver scheme presented in Section 6.2, it is essential to devise appropriate methods to power high-side gate drivers operating at different voltage domains. There are many methods to achieve this goal, as also presented in the comprehensive review reported in [82]. However, the methods have their limitations, which come in the way of practical implementation for a compact and reliable solution. This paper investigates three suitable powering schemes for the multi-inductor hybrid converter and provides a more detailed comparison and design insights to help converter designers choose a suitable solution.

Three powering schemes of particular interest are isolated power modules (Fig. 6.3a), regulated supplies from switch blocking voltage (Fig. 6.3b), and regulated supplies from cascaded bootstrap (Fig. 6.3c). In this chapter, they are implemented and demonstrated with the optimal half-bridge driver scheme described above. This section will provide descriptions of their operations, trade-offs, and design insights, while experimental demonstrations and measured performances are provided in Section 6.4.

6.3.1 Use of Isolated Power Modules

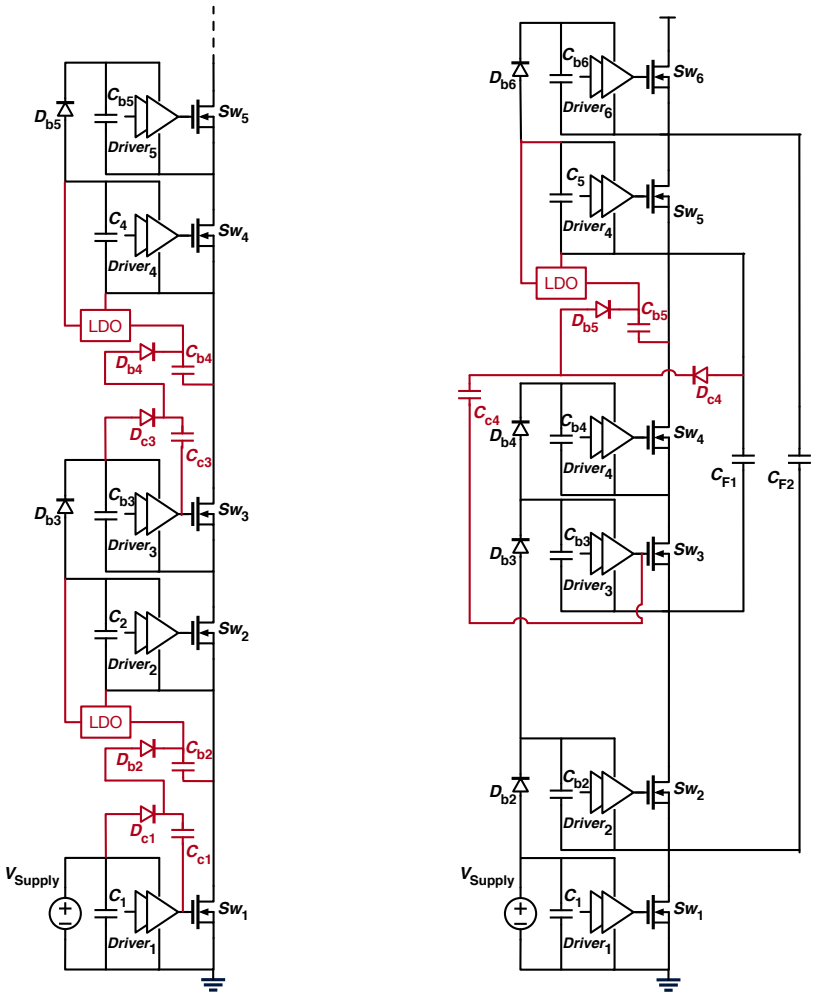
As a straightforward method, isolated power modules can be used for driving high-side switches, Sw_1 and Sw_2, shown in Fig. 6.3a. When the SCBC is extended to a larger number of levels, i.e. more SC stages, this powering method can be reliable as will be shown in Section 6.4. However, isolated power modules often have relatively large parasitic capacitance between the primary and secondary ground which can significantly limit the switching frequency and transient performance of the converters and increase switching loss. Therefore, an exhaustive search for isolated DC-DC converter modules is recommended to find the lowest possible isolation capacitance to improve converter performance [85]. A key drawback of isolated power modules is their sizes which are often significantly larger than other components of the circuit, including

both power switches and gate driver ICs [85, 86]. In addition, they are relatively inefficient, with efficiency limited to below 60%, and capable of a relatively small load range [85]. The inefficiency increases gate driving losses that could be significant at light loads, which worsen when many modules are used for multiple high-side switches. It is desirable to find a more compact and efficient method to power high-side switch drivers.

6.3.2 Regulated Supplies from Switch Blocking Voltages

In multi-level converters, there are many intermediate voltage nodes switching at levels that can be utilized to generate flying voltage domains to drive high-side switches. From this recognition, another method to generate flying power rails from the converter switching nodes is explored to replace the isolated power modules in Fig. 6.3a. In the circuit shown in Fig. 6.3b, the blocking voltages of high-side switches Sw_1 and Sw_2 when they are off can be used to generate its V_{GS} driving voltage. For example, when switch Sw_1 is off, the voltage between its drain and source terminals can be used to charge capacitor C_{x1} via diode D_1. In multilevel converters, this capacitor voltage is often larger and can then be regulated down to the required ~5-V level to drive Sw_1 using a linear low-dropout regulator (LDO). A similar operation can be observed for Sw_2 and its related circuit. Although this method consists of multiple discrete components, including an LDO, a diode, and two capacitors, because they are compact, the implementation space for this regulated flying supply domain is still significantly smaller compared to a standard isolated module. Therefore, this flying rail powering method helps reduce the overall area for gate driving circuits.

A key limitation of this powering method is the intrinsic nature of the LDO: its efficiency is low when there is a big difference between the blocking voltage (~$V_{C_{x1}}$) and the required V_{GS} level (~5 V). Unfavorably for this method, the blocking voltage depends on the converter topology, input voltage, and output current. When the input voltage increases, the blocking voltage increases linearly; hence, the LDO efficiency decreases, and gate driver power loss increases. Although having less impact, higher output currents also cause efficiency degradation



(a) Double charge-pump.

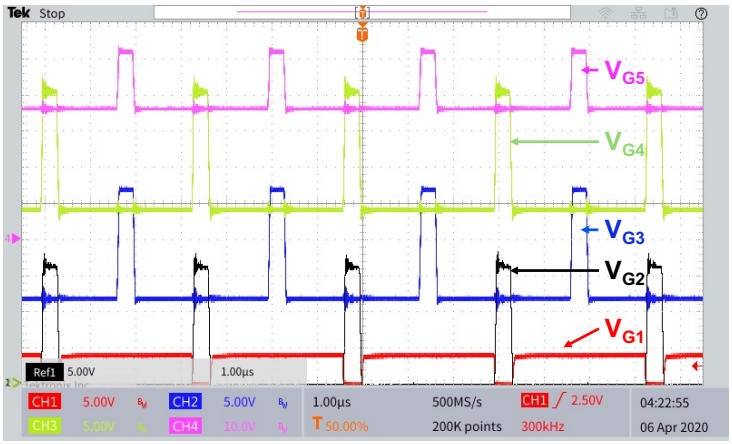
(b) Gate driven charge-pump.

Figure 6.4. Example of charge-pumps

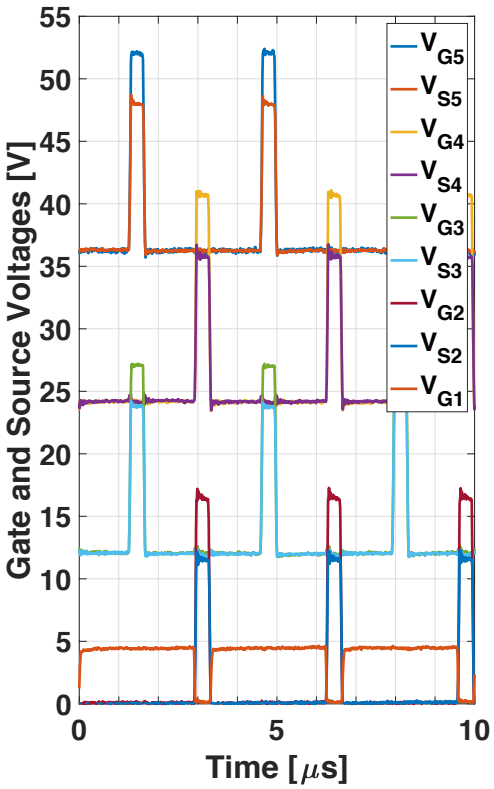
in the LDOs and gate drivers as a consequence of larger voltage ripples on the main flying capacitors, leading to larger differences between the blocking voltages of high-side switches (~V_{Cx1}) and the LDOs' output (~5 V).

6.3.3 Regulated Supplies from Cascaded Bootstrap Circuits

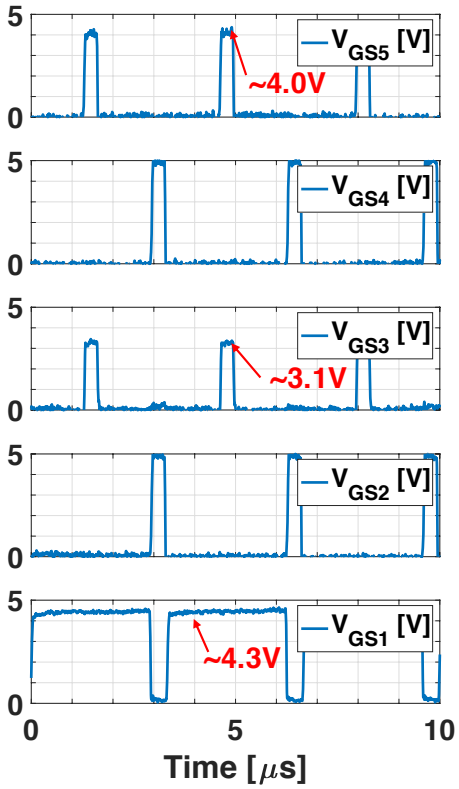
To reduce the voltage difference between the input and output of gate driver LDOs and avoid the dependence on the converter's input voltage and output current, another powering scheme for high-side gate drivers is desirable. Figure 6.3c shows a circuit for a cascaded bootstrap



(a) Measured gate signals of switches $Sw_{1\text{-}5}$.



(b) Measured gate and source voltages of switches $Sw_{1\text{-}5}$.



(c) Measured gate to source voltages of switches $Sw_{1\text{-}5}$.

Figure 6.5. Experimental waveforms of gate to source voltages of stacked switches using modified charge pump method

circuit with additional LDOs added to all power domains of gate drivers. Although this cascaded bootstrap structure still has a diode voltage loss at every stack level, the input supply voltage V_{Supply} can be increased to overcome the series diode stack to support the top driver while the

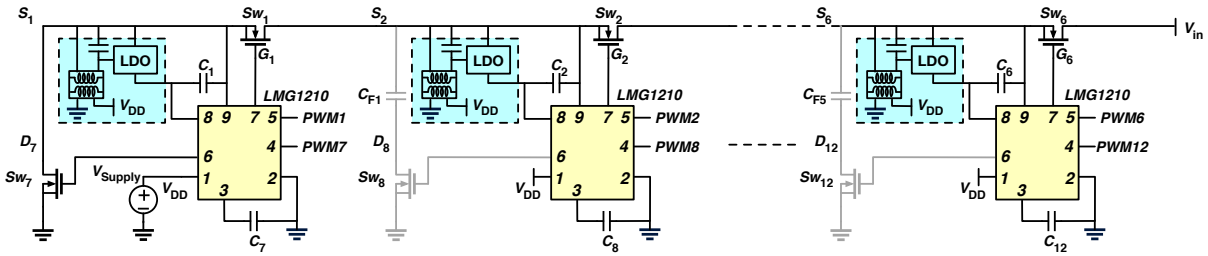
LDOs regulate the same safe driving voltage for all the gate drivers. Particularly, in the circuit shown in Fig. 6.3c, V_{Supply} is provided at ~5.6V, accounting for 0.5V diode drop in 2 cascaded stages to provide ~5.1 V at C_{x2}. From C_{x2}, the LDO can have a 100mV drop-out voltage margin to regulate a 5V supply for the flying voltage domain driving Sw_2.

In this method, cascading bootstrap circuits for a large number of stack switches will result in a large accumulation of multiple diode drops, requiring a large V_{Supply} for operation. A large V_{Supply}, in turn, put the LDOs at the bottom and lower voltage domains of the stack at low efficiencies because of large input/output voltage differences. Therefore, there have been new engineering efforts in both industry and academia to replace the bootstrap diodes with synchronous active devices in a more integrated approach [71, 87]. This can mitigate the requirement for high V_{Supply} and reduce the number of LDOs to improve gate driver efficiency. This paper focuses on commercially available parts for our developments, but it is still worth mentioning that ultimately, one would like to have a similar more integrated solution to achieve a more optimal power driving scheme which will need further investigations.

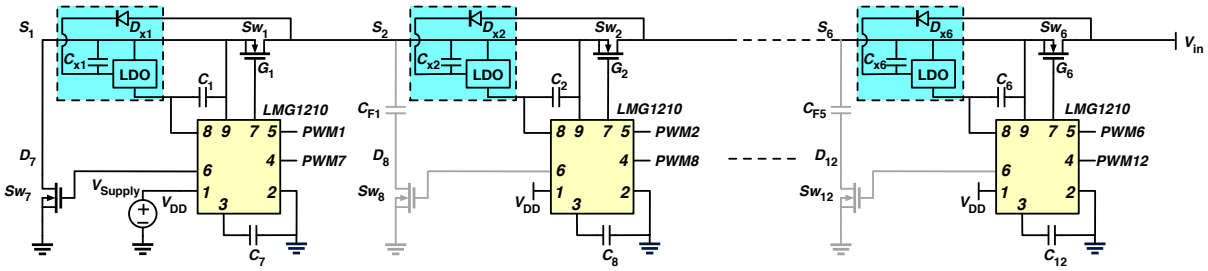
6.3.4 Discussion on Recently Popular Charge-Pump Methods

A double charge-pump bootstrap circuit together with LDOs was proposed as an alternative [88] illustrated in Fig. 6.4a. This method uses a lower-level driver to charge-pump higher bootstrap voltage instead of using a separate switch as in [89, 90]. The key idea in double charge-pump circuits is to utilize two cascaded charge-pump to double the bootstrap voltage to overcome diode voltage drops, then use an LDO to regulate the driver supply voltage to the desired $\sim$5V level. This method has been popular recently, and there is also a variation of this circuit named gate-driven charge pump claimed preferred option for hybrid converters [82, 88]. This method is also shown in Fig. 6.4b.

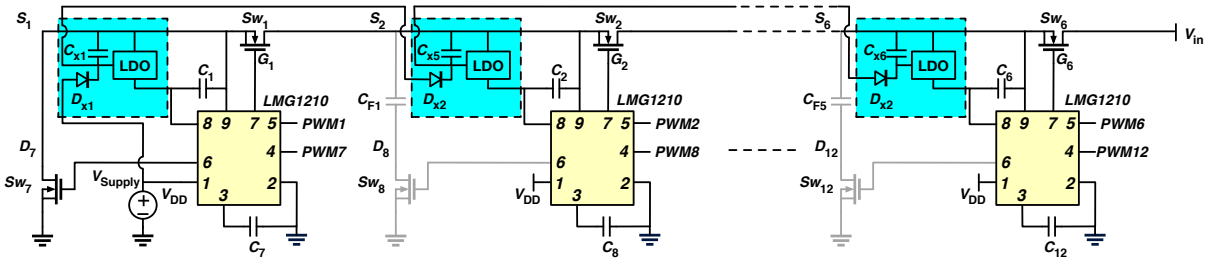
While the operations of the charge pump circuits can use the same V_{Supply} level, they suffer from a serious practical issue that comes from the loading effect on drivers at lower voltage domains. In today's gate driver ICs commercially available for GaN FETs, the drivers



(a) Stacked switches of 6-Level MIH Converter using optimized half-bridge drivers and isolated power supply modules.



(b) Stacked switches of 6-Level MIH Converter using optimized half-bridge drivers and regulated supplies from switch blocking voltages.



(c) Stacked switches of 6-Level MIH Converter using optimized half-bridge drivers and regulated supplies from the cascaded bootstrap method.

Figure 6.6. Schematic diagrams of the implemented converter prototype using different driver, signal isolator, and powering schemes (Stacked switches and their driver circuits are shown. Inductors, output capacitor, and load are not shown.)

are generally designed to drive one switch. However, in the operations of double charge pump circuits, the bootstrapped driver ($Driver_j$) of each voltage domain needs to also drive the charge to bootstrap capacitors for higher domains. Particularly, during the charging of C_{b2} and C_{b4} in the double charge-pump circuit of Fig. 6.4a, $Driver_1$ and $Driver_3$ carry turn-on current for switch Sw_1 and switch Sw_3 and the current required to charge capacitor C_{b2} and C_{b4} respectively. Furthermore, when more switches and stages are stacked on top of switch Sw_4, the heavy

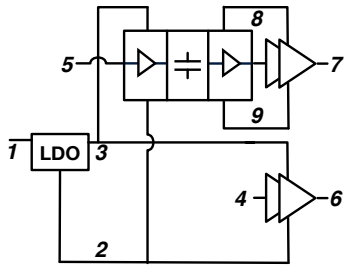


Figure 6.7. Block diagram of LMG1210 [91], a half-bridge driver IC with integrated signal isolator and linear regulator (LDO), used in Fig. 6.6

accumulated loading comes to $Driver_3$ and ultimately $Driver_1$. In practice, as the gate driver is not generally designed to carry this level of large loads, its ON resistance comes into the picture, lowering the actual V_{GS1} of Sw_1 and V_{GS3} of Sw_3. Because of these non-idealities, actual values of V_{GS1} and V_{GS3} can become as low as ~4.3 V and ~3.1 V. This ~3.1V is far below the required level to properly turn on switch Sw_3, leading to low converter efficiency and failure of Sw_3. Note that this effect is separate from the effect of the gate voltage drop from the bootstrap diode. In Fig. 6.4a, bootstrap diode has effect on V_{GS3} and V_{GS5}. The driver's loading effect affects V_{GS1} and V_{GS3}. As the non-ideality of V_{GS3} comes from both sources, the worst case can be seen in the magnitudes of it, and it has higher chances of failure. Depending on the nature of a multilevel converter, a failure of one switch can expose other switches to voltage levels much higher than their ratings, causing cascaded failures and irreversible damage to the whole converter. An experimental demonstration of this phenomenon has been provided in Fig. 6.5. The circuit in Fig. 6.4 has been implemented, all the gate and source voltages have been measured, and the gate-to-source voltages have been calculated from the measurements.

This practical problem is common in many double charge-pump circuits. The gate-driven charge pump method claimed as preferred in [82] and illustrated in Fig. 6.4b also suffers from the same problem. $Driver_3$ in Fig. 6.4b supply the currents to turn on switch SW_3 as well as Sw_5 and Sw_6 by charging C_{b5}. The key solution to this problem is to utilize the strong power switches of the converter, rather than those weaker transistors of the gate drivers, to drive the charge-pump capacitors, as shown in the two powering schemes discussed in subsection 6.3.2

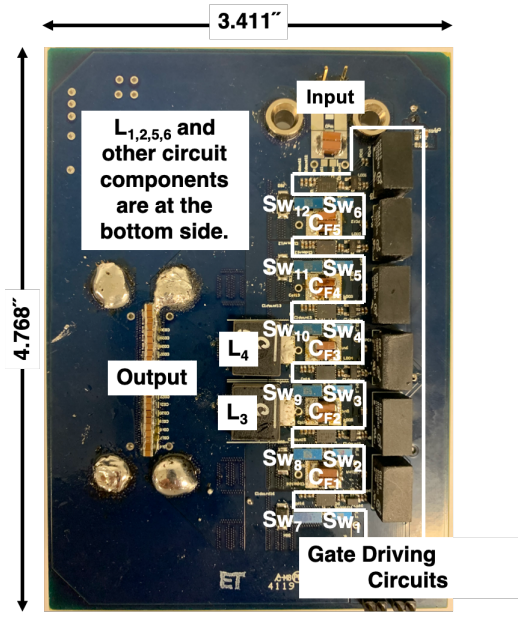


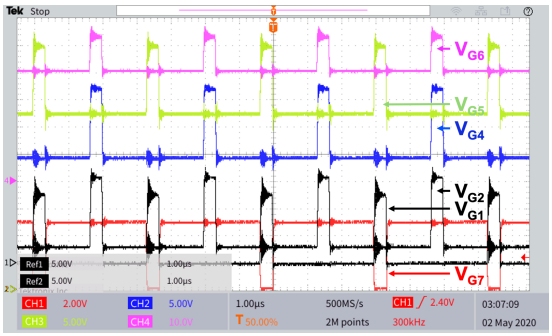
Figure 6.8. Multi-level multi-inductor hybrid converter prototype, reconfigurable for different schemes in gate driver, signal isolator, and powering flying voltage domains.

(Fig. 6.3b) and Section 6.3.3 (Fig. 6.3c) above. The strength of the main power switches is capable of satisfying the current stress needed by multiple gate driver bootstrap circuits.

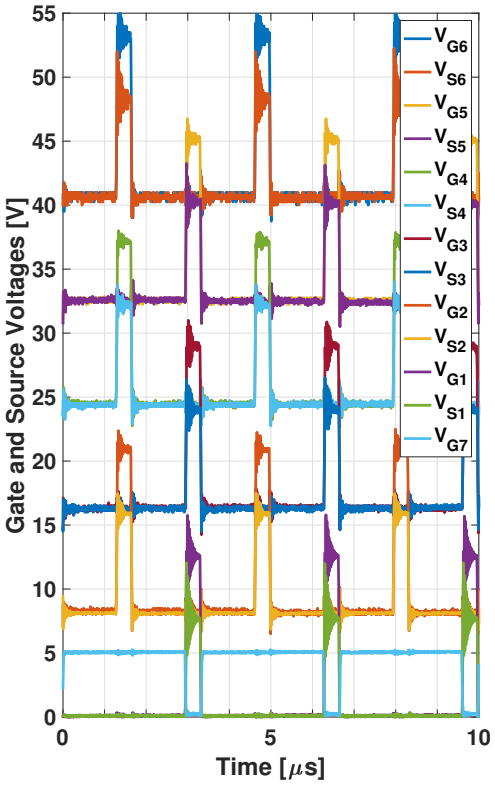
6.4 Hardware Implementations and Experimental Results

To verify their steady-state and transient operations of the proposed level shifting method in Section 6.2, a multilevel multi-inductor hybrid (MIH) converter has been implemented whose schematic is shown in Fig. 6.1. The hardware prototype, shown in Fig. 6.8, has been designed with careful layout considerations to have short gate driving loops decoupled from the power loops.

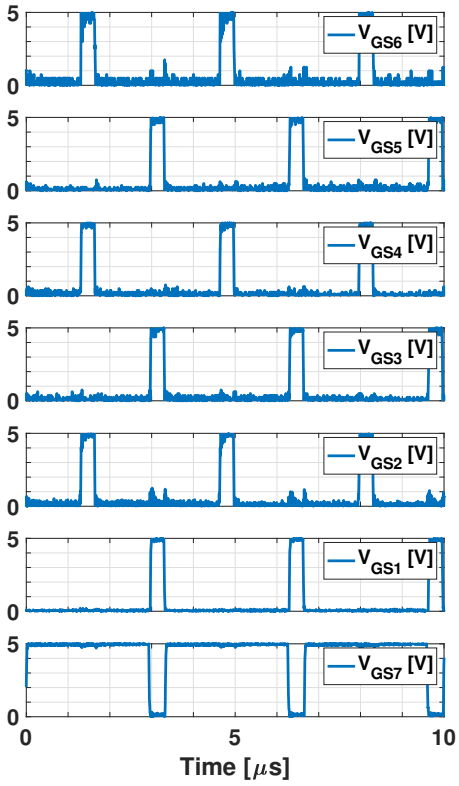
The prototype in Fig. 6.8 does not use any separate level shifters for the floating switches of multiple levels. Instead, it has been implemented with the isolator-less, optimized half-bridge driver method using the internal integrated level shifter of a standard commercial half-bridge gate driver IC LMG1210. A detailed diagram of LMG1210 is shown in Fig. 6.7. To compare the trade-offs of the powering methods, the prototype board has been reconfigured for different



(a) Measured gate signals of switches $Sw_{1\text{-}2,4\text{-}7}$



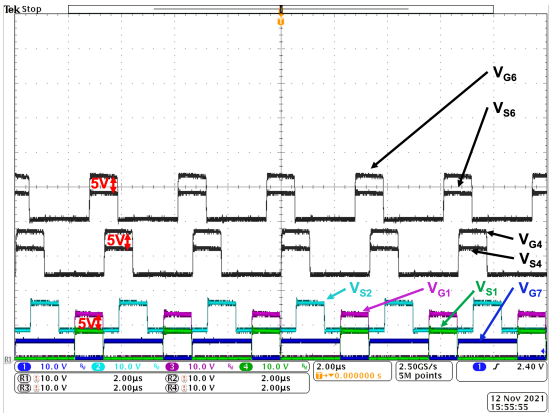
(b) Measured gate and source signals of switches $Sw_{1\text{-}7}$.



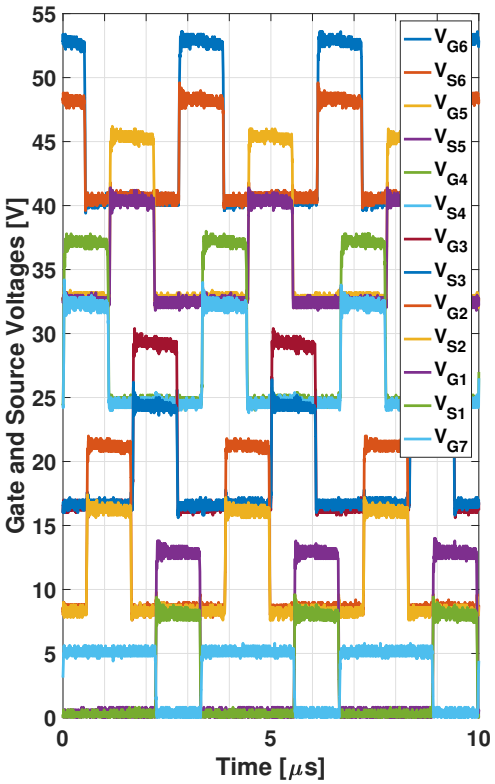
(c) Measured gate to source voltages of switches $Sw_{1\text{-}7}$.

Figure 6.9. Experimental waveforms of the MIH converter using optimized half-bridge drivers and regulated supplies from the cascaded bootstrap method (Operating condition: Number of phases=2, V_{in}=48V, I_{Load}=10A and Duty cycle=10%)

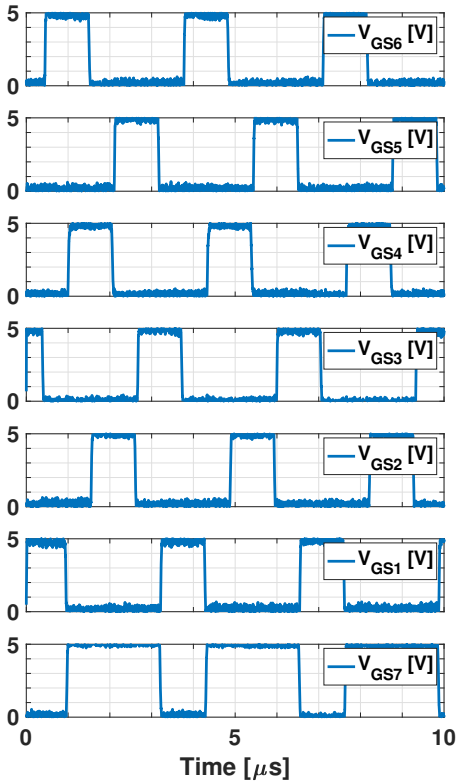
powering schemes as drawn in detail in Fig. 6.6. Fig. 6.6 illustrates the main power components including all the switches and flying capacitor and the detailed connections of the gate driving circuits using a 9-pin block for the LMG1210 gate driver IC. Particularly, Fig. 6.6a, 6.6b and



(a) Measured gate signals of switches $Sw_{1,4,6,7}$ and source signals of switches $Sw_{1,3,4,6}$



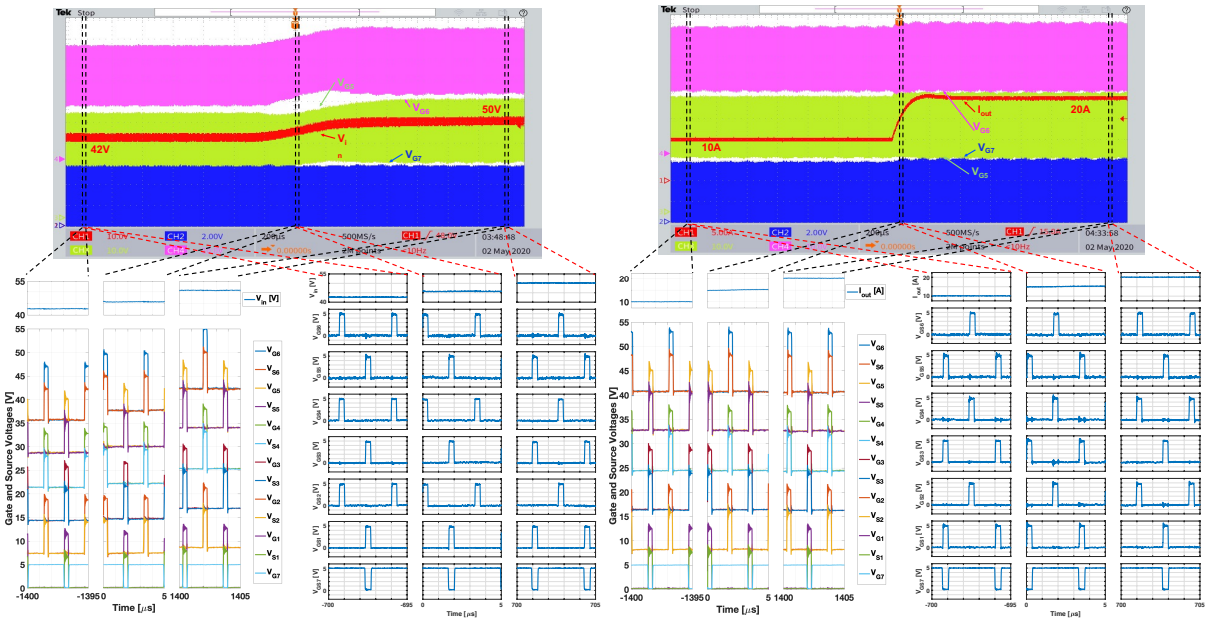
(b) Measured gate and source signals of switches $Sw_{1\text{-}7}$.



(c) Measured gate to source voltages of switches $Sw_{1\text{-}7}$.

Figure 6.10. Experimental waveforms of the MIH converter using optimized half-bridge drivers and regulated supplies from the cascaded bootstrap method (Operating condition: Number of phases=6, V_{in}=48V, I_{Load}=10A and Duty cycle=32%)

6.6c show three different high-side driver powering schemes: isolated power supply modules, regulated supplies from switch blocking voltages, and regulated supplies from the cascaded



(a) 42V to 50V line transient waveforms. **(b)** 10A to 20A load transient performance.

Figure 6.11. Measured transient gate signals of the MIH converter prototype using the optimized half-bridge driver and regulated supplies from the cascaded bootstrap method.

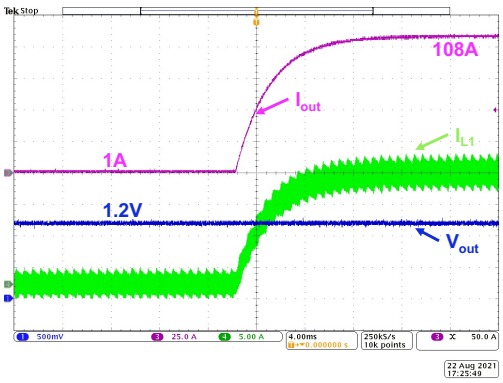
bootstrap method. With experimental demonstrations, the validity of the level-shifting technique has been shown and different powering schemes have been compared for trade-offs.

The hybrid converter in Fig. 6.1 can be operated with a minimum of 2 to a maximum of 6 energizing phases. Operating the converter at multiple phases, the ripple currents of the six inductors can be minimized to have low output voltage ripple. The converter has twelve switches in total, six of which, $Sw_{7\text{-}12}$, are at the ground level and the other six, $Sw_{1\text{-}6}$, are stacked on Sw_7. Six half-bridge drivers LMG1210 ICs are employed to drive the 12 switches in this implementation. While Sw_1-Sw_7 pair is directly connected and operated as a conventional half-bridge, the remaining 5 switch pairs, Sw_2-Sw_6 to Sw_8-Sw_{12}, are connected via 5 flying capacitors, C_{F1} to C_{F5}, respectively. All the switch pairs which receive complimentary driving signals are driven with separate gate driver ICs. Hence, six half-bridge driver ICs are used for six switch pairs.

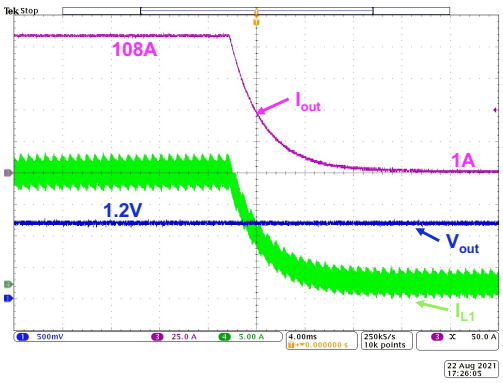
In the circuit in Fig. 6.6a, an LDO is used after each isolated power module to regulate

the gate driver supply voltage at ~5.0-5.5 V, recommended for sensitive GaN switches [85, 92]. These LDOs can be avoided if the isolated power modules can maintain a tight voltage close to 5 V. As the implementation also targeted reconfigurability for other powering scheme validation, these LDOs provide benefits of simple modification from one powering scheme to another described in Fig. 6.6. Note that the LMG1210 driver conveniently comes with an integrated LDO for its bottom driver. Therefore, no additional discrete LDO is needed for the ground switches Sw_7-Sw_{12}, while operating with the cascaded bootstrap method shown in Fig. 6.6c.

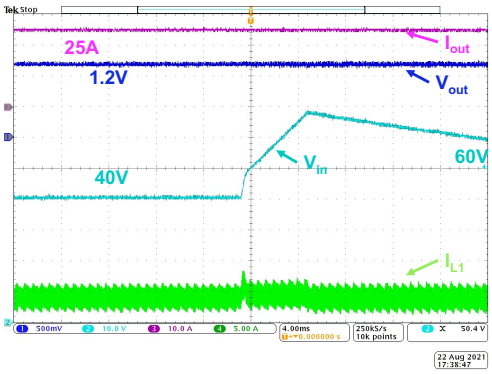
The powering method where switch blocking voltages are used to derive the power rails (Fig. 6.6b) does not work when the input voltage is low such that switch blocking voltages are reduced to less than 5 V, i.e., not enough voltage to provide to the LDOs. This scenario



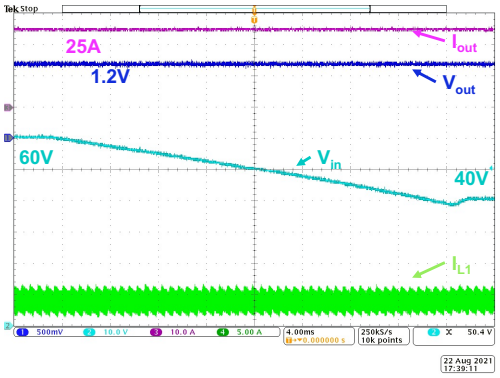
(a) Load transient of 1A to 108A of 6-level MIH converter for 48V to 1.2V operation



(b) Load transient of 108A to 1A of 6-level MIH converter for 48V to 1.2V operation



(c) Line transient of 40V to 60V of 6-level MIH converter for 1.2V/25A operation



(d) Line transient of 60V to 40V of 6-level MIH converter for 1.2V/25A operation

Figure 6.12. Reliability testing of the demonstrated gate driving circuits at very high transients

can be seen at startup when the input voltage starts increasing from zero. In this particular implementation, this powering scheme starts working for an input voltage from ~18 V. In normal operations of the converter with V_{in} at 40-60 V, switch blocking voltages are at least ~6.5V for LDOs for $Sw_{1,6}$ and ~13V for LDOs for $Sw_{2\text{-}5}$. These voltages are high enough to warrant the intended operation of the circuits.

In Fig. 6.6c, the implemented cascaded bootstrap circuit involves a chain of seven drivers. Among these seven drivers, the top six are the high-side drivers of six different gate driver ICs. This is a new demonstration of the cascaded bootstrap method where the cascading between the drivers involves both being the high-side drivers. Previous implementations were only done within the half-bridge driver IC or from one sigh side driver of a lower level half-bridge driver IC to the low side of another higher level half-bridge driver IC.

The 2P6IHC prototype with all three driver powering schemes was also tested for durability and reliability in both steady-state and transient conditions. These methods did not show any significant differences in their performances under the test conditions. As the cascaded bootstrap method is the most attractive one among them in terms of efficiency and area, test results associated with this method are particularly shown in this chapter. The steady-state operation is measured in Fig. 6.9 showing the intended operation to provide the right 5V V_{GS} for all stacked GaN switches. This measurement has been taken at 48 V input voltage with 10% duty cycle operation for all the phases. The gate and source signals are measured separately using separate probes with respect to the ground. Fig. 6.9a shows measurements of some of the gate signals, while the converter was in operation. Separately measured data were collected and plotted together in Fig. 6.9b to clearly show the distinctive levels of the different gate and source signals. Fig. 6.9c illustrates the gate-to-source voltages of each of the stacked switches separately. This validates the proposed level-shifting method for the application of a multi-level converter along with the powering scheme.

To show the effectiveness of this method over a broader range of duty cycle and multi-phase operations, this experiment has been repeated in Fig. 6.10 with the converter operating

in 6 phases with 32% duty cycle. Fig. 6.10a includes the measurements of multiple gates and source voltages of the converter, Fig. 6.10b includes the plot of all the gate and source voltages of the stacked switches and Fig. 6.10c includes the gate-to-source voltages of each individual stacked switch.

It is also desirable to verify the performance of the proposed level-shifting technique during operation transients. 8V line transients and 10A load transients with cascaded bootstrap method are also shown in 6.11a, and 6.11b. In these figures, all the gate and source voltages are measured. Gate-to-source voltages are calculated from these measurements and plotted before, during, and after the transients. Steady 5V for all the V_{GS} suggests this method is reliable during all the transient states. The converter has been also exposed to very high line voltage and load current change, and the converter was reliable during the measurements. These measurements are included in Fig. 6.12. Figs. 6.12a-6.12b show the load change of ~100A and Fig. 6.12c-6.12d show the line voltage change of ~20V. Fixed output voltages with large transients prove the effectiveness of the demonstrated method with dynamic duty cycle changes during the transients. These measurements have been conveyed with the converter operating in 6 phases.

Table 6.1 includes a comparison of the gate driving and powering methods investigated in this paper on a number of characteristics and trade-offs. Optimal utilization of the signal isolator built-in to commercial half-bridge drivers creates new opportunities to save significant areas of discrete signal isolators. This method combined with either regulated power supplies from switch-blocking voltages or regulated power supplies with cascaded bootstrap can yield an overall significantly smaller area while achieving both high driving efficiency and reliability. In these better powering schemes, the cascaded bootstrap and LDO regulation for every stage produce a high driving efficiency of ~70% because of the flexibility to set small voltage drops across the LDOs. The driving efficiency is calculated from the gate driving loss from the data sheet and the measured driving power in the experiment.

Table 6.1. List of components and comparison for different gate drivers and powering schemes

Gate driver	Half-bridge drive	Optimized half-bridge driver		
Powering scheme	Modified double charge-pump	Isolated supply modules	Regulated supplies from switch blocking voltages	Cascaded bootstrap + LDOs
Converter prototype	2-Phase 4-inductor Hybrid Converter [17]	2-Phase 6-Inductor Hybrid Converter [24]		
Number of levels	4	6	6	6
Total number of switches	8	12	12	12
Ground level switches	4 (2xEPC2023)	6 (2xEPC2023)	6(EPC2023)	6(EPC2023)
Stacked switches	4 (2xEPC2015c)	6 (2xEPC2015c)	6(EPC2015c)	6(EPC2015c)
Single gate drivers	4 (LM5114)	0	0	0
Half-bridge drivers	2 (LMG1205)	6 (LMG1210)	6 (LMG1210)	6 (LMG1210)
Isolated supply modules	0	6 (CRE1S0505S3C)	0	0
Signal isolators	2 2-channel (Si8423BB-D-IS)	0	0	0
Diodes	4 (CRS08)	0	6(CRS08)	6(CRS08)
LDOs	2 (TPS70950DBVR)	6 optional (TPS70950DBVR)	6 (TPS70950DBVR)	6 (TPS70950DBVR)
Driver supply voltage and current	5V/123mA	5V/247mA	5V/37mA + 48V/6mA	6.7V/53mA
Gate switching power*	0.332W	0.498W	0.249W	0.249W
Driver efficiency***	54%	40.32%	52.64%	70.1%
Implementation area†	265 mm^2	520.54 mm^2	124.8 mm^2	124.8 mm^2
Performance	poor	moderate	good	good
Favorable solution	no	Area dependent	yes	yes

*Calculated with gate charge provided in the switch data sheets.
** Measurements are taken at no load.
*** Efficiency $= \frac{\text{Gate Switching Power}}{\text{Drive supply voltage} \times \text{Drive supply current}}$
† Calculated without the area of the capacitors used in the gate driving circuits.

6.5 Chapter Summary

In summary, a number of methods to power and drive stacked switches in a GaN-based multi-level multi-inductor (MIH) hybrid converter have been discussed and experimentally demonstrated in this chapter. Their trade-offs and challenges have been discussed from different

aspects of practical implementations to help designers choose a suitable solution for particular design needs. In practice, gate driver circuits can cause faults and failures in converters using sensitive GaN FETs. Hence, it is desirable to choose a set of proper level-shifting techniques for PWM signals and powering schemes for reliable operations while maintaining an overall compact and efficient implementation. An isolator-less method has been devised for small-area implementation and demonstrated with different powering schemes for elevated domains. A 6-level 6-inductor hybrid converter prototype was used to demonstrate the gate driving and powering schemes, validate their operations, and discuss performance and design trade-offs. The experiments, circuits, and discussions in this paper are aimed to be a good source of reference for future engineering efforts in designing multi-level hybrid converters.

Chapter 6, in full, is a reprint of the material as it appears in "Gate Driver Circuits With Discrete Components for GaN-Based Multilevel Multi-Inductor Hybrid Converter," in IEEE Transactions on Industrial Electronics, vol. 70, no. 2, pp. 1105-1114, Feb. 2023 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Part III

General Analyses of Hybrid Switched-Capacitor Converters

Chapter 7

Demystifying Capacitor Voltages and Inductor Currents in Hybrid Converters

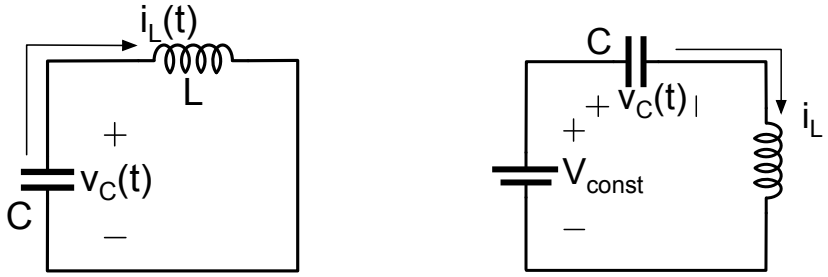
7.1 Introduction

The demand for more efficient and compact point-of-load (PoL) step-down power converters has increased significantly in virtually all power delivery networks to support last-millimeter high-output-current delivery for high-performance loads, particularly in data centers and telecommunication systems. In 48-V systems, these PoL converters can provide either the last conversion stage [64] in a two-stage structure [93] or a direct 48V-to-1V single conversion stage [16,17,39,40,49]. To satisfy system requirements, PoL converters often have the following common characteristics: 1) favor non-isolated hybrid architecture to achieve high efficiency and avoid bulky transformers, 2) support relatively large conversion ratios to reduce stress on the input current distribution [34], and 3) achieve high efficiency at high power density and high current density [17].

Recent developments of the multi-inductor hybrid (MIH) converter family have shown promising converter architectures that can achieve seamless pulse-width-modulated (PWM) operations of multi-phase Buck converters, low volt-seconds applied to filtering inductors, and large duty cycle while still supporting large or even extremely large conversion ratios [17]. Furthermore, the MIH converter family can be extended to have many different configurations to efficiently support various input/output requirements in different applications [16, 17, 49].

Configuration examples include different numbers of flying capacitors (and thus different number of voltage levels), output inductors, capacitors soft-charged by one inductor and different inductor charging phases. These converters add to the set of hybrid converters that have an input switched-capacitor network followed by output filtering inductors originating from multi-level converters [94] or flying-capacitor multi-level (FCML) converters [95]. A well-known challenge in designing hybrid converters is to achieve voltage balance for flying capacitors [34, 96, 97].

In this chapter, expanding on prior efforts we present a more general and complete method to analyze and accurately predict levels as well as waveforms of voltages and currents in hybrid converters. This method, developed in Section 7.2, combines circuit operation inspection, theoretical analysis, and relatively simple equations to reach intuitive results with minimal effort. Analytical results and verifications using simulation results at different operating conditions for a Dual Phase Multi-Inductor Hybrid (DPMIH) converter [17] (also called Series Capacitor Buck or SCB converter reported in [52–54]) of the MIH converter family, and for a 3-level Buck (3LB) converter representing FCML converters are presented in Section 7.3 and Section 7.4, respectively. The chapter is summarized and concluded in Section 7.5.



(a) Discharging **(b)** Charging

Figure 7.1. Circuit model of capacitor charging and discharging phases in hybrid converters

Table 7.1. Capacitor voltages

Phase	$v_C(0)$	$v_C(DT_S)$	$v_C(t)$	$V_{C,av}$
Discharging	$V_C + \frac{Q}{2C}$	$V_C - \frac{Q}{2C}$	$\left(V_C + \frac{Q}{2C}\right) cos\left(t/\sqrt{LC}\right) + \frac{(V_C - \frac{Q}{2C}) - (V_C + \frac{Q}{2C}) cos\left(DT_S/\sqrt{LC}\right)}{sin\left(DT_S/\sqrt{LC}\right)} sin\left(t/\sqrt{LC}\right)$	bV_C
Charging	$V_C - \frac{Q}{2C}$	$V_C + \frac{Q}{2C}$	$2V_C - \left(V_C + \frac{Q}{2C}\right) cos\left(t/\sqrt{LC}\right) - \frac{(V_C - \frac{Q}{2C}) - (V_C + \frac{Q}{2C}) cos\left(DT_S/\sqrt{LC}\right)}{sin\left(DT_S/\sqrt{LC}\right)} sin\left(t/\sqrt{LC}\right)$	aV_C
Discharge coefficient $b = 2\left(1 - cos\frac{DT_S}{\sqrt{LC}}\right)\left(\frac{DT_S}{\sqrt{LC}} sin\left(\frac{DT_S}{\sqrt{LC}}\right)\right)$, and charge coefficient $a = (2 - b)$.				

7.2 Median and Average Values of Component State Variables

In non-isolated hybrid converters, an input charge is transferred to output through synchronous operations where an inductor soft-charges or soft-discharges a number of flying capacitors. Figure 7.1 illustrates general circuit models in two operating phases, capacitor charging and discharging. For simplicity, one capacitor C is used in this analysis, while the method can be expanded, as shown in Section 7.3, to analyze multiple capacitors connected in series or parallel in place of C.

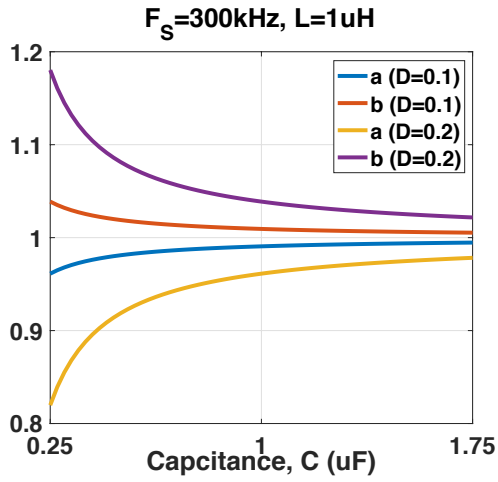


Figure 7.2. Charging and discharging coefficients with different duty cycles and flying capacitance

In a typical steady-state analysis, nominal average values with small ripples are considered for capacitor voltage and inductor current. For example, a constant value of capacitor voltage is assumed to find an inductor current ripple, while a constant inductor current is assumed to find the capacitor voltage ripple. A byproduct of this assumption is the linear ripple approximation where the average values are the same as the median values. The median value is the mean of the maximum and minimum values. While this traditional linear-ripple analysis is convenient, e.g. in calculating steady-state solution and conversion ratios, it ignores the resonant nature of the L-C tank that causes median values to deviate from average values. As a result, the typical steady-state analysis fails to explain practical behaviors such as unbalanced voltage levels of flying capacitors and fluctuations in inductor current ripples because of control timing imperfections. To address the modeling of balancing performance, state-space approaches have been considered in [97, 98]. While general in nature, these approaches do not offer intuitive circuit interpretations and converter true characteristics for higher-order effects which, in some cases, impact the balancing performance significantly.

In order to develop a more intuitive analytical method to explain the balancing issues in the hybrid converters, we start by recognizing and calculating the difference between average and median values. From the circuit model in Fig. 7.1, expressions for capacitor voltage $v_C(t)$ and average voltage $V_{C,av}$ during charging and discharging phases can be found in Table 7.1. The values are expressed using median capacitor voltage V_C, median inductor current I_L, charge Q, switching period T_S, duty cycle D, and capacitor voltages $v_C(0)$ and $v_C(DT_S)$ at the beginning and the end of a charging phase, respectively. The discharge coefficient b and charge coefficient a express the relationship between average and median capacitor voltages in the two operating phases. Accordingly, the relationship between median inductor current I_L and its average $I_{L,av}$ value can be derived as $I_L = \frac{1}{b} I_{L,av}$. Assuming steady-state operation in one cycle including one charging and one discharging phase, the ripple of the inductor current can be calculated as $\triangle i_L = bV_C \frac{DT_S}{L}$, where V_C is the median voltage across the inductor in the discharging phase (Fig. 7.1a). More detailed derivations are provided in Appendix D.

In this section, we assume the same D and Q, i.e. charge balance, for both the charging and discharging phases. More detailed analyses with variations in D and Q and other related parameters, e.g, due to control timing imperfections, are considered in Sections 7.3 and 7.4.

As illustrated in Fig. 7.2, coefficients a and b are symmetric across unity, indicating that the deviations of average values from the median in the charging and discharging phases have the same absolute value and opposite signs. Also from expressions in Table 7.1, the coefficients, and thus average-median deviations, are independent of the capacitor the bias voltage, which means that the expressions can be applied directly to the analysis of voltage levels for different capacitors in multi-level hybrid converters. In particular, both median values and charging coefficients are utilized to represent actual average values for accurate calculations of capacitor voltages and inductor currents and explanations of behavior when applied to DPMIH and 3LB converters in Sections 7.3 and 7.4, respectively.

7.3 Application to the DPMIH Converter

7.3.1 Ideal Timing

A four-level DPMIH converter shown in Fig. 7.3 is chosen as an example from the MIH converter family. The converter has 3 identical capacitors, 4 identical inductors, and four switching nodes 1-4 whose voltages are averaged by the inductors to generate the output voltage. Details of converter operation can be found in [17]. The analysis in [17] uses small ripple approximation, i.e. only the DC value for the output capacitor voltage with a reasonable assumption that its capacitance is significantly larger than the capacitance of flying capacitors.

Table 7.2 summarizes the voltage-second balance expressions for the inductors during inductor charging states 1 and 3 using the median voltages $V_{C_{1-3}}$ of the flying capacitors and coefficients b and b_S. Consistent with the analysis in Section 7.2, the coefficient of an inductor when connected with one capacitor is b. This is the case for L_1 and L_4. On the other hand, when charged, L_2 and L_3 are connected in series with two series-connected capacitors, one being

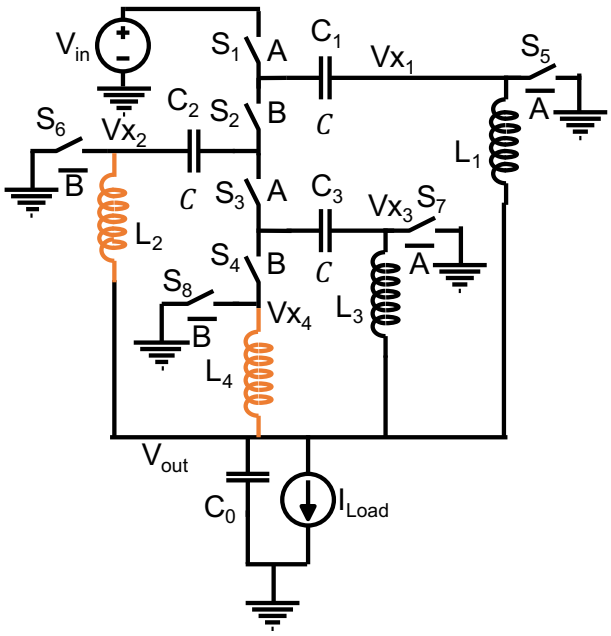


Figure 7.3. A four-level DPMIH converter

Table 7.2. Volt-Second Balance at inductors of DPMIH converter

Inductor	Expressions
L_1	$(V_{in} - V_{C_1} - V_{out})\, bD_1 = V_{out}\,(1 - D_3)$
L_2	$(V_{C_1} - V_{C_2} - V_{out})\, b_S D_3 = V_{out}\,(1 - D_1)$
L_3	$(V_{C_2} - V_{C_3} - V_{out})\, b_S D_1 = V_{out}\,(1 - D_3)$
L_4	$(V_{C_3} - V_{out})\, bD_3 = V_{out}\,(1 - D_1)$
$b_S = 2\left(1 - cos\frac{DT_S}{\sqrt{L\frac{C}{2}}}\right)\left(\frac{DT_S}{\sqrt{L\frac{C}{2}}} sin\left(\frac{DT_S}{\sqrt{L\frac{C}{2}}}\right)\right)$	

charged, and one being discharged. Hence, a different coefficient b_S, as expressed in Table 7.2, is required. In the expression for b_s, $C/2$ accounts for two capacitors connected in series.

In the scenario of ideal control timing, $D_1 = D_3 = D$, expressions for output voltage V_{out}, capacitor median voltages $V_{C_{1-3}}$ and inductor median currents $I_{L_{1-4}}$ can be calculated as functions of V_{in}, D, and coefficients b, and b_S as shown in Table 7.3.

Some interesting converter characteristics can be inferred from the analytical results. For example, as $b > 1$, V_{out} is always greater than $\frac{DV_{in}}{4}$, the expected nominal voltage. This was also described in [17]. In addition, the inductor current peak-to-peak ripples are always equal to each other regardless of the equivalent capacitance they are connected with. The median

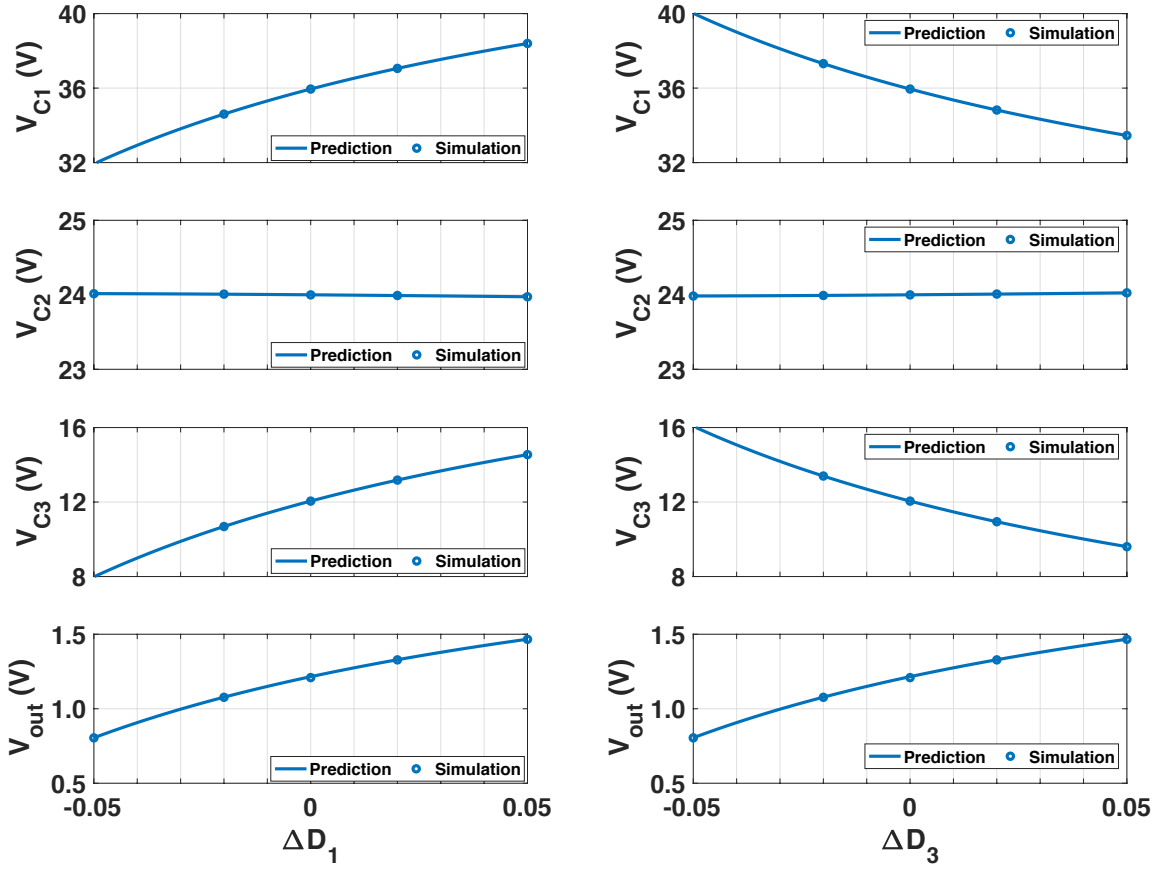
Table 7.3. Capacitor voltages and inductor currents in DPMIH converter (Ideal Timing)

Output Voltage	$V_{out} = \frac{V_{in}}{2\left(1+\frac{1-D}{bD}\right)+2\left(1+\frac{1-D}{b_S D}\right)}$
Flying Capacitor Median Voltages	$V_{C_1} = \frac{\left\{2\left(1+\frac{1-D}{bD}\right)+\left(1+\frac{1-D}{b_S D}\right)\right\}V_{in}}{2\left(1+\frac{1-D}{bD}\right)+2\left(1+\frac{1-D}{b_S D}\right)}$
	$V_{C_2} = \frac{V_{in}}{2}$
	$V_{C_3} = \frac{\left(1+\frac{1-D}{bD}\right)V_{in}}{2\left(1+\frac{1-D}{bD}\right)+2\left(1+\frac{1-D}{b_S D}\right)}$
Inductor Median Currents	$I_{L_1} = I_{L_4} = \frac{1}{bD} * \frac{I_{out}}{2\left(1+\frac{1-D}{bD}\right)+2\left(1+\frac{1-D}{b_S D}\right)}$
	$I_{L_2} = I_{L_3} = \frac{1}{b_S D} * \frac{I_{out}}{2\left(1+\frac{1-D}{bD}\right)+2\left(1+\frac{1-D}{b_S D}\right)}$

Table 7.4. Capacitor voltages and inductor currents in DPMIH converter (Non-ideal Timing)

Output Voltage	$V_{out} = \frac{V_{in}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
Flying Capacitor Median Voltages	$V_{C_1} = \frac{\left\{\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)\right\}V_{in}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
	$V_{C_2} = \frac{\left\{\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)\right\}V_{in}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
	$V_{C_3} = \frac{\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)V_{in}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
Inductor Median Currents	$I_{L_1} = \frac{1}{b_{(1)}D_1} * \frac{I_{out}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
	$I_{L_2} = \frac{1}{b_{S(3)}D_3} * \frac{I_{out}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
	$I_{L_3} = \frac{1}{b_{S(1)}D_1} * \frac{I_{out}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$
	$I_{L_4} = \frac{1}{b_{(3)}D_3} * \frac{I_{out}}{\left(1+\frac{1-D_1}{b_{(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{S(3)}D_3}\right)+\left(1+\frac{1-D_1}{b_{S(1)}D_1}\right)+\left(1+\frac{1-D_3}{b_{(3)}D_3}\right)}$

currents are the same for the inductors connected to the same equivalent capacitance but they differ with different equivalent capacitances. Particularly, the median currents are smaller for inductors connected to smaller equivalent capacitance. Specific to this DPMIH converter, one can predict that $i_{L_{2,3}}$ are slightly lower than $i_{L_{1,4}}$. However, it is important to note that their average current values $I_{L_i,av}$ during inductor charging states are the same because of the charge



(a) D_1 Variation

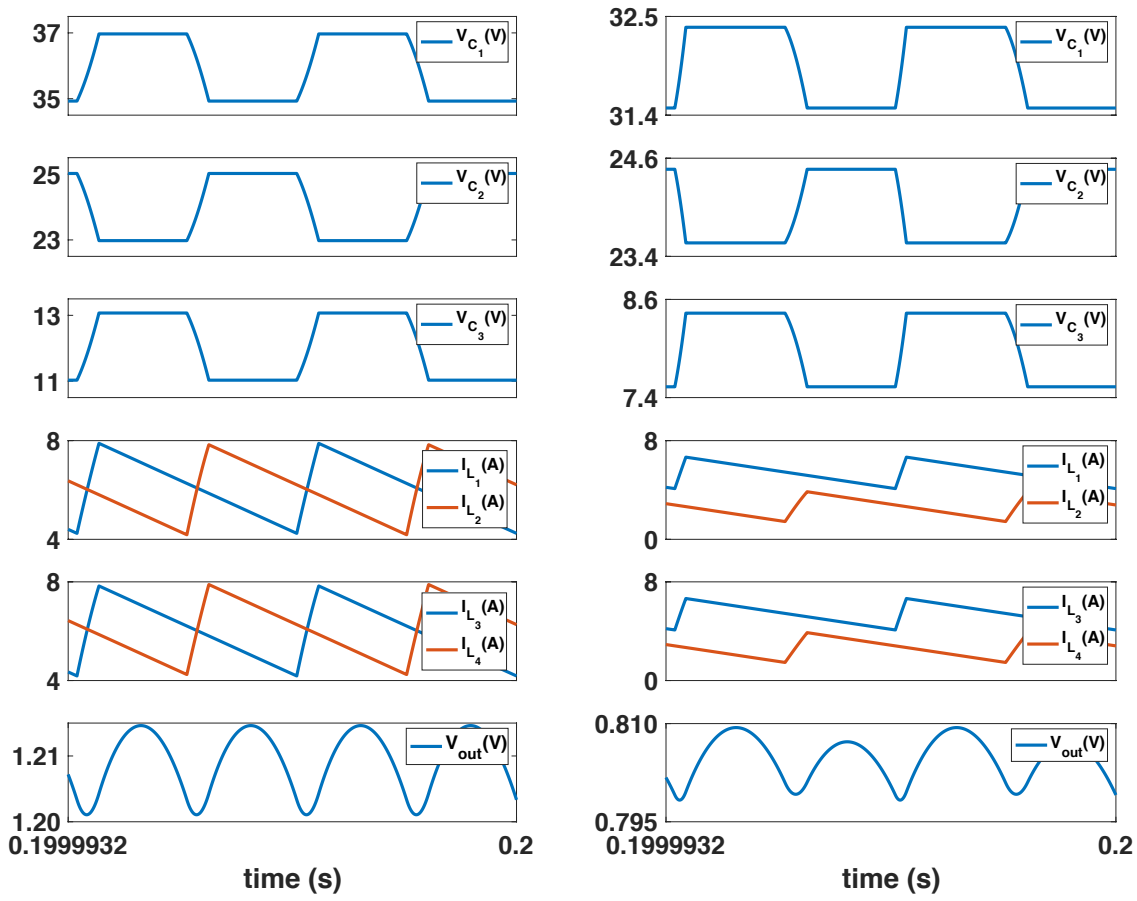
(b) D_3 Variation

Figure 7.4. Variation of flying capacitor and output voltages in DPMIH converter with non-ideal timing (Operating condition: $V_{in} = 48V$, $C_1 = C_2 = C_3 = 1\mu F$, and $L_1 = L_2 = L_3 = L_4 = 1\mu H$, $f_S = 300kHz$ and $R_{Load} = 0.05\Omega$)

balance of capacitors in a steady state.

7.3.2 Non-Ideal Timing

The analysis of Section 7.3.1, which assumes ideal timing can be modified to incorporate duty cycle mismatches caused by control timing imperfections. In this section, we consider two different duty cycles, D_1 for phase A (State 1) and D_3 for phase B (State 3) in the DPMIH converter in Fig. 7.3 [17]. Accordingly, the expressions for the output voltage, flying capacitor median voltages, and inductor median current from Table 7.3 can be rewritten as shown in Table



(a) DPMIH converter with ideal timing ($D_1 = D_3 = D = 0.1$)

(b) DPMIH converter with non-ideal timing ($D_1 = 0.05, D_3 = 0.1$)

Figure 7.5. Waveforms of DPMIH converter in steady-state operation (Operating condition: $V_{in} = 48V$, $C_1 = C_2 = C_3 = 1\mu F$, $L_1 = L_2 = L_3 = L_4 = 1\mu H$, $f_S = 300kHz$ and $R_{Load} = 0.05\Omega$)

7.4. Since coefficient b depends on the duty cycle in each inductor charging state, D_1 for State 1 and D_3 for State 3, the expressions in Table 7.4 include $b_{(1)}$ and $b_{S(1)}$ for State 1, and $b_{(3)}$ and $b_{S(3)}$ for State 3. In an ideal timing operation where $D_1 = D_3 = D$ and thus $b_{(1)} = b_{(3)} = b$ and $b_{S(1)} = b_{S(3)} = b_S$, the expressions in Table 7.4 are simplified and become equal to the expressions in Table 7.3.

7.3.3 Verification

The equations from Table 7.4 have been used to predict changes in the flying capacitor and output voltages with variations of duty-cycles D_1 and D_3 for a DPMIH (SCB) converter and then compared with simulation results using PLECS simulator, as illustrated in Figs. 7.4 and 7.5. For the simulations in PLECS, the DPMIH (SCB) converter circuit is implemented using a nearly ideal switches, inductors, and capacitors with insignificant resistance and parasitics.

Considering a nominal duty cycle value of 0.1, D_1 is varied by a maximum amount of ± 0.05 while D_3 is kept at 0.1. (Fig. 7.4a) and vice versa (Fig. 7.4b). As shown in Fig. 7.4, the simulated results and analytical predictions match perfectly, verifying the method to predict the converter behavior. From the result in Fig. 7.4 and also from V_{out} expression in Table 7.4, it is intuitive that duty cycle variations in D_1 and D_3 affect the output voltage V_{out} in exactly the same significant way. Interestingly, however, the relatively large imperfections in the duty cycles do not shift the flying capacitor voltages from their ideal values by any significant amount. Particularly, a 50% change of duty cycle, i.e. from 0.1 to 0.05 or 0.15, only changes V_{C_1} and V_{C_3} by less than 10% and ~33%, respectively. Fig. 7.5 visually depicts the converter operational waveforms of capacitor voltages, inductor currents, and output with ideal timing (Fig. 7.5a) and with imperfect timing (Fig. 7.5b). In the non-ideal timing scenario (Fig. 7.5b), the inductor currents are very different, i.e. $i_{L_{13}}$ is ~2 times $i_{L_{2,4}}$, approximately proportional to the charging duty cycle, i.e. $D_3 = 2D_1$, in order to maintain the same charge flow Q through the two inductor charging phases, as required for charge balance on the flying capacitors.

7.4 Application to the 3-Level Buck Converter

It has been shown that in odd-level FLML converters flying capacitor voltages are very sensitive to timing mismatches and other higher-order effects [98]. In this section, it is shown how the proposed method yields accurate predictions in the 3LB converter, which is a representative of odd-level FCML converters.

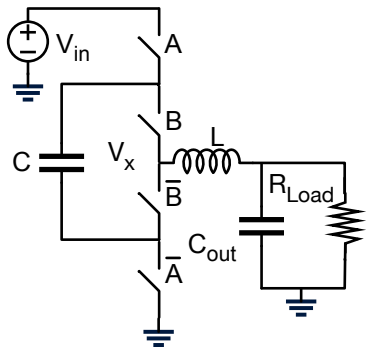


Figure 7.6. A 3-level Buck (3LBC) converter schematic

Table 7.5. 3-Level Buck converter parameters with ideal timing

$(Vin - V_C - V_{out})bD + (V_C - V_{out})bD = V_{out}(1-2D)$
$V_{in} - aVc = bV_c$
$V_{out} = \frac{V_{in}}{2+\frac{(1-2D)}{bD}}$
$V_C = \frac{1}{b+a}V_{in} = \frac{1}{2}V_{in}$

7.4.1 Ideal Timing

The 3-Level Buck (3LB) converter depicted in Fig. 7.6 is ideally operated using a two non-overlapped 180^o-out-of-phase signals A and B that have the same duty cycle D with no timing mismatch. Applying the same method above with average values described by median values and coefficients a and b, the converter electrical parameters can be derived as shown in Table 7.5, reflecting the results that could be obtained using exact numerical solution based on the augmented state-space approach, as discussed in [98].

Table 7.6. Inductor currents of a 3-level Buck converter with non-ideal timing

State	Median Current	Minimum Current	Maximum Current
1	$I_{L(1)} = \frac{Q_1}{b_{(1)}D_1T_S}$	$I_{L,min(1)} = I_{L_1} - \frac{1}{2}\{(V_{in}-V_C)-V_{out}\}\frac{b_{(1)}D_1T_S}{L}$	$I_{L,max(1)} = I_{L_1} + \frac{1}{2}\{(V_{in}-V_C)-V_{out}\}\frac{b_{(1)}D_1T_S}{L}$
2	$I_{L(2)} = \frac{1}{2}(I_{L(1)}+I_{L(3)}) + \frac{1}{4}\{b_{(1)}D_1(V_{in}-V_C-V_{out}) - b_{(3)}D_3(V_C-V_{out})\}\frac{T_S}{L}$	$I_{L,min(2)} = I_{L_2} - \frac{1}{2}V_{out}\frac{D_2T_S}{L}$	$I_{L,max(2)} = I_{L_2} + \frac{1}{2}V_{out}\frac{D_2T_S}{L}$
3	$I_{L(3)} = \frac{Q_3}{b_{(3)}D_3T_S}$	$I_{L,min(3)} = I_{L_3} - (V_C - V_{out})\frac{b_{(3)}D_3T_S}{L}$	$I_{L,max(3)} = I_{L_3} + \frac{1}{2}(V_C - V_{out})\frac{b_{(3)}D_3T_S}{L}$
4	$I_{L(4)} = \frac{1}{2}(I_{L_1}+I_{L_3}) - \frac{1}{4}\{b_{(1)}D_1(V_{in}-V_C-V_{out}) - b_{(3)}D_3(V_C-V_{out})\}\frac{T_S}{L}$	$I_{L,min(4)} = I_{L_4} - \frac{1}{2}V_{out}\frac{D_4T_S}{L}$	$I_{L,max(4)} = I_{L_4} + \frac{1}{2}V_{out}\frac{D_4T_S}{L}$

7.4.2 Non-Ideal Timing

The benefits of the proposed method are more apparent when it is applied to predict the 3LB converter behavior with non-ideal timing. To generalize and reflect timing imperfections, one switching cycle is divided into 4 states associated with 4 duty cycles: D_1 and D_3 for two inductor charging states, and D_2 and D_4 for two inductor freewheeling states; and $D_1 + D_2 + D_3 + D_4 = 1$. Accordingly, the inductor median currents in these states are $I_{L(1)}$, $I_{L(2)}$, $I_{L(3)}$ and $I_{L(4)}$. The charge from V_{in} to flying capacitor C during D_1 interval is Q_1. The charge from C transferred to V_{out} in D_3 interval is Q_3. Using the same method from Section 7.2 and volt-second balance, the median, maximum, and minimum inductor currents can be derived as shown in Table 7.6, describing the converter behavior in terms of inductor current in all 4 operating states.

In the operation of a 3LB converter, States 1 and 3 are of interest as the flying capacitor gets charged by Q_1 and discharged by Q_3. The relationship between these two quantities can be derived from parameters in Table 7.6 as:

$$Q_3 = \left[\frac{Q_1}{b_{(1)} D_1} - \frac{1}{2} \frac{V_{out} T_S^2}{L} (D_2 - D_4) \right] b_{(3)} D_3. \tag{7.1}$$

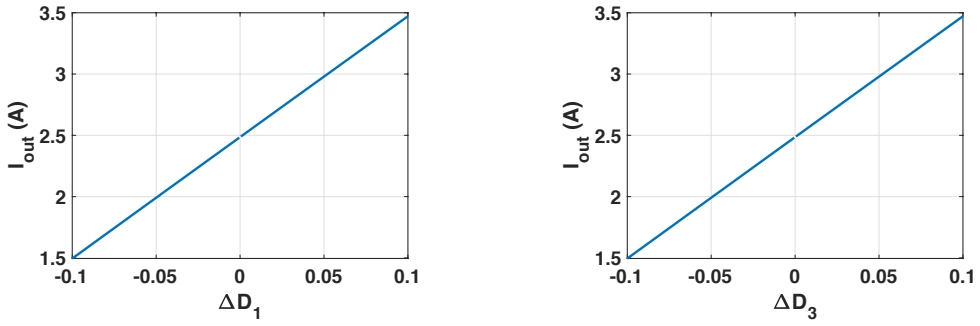
From this $Q_1 - Q_3$ relationship in Eq. 7.1, the accumulated voltage in the flying capacitor during one switching the period can be calculated as:

$$\triangle V_C(T_S) = \frac{Q_1}{C} - \frac{Q_3}{C} = \frac{1}{C} \left[\left(1 - \frac{b_{(3)} D_3}{b_{(1)} D_1} \right) Q_1 + \frac{1}{2} \frac{V_{out} b_{(3)} D_3 T_S^2}{L} (D_2 - D_4) \right] \tag{7.2}$$

In Eq. 7.2, the capacitor voltage accumulated in one switching period $\triangle V_C(T_S)$ has two terms, the first depends on D_1 and D_3 relationship while the second depends on D_2 and D_4, as detailed by 11 cases in Table 7.7. In Case 1 of ideal timing with no duty cycle mismatch, i.e. $D_1 = D_3$ and $D_2 = D_4$, these two terms go to zero and so does $\triangle V_C(T_S)$, leading to the ideal balanced capacitor voltage of $V_C = \frac{1}{2} V_{in}$. However, a mismatch in one of the duty cycle

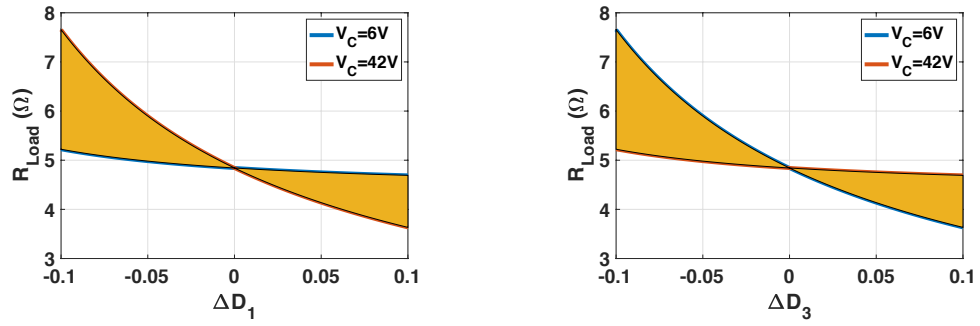
pairs, $D_1 \neq D_3$ ($D_2 \neq D_4$), while the other pair is matched , $D_2 = D_4$ ($D_1 = D_3$), would lead to a non-zero voltage $\triangle V_C(T_S)$ accumulated every cycle, which eventually causes the flying capacitor voltage V_C to saturate to V_{in} or zero dependent on the sign of $\triangle V_C(T_S)$. Particularly, positive charge and voltage accumulation on C in every switching cycle will cause V_C saturated to V_{in}, while V_C saturates to zero with negative charge and voltage accumulation. These are Cases 2-5 in Table 7.7.

When the two duty cycle pairs have opposite mismatches, $\triangle V_C(T_S)$ can still have a non-zero value leading to V_C saturation as in Cases 6, 8, 9, and 11 in Table 7.7. However, the differences between D_1-D_3 pair and D_2-D_4 pair can also be just right, as in Cases 7 and 10, to make the first term in Eq. 7.2 complement the second term, leading to $\triangle V_C(T_S) = 0$. In Cases 7



(a) D_1 Variation **(b)** D_3 Variation

Figure 7.7. Current-source behavior of 3LB converter with non-ideal timing (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$ and $D_{1-4}(ideal) = 0.25$)



(a) D_1 Variation **(b)** D_3 Variation

Figure 7.8. Output resistive load range for 3LB converter to maintain $V_{in}/8 \leq V_C \leq 7V_{in}/8$ (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$ and $D_{1-4}(ideal) = 0.25$)

Table 7.7. Flying capacitor voltage with timing mismatch

Case	$D_1$and D_3	D_2 and D_4	$\triangle V_C(T_S)$	Comment
1	$D_1 = D_3$	$D_2 = D_4$	0	Ideal,$V_C = \frac{1}{2}V_{in}$
2	$D_1 = D_3$	$D_2 > D_4$	+	V_C saturates to V_{in}
3	$D_1 = D_3$	$D_2 < D_4$	-	V_C saturates to $0V$
4	$D_1 > D_3$	$D_2 = D_4$	+	V_C saturates to V_{in}
5	$D_1 < D_3$	$D_2 = D_4$	-	V_C saturates to $0V$
6	$D_1 > D_3$	$D_2 < D_4$	+	V_C saturates to V_{in}
7			0	$0 < V_C < Vin$
8			-	V_C saturates to $0V$
9	$D_1 < D_3$	$D_2 > D_4$	+	V_C saturates to V_{in}
10			0	$0 < V_C < Vin$
11			-	V_C saturates to $0V$

and 10, V_C can settle to a steady-state voltage between V_{in} and zero.

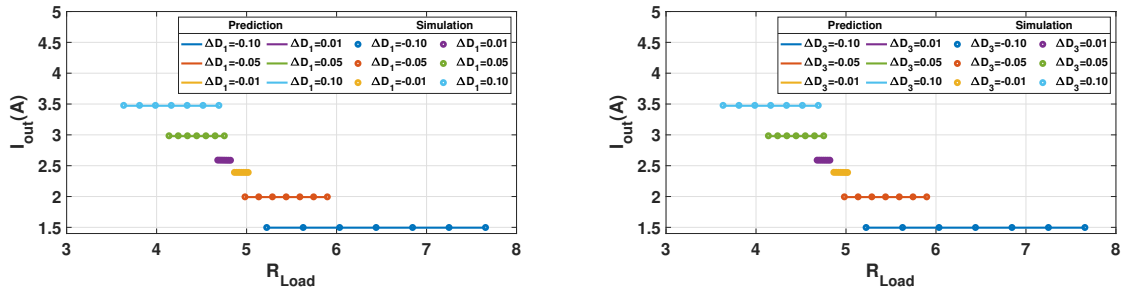
While it is intuitive in the cases where V_C saturates to supply rails because of positive or negative charge accumulation on C in each cycle, it is of interest to analyze the converter characteristics for non-saturated V_C, i.e. for $\triangle V_C(T_S)$ to become zero. Assuming insignificant losses from parasitic resistances, utilizing $Q_1 = \frac{V_{out}Q_{out}}{V_{in}}$, the converter output current can be found as:

$$I_{out} = \frac{V_{in}T_S(D_4 - D_2)}{2L\left(\frac{1}{b_{(3)}D_3} - \frac{1}{b_{(1)}D_1}\right)} \tag{7.3}$$

This expression of I_{out} implies that 3LB converter behaves as a DC current source whose value is controlled by timing mismatches in duty cycles D_{1-4}, and independent of V_{out}. Figure 7.7 illustrates the current source behavior with duty cycle variations in D_1 and D_3. This current-

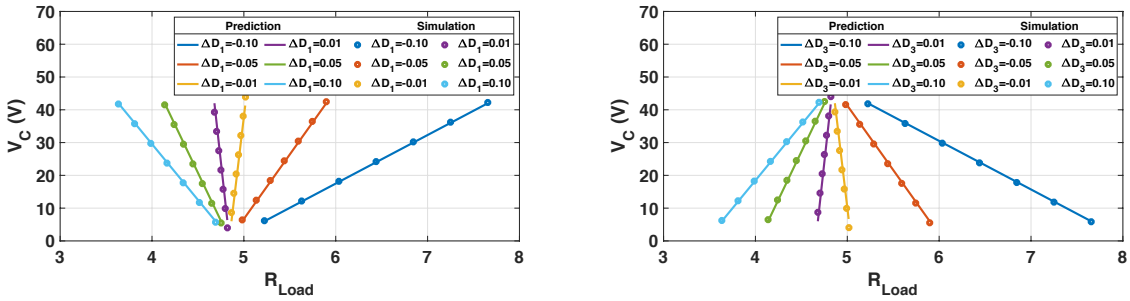
Table 7.8. 3-Level Buck converter with non-ideal timing

$b_{(1)}(V_{in} - V_C - V_{out})D_1 + b_{(3)}(V_C - V_{out})D_3 = V_{out}(D_2 + D_4)$
$V_{out} = I_{out}R_{Load} = \frac{V_{in}T_S(D_4-D_2)}{2L\left(\frac{1}{b_{(3)}D_3} - \frac{1}{b_{(1)}D_1}\right)}R_{Load}$
$V_C = \frac{\left(b_{(1)}D_1 + b_{(3)}D_3 + D_2 + D_4\right)V_{out} - b_{(1)}D_1V_{in}}{b_{(3)}D_3 - b_{(1)}D_1}$
$R_{Load} = \frac{V_C(b_{(3)}D_3 - b_{(1)}D_1) + b_{(1)}D_1V_{in}}{\left(b_{(1)}D_1 + b_{(3)}D_3 + D_2 + D_4\right)I_{out}}$



(a) D_1 Variation **(b)** D_3 Variation

Figure 7.9. Predicted and simulated current-source behavior of 3LB converter (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$ and $D_{1-4}(ideal) = 0.25$)

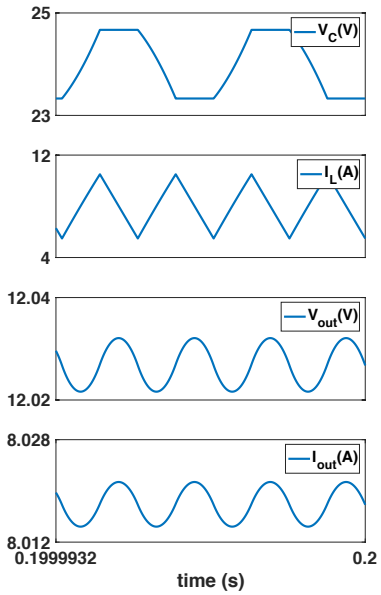


(a) D_1 Variation **(b)** D_3 Variation

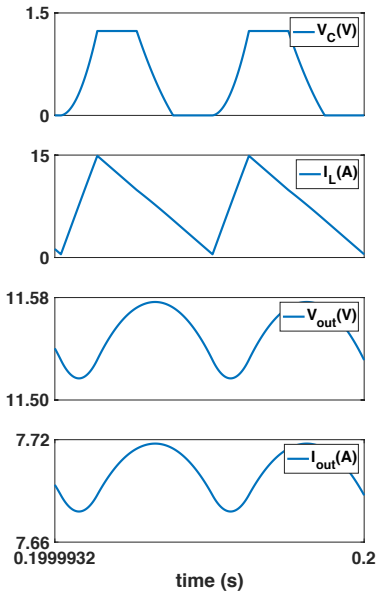
Figure 7.10. Predicted and simulated flying capacitor voltage variations versus load resistance for 3LB converter (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$ and $D_{1-4}(ideal) = 0.25$)

source behavior can cause output voltage saturation if the converter is tested with a current-source load whose value is not exactly matched with I_{out} in Eq. 7.3.

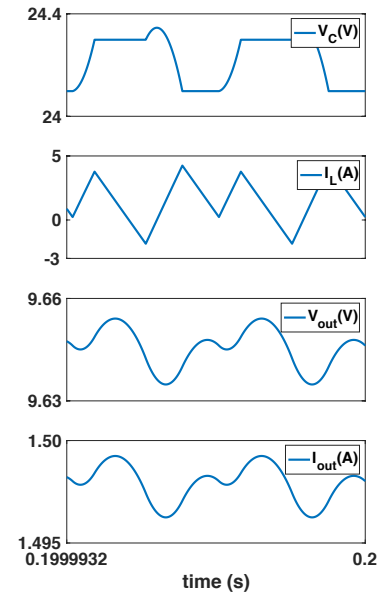
Using a resistive load, it is possible to calculate output voltages as shown in Table 7.8. The current-source behavior also causes the flying capacitor median voltage V_C to move with the resistive load R_{Load}. Therefore, a constraint in the range of V_C would set a feasible range of R_{Load}. Fig. 7.8 illustrates an example of R_{Load} required for V_C to stay within $\frac{V_{in}}{8} \leq V_C \leq \frac{7V_{in}}{8}$ when there are variations in D_1 or D_3. Fig. 7.9 presents R_{Load} ranges for different I_{out} generated by D_1 or D_3 variations. Fig. 7.10 shows that flying capacitor voltage varies linearly with changes in output load resistance. Interestingly, the smaller the duty-cycle the mismatch is the more sensitive the flying capacitor voltage is to the resistive load value. Table 7.8 lists the expressions and parameters related to the 3LB converter.



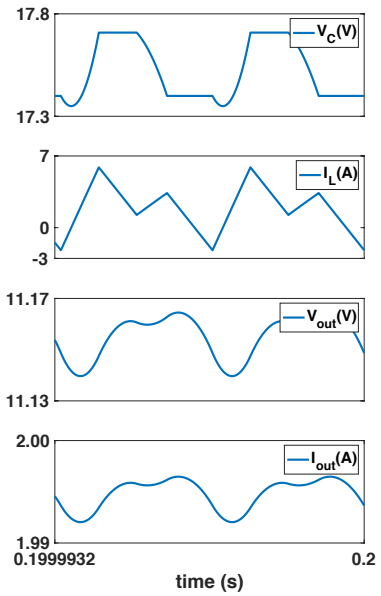
(a) Ideal timing: $D_{1-4} = 0.25$ and $R_{Load} = 1.5\Omega$



(b) Non-ideal timing: $D_1 = 0.24$, $D_2 = 0.26$, $D_{3-4} = 0.25$ and $R_{Load} = 1.5\Omega$



(c) Non-ideal timing: $D_1 = 0.15$, $D_2 = 0.35$, $D_{3-4} = 0.25$ and $R_{Load} = 6.4393\Omega$



(d) Non-ideal timing: $D_3 = 0.2$, $D_4 = 0.3$, $D_{1-2} = 0.25$ and $R_{Load} = 5.5921\Omega$

Figure 7.11. Waveforms of 3LB converter with different timing scenarios and load resistances (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, and $f_S = 300kHz$)

7.4.3 Verification

A simulation setup similar to the DPMIH converter above is used for a 3LB converter. Simulation results have been overlaid on the same graph with the analytical prediction in Figs. 7.9 and 7.10, verifying the analytical results and calculations for the 3LB converter. To visually illustrate the operation and behavior of the converter in different timing scenarios, i.e., ideal and non-ideal timing, Fig. 7.11 is added. Fig. 7.11a shows an operation with ideal timing. In Fig. 7.11b, with a small duty cycle mismatch for D_1 and D_2, the flying capacitor voltage saturates to 0 when an undesirable R_{Load} outside of the range calculated in Section 7.4.2 is used. Figs 7.11c and 7.11d show operations of the converter at relatively large duty cycle mismatch, but the flying capacitor voltage maintains its level around $\sim V_{in}/2$ when a proper load resistance is used.

7.5 Chapter Summary

This chapter presents a simple, intuitive, and general method to predict the state variables, flying capacitor voltages, and inductor currents, in hybrid converters. The method has been demonstrated and verified using two example converters, a Dual Phase Multi Inductor (DPMIH) or Series Capacitor Buck (SCB) converter and the 3-Level Buck(3LB) converter representing the MIH converter family and FCML converters, respectively.

The results from this work also distinguish the two converter characteristics when timing imperfections are applied to the operation. With timing mismatches, flying capacitor voltage levels in both converters change. However, while the flying capacitor voltages of the DPMIH converter do not vary significantly, the flying capacitor voltage of the 3LB converter can vary a lot and even saturate to either V_{in} or ground. It is also found that the 3LB exhibits characteristics of an ideal current source under certain operating conditions.

Chapter 7, in partial, is a reprint of the material as it appears in "Demystifying Capacitor Voltages and Inductor Currents in Hybrid Converters," in 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8 by the authors Das, Ratul; Celikovic, Janko; Abedinpour, Siamak; Mercer, Mark; Maksimovic, Dragan and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

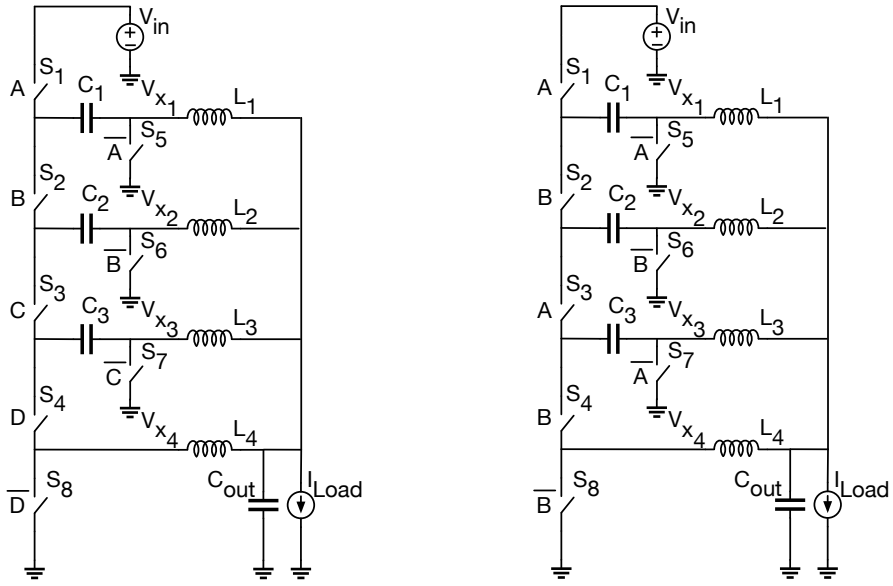
Chapter 8

An Accurate Approach to Calculate and Measure Capacitor Voltage and Inductor Current Levels in Hybrid Converters

8.1 Introduction

In power converters, it is essential to understand, calculate and measure the right voltage and current levels of the circuit components to evaluate the converters' operation and performance. Particularly important in hybrid converters, these levels are to determine if the converter has voltage or current imbalances. Traditionally, average values are used to determine voltage and current levels. While average values accurately show the voltage and current stresses on the components, they do not represent the right operating levels. In the case of the hybrid converters, they can lead to misinterpretations of the converter states and levels and, thus, to problems in converter control and regulation.

In a switching converter, the components' current and voltage waveforms have either triangular, trapezoidal, sinusoidal, or semi-sinusoidal ripples on top of the DC levels. While triangular, sinusoidal, or semi-sinusoidal waveforms are found in traditional pulse-width modulated (PWM) or resonant converters, trapezoidal waveforms are more unique to the flying capacitor voltages in switched-capacitor based hybrid converters operated with PWM duty cycle control. Because the trapezoidal waveforms can have ripples with large amplitudes, different



(a) 4-phase **(b)** 2-phase

Figure 8.1. 4-level multi-inductor hybrid converter as an example of hybrid converter

phase shifts, and different duty cycles, using their average values provides a misinterpretation of the capacitor voltage levels. Moreover, the capacitor voltage values are also used to calculate inductor current values and output voltage levels. Therefore, it is necessary to have an accurate method to calculate the voltage and current levels to evaluate the converter operations. To meet this need, the work reported in [34] mentioned the usage of median values instead of average values in converter analyses. Later, [19] emphasized the matter and included a method to directly calculate the median voltages and currents through volt-second balance analysis. However, detailed explanations and verification were not provided in the chapter that focused on hybrid converters' balance/imbalance performance.

The key contribution of this chapter is to provide detailed descriptions and verification to clearly illustrate the important characteristics and modeling of hybrid converters, including popular flying capacitor multilevel (FCML) and multi-inductor hybrid (MIH) converters, using median values. The converter shown in Fig. 8.1 is used as an example of hybrid converters for the analysis. To reduce secondary effects from practical implementation [17], simulation results

are used to verify the analysis and modeling method.

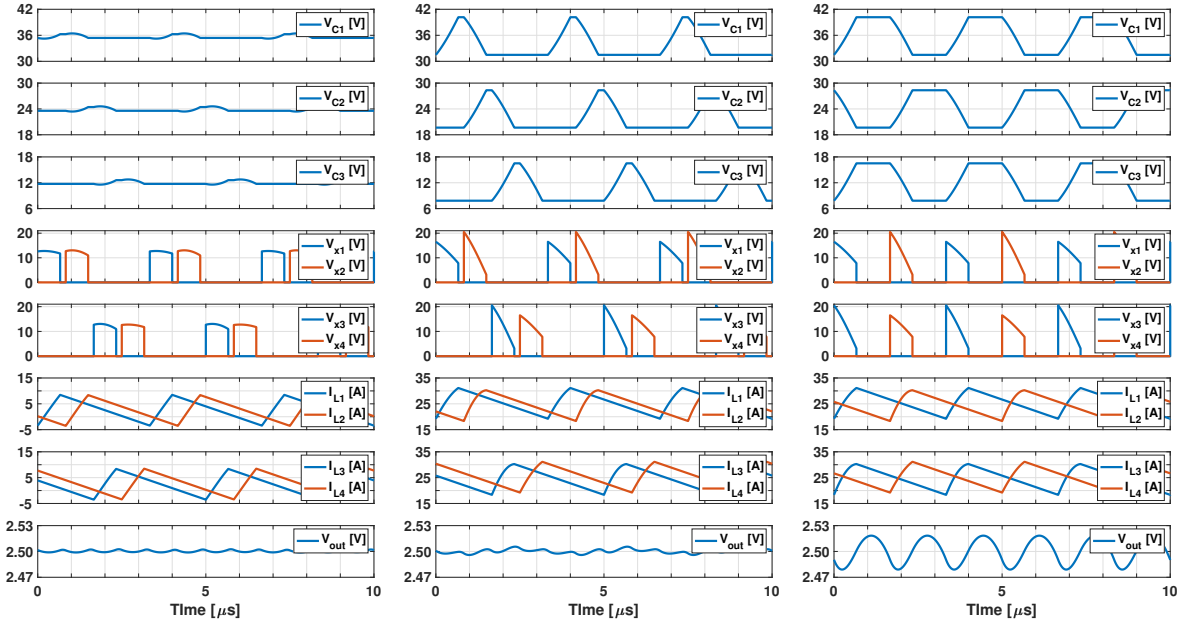
The chapter is organized as follows. In section 8.2, we briefly describe the example hybrid converter as a vehicle for the analysis part in section 8.3 to show different effects on the levels of the flying capacitor voltages, output voltages, and inductor currents originated from practical finite capacitance selections. The chapter is summarized and concluded in section 8.4.

8.2 4-level Multi-Inductor Hybrid Converter

A 4-level multi-inductor hybrid (MIH) converter, shown in Fig. 8.1 is selected as the vehicle for the analysis. The operating principles and experimental results of this converter can be found in [17]. Similar converters with a different number of levels can also be found in [52, 53]. The example converter can be operated with either four 90°-phase-shifted control signals (Fig. 8.1a) or two 180°-phase-shifted signals (Fig. 8.1b). The converter's power density mostly depends on the passive components, the inductors, and the flying capacitors. Therefore, to increase current and power density, the passive component sizes should be minimized while keeping acceptable efficiency and circuit operation. With the design constraints, a typical component selection and operating conditions are provided in Table 8.1. Based on this selection, the converter has been simulated with 4-phase operations in light load (10A) and heavy load (100A) conditions, as shown in Fig. 8.2a and 8.2b. The 2-phase operation in a heavy load condition is also provided in 8.2c. The simulation results show that the average values of the

Table 8.1. Typical component selection and operating conditions of the example MIH converter

Input Voltage, V_{in}	48V
Flying Capacitors, $C_{1,2,3}$	$2\mu F$
Inductors, $L_{1,2,3,4}$	$560nH$
Duty cycle, D	0.2
Output Capacitor	$100\mu F$
Operating Frequency	300kHz
Heavy Load	100A
Light Load	10A



(a) 4-phase operation, 10A **(b)** 4-phase operation, 100A **(c)** 2-phase operation, 100A

Figure 8.2. Waveforms of 4-level MIH converter with different operations and loads

capacitor voltages and inductor currents significantly depend on the ripples and curvatures in the charging and discharging phases and their timing. More curvatures can be seen at heavier loads where using average values is expected to result in larger errors.

8.3 Median and Average Value Analysis

To find a more accurate method to model and calculate the converter voltages and currents, the converter is first analyzed using the standard Volt-Second balance at the inductors with a small ripple approximation for capacitor voltages and inductor currents (i.e., approximated

Table 8.2. Traditional Volt-Second balance at inductors of the MIH converter (Approximated model)

Inductor	Expressions
L_1	$(V_{in} - V_{C_1} - V_{out})\,D_1 = V_{out}\,(1 - D_1)$
L_2	$(V_{C_1} - V_{C_2} - V_{out})\,D_2 = V_{out}\,(1 - D_2)$
L_3	$(V_{C_2} - V_{C_3} - V_{out})\,D_3 = V_{out}\,(1 - D_3)$
L_4	$(V_{C_3} - V_{out})\,D_4 = V_{out}\,(1 - D_4)$

Table 8.3. Modified Volt-Second balance at inductors of MIH converter (Accurate model for median values)

Inductor	Expressions
L_1	$(V_{in} - V_{C_1} - V_{out})\, bD_1 = V_{out}\,(1 - D_1)$
L_2	$(V_{C_1} - V_{C_2} - V_{out})\, b_S D_2 = V_{out}\,(1 - D_2)$
L_3	$(V_{C_2} - V_{C_3} - V_{out})\, b_S D_3 = V_{out}\,(1 - D_3)$
L_4	$(V_{C_3} - V_{out})\, bD_4 = V_{out}\,(1 - D_4)$
$b_S = 2\left(1 - cos\frac{DT_S}{\sqrt{L\frac{C}{2}}}\right)\left(\frac{DT_S}{\sqrt{L\frac{C}{2}}} sin\left(\frac{DT_S}{\sqrt{L\frac{C}{2}}}\right)\right)$	
$b = 2\left(1 - cos\frac{DT_S}{\sqrt{LC}}\right)\left(\frac{DT_S}{\sqrt{LC}} sin\left(\frac{DT_S}{\sqrt{LC}}\right)\right)$	

model). The result of this traditional analysis is shown in Table 8.2. The converter is then analyzed using the modified Volt-Second Balance introduced in [19], as shown in Table 8.3 (i.e., accurate model). In this new method, the results are median values. Using the design numbers in Table 8.1, the results of these two modeling methods are compared in Table 8.4. While the approximated model gives intuitive results, it does not accurately account for the secondary effects of the converter from heavy loading and passive component constraints. More importantly, because of the small ripple approximation by definition, this traditional method confuses average values with median values, and that creates possible errors in calculations and control of the converters. The following sections will provide more detailed explanations and verification with simulation results summarized in Table 8.5 and Fig. 8.3.

8.3.1 Flying Capacitor Voltages

To support heavy loads while maintaining a small footprint for higher power density, large ripples are allowed in the example converter operation. As a result, there is a clear need for proper calculations of the balanced and imbalanced levels. As shown in Fig. 8.2b and 8.2c, for 100A output currents, peak-to-peak voltage ripples of $\sim$9 V are observed on the flying capacitors; however, their magnitudes over the switching period are still centered around the same levels in both cases. It can be observed that in the 4-phase operation, using the traditional measurement of average voltage would give significantly lower capacitor voltages because of the nature of

their duty-cycled waveforms. These lower average capacitor voltage values would represent the average stress on the capacitors but not their accurate levels for voltage conversion calculation.

The converter was simulated in different cases to capture the average and median values of flying capacitor voltages and inductor currents, shown in Fig. 8.2 and summarized in Table 8.5 and Fig. 8.3. It can be seen that average voltages differ significantly from case to case because of load conditions and duty-cycle controlled operations, while the median values are consistent for all the cases. While average values are not acceptable for heavy load conditions, they can be acceptable for light load conditions (Fig. 8.2a) as they are close to the median values with small ripples. The simulated median values are the same as calculated in Table 8.4. This suggests that calculation based on median values is more appropriate and reflective of the hybrid converter operations than the average method, especially in heavy load conditions of interest. Accurate measurement of capacitor voltages using median values would also yield correct balancing regulation in hybrid converters, such as the 4-level Buck converter in [64] or a higher-level FCML converter in [34] or other hybrid converters [15, 16, 49, 66, 99]. For these converters, measurements of average values could lead to inaccurate voltage balance information and possible failures of the balance regulation. One method to acquire the median values is to sample the voltages at half-time through a capacitor's charging or discharging duration. This method will result in very close median measurements in most cases. More accurately, another method can be to take the mean of the two values at the flat portions of the capacitor voltages when the switched capacitor network is inactive.

8.3.2 Inductor Currents

From Fig. 8.2b and 8.2c, it can be seen that the currents of inductor L_2 and L_3 have higher peak and valley values compared with L_1 and L_4 currents. Let us group L_1 and L_4 in inductor group 1 and L_2 and L_3 in group 2. The inductor currents in the same group are the same, but the two groups have different DC average and median levels. However, each inductor still processes an equal amount of charge over the cycle to maintain charge balance in the converter

Table 8.4. Steady state condition from two volt-second balance models

Parameter	Approximated model (|Error|)	Accurate model using median values
V_{C_1}	36V (0.47%)	35.831V
V_{C_2}	24V (0%)	24V
V_{C_3}	12V (1.39%)	12.169V
I_{L_1}	$I_{out}/4$(0.79%)	$I_{out}\times 0.252$
I_{L_2}	$I_{out}/4$(2.88%)	$I_{out}\times 0.243$
I_{L_3}	$I_{out}/4$(2.88%)	$I_{out}\times 0.243$
I_{L_4}	$I_{out}/4$(0.79%)	$I_{out}\times 0.252$
V_{out}	2.4V (4%)	2.5V
Error percentages provided in brackets are calculated based on the median measurements/calculations. Median values are the same from calculations and measurements.		

operation. A close inspection reveals that during the charging intervals, L_2 and L_3 currents are more curvy compared to L_1 and L_4 currents. This is more apparent in Figs. 8.2b and 8.2c. This extra curvature comes from the fact that L_2 and L_3 see a smaller capacitance which is a series combination of C_1 and C_2 for L_2, or C_2 and C_3 for L_3. Using the same capacitance C for all flying capacitors (Table 8.1), the series capacitance is $C/2$. On the contrary, inductor L_1 and L_4 sees the same capacitance C from C_1 and C_3, respectively, when they get charged. Therefore, the currents of L_2 and L_3 are curvier while all inductors still carry the same amount of charge during the charging intervals. Even though the DC average levels of the inductors, L_2, and L_3 are slightly lower, their extra curvature during the charging interval allows them to have the same amount of charge under that curve. Note that the inductor discharge rate is the same for all inductors because they all block the same output voltage during the discharging intervals. Since these discharging intervals are the same for all inductors, the inductors have the same current ripples, although their DC and median levels are different. The modified Volt-Second balance method described in Table 8.3 is used to calculate the median currents shown in Table 8.4 which perfectly match with the measured median values. The DC or average levels of the inductor currents can be calculated from the median currents using, $I_{av} = [bD + (1-D)]\, I_{median}$ [19]. The consistency in the method of using median values also validates its accuracy in the inductor

Table 8.5. Measured average and median values from simulation

	2-phase heavy load operation		4-phase heavy load operation		4-phase light load operation	
Parameter	Average (|Error|)	Median	Average (|Error|)	Median	Average (|Error|)	Median
V_{C_1}	35.83V (0%)	35.83V	33.66V (6.05%)	35.83V	35.62V (0.60%)	35.83V
V_{C_2}	24V (0%)	24V	21.83V (9.04%)	24V	23.78V (0.90%)	24V
V_{C_3}	12.17V (0%)	12.17V	10V (17.84%)	12.17V	11.95V (1.79%)	12.17V
I_{L_1}	25.35A (0.69%)	25.18A	25.35A (0.66%)	25.18A	2.54A (0.68%)	2.52A
I_{L_2}	24.65A (1.44%)	24.3A	24.65A (1.44%)	24.3A	2.46A (1.44%)	2.43A
I_{L_3}	24.65A (1.44%)	24.3A	24.65A (1.44%)	24.3A	2.47A (1.44%)	2.43A
I_{L_4}	25.35A (0.69%)	25.18A	25.35A (0.69%)	25.18A	2.54A (0.679%)	2.52A
V_{out}	2.50V (0%)	2.5V	2.5V (0%)	2.5V	2.5V (0%)	2.5V
Error percentage provided in brackets are calculated based on the median measurements/calculations.						

current calculations as they match exactly with the simulation results in Table 8.5 and Fig. 8.3 for all operating conditions.

8.3.3 Output Voltage

The MIH converter operation is similar to a multi-phase Buck converter in terms of current sharing in the inductors and output voltage ripple. Therefore, the 4-phase operation has smaller output voltage ripples compared with the 2-phase operation, as expected and clearly visible in Figs. 8.2b and 8.2c. Interestingly, the DC level of the output voltage is at 2.5V, which is 100mV higher than 2.4V from the traditional approximated model in Tables 8.2 and 8.4. This is because the voltage ripples in the finite flying capacitors collectively make the charging voltages V_x for the inductors higher than in the simple approximated model, giving a higher output voltage, as shown in Fig. 8.2. The modified volt-second balance method using median values accounts for the actual voltage and current ripples to accurately calculate the output voltage as reported in Table 8.4 and verified with the simulation results in Table 8.5 and Fig. 8.3.

8.4 Chapter Summary

This chapter discusses the differences, advantages, and accuracy of modeling hybrid converters using the median values in calculating voltages and currents compared with using average values. The modified volt-second balance method proves to have accurate calculations of median values verified in simulations for both capacitor voltages and inductor currents, while

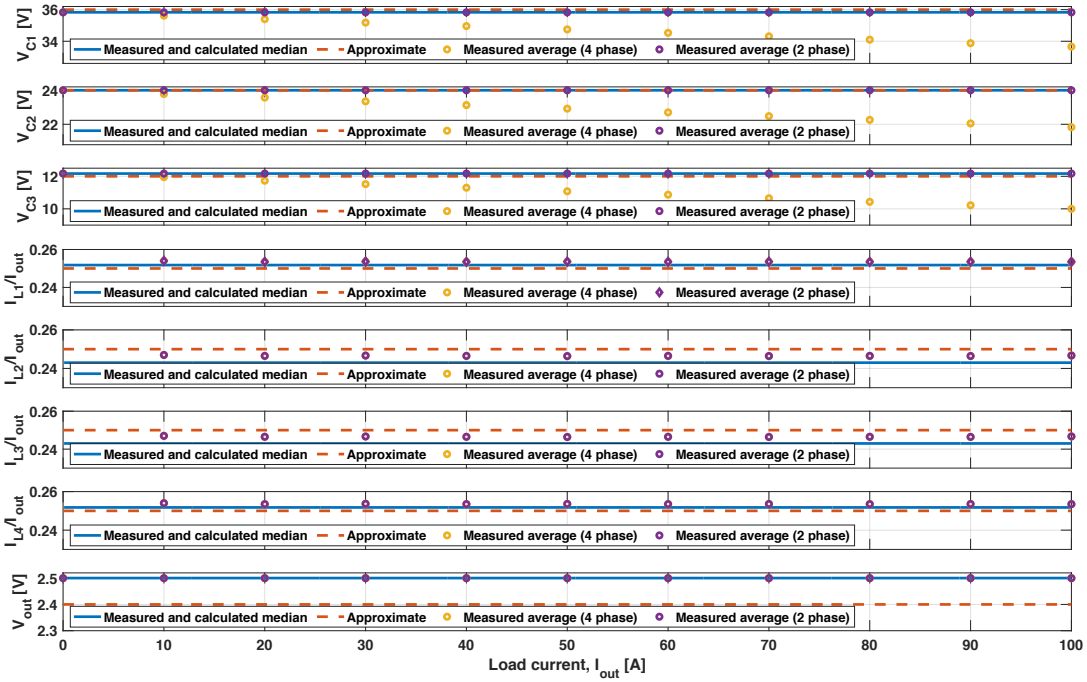


Figure 8.3. Comparison among median, approximate, and measured average levels from simulation

the traditional volt-second balance method suffers from inaccuracy because of simple small ripple approximations. The median values are also consistent in different operating points of the converter example and represent its operation nature. While the average values can be used for light load conditions, their variations and dependence on heavy loads and operation modes would lead to possible errors and failures in balance operation and control of hybrid converters in different load scenarios.

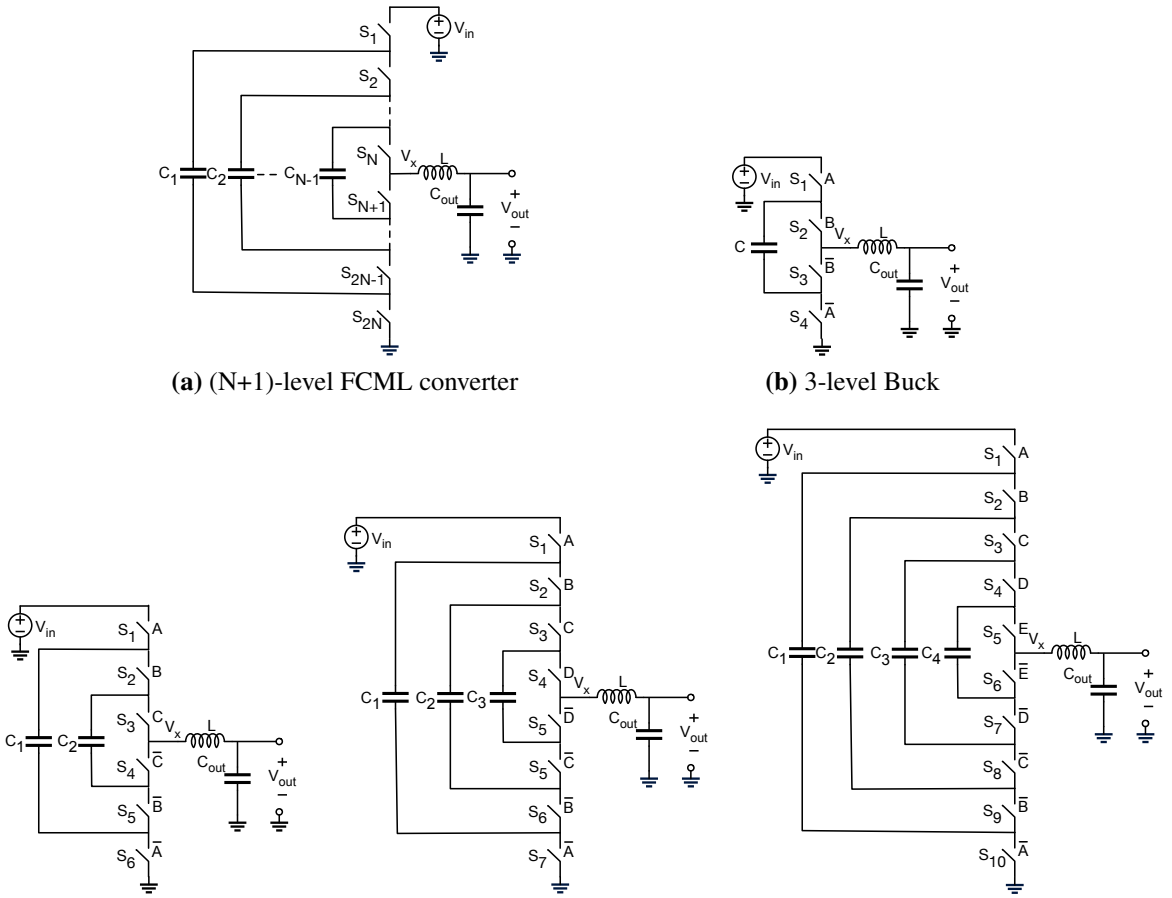
Chapter 8, in full, is a reprint of the material as it appears in "An Accurate Approach to Calculate and Measure Capacitor Voltage and Inductor Current Levels in Hybrid Converters," in 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021, pp. 1-5 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 9

Analysis of Capacitor Voltage Imbalance in Hybrid Converters and Inherently Balanced Operation Using Symmetric Architecture

9.1 Introduction

Switched-capacitor (SC)-based converters with added inductors for partial or full soft-charging of flying capacitors, simply known as hybrid converters, have drawn a lot of recent interest from industry and academia because of their benefits in optimizing both passive components, inductors, and capacitors for higher performance operations [48, 64]. Voltage balancing of flying capacitors in Flying Capacitor Multi-Level (FCML) converters is a well-known challenge that attracts a lot of effort in the research community. While effective solutions can be relatively diverse [34, 100], it is important to understand the original mechanism that causes this problem. Using two different approaches, Fourier-based Harmonic analysis in [101] and state-space analysis in [97], it has been shown that capacitor voltages in an (N+1)-level FCML converter (N is the number of flying capacitors), shown in Fig. 9.1a, becomes exponentially unbalanced at some nominal conversion ratios. Additional operating states were introduced in [102] to overcome the problems in a 5-level FCML converter. Analytical efforts to explain the problem with practical timing mismatches in FCML converters were also carried out in [19, 98]. The work in [98]



(a) (N+1)-level FCML converter **(b)** 3-level Buck

(c) 4-level FCML Converter **(d)** 5-level FCML Converter **(e)** 6-level FCML Converter

Figure 9.1. Schematics of several FCML converters

numerically shows that the balancing performance of odd-level (N is even) FCML converters are more sensitive than that of even-level (N is odd) ones. This analysis is also aligned with the one reported in [103] for identifying the difference between odd- and even-level converters. In [19], the sensitivity of the flying capacitor voltage was calculated for a 3-level Buck and a 4-level Series Capacitor Buck (SCB) converter.

The analysis in this chapter focuses on the converters with output voltages V_{out} satisfying $V_{out} < \frac{V_{in}}{N}$, where V_{in} is the input voltage, and develops a general method to identify the balancing issue in hybrid converters with fundamentally different structures. The chapter starts with deriving the voltage-charge relationship, which is later applied to explain the differences in the balancing performances of different hybrid converters. A modified symmetric architecture is

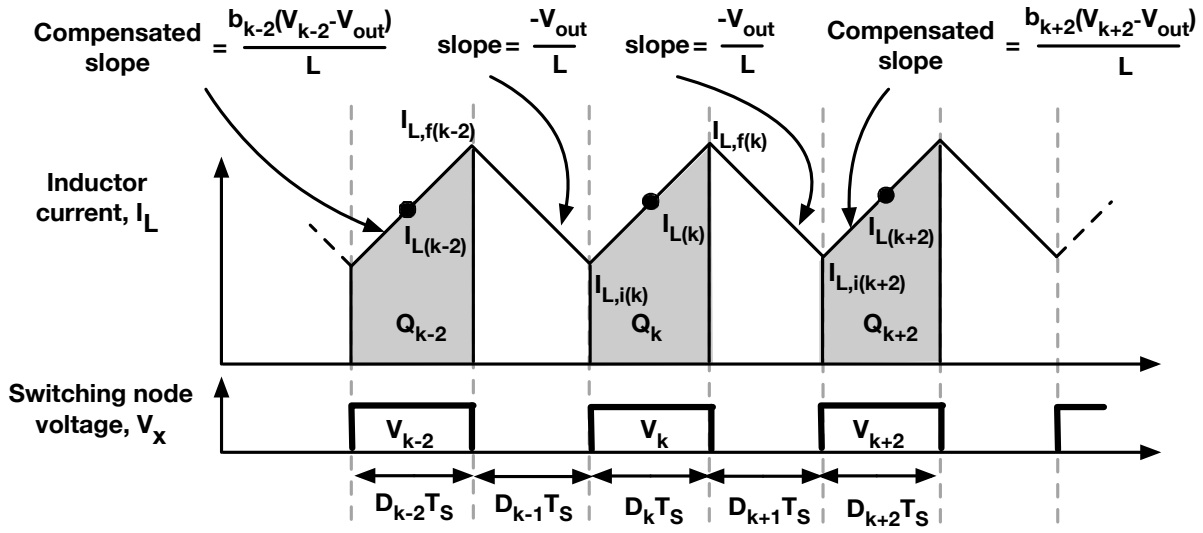


Figure 9.2. Inductor current in an FCML converter with PWM operation

also proposed to achieve inherent balance in popular FCML converters.

9.2 Voltage-Charge Relationship

In order to accurately determine the capacitor voltages to analyze a possible voltage imbalance scenario, it is critical to monitor the switching node voltages that directly reflect flying capacitor voltages as well as inductor currents. For this goal, we first develop a relationship between the charge flow and switching node voltages in a general FCML converter shown in Fig. 9.1a. This relationship can be constructed by the inductor current ripples that actually carry the information of the switching node voltages, the output voltage, as well as the charges passing through each capacitor.

Figure 9.2 depicts a general waveform of the inductor current of an FCML converter in

Table 9.1. V_x of 6-level FCML converter

States	1	3	5	7	9	2,4,6,8,10
V_x	V_{in}-V_{C_1}	V_{C_1}-V_{C_2}	V_{C_2}-V_{C_3}	V_{C_3}-V_{C_4}	V_{C_4}	0

Table 9.2. V_x of 5-level FCML converter

States	1	3	5	7	2,4,6,8
V_x	V_{in}-V_{C_1}	V_{C_1}-V_{C_2}	V_{C_2}-V_{C_3}	V_{C_3}	0

Fig. 9.1a, operating in the inductive region and $V_{out} < \frac{V_{in}}{N}$. $D_{k-2}T_S, D_kT_S$, and $D_{k+2}T_S$ represent three consecutive charging intervals, while $D_{k-1}T_S$ and $D_{k+1}T_S$ are the intermediate freewheeling intervals when the inductor is connected between ground and V_{out}. Note that in a 3-level Buck converter (Fig. 9.1b), a special FCML converter, $D_{k-2}T_S$ and $D_{k+2}T_S$ denote the same interval of two consecutive switching periods.

Assume Q_{k-2}, Q_k, and Q_{k+2} are the charges through the corresponding voltages at the switching node V_x (Fig. 9.1a), V_{k-2}, V_k, and V_{k+2} during the timing intervals $D_{k-2}T_S$, D_kT_S, and $D_{k+2}T_S$, respectively. Using the median currents and discharging coefficients, b_{k-2}, b_k, and b_{k+2} in Fig. 9.2 for the Voltage-second balance and charge balance, a relation among these charges and the corresponding switch node voltages, V_{k-2} and V_{k+2}, can be found:

$$\begin{aligned} &(V_{k-2} - V_{out}) \frac{b_{k-2}D_{k-2}T_S}{L} - (V_{k+2} - V_{out}) \frac{b_{k+2}D_{k+2}T_S}{L} \\ &= \frac{2}{T_S} \left\{ \frac{2Q_k}{b_kD_k} - \left(\frac{Q_{k-2}}{b_{k-2}D_{k-2}} + \frac{Q_{k+2}}{b_{k+2}D_{k+2}} \right) \right\} + 2V_{out} (D_{k-1} - D_{k+1}) \frac{T_S}{L} \end{aligned} \tag{9.1}$$

As shown in [19], while b_{k-2}, b_k and b_{k+2} are very close to 1 in most practical cases, their actual values are important for modeling accuracy. The relationship described by (9.1), which was not established in [19], is general for all step-down $V_{out} < \frac{V_{in}}{N}$ hybrid converters with the inductor(s) at the output and freewheeling to the ground, regardless of timing mismatches, voltage imbalances, or other non-idealities in the converter operations. The derivation of eqn. 9.1 is included in Appendix E.

Analyzing this relationship in an ideal (no mismatch) case or in case of small mismatches among parameters of the same type that satisfy the following four conditions: (1) $b_{k-2} \to b_k \to b_{k+2}$, (2) $D_{k-2} \to D_k \to D_{k+2}$, (3) $D_{k-1} \to D_{k+1}$, and (4) $Q_{k-2} \to Q_k \to Q_{k+2}$ (the arrow $\to$ means "approaches" or "approximately equals"), one can find that the two alternate charging voltages converge:

$$V_{k-2} \to V_{k+2} \tag{9.2}$$

This corollary is true for any alternate charging voltages at V_x regardless of their positions in the cycle or across two switching cycles of the converter. While the alternate charging voltages converge, the two consecutive charging voltages at V_x node, V_{k-2} and V_k, or V_k and V_{k+2}, can diverge and become significantly different along with capacitor voltage imbalances because of load conditions and various non-idealities, such as input impedance, ESR, parasitic resistance, and timing mismatches in the circuit. The exact amount of divergence can only be calculated if all these parameters are known. The two consecutive voltages only converge in the case of balanced operation. In other words, the V_x swing in the FCML converter essentially has one of the two voltage levels in the current charging phases of the inductor. These two voltage levels are at two consecutive charging phases. They diverge in imbalanced operations but converge when balanced. The corollary can be used to understand the voltage imbalance and inductor current fluctuations in FCML converters as well as other hybrid converters.

9.3 Application to Multi-Level Converters

Odd- and even-level FCML converters show significantly different balancing performances. In a traditional architecture and operation, an even-level (odd-level) FCML converter has an odd (even) number of flying capacitors and an odd (even) number of inductor charging intervals. In our analysis, we found that the balancing performance difference resulted directly from the number of inductor charging intervals rather than the capacitor numbers or the switched capacitor (SC) voltage division. Sections 9.3.1 and 9.3.2 explain this difference using the voltage-charge relationship and its corollary.

9.3.1 Inductor Current with Odd Number of Charging Intervals

As an example, Table 9.1 lists the switching node voltages at V_x of a 6-level (N=5) FCML converter (Fig. 9.1e). There are 10 state intervals, 5 of which (1,3,5,7 and 9) create the rising slopes in the inductor current while it is connected to the flying capacitors, while it freewheels

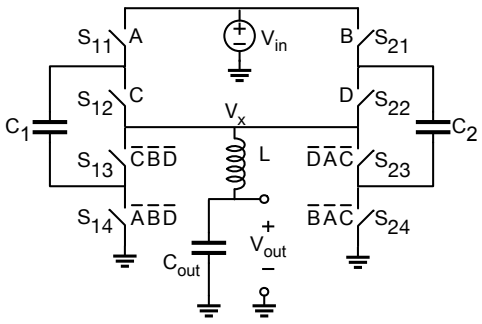
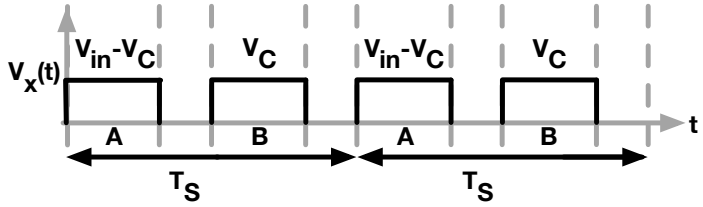


Figure 9.3. Symmetric 3-level Buck converter

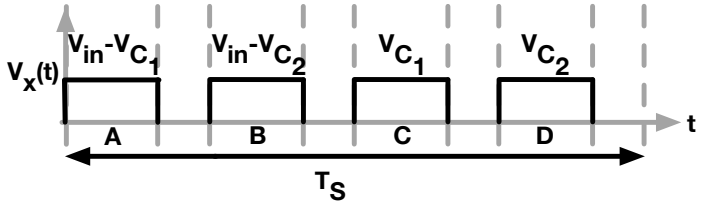
from the ground to V_{out} in the remaining states. As analytically proved in the corollary above, there are two sets of voltages at V_x. Switching node voltages at V_x during alternate charging intervals 1, 5, and 9 converge to the same value, $V_{in} - V_{C_1} = V_{C_2} - V_{C_3} = V_{C_4}$. Similarly, V_x voltages during interval 3 and 7 also converge, $V_{C_1} - V_{C_2} = V_{C_3} - V_{C_4}$. More interestingly, interval 7 of the current switching cycle and interval 1 of the next cycle are also one charging interval (interval 9) apart from each other. From the volt-charge relationship and its corollary above, these two charging voltages also converge, $V_{C_3} - V_{C_4} = V_{in} - V_{C_1}$. As a result, all the voltages of V_x during the inductor charging intervals converge to the same value, making a balanced operation. This characteristic is true for all even-level FCML converter (N is odd) that ensures inherently balanced operations, as they have an odd number of inductor charging intervals. On the contrary, the same analysis gives a different result for odd-level FCML converters (N is even).

9.3.2 Inductor Current with Even Number of Charging Intervals

Table 9.2 shows the switching node voltages at V_x of a 5-level (N=4) FCML converter (Fig. 9.1d). There are 4 charging intervals (1,3,5,7) and 4 discharging intervals (2,4,6,8) for the inductor current. Switching node voltages at V_x during intervals 1 and 5 make one converging group, $V_{in} - V_{C_1} = V_{C_2} - V_{C_3}$, where those of intervals 3 and 7 make another, $V_{C_1} - V_{C_2} = V_{C_3}$. Note that, unlike even-level converters, these two sets of charging voltages neither exchange in the next cycle nor converge. Therefore, when timing mismatches occur, these two sets of voltages can diverge and cause voltage imbalance in flying capacitors as well as fluctuations in the inductor current. The same characteristic is present in all other odd-level members (N



(a) 3-level Buck Converter



(b) Symmetric 3-level Buck Converter

Figure 9.4. Switching node voltages

is even) of the FCML converters that becomes a challenge in fully utilizing the benefits of the FCML architecture.

9.3.3 Balancing Performance of Other Conventional Hybrid Converters with $V_{out} < \frac{V_in}{N}$

The results using the Voltage-Charge relationship and its corollary so far align with the results found in [98, 103] for the imbalance performance of odd and even level FCML converters, but the analysis provides a more intuitive approach to understanding the imbalance mechanism in other hybrid converters. The key is in the number of inductor current charging phases in a switching cycle.

Converters having inductors with an odd number of charging intervals in a switching period, such as even-level FCML converters [64], 6-phase 6-level Dual Inductor Hybrid converters [49], or series capacitor Buck converter [52], have naturally balanced operations. The work in [15] demonstrated a hybrid converter with 7 (odd) SC levels and 1 charging interval for each inductor, exhibiting no capacitor voltage imbalance. As another example, the hybrid converter in [49] provides $\frac{1}{6}$ division (even-level) to the switching node voltages with each

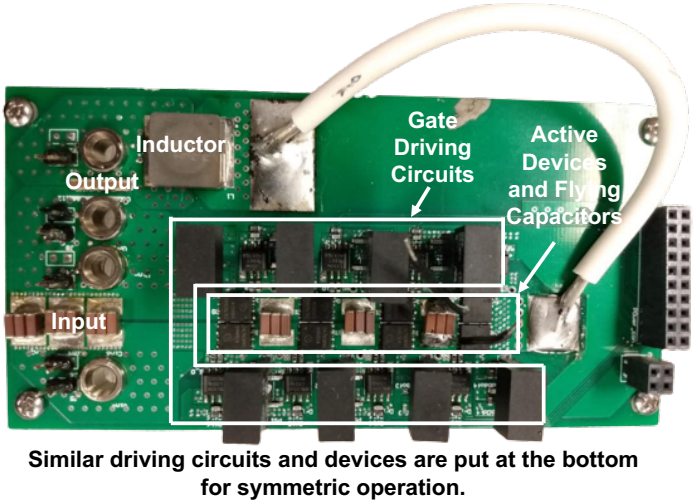


Figure 9.5. Implementation of 3-level, 4-level, and symmetric 3-level Buck converters in a single PCB

inductor having 3 charging intervals each fundamental switching period, also exhibiting naturally balanced operations.

On the contrary, an even number of inductor charging phases causes odd-level FCML converter operation to be highly susceptible to small timing mismatches and imbalanced capacitor voltages. All traditional odd-level FCML converters, including the 3-level Buck converter, fall into this category. 2-level series-capacitor Buck converter [52] with a partially coupled inductor also has an even number of inductor charging phases if modeled with a transformer, and inductor [104] and hence, it is also susceptible to voltage imbalance. Note that some other factors, for instance, parasitic resistance and/or hard-charging operation between flying capacitors in higher-level Hybrid Dickson converters [36] or 4-phase 4-level dual inductor hybrid converters [74], can inadvertently desensitize and minimize imbalance issues at the cost of degraded efficiency.

9.4 Multi-phase Symmetric Converter Architecture for Voltage Balancing

Inspired by the analysis above, we propose a new symmetric architecture that can provide naturally balanced operation even with an even number of inductor charging intervals, particularly applicable to balance odd-level FCML converter operations. Figure 9.3 shows a symmetric 3-level converter that has two symmetric SC halves tied to a common switching node with one inductor. This converter is operated with four 90°-phased-shifted PWM signals, A, B, C, and D, and derived signals ($\overline{\text{C}}\,\overline{\text{B}}\,\overline{\text{D}}$), ($\overline{\text{A}}\,\overline{\text{B}}\,\overline{\text{D}}$), ($\overline{\text{D}}\,\overline{\text{A}}\,\overline{\text{C}}$), and ($\overline{\text{B}}\,\overline{\text{A}}\,\overline{\text{C}}$). This operation also ensures that there is no charge sharing between the two SC halves.

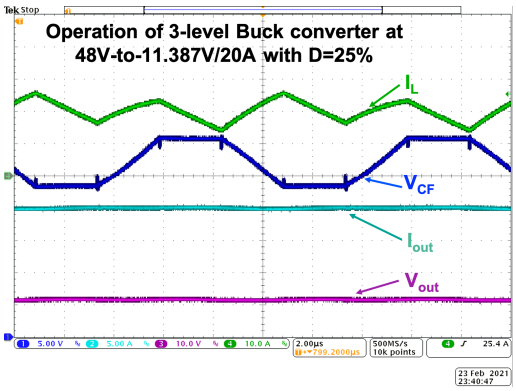
Figures 9.4a and 9.4b show the switching node voltages of a conventional 3-level Buck and a symmetric 3-level Buck converter. In the conventional 3-level Buck converter (Fig. 9.1b), alternate switching node voltages are generated in the same way every cycle. Therefore, V_x has two levels, $V_{in}-V_C$ and V_C, that do not naturally converge, as proved by (9.1) and (9.2). On the contrary, for the symmetric 3-level Buck converter (Fig. 9.3), the interleaved operation forces $V_{in}-V_{C1}$ and V_{C1} ($V_{in}-V_{C2}$ and V_{C2}) to converge as they are the alternate switching node voltages. As the result, the flying capacitors have half of the input voltage, $V_{C1}=V_{C2}={}^{V_{in}}/_{2}$, ensuring an inherently balanced operation. Besides generating the right PWM signals, no separate control is required to tackle voltage imbalance. Moreover, the inductor in this converter operates with $4\times F_S$, where F_S is the fundamental switching frequency of the converter, whereas a traditional 3-level Buck converter's inductor has twice the fundamental frequency. This enables the choice of a much smaller inductor. Similar symmetric SC structures can be applied to higher odd-level FCML converters to solve a similar voltage imbalance problem.

9.5 Experimental Verifications

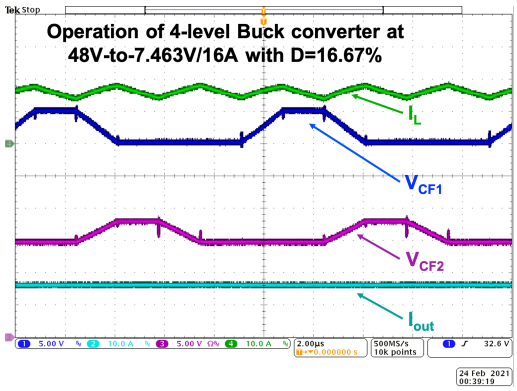
To verify the Voltage-Charge relationship and its analytical results above, a 3-level Buck and a 4-level Buck converter have been implemented to represent odd-level and even-level

members of FCML converters that have an even and an odd number of inductor charging intervals shown in Fig. 9.1b and 9.1c, respectively. A symmetric 3-level Buck converter has also been built to verify the proposed inherent balancing. All these three converter prototypes have been built on the printed circuit board, shown in Fig. 9.5, using the same active and passive components and have the same input voltage of 48V. Re-configurations for different converters in experiments only require different PWM control signals for different active devices. No duty cycle adjustment has been done for any of the converters for the demonstration of good or poor mismatch.

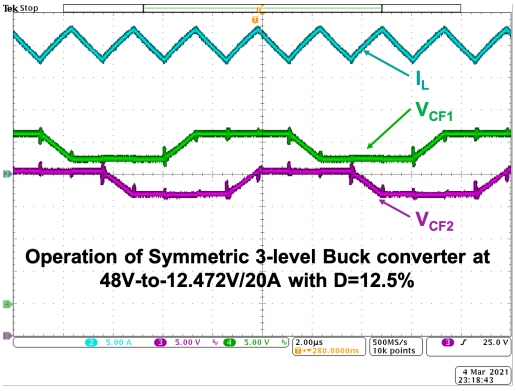
The inductor current and flying capacitor voltage waveforms of these three converters are shown in Fig. 9.6. In Fig. 9.6a, the 3-level Buck converter exhibits a poor balancing performance, particularly visible in its inductor current. In fact, its balancing problem is also



(a) 3-level Buck converter

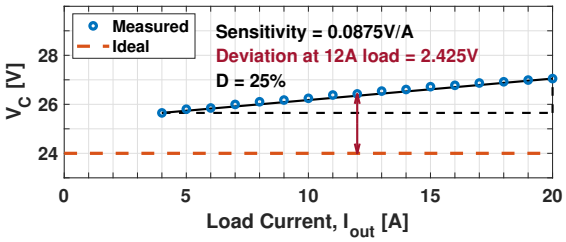


(b) 4-level Buck converter

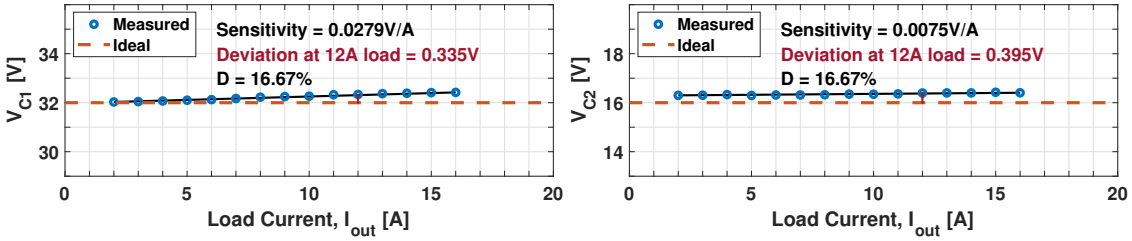


(c) Symmetric 3-level Buck converter

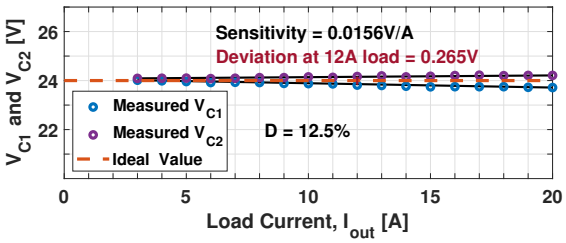
Figure 9.6. Measured waveforms of three hybrid converter prototypes



(a) 3-level Buck converter



(b) 4-level Buck converter



(c) Symmetric 3-level Buck converter

Figure 9.7. Measured median voltages of flying capacitors of hybrid converter prototypes with the same input voltages in Fig. 9.6

corroborated by its median capacitor voltage shown in Fig. 9.7a, which deviates from the ideal value of 24V and quickly deteriorates with higher currents. Figures 9.6b and 9.6c show the waveforms of the 4-level Buck and symmetric 3-level Buck converters, respectively, proving their balanced operations with no apparent visual fluctuation in the inductor currents. Their median capacitor voltages in Figs. 9.7b and 9.7c also reveal better-balanced operations with $\sim$10X smaller deviation from the ideal values and up to $\sim$10X less variation across the load range.

9.6 Chapter Summary

A fundamental volt-charge relationship has been devised in this chapter to provide a direct, intuitive analysis of flying capacitor imbalance in hybrid converters with $V_{out} < \frac{V_{in}}{N}$[1]. The analysis in the chapter shows that the reason for different balancing performances comes from the number of inductor charging intervals, even or odd. This approach simplifies identifying balanced or imbalanced characteristics in traditional hybrid converters to only counting the number of inductor charging intervals within a fundamental switching period. Experimental results for verification of the analysis were achieved with 3-level and 4-level FCML converters. A new symmetric architecture has also been proposed, implemented, and verified for a 3-level Buck converter (representing traditional odd-level FCML converters) to show that hybrid converters with an even number of inductor charging intervals can be made naturally balanced with appropriate architecture and operation. The analysis and method for identifying imbalanced converters and the proposed symmetric architecture to achieve naturally balanced operations in odd-level FCML converters can be extended to other hybrid converters.

Chapter 9, in full, is a reprint of the material as it appears in "Analysis of Capacitor Voltage Imbalance in Hybrid Converters and Inherently Balanced Operation Using Symmetric Architecture," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 3, no. 4, pp. 1205-1209, Oct. 2022 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

[1] A similar analysis for all V_{out} has also been performed and included in Appendix F. It can be shown that the conclusions in this chapter about member FCML converters being balanced or not balanced are true for all ranges of V_{out}.

Chapter 10

General Analysis of Flying Capacitor Multi-Level Converters For Balancing Issues

10.1 Introduction

Very few publications investigated the origin of imbalance in flying capacitor multi-level (FCML) converters [19, 97, 98, 101]. In [101], a harmonic-based analysis has been followed and shown that at some particular conversion ratios, FCML converters have balancing issues. [97] reached the same conclusion using state space analysis. In [19, 98], the effect of non-ideal timing on the flying capacitor voltages is analyzed.

This work is extended from [19, 21] and investigates the FCML converters with volt-second and volt-current relationships. This analysis provides the direct expressions of the flying capacitor median voltages in terms of the timing intervals. It can be revealed from the analysis that the flying capacitor voltages are dependent on the loads. For even-level converters, the dependency is relatively small and only significantly visible with very high load current or highly mismatched timing intervals. The converter becomes a current source for odd-level converters, and the flying capacitor voltages depend on the output voltage. Section 10.2 includes the method for general analysis. Section 10.3 and 10.4 discusses even and odd converters, respectively. Section 10.5 summarizes and concludes the chapter.

10.2 Analysis of FCML Converters

FCML converters and many hybrid converters have been derived from switched capacitor (SC) based converters by adding inductors for soft-charging purposes and, thereby, adding low-loss regulative operation. In most cases, the flying capacitor voltages in hybrid converters coincide with their parent converter. But, in reality, capacitor voltages and inductor current(s) modulate each other and charging or discharging interval timings modulate both of them. In some cases, this results in capacitor voltage imbalance from the expected values. In this subsection, a general method to derive the steady-state capacitor voltages has been provided for FCML converters.

Assuming $Q_{k-2} = Q_k = Q_{k+2} = Q$ and $V_{in}Q = V_{out}I_{out}T_S$, a voltage-current relationship can be derived from Fig. 9.2 as below:

$$\begin{aligned} &b_{k-2}D_{k-2}\left(V_{k-2} - V_{out}\right) - b_{k+2}D_{k+2}\left(V_{k+2} - V_{out}\right) \\ &= \frac{2V_{out}I_{out}}{V_{in}}\frac{L}{T_S}\left\{\frac{2}{b_kD_k} - \left(\frac{1}{b_{k-2}D_{k-2}} + \frac{1}{b_{k+2}D_{k+2}}\right)\right\} + 2V_{out}\left(D_{k-1} - D_{k+1}\right) \end{aligned} \tag{10.1}$$

For a (N+1)-level FCML converter shown in Fig. 9.1a, N such equations can be derived for $k = 1,3,5,...,2N-1$ writing $V_k = V_{C_{k-1}} - V_{C_k}$. For, $k = 1$, $V_1 = V_{in} - V_{C_1}$ and $k = N$, $V_N = V_{C_k}$. Besides these equations, a volt-second balance equation can also be derived from the inductor current,

$$\sum_{k=1,3,5,...}^{2N-1} b_kD_k\left(V_k - V_{out}\right) = \left(\sum_{k=2,4,6,...}^{2N} D_k\right)V_{out} \tag{10.2}$$

Using the set of eqns. 10.1 and 10.2, it is possible to determine the steady state voltages and currents of any hybrid converters. Definition of discharging coefficients, b can be found in [19] In brief, steady state analysis reveals that all ideal odd level FCML converters with timing mismatches operates as ideal current source if no flying capacitor voltage is railed out.

For any (N+1)-level odd converter with timing mismatches, the output current can be derived as,

$$I_{out} = \frac{\frac{V_{in}T_S}{2L}\left(-\sum_{m=1}^{N/2}\left((-1)^m D_{2m}\right)\right)}{-\sum_{m=1}^{N/2}\frac{(-1)^m}{b_{2m-1}D_{2m-1}}} \tag{10.3}$$

This analysis directly matches the results derived earlier for the 3-level Buck converter in [19].

Similar steady-state analysis can also be done for all even-level converters. However, they always behave as voltage source converters. Output voltage for an even level (N+1) FCML converter can be derived as,

$$V_{out} = \frac{V_{in}}{N - \sum_{k=1,3,5,\ldots}^{2N-1}\frac{\left[\sum_{m=k+3,k+5,\ldots}^{k+2N-1}\left\{-(-1)^{\frac{m-k-1}{2}}\left(D_{mod(m,2N)}\right)\right\} \quad -D_{k+1}\right]}{b_k D_k}} \tag{10.4}$$

Solving eqns. 10.1 and 10.2, flying capacitor voltages for any FCML converter can also be derived. Table 10.1 and 10.2 shows the flying capacitor voltages in the steady state of a 3-level (shown in Fig. 9.1b) and 4-level converter (shown in Fig. 9.1c) as examples. For even-level converters, the capacitor voltages and output voltage can be generalized in Table 10.3. In a similar way, the flying capacitor voltages of odd-level converters can also be derived. However, although the author has analyzed multiple odd-level (3, 5, 7, and 9) converters, there was no apparent pattern in those complex expressions. For simplicity of the discussion, the expressions are not added in this dissertation.

In brief, flying capacitor voltages can be modeled as $V_{C_k} = xV_{in} + yF$, where F is a function of V_{out} for odd-level converters and I_{out} for even level converters. For ideal timing, $x \to {}^{N-k}/_{N}$ and $y \to 0$. Intended operation of the FCML converters are expected to be with ideal timing; hence, $V_{C_k} = \frac{N-k}{N}V_{in}$ holds most of the time. The following sections will discuss the behavior of odd and even level converters with non-ideal timing.

Table 10.1. 3-Level Buck converter steady-state solutions

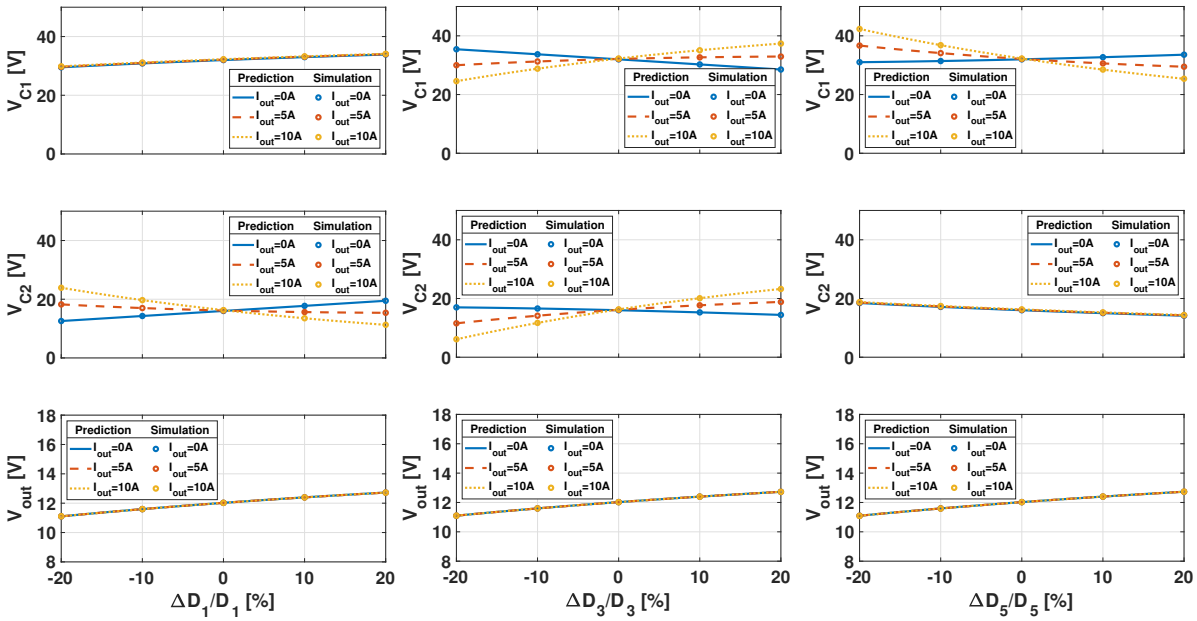
Ideal Timing: Voltage source behavior	Non-ideal Timing: Current source behavior
$V_{out} = \frac{V_{in}}{2+\frac{(1-2D)}{bD}}$	$I_{out} = \frac{\frac{V_{in}T_S}{2L}(D_2-D_4)}{\frac{1}{b_{(1)}D_1}-\frac{1}{b_{(3)}D_3}}$
$V_C = \frac{1}{b+a}V_{in} = \frac{1}{2}V_{in}$	$V_C = \frac{\left(b_{(1)}D_1+b_{(3)}D_3+D_2+D_4\right)V_{out}-b_{(1)}D_1V_{in}}{b_{(3)}D_3-b_{(1)}D_1}$

Table 10.2. Steady state solution of a 4-level converter

Parameter	Expression
V_{C_1}	$\frac{V_{in}\left[2+\frac{2LI_{out}}{T_SV_{in}}\left(\frac{\frac{1}{b_{(5)}D_5}-\frac{1}{b_{(1)}D_1}}{b_{S(3)}D_3}+\frac{\frac{1}{b_{(1)}D_1}-\frac{1}{b_{S(3)}D_3}}{b_{(5)}D_5}\right)-\left(\frac{D_6-D_2-D_4}{b_{S(3)}D_3}+\frac{D_2-D_4-D_6}{b_{(5)}D_5}\right)\right]}{3-\left\{\frac{D_4-D_6-D_2}{b_{(1)}D_1}+\frac{D_6-D_2-D_4}{b_{S(3)}D_3}+\frac{D_2-D_4-D_6}{b_{(5)}D_5}\right\}}$
V_{C_2}	$\frac{V_{in}\left[1+\frac{2LI_{out}}{T_SV_{in}}\frac{\frac{1}{b_{(1)}D_1}-\frac{1}{b_{S(3)}D_3}}{b_{(5)}D_5}-\frac{D_2-D_4-D_6}{b_{(5)}D_5}\right]}{3-\left\{\frac{D_4-D_6-D_2}{b_{(1)}D_1}+\frac{D_6-D_2-D_4}{b_{S(3)}D_3}+\frac{D_2-D_4-D_6}{b_{(5)}D_5}\right\}}$
V_{out}	$\frac{V_{in}}{3-\left\{\frac{D_4-D_6-D_2}{b_{(1)}D_1}+\frac{D_6-D_2-D_4}{b_{S(3)}D_3}+\frac{D_2-D_4-D_6}{b_{(5)}D_5}\right\}}$

Table 10.3. Steady state solution of even level FCML converters

Parameter	Expression
V_{C_n}	$V_{in}\frac{\left[\begin{array}{c}(N-n)\\ +\frac{2I_{out}}{V_{in}}\frac{L}{T_S}\sum\limits_{k=2n+1,2n+3,2n+5,\ldots}^{2N-1}\left[\frac{\sum\limits_{m=k+2,k+4,\ldots}^{k+2N-2}\left\{-(-1)^{\frac{m-k}{2}}\frac{1}{b_mD_m}\right\}}{b_kD_k}\right]-\\ \sum\limits_{k=2n+1,2n+3,2n+5,\ldots}^{2N-1}\left[\frac{\sum\limits_{m=k+3,k+5,\ldots}^{k+2N-1}\left\{-(-1)^{\frac{m-k-1}{2}}\left(D_{mod(m,2N)}\right)\right\}-D_{k+1}}{b_kD_k}\right]\end{array}\right]}{N-\sum\limits_{k=1,3,5,\ldots}^{2N-1}\left[\frac{\sum\limits_{m=k+3,k+5,\ldots}^{k+2N-1}\left\{-(-1)^{\frac{m-k-1}{2}}\left(D_{mod(m,2N)}\right)\right\}-D_{k+1}}{b_kD_k}\right]}$
$V_{C_{out}}$	$\frac{V_{in}}{N-\sum\limits_{k=1,3,5,\ldots}^{2N-1}\left[\frac{\sum\limits_{m=k+3,k+5,\ldots}^{k+2N-1}\left\{-(-1)^{\frac{m-k-1}{2}}\left(D_{mod(m,2N)}\right)\right\}-D_{k+1}}{b_kD_k}\right]}$

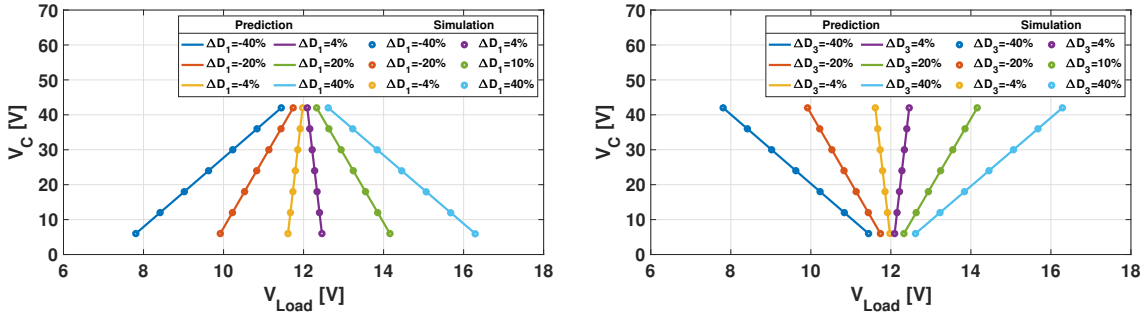


(a) D_1 Variation **(b)** D_3 Variation **(c)** D_5 Variation

Figure 10.1. Predicted and simulated flying capacitor voltage variations for 4LB converter (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$, $D_{1,3,5}(ideal) = 0.25$ and $D_{2,4,6}(ideal) = 0.08\overline{3}$)

10.3 Discussion on Even Level FCML Converters with Non-Ideal Timing

Unlike odd-level converters, even converters stay as voltage sources with non-ideal timing. However, the capacitor voltages depend on different timing intervals and output currents. The best way to model the flying capacitor voltages is with $V_{C_k} = xV_{in} + yI_{out}$, where x and y values are still close to $\frac{N-k}{N}$ and 0 respectively, but their magnitudes can deviate significantly dependent on the amount of the timing mismatches. As a result, flying capacitor voltages can move from their expected position with the output current changes. However, in a typical operation, the timing mismatches are insignificant, so only a small amount of deviation is expected, which does not create any problem in circuit operation. For example, the flying capacitor voltages of a 4-level converter are plotted along with the output voltage with small to moderate amounts of timing mismatches in Fig. 10.1. It can be observed that the flying capacitor voltages do deviate



(a) D_1 Variation with load voltage at the output ($V_{Load} = I_{out}R_{load}$)

(b) D_3 Variation with load voltage at the output ($V_{Load} = I_{out}R_{load}$)

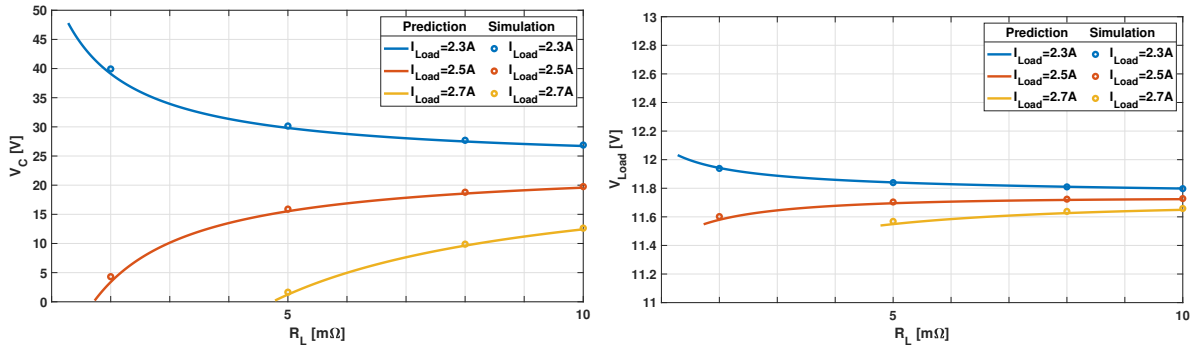
Figure 10.2. Predicted and simulated flying capacitor voltage variations versus load voltage for 3LB converter (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$ and $D_{1-4}(ideal) = 0.25$)

in response to the load current variation with a small dependency.

10.4 Discussion on Odd Level FCML Converters with Non-Ideal Timing

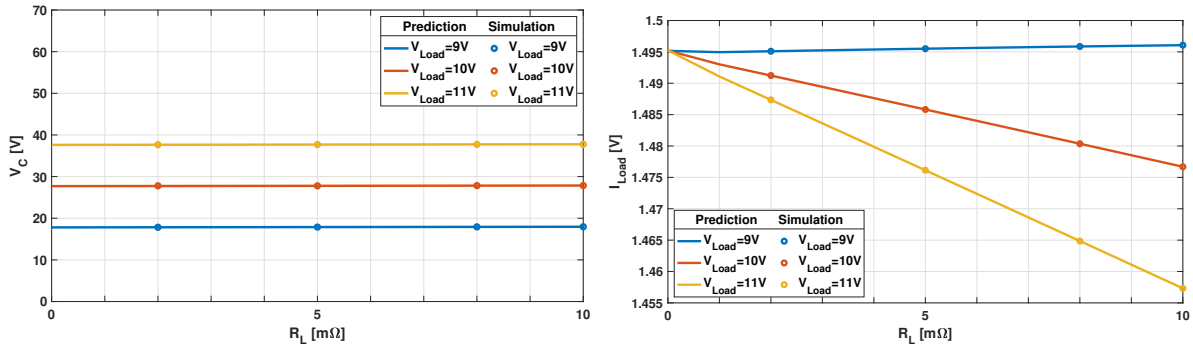
For odd-level FCML converters with non-deal timing, the flying capacitor voltages can be modeled as $V_{C_k} = xV_{in} + yV_{out}$, where x deviates from $\frac{N-k}{N}$ and y deviates from 0. In this equation, V_{out} can either be a voltage source load or can be found out from $V_{out} = I_{out}R_{load}$ if a resistive load R_{load} is used. As with the non-deal timing, the converter becomes a current source, a current source load can easily saturate the converter. Fig. 10.2 depicts the variation of the flying capacitor voltage with the load. Timing mismatches are exaggerated to understand better what happens with non-ideal timing. In brief, ideal odd-level FCML converters become current source converters with non-deal timing and stay voltage sources with ideal timing A similar analysis was conducted in chapter 7; however, it did not provide the contexts in terms of output voltages.

The modeling approach so far assumed no loss element in the converters. With any practical losses, generally, the converters' steady-state voltages and currents are not expected to be changed by a significant amount. However, in odd-level FCML converters, that is not the case. Any loss in the circuit modifies the converters' steady-state voltages, especially the flying



(a) Flying capacitor voltage variation **(b)** Output voltage variation

Figure 10.3. Behavior of 3LB converter operating in voltage source mode with current source load with lumped resistance in series with the inductor (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$, $D_1 = 0.24$, $D_2 = 0.26$, $D_3 = 0.25$ and $D_4 = 0.25$)



(a) Flying capacitor voltage variation **(b)** Output current variation

Figure 10.4. Behavior of 3LB converter operating in current source mode with voltage source load with small timing mismatches and lumped resistance in series with the inductor (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$, $D_1 = 0.15$, $D_2 = 0.35$, $D_3 = 0.25$ and $D_4 = 0.25$)

capacitor voltages. The losses are modeled as a lumped resistance in series with an inductor, and the effect is incorporated in eqns. 10.1 and 10.2. The analysis shows that the lumped resistance helps balance an unbalanced flying capacitor voltage operating in the voltage source mode. And the higher the losses, the better the balancing performance of a converter. This has been verified in Fig. 10.3.

For some applications, for example, LED drivers and battery chargers, the current source behavior of the odd level FCML converter can be utilized [105]. It is desirable to analyze the converter operating in the current source mode (with big timing mismatches) with the losses.

It can be seen from Fig. 10.4 that the loading effect also modifies the output current of a 3-level converter in the current source mode. However, the output current deviates by a very small amount. Interestingly, the flying capacitor voltage does not change with the losses in the converter (Fig. 10.4a). The converter can be designed to operate in the current source mode with the flying capacitor voltage being equal to $V_{in}/2$, and this level won't change with the practical losses in the converter.

10.5 Chapter Summary

This chapter provides a general method of determining the flying capacitor voltages of the FCML converters directly. It has been shown that current source behavior is common to all odd-level FCML converters with non-ideal timing. General expressions for the current source value have been determined. For even-level FCML converters, even with non-ideal timing, the voltage source behavior does not change. This chapter also discusses the effect of losses on the flying capacitors and shows that for a 3-level converter, losses help the flying capacitor voltage to be stable around the expected level of operation.

Chapter 10, contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Part IV

Full Power Delivery Architecture

Chapter 11

Two-Stage Power Delivery Architecture Using Hybrid Converters

11.1 Introduction

Improving power delivery and management plays a key role in minimizing the cost of building and operating future green data centers to meet the fast growth of high-performance computing. Toward this important goal, a reduced number of conversion stages with large conversion ratio converters can be one of the most viable approaches to adopt simplify the power delivery rack and improve efficiency. With this motivation, in this chapter, an AC-to-core power delivery architecture for data centers and telecommunication systems has been included comprised of only two direct conversion stages: 1) AC to 48-60V step-down PFC rectifier and 2) 48-60V to 0.8V-3.3V DC-DC converter stages. The proposed power delivery architecture is shown in Fig. 11.1.

The two converter stages have been designed by employing hybrid converters that take advantage of the switched capacitor and inductor operations for better efficiency and power density. Full structure with device-level details is shown in Fig. 11.2. The PFC rectifier stage in this chapter utilizes a new multi-level hybrid converter based on partial series-parallel switched-capacitor operations to reduce inductor value and total harmonic distortion. It also steps down and moves the DC link to a lower voltage level, at 48-V nominal, where high-density capacitors can be utilized for energy buffer. This converter can simultaneously regulate the output voltage

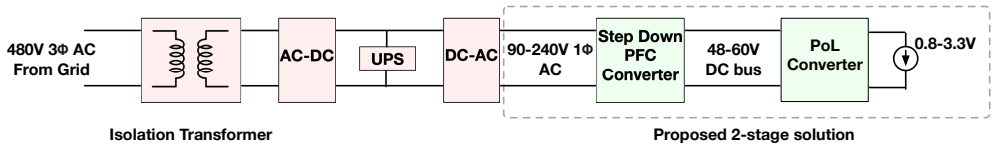


Figure 11.1. Proposed power delivery architecture

and input current to maintain good power and efficiency by employing fast input current and slower output voltage control loops. The last-centimeter point of load (PoL) converter in this demonstration is a GaN-based multi-phase multi-inductor hybrid (MPMIH) converter designed to provide very high output currents at low voltages with very high current density. This chapter is organized as follows. Section 11.2 and 11.3 discuss the PFC step down and the MPMIH converter in detail with operations and design considerations respectively. Section 11.4 presents the experimental results. The chapter is summarized and concluded in section 11.5.

11.2 Step Down PFC Converter

Traditional AC-DC conversion with moderate to high power generally uses a bridge-less structure [106, 107] shown in Fig. 11.3a. In this converters, V_{out} is maintained at a higher voltage than the peak voltage of the AC input voltage, V_m. With a suitable modulation scheme, the switching nodes, V_x and V_y, are connected to either V_{out} or ground as required to maintain the average voltage of V_{xy} over a switching period equal to V_{in}. This operation ensures a well-maintained average input current proportional to the input voltage to obtain a high power factor. There are different control schemes to regulate input current and output voltage to support the basic operation of this converter [108]. While this operation can achieve a good displacement power factor or near zero phase lag between the input voltage and current, the distortion power factor can still deteriorate because of switching current ripple at high input voltages. Switching current ripple magnitude can be made smaller with larger input inductance, higher switching frequency, and/or lower voltage stress. However, increasing the inductance requires a larger sized inductor that leads to lower power density, and increasing the switching frequency may not

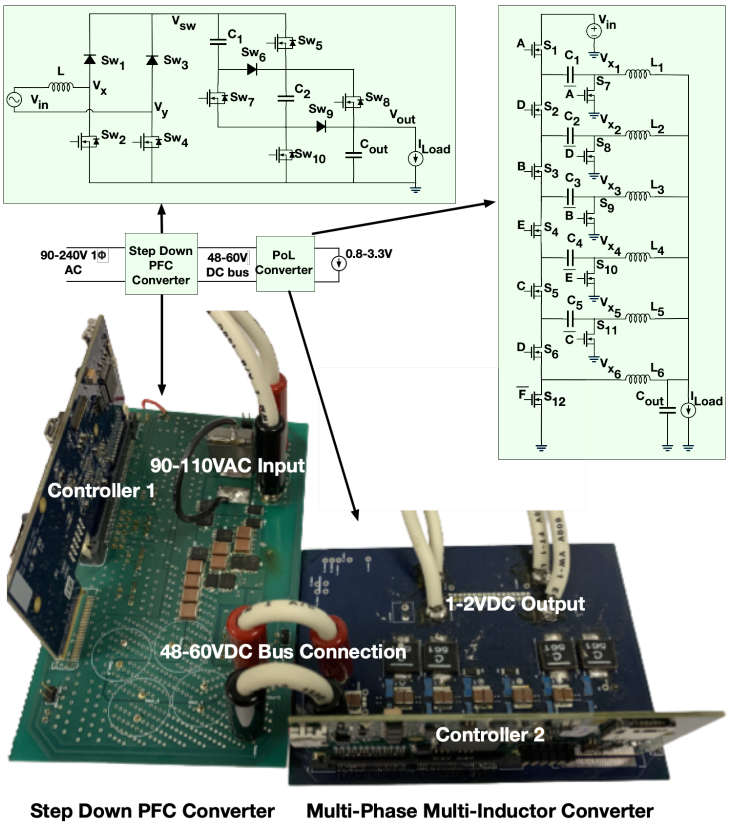
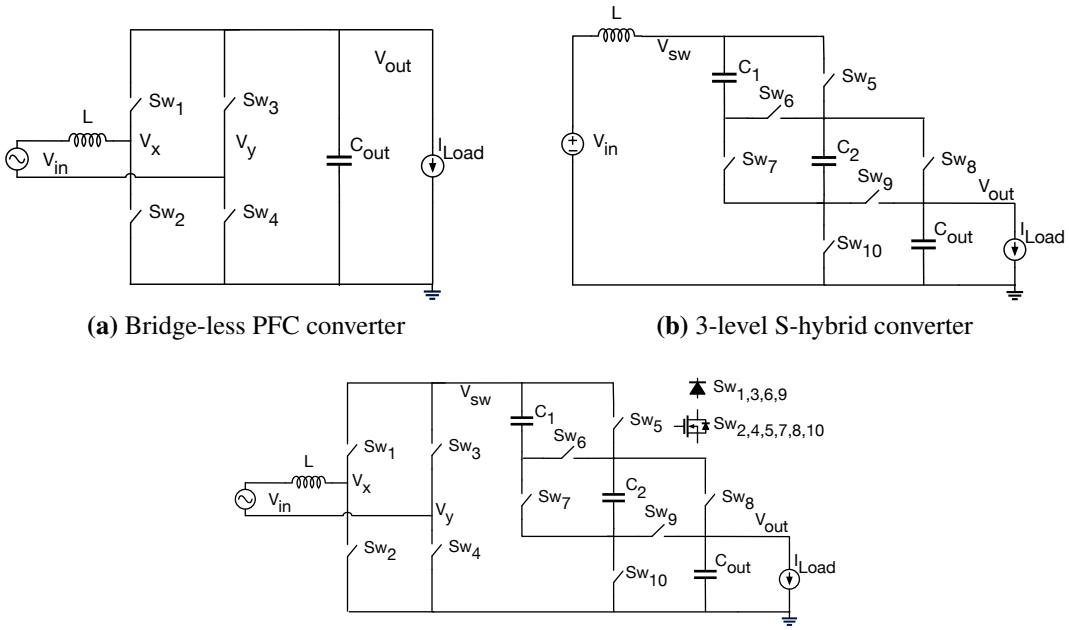


Figure 11.2. New Power delivery architecture with stages implemented using new SC-based hybrid converters

be desirable because an optimal value is highly dependent on particular semiconductor devices and core materials of the inductor. From this consideration, topological modifications for smaller voltage stress on the input inductor and active devices can give a better solution to achieve the design goal.

The modular multilevel converter has been popular for its topological advantages and is widely used in DC-AC applications. There are also reports on switched-capacitor architectures for conversion from a single DC voltage to a high voltage AC output [109–111]. However, the converter type is found to be less explored in AC-DC conversion applications. In this chapter, the architecture of an S-hybrid converter [112] has been modified and merged with a bridge-less or totem pole PFC converter for AC-DC applications. The s-hybrid converter is a step-down hybrid DC-DC converter extended from a switched-capacitor (SC) converter with an inductor at



(a) Bridge-less PFC converter

(b) 3-level S-hybrid converter

(c) New PFC step down converter

Figure 11.3. S-hybrid Converter and derived PFC converter

the input, i.e., an inductor-first structure in step-down conversion. This architecture allows small input current stress on the inductor, leading to reduced conduction loss, in addition to the benefits of low voltage stress on active devices [112]. A 3-level S-hybrid converter in this category is shown in Fig. 11.3b. This converter comprises an inductor at its input and a partial series-parallel network for step-down operation that allows the inductor to be switched in three small voltage domains of the input voltage. The combination of this converter with the bridge-less PFC converter in Fig. 11.3a results in the new final PFC step-down hybrid converter depicted in Fig. 11.3c.

11.2.1 Topology and Operation

As shown in Fig. 11.3c, the presented PFC step-down hybrid converter has one current shaping inductor, L, and four switches $Sw_{1\text{-}4}$ in the main rectifier. These switches operate at high frequency during the fraction of the line cycle at low voltage while staying idle, on or off, for the remaining time. A switched-capacitor (SC) circuit follows the rectifier to provide the

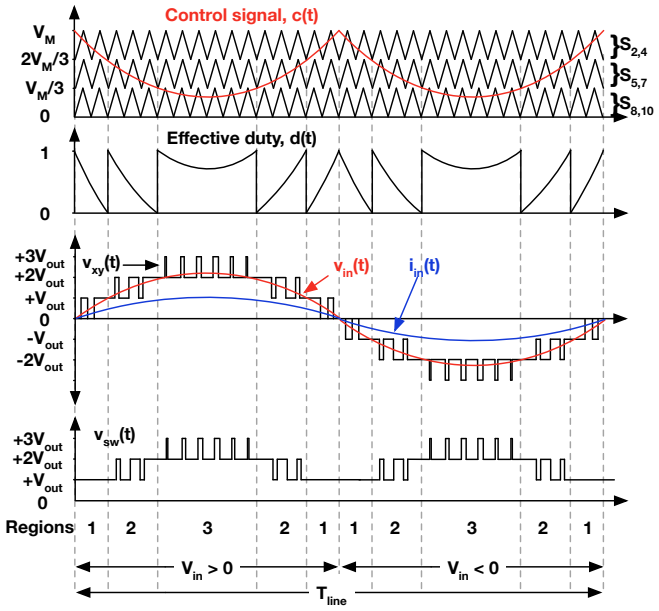
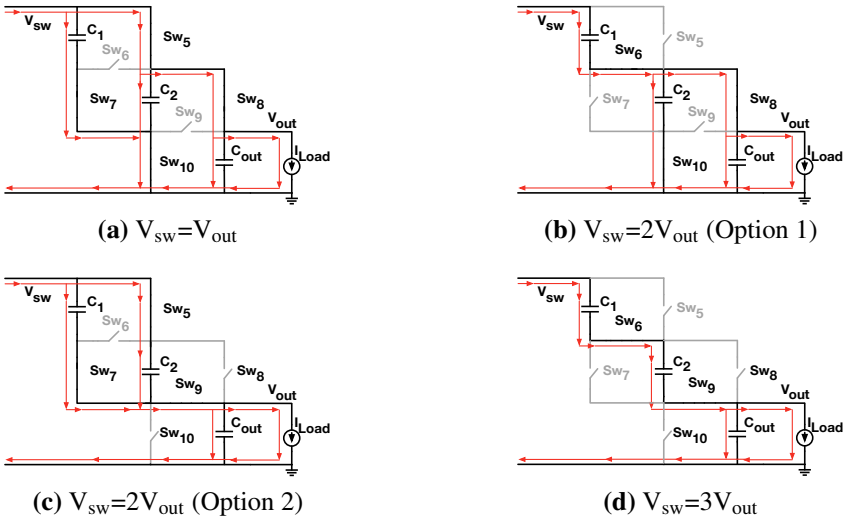


Figure 11.4. Ideal operational waveforms

stepped-down output and multilevel switching voltages to limit the inductor blocking voltage to V_{out}. In this demonstration, the SC circuit has two flying capacitors $C_{1\text{-}2}$ and six switches $Sw_{5\text{-}10}$. These switches also operate at the converter's operating frequency during designated periods of the line cycle.

Figure 11.4 depicts the simplified ideal operational waveforms of the full converter during a full line cycle. All capacitors are expected to have negligible voltage ripples and equal voltages. Assume an input voltage with a peak value of V_m such that $2V_{out} \leq V_m < 3V_{out}$, the full line-cycle can be divided into three time regions: 1) region 1: $0 \leq |V_{in}| < V_{out}$ 2)region 2: $V_{out} \leq |V_{in}| < 2V_{out}$, and 3) region 3 : $2V_{out} \leq |V_{in}| < 3V_{out}$. For any of these regions, the converter switches are operated in such a way that V_{xy} switches in a pulse-width-modulated (PWM) control manner between the upper and lower limit of the region to synthesize an average voltage equal to V_{in}. The rectifier switches, $Sw_{1\text{-}4}$, take care of selecting the right polarity of V_{xy} in accordance with the input voltage being positive or negative. As a result, V_{xy} switches among 7 levels (0, $\pm V_{out}$, $\pm 2V_{out}$ and $\pm 3V_{out}$).

The SC configurations to generate different switching node V_{sw} voltages suitable for



(a) V_{sw}=V_{out} **(b)** V_{sw}=2V_{out} (Option 1)

(c) V_{sw}=2V_{out} (Option 2) **(d)** V_{sw}=3V_{out}

Figure 11.5. SC configurations to generate different switching node voltages

different input voltage levels are shown in Figure 11.5. In operation, $Sw_{5,7}$ turn ON and OFF together while Sw_6 is their complementary switch. In a similar way, Sw_9 is the complementary of $Sw_{8,10}$. The rectifier switches, $Sw_{1\text{-}4}$ bridge the SC configurations with the input inductor and the source. In this proof of concept demonstration, $Sw_{1,3,6,9}$ are implemented with diodes for simplicity, while $Sw_{1,2,5,7,8,10}$ are implemented with MOSFETs to control the operation of the converter. The switch selection for the main rectifier has been done following a standard bridge-less PFC converter design [106].

To control the switches, PWM control signals can be acquired by comparing a control signal c(t) with 3 separate carrier signals at 3 different voltage domains, as shown in Fig. 11.4. The control signal can be generated by weighing regulation information of output voltage and input current by the required output power and the input voltage. Particularly, when c(t) is in the first region, Sw_2 is switched at the carrier frequency when $V_{in}>0$, while switching of Sw_4 is activated when $V_{in}<0$. $Sw_{5,7}$ and $Sw_{8,10}$ are activated with c(t) in the second and third regions, respectively. In a practical implementation with digital PWM modules in a microcontroller, the effective duty cycle, d(t), can be calculated digitally based on similar information and used to generate the PWM signals. Following [112], d(t) can be calculated as:

$$d(t) = \begin{cases} 1 - \frac{|V_{in}|}{V_{out}} & \text{when, } 0 \leq |V_{in}| < V_{out} \\ 2 - \frac{|V_{in}|}{V_{out}} & \text{when, } V_{out} \leq |V_{in}| < 2V_{out} \\ 3 - \frac{|V_{in}|}{V_{out}} & \text{when, } 2V_{out} \leq |V_{in}| < 3V_{out} \end{cases} \tag{11.1}$$

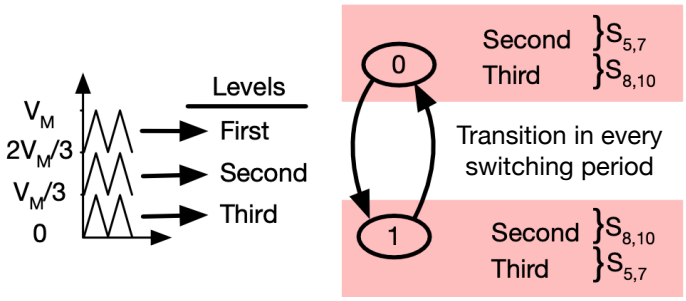
Utilizing Eqn. 11.1 and assuming $V_M = 1$, a separate set of expressions for d(t) can be derived in terms of c(t) which is useful to directly generate the PWM signals for the switches using different PWM modules in micro-controller:

$$d(t) = \begin{cases} 3c(t) - 2 & \text{when, } \frac{2}{3} \leq c(t) \\ 3c(t) - 1 & \text{when, } \frac{1}{3} \leq c(t) < \frac{2}{3} \\ 3c(t) & \text{when, } 0 \leq c(t) < \frac{1}{3} \end{cases} \tag{11.2}$$

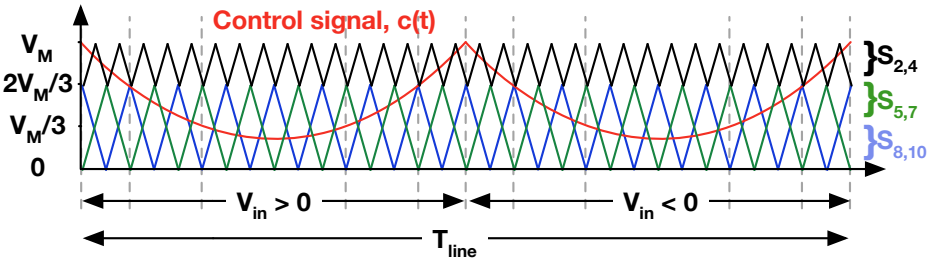
Note that the switches in the SC circuit block 3x times smaller voltages than the switches in the main rectifier. Therefore, these switches can be selected with a smaller voltage rating, lower $R_{DS,on}$, and lower parasitic capacitance to improve overall performance with reduced conduction and switching losses.

11.2.2 Modified Operation for Capacitor Balancing

In operation described with Fig. 11.5, flying capacitors $C_{1\text{-}2}$ and output capacitor C_{out} are placed either parallel or stacked in series to generated V_{out}, $2V_{out}$ and $3V_{out}$ levels at the switching node, V_{sw}. To generate $2V_{out}$, C_1 can be stacked on top of C_2 and C_{out} (configuration option 1) in Fig. 11.5b, or a parallel combination of C_1 and C_2 is placed on top of C_{out} in Fig. 11.5c (configuration option 2). Although theoretically capable of supporting the $2V_{out}$ needed for operation, using only one of these configurations causes a high capacitor voltage ripple problem for capacitor C_1 and C_2 in region 3, where V_{sw} is switched between $2V_{out}$ and $3V_{out}$. If only configuration option 1 is used, C_1 keeps receiving charges without redistribution to lower capacitors as the converter stays in region 3. On the other hand, if only configuration



(a) Logical flow of the modified operation



(b) Practical implementation of the modified operation

Figure 11.6. Modified operation

option 2 is used, both C_1 and C_2 keep receiving charges without redistribution to C_{out} and the load. The excessive charge for the flying capacitor(s) in region 3, where the input current is at its peak, will cause a high voltage ripple, significant hard-charging loss, and risks of over-voltage damages for both capacitors and active switches. In addition, the over-charged voltage in the flying capacitors also causes unwanted variations in the average voltage of V_{xy}, which distorts the current waveform, increasing current harmonics and reducing power factor.

The overcharging problem in flying capacitors was identified in [109] for a demonstration of an inverter with a slightly different topology and operation. It was also suggested to size the flying capacitor large enough to keep the over-voltage within a specific range. However, this method becomes less effective in high-power applications where the input charging current is significant or very large capacitors are required. To avoid spending excessive area for more capacitance, in this chapter, a relatively simple operational solution has been provided to solve this problem.

Recognizing that the key to the solution is charge redistribution among the flying capacitors and to the output capacitor, both the configurations have been combined and alternated, option 1 (Fig. 11.5b) and option 2 (Fig. 11.5c), in each switching cycle to generate V_{sw}=2V_{out}. This way, the input charge is redistributed to the load every two switching cycles.

To implement this modified control, simple logic conditions can be added to generate alternative PWM signals from the second and third levels of multilevel carrier signals in Fig. 11.4 for $Sw_{5,7}$ and $Sw_{8,10}$. These conditions can be active for the full line cycle without changing the basic operation of the converter. Fig. 11.6a depicts the simplified logical diagram for the modified operation.

To generate these control signals with a smooth transition between different regions in a more practical implementation in a micro-controller, carrier signals can be modified as in Fig. 11.6b, where the second and third carrier signal levels are implemented with two 180°phase-shifted PWM signals with magnitudes from 0 to $^{2V_M}/_3$. In this way, at least once in every two switching periods, C_1 is also placed in parallel to C_2 and C_2 is placed in parallel to C_{out}, which is tightly regulated. This operation makes sure the flying capacitors closely track the regulated output voltage V_{out} as frequently as every other switching cycle.

It is worth noting that this over-voltage problem does not come into the scene during regions 1 and 2 as charge redistribution to C_{out} and V_{out} happens once in every switching period, keeping an equal voltage for all the capacitors, $V_{C_1} = V_{C_2} = V_{C_{out}} = V_{out}$. Also, the increased voltage for C_1 in this converter is different than the imbalance problem in FCML converters. The resultant voltage variation in this converter is at line frequency, does not depend on small timing mismatches [19], and can be calculated quite precisely with existing models.

11.2.3 Advantage of the Proposed Converter: Reduced Inductor Current Ripple

With two flying capacitors and an output capacitor, this converter can generate seven levels for V_{xy} node voltage. As a result, in a major portion of the line cycle, the inductor is

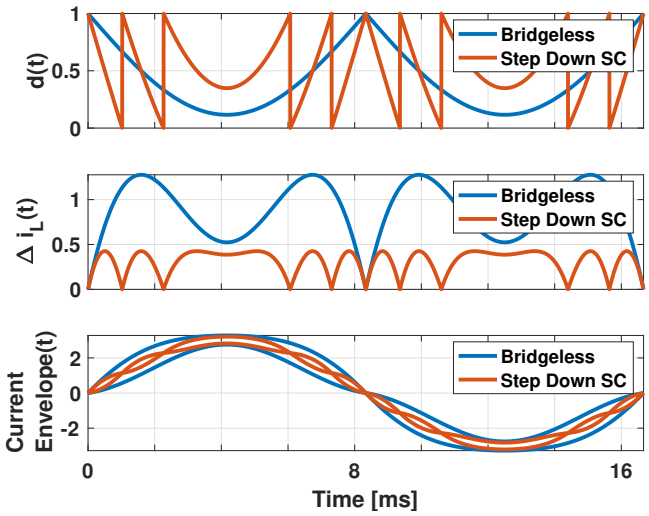


Figure 11.7. Comparison of current ripples of the step-down PFC converter (90Vrms-to-48V/4A) and bridge-less PFC converter (90Vrms-to-3×48V/4/3A) for same output power operation with 47 μH inductor anf 600 kHz switching frequency

charged and discharged by a smaller amount of voltage than a bridge-less or totem pole PFC converter. Particularly, in region 1, the inductor is switched to either input voltage or V_{out} which is smaller than V_m. In region 2, the inductor voltages are $|V_{in}|$-V_{out} and $2V_{out}$-$|V_{in}|$, while in region 3, they are $|V_{in}|$-$2V_{out}$ and $3V_{out}$-$|V_{in}|$. Using the inductor voltage information, the current ripple of the step-down PFC converter is calculated and compared with a bridge-less/totem-pole PFC converter at the same power and operating point in Fig. 11.7. It can be observed that the new step-down PFC converter maintains smaller current ripples and, thus, a narrower envelope of the inductor current throughout the operation. Hence, one can also predict a superior THD performance in the new converter compared with a bridge-less/totem-pole PFC converter at the same operating condition.

11.2.4 Advantage of the Proposed PFC Converter: DC-Link Filtering with Low-Voltage Capacitors

In any AC-DC or DC-AC application, the choice of total DC link capacitance depends on the line frequency, maximum power, and maximum allowed voltage ripple. The amount of capacitance is typically very large considering large output power and low line frequency.

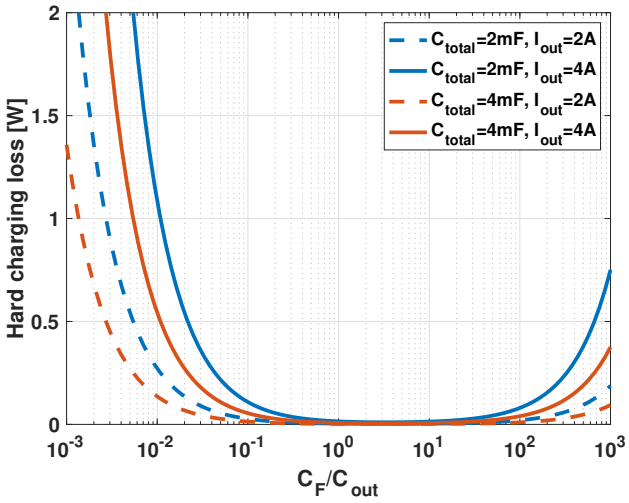


Figure 11.8. Capacitor loss comparison between ceramic and electrolytic (EK) flying capacitors

The presented step-down PFC converter also falls in this general category. However, unlike conventional PFC converters, this converter carries out the DC-link filtering function at low-output voltage levels. More importantly, the switched-capacitor operation with efficient charge redistribution, described in subsection 11.2.2, allows all flying capacitors and output capacitors to participate as DC-Link capacitors. A key benefit here is that this allows the large DC-Link capacitance to be distributed among the flying capacitors with no difference in energy buffering performance. As an additional benefit, large values of flying capacitors minimize their switching-frequency ripple and hard-charging loss to improve overall efficiency. The low output voltage rating requirement also enables the selection of higher-density capacitors to reduce overall implementation size and increase the system power density.

However, it is of interest to analyze the resultant losses with the choice of capacitance. Figure 11.8 compares the hard-charging losses for a different choice of total capacitance and operating condition. It can be seen that the minimum loss choice would be selecting the flying capacitance to be 1-5 times the output capacitance. Intuitively, flying capacitors charge and discharge with the input charges of the converter during most of the line cycle, while the output capacitor deals with the charge resultant by subtracting the output charge of the converter from the

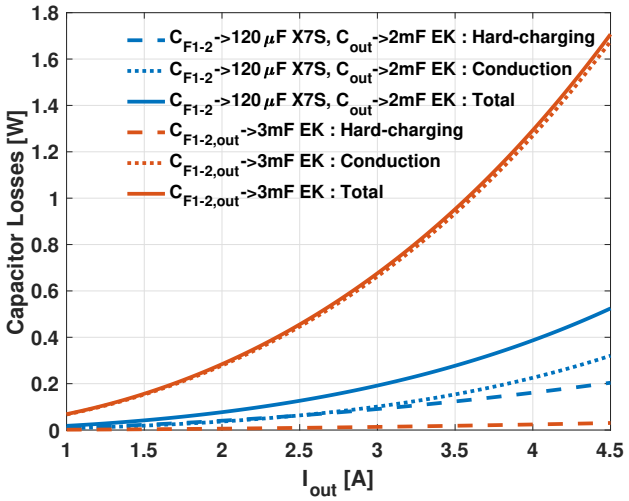


Figure 11.9. Capacitor loss comparison between ceramic and electrolytic (EK) flying capacitors

input charge. Therefore, the output capacitor should be smaller in nominal operating conditions than the flying capacitors.

As a design aspect, one needs to select between electrolytic and ceramic capacitors for the converter. The design can be made electrolytic-free by using ceramic capacitors either with or without methods to enhance the energy buffering capability of the capacitors, for example, using series stacked energy buffer [113] or stacked switched capacitor buffer [114]. While there are certain benefits in an electrolytic-free implementation, the main drawback of using only ceramic capacitors for both flying and output capacitors is that they are more expensive and have relatively lower energy density than those of electrolytic capacitors.

As a proof of concept, in this chapter, electrolytic capacitors have been used for their large energy buffering capability owing to their higher capacitance density and for a relatively simpler implementation. However, as these capacitors have high ESRs, using them for flying capacitors would cause excessive conduction loss. Figure 11.10 shows an analytical comparison of capacitor conduction and hard-charging losses between the two cases: 1) small ceramic capacitors (X7S) are used for the flying capacitors and high-density electrolytic (EK) capacitors for the output filtering, and 2) all capacitors are electrolytic. The result is clear that the first

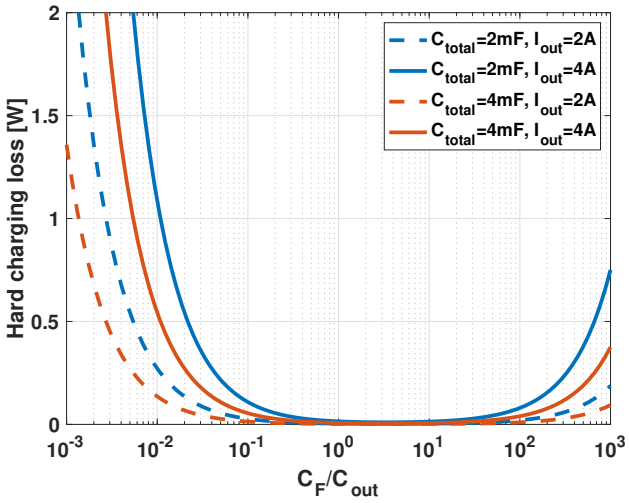


Figure 11.10. Capacitor loss comparison between ceramic and electrolytic (EK) flying capacitors

case exhibits significantly smaller losses compared to the other one even has a smaller total capacitance. Following the analysis, the converter implementation in this chapter, presented in Section 11.4.1, utilizes a combination of ceramic and electrolytic capacitors for flying capacitors and output capacitors, respectively.

11.2.5 Control and Sensing Circuits

The traditional feed-forward average current mode control [115] for the PFC boost converter has been employed to control this new converter. Figure 11.11 illustrates the block diagram of the control procedure in a microcontroller. Small-signal model analysis of the converter's input current response and output voltage indicates the converter behaves the same way as multi-level converters and standard PFC boost converters [115]. Thus, the long-existing and well-adopted knowledge for the control of a PFC boost converter can readily be used to design the voltage compensator, G_{cv} and current compensator, G_{ci}. Detailed steps for this design can also be found in [115]. Delay-associated poles from the micro-controller have also been considered to properly design the compensators [116].

However, sensing the input signals to be used in a microcontroller can be tricky as the

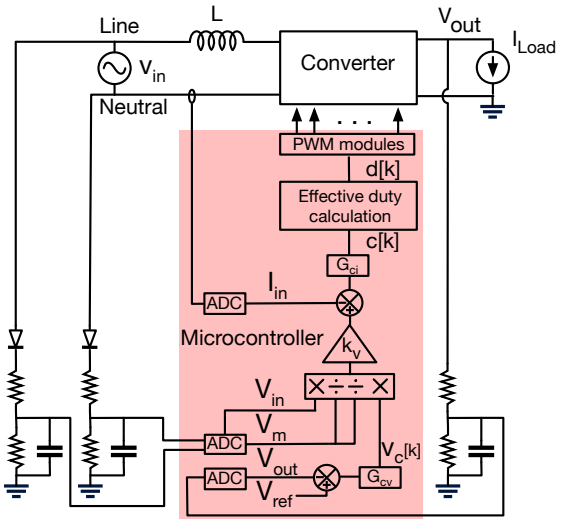


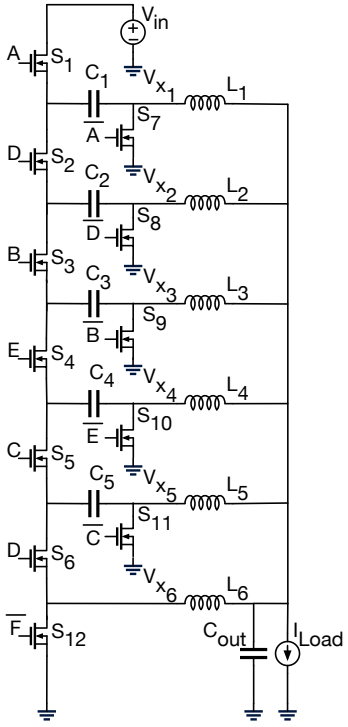
Figure 11.11. Controller with sensing circuits

system ground is different from any of the terminals of the input source. Two separately rectified resistive divider circuits with R-C filter have been used from the line and neutral terminal of the input source to the system ground to create a low voltage reference for the microcontroller's ADC following [117]. This method only provides good reference when Sw_4 is ON during $V_{in}>0$ and Sw_2 is ON during, V_2 in ON during $V_{in}<0$, which are the cases for nominal operation. As the control of the full converter, depends on sensing the input signals, at the beginning of the operation, the controller has to force them to switch so that a good input reference can be generated and sensed. If Sw_2 or Sw_4 malfunctions, a debug procedure based on reference sensing will also be faulty. On the other hand, output voltage sensing can be conveniently done with a direct resistive divider. In this chapter, current sensing has been conveyed very conveniently with a hall current sensor[1].

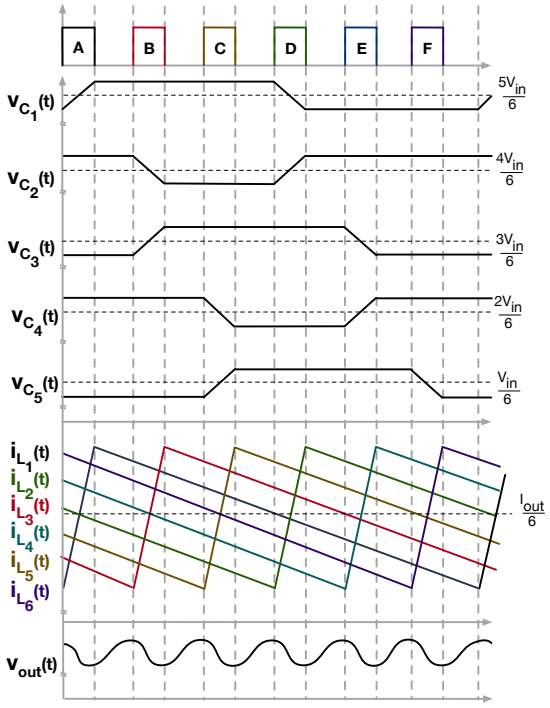
[1]At the time of organizing this dissertation around late 2022, the author has found a current control loop less controlling method for this AC-DC Step-Down Converter. Unfortunately, the experimental results can not be produced due to a busy schedule around the time of graduation. A brief discussion on this control can be found in Appendix I.

11.3 Multi-phase Multi-Inductor Hybrid Converter

Recently, the last stage converter for 48V-to-1V conversion has received a lot of interest in the industry and academic research with remarkable implementations using both isolated [72,118] and non-isolated architectures [9]. In this chapter, a member of the multi-inductor hybrid (MIH) converter family [15–17,41,54], a 6-level converter extension of the previously demonstrated DP-MIH converter reported in [17] has been utilized. The additional inductors and interleaved phases are extended to support larger output currents compared with prior works.



(a) 6-level multi-phase multi-inductor (MPMIH) hybrid converter



(b) Operation of the presented MPMIH converter

Figure 11.12. 6-level multi-phase multi-inductor (MPMIH) hybrid converter and its operation with AD-BE-CF phase sequence

11.3.1 Multi Inductor Converter with Multi-Phase Operation

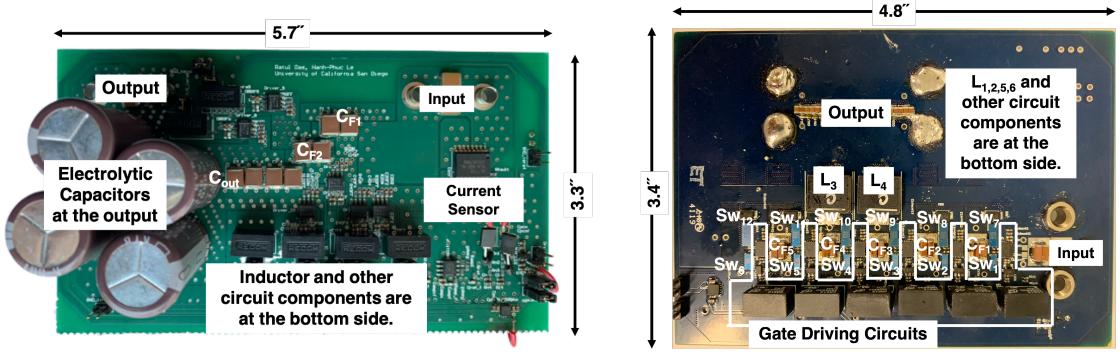
The 6-level MPMIH converter is depicted in Fig. 11.12a. It has twelve switches S_{1-12}, five flying capacitors C_{1-5} and six inductors L_{1-6}. The input switched-capacitor (SC) network divides the input voltages by 6 times to feed into the Buck-like output filter inductors that, in turn, synchronously soft-charge and soft-discharge the flying capacitors. The high-side six switches S_{1-6} are controlled by six multi-phase pulse width modulated (PWM) signals, A-F with duty cycle, D, while the ground-connected freewheeling switches S_{7-12} are controlled by six complementary signals, $\overline{A}$-$\overline{F}$, respectively. Accordingly, the output voltage and flying capacitor C_i voltages can be represented by $V_{out} = \frac{DV_{in}}{6}$ and $V_{C_i} = \frac{6-i}{6}V_{in}$ where $i = 1-5$. The key constraint in the converter operation is that no two consecutive signals controlling two consecutive high-side switches in S_{1-6} can overlap. Following this constraint, the converter can support an operation of two to six interleaving phases with the six inductors of the six-level converter. While a maximum number of phases yields advantages in output voltage ripple and transient response as well as switching loss reduction, it also limits the maximum duty cycle and, thus, maximum output voltage. For example, six phases are non-overlapped and evenly distributed with 60° phase shift and A-F are arranged for the switches $\mathrm{Sw}_{1\text{-}6}$ sequentially, each of the phases A-E has a maximum duty cycle of $1/6$, limiting the maximum output voltage to $V_{in}/36$. However, it is also possible to arrange the phases in a different, non-sequential method to allow a larger maximum duty cycle while satisfying the requirement of no overlap in consecutive phases. Figure 11.12b depicts an example operation where steady-state operation of the MPMIH converter uses this strategy. The six non-overlapped phases, in the order of A to F, are limited to $3/6$, $2/6$, $2/6$, $3/6$, $3/6$, and $3/6$ respectively. This arrangement allows a maximum output voltage $V_{in}/18$ while still obtaining the benefits of a 6-phase interleaving operation with equal duty cycles. When a maximum output voltage is prioritized, the converter operation can be changed to 2-phase interleaving to reach an output voltage of $V_{in}/12$.

11.4 Experimental Results

The two-stage 110VAC-to-1VDC power delivery architecture has been implemented using two converter prototypes, shown in Fig. 11.13a and 11.13b. Key components for the converters are listed in Table 11.1 and 11.2. These converters have been tested separately and in combination to demonstrate the full structure.

11.4.1 Step-Down PFC Converter

Figure 11.14a shows the key waveforms of the converter at 90VAC to 48V/4A operation. It can be seen that the input current follows the input voltage, verifying the key PFC operation. The performance of the converter is shown in Fig. 11.16 in terms of efficiency and power factor. The converter maintains higher than 96% efficiency for a wide range of operations and more than 95% for almost all operating points. As shown in Fig. 11.16b, the converter achieves a power factor of 0.98 at 2.6 A effective input current. The power factor goes down at lower input current, i.e. lower output power, because of noise and harmonics caused by multi-level switching operations that couple to and reduce the accuracy of the current sensor and the current regulation loop. The power density of this converter at full power is 73W/in^3, including all the components, including output electrolytic capacitors.



(a) Step-down PFC multi-level AC-DC converter

(b) 6-level MPMIH DC-DC converter using GaN FETs

Figure 11.13. Two converter prototypes of the 110VAC-to-1VDC power delivery architecture

Table 11.1. Components used in PFC step-down converter

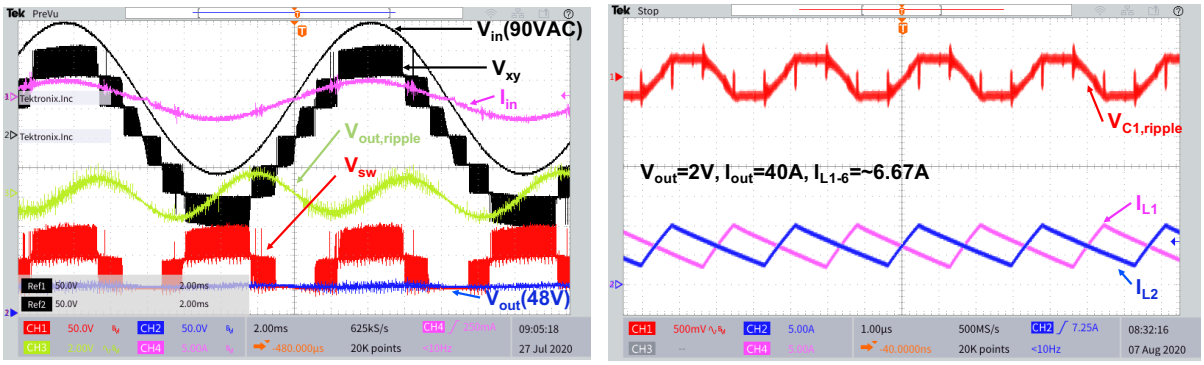
Components	Part Number
$Sw_{1,3}$	SBR10U200P5DICT-ND
$Sw_{2,4}$	BSC500N20NS3GATMA1CT-ND
$Sw_{5,7,8,10}$	BSC123N08NS3GATMA1
$Sw_{6,9}$	SBRT20M80SP5-13
$C_{1,2}$	8xC5750X7S2A156M250KB
C_{out}	8xC5750X7S2A156M250KB+ 4xEKYB101ELL102MM40S
L	IHLP6767GZER470M11
Gate driver	UCC5350MCDR
Current Sensor	ACS716KLATR-6BB-NL-T

Table 11.2. Components used in MPMIH converter

Components	Part Number
$Sw_{1\text{-}6}$	2xEPC2015c
$Sw_{7\text{-}12}$	2xEPC2023
$C_{1\text{-}5}$	4xCGA8M3X7S2A335M200KB
$L_{1\text{-}6}$	XAL1030-561ME
Gate Driver	LMG1210

11.4.2 MPMIH Converter

Figure 11.15 shows the key waveforms of the MPMIH converter in a 48V to 2V/40A operation example. Using a phase sequence selection presented in Fig. 11.12, the converter's output current was a 6-phase interleaved combination of inductor currents. The converter can also support up to ~4 VDC output. The standalone performance of this converter is presented in Fig. 11.17. At 48V-to-1V operation, this converter achieved a peak efficiency of 90.75% at 40A load current, whereas, 92.31% was achieved for a 48V-to-1.8V conversion and at 50A output current. The converter was tested to a maximum load current of 220 A at 1V and 240 A at 1.2-1.8V. Considering the components in the power flow path, this converter achieved a current density of 1.03 kA/in^3 for 1V and 1.123 kA/in^3 for other output voltages, which translates into 1.03 kW/in^3 and 2.02 kW/in^3 peak power densities for 1V and 1.8V output voltages, respectively. Similar experiments have also been carried out for 54V input voltage. At 54V input voltage, this converter achieved peak efficiency of 90.6% and 92% for 1V and 1.8V output voltage,



(a) Steady state waveforms at 90Vrms to 48V/4A operation

(b) Experimental waveforms , I_{L1}, I_{L_2} and V_{C1} of MPMIH converter for 48V to 2V/40A conversion at 300kHz with AD-BE-CF phase sequence

Figure 11.14. Steady-state operation of step-down PFC converter and the MPMIH converter

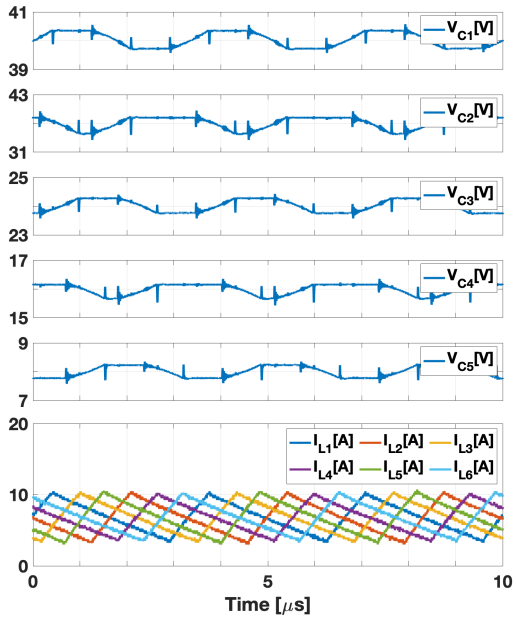
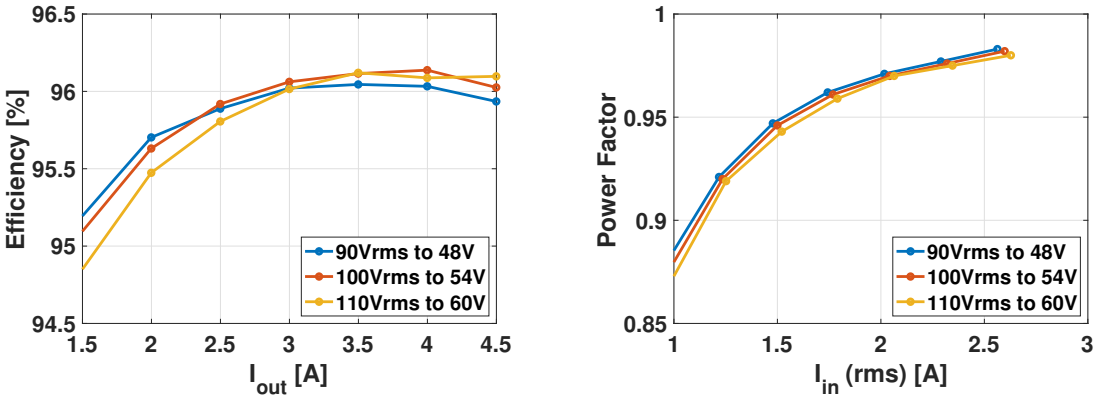


Figure 11.15. Measured capacitor and inductor waveforms of the MPMIH converter prototype for 48V to 2V/40A operation

respectively.

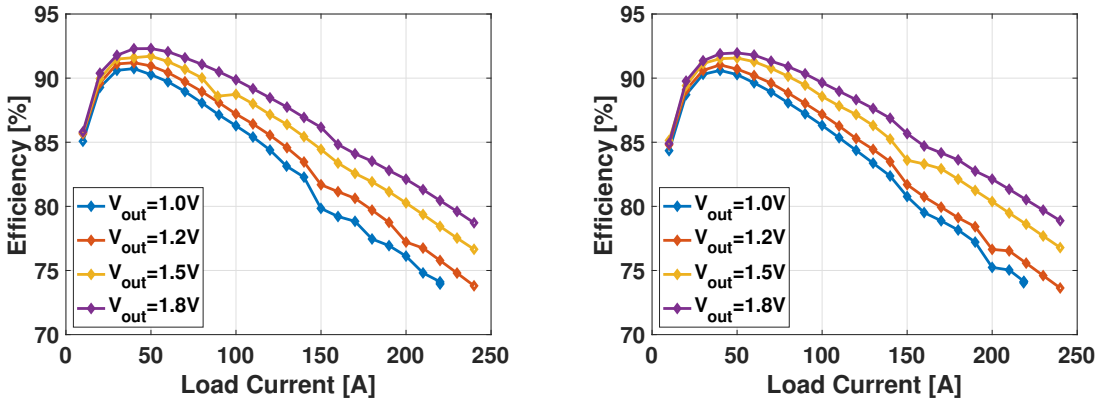
11.4.3 Full System Verification

The MPMIH converter was connected to the step-down PFC converter's output to complete the full power delivery system that bridges an AC distribution voltage to core DC voltages.



(a) Efficiency **(b)** Power factor

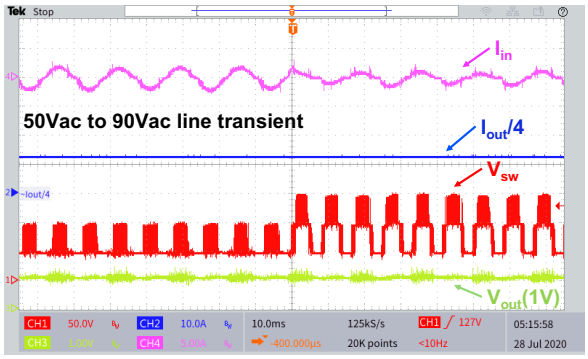
Figure 11.16. Performance of the step-down PFC Converter



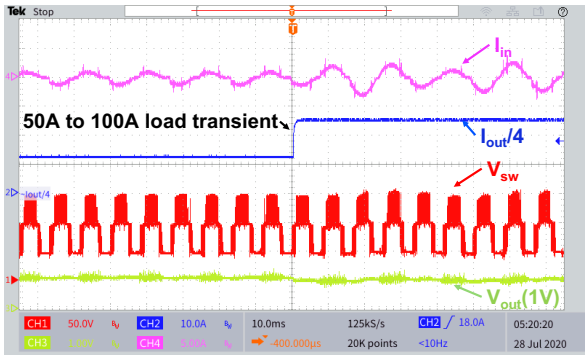
(a) V_{in}=48 **(b)** V_{in}=54V

Figure 11.17. Efficiency of the MPMIH converter

Figure 11.18 shows the operations of the full system in line and load transients. The waveforms of input inductor current (I_{in}), output current ($\frac{I_{out}}{4}$), switching voltage (V_{sw}), and output voltage (V_{out}), illustrate stable operations and regulations of the converter and output voltage when the converter is exposed to a 40 Vrms line voltage step (Fig. 11.18a) and a 50A load step (Fig. 11.18b). The first-stage step-down PFC hybrid converter can provide a fast response toward big line transients thanks to the flying capacitors capable of changing multiple levels while the second stage regulation manages the remaining variations at the input ~48V bus (the output of the first stage) and finally provides final regulated ~1V output. The seamless duty cycle control



(a) Operation at 1V/50A for a 50Vrms to 90Vrms line transient



(b) Operation at 1V from 90Vrms input voltage for a 50A to 100A load transient

Figure 11.18. Measured waveforms of the complete two-stage architecture for line and load transients

from the second stage also takes care of the high load current transient at the final output. The system's overall efficiency is shown in Fig. 11.19. For 110VAC-to-1VDC operation, the overall efficiency peak is 84.1%. The peak output current when testing the full system is limited to 160A because of a non-fundamental limit in the design of the first-stage AC-DC converter, which has an output current under 4.5A.

For comparison, a conventional power delivery architecture using 4 conversion stages for the same application would require all stages to individually achieve, on average, an efficiency of

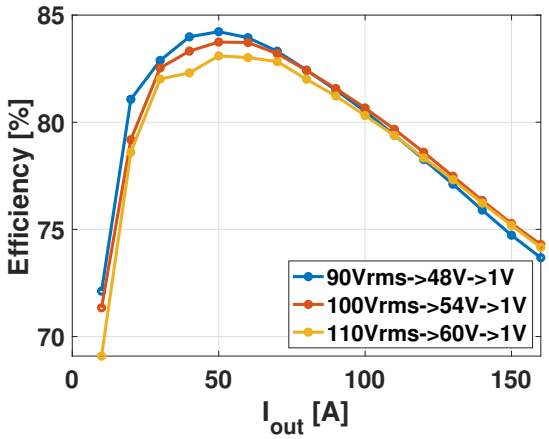


Figure 11.19. Efficiency of the full AC Grid-to-Core voltages system

95.8% to reach an equivalent performance of this proposed two-stage architecture. Considering the full conversion from 110 VAC to 1 VDC, to the authors' best knowledge this has not been demonstrated.

11.5 Chapter Summary

In this chapter, a demonstration of the two-stage architecture is provided to directly convert AC distribution voltage to the core voltages that can be applied to power delivery in data centers and telecommunication systems. The demonstration includes a new switched-capacitor multi-level step-down PFC converter and a 6-level switched-capacitor-based multi-phase multi-inductor hybrid (MPMIH) converter. The operation of the step-down PFC converter was discussed with control mechanisms for output voltage and input current regulations. A simple method of charge redistribution for flying capacitor voltage balancing at the carrier switching frequency was also provided. In designing the MPMIH converter, a new phase sequence has been proposed and verified in experiments for larger output voltage and current ranges. The converter designs are verified separately and together in the complete two-stage AC grid-to-Core voltage system, demonstrating a bright promise for future applications to contribute to more green and energy-efficient data centers, telecommunication, and other IT systems.

Chapter 11, in full, is a reprint of the archived unpublished materials in "Two-Stage Power Delivery Architecture Using Hybrid Converters for Data Centers and Telecommunication Systems," in TechRxiv.org by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Part V

Partial Power Processing

Chapter 12

Modular Hybrid Step-Down PFC Converter for Direct AC/DC Conversion with Partial Power Processing in Data Centers

12.1 Introduction

In data and cloud computing centers and telecommunication systems, the ultimate loads are high-performance processors that require low voltages, ranging from 0.6V to 1.2V for cores and up to 3.3V for other peripheral circuits, but very high currents, up to 1000A at core voltages. Many industries and research efforts have tried to address the challenge of providing low-voltage, extremely high-current outputs for these processors with new last-centimeter Point-of-Load (POL) converters. In order to reduce the current delivery loss, these converters receive an input voltage as high as 48 VDC. It is an equally difficult challenge to efficiently provide this 48 VDC bus from an AC distribution line. Typically, this is done in two stages: 240 VAC to 400 VDC and 400 VDC to 48 VDC [10]. In this work, a new AC/DC converter approach has been presented that can directly convert a high-voltage AC to a low-voltage DC, particularly of interest, 240 VAC to 48 VDC.

In recent years, the use of switched-capacitor (SC) based hybrid converters has been significantly increased with hybrid DC-DC step-down converter architectures. These hybrid converters differ in locating inductors at the input [48, 112], at the output [16, 17, 34], or directly

connected and distributed with flying capacitors [26]. In these converters, the switched capacitors are proven to be a key factor in reducing voltage stress on active and passive components, reducing overall implementation area, and increasing system efficiency. While SC is gaining momentum in DC-DC conversions, its use is still relatively limited with conversions related to AC, including both AC/DC and DC/AC conversions. One can find examples of SC-based inverters (DC/AC conversion) [109–111], but much less for AC/DC applications that require more stringent current sensing and control and thus, this is a more challenging and compelling task.

In this work, a new SC-based AC/DC hybrid converter modular architecture is proposed and demonstrated. In this architecture, a converter module can provide a good power factor by shaping the current through an input inductor and at the same time, stepping down the voltage. Multiple converter modules can be connected in series to support higher AC input voltages while simultaneously powering multiple outputs to get the benefits of partial power processing in AC/DC applications. Sections 12.2 and 12.3 of this chapter discuss the operations of a single converter module and multiple series-connected modules. Section 12.4 includes experimental results for verification. Section 12.5 summarizes and concludes this chapter.

12.2 AC/DC Step Down Converter

12.2.1 Topology

A 4-level hybrid step-down converter is shown in Fig. 12.1. The converter consists of a current-shaping inductor and a full bridge rectifier followed by a switched capacitor circuit. Both the rectifier and the SC circuit take part in the current shaping for PFC operation. The full-bridge rectifier consists of four switches, S_{1-4}. Note that there is no DC link capacitor required in this converter for energy buffering purposes. Instead, the energy buffering capacitors are distributed as the flying capacitors of the SC network that also provides up to 4X step-down conversion from the rectified voltage. As a common characteristic of SC-based converters, this SC circuit can also

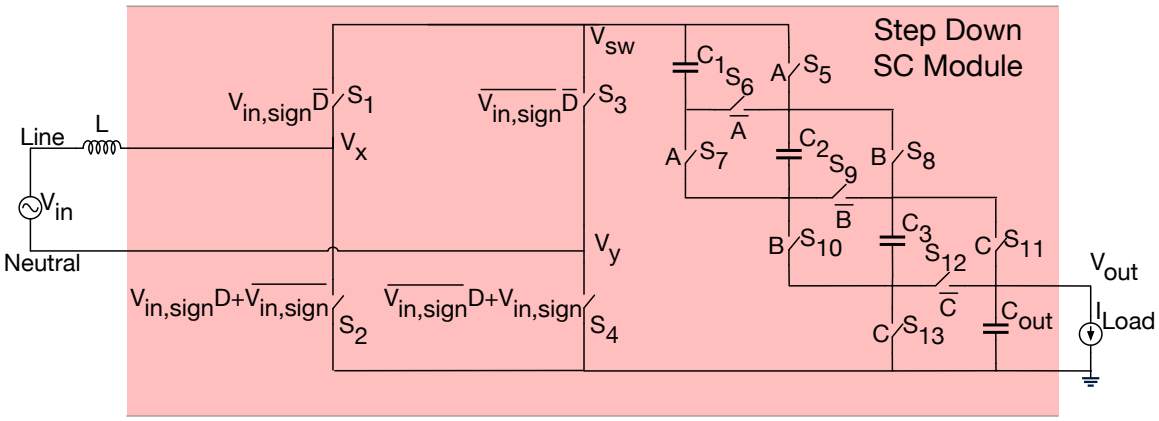


Figure 12.1. 4-level hybrid step-down PFC converter

be constructed with a larger or smaller number of levels according to a certain maximum input voltage requirement. In this work, a four-level version for the SC network has been selected, which has nine switches, S_{4-13}, three flying capacitors, C_{1-3} and one output capacitor, C_{out}. With a proper switching scheme, all capacitors block the same voltage as the output and together act as the line-frequency filtering capacitor at this low voltage. Compared with a popular choice of DC-link capacitors at high voltage right after the rectifier, these low-voltage capacitors can have significantly higher capacitance and power density to achieve a compact implementation size.

12.2.2 Operation

The converter operation of the SC network and the input full-bridge rectifier can be explained with a timing diagram shown in Fig. 12.2. The converter employs a control signal, $c(t)$, calculated from weighted values of power and input voltage. This control signal is compared with four different triangular (or saw-tooth) carrier signals to generate the required PWM signals for the switches. Three 120°phase-shifted signals, A, B, and C are utilized to control switches, S_{5-7}, S_{8-10} and S_{11-13}. They occupy $3/4$ of the total modulation voltage V_M and are referenced to the ground level. The full-bridge rectifier switches are controlled with another carrier signal D, which has the magnitude of $V_M/4$ and is referenced to the peak voltage of A, B, and C signals at $3V_M/4$. The rectifier switches are operated according to the input voltage polarity, determined

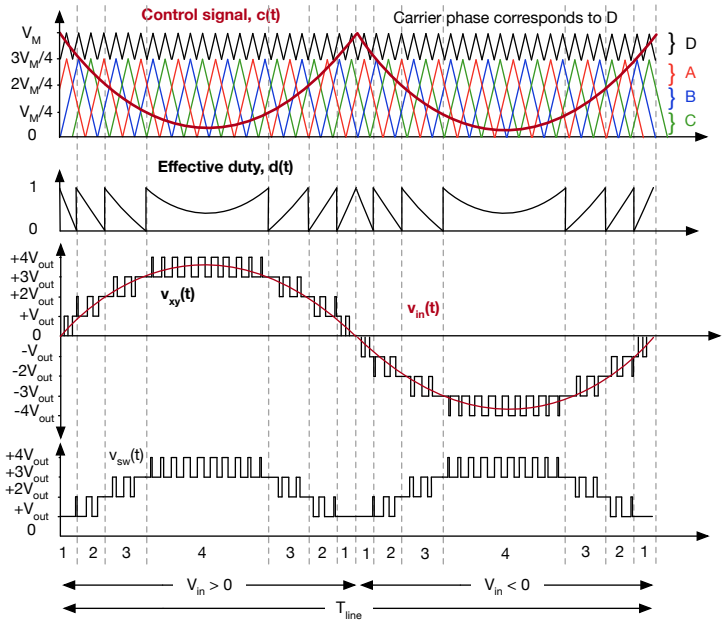


Figure 12.2. Operation of the proposed converter module

by $V_{in,sign}$.

With appropriate control signal $c(t)$, the switched capacitor circuit can be reconfigurable to provide step-down ratios of 1X, 2X, 3X, or 4X from its input node, V_{sw}. In other words, similar to flying capacitor multi-level (FCML) AC/DC converter [113], by stacking a different number of capacitors in the SC network, V_{sw} can be switched at any level or between any two adjacent levels out of these 4 voltage levels, $1 \times V_{out}$, $2 \times V_{out}$, $3 \times V_{out}$ or $4 \times V_{out}$ when the absolute value of input voltage is $0 < |V_{in}| < (1 \times V_{out})$, $(1 \times V_{out}) < |V_{in}| < (2 \times V_{out})$, $(2 \times V_{out}) < |V_{in}| < (3 \times V_{out})$ or $(3 \times V_{out}) < |V_{in}| < (4 \times V_{out})$ respectively. The duty cycle of V_{sw} at a certain voltage level is modulated to synthesize a desired input current shape. V_{sw} voltage is translated into differential voltage, V_{xy}, that, via the inductor, maintains an average voltage that follows the input voltage. This operation ensures that the input current closely follows the input voltage to maintain a good power factor. Small V_{sw} voltage swing at high switching frequency enables small current-shaping inductor L and lowers total harmonic distortions (THDs) in the input current. The control signal, $c(t)$ generation is similar to the existing boost PFC rectifier [108].

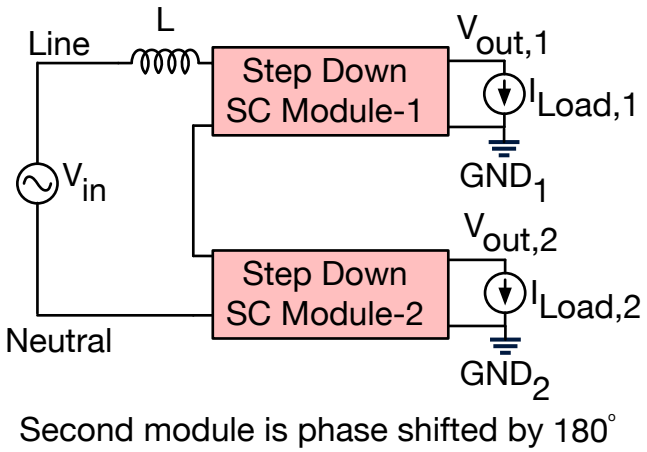


Figure 12.3. Modular architecture for partial power processing

12.3 Modular Architecture

The proposed AC/DC step-down PFC converter can reconfigure to convert any AC voltages with peak voltage less than the $4 \times V_{out}$. To support an AC input voltage higher than this level, multiple converter modules can be stacked in series as shown in Fig. 12.3. In this architecture, only one input current shaping inductor is required for the two series-connected modules. The outputs of the two modules are separated from each other and do not share the same power ground. In data center applications, a similar partial power processing architecture has been proposed with significant benefits in power delivery and system efficiency but limited to DC-DC conversion stages after the high-voltage AC/DC rectification stage [119]. This work is unique with partial power processing in the single direct AC/DC conversion stage. The separated output domains from this modular architecture can be used to power separate loads with no common ground using non-isolated DC-DC converters [15–17, 41] or to power the same high-power processor using isolated 48V POL converters similar to the one reported in [22, 118].

A challenge in implementing this modular architecture is the control, including generating multiple PWM control signals, carrier signals, and certain communications between converter modules to ensure appropriate individual regulations. In this demonstration, each of the converter modules uses a separate microcontroller capable of providing the required number of PWM

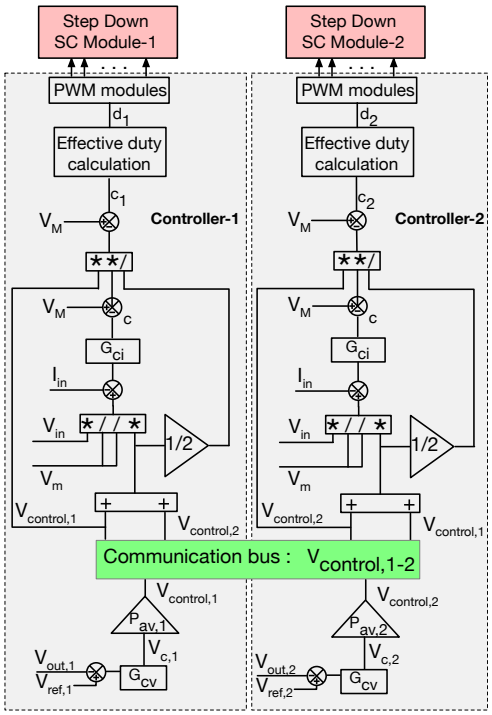


Figure 12.4. Control of the modular architecture in multi-module operation

modules for switch control signals. The two microcontrollers are connected through a Controller Area Network (CAN) communication bus.

Figure 12.4 shows the proposed control method for the modular architecture. The controllers control the two outputs separately but share the same control of the input current. For proper partial power processing operation, the converter modules need to exchange information on output power and output voltage. This information is presented by $V_{control,1}$ in Controller-1 and $V_{control,2}$ in Controller-2 that are shared through the CAN bus. The PWM modules between the micro-controllers are synchronized using master-slave configuration[1].

12.4 Experimental Results

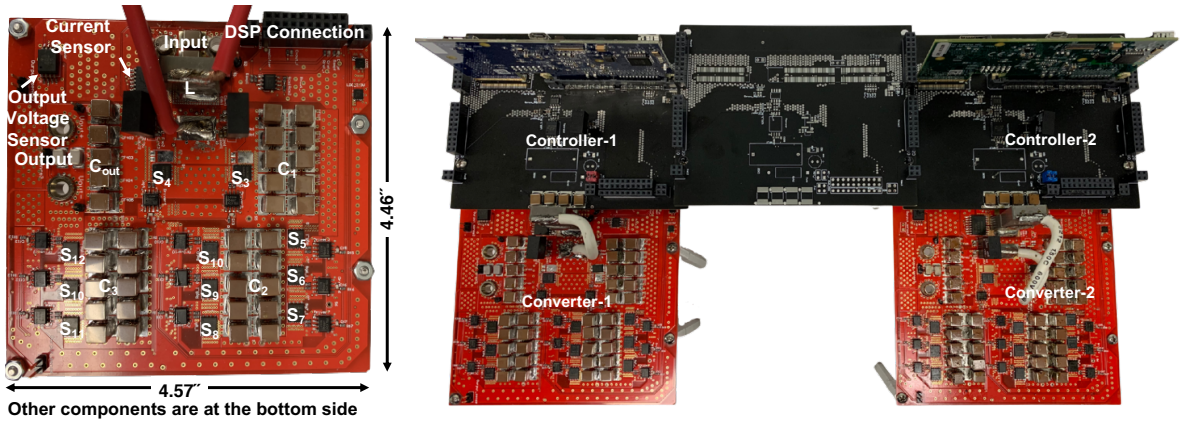
The converter prototypes in a single module and a series connection of two modules are shown in Fig. 12.5. Major PCB components are listed in Table 12.1. Figure 12.6a illustrates and

[1]At the time of organizing this dissertation around late 2022, the author has found a simple current control loop less controlling method. Unfortunately, the experimental results can not be produced due to a busy schedule around the time of graduation. A brief discussion on this control can be found in Appendix I

Table 12.1. List of components

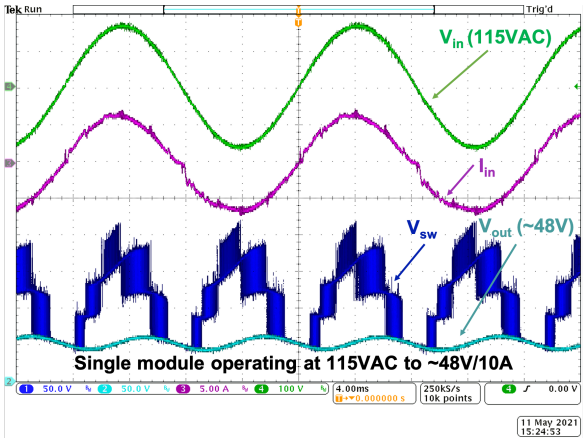
Components	Parts
$S_{1,3}$	200V Diodes (Diodes Inc.)
$S_{2,4}$	200V MOSFET (Infineon)
S_{5-13}	80V MOSFET (Infineon)
C_{1-3}	60x 100V 22 μF TDK
C_{out}	20x 100V 22 $^{-}$F TDK
Gate driver	UCC5350MC
Current Sensor	ACS716KLATR-12BB-T
Isolated output voltage sensor	AMC1311B
Isolated input voltage sensor	AMC1300BDWV

verifies the key operation of the single module prototype in a 115VAC-to-48VDC/10A conversion example. The operation of the single converter module demonstrates its reconfigurability with different numbers of capacitors connected in series and respective voltage levels to support different AC input voltages. Similar to other multi-level operations, the inductor in this converter experiences low voltage stress and has small ripples. In addition, the flying capacitors and output capacitors collaboratively perform the work of energy buffering for AC/DC power conversion at the low output voltage level, as evident in the 2X line frequency ripple seen at the output

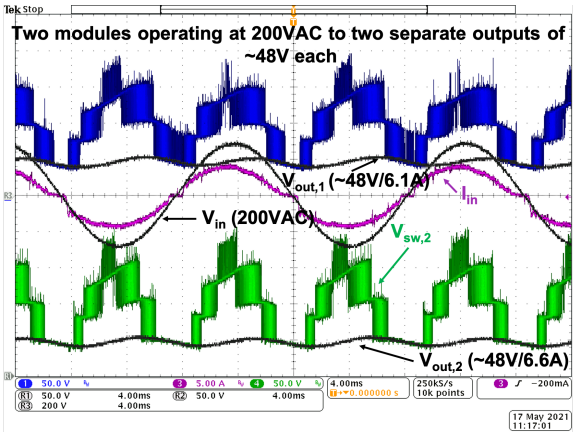


(a) Single converter module **(b)** In multi-module AC-stack configuration

Figure 12.5. Prototypes of the proposed module converter

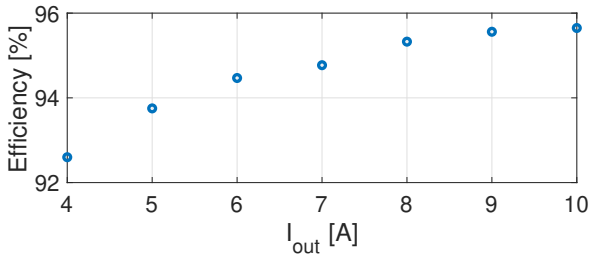


(a) Operation of a single module at 115VAC to 48VDC/10A

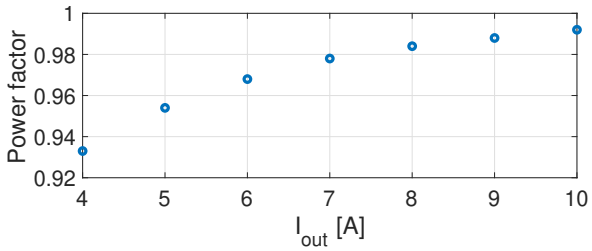


(b) Operation of series connected two modules at 200VAC to two -48VDC with 6.1A and 6.6A load

Figure 12.6. Experimental verification of the converter prototypes in single and multi-module configurations



(a) Efficiency



(b) Power Factor

Figure 12.7. Measured efficiency and power factor of a single module operating at 115VAC-to-48VDC

voltage and also in all flying capacitors. Figures 12.7a and 12.7b list the performance of a single converter in terms of efficiency and power factor.

Figure 12.6b captures the operational waveforms of the prototype with two converter modules connected in series, shown in Fig. 12.5b. The modular operation is at conversion from 200VAC to two 48 V outputs. As can be observed from the operational waveforms, the modular control method is verified to enable separate voltage regulations for the two outputs while sharing a common input current and its modulation for power factor correction.

12.5 Chapter Summary

In summary, a new hybrid converter module architecture is proposed that can be configured to support a direct AC/DC conversion. The converter features an inductor at the input followed by a switched-capacitor rectifier network. Converter modules can be reconfigured and controlled as individuals or together in a series stack to provide partial power processing through a direct-conversion single AC/DC stage to support higher input AC voltages while achieving both power factor correction and output regulations. The converter and the series stack architecture can be good candidates for the power distribution network in future data centers and telecommunication systems.

Chapter 12, in full, is a reprint of the material as it appears in "Modular Hybrid Step-Down PFC Converter for Direct AC/DC Conversion with Differential Power Processing in Data Centers," in 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 2219-2223 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Note that, in the actual published paper, the term "Differential" was used where, in this dissertation, it has been replaced with "Partial" to match with the traditional use of both these terms. The context is the same.

Chapter 13

Modular Isolated Vertically Symmetric Dual Inductor Hybrid Converter For Partial Power Processing

13.1 Introduction

DC-DC converters with large conversion ratios are required in many applications, such as automotive, data centers, solar plants, etc. Recently, the demand for high-voltage buses has been much more severe because of the increased current from or to the bus for high demand on the user's end, leading to significant relevant efforts from the industry and academia.

In data centers, last-centimeter conversion capable of supplying a moderate conversion ratio of 48V to 1-3.3V is desirable in recent emerging power delivery architecture. Recent demonstrations of different non-isolated DC-DC converter topologies for this application include a two-stage architecture with a 12V intermediate bus in [120] or a single-stage direct-conversion solution from 48V to core voltages in [34, 118]. In the non-isolated category, these solutions are switched-capacitor-based hybrid converters with or without regulation [34, 120]. In the isolated category, LLC and ICN-based converters have been also demonstrated [83, 118, 121, 122]. In this work, we are proposing a new architecture with a combination of switched-capacitor and transformer stages. The switched capacitor (SC) stage tolerates the high input voltage while the transformer stage provides isolation capability. In this design, to improve the output current

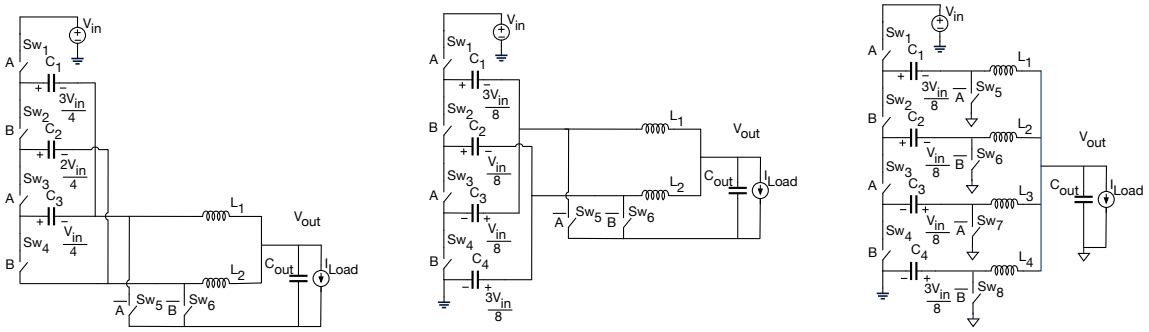
capability a current doubler rectifier is employed at the secondary side of the transformer. The converter architecture is called Isolated Vertically Symmetric Dual Inductor Hybrid (IVS-DIH) converter as it has two output inductors and a symmetric configuration across its vertical center. The switched capacitor portion tolerates symmetrical voltages at the two terminals of the transformer's primary.

Section 13.2 discusses the converter topology, operation, and steady-state analysis. Multiple modules of the converter can also be stacked to get the benefits of partial power processing. This stacked input/parallel output modular architecture is presented in section 13.3. Section 13.4 lists the experimental results obtained. The work is summarized and concluded in section 13.5.

13.2 Topology

13.2.1 Derivation

Multi-level Dual Inductor Hybrid (DIH) converters were first demonstrated for 48V-to-1V POL applications [15, 41, 74]. These converters provide seamless control of the output voltage with normal Buck-like pulse width modulated (PWM) duty cycle control. Fig. 13.1a shows a



(a) 4-level Dual Inductor Hybrid (DIH) converter

(b) 4-level Vertically Symmetric Dual Inductor Hybrid (VS-DIH) converter

(c) 4-level Vertically Symmetric Multi Inductor Hybrid (VS-MIH) converter

Figure 13.1. Derivation of the vertically symmetric dual inductor hybrid (VS-DIH) and multi inductor hybrid (VS-MIH) converter

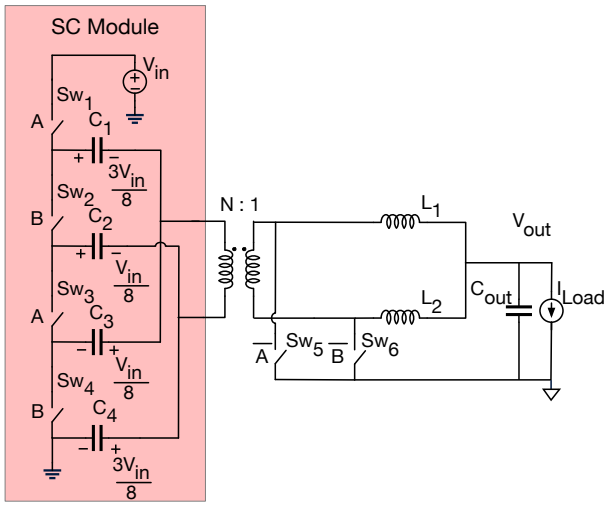


Figure 13.2. 4-level isolated vertically symmetric dual inductor hybrid (IVS-DIH) converter

4-level DIHC converter with a conversion ratio of $^{DV_{in}}/_{4}$. These converters can be utilized in applications that require large conversion ratios. However, the drawback of this converter family is that it requires a large bias voltage for the top capacitors, leading to capacitance degradation due to high DC voltage bias and larger capacitor sizes, which in turn, lead to limits in efficiency and/or power density [15].

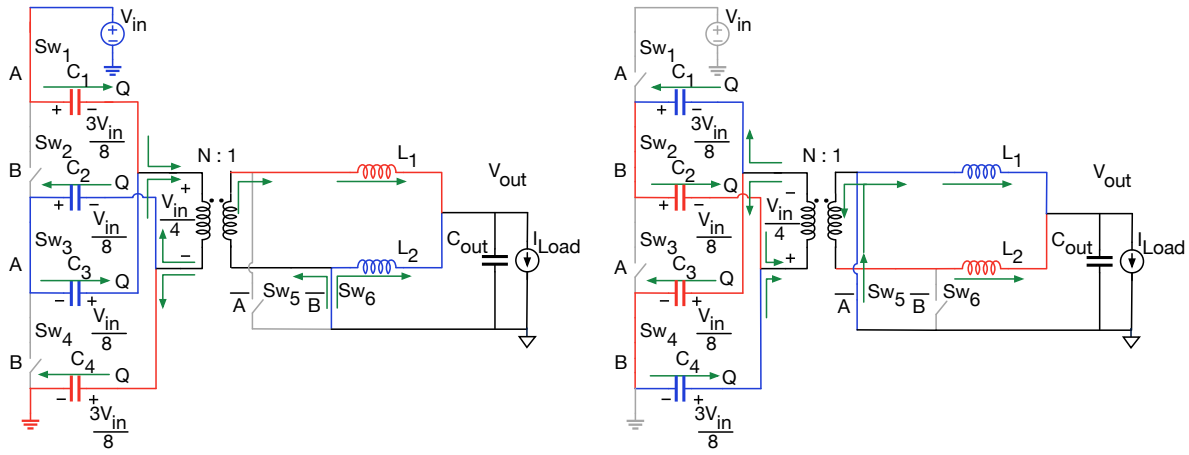
To reduce the voltage stress and completely remove hard-charging on flying capacitors. Fig. 13.1b shows the configuration where, output, inductors, and free-wheeling switches are placed midway between the positive and negative rails of the input. These components are functionally isolated from the main switched capacitor architecture with the flying capacitors. If these capacitors can be chosen as safety rated, this converter can be used as an isolated converter. However, safety-rated capacitors typically have small values while high current applications require much larger capacitance for proper voltage operations in multi-level hybrid converters. Fig. 13.1b shows a dual inductor hybrid converter where the output and voltage distribution on the flying capacitors is vertically symmetric. Following the same derivation of Multi Inductor Hybrid (MIH) topologies in [15–17, 41, 49], multiple inductors can also be arranged at the output to support large output currents. The configuration is shown in Fig. 13.1c.

In order to provide proper safety-rated isolation and additional voltage conversion, a

transformer can be inserted between the switched capacitor architecture and the output inductive stage, which results in the circuit shown in Fig. 13.2. The input switched capacitor stage of this converter consists of four switches, Sw_{1-4} and four capacitors, C_{1-4}. On the secondary side, there are two switches Sw_{5-6} and two inductors L_{1-2} forming a current doubler rectifier. Following this converter architecture, the transformer and secondary inductive stage can be other well-known isolated converters such as LLC, Impedance Control Network (ICN), etc. [118].

13.2.2 Operation

The converter is operated with two 180°phase-shifted signals, A and B, in the primary side and their inverted signals, $\overline{A}$ and $\overline{B}$, in the secondary side. It is possible to control, regulate and change the output voltage by changing the duty cycles of A and B phases up to the maximum value of $\sim$50%. In this demonstration, we target to operate the converter at near 50% duty cycle, yielding two operating states shown in Figs. 13.3a and 13.3b. In these operating states, the red color indicates components being charged, and the blue color for components being discharged. The operation of the converter can be explained using these two figures along with the timing diagram shown in Fig. 13.4.



(a) State 1 **(b)** State 2

Figure 13.3. Operation of the converter (Red color for charging and Blue color for discharging components)

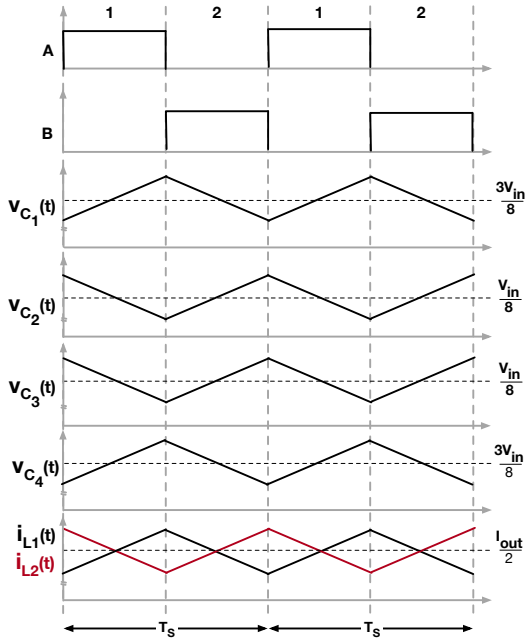


Figure 13.4. Ideal timing diagram of the operation

During state 1, the on-time of phase A, switches $Sw_{1,3}$ in the SC architecture and Sw_6 in the secondary side are ON, while other switches $Sw_{2,4,5}$ are kept OFF. In the SC architecture, current starts flowing through the capacitors by charging capacitors C_1 and C_4 and discharging capacitors $C_{2,3}$. The charging current of C_1 and discharging current of C_3 combine and flow through the primary side of the transformer and split into two parts to discharge C_2 and charge C_4. The voltage and current of the primary side of the transformer are induced to the secondary side to charge the inductor L_1. Sw_5 provides a path for the secondary current of the transformer as well the free-wheeling current of L_2. As the charging and discharging currents of the capacitors are reflected on the secondary side and eventually flow through L_1, this operation makes sure the capacitors are being softly charged and discharged.

State 2 is complementary of state 1. $Sw_{2,4,5}$ are ON and the other switches are OFF. This configuration allows the charged capacitors of state 1, $C_{1,4}$, to discharge and discharged capacitors of state 1, $C_{2,4}$, to charge. The combined current flow in the reverse direction of the transformer's primary side compared to state 1. The reflected current in the secondary flows through the inductor L_2. L_2 ensures the soft-charging of $C_{2,3}$ and soft-discharging of $C_{1,4}$. During

this state, Sw_5 carries the transformer current and the free-wheeling current of L_1.

13.2.3 Steady-State Analysis

Considering the duty-cycle D of phases A and B and transformer turn ratio N:1, we can get the following equations by applying volt-second balance on the inductors L_{1-2}:

$$\left[[V_{in}-(V_{C_1}+V_{C_4})]\frac{1}{N}-V_{out}\right]D-V_{out}(1-D)=\left[[(V_{C_2}+V_{C_3})]\frac{1}{N}-V_{out}\right]D-V_{out}(1-D)=0 \quad (13.1)$$

$$\left[[(V_{C_1}-V_{C_2})]\frac{1}{N}-V_{out}\right]D-V_{out}(1-D)=\left[[(V_{C_4}-V_{C_3})]\frac{1}{N}-V_{out}\right]D-V_{out}(1-D)=0 \quad (13.2)$$

Using equation 13.1 and 13.2, the conversion ratio and the capacitor voltages can be derived as,

$$V_{out}=\frac{DV_{in}}{4N}, V_{C_1}+V_{C_4}=\frac{3V_{in}}{4}\text{and } V_{C_2}+V_{C_3}=\frac{V_{in}}{4} \quad (13.3)$$

The individual voltages on the capacitors can be calculated as,

$$V_{C_1}=\frac{C_4}{C_1+C_4}\frac{3V_{in}}{4}, V_{C_2}=\frac{C_3}{C_2+C_3}\frac{V_{in}}{4}, V_{C_3}=\frac{C_2}{C_2+C_3}\frac{V_{in}}{4} \text{ and } V_{C_4}=\frac{C_1}{C_1+C_4}\frac{3V_{in}}{4} \quad (13.4)$$

As an equitable voltage bias on the capacitors are wanted, capacitors can be chosen so that, $C_1=C_4$ and $C_2=C_3$. This choice will ensure a balanced operation in the switched capacitor architecture with,

$$V_{C_1}=\frac{3V_{in}}{8}, V_{C_2}=\frac{V_{in}}{8}, V_{C_3}=\frac{V_{in}}{8} \text{ and } V_{C_4}=\frac{3V_{in}}{8} \quad (13.5)$$

Based on the derived capacitor voltages and considering small ripples, the maximum voltage stress on the switches, Sw_{1-4} are $V_{in}/2$. Secondary-side switches, Sw_{5-6} experience a voltage stress of $V_{in}/4N$.

The division by 4 in the conversion ratio in Eqn. 13.3 comes from the number of switched-capacitor levels. In this particular demonstration, we have restricted the operation of the converter to D=50% with the transformer's turn ratio of 4:2, the conversion ratio becomes in total, 16. If a higher conversion ratio is required, either the transformer turn ratio or the levels in the SC architecture can be increased.

For a converter with the L number of SC levels with L stack switches and L capacitors, and an N:1 transformer, the conversion ratio, and the capacitor voltages can be calculated as:

$$V_{out} = \frac{DV_{in}}{LN} \text{ and } V_{C_k} = V_{C_{L-k+1}} = \frac{[L-(2k-1)]\,V_{in}}{2L}, \text{ where, k } = 1,2,3,...,\frac{L}{2} \tag{13.6}$$

13.2.4 Capacitor Sizing

While conventional Dickson SC converter requires equal capacitor sizing for low loss operation [50], in a Dickson-based hybrid converter, a new capacitor sizing method was proposed to ensure full soft-charging and soft-discharging of all flying capacitors [15]. This method is based on circuit branch impedance in the hybrid converter operation and requires significantly different capacitance values, which can lead to complications in selecting flying capacitors. In the converter presented in this work, the transformer sees two capacitor branches comprised of series connected C_1 and C_4 in parallel with series connected C_2 and C_3 during State 1 in Fig. 13.3a). During state 2 in Fig. 13.3b, the converter sees again two branches of capacitors, series connected C_1 and C_2 in parallel with series connected C_3 and C_4. To ensure the same capacitance in each branch connected in any state, all the capacitance can be selected with the same value. This simplifies capacitor selection back to the simple equal capacitors in the Dickson SC converter and eliminates the requirement of different capacitors in [15] or the complex split-phase operation

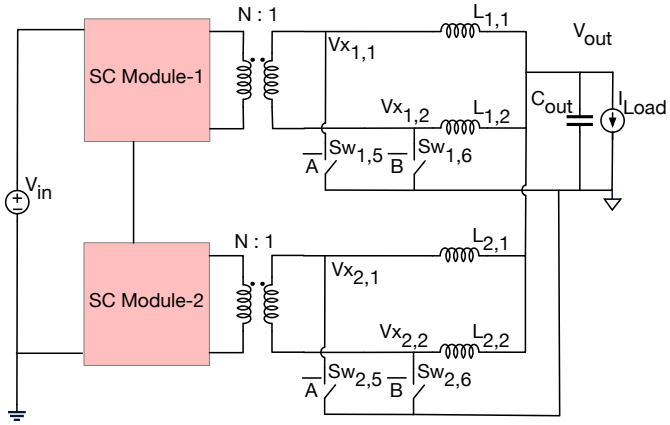


Figure 13.5. Modular architecture for partial power processing

in [35].

13.3 Modular Architecture For Partial Power Processing

As modern electrical power delivery requires higher voltage buses to reduce the distribution copper loss, converters are being exposed to higher and higher voltages. Although the input SC stage can increase the capacitor stages to support a higher input voltage, this also means there are more capacitors exposed to higher operating voltages. To mitigate this problem, a modular structure as shown in Fig. 13.5 can be used. In this structure, two converters of Fig. 13.2 can be connected in a stacked input/parallel output configuration. Each converter effectively only receives an input voltage of $V_{in}/2$ and processes half of the total output power. While the conversion ratio becomes $V_{out} = \frac{DV_{in}}{8N}$, DC bias voltages of each module's capacitors are reduced to $3V_{in}/16$ and $V_{in}/16$. For M number of modules of L SC levels with N:1 transformers, Eqn. 13.6 can be rewritten as,

$$V_{out} = \frac{DV_{in}}{MLN} \text{ and } V_{C_k} = V_{C_{L-k+1}} = \frac{[L-(2k-1)]V_{in}}{2ML}, \text{ where, k } = 1,2,3,...,\frac{L}{2}. \tag{13.7}$$

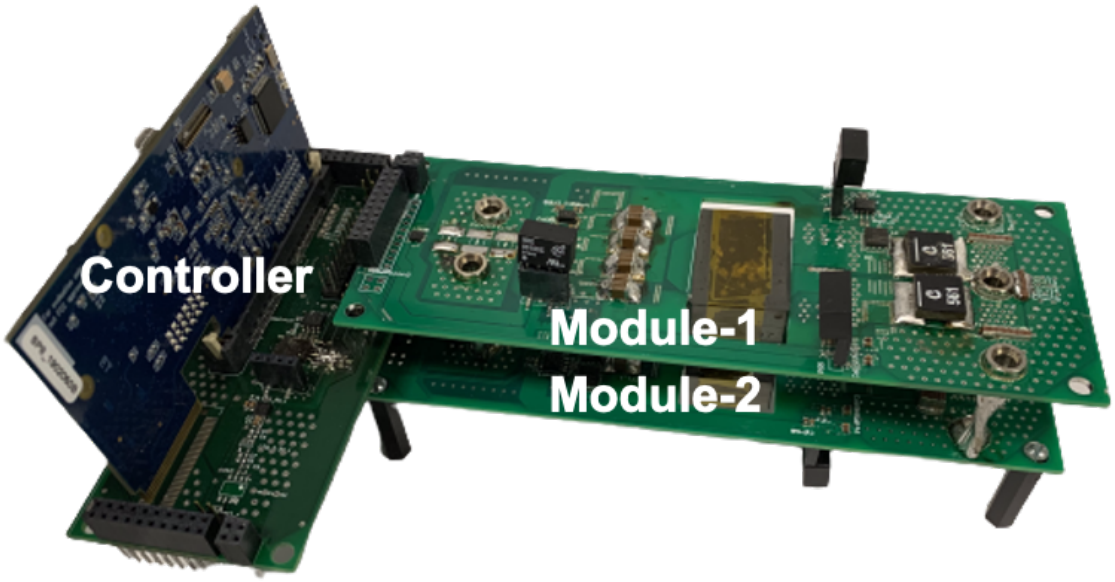


Figure 13.6. DC-stack modular configuration with two modules

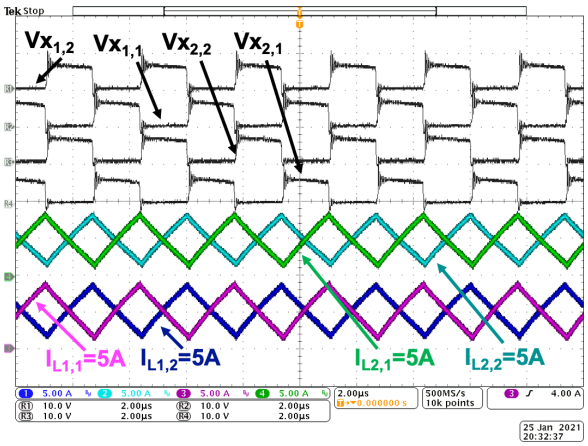
13.4 Experimental Results

A proof-of-concept prototype of the converter in Fig. 13.2 is built using the components in Table 13.1. Two modules of the converter are stacked as in Fig. 13.6 to demonstrate the modular architecture. Figure 13.7 shows the operation of the converter at 100V to 2.85V/20A with an operating frequency of 300kHz.

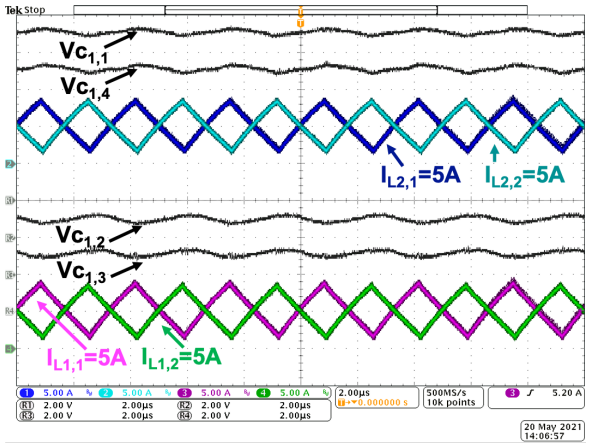
Figures 13.7b and 13.7c show the capacitor voltages of the converter. As most of the flying capacitors are floating, measurement probes are required to be placed across the capacitors rather than referencing them to the ground. Interestingly, capacitor voltages drift very slowly if

Table 13.1. List of components

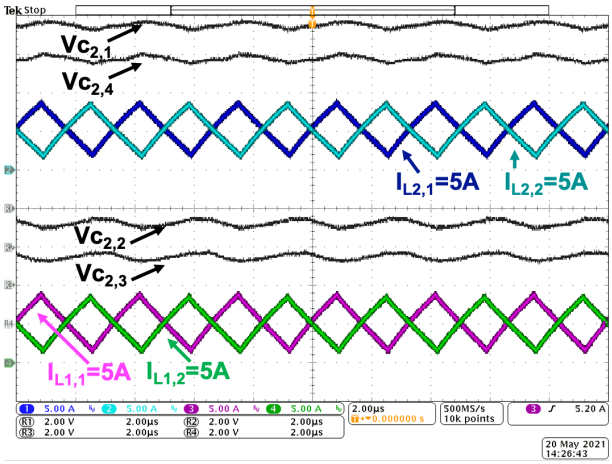
Components	Parts
S_{1-6}	40V MOSFET (Infineon)
C_{1-4}	2x1.4 ÂμF COG (KEMET)
Transformer	4:2 turn ratio with planar N97 ER32 core (EPCOS TDK)
$L_{1,2}$	560 nH (Coilcraft)
Gate driver	UCC5350MC



(a) Switching node voltage of the converter



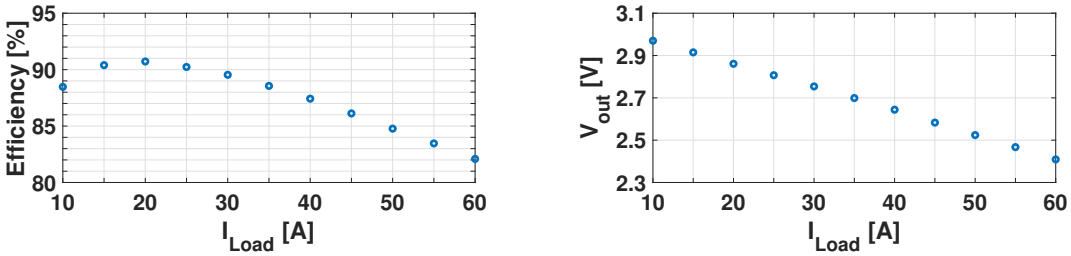
(b) Capacitor voltages of the first module



(c) Capacitor voltages of the second module

Figure 13.7. Multi-module DC-stack operation at a 100V-to-2.85V/20A operation

measured with any single-ended or even differential probe. The leakage in the voltage probes introduces some extra charge loss in the converter which is responsible for this drifting. To overcome this problem, two similar differential probes have been used to measure the similar type of capacitor voltages so that the leakages from both probes nullify the results drifting each other. During the measurements, the voltages of the first module's flying capacitors C_1 and C_4, and C_2 and C_3 have been measured together. The same procedure was applied to measure the voltages of the second module's C_1 and C_4, and C_2 and C_3. Figures 13.7b and 13.7c show the capacitor voltages are balanced in the steady-state operation.



(a) Converter efficiency **(b)** Output voltage

Figure 13.8. Measured performance of the modular converter prototype with two DC-stack modules at 100V input voltage

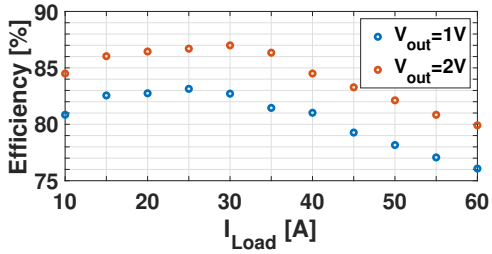


Figure 13.9. Measured efficiency of the converter at 100V input and regulated output voltages

The measured performance of the converter is provided in Fig. 13.8a with its efficiency. Figure 13.8b shows its measured output voltage versus output current to illustrate its output resistance and conduction loss. The converter reached a peak efficiency of 91% for a 100V-to-2.85V/20A conversion. The converter's maximum output current was measured at 60A while the converter obtains 2.41V output voltage and achieves 82.1% efficiency. The regulation capability of the converter is also shown in Fig. 13.9 with regulated outputs of 2V and 1V with 87% and 83.15% peak efficiencies at 30A and 25A respectively.

13.5 Chapter Summary

In summary, this chapter presents a new isolated hybrid converter architecture with a new input SC stage that can be combined with traditional isolated solutions, e.g., the current doubler rectifier, to exploit the full benefits of both large courses step-down by the SC stage and fine output regulation and isolation by the transformer and inductive stage. This SC circuit is

more advantageous compared with the traditional Dickson-based solution because the maximum capacitor voltage stress can be significantly reduced. To further reduce the capacitor voltage stress, the modular architecture of the converter module can be utilized. The modular operation also provides the benefits of partial power processing to reduce the power stress for each converter module. A proof-of-concept converter prototype was implemented and measured for the modular operation to support POL applications from 100V input. The modular operation reached a peak efficiency of 91% for 100V to 2.85V operation.

Chapter 13, in full, is a reprint of the material as it appears in "Modular Isolated Vertically Symmetric Dual Inductor Hybrid Converter For Differential Power Processing," in 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 2439-2443 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Note that, in the actual published paper, the term "Differential" was used where, in this dissertation, it has been replaced with "Partial" to match with the traditional use of both these terms. The context is the same.

Part VI

Multi-Output DC-DC Converters

Chapter 14

Multi-Inductor Multi-Output Hybrid (Mi-MoH) Converter for Large Conversion Ratio and Multiple Outputs

14.1 Introduction

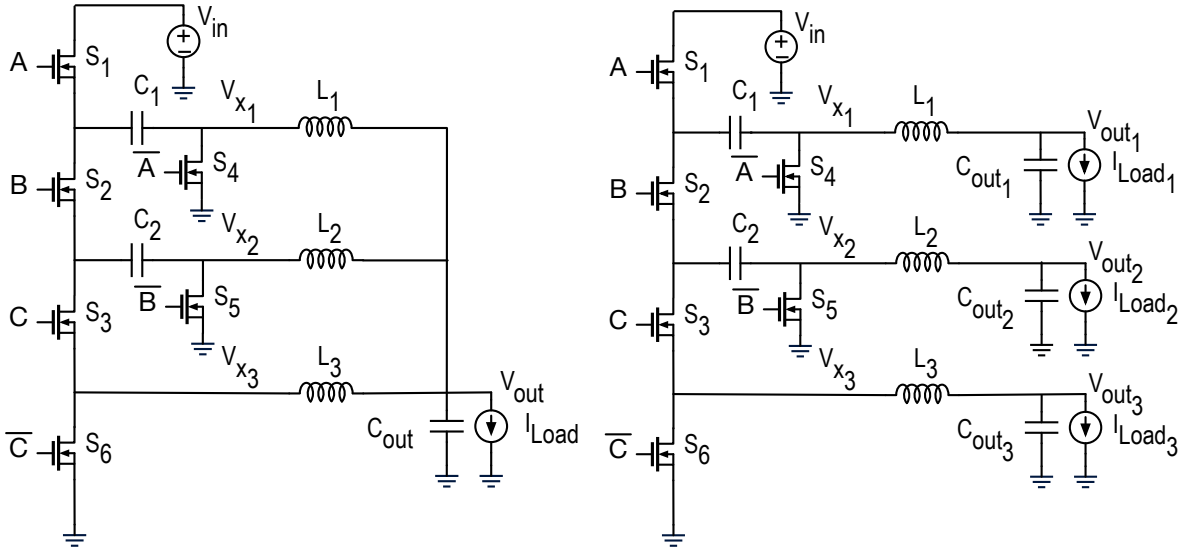
Each modern electronic appliance is a set of individual smaller electronic systems dedicated to more specific tasks. These smaller systems complement and coordinate with each other to finally serve the purpose of the whole system. In most cases, the whole system is powered by a single voltage source, while the smaller parts use different voltage rails for their operation. Modern televisions, mobiles, computers, etc., are examples of different power rails for processors, displays, memory, communication devices, and other individual functional blocks. Even within a processor chip, computation demands have driven the design to have multiple cores that require different voltage levels (in dynamic voltage and frequency scaling, or DVFS) and power to achieve optimal energy per computation efficiency.

To support these multiple voltage rails, the system power delivery often starts from a higher voltage level and uses either multiple high-voltage (HV) high conversion ratio converters or multiple stages comprised of a single HV converter followed by multiple low-voltage (LV) Buck converters. These solutions suffer from a deficiency in area utilization or low efficiency from the series connection of multiple stages. Therefore, it is desirable to seek a new converter

architecture that can deliver high conversion ratios while providing multiple outputs in a single converter stage. In literature, multi-output converters use transformers with multiple secondary windings for multiple outputs [123] or single inductor multiple outputs (SIMO) architectures with minimal voltage conversion capability [124–126]. In this chapter, we propose a switched capacitor-based hybrid converter to operate at a high conversion ratio and provide simultaneous multiple outputs. Section 14.2 describes the converter with its operation, and section 14.3 follows with the steady-state analysis. The converter hardware implementation and experimental verification are included in Section 14.4. The chapter is summarized and concluded in Section 14.5.

14.2 Proposed MiMoH Converter

Historically, Series Capacitor Buck (SCB) converter shown in Fig. 14.1a was proposed and demonstrated in [54], although the popular customary name was given in a later publication [52]. The same topology was also synthesized from the switched capacitor-based converter's perspective later in [15,17,41,49]. Following the synthesis of the series capacitor Buck converter



(a) SCB Converter **(b)** Proposed MiMoH Converter

Figure 14.1. Synthesis of the new topology

from a Dual inductor hybrid converter in [56], recent high current demonstrations for data center applications have been done with the favorable modification of the SCB converter [24, 57, 58]. The inductors in the SCB converter serve one output. However, we recognize that these inductors can be separated to provide multiple individual outputs, thus constructing the multi-inductor multi-output hybrid (MiMoH) converter. There can be multiple variations of MiMoH converter in terms of the number of levels, capacitors and their connections, inductors, and outputs [127]. However, in this work, we focus on the 3-level 3-inductor 3-output converter, shown in Fig. 14.1b, that can carry the essence of the MiMoH converter.

The proposed MiMoH converter has two flying capacitors $C_{1\text{-}2}$, three inductors $L_{1\text{-}3}$, and three pairs of switches ($S_{1,4}$, $S_{2,5}$, and $S_{3,6}$) working at three different phases A, B and C. Two complementary signals control two switches in a pair. The operation of the converter can be explained with the timing diagram in Fig. 14.2 and the converter states in Fig. 14.3. Three operating phases divide the switching period into six different converter states. In state 1 (Fig. 14.3a) when switch S_1 is on, inductor L_1 softly charges capacitor C_1 while also supplying the load at V_{OUT_1}. Similarly in state 3 (Fig. 14.3b), inductor L_2 discharges C_1, charges C_2, and

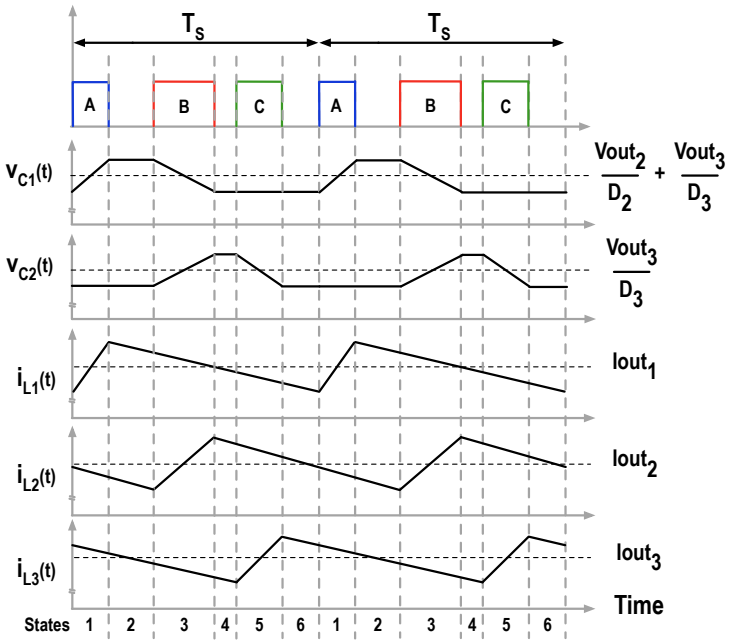
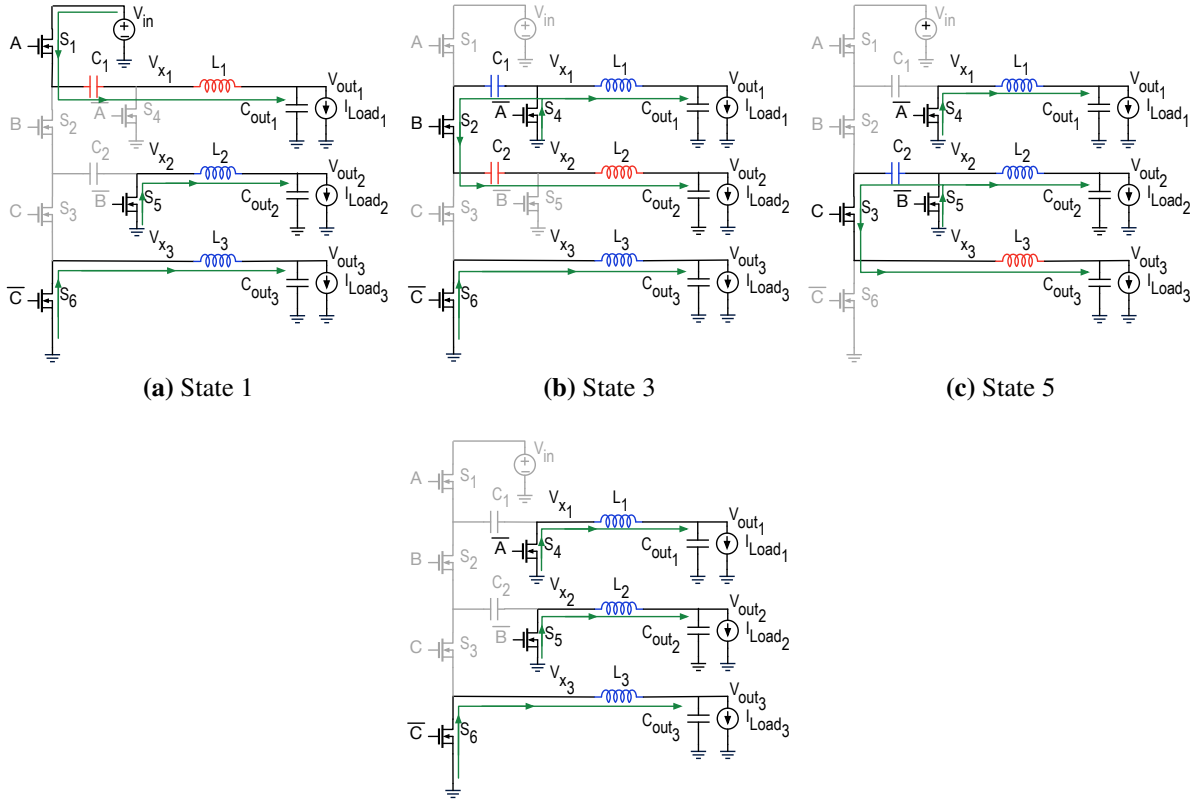


Figure 14.2. Timing diagram

supplies V_{OUT_2}. Then, inductor L_3 discharges C_2 to supply V_{OUT_3} in state 5. While in states 1, 3, and 5, one inductor current is charged, and the other two are discharged in freewheeling; all three inductors freewheel in states 2, 4, and 6. For normal operation, the non-overlapped operation needs to be maintained between states 1 and 3 and between states 3 and 5. The operating phases A, B, and C, corresponding to states 1, 3, and 5, can be arranged in any order or phase shifts as long as the non-overlap condition is satisfied. As three inductors serve the three outputs separately, the outputs can be regulated by the time the inductors get charged and thus, changing the slopes of the inductor currents.



(a) State 1 **(b)** State 3 **(c)** State 5

(d) State 2, 4 and 6

Figure 14.3. Operating states of the proposed MiMoH converter

14.3 Steady State Analysis

Assume the duty cycles of the phases A, B, and C are D_1, D_2, and D_3, respectively and voltages of capacitors $C_{1\text{-}2}$ are $V_{C_{1\text{-}2}}$. Applying the volt-second balance to the inductors, we can get the following relationships among input, output, and flying capacitor voltages:

$$V_{in} = \frac{V_{out_1}}{D_1} + \frac{V_{out_2}}{D_2} + \frac{V_{out_2}}{D_3},\ V_{C_1} = \frac{V_{out_2}}{D_2} + \frac{V_{out_3}}{D_3},\ and\ V_{C_2} = \frac{V_{out_3}}{D_3} \tag{14.1}$$

However, (14.1) does not provide information on how to regulate each output voltage individually. Thus, this converter breaks the norms of traditional pulse-width modulated (PWM) converters such as Buck, Boost, or even the parent SCB converter, [17, 54] where the duty cycle can be directly calculated by deriving the input to output conversion ratio from the volt-second balance. So, we need to look into other fundamental relationships.

Other ways to analyze a power converter are to use charge balance and/or power balance. In a switched capacitor-based converter, the same charge normally flows from one flying capacitor to another. This charge is directly linked to the output current. In the proposed MiMoH converter, the inductors can carry different currents to support their respective outputs, or I_{L_i}=I_{out_i}. These currents charge and discharge flying capacitors $C_{1\text{-}2}$ during states 1, 3, and 5. For simplicity in analysis, second-order effects from the L-C interaction listed in [19] are considered insignificant. Thus, the inductor currents are assumed to charge and discharge with constant slopes. Hence, applying the charge balance on $C_{1\text{-}2}$, we get the following relationship:

$$I_{out_1} D_1 = I_{out_2} D_2 = I_{out_3} D_3 \tag{14.2}$$

We can also write the theoretical power balance equation in the converter and apply (14.2):

$$P_{in} = P_{out} = P_{out_1} + P_{out_2} + P_{out_3} \tag{14.3}$$

$$V_{in}I_{in} = V_{in}I_{out_1}D_1 = V_{in}I_{out_2}D_2 = V_{in}I_{out_3}D_3 = V_{out_1}I_{out_1} + V_{out_2}I_{out_2} + V_{out_3}I_{out_3} \tag{14.4}$$

From (14.4), the duty cycles for the three phases can be calculated to have relationships with different voltages, currents, and power for different outputs as follow:

$$D_1 = \frac{V_{out_1}}{V_{in}} + \frac{V_{out_2}}{V_{in}}\frac{I_{out_2}}{I_{out_1}} + \frac{V_{out_3}}{V_{in}}\frac{I_{out_3}}{I_{out_1}} = \frac{V_{out_1}P_{out}}{V_{in}P_{out_1}} \tag{14.5}$$

$$D_2 = \frac{V_{out_1}}{V_{in}}\frac{I_{out_1}}{I_{out_2}} + \frac{V_{out_2}}{V_{in}} + \frac{V_{out_3}}{V_{in}}\frac{I_{out_3}}{I_{out_2}} = \frac{V_{out_2}P_{out}}{V_{in}P_{out_2}} \tag{14.6}$$

$$D_3 = \frac{V_{out_1}}{V_{in}}\frac{I_{out_1}}{I_{out_3}} + \frac{V_{out_2}}{V_{in}}\frac{I_{out_2}}{I_{out_3}} + \frac{V_{out_3}}{V_{in}} = \frac{V_{out_3}P_{out}}{V_{in}P_{out_3}} \tag{14.7}$$

In a voltage converter, the most important feature would be regulating the right output voltage(s). As shown in (14.5)-(14.7), controlling the duty cycle to regulate an output voltage in the MiMoH converter depends on the power requirement of other outputs. This behavior has an impact on the flying capacitor voltages. At the converter switching frequency, flying capacitors can be considered voltage sources. While the input is the power source for all three outputs, capacitor C_1 acts as an intermediate power source for V_{out_2} and V_{out3}, and capacitor C_2 as an intermediate power source for V_{out_3}. As the input voltage is constant, the flying capacitor voltages need to move around to accommodate the power increase or decrease in different outputs. This behavior of the flying capacitor voltages can be modeled by modifying the equations of (14.1) using (14.5)-(14.7) as follows:

$$V_{C_1} = \frac{V_{in}\left(P_{out_2} + P_{out_3}\right)}{P_{out}},\ and\ V_{C_2} = \frac{V_{in}P_{out_3}}{P_{out}} \tag{14.8}$$

Note that the flying capacitor voltages in the MiMoH converter are fully predictable based on (14.8), and do not suffer from the known balancing issue of 3-level Buck converter [19, 98].

14.4 Experiment Results

A proof-of-concept prototype of the converter, shown in Fig. 14.4, was built using the components listed in Table 14.1. GaN devices have been used to implement all the power switches in the converter. The cascaded bootstrap technique is applied to power gate driving circuits [18]. The measured waveforms of the converter are shown in Figs. 14.5a and 14.5b, proving its intended stable operation. These waveforms are taken at 24V to simultaneous three regulated output operations at 1.5V/5A, 1.8V/5A, and 1.2V/5A. It can be seen from Fig. 14.5b that the flying capacitors are softly charged and discharged by the inductors. The switching node voltages $V_{x_{1\text{-}3}}$ have different swings as they support different output voltages. $V_{x_{1\text{-}3}}$ levels can be calculated from the flying capacitor voltages in 14.8. The inductor currents are at the same DC levels as the output currents.

There can be numerous settings of output voltages and power that the MiMoH converter can support. In this chapter, we include measured performances of the converter in several example combinations for output voltages from 1.2V to 2.2V in Fig. 14.6 and 14.7. Figures 14.6a-14.6c show the performance of the converter with different combinations of output voltages 1.2V, 1.5V, and 1.8V from an input voltage of 24V, achieving a peak efficiency of 91.8%. Figure

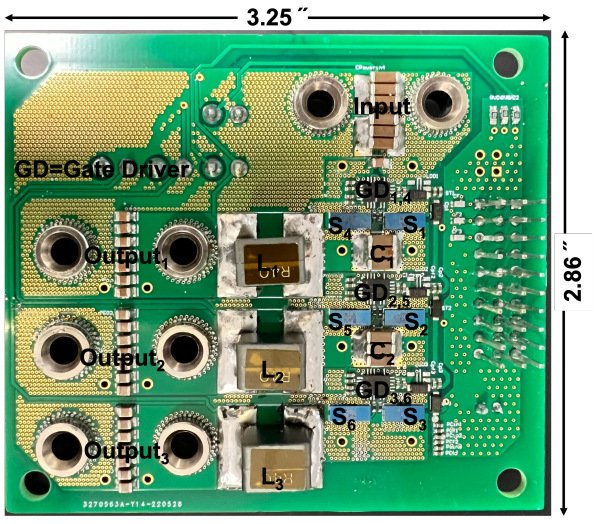


Figure 14.4. Prototype of the converter

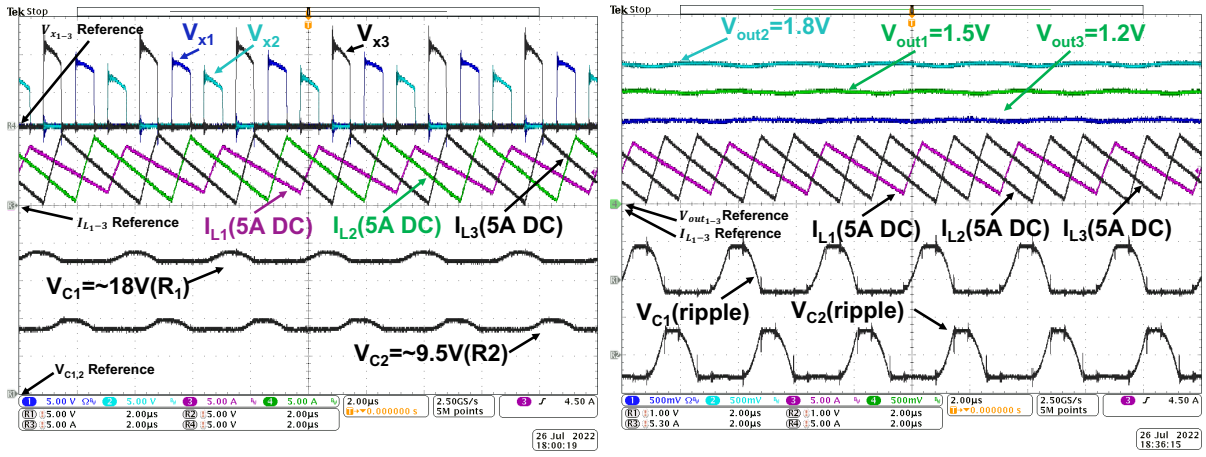
Table 14.1. Components used in MiMoH converter

Components	Part Number
$Sw_{1\text{-}3}$	60V EPC2020
$Sw_{4\text{-}6}$	30V 2xEPC2023
$C_{1\text{-}5}$	2x1.4uF 50V C1812C145J5JLC7805
$L_{1\text{-}3}$	400nH VLBU1007090T-R40L
Gate Driver	LMG1210

14.7 shows the efficiency measurement at 48V input voltage and 2.2V, 1.8V, and 2V output voltages. In this operating condition, the converter achieves 88.9% efficiency. The peak power delivered by this converter in this set of measurements is 40W.

During all these measurements, a control loop was employed to robustly regulate output voltages in an automated manner for all the conditions of output current, voltage, and power levels. This control loop was designed based on equations (14.5)-(14.7)[1].

[1]A discussion on the controller is included in Appendix J.



(a) Switching node voltages and inductor currents with DC coupled flying capacitor voltages

(b) Output voltages and inductor currents with AC coupled flying capacitor voltages

Figure 14.5. Measured waveforms at 24V to simultaneous 1.2V/5A, 1.5V/5A, and 1.8V/5A operation

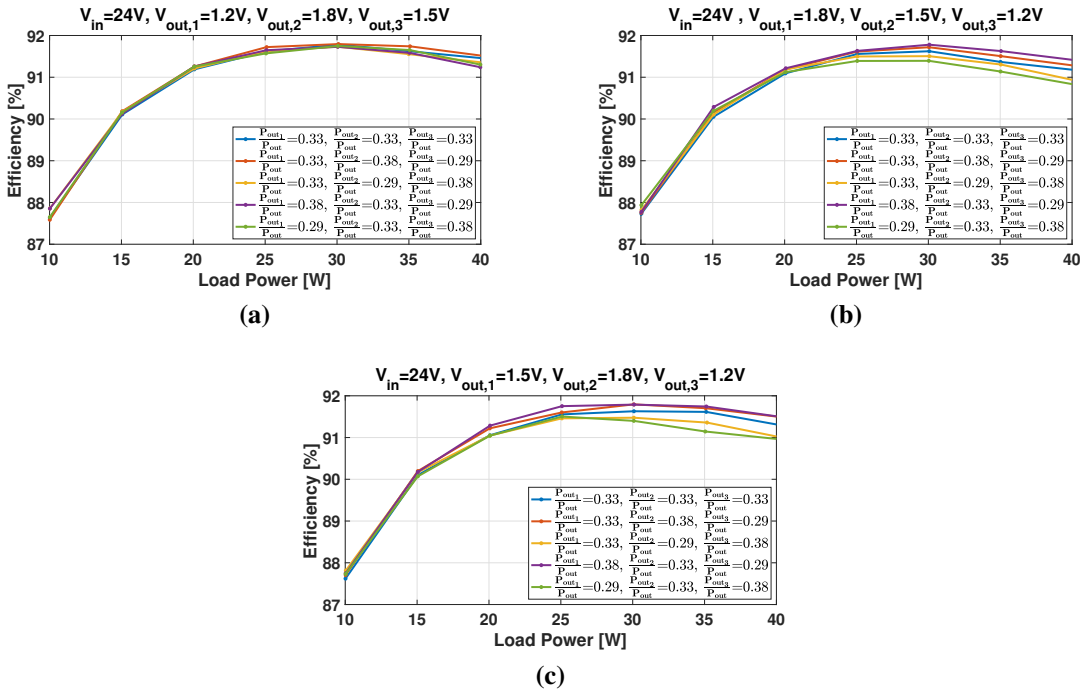


Figure 14.6. Performance of the converter at 24V input

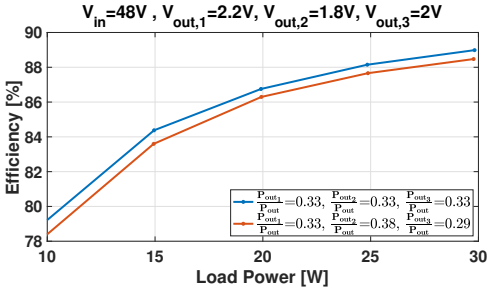


Figure 14.7. Performance of the converter at 48V input

14.5 Chapter Summary

A high conversion ratio multi-inductor multi-output hybrid (MiMoH) converter has been proposed and demonstrated in this chapter. Experimental results prove the intended operation and validate the analysis of the converter. This is the first demonstration of a converter achieving a high conversion ratio while providing multiple outputs without a transformer. MiMoH converter extends the application spectrum of switched capacitor-based hybrid converters to a broader range.

Chapter 14, in full, is a reprint of the accepted materials in "Multi-Inductor Multi-Output Hybrid (MiMoH) Converter for Large Conversion Ratio and Multiple Outputs," in 2023 Applied Power Electronics Conference and Exposition (APEC), 2023 by the authors Das, Ratul and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Chapter 15

Conclusions

15.1 Thesis Summary

Energy usage is a good metric for determining which nation has advanced further in science, technology, and human lifestyle. Standing amid the fourth industrial revolution, we are on the verge of a rapid expansion of energy usage. It is high time we find new energy sources, use more renewable energy, and invent new technologies to harness more power and use them efficiently. As electricity is the primary form of energy that can be used with devices, appliances, instruments, and vehicles for human comforts and industrial automation and is suitable to transmit to a distant and remote location easily, it is and always will be relevant in the grand scheme of things. Electrical and electronic appliances can not directly consume electricity if it is not processed in specific ways. These processes involve DC-DC and AC-DC power conversions. All these processes require the applications of power electronics. The time has come to broaden power electronics applications and develop integrated and miniaturized power converters suitable for next-generation devices, appliances, and technologies.

This dissertation included many problems and solutions in diversified power electronics and power management applications. The work is themed on power delivery applications for data centers and telecommunication systems. A significant portion of the dissertation is focused on designing switched-capacitor (SC) based multilevel DC-DC and AC-DC hybrid converters targeting high conversion ratios for data center applications. Besides, synthesis, modeling,

and control techniques for new and old hybrid power converters are introduced, discussed, and analyzed. The final goal of the dissertation is to use the knowledge to build miniaturized power converters that are more efficient, compact, and controllable. The studies conducted are interchangeable with most modern electronic applications.

In the DC-DC applications category, it has been shown that if inductors can be strategically placed in the switched capacitors converters, they eliminate the capacitor-to-capacitor charging losses. It is easier to achieve a high conversion ratio, high current, and seamless control if multiple capacitors and inductors are combined for power processing. The capacitors can block high voltages, and multiple inductors help supply high currents at the output. The research introduced a new multi-inductor hybrid (MIH) family. Multiple demonstrations are included in this dissertation. One implementation achieved a record $> 1kA/in^3$ current density at 48V-to-1V conversion. Multiple demonstrations achieved $> 94\%$ efficiency for a range of operating conditions.

In the AC-DC applications research, an SC structure has been used that can provide an inherent step down while helping the power factor correction (PFC). A hybrid SC converter in this application reduces the inductance at the input for current shaping and increases system efficiency with the usage of low voltage switches and low voltage higher density distributed buffer capacitors. As a result, the system achieved $> 96\%$ efficiency and > 0.995 power factor while operating 3x or 4x times smaller output voltages.

It has also been demonstrated that by using hybrid SC converters for AC to 48V front end and 48V to 1V back end, it is possible to deliver the necessary power to the core processors in the data centers in a minimum number of stages. It was one of the first demonstrations to show the two-stage power delivery architecture for a full AC-to-core level power delivery.

While working on DC-DC converters, two fundamental problems related to SC-based hybrid converters were encountered. First, hybrid converters were infamous for balancing issues. Previously, there was no universal method of identifying converters with balancing issues. Using a straightforward mathematical model, a method has been devised to determine if a hybrid

converter is balanced or unbalanced. The method can help future engineers by reducing the workload of complex mathematical analysis to a straightforward parity-based counting method.

The other significant problem was the determination of the small signal model for controlling these hybrid converters. Recently synthesized switched capacitor-based multilevel converters have more inductors, capacitors, and many switches. Employing the average switching method, it has been shown that the new MIH converter family demonstrated in this dissertation behaves like simple second-order filters or Buck converters and can be controlled similarly. This knowledge simplifies the design of the feedback loops of these hybrid SC-based converters significantly.

Differential power processing is one of the most effective solutions to distribute the load on various converters, hence, designing a more efficient and compact system-level solution. differential power processing involves using multiple modules and dividing the input voltages of each module into a smaller value by series connecting the modules' inputs. Most of the previous implementations of differential power processing only considered DC-DC applications. In this dissertation, it has been shown that multiple AC-DC converters can also be stacked together to share the input voltage and power and thus benefit from differential power processing. This way, the AC-DC and DC-DC conversion stages can be simplified with one stage, and stepped-down DC voltage can also be extracted from the structure. DC-DC differential power processing has also been visited to highlight that using SC structures as the front end can nullify the requirement of controlling each module's input voltage actively.

Last but not least, a multi-output high conversion ratio converter has been demonstrated. Having the same structure for multiple outputs saves semiconductor and board area and thus can reduce the overall implementation cost of future power management units. Interestingly, a simple change in the original converter can generate multiple outputs. Experimental results and control techniques have also been included.

15.2 Future Directions

The semiconductor industry has followed Moore's law for more than fifty years and has reached the seeming limit in recent years. The U.S. Department of Energy (DOE) is urging researchers from industry and academia to come forward to establish Moore's law in power electronics as well as target to increase energy efficiency or decrease the power loss to over a thousand times within the next two decades [128]. The author also believes that despite many innovations and improvements in the power electronics field, power delivery systems are the bottlenecks of many high-performance systems. Next few years, we will see a lot of improvements in the power delivery technologies involving architecture, topologies, and control techniques. New ideas, philosophies, and goals will be considered to apply the knowledge of power electronics in a broader spectrum of applications.

The hybrid topologies and architectures presented in this dissertation can be excellent candidates for multiple stages of power deliveries in space applications. The power converters and associated circuits in space applications must be tolerant of radiation, and extreme heat and cold conditions [129]. Using wide band gap radiation tolerant devices for building the hybrid switched-capacitor (SC) converters, including the gate driving circuits and controllers, can be one direction for exploration. Using hybrid SC converters can also potentially reduce the requirement of magnetic elements and hence, the overall weight of the power delivery systems in space applications.

Wide-scale use of solar energy requires renovating the existing AC grid to accommodate high-voltage DC and, in some cases, totally replacing the AC grid with DC. In addition, high voltage grid connection and power delivery to electrical appliances require new high conversion ratio converters. From the works of this dissertation, SC-based multilevel hybrid converters have been proven effective in high conversion ratio applications. The next step can be nor identification, analysis and design of suitable multilevel converters for solar energy conversion applications.

The research on high voltage generation was motivated by tearing up atoms into particles and accelerating them for collisions to break into more fundamental particles. With newer applications on the horizon, particle accelerators will be more frequent [130]. Accelerators are already common in the lithography process and radio-isotope generation. We need low-cost, space-efficient, smaller energizing power converters to reflect the advantages on the accelerator side. Using SC-based high-frequency DC-DC and AC-DC converters can make a difference in the power management of this application.

The United States will operate only with carbon-neutral vehicles in the coming decades. Many states are already taking the initiative of banning fossil fuel-based vehicles within the next few years. Any car has many electronic appliances for safety and control. There are power converters in the power train and battery management systems as well. Furthermore, future electric cars need to be more powerful and efficient in energy usage. In that regard, research is being conducted to build more efficient electric motors. The applications of hybrid SC converters have the potential to make breakthroughs in the optimization of powertrains and inverters for motors.

The manufacturers tend to increase the battery voltages of electric vehicles from 400V to 800V or even 1200V so that the batteries can be charged quickly using the same amount of current. Relatively infant charging infrastructure needs to be accommodating to these ongoing changes. There are requirements for high-power chargers and their grid integration with high-voltage AC-DC and DC-DC Converters. High-frequency hybrid SC converters with wide band gap devices can make these converters smaller and more efficient.

Battery chargers are required to provide two functionalities, constant voltage (CV) and constant current (CC) mode operation. While CV mode operation is ubiquitous for most power converters, CC operation can be naturally found primarily in resonant converters. One discovery made and included in this dissertation is that pulse width modulated (PWM) hybrid SC converters can also be naturally operated in the CC mode. Therefore, the possibilities of these hybrid converters' high-power CC mode operation must be evaluated. At the same time,

these converters can also be good candidates for low-power LED driver applications because of their excellent current source behavior for brightness control and fast response.

The current household and domestic power delivery using single-line 110VAC and double-line 220VAC are unsafe for humans. Future smart homes should accommodate DC microgrids within each house, and the socket voltages should also be reduced to a level suitable for human safety. Following up on this idea, as most electronic appliances run with DC power, low-voltage DC microgrids can help remove the use of separate AC-DC power converters in each appliance. Instead of AC wall sockets, there can be USB-C or more standardized ports in the walls to deliver power. A lot of research directions can be explored for the power delivery of smart devices in smart homes. All these low-voltage DC sockets at the walls must be powered up from either high-voltage AC distribution voltage or high-voltage DC distribution voltage. The design of hybrid SC power converters for safety-rated operation and synchronization of the control among multiple modules connected to the same microgrid can be a good direction for future research.

The author also believes that unless there is any fundamental limit, for example, safety or cooling, all relatively low voltage and low power converters will be integrated in the future. Power management in ICs will receive more interest in a few years, and industries will focus on building a complete system of high-performance loads, such as digital systems and power converters. Many power converters presented in this dissertation are suitable for future integration. A more focused study is required to analyze the feasibility of these converters for different applications and finally integrate them. Besides, using integrated passive components in the ICs and packages or even at the board level can potentially boost these systems' power density. Future research can study the coordinated design of power converters and passive components as well.

Appendix A

General Capacitor Sizing Method for Multi Inductor Hybrid Converter Family

In any converter, capacitors should be chosen according to the amount of maximum voltage ripple that can be allowed on that capacitor. All the flying capacitors within the MIH converter family should also be chosen to maintain the same principle. For proper operation, all these flying capacitances should be chosen so that the capacitor voltage levels can be maintained higher than their immediate lower or lower than their immediate higher capacitor voltage levels. This criterion provides the minimum capacitance requirement for each capacitor. Depending on the allowable voltage ripples, the capacitance needs to be even sized larger. For any particular MIH converter, all the flying capacitors carry the same charge while charging or discharging. Considering that, this is customary that all the capacitances in a particular converter are sized equally. But, this leads to residual hard-charging in some converters, especially dual inductor converters (Fig. 5.2a [41] and 5.2b [15]) or multi-inductor hybrid converters with multiple capacitor branches connected with each inductor 5.2d [16]. The basic principles of capacitor sizing have been previously included in [15] on only dual inductor hybrid converters. For these converters, capacitor sizing can be applied if it is not desired to move to other converters for residual hard-charging less operation. We have included a general solution for capacitor sizing. For an L level m-inductor converter with $(L-1)$ number of capacitors where $L \geq m$, n is the

Table A.1. Capacitor sizing strategy

Conditions	Capacitor Sizing	Example
$L = m$	$C_d = C$, where, $d \leq L-1$	Series Capacitor Buck Converter of any level
$L = m(n-1)+k$, where, m is odd, $n = 2$, k is odd and $k \leq m$	$C_{k,m,m+1} = 2C$, if $k > 1$, $C_m = C$, if $k = 1$, $C_d = C$, if $k < d < m$, $C_d = C_{m+1+d} = C$, if d is odd and $d < k-1$ $C_d = C_{m+1+d} = 2C$, if d is even and $d \leq k-1$	3-inductor 4/6 level converter, 5-inductor 6/8/10 level converter
$L = m(n-1)+k$, where, m is odd, $n = 2$, k is even and $k <= m-1$	$C_m = \infty$ $C_d = C$, if $k < d < m$, $C_d = C_{m+d} = C$, if d is odd and $d < k$ $C_d = C_{m+d} = \infty$, if d is even and $d \leq k-2$	3-inductor 5 level converter, 5-inductor 7/9 level converter
$L = m(n-1)+k$, where, $n >= 2$, m is even, k is odd and $k < m$	$C_d = \frac{L-1}{L-d}C$, *when d is an odd number*, $C_d = \frac{L-1}{d}C$, *when d is an even number*, $C_d = C_{L-d}$, *where*, $d = 1,2,...,\ \frac{L-1}{2}$	Odd level DIHC, 4-inductor 5/7/9 level, 6 inductor 7/9/11/13 level
$L = m(n-1)+k$, where, $n >= 2$, and m and k is even, and $k \leq m$	$C_{mp} = C_{m(p-1)+d} = \infty$, where, $p = 1,2,...n$ and $d = 2,4,...k-2$. All other capacitance can be chosen as C.	Even level DIHC, 4-inductor 6/8/10 level converter, 6-inductor 8/10 level
$L = m(n-1)+k$, where, $n > 2$, m is odd, n is even and k is odd	$C_d = C$, if d is odd, $C_d =$, if d is even,	3-inductor 10 level, 5-inductor 18 level converter
$L = m(n-1)+k$, where, $n > 2$, m is odd, n is even and k is even	No solution (At least one needs to be negative)	3-inductor 11 level, 5-inductor 17 level converter
$L = m(n-1)+k$, where, $n > 2$, m is odd, n is odd and k is even	$C_d = C$, if d is odd, $C_d =$, if d is even	3-inductor 8 level, 5-inductor 14 level converter
$L = m(n-1)+k$, where, $n > 2$, m is odd, n is odd and k is odd	No solution (At least one needs to be negative)	3-inductor 7 level, 5-inductor 3 level

highest number of capacitor branches connected with any inductor, and k is the number of inductors with $n-1$ number of capacitor branches, capacitance sizing can be done according to Table A.1.

Appendix A contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix B

Inductor Current Equalization of Multi-Inductor Hybrid Converters

In any multi-inductor hybrid (MIH) converter, each flying capacitor charges and discharges with the same charge. If the capacitor branches are activated for the same time, they carry the same current on average during their activation time. However, many of the MIH converters have a different number of capacitor branches connected with different inductors. If the same on-time for their charging is used, which is the typical case, the DC level of the inductor currents becomes different. Previously it has been shown with an odd DIH converter, and a method of equalizing the DC levels has been demonstrated in [15]. Current equalization is useful when the DC conduction loss in the inductor is the dominant loss in the converter and the load. The switch selection allows capacitor voltage levels to shift slightly from their ideal levels. A discussion on current equalization for any MIH converter is provided here.

B.0.1 Current Equalization in General MIH converters

If any member converter of the converter has unequal inductor currents, there can only be two sets of inductors with different currents. For a converter with the level number $L = m(n-1)+k$, where m is the number of inductors in the converter, assume the two sets are A and B set, and the inductors of set A are each connected with n number of capacitor branches, while the inductors of set B each are connected with $n-1$ number of capacitor branches. That also means that there

are k inductors in set A and $(m-k) inductors in set B. Now, if Q amount of charge is flowing through each of the capac$

$$I_{L_A} = \frac{nQ}{D_A T_S} \text{ and } I_{L_A} = \frac{(n-1)Q}{D_B T_S} \tag{B.1}$$

In Eqn. B.1, D_A and D_B are the duty cycles of each phase associated with the inductor charging. Normally, these duty cycles are equal or $D_A = D_B = D$. Assuming D_A and D_B are different and not equal to D, the input to output relationship becomes

$$V_{out} = \frac{V_{in}}{\frac{nk}{D_A} + \frac{(m-k)(n-1)}{D_B}} \tag{B.2}$$

Here, our goal is to modify the duty cycles D_A and D_B so that the currents are equal and the converter still generates the same output described by the typical input-output relationship. The conditions can be written as follows:

$$\frac{DV_{in}}{m(n-1)+k} = \frac{V_{in}}{\frac{nk}{D_A} + \frac{(m-k)(n-1)}{D_B}} \tag{B.3}$$

$$\frac{nQ}{D_A T_S} = I_{L_A} = \frac{(n-1)Q}{D_B T_S} = I_{L_B} \tag{B.4}$$

Modified duty cycles can be calculated from these equations as follow:

$$D_A = \frac{mn}{m(n-1)+k} D \text{ and } D_B = \frac{m(n-1)}{m(n-1)+k} D \tag{B.5}$$

B.0.2 Current Equalization in Optimal MIH Converters

For the optimal inductor hybrid converter, the current of the first and last inductors is much smaller than the other two inductors. They can be chosen with lower saturation current inductors. However, if any design constraint forces the currents of every inductor to be the same, the following methods can be followed.

Assume the converter has an L number of levels. The method can vary slightly depending on whether L is odd or even.

Even Level Optimal MIH Converter

Equation B.1, B.3, B.4 and B.5 can be re-written for Even Level Optimal MIH Converter as follow:

$$I_{L_{1,4}} = \frac{Q}{D_{1,4}T_S} \; and \; I_{L_{2-3}} = \frac{\frac{L-2}{2}Q}{D_{2,3}T_S} \tag{B.6}$$

$$\frac{DV_{in}}{L} = \frac{V_{in}}{\frac{2}{D_{1,4}} + \frac{L-2}{D_{2,3}}} \tag{B.7}$$

$$\frac{Q}{D_{1,4}T_S} = \frac{\frac{(L-2)}{2}Q}{D_{2,3}T_S} \tag{B.8}$$

$$D_{1,4} = \frac{4}{L}D \; and \; D_{2,3} = \frac{2\,(L-2)}{L}D \tag{B.9}$$

Odd Level Optimal MIH Converter

Equation B.1, B.3, B.4 and B.5 can be re-written for Odd Level Optimal MIH Converter as follow:

$$I_{L_{1,4}} = \frac{Q}{D_{1,4}T_S}, \; I_{L_2} = \frac{\frac{L-1}{2}Q}{D_2T_S} \; and \; I_{L_3} = \frac{\frac{L-3}{2}Q}{D_3T_S} \tag{B.10}$$

$$\frac{DV_{in}}{L} = \frac{V_{in}}{\frac{2}{D_{1,4}} + \frac{\frac{L-1}{2}}{D_2} + \frac{\frac{L-3}{2}}{D_3}} \tag{B.11}$$

$$\frac{Q}{D_{1,4}T_S} = \frac{\frac{L-1}{2}Q}{D_2T_S} = \frac{\frac{L-3}{2}Q}{D_3T_S} \tag{B.12}$$

$$D_{1,4} = \frac{4}{L}D, \; D_2 = \frac{2\,(L-1)}{L}D \; and \; D_3 = \frac{2\,(L-3)}{L}D \tag{B.13}$$

Appendix B contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix C

Output Resistance of the MIH Converters

While designing power converters, output resistance is a very important parameter. Designers try to minimize the output resistance as it directly contributes to the efficiency of the converters. It is also of interest to determine the output resistances of the MIH Converter family. Employing the average model, the output resistances have been calculated and listed for several MIH converters in Table C.1.

Table C.1. Output resistance of MIH converter family

Converter	Rout
General MIH	$\left(\frac{1}{m(n-1)+k}\right)^2 \sum_{i=1}^{m(n-1)+k}\left(D_i R_{hon,i}\right) + \left(\frac{n}{m(n-1)+k}\right)^2 \sum_{i=1}^{k}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right]$ $+\left(\frac{n-1}{m(n-1)+k}\right)^2 \sum_{i=1}^{m-k}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right]$
MPDIHC	$\frac{1}{L^2}\sum_{i=1}^{L}\left(D_i R_{hon,i}\right) + \frac{1}{4^2}\sum_{i=1}^{2}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right]$
SCB	$\frac{1}{L^2}\sum_{i=1}^{L}\left(D_i R_{hon,i}\right) + \frac{1}{L^2}\sum_{i=1}^{L}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right]$
Optimal (even)	$\frac{1}{L^2}\sum_{i=1}^{L}\left(D_i R_{hon,i}\right) + \frac{1}{L^2}\left[(1-D_1)R_{lon,1}+R_{ind,1}+(1-D_L)R_{lon,L}+R_{ind,L}\right]$ $+\frac{(L-2)^2}{4L^2}\sum_{i=2,4,..}^{L-2}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right] + \frac{(L-2)^2}{4L^2}\sum_{i=3,5,..}^{L-1}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right]$
Optimal (odd)	$\frac{1}{L^2}\sum_{i=1}^{L}\left(D_i R_{hon,i}\right) + \frac{1}{L^2}\left[(1-D_1)R_{lon,1}+R_{ind,1}+(1-D_L)R_{lon,L}+R_{ind,L}\right]$ $+\frac{(L-1)^2}{4L^2}\sum_{i=2,4,..}^{L-1}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right] + \frac{(L-3)^2}{4L^2}\sum_{i=3,5,..}^{L-2}\left[(1-D_i)R_{lon,i}+R_{ind,i}\right]$

Appendix C contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix D

General Model of Series Connected Inductor Currents and Capacitor Voltages

Capacitor discharging:

Initial condition,

$$v_C(0) = V_C + \frac{Q}{2C} \tag{D.1}$$

Final condition,

$$v_C(DT_S) = V_C - \frac{Q}{2C} \tag{D.2}$$

Time domain state equation for capacitor voltage,

$$v_C(t) = (V_C + \frac{Q}{2C})cos(\frac{t}{\sqrt{LC}}) + \frac{(V_C - \frac{Q}{2C}) - (V_C + \frac{Q}{2C})cos(\frac{DT_S}{\sqrt{LC}})}{sin(\frac{DT_S}{\sqrt{LC}})} sin(\frac{t}{\sqrt{LC}}) \tag{D.3}$$

Average capacitor voltage,

$$V_{av(discharge)} = \frac{1}{DT_S} \int_0^{DT_S} v_C(t)dt = \frac{2(1 - cos\frac{DT_S}{\sqrt{LC}}))}{\frac{DT_S}{\sqrt{LC}} sin(\frac{DT_S}{\sqrt{LC}})} V_C = bV_C \tag{D.4}$$

Time domain state equation for inductor current,

$$i_L(t) = -\frac{C}{\sqrt{LC}}\left[-(V_C + \frac{Q}{2C})sin(\frac{t}{\sqrt{LC}}) + \frac{(V_C - \frac{Q}{2C}) - (V_C + \frac{Q}{2C})cos(\frac{DT_S}{\sqrt{LC}})}{sin(\frac{DT_S}{\sqrt{LC}})}cos(\frac{t}{\sqrt{LC}})\right] \quad \text{(D.5)}$$

Median inductor current,

$$I_L = \frac{i_L(0) + i_L(DT_S)}{2} = \frac{I_{av}}{b} \quad \text{(D.6)}$$

Inductor current ripple,

$$\triangle i_L = i_L(DT_S) - i_L(0) = bV_C\frac{DT_S}{L} \quad \text{(D.7)}$$

Capacitor charging:

Initial condition,

$$v_C(0) = V_C - \frac{Q}{2C} \quad \text{(D.8)}$$

Final condition,

$$v_C(DT_S) = V_C + \frac{Q}{2C} \quad \text{(D.9)}$$

Time domain state equation for capacitor voltage,

$$v_C(t) = 2V_C - \left(V_C + \frac{Q}{2C}\right)cos\left(\frac{t}{\sqrt{LC}}\right) - \frac{\left(V_C - \frac{Q}{2C}\right) - \left(V_C + \frac{Q}{2C}\right)cos\left(\frac{DT_S}{\sqrt{LC}}\right)}{sin\left(\frac{DT_S}{\sqrt{LC}}\right)}sin\left(\frac{t}{\sqrt{LC}}\right) \quad \text{(D.10)}$$

Average capacitor voltage,

$$V_{av(charge)} = \frac{1}{DT_S}\int_0^{DT_S} v_C(t) = (2-b)\,V_C = aV_C \quad \text{(D.11)}$$

Appendix D, in partial, is a reprint of the material as it appears in "Demystifying Capacitor Voltages and Inductor Currents in Hybrid Converters," in 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8 by the authors Das, Ratul, Celikovic, Janko; Abedinpour, Siamak; Mercer, Mark; Maksimovic, Dragan and Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

Appendix E

Derivation of Voltage-Charge Relationship for $V_{out} < \frac{V_{in}}{N}$

A voltage-charge relationship can be derived from the relationships of median currents $I_{L(k-2)}$, $I_{L(k)}$ and $I_{L(k+2)}$ of the inductor in charging intervals $D_{k-2}T_S$, D_kT_S and $D_{k+2}T_S$ in Fig. 9.2. If the peak currents of the intervals $D_{k-2}T_S$ and D_kT_S are $I_{L,f(k-2)}$ and $I_{L,f(k)}$, and the valley currents of the intervals D_kT_S and $D_{k+2}T_S$ are $I_{L,i(k)}$ and $I_{L,i(k+2)}$, it can be written that,

$$\begin{aligned} I_{L(k)} &= \frac{I_{L,i(k)} + I_{L,f(k)}}{2} \\ &= \frac{\left\{I_{L,f(k-2)} - \frac{V_{out}}{L}D_{k-1}T_S\right\} + \left\{I_{L,i(k+2)} + \frac{V_{out}}{L}D_{k+1}T_S\right\}}{2} \\ &= \frac{\left(I_{L(k-2)} + \frac{b_{k-2}(V_{k-2}-V_{out})}{2L}D_{k-2}T_S\right) - \frac{V_{out}}{L}D_{k-1}T_S}{2} + \frac{\left(I_{L(k+2)} - \frac{b_{k+2}(V_{k+2}-V_{out})}{2L}D_{k+2}T_S\right) + \frac{V_{out}}{L}D_{k+1}T_S}{2} \\ &= \frac{I_{L(k-2)} + I_{L(k+2)}}{2} + \frac{T_S}{4L}\left\{b_{k-2}D_{k-2}\left(V_{k-2} - V_{out}\right) - b_{k+2}D_{k+2}\left(V_{k+2} - V_{out}\right)\right\} - V_{out}\frac{T_S}{2L}\left(D_{k-1} - D_{k+1}\right) \end{aligned} \tag{E.1}$$

If we replace $I_{L(k)} = \frac{Q_k}{b_kD_kT_S}$, $I_{L(k-2)} = \frac{Q_{k-2}}{b_{k-2}D_{k-2}T_S}$ and $I_{L(k+2)} = \frac{Q_{k+2}}{b_{k+2}D_{k+2}T_S}$ in Eqn. E.1, it can be rewritten as,

$$\begin{aligned} \frac{Q_k}{b_kD_kT_S} = \frac{1}{2}\left(\frac{Q_{k-2}}{b_{k-2}D_{k-2}T_S} + \frac{Q_{k+2}}{b_{k+2}D_{k+2}T_S}\right) + \frac{T_S}{4L}\left\{b_{k-2}D_{k-2}\left(V_{k-2} - V_{out}\right) - b_{k+2}D_{k+2}\left(V_{k+2} - V_{out}\right)\right\} \\ - V_{out}\frac{T_S}{2L}\left(D_{k-1} - D_{k+1}\right) \end{aligned} \tag{E.2}$$

Eqn. E.2 can be re-arranged as the volt-charge relationship in Eqn. 9.1.

Appendix E contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix F

Analysis of FCML Converters for Balancing Issues (All V_{out} Ranges)

For other operating conditions where the inductor is also discharged by a combination of flying capacitor voltages and output voltages, the volt-charge relationship provides the following results:

$$\begin{aligned}
&(V_{k-2}-V_{out})\frac{b_{k-2}D_{k-2}T_S}{L}-(V_{k+2}-V_{out})\frac{b_{k+2}D_{k+2}T_S}{L}\\
&=\frac{2}{T_S}\left\{\frac{2Q_k}{b_kD_k}-\left(\frac{Q_{k-2}}{b_{k-2}D_{k-2}}+\frac{Q_{k+2}}{b_{k+2}D_{k+2}}\right)\right\}\\
&\quad-2V_{out}\left[(V_{k-1}-V_{out})\,b_{k-1}D_{k-1}-(V_{k+1}-V_{out})\,b_{k+1}D_{k+1}\right]\frac{T_S}{L}
\end{aligned} \tag{F.1}$$

If we apply the similar analysis method introduced in this paper for more generalized cases, a more generalized version of Eqn.(9.2) will be:

$$2V_{k-1}D_{k-1}+V_{k-2}D_{k-2}=2V_{k+1}D_{k+1}+V_{k+2}D_{k+2} \tag{F.2}$$

If $V_{k+1}=V_{k-1}=0$, Eqn. (F.2) turns into Eqn. (9.2), which is the analysis presented in this paper for the cases where $V_{out}<\frac{V_{in}}{N}$. While Eqn. F.2 is general and can be used for the analysis of all cases, including $V_{out}>\frac{V_{in}}{N}$, the analysis can not be generally simplified and intuitive as in the case of $V_{out}<\frac{V_{in}}{N}$. However, if we analyze case by case using Eqn. F.2, the same conclusion of chapter 9 related to the odd or even number of charging phases for balancing performance in FCML converters still holds.

Therefore, irrespective of V_{out} being greater or less than $\frac{V_{in}}{N}$, all FCML converters with an even number of inductor charging intervals are susceptible to timing mismatches, whereas the FCML converters with an odd number of inductor charging intervals are not.

Appendix F contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix G

Analysis of 3-Level Buck Converter with Losses Lumped into the ESR of the Inductor

Table G.1, G.2 and G.1 provides steps of the analytical method followed to determine the steady state solution of a 3-level Buck converter with lumped resistance. The general methodology follows the procedures of Appendix D. The process was repeated using a series lumped resistance series with the inductor. Table G.1 lists the initial conditions, average and median values of the voltages and currents, and inductor current ripples. Some new parameters have

Table G.1. Different converter parameters and their expressions

	Inductor Charging	Inductor Discharging
Initial condition	$v_C(0) = V_C + \frac{Q}{2C}$	$i_L(0) = I_0$
Final condition	$v_C(DT_S) = V_C - \frac{Q}{2C}$	
Capacitor voltage	$v_C(t) = k_1 e^{\omega_0 t\left(-\zeta+\sqrt{\zeta^2-1}\right)} + k_2 e^{\omega_0 t\left(-\zeta-\sqrt{\zeta^2-1}\right)}$, where, $k_1 = V_C \frac{x-\frac{1}{y}}{y-\frac{1}{y}} - \frac{Q}{2C}\frac{x+\frac{1}{y}}{y-\frac{1}{y}}$ and $k_2 = -V_C \frac{x-y}{y-\frac{1}{y}} + \frac{Q}{2C}\frac{x+y}{y-\frac{1}{y}}$	
Inductor current	$i_L(t) = -C\frac{dv_C(t)}{dt}$	$i_L(t) = I_0 e^{-2\zeta\omega_0 t} - \frac{V_{out}}{R_L}\left(1 - e^{-2\zeta\omega_0 t}\right)$
Inductor voltage	$v_L(t) = v_C(t) - i_L(t) R_L$	$v_L(t) = L\frac{di_L(t)}{dt}$
Average Inductor Current	$I_{Lav}(DT_S) = \frac{Q}{DT_S}$	$I_{Lav}(D_d T_S) = I_L(D_d T_S) - \frac{\rho}{2}\Delta i_L$ $= I_L(D_d T_S) - \rho^* \Delta i_L$
Average inductor voltage	$V_{L,av}(DT_S) = \frac{1}{DT_S}\int_0^{DT_S} v_L(t)\,dt$ $= \alpha V_C - \beta\frac{Q}{2C} = \alpha V_C - \beta^* I_{Lav}(DT_S)$	$V_{L,av}(DT_S) = \frac{1}{D_d T_S}\int_0^{D_d T_S} v_L(t)\,dt$ $= [V_{out} + I_0 R_L]\,\eta$
Median inductor current	$I_L(DT_S) = \frac{i_L(0)+i_L(DT_S)}{2}$ $= \gamma V_C + \delta\frac{Q}{2C} = -\gamma^* V_C + \delta^* I_{Lav}(DT_S)$	
Inductor current ripple	$\Delta i_L(DT_S) = V_{L,av}(DT_S)\frac{DT_S}{L}$	$\Delta i_L(D_d T_S) = V_{L,av}(D_d T_S)\frac{D_d T_S}{L}$

Table G.2. Parameters used in Table G.1

Parameter	Expression	Parameter	Expression
ω_0	$\frac{1}{\sqrt{LC}}$	β^*	$\beta\frac{DT_S}{2C}$
ζ	$\frac{R_L}{2\omega_0 L}$	γ^*	$-\gamma$
x	$x=e^{\omega_0 DT_S\zeta}$	δ^*	$\delta\frac{DT_S}{2C}$
y	$e^{\omega_0 DT_S\sqrt{\zeta^2-1}}$	z	$e^{2\zeta\omega_0 D_d T_S}$
α	$\frac{2}{\omega_0 DT_S}\frac{\left(x+\frac{1}{x}-y-\frac{1}{y}\right)}{\left(y-\frac{1}{y}\right)}\sqrt{\zeta^2-1}$	η	$\frac{\frac{1}{z}-1}{2\zeta\omega_0 D_d T_S}$
β	$\frac{2}{\omega_0 DT_S}\left[\zeta+\frac{\left(x-\frac{1}{x}\right)}{\left(y-\frac{1}{y}\right)}\sqrt{\zeta^2-1}\right]$	ρ	$\frac{\left(1+2\eta+\frac{1}{z}\right)}{\left(1-\frac{1}{z}\right)}$
γ	$\omega_0 C\left\{\zeta-\frac{\left(x-\frac{1}{x}\right)}{\left(y-\frac{1}{y}\right)}\sqrt{\zeta^2-1}\right\}$	ρ^*	$\frac{\rho}{2}$
δ	$\omega_0 C\frac{\left(x+\frac{1}{x}+y+\frac{1}{y}\right)}{\left(y-\frac{1}{y}\right)}\sqrt{\zeta^2-1}$		

Figure G.1. Steady state solution of a 3-level Buck converter

Median voltage across inductor during state 1	$V_{C1}=V_{in}-V_{CF}-V_{out}$
Median voltage across inductor during state 3	$V_{C3}=V_{CF}-V_{out}$
Charge balance	$Q_{out}=Q\left(2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}\right)+\lambda_1 V_{C1}+\lambda_3 V_{C3}$, where, $\sigma_1=\left[\delta_1\left\{\frac{1}{2}(1-\rho_2)D_2T_S+\frac{1}{2}(1+\rho_4)D_4T_S\right\}-\frac{\beta_1}{2L}D_1T_S\left\{\frac{1}{2}(1-\rho_2)D_2T_S-\frac{1}{2}(1+\rho_4)D_4T_S\right\}\right]$ $\sigma_3=\left[\delta_3\left\{\frac{1}{2}(1+\rho_2)D_2T_S+\frac{1}{2}(1-\rho_4)D_4T_S\right\}+\frac{\beta_3}{2L}D_3T_S\left\{\frac{1}{2}(1+\rho_2)D_2T_S-\frac{1}{2}(1-\rho_4)D_4T_S\right\}\right]$ $\lambda_1=\left[\gamma_1\left\{\frac{1}{2}(1-\rho_2)D_2T_S+\frac{1}{2}(1+\rho_4)D_4T_S\right\}+\frac{\alpha_1}{2L}D_1T_S\left\{\frac{1}{2}(1-\rho_2)D_2T_S-\frac{1}{2}(1+\rho_4)D_4T_S\right\}\right]$ $\lambda_3=\left[\gamma_3\left\{\frac{1}{2}(1+\rho_2)D_2T_S+\frac{1}{2}(1-\rho_4)D_4T_S\right\}-\frac{\alpha_3}{2L}D_3T_S\left\{\frac{1}{2}(1+\rho_2)D_2T_S-\frac{1}{2}(1-\rho_4)D_4T_S\right\}\right]$
Volt-second balance	$D_1V_{L,av}(D_1T_S)+D_2V_{L,av}(D_2T_S)+D_3V_{L,av}(D_3T_S)++D_4V_{L,av}(D_4T_S)=0$
Current continuation	$i_L(0)=I_L(D_1T_S)-\frac{\Delta i_L(D_1T_S)}{2}=I_L(D_3T_S)+\frac{\Delta i_L(D_3T_S)}{2}-\Delta i_L(D_4T_S)$
Volt-second balance+ Charge balance+ Current continuation	$XV_{Ci}=-Y_V V_{out}+Y_{Ii}I_{out}\implies V_{Ci}=NV_{out}+RI_{out}$, where, $X=\begin{bmatrix}X_{11}&X_{12}\\X_{21}&X_{22}\end{bmatrix}, Y_V=\begin{bmatrix}Y_{V1}\\Y_{V2}\end{bmatrix}, Y_I=\begin{bmatrix}Y_{I1}\\Y_{I2}\end{bmatrix}$, $X_{11}=\left\{\alpha_1D_1+\eta_2D_2\left[\gamma_1+\frac{\alpha_1}{2L}D_1T_S\right]R_L\right\}+\frac{\lambda_1}{2C}\frac{\left\{\beta_1D_1-\eta_2D_2\left[\delta_1-\frac{\beta_1}{2L}D_1T_S\right]R_L\right\}+\left\{\beta_3D_3-\eta_4D_4\left[\delta_3-\frac{\beta_3}{2L}D_3T_S\right]R_L\right\}}{2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}}$, $X_{12}=\left\{\alpha_3D_3+\eta_4D_4\left[\gamma_3+\frac{\alpha_3}{2L}D_3T_S\right]R_L\right\}+\frac{\lambda_3}{2C}\frac{\left\{\beta_1D_1-\eta_2D_2\left[\delta_1-\frac{\beta_1}{2L}D_1T_S\right]R_L\right\}+\left\{\beta_3D_3-\eta_4D_4\left[\delta_3-\frac{\beta_3}{2L}D_3T_S\right]R_L\right\}}{2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}}$, $X_{21}=\left[\gamma_1-\frac{\alpha_1}{2L}D_1T_S\right]-\lambda_1\frac{1}{2C}\frac{\left\{\left[\delta_1+\frac{\beta_1}{2L}D_1T_S\right]-\frac{1}{z_4}\left[\delta_3-\frac{\beta_3}{2L}D_3T_S\right]\right\}}{2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}}$, $X_{22}=-\left[\frac{1}{z_4}\left[\gamma_3+\frac{\alpha_3}{2L}D_3T_S\right]+\lambda_3\frac{1}{2C}\frac{\left\{\left[\delta_1+\frac{\beta_1}{2L}D_1T_S\right]-\frac{1}{z_4}\left[\delta_3-\frac{\beta_3}{2L}D_3T_S\right]\right\}}{2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}}\right]$, $Y_{V1}=\eta_2D_2+\eta_4D_4$, $Y_{V2}=\frac{1}{R_L}\left(1-\frac{1}{z_4}\right)$, $Y_{I1}=T_S\frac{n_1}{K}=\frac{T_S}{2C}\frac{\left\{\beta_1D_1-\eta_2D_2\left[\delta_1-\frac{\beta_1}{2L}D_1T_S\right]R_L\right\}+\left\{\beta_3D_3-\eta_4D_4\left[\delta_3-\frac{\beta_3}{2L}D_3T_S\right]R_L\right\}}{2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}}$, $Y_{I2}=-T_S\frac{1}{2C}\frac{\left\{\left[\delta_1+\frac{\beta_1}{2L}D_1T_S\right]-\frac{1}{z_4}\left[\delta_3-\frac{\beta_3}{2L}D_3T_S\right]\right\}}{2+\frac{\sigma_1}{2C}+\frac{\sigma_3}{2C}}$, $N=-X^{-1}Y_V, R=X^{-1}Y_I$
$V_{in}=(2+N_1+N_2)V_{out}+(R_1+R_2)I_{out}$ and $V_{CF}=(1+N_2)V_{out}+R_2I_{out}$	

been introduced to simplify some expressions, which are combinations of the basic parameters. These new parameters are listed in Table G.2. Next, a combination of voltage-second balance, charge balance, and current continuation equations have been combined to calculate the steady state of the 3-level Buck converter.

Appendix G contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this paper.

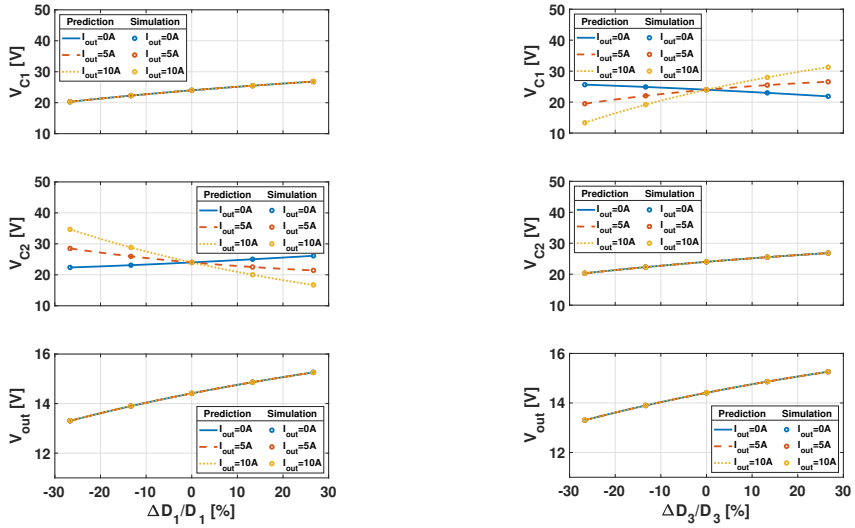
Appendix H

Analysis of a Symmetric 3-level Buck Converter

Recently, a symmetric 3-level Buck converter has been proposed in Fig.chapter 9. This converter provides balanced capacitor voltages with non-ideal timing and other advantages. A similar analysis in this work can be done and it can be shown that this converter does not change its behavior even operated with non-ideal timing. Table H.1 provides the expressions for this converter's capacitor voltages and output voltage. Fig. H.1 shows the flying capacitor voltage

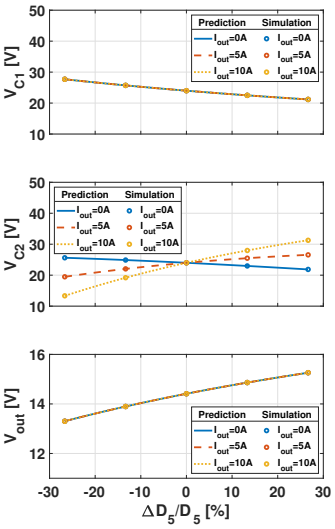
Table H.1. Steady state solution of a symmetric 3-level Buck converter

Parameter	Expression
V_{out}	$\frac{2V_{in}\left(\frac{1}{\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(5)}D_5}\right)}+\frac{1}{\left(\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(7)}D_7}\right)}\right)}{[\left(D_2+D_4+D_6+D_8+b_{(1)}D_1+b_{(3)}D_3+b_{(5)}D_5+b_{(7)}D_7\right)}$ $+\left\{\frac{\{(D_2-D_4)-(D_6-D_8)\}\left(\frac{1}{b_{(1)}D_1}-\frac{1}{b_{(5)}D_5}\right)}{\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(5)}D_5}\right)}-\frac{\{(D_8-D_2)-(D_4-D_6)\}\left(\frac{1}{b_{(3)}D_3}-\frac{1}{b_{(7)}D_7}\right)}{\left(\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(7)}D_7}\right)}\right\}$ $-(D_2-D_4+D_6-D_8)\frac{\left(\frac{1}{b_{(3)}D_3}-\frac{1}{b_{(7)}D_7}\right)\left(\frac{1}{b_{(1)}D_1}-\frac{1}{b_{(5)}D_5}\right)}{\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(5)}D_5}\right)\left(\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(7)}D_7}\right)}$ $-\left\{\frac{b_{(1)}D_1b_{(5)}D_5\left(\frac{1}{b_{(1)}D_1}-\frac{1}{b_{(5)}D_5}\right)^2}{\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(5)}D_5}\right)}+\frac{b_{(3)}D_3b_{(7)}D_7\left(\frac{1}{b_{(3)}D_3}-\frac{1}{b_{(7)}D_7}\right)^2}{\left(\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(7)}D_7}\right)}\right\}]$
V_{C_1}	$-\frac{\left(\frac{1}{b_{(3)}D_3}-\frac{1}{b_{(7)}D_7}\right)}{\left(b_{(1)}D_1+b_{(5)}D_5\right)}\frac{\frac{V_{out}I_{out}}{V_{in}}\frac{2L}{TS}\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(5)}D_5}\right)-V_{out}(D_2-D_4+D_6-D_8)}{\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(5)}D_5}+\frac{1}{b_{(7)}D_7}\right)}$ $-V_{out}\frac{\{(D_2-D_4)-(D_6-D_8)\}}{\left(b_{(1)}D_1+b_{(5)}D_5\right)}+\frac{b_{(1)}D_1}{\left(b_{(1)}D_1+b_{(5)}D_5\right)}V_{in}-\frac{\left(b_{(1)}D_1-b_{(5)}D_5\right)}{\left(b_{(1)}D_1+b_{(5)}D_5\right)}V_{out}$
V_{C_2}	$\frac{\left(\frac{1}{b_{(1)}D_1}-\frac{1}{b_{(5)}D_5}\right)}{\left(b_{(7)}D_7+b_{(3)}D_3\right)}\frac{\frac{V_{out}I_{out}}{V_{in}}\frac{2L}{TS}\left(\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(7)}D_7}\right)+V_{out}(D_2-D_4+D_6-D_8)}{\left(\frac{1}{b_{(1)}D_1}+\frac{1}{b_{(3)}D_3}+\frac{1}{b_{(5)}D_5}+\frac{1}{b_{(7)}D_7}\right)}$ $+V_{out}\frac{\{(D_8-D_2)-(D_4-D_6)\}}{\left(b_{(7)}D_7+b_{(3)}D_3\right)}+\frac{b_{(3)}D_3}{\left(b_{(7)}D_7+b_{(3)}D_3\right)}V_{in}+V_{out}\frac{\left(b_{(7)}D_7-b_{(3)}D_3\right)}{\left(b_{(7)}D_7+b_{(3)}D_3\right)}$

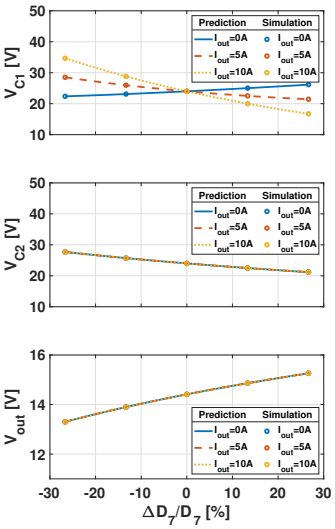


(a) D_1 Variation

(b) D_3 Variation



(c) D_5 Variation



(d) D_7 Variation

Figure H.1. Predicted and simulated flying capacitor voltage variations for a symmetric 3LB converter (Operating condition: $V_{in} = 48V$, $C = 5\mu F$, $L = 2\mu H$, $f_S = 300kHz$, $D_{1,3,5,7}(ideal) = 0.15$ and $D_{2,4,6,8}(ideal) = 0.10$)

variation with the duty cycles and output load. However, the variation is very small unless the duty-cycle variations are large.

Appendix H contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix I

Current Control Loop Less Control for AC-DC converters

Non-linear carrier control was first proposed in [131]. This method eliminated the requirement of sensing the input voltage for the PFC rectifier. Considering a system-level implementation, the controller becomes much simpler and can be implemented with fewer sensing components and computing power from the microcontroller if employed. This method is motivated by the one-cycle control method for DC-DC converters [132]. Non-linear carrier control requires cycle-by-cycle integration of the current through a particular switch. Later, a

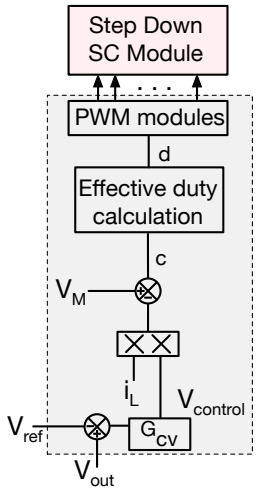


Figure I.1. Current control loop-less control for single module operation

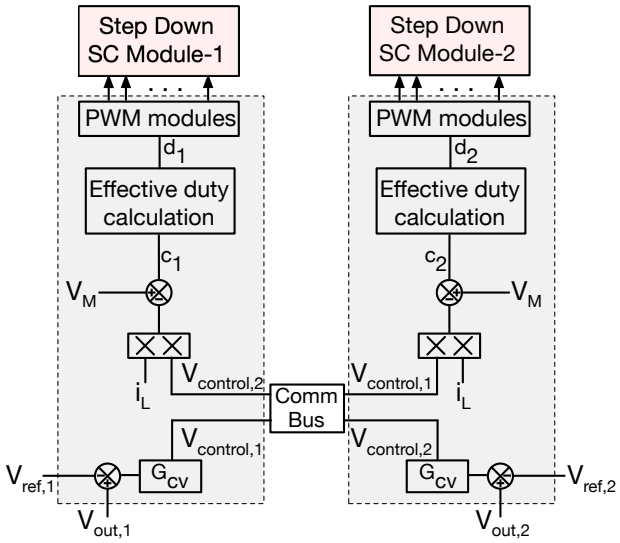


Figure I.2. Current control loop-less control for multi module operation

very simple digital PFC controller was demonstrated in [133] demonstrated that simple input current sensing is enough for performing the PFC operation. Even cycle-by-cycle integration is not required. The same method can also be employed to control the single module of the PFC Step down converter listed in chapters 11 and 12. One extra step of effective duty cycle calculation is required as this is a multi-level converter, and the effective charging time the inductor sees is different from the ON time of the switches. The control method for a single module is depicted in Fig. I.1.

The more exciting application of this current control loop-less method is the modular connection listed in chapter 12. The method shown in chapter 12 already uses the CAN bus to communicate among controllers. The power and output voltage weighted control signals are still required to be shared over the communication bus. The individual controllers are required to sense the input current separately and generate the control signals and duty cycles based on the gathered data from the bus. Fig. I.2 depicts the current control loop-less control method for modular operation.

Appendix I contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

Appendix J

Controller for Multi Inductor Multi Output Hybrid (MiMoH) Converter

J.0.1 Slow Steady State Controller

The important part of realizing is that because of the co-dependency of the outputs, the converter can not act as a voltage source, current source, or even power source. Only the right control method can operate the converter at a voltage mode operation. From eq. 14.5, 14.6 and 14.6, it is apparent that the duty cycles are required to be set by the amount of power from the combination of all the outputs. Average power control is normally employed in AC-DC converters for Power Factor Correction (PFC) operation as in chapters 11 and 12.

The first intuition to control the MiMoH was to use the same average power control method in chapter 12. In chapter 12, two separate outputs were controlled from a common AC input. The problem here is similar except the input is a DC voltage. Observing the similarities, the average power control method in Fig. J.1 was conceptualized. For three separate outputs, three separate voltage compensators are required. These compensators generate current references, $Iref_{1,2,3}$. The output current can then the sensed and compared. The currents of the different outputs are entangled with each other as follows:

$$I_{out_1}D_1 = I_{out_2}D_2 = I_{out_3}D_3 \tag{J.1}$$

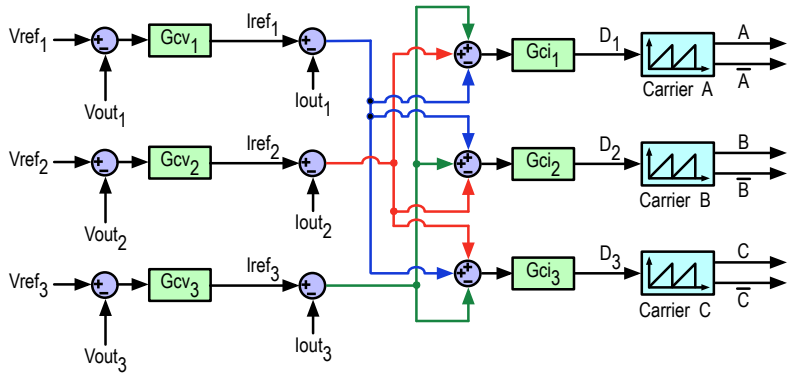


Figure J.1. Conceptualized control method using average power control method of modular PFC converters

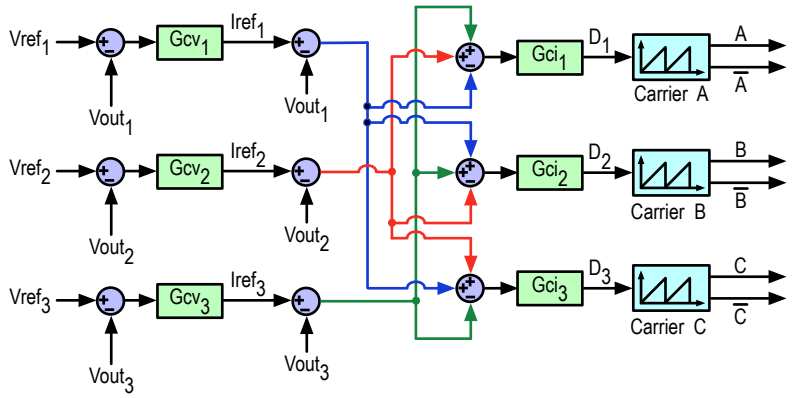
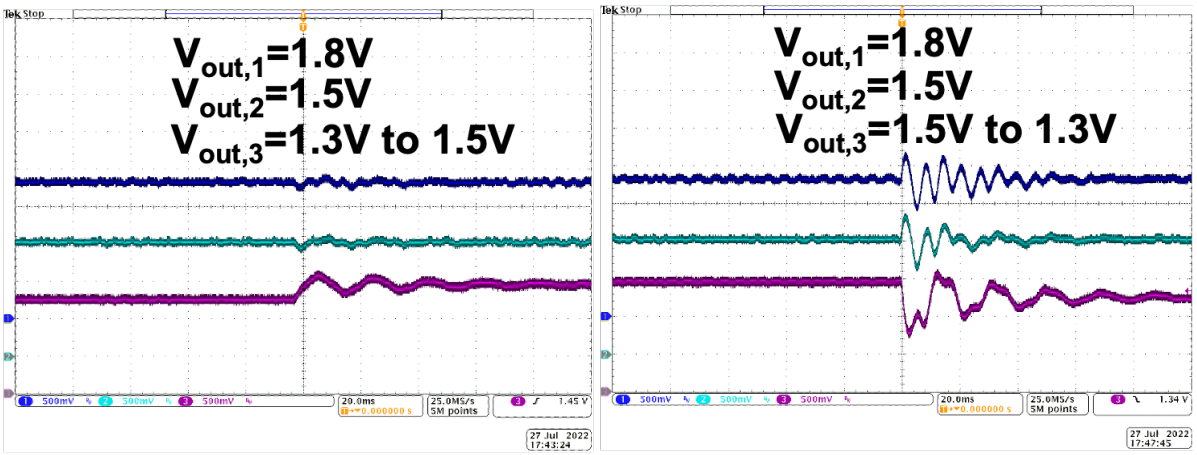


Figure J.2. Slow steady-state control method : a combination of V^2 controller motivated from modular PFC converters' control



(a) Transient response for low to high reference change at $V_{out,3}$ **(b)** Transient response for high to low reference change at $V_{out,3}$

Figure J.3. Transient verification of the steady-state control method of Fig. J.2

Following the eqn. J.1, the differences between the current references and sensed currents in Fig. J.1 can be coupled to finally compensate and generate the duty cycles for the output voltages. As PFC controllers depend on average current, the sensed current in this control method also has to be the average current. However, there is no restriction on the current shape of this converter following the input current like PFC. Sensing the currents from three separate outputs seems costly at the implementation time.

Then, the following fact was discovered, in a steady state, when the output load is nearly constant or the load behaves like a resistor, the output voltages are directly proportional to the output currents. Instead of sensing currents in Fig. J.1, output voltages can also be used as in Fig. J.1. The compensator's gains need to be adjusted according to the average loading of the outputs. Note that using either the current or voltages can not make the transient fast. The reason is the controller principle is based on the average power control of the PFC controller, which is, by design, very slow. Using the output voltages instead of the currents, as in Fig. J.2, a control loop has been designed and verified for transient response shown in Fig. J.3.

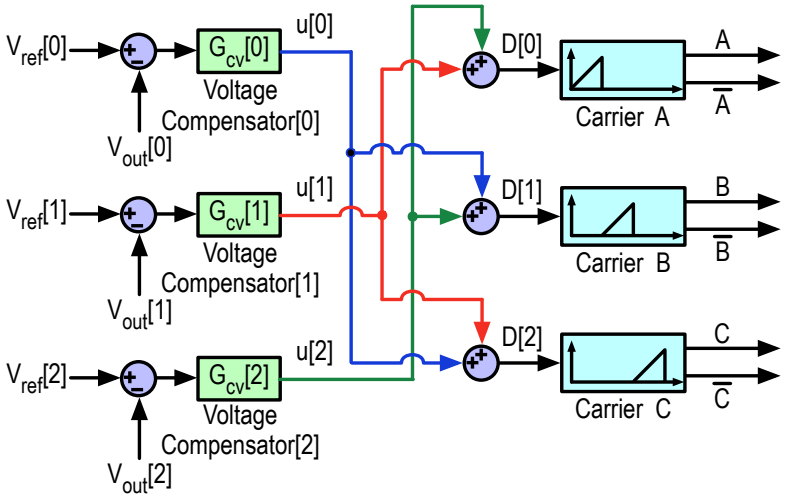


Figure J.4. Fast control method: motivated from the current control loop less modular PFC converters

J.0.2 Fast Controller

It was mentioned that the steady state controller was motivated by the average power control of modular AC-DC controller in chapter 12. In DC-DC applications, very often fast transient response is desired. Especially one very good application of the proposed MiMoH converter in chapter 14 can be multi-core processor power delivery. But, a fast control method is required to accompany the converter in this application. When a current control loopless method was discovered to apply for the modular AC-DC PFC converters in Appendix I, the idea was extended to the MiMoH converter as well. In this method, the second compensation in every output control path can be eliminated. The simplified control is shown in Fig. J.4. This control method is very fast and comparable to traditional pulse width modulated (PWM) converters, for example, Buck converter. Future publications will follow up on this topic with experimental validation of this control method.

Appendix J contains unpublished materials coauthored with Le, Hanh-Phuc. The dissertation/thesis author was the primary investigator and author of this work.

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