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**RFIC Design for High-Speed Optical and Multigigabit Wireless
Communication Systems**

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Joohwa Kim

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Gert Cauwenberghs
Professor Larry E. Larson
Professor Gabriel M. Rebeiz
Professor Steven Swanson

2011

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The dissertation of Joohwa Kim is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2011

DEDICATION

To my parents and wife.

EPIGRAPH

*Genius is one percent inspiration
and ninety-nine percent perspiration.*

—Thomas A. Edison

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PUBLICATIONS

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ABSTRACT OF THE DISSERTATION

**RFIC Design for High-Speed Optical and Multigigabit Wireless
Communication Systems**

by

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In this dissertation, high-speed and high-frequency millimeter-wave circuit techniques are introduced for silicon integrated circuit processes. A transimpedance limit for multistage transimpedance amplifiers (TIAs) is derived and applied to a bandwidth enhancement technique using inductive-series π networks. A 40-Gb/s TIA is demonstrated in a 0.13 μm CMOS process and achieves a transimpedance gain of 50 $\text{dB}\Omega$ with a 3-dB bandwidth of 29 GHz.

A low-power optical front-end is implemented in a 45-nm silicon-on-insulator (SOI) CMOS process. The modulator driver uses floating body devices to generate a voltage swing of more than 2 Volts. The optical receiver exhibits a transimpedance exceeding 55-dB $\cdot\Omega$ over 30 GHz and consumes only 9 mW from a 1 V

supply.

Next, a 160-Gb/s amplifier is realized with stagger-tuned stages that are equalized for high bandwidth and low gain ripple. The staggered response is demonstrated with a Darlington feedback amplifier and a constructive wave amplifier. The broadband amplifier is implemented in a 0.12- μm Silicon-Germanium (SiGe) BiCMOS process and achieves a gain of 10 dB and 3-dB bandwidth of 102 GHz. In contrast, a 45-nm SOI CMOS, cascode distributed amplifier exhibits 9-dB gain over a 3-dB bandwidth of 92 GHz.

In the second part of this dissertation, millimeter-wave circuit design techniques for wireless communication systems are presented. Constructive wave amplification is shown to amplify forward traveling waves along a single transmission line. A 0.12- μm SiGe BiCMOS constructive wave amplifier achieves more than 37.5-dB gain with a 3-dB bandwidth of 14.6 GHz and, consequently, demonstrates a gain-bandwidth product as high as 1,095 GHz.

A *Q*-band (40~45 GHz) bidirectional transceiver is demonstrated that eliminates the need for transmit/receive switches with a novel PA/LNA circuit. The transmitter P_{sat} is 9.5 dBm while the receiver noise figure is 4.7 dB.

Finally, using the constructive wave amplifier technique, a *W*-band, bidirectional constructive wave amplifier is demonstrated to allow amplification in one of two directions. The amplifier has a peak gain of 16 dB and tuned between 77 and 94 GHz.

Chapter 1

Introduction: High Capacity Communication

This dissertation discusses high-frequency and high-speed radio-frequency integrated circuit (RFIC) design in silicon processes. High capacity communication refers to data transmission rates over a single communication channel that exceed 10 Gb/s. A decade ago, 10 Gb/s data rates were only available with optical communication systems. Optical transmission media inherently could offer tremendous amounts of bandwidth compared to the bandwidth of electronic transmitters and receivers. With higher speed integrated circuits and bandwidth enhancement circuit techniques, the data rate could be increased beyond 10 Gb/s. In this dissertation, new solutions are proposed to build optical transmitters and receivers capable of data rates beyond 100 Gb/s.

More recently, utilization of millimeter-wave wireless channels could rival optical communication techniques through the use of beamforming. Wireless systems might be preferable due to the lack of a physical transmission media as well as the ability to use more spectrally-efficient modulation schemes. Attempts to commercialize wireless HDMI links over a 60 GHz channel have resulted in 4 Gb/s data rates. The future could offer more sophisticated signal processing in conjunction with parallel arrays to increase these data rates beyond 10 Gb/s. This dissertation discusses novel millimeter-wave front-end circuitry that support bidirectional transceiver arrays.

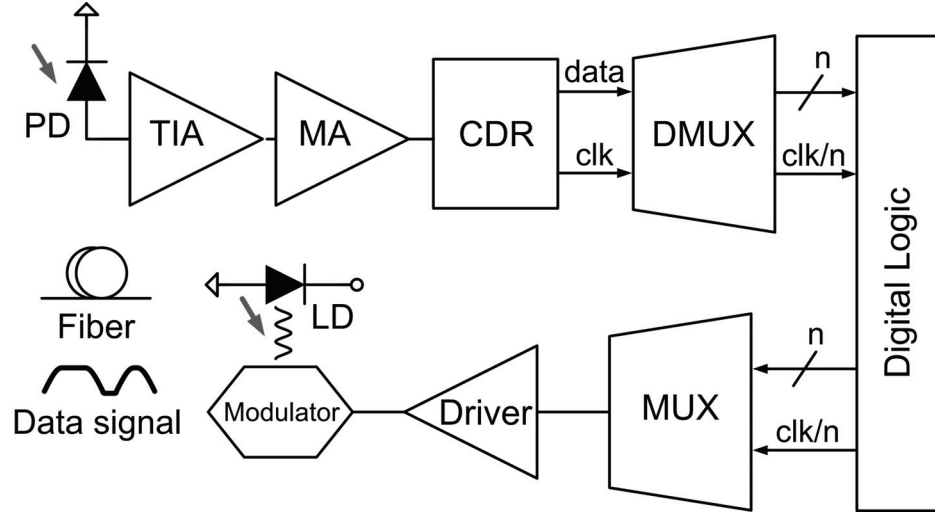


Figure 1.1: Block diagram of an optical transceiver

1.1 Optical Communication Systems

Fiber optic communication is the core of modern networking and telephony infrastructure. Silica fibers offer low attenuation and large bandwidth for long distance, high information capacity communication networks. A migration of optical communication to shorter distance scales such as storage area networks, memory links, and even chip scale interconnects promises the bandwidth not available over electrical interconnects [1,2]. Optical interconnects would offer scalable bandwidth through Wavelength Division Multiple Access (WDMA) as well as novel interconnect network architectures such as passive star or ring networks that are not possible using electrical signaling in board-to-board and chip-to-chip links [3]. Homogeneous integration with standard bulk silicon CMOS processes is favored for low-cost of integration with existing fabrication facilities. Alternatively, integration on silicon-on-insulator (SOI) technologies has been demonstrated for 10 Gb/s communication with a slight cost penalty [4].

1.1.1 Optical Transceivers

Fig. 1.1 shows the block diagram of a typical optical transmitter and receiver. First, the multiplexer (MUX) serializes an N bit bus operating at a lower

speed into a serial data stream operating at a higher data rate f_B . This serial data is amplified to the specific swing required to drive an optical modulator at a sufficient extinction ratio. The extinction ratio is the ratio of the logical "1" optical power to the logical "0" optical power and determines the maximum signal-to-noise (SNR) ratio of the optical link. The optical carrier is modulated with an envelope that resembles the electrical serial data.

The receiver should demodulate the envelope information from the optical carrier and convert the received analog signal back to digital values. A photodetector or photodiode (PD) converts the received optical power into an electrical current based on the diode responsivity. Responsivity is the ratio of the current produced for a given power. In many photodiodes, the responsivity is between 0.8 A/W and 1 A/W. The current is converted into a voltage with a transimpedance amplifier (TIA). The TIA is distinguished by the specification of a low input impedance required to sink current from the photodiode but a large transimpedance as defined from the transfer of the input current to an output voltage.

Typically, a single TIA stage is insufficient to amplify the input current to the voltage levels that reflect logical levels. A post amplifier or limiting amplifier (LA) provides additional voltage gain to amplify the signal to a desired signal swing that meets the sensitivity of a digital comparator. The comparator recovers a digital value - correctly or incorrectly - from the received analog signal. When the signal swing is large, the comparator probabilistically recovers the correct digital value. The comparator is typically part of a clock and data recovery circuit (CDR) that not only samples the serial data but also extracts a clock at the data rate from the received serial data.

Finally, a demultiplexer (DMUX) deserializes the received high-speed serial data stream back into an N bit bus operating at a lower rate compatible with electronic interconnects and digital processing. Parallel sampling CDR architectures perform the DMUX task within the data recovery circuitry [5]. Once the electrical bus is recovered, digital signal processing blocks decode the bits, perform error checks, and extract the payload data from the framing information [6].

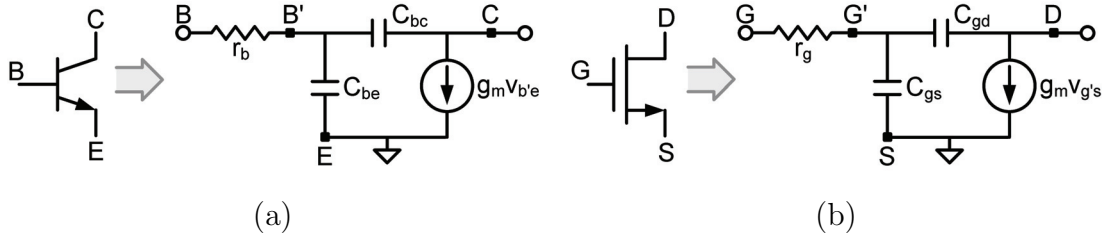


Figure 1.2: Small-signal model of (a) HBT device and (b) CMOS device.

1.1.2 Devices for High-Speed Optical Transceivers

The demands of data-intensive networking have driven bandwidth demands over optical fiber particularly for storage area networks. Simultaneously, a concerted effort to develop optical components in a standard CMOS process promises to make optical communication pervasive and economical. New advances in silicon photonic devices could support O/E interfaces at 40-Gb/s and higher [7]. Therefore, the bandwidth of optical elements could be unleashed at chip scales and drive the demands for short reach optical transceivers from 10-Gb/s to 40-Gb/s and beyond [8]. Broadband transceivers are required for high-speed optoelectronic (O/E) signal conversion.

The bandwidth of active circuits is limited by the devices of the process technology. One useful metric for broadband circuits is f_T which is defined as the unity current gain cutoff frequency. In other words, a transistor produces current gain between the gate and drain current for a metal-oxide-semiconductor field-effect transistor (MOSFET). The current gain is defined as

$$h_{21}(f_T) = \frac{i_d}{i_g} \approx \frac{g_m}{C_{gs}}, \quad (1.1)$$

where g_m is the transconductance and C_{gs} is the gate-source capacitor of the transistor. Historically, broadband electronics have relied on III-V semiconductor technologies such as GaAs and InP because of the inherent device f_T and high breakdown characteristics [9]. Compound semiconductors typically have high transconductance and small junction capacitance.

In the receiver amplifiers, the f_T of devices fundamentally bounds the maximum gain-bandwidth product (GBW) of the circuit. In other words, a single stage

amplifier with voltage gain A_v must have limited bandwidth since $f_T \geq GBW = A_v BW$ where BW is the required bandwidth. Typically, the maximum GBW is reduced by undesirable parasitics and mismatched transistor biasing for peak f_T current density. Consequently, as data rate increases the required bandwidth is also increased but the available gain decreases.

However, the advance of silicon and silicon germanium circuit techniques to highly scaled feature sizes has pushed transistor cutoff frequencies (f_T) beyond 200 GHz. Fig. 1.3 shows the scaling trends of f_T and f_{max} [10]. In particular, SOI process technologies have realized gate lengths under 22 nm with f_T approaching 400 GHz. This suggests that compound semiconductor can be replaced for broadband receivers. The potential for homogeneous optoelectronic circuit technologies could yield a combination of low-power and high-speed operation for energy efficient transceiver circuits [11], [12]. Modern optical transceiver design places a high premium on the speed and energy efficiency. Receiver design metrics focus on the transimpedance gain-bandwidth versus the power consumption.

The high voltage drive levels that were historically demanded for optical modulators have been relaxed through the invention of silicon photonic ring modulators. These devices require less bias voltage (< 2 V) compared to traditional Mach-Zehnder modulators (> 6 V). This shift makes the proposed use of homogeneous silicon platforms more palatable since the high-speed CMOS technologies allow only limited breakdown voltage.

1.1.3 Optical Receivers

The transimpedance amplifier determines the sensitivity of high-speed optical receivers. CMOS TIAs for data rates exceeding 40-Gb/s optic communication systems have been demonstrated [13], [14] and [15]. In high-speed optical receivers, broadband receiver bandwidth is required to avoid intersymbol interference (ISI) and a rule of thumb for non-return-to-zero (NRZ) receivers need the optimum 3-dB bandwidth is

$$BW \approx \frac{2}{3} \cdot f_B \quad (1.2)$$

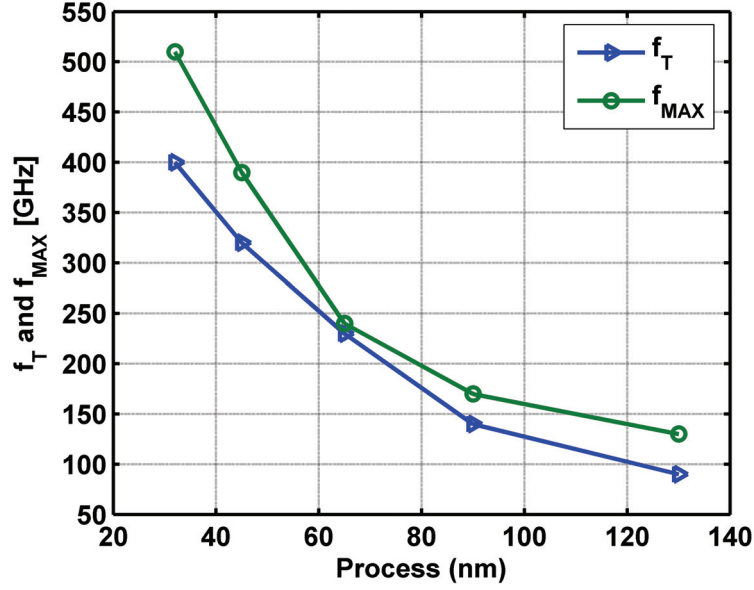


Figure 1.3: f_T and f_{max} versus CMOS process.

where f_B is the bit rate [6]. For example, a 40-Gb/s optical receiver requires a 3-dB bandwidth of at least 26 GHz.

The required bandwidth of the TIA can be directly related to the maximum available transimpedance for a shunt feedback TIA.

$$R_T = \frac{f_T}{2\pi BW^2 C_T}, \quad (1.3)$$

where C_T is the total capacitance at the input of the transimpedance amplifier. This capacitance consists of the photodiode capacitance and the amplifier input capacitance. Clearly, the transimpedance drops rapidly as the bandwidth of the receiver must increase. To compensate the transimpedance of a high-speed optical receiver, multistage post-amplifiers are typically used to amplify the signal and meet the decision circuit sensitivity. However, additional stages introduce higher power consumption. Additionally, each post-amplifier stage introduces additional poles, and the bandwidth drops as the number of stages increases.

As a rule of thumb, the f_T of the device should be at least four times the BW . This has limited the use of silicon processes for speeds greater than 100 Gb/s. To meet the 3-dB bandwidth requirement with relatively mature process

technologies, many different techniques have been proposed using passive networks such as shunt peaking, series peaking, and t-coil coupling [16] [17] [18] [19]. However, many of these bandwidth enhancement techniques often sacrifice group delay variation. Group delay variation reflects the deviation of the frequency response from linear phase. Large group-delay variation results in data-dependent jitter (DDJ) which degrades the signal integrity of the data eye [6], [15]. Consequently, bandwidth enhancement techniques that introduce large group-delay variation do not merit great practical value.

The relevant figure of merit (FOM) explored for broadband receivers in silicon integrated processes considers the transimpedance, bandwidth, and power consumption;

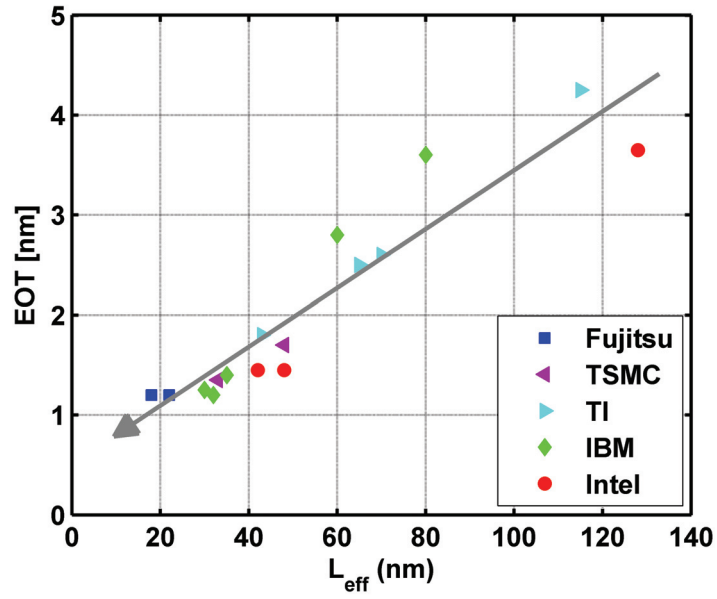
$$FOM = \frac{R_T f_B}{P_{DC}}, \quad (1.4)$$

where P_{DC} is the power consumption.

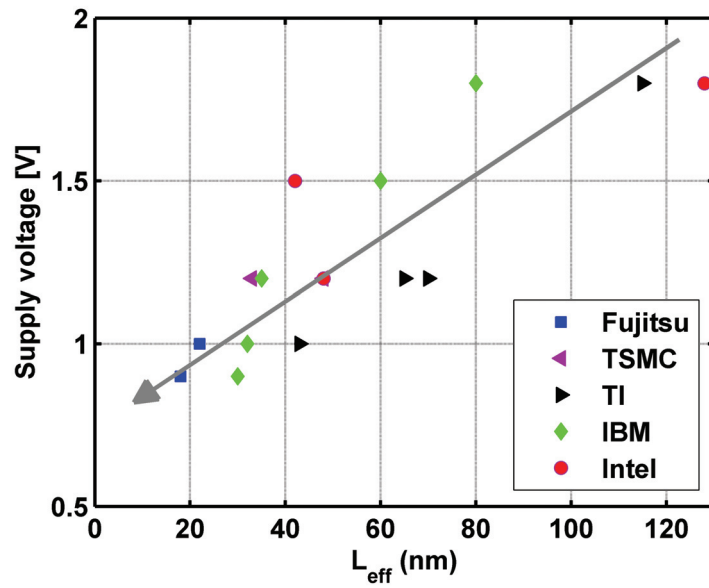
1.1.4 Optical Transmitters

The circuit design for an optical transmitter depends on the choice of optical modulator. For 40 Gb/s operation, Mach-Zehnder Modulators (MZM) have historically been the only option. At 10 Gb/s, modulators are either MZMs, electro-absorption modulators (EAMs), or photonic ring modulators (PRMs). Originally, research in silicon photonics had demonstrated the use of MZMs for 10 Gb/s serial transmission [4]. MZMs are notorious for requiring large voltage swings to provide sufficient extinction ratio. Consequently, modulator drivers typically require high-voltage swing ($> 2 V_{PP}$) to induce a π phase shift to the optical carrier through the MZM.

The required high-voltage swing is at odds with CMOS scaling. Low breakdown voltage and high knee voltage of the MOSFET limits the drain voltage swing [20]. Fig. 1.4(a) shows that the equivalent oxide thickness (EOT) versus effective gate length for different processes [21]. As CMOS processes are scaled, the EOT decreases and the oxide breakdown voltage must decrease [22]. Consequently, the power supply must be reduced to avoid oxide breakdown. Fig. 1.4(b) shows that power supply voltage versus effective gate length for different processes [21].



(a)



(b)

Figure 1.4: (a)Equivalent oxide thickness and (b)power supply voltage versus effective gate length.

Notably, the power supply is decreased up to 0.9 V at $L_{eff} = 20$ nm as CMOS technology scales down. This voltage headroom limitation imposes severe circuit design challenges for single transistor topology to generate the necessary voltage swing. Consequently, while receiver front-ends benefit from highly-scaled CMOS processes, high-swing broadband modulator drivers using scaled CMOS technology are complicated by the low breakdown voltage.

More recently, ring modulators in silicon-on-insulator (SOI) processes have been demonstrated at 10 Gb/s for high-speed modulation [23]. Ring modulators relax the drive voltage requirements to between one and two volts.

1.1.5 Passing the 40-Gb/s Barrier in Silicon

In this dissertation, several contributions to the state-of-the-art in broadband front-ends are proposed. First, the transimpedance limit is derived for multi-stage amplifiers. The new transimpedance limit demonstrates that low f_T/BW not only results in low transimpedance but is in fact incapable of realizing the necessary gain to amplify the serial stream to necessary received voltage swing. Second, the use of highly scaled (45nm) CMOS SOI processes is shown to allow significant energy reduction. Third, a new circuit technique is proposed which enables extremely broadband response (> 102 GHz) with relatively low f_T without sacrificing group delay variation.

This dissertation presents 40-Gb/s to 160-Gb/s low power receivers and transmitters using 0.13- μ m CMOS, 0.12- μ m SiGe BiCMOS and 45 nm SOI CMOS technologies. First, a compact low group-delay 40-Gb/s TIA with post amplifier is demonstrated. A transimpedance limit for multistage TIAs is derived, and a bandwidth-enhancement technique while avoiding large group-delay variation using inductive-series π -networks is analyzed. Next, low power 40-Gb/s SOI CMOS transceiver is presented. To overcome circuit design issues for high-speed optical front-ends described in Section 1.1.1 several design techniques are explored that can enable the implementation of both 40-Gb/s receiver and transmitter in highly scaled CMOS technology.

A new bandwidth enhancement scheme is proposed in the later part to

achieve 100–160-Gb/s optical data rate and the 3-dB bandwidth of 102-GHz with a gain ripple of less than 1.5 dB is achieved. A 92-GHz distributed amplifier is also demonstrated and can be used for 100-Gb/s main amplifier.

1.2 Mm-Wave Wireless Communication Systems

Millimeter-wave (mm-Wave) bands (>30 GHz) offer new opportunities for silicon integrated circuits in communication, radar, and imaging applications. The *Q*-band (33–50.0 GHz) is used for satellite communications (SATCOM) data links [24], [25], the 77 GHz band is used for automotive collision avoidance radars, and the 60 GHz band is allocated for unlicensed short range data links at multi-gigabit/s data rates [26], [27]. In addition, *W*-band (75–111GHz) is also used for point-to-point high-bandwidth wireless communication links [28], [29] as well as active or passive imaging systems [30], [31].

Millimeter-wave circuits have also historically required GaAs or InP devices, but recent research investigations demonstrate silicon front-ends for *Q*-band and *W*-band imaging and communications in spite of the low intrinsic gain of silicon devices compared to III–V devices [25], [32]. At millimeter-wave frequencies, new challenges exist for silicon low-power, high-gain, and wideband circuits. Circuit design is confronted by concerns of process variations and low quality passives for monolithic arrays. Narrowband matching allows the highest available power gain for a given transistor since resonant networks match the impedance at the gate, source, or drain of the device to the source and load impedance. These input and output matching networks are well suited to integrated implementations with finite quality factor passives and can alternatively optimize the noise, linearity, or output power of the amplifier stage. However, a drawback of narrowband matching is that the input and output matching are only acceptable over a narrow bandwidth that is typically sensitive to the parasitic components (*RLC*) at mm-Wave frequencies.

1.2.1 Mm-Wave Switchless Bidirectional Transceivers

Bidirectional amplifiers are motivated by the requirements of scalable microwave and millimeter-wave phased array transceivers. Research efforts have moved towards large scale integration of phased array transceivers based on silicon/ silicon-germanium (Si/SiGe) processes. Previous work on phased arrays has demonstrated either receive arrays at 6-18 GHz [33] [34], 24 GHz [35] [36], 45 GHz [24], 60 GHz [37], and 77 GHz [38] or transmit arrays at 24 GHz [39], 45 GHz [25], 60 GHz [40], and 77 GHz [41]. The complexity of fully integrated phased array circuitry is illustrated with as many as 32 channel arrays on a single die [26]. Significant die area is required to implement separate transmitter and receiver arrays on a single die and recent approaches have proposed bidirectional circuit elements for multifunction arrays [42].

Bidirectional amplifiers are necessary at two locations in a phased array transceiver as shown in Fig. 1.4. First, the bidirectional amplifier switches between a receive mode with a low-noise amplifier (LNA) and transmit mode with a power amplifier (PA) at the antenna. Second, the bidirectional circuit element is necessary after beamforming in this RF phase shifting array. While the antenna LNA sets the sensitivity of the receiver, a passive phase shifter typically introduces higher noise figure and loss.

To isolate the noise figure of the mixer, an LNA is introduced after the power combiner in Fig. 1.4. In transmit mode, the pre-PA provides the necessary driver power to the RF power splitter such that ample power is available at the final PA stage in each channel. For instance, if each final PA delivers $P_o = 20$ dBm to the antenna with a combined PA and phase-shifter gain of $G_{TX} = 10$ dB, the pre-PA must deliver a power of $P_o - G_{TX} + 10 \log_{10} N$. For a 16-element array, the input power must be 22 dBm. Clearly, the power handling requirements of the pre-PA are similar to the final PA stage when $G_{TX} \sim 10 \log_{10} N$.

Earlier work focused on a GaAs HEMT common gate topology as a bidirectional amplifier but is limited by the difficulty to simultaneously optimize the common gate device for both low-noise and high-power [43]. Further development of this approach was motivated by the need for scalable bidirectional transceiver

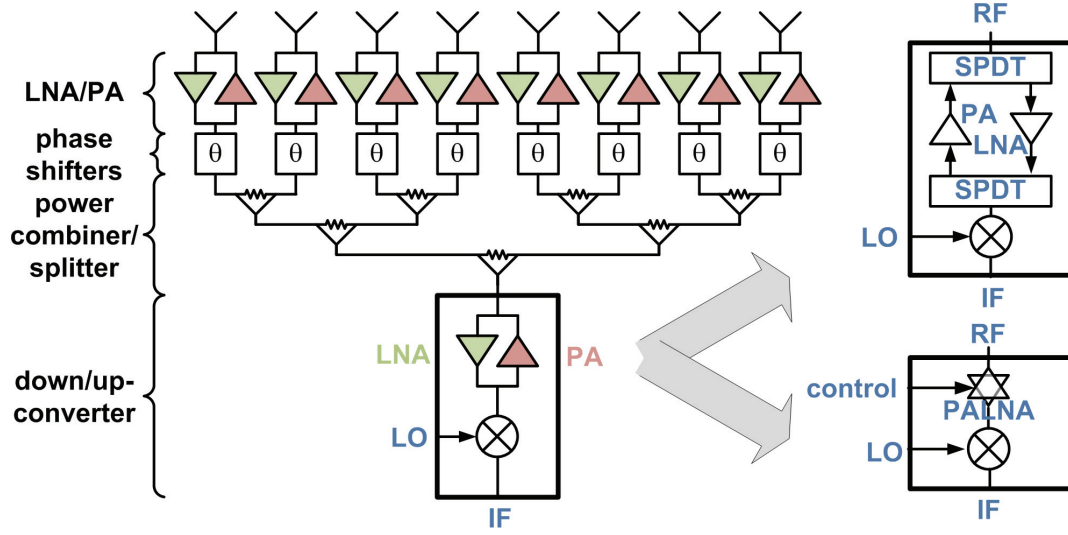


Figure 1.5: Motivation for bidirectional amplifiers for phased array front ends and approaches for bidirectional elements.

front-end elements for phased arrays implemented in GaAs [44] [45]. Recent work in silicon has investigated bidirectional front-end elements based on microwave switches before and after the LNA as shown in Fig. 1.4 [42]. The disadvantage of this switch is that it contributes loss to the RF signal path which ultimately limits receiver sensitivity as well as reducing PA output power and efficiency.

This dissertation investigates the design of a PALNA (PA-LNA) bidirectional amplifier that uses transmission line matching techniques to isolate the power amplifier and low-noise amplifier under different bias conditions and eliminates the sensitivity penalty of microwave switches at the front-end. This dissertation demonstrates a SiGe bidirectional transceiver for 45 GHz satellite communications based on a bidirectional amplifier (PALNA) circuit that eliminates the need for microwave switches before and after the low-noise amplifier and power amplifier [46].

1.2.2 Cascaded Constructive Wave Amplification

Additionally, the dissertation also presents the another bidirectional amplifier based on the cascaded constructive wave amplifier CCWA topology at W -band that obviates the need for a switch at the aperture. To provide high-gain and

broadband-matching, the constructive wave amplification is proposed. As opposed to distributed amplifiers, the proposed CCWA amplifies forward traveling waves while attenuating backward traveling waves through a single transmission line. A CCWA topology is ideal for a direct-detection imaging applications since high-gain is achieved with comparable noise performance. A *W*-band SiGe BiCMOS CCWA is presented with more than 37-dB gain at 90 GHz and a 3-dB bandwidth of 14.6 GHz. Consequently, this amplifier demonstrates a gain-bandwidth product as high as 1,095 GHz. To date, this is the highest gain-bandwidth shown in a silicon process.

A *W*-band switchless bidirectional front-end is demonstrated using the CCWA technique in a 0.12- μm SiGe BiCMOS technology. The CCWA requires only a single transmission line around which active feedback circuits are shunted. The proposed bidirectional amplifier alternates active feedback in different directions along the transmission line to allow for bidirectional gain.

1.3 Dissertation Organization

Background material and relevant circuit design issues for RFIC design of high-speed optical communication systems and high-speed millimeter wave wireless communication systems has been introduced in the first chapter.

Chapter 2 rederives the transimpedance limit for multistage amplifiers. This new limit reveals the tradeoffs between transimpedance, bandwidth, and process technology. A 40-Gb/s TIA with post-amplifiers is presented using multistage inductive-series peaking for low group delay variation. Next, a bandwidth enhancement technique using inductive-series π -networks is analyzed. A design method for low group delay constrained to 3-dB bandwidth enhancement is suggested. The TIA is implemented in a 0.13 μm CMOS process and achieves a 3-dB bandwidth of 29 GHz. The transimpedance gain is 50 dB Ω and the transimpedance group delay variation is less than 16 ps over the 3-dB bandwidth. The chip consumes 45.7 mW from a 1.5 V supply. The measured TIA demonstrates a transimpedance figure of merit of 200.7 Ω/pJ .

Chapter 3 presents a low-power, 40-Gb/s silicon on insulator (SOI) transceiver front-ends with a TIA, main amplifier, and single-ended/differential 50 $\cdot\Omega$ modulator drivers implemented in a 45 nm SOI CMOS technology. A modulator driver uses floating body devices to realize differential voltage swing of more than 4.5 V_{PP} with a single-ended small-signal gain of 7.6 dB over 33 GHz. The optical receiver consists of a TIA and post-amplifier with 55-dB $\cdot\Omega$ of transimpedance over 30 GHz. The group-delay variation is ± 3.9 ps over the 3-dB bandwidth and the average input-referred noise density is 20.47 $pA/\sqrt{Hz}$. The TIA consumes 9 mW from a 1 V supply for a transimpedance figure of merit of 1874.5 Ω/pJ .

Chapter 4 presents a 160-Gb/s receiver in a 0.12- μm SiGe BiCMOS process. The 160-Gb/s receiver is realized with cascaded stagger-tuned stages that are equalized for high bandwidth and low gain ripple. The staggered frequency response is demonstrated to improve the transimpedance limit of active circuits. The staggered response is demonstrated with a Darlington feedback amplifier and a constructive wave amplifier to demonstrate low group delay. The amplifier achieves a 3-dB bandwidth of 102 GHz and gain of 10 dB with 1.5 dB gain-ripple and group-delay variation under ± 6 ps over the entire 3-dB bandwidth. The chip consumes 73 mW from a 2 V supply.

In addition, a low-power cascode distributed amplifier is demonstrated in a 45-nm SOI CMOS process. The amplifier is suitable for more than 100-Gb/s main amplifier. The amplifier achieves a 3-dB bandwidth of 92 GHz. The peak gain is 9-dB with a gain-ripple of less 1.5 dB over the 3-dB bandwidth. The group-delay variation is under ± 4.7 ps over the 3-dB bandwidth. The amplifier consumes 73.5 mW from a 1.2 V supply and results in a gain-bandwidth efficiency figure of merit of 3.53 GHz/mW. The chip occupies an area of 0.45 mm² including the pads.

In chapter 6, a wideband, high-frequency amplifier technique is introduced based on traveling wave amplification. The behavior of the cascaded constructive wave amplifier (CCWA) is analyzed in terms of gain, bandwidth, stability, and noise figure. Using CCWA topology, the W-band (75-111GHz) amplifiers are demonstrated in a 0.12- μm SiGe BiCMOS process with multi cascaded amplification stages and achieves 37.5-dB gain at 90 GHz with a 3-dB bandwidth of 14.6

GHz. Consequently, this amplifier demonstrates a gain-bandwidth product as high as 1,095 GHz. At nominal bias condition, input and output return losses are better than 11 dB over the entire 3-dB bandwidth and the amplifier consumes 65 mW from a 1.8 V. The amplifiers can potentially be used for medical and security imaging, as well as high capacity wireless communications at *W*-band frequencies.

In chapter 7, a fully integrated *Q*-band (40~45 GHz) bidirectional transceiver is demonstrated in a 0.12- μ m SiGe BiCMOS technology. The RF front-end design eliminates the need for transmit/receive switches by demonstrating a novel PA/LNA circuit. The transceiver has a transmit conversion gain of 35 dB with a 3-dB bandwidth of 4 GHz. The OP1dB is 8.5 dBm and Psat is 9.5 dBm. The transceiver has a receive conversion gain of 34 dB with a 3-dB bandwidth of 3 GHz. The noise figure is 4.7 dB and OP1dB is -5 dBm at 43 GHz. The chip consumes 119.4 mW when transmitting and 54 mW when receiving. To the author's knowledge, this work represents the first switchless millimeter-wave bidirectional transceiver in a CMOS or BiCMOS processes. In this chapter, a *W*-band, bidirectional constructive wave amplifier (BCWPA) is also demonstrated in a 0.12- μ m SiGe BiCMOS technology. The amplifier allows symmetric amplification in one of two directions. The amplifier has a peak gain of 16 dB and bandwidth of 14.5 GHz. The center frequency is electronically controlled between 77 and 94 GHz. The amplifier is illustrated to remain stable over all operating conditions. The circuit operates from a 2 V supply and consumes approximately 32 mA under nominal conditions.

Chapter 8 concludes the dissertation with remarks about the future of high-capacity communication for the short-reach optical communication and last-mile wireless communication.

Chapter 2

Revisiting Transimpedance Limits

2.1 Background: Single Stage Transimpedance Limit

Fig. 2.1 illustrates a typical 40-Gb/s optical receiver. A photodetector converts light into current based on the diode responsivity, and the photocurrent is converted into a voltage with a transimpedance amplifier (TIA). The TIA sets the receiver 3 dB bandwidth associated with the photodiode capacitance, C_{PD} , and the input resistance of the transimpedance stage. A shunt feedback TIA is commonly employed because it offers high transimpedance and low input resistance. The shunt feedback amplifier consists of an inverting amplifier with gain, A , and feedback resistance, R_F . The total input capacitance, C_T , is the combination of the photodetector, C_{PD} , and the input of the transimpedance amplifier, C_I . These capacitances generally have equal magnitude for optimum sensitivity [6]. To increase the 3-dB bandwidth associated with C_T , a series inductance can be inserted between the capacitors to add higher-order poles which compensate the current transfer function. The transimpedance transfer function of the shunt feedback TIA is

$$Z_T(s) = -R_T \frac{1}{\left(\frac{s}{\omega_o}\right)^2 + s \frac{1}{\omega_o Q_o} + 1} \quad (2.1)$$

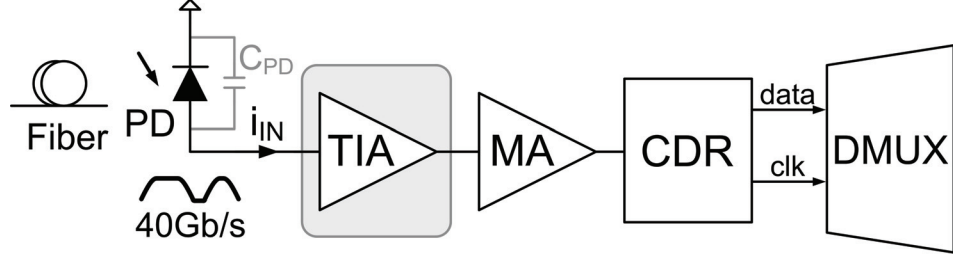


Figure 2.1: Shunt feedback transimpedance amplifier with n -th stage post amplifier

where $R_T = R_F \cdot A/(A+1)$ is the d.c. transimpedance, $\omega_o = \sqrt{\frac{(A+1)2\pi f_A}{R_F C_T}}$ is the transimpedance pole, f_A is the frequency of the dominant open-loop pole of the amplifier, and Q_o is the pole quality factor. A Butterworth response, $Q_o = 1/\sqrt{2}$, is often chosen for maximal gain flatness [6]. For the Butterworth response, the 3-dB bandwidth of the TIA stage is

$$BW_{TIA} = f_o = \frac{\sqrt{2A(A+1)}}{2\pi R_F C_T}. \quad (2.2)$$

Consequently, a well-known transimpedance limit is derived for the Butterworth response based on the shunt feedback topology given a transistor speed, f_T , and is inversely proportional to the square of the required 3-dB bandwidth, BW , [47]; *i.e.*

$$R_T \leq \frac{f_T}{2\pi C_T BW^2}. \quad (2.3)$$

For instance, a 0.13- μm NMOS offers f_T of approximately 85GHz. Additionally, the photodiode capacitance for 30 GHz bandwidth requires the *total* input capacitance to be at least $C_T = 100$ fF. Therefore, the transimpedance is limited to 150 Ω or 43.5dB Ω for a 30GHz bandwidth. Consequently, III-V TIAs are generally preferred because the higher f_T and lower noise outperform silicon receivers for wideband (40-Gb/s+) optical communications [48].

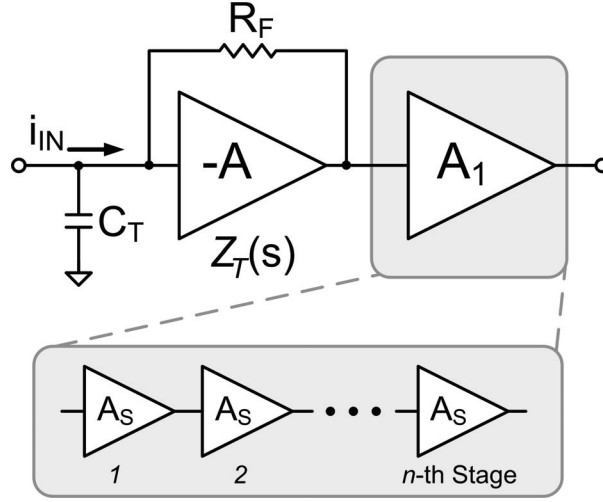


Figure 2.2: Shunt feedback transimpedance amplifier with n -th stage post amplifier

2.2 Transimpedance Limitations in Multistage TIA

Since the shunt feedback amplifier has limited transimpedance at high speeds from (2.3), additional post amplifiers shown in Fig. 2.2 with a total gain, A_1 , are introduced to increase the transimpedance. Each post-amplifier stage introduces additional poles and the bandwidth drops as the number of stages increases. Each of the n post-amplifier stages provides a voltage gain, A_s and is limited to the maximum gain-bandwidth product (GBW) of the device technology, f_T , *i.e.* $GBW = A_s \cdot f_s \leq f_T$ where f_s is the post amplifier bandwidth. The maximum GBW is reduced by undesirable parasitics and mismatched transistor biasing for peak f_T current density.

The overall transimpedance is the product of the transimpedance of the shunt feedback amplifier and the gain of n post amplifier stages; *i.e.*

$$Z_{T,total} = Z_T(s) \prod \frac{A_s}{\left(\frac{s}{\omega_s}\right)^2 + \frac{s}{Q_s\omega_s} + 1}, \quad (2.4)$$

where $Z_T(s)$ is defined in (2.1) and the post amplifier stages are assumed to have a second order response. For maximal gain flatness, the pole quality factor is

also assumed to behave as a Butterworth response, $Q_s = 1/\sqrt{2}$. The overall d.c. transimpedance is increased with additional post-amplifier stages,

$$R_{T,total} = R_T \cdot A_s^n = R_F \frac{AA_s^n}{A+1}, \quad (2.5)$$

but the receiver bandwidth drops rapidly due to the introduction of additional poles. If each post-amplifier has a bandwidth equal to the TIA bandwidth, $f_s = f_o$, then

$$BW_{total} = f_s \cdot (2^{1/(n+1)} - 1)^{1/4}. \quad (2.6)$$

The overall 3-dB bandwidth for two post amplifier stages with 30 GHz bandwidth is $0.7 \times f_o = 21\text{GHz}$ and is unsuitable for 40-Gb/s communication because of the increased intersymbol interference (ISI) and data-dependent jitter (DDJ) [6]. Accordingly, the 3-dB bandwidth of the TIA and post amplifiers must increase to compensate the bandwidth lost by multistage post amplification. Substituting the TIA bandwidth from (2.2) for f_s and the overall transimpedance from (2.5) for R_F , the overall bandwidth is

$$BW_{total} = \frac{A_s^n}{2\pi R_{T,total} C_T} \cdot A \sqrt{\frac{2A}{A+1}} \cdot (2^{1/(n+1)} - 1)^{1/4}. \quad (2.7)$$

A multistage transimpedance limit is found by solving (2.7) for $R_{T,total}$. Since $f_T = A \cdot f_A$, the ratio of the device cutoff frequency to the 3dB bandwidth of the TIA stage is

$$\frac{f_T}{f_o} = \frac{A \cdot f_A}{\frac{\sqrt{2A(A+1)}}{2\pi R_F C_T}} = \frac{A \cdot \frac{2A}{2\pi R_F C_T}}{\frac{\sqrt{2A(A+1)}}{2\pi R_F C_T}} = A \sqrt{\frac{2A}{A+1}}, \quad (2.8)$$

which is valid for $A \gg 1$ for the shunt feedback TIA [6]. Substituting this expression and $A_s \leq f_T/f_s$ for the gain terms in (2.7), and substituting the total 3-dB bandwidth in (2.6) for $f_s = f_o$, the multistage transimpedance limit is

$$R_{T,total} \leq \frac{f_T^{n+1}}{2\pi C_T BW_{total}^{n+2}} (2^{1/(n+1)} - 1)^{(n+2)/4}. \quad (2.9)$$

This is a generalization of (2.3) for n post-amplifier stages using a Butterworth response. In the limit that no post amplification is introduced ($n =$

0), this expression degenerates to (2.3). Fig. 2.3 plots the maximum achievable transimpedance over n stages and illustrates several important results about the possible transimpedance for a given device technology. For $f_T=85$ GHz and $C_T=100$ fF, a desired transimpedance bounds the minimum number of required stages. For example, a total transimpedance of 50 dB Ω requires at least two stages. When the peak f_T is reduced by 10% to 77 GHz, at least four post amplifier stages are necessary to reach a transimpedance of 50 dB Ω . The expression in (4.2) is extremely sensitive to the ratio of f_T/BW_{Total} as the number of stages increases.

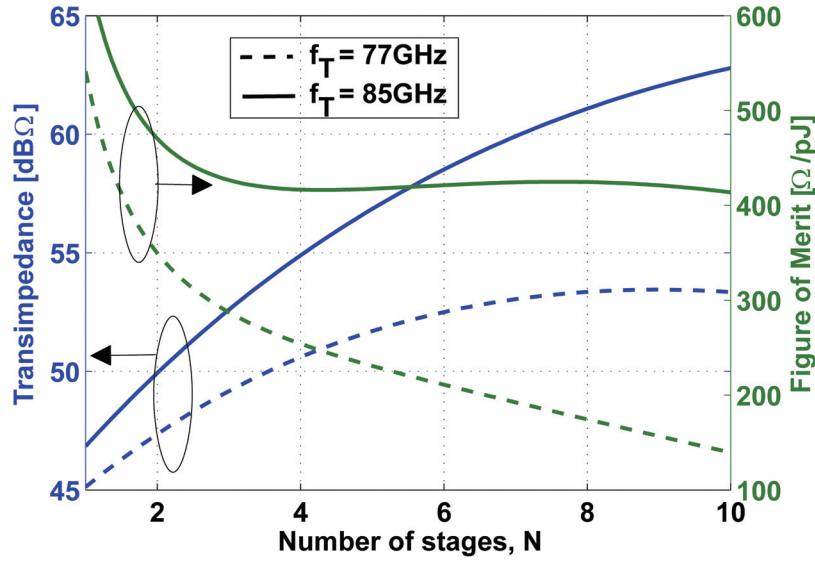


Figure 2.3: Maximum achievable transimpedance and transimpedance-bandwidth per power consumption as a function of the number of cascaded stages of a post amplifier ($C_T=100$ fF and $BW = 30$ GHz)

Secondly, adding post-amplifier stages provides diminishing returns when the device f_T is low compared to the bit rate and the transimpedance reaches a maximum value subject to f_T and C_T . Consequently, introducing additional stages requires too much bandwidth and ultimately reduces the transimpedance gain. For the low f_T shown in Fig. 2.3, the total transimpedance reaches a maximum value at eight stages and begins to gradually drop. The larger bandwidth additionally integrates more input-referred noise current and reduces the overall signal to noise ratio for the receiver. While we have assumed that bandwidth of the TIA and post-

amplifier stages is identical, relaxing this constraint to reduce the TIA bandwidth with respect to the post-amplifier bandwidth arrives at similar limitations.

A useful figure of merit (FOM) for the efficiency of photocurrent conversion is the maximum achievable transimpedance-bandwidth product per d.c. power consumption ($BW\Omega/P_{DC}$) is plotted in Fig. 2.3. This FOM has units of $\text{GHz} \cdot \Omega/\text{mW}$ or Ω/pJ . For $f_T=85$ GHz, this FOM remains constant as adding stages provides a linear improvement in the transimpedance. However, for $f_T=77$ GHz, this FOM decreases substantially as the number of stages increase since the transimpedance increases sublinearly. Lower f_T silicon technologies are particularly strained to achieve both the higher transimpedance but also lower power consumption at 40-Gb/s. To reach the transimpedance limits for a single stage and multistage TIA design, interstage broadband networks are necessary to extend the bandwidth [6]. While previous work has explored techniques for bandwidth enhancement, these networks do not necessarily offer a low group delay variation over the 3dB bandwidth.

2.3 Group Delay Constrained Bandwidth Enhancement

Passive networks such as shunt peaking, series peaking, and t-coil coupling have been proposed to improve the transimpedance-bandwidth limits for high-speed optical communication [16] [17] [18] [19]. In this section, we illustrate an implementation of series peaking that provides bandwidth enhancement while avoiding large group delay variation.

Fig. 2.4 illustrates an inductance, L , inserted in series between two amplifier stages and an equivalent small-signal model for the interstage network. The introduction of series inductance isolates the drain capacitance of the first stage, C_1 , and the gate capacitance of the subsequent stage, C_2 in a π -network [49]. In the absence of the series inductor, the current i_{in} , provided by transconductance of the first common source stage, $i_{in} = g_m\nu_{gs}$, splits between the output resistance, R , and capacitance, $C_1 + C_2$, at the output of the first device and the output voltage

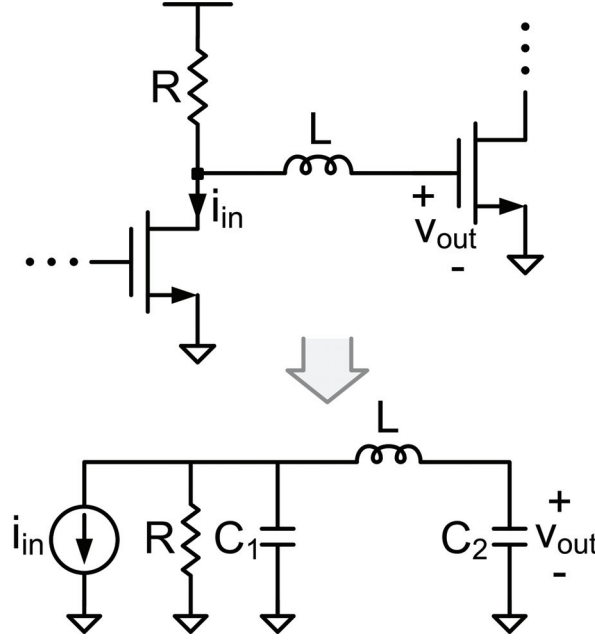


Figure 2.4: Series interstage inductance and the equivalent small-signal model

response, v_{out} , is limited to the RC time constant. Introducing L isolates C_1 and C_2 and the current initially charges C_1 . Therefore the voltage response has more bandwidth but also increased delay [50]. Extending inductive peaking methods to isolate parasitic capacitances provides excellent gain-bandwidth response but accumulates frequency dependent network delay that causes signal distortion.

The transimpedance of the π -network between the drain of one stage and the gate voltage of the subsequent stage with inductive series peaking behaves as a third order response,

$$Z_{\pi}(s) = \frac{v_{out}(s)}{i_{in}(s)} = \frac{R}{s^3 R L C_1 C_2 + s^2 L C_2 + s R (C_1 + C_2) + 1} \quad (2.10)$$

$$= \frac{R}{\left(\frac{s}{\omega_u}\right)^3 m n (1-n) + \left(\frac{s}{\omega_u}\right)^2 m n + \frac{s}{\omega_u} + 1},$$

where $m = L/R^2(C_1 + C_2)$ and $n = C_2/(C_1 + C_2)$ are dimensionless parameters and the frequency response is normalized to $\omega_u = \frac{1}{R(C_1 + C_2)}$, the 3-dB bandwidth for the uncompensated transimpedance with $L = 0$. The m parameter is characterized by the product of the L/R and RC time constants while the n parameter characterizes the capacitance ratio of C_1 and C_2 and is primarily determined by the relative

size of active devices and associated device parasitic capacitances. Assuming the gate capacitance is three times larger than the drain capacitances for devices of similar size, n is approximately $3/4$. Normalizing C_1 and C_2 to 0.25 F and 0.75 F, respectively, the 3-dB bandwidth of uncompensated case is unity and $R = 1 \Omega$.

Table 2.1: Properties of the inductive-series peaking π -network for $n = 0.75$

m	BWER	Phase delay variation ($1/\omega_u$)	Group delay variation ($1/f_u$)	GDV [UI]
0	1	0.215	0.5	0.114
0.3	1.53	0.197	0.397	0.138
0.48	2.13	0.058	0.139	0.067
0.67	2	0.182	0.371	0.169
0.9	1.78	0.412	0.824	0.333

$\omega_u = 2\pi f_u$ is the bandwidth for the uncompensated response

Fig. 2.5 graphs the magnitude of the normalized transimpedance response of the π -network for values of m . The uncompensated case, $m = 0$, provides a reference with unity 3-dB bandwidth. The transimpedance and 3-dB bandwidth are varied as m increases and the bandwidth-enhancement-ratio (BWER) for various values of m are listed in Table I. A Butterworth response (maximally flat magnitude) is achieved when $m = 2/3$ and $n = 3/4$ and yields a 100% improvement in bandwidth. A Bessel response provides maximally flat group delay but is achieved only when $m = 0.48$ and $n = 0.83$ and is not plotted. The BWER for the Bessel response is reduced to 1.8. The lower BWER of the Bessel response significantly degrades the transimpedance limit from (2.8). Clearly, the maximum achievable BWER is 2.13 when $m = 0.48$ and $n = 0.75$ and the BWER decreases as m increases beyond 0.48.

A trade-off between BWER and the phase linearity is often overlooked for bandwidth enhancement techniques. Linear phase delay is represented by a flat group delay response. Large group delay variation results in data-dependent jitter

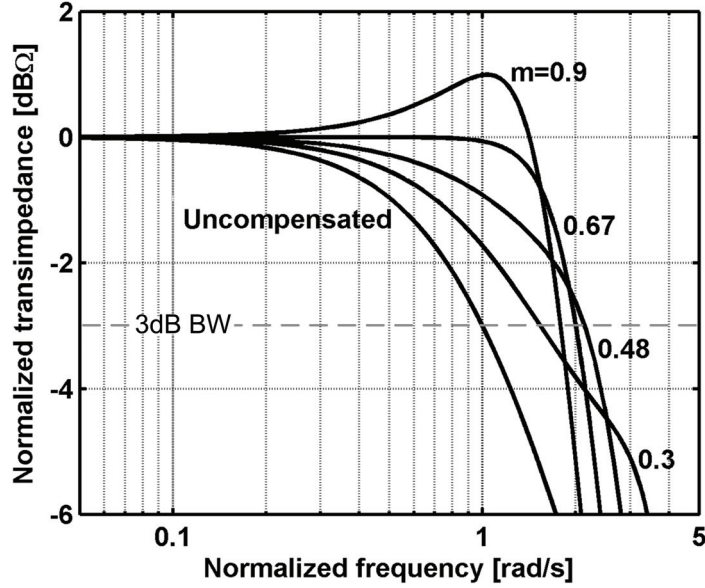


Figure 2.5: Normalized transimpedance response of inductive-series peaking π -network with different m values using (2.10) ($R = 1\Omega$ and $n = 3/4$)

which degrades the signal integrity of the data eye. The denominator in (2.10) is a third-order polynomial with at least one real pole, $s_1 = \sigma_1$, and two complex poles, $s_2, s_3 = \sigma_2 \pm j\omega_2$. The phase response is obtained by $\phi_k(\omega)$ and summing the phase contribution of each pole [51].

$$\phi(\omega) = \arg\{Z_\pi(\omega)\} = \sum_{k=1}^3 \arctan \frac{\omega \pm \omega_k}{\sigma_k}. \quad (2.11)$$

The normalized Butterworth poles are $s_1 = -2$ and $s_2, s_3 = -1 \pm j1.73$. The normalized Bessel poles are $s_1 = -2.32$ and $s_2, s_3 = -1.84 \pm j1.75$. For the maximum BWER, the normalized poles are $s_1 = -1.51$ and $s_2, s_3 = -1.24 \pm j2.41$. Since the group delay is defined by $\tau_g = -\frac{d\phi(\omega)}{d\omega}$, the group delay for the π -network is found by differentiating (2.11); *i.e.*

$$\tau_g = - \sum_{k=1}^3 \left(\frac{\sigma_k}{\sigma_k^2 + (\omega \pm \omega_k)^2} \right). \quad (2.12)$$

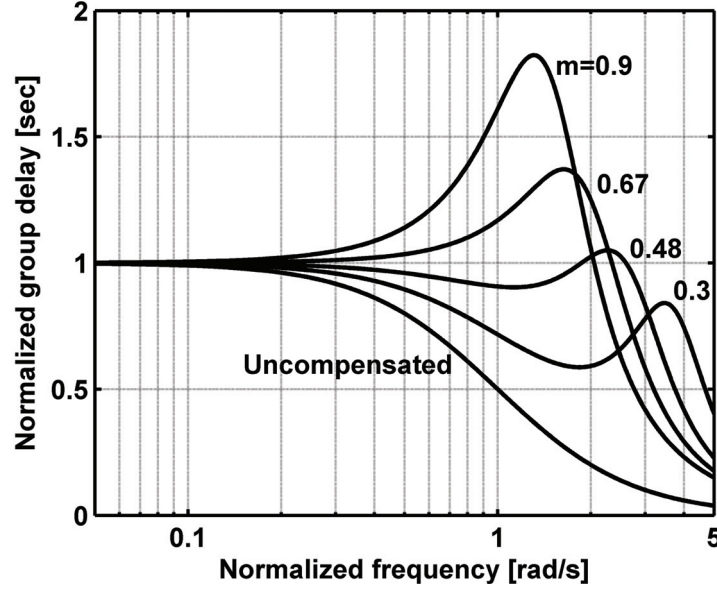


Figure 2.6: Normalized group delay response of inductive-series peaking π -network with different m values using (2.10) and (2.13) ($R = 1\Omega$ and $n = 3/4$)

Fig. 2.6 plots the group delay for the inductive series-peaking response and can be compared to the frequency response in Fig. 2.5. We find that while there are several responses that offer high BWER the group delay of the response is not always minimized for the BWER. Referring back to Table I, we can predict the group delay variation normalized to the unit interval. Since the BWER is used to achieve a suitable bandwidth for optical communication, typically $f_{3dB} = BWER \cdot f_u = 0.7f_b$ where f_b is the bit rate, the group delay variation is related to the BWER, *i.e.*

$$GDV [UI] = \frac{1}{0.7 \times 2\pi} \cdot GDV_u \cdot BWER, \quad (2.13)$$

where GDV_u is the group delay variation normalized to the uncompensated 3dB bandwidth. For the uncompensated response ($m = 0, n = 0.75$), the group delay variation is $\sim 0.114UI$, while for the Butterworth response the group delay variation is $\sim 0.169UI$. This is nearly three times the group delay variation for a comparable second-order Butterworth response (*i.e.* $\sim 0.06UI$). If multiple stages

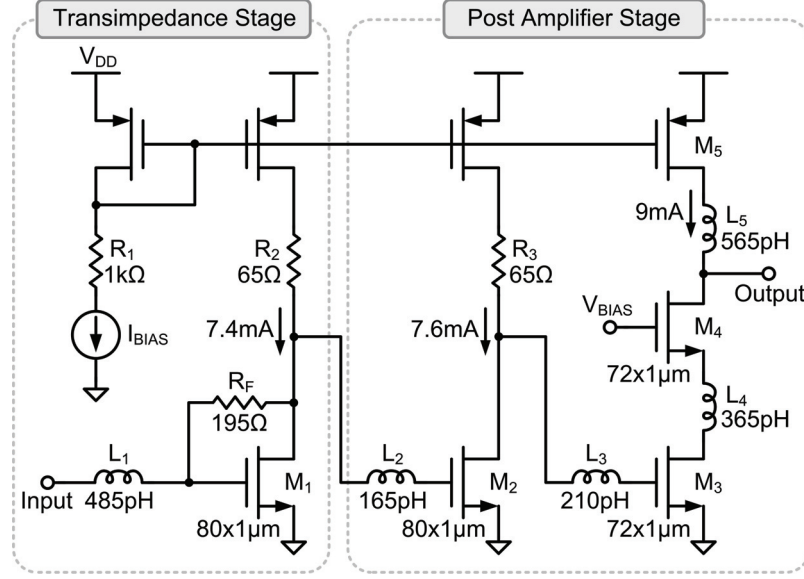


Figure 2.7: Circuit schematic of proposed transimpedance amplifier

each with a Butterworth response are cascaded as proposed in the derivation of Section 2.2, the group delay accumulates through the additional poles introduced to (2.12) and the circuit would have an undesirably large group delay variation with respect to the unit interval. Neither the Bessel nor Butterworth responses are particularly attractive for multistage inductive-series peaking π -networks. For the maximum BWER illustrated in Table I ($m = 0.48$ and $n = 0.75$), the group delay variation is $\sim 0.067UI$ and is the most desirable response. Our circuit design tailors these results to the group-delay optimized π -network in a multistage TIA for bandwidth enhancement.

2.4 TIA Circuit Implementation

The 40-Gb/s transimpedance amplifier (TIA) is realized in a 0.13- μm CMOS technology with $f_T = 85\text{ GHz}$. Fig. 2.7 shows that the proposed TIA which consists of three stages including one transimpedance stage and two-stage post amplifier that employ interstage inductive-series π -network for low group delay variation and wide bandwidth.

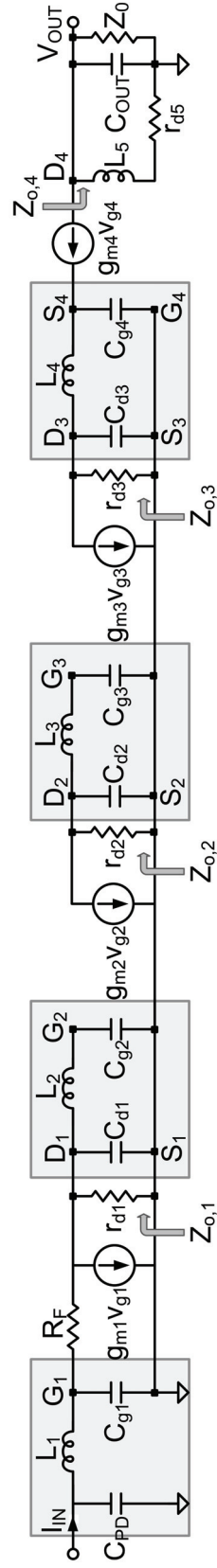


Figure 2.8: Simplified circuit schematics of each stage including the photodetector capacitance with equivalent small-signal model

2.4.1 Transimpedance Stage

The transimpedance stage is implemented with common source NMOS, M_1 , and PMOS load. Fig. 2.8 shows the small-signal model of the proposed TIA with interstage inductive-series π -networks. The PMOS FETs are used for current-source loads. From the simulation, the drain currents of M_1 , M_2 and M_3 are 7.38 mA, 7.55 mA and 8.97 mA, respectively. In Fig. 2.7, all stages are d.c. coupled. The resistances R_2 and R_3 are inserted between the current-source load and the drains of M_1 and M_2 to match the bias voltages and drain currents across each of the amplifier stages but could be eliminated with reduced sizing of the PMOS load.

The finite gain of the TIA amplifier, M_1 , creates a finite input impedance of the transimpedance stage, *i.e.* $R_{in} = R_F/(A+1)$. In this design, the input impedance is matched to $50\ \Omega$ for electrical measurement. The photodiode capacitance is bounded between 50 fF and 80 fF based on commercially available 30 GHz photodiodes and the bondpad capacitance contributes around 40 fF [52]. The input pole for the TIA is

$$\omega_p = \frac{A+1}{R_F C_T} = \frac{1}{R_{in} C_T}. \quad (2.14)$$

For $50\ \Omega$ input impedance, the 3dB cutoff is under 28 GHz if $C_T \geq 113\text{ fF}$. To relax this bandwidth constraint, inductor $L_1 = 485\text{ pH}$ is inserted in series between the bondpad and the transimpedance stage. Isolating the photodiode capacitance, the pole is increased to approximately $\frac{A+1}{R_F C_I}$. The transimpedance transfer function from (2.1) is expressed in terms of the circuit parameters in Fig. 2.8 as

$$\begin{aligned} Z_T(s) &= \frac{v_{D1}(s)}{i_{in}(s)} \\ &= \frac{Z_{o,1}(g_{m1}R_F-1)}{g_{m1}Z_{o,1}+1} \frac{1}{s^3\tau_{t3}+s^2\tau_{t2}+s\tau_{t1}+1} \end{aligned} \quad (2.15)$$

where $\tau_{t1} = \frac{R_F+Z_{o,1}}{g_{m1}Z_{o,1}+1}C_T$, $\tau_{t2} = L_1C_{PD}$, and $\tau_{t3} = \frac{R_F+Z_{o,1}}{g_{m1}Z_{o,1}+1}L_1C_{PD}C_I$. The transimpedance depends on the output impedance of the first stage, $Z_{o,1}$, as well as R_F . The output impedance of each stage is

$$Z_{o,x} = \frac{s^2C_{g,x+1}L_{x+1}r_{d,x} + r_{d,x}}{s^3\tau_{i3} + s^2\tau_{i2} + s\tau_{i1} + 1} \text{ for } x = 1, 2 \text{ and } 3, \quad (2.16)$$

where $\tau_{i1} = r_{d,x}(C_{g,x+1} + C_{d,x})$, $\tau_{i2} = L_{x+1}C_{g,x+1}$, and $\tau_{i3} = r_{d,x}L_{x+1}C_{g,x+1}C_{d,x}$.

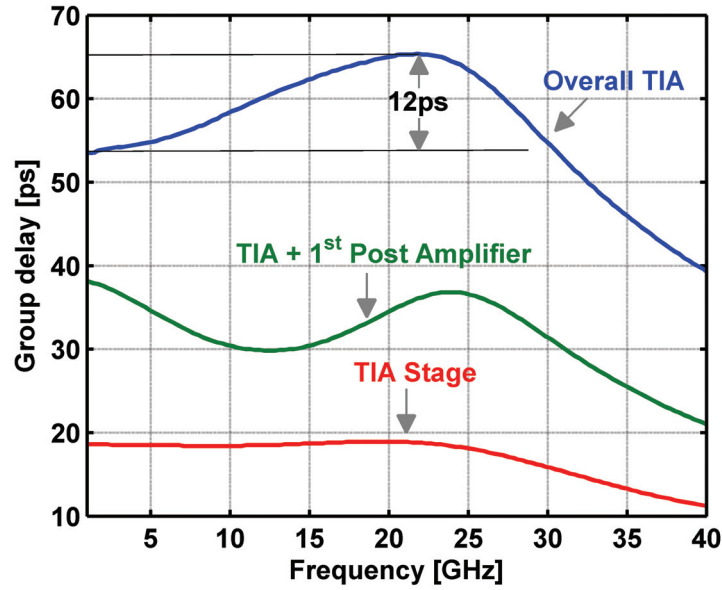


Figure 2.9: Spectre simulations of group delay through multistage TIA

The poles of the transimpedance stage in (2.15) can be chosen according to the analysis for BWER and group delay variation in (2.10) in Section 2.3. Since the π -network is reciprocal, (2.10) is still valid except the capacitance ratio becomes $n = (C_{PD}) / (C_{PD} + C_I)$. In this case, the value of n is approximately 0.8. Based on (2.10) and (2.13), the parameter, m , for minimum group delay variation is chosen (≈ 0.52) to achieve minimum group delay variation over the 3-dB bandwidth of the TIA stage as shown in Fig. 2.9.

Fig. 2.10 graphs the Spectre simulations of the frequency response of the TIA stage and compares it to the analysis from (2.15). The predicted frequency response is accurate over the 3-dB bandwidth but the analysis predicts a slightly higher bandwidth due to an underestimation of the poles above the simulated 3dB bandwidth. The low group delay of the first TIA stage causes transimpedance ripple of 5 dB Ω at 18 GHz as shown in Fig. 2.10. Therefore, extending the 3-dB bandwidth with low group delay variation in the post amplifier stages requires the π -network over the two subsequent stages to compensate the TIA transimpedance ripple.

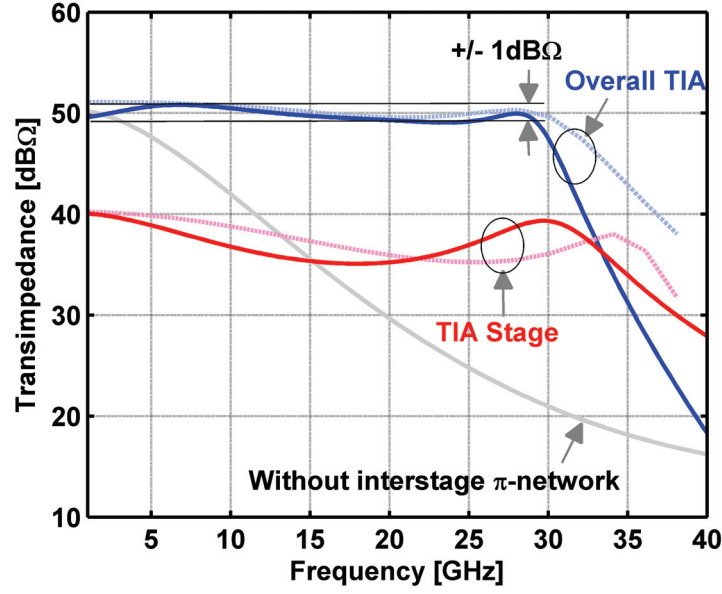


Figure 2.10: Spectre simulations (solid lines) and analytical results (dotted lines) using Equ. (2.15)-(2.19) of the transimpedance in a multistage TIA

2.4.2 Post Amplifier Stages

Two post amplifier stages with interstage inductive-series peaking provide voltage gain while mitigating group delay variation. The interstage voltage gain from node D_x to D_{x+1} is expressed as

$$\begin{aligned} \frac{v_{D,x+1}}{v_{D,x}} &= g_{m,x+1} Z_{\pi,x+1} \frac{Z_{o,x+1}}{Z_{o,x}} \\ &\approx g_{m,x+1} Z_{\pi,x+1}, \text{ for } x = 1 \text{ and } 2', \end{aligned} \quad (2.17)$$

where the output impedances for consecutive stages cancel to the extent that their impedances over the frequency response are identical. Consequently, the π -network transfer function described in (2.10) gives the frequency response and the overall transimpedance is derived as

$$Z_{T,total} = Z_T(s) \prod_{x=1}^n g_{m,x+1} Z_{\pi,x+1}(s). \quad (2.18)$$

The first common source post-amplifier, M_2 , absorbs C_{d1} and C_{g2} , into the π -network in Fig. 2.8. Based on the device capacitances, the capacitance ratio, n , is 0.75.

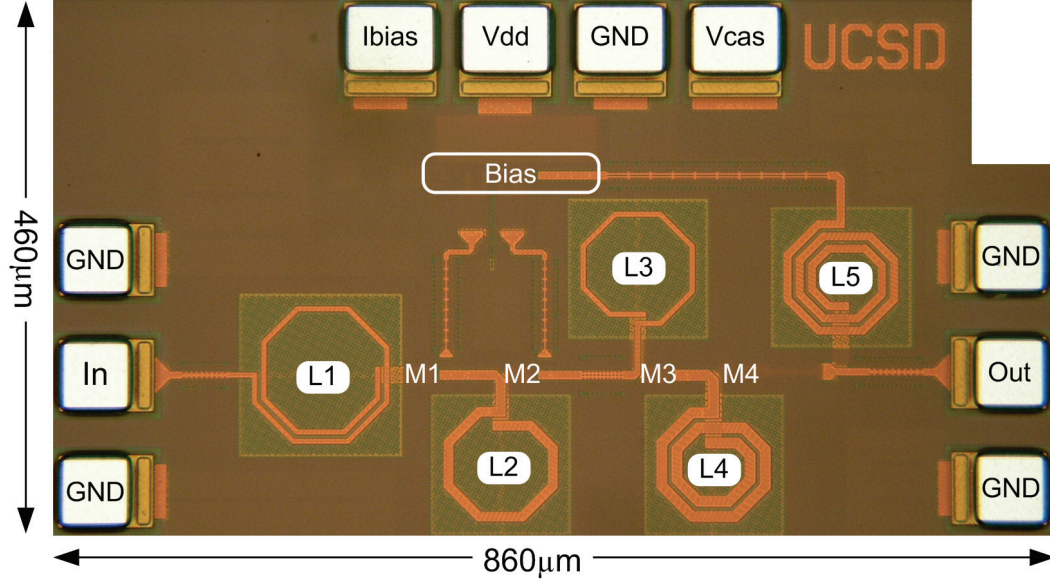


Figure 2.11: Chip microphotograph of the transimpedance amplifier in 0.13- μm CMOS

Given an output resistance of the transimpedance stage of $100\ \Omega$ and total capacitance at the output of M_2 of 35 fF, m is 0.48 if $L_2 = 165\text{ pH}$. The second common source stage absorbs C_{d2} and C_{g3} . Given a higher output resistance at the first transimpedance amplifier stage of $120\ \Omega$ and total capacitance at the output of M_2 of 30 fF, m is 0.48 if $L_3 = 210\text{ pH}$. Consequently, the transimpedance of the TIA and 1st post-amplifier increases uniformly across the 3dB bandwidth in Fig. 2.10. A group delay variation of 10 ps is introduced in the response as shown in Fig. 2.9. In Fig. 2.7, resistor R_3 is inserted between PMOS and NMOS drain to shift the bias the consecutive NMOS gate.

The last stage is a cascode of M_3 and M_4 with an interstage π -network consisting of C_{d3} and C_{g4} and L_4 to compensate the transimpedance ripple. In this cascode network, n is approximately 0.75 but $m \approx 0.8$ to create midband peaking for flat overall transimpedance. Additionally, inductor L_5 provides shunt peaking. Consequently, the output impedance seen at the final cascode node is

$$Z_{o,4} = Z_o \parallel r_{d5} \frac{1 + sL_5/r_{d5}}{s^2 L_5 C_{out} \left(\frac{Z_o}{r_{d5} + Z_o} \right) + s \left(C_{out} \cdot Z_o \parallel r_{d5} + \frac{L_5}{r_{d5} + Z_o} \right) + 1} \quad (2.19)$$

As seen in Fig. 2.9, the group delay illustrates peaking near 20 GHz but maintains an overall simulated group delay variation at 12 ps over the 3-dB bandwidth. Fig. 2.10 illustrates that inductive peaking in the TIA provides a 3-dB bandwidth of 30GHz; five times the bandwidth absent any inductive-series peaking technique. Spectre simulations of the circuit are compared with the analytical result from calculating (2.18) in Fig. 2.10 and again show agreement to the 3-dB bandwidth of the circuit. Additionally, the circuit simulation for the transimpedance matches the prediction of the maximum achievable transimpedance of $\approx 50 \text{ dB}\Omega$ for $N = 3$ in Fig. 2.3. Therefore, the proposed TIA design achieves the desired bandwidth enhancement with low group delay variation.

2.5 Measurements

The circuit is implemented in 0.13- μm IBM 8RF-LM CMOS technology with $f_T \approx 85 \text{ GHz}$. This technology has a digital back-end-of-the-line with 1 μm thick copper interconnects. The chip microphotograph is shown in Fig. 2.11 and occupies an area of 0.86mm x 0.46mm (0.4mm²) including the pads.

S-parameters are measured using the Agilent E8361A two-port network analyzer and on-wafer probing with Picoprobe coplanar 67A GSG probes for S-parameters, noise figure and eye diagram measurements. The transimpedance is derived from the measured S-parameters as

$$Z_T = Z_0 \frac{S_{21}}{1 - S_{11}}, \quad (2.20)$$

where Z_0 is the characteristic impedance of 50 Ω [53]. The measured transimpedance is reported in Fig. 2.12 and demonstrates a transimpedance of 50 dB Ω with a 3-dB bandwidth of 29 GHz. The transimpedance rolls off to the 3-dB bandwidth with no gain peaking. At low frequency, the external bias-tee limits the frequency response measurement.

Since only the bondpad parasitic capacitance is present, the photodiode capacitance is not taken into account in the measurement. Practically, a photodetector and the TIA chip are, however, co-located in the same package or module to

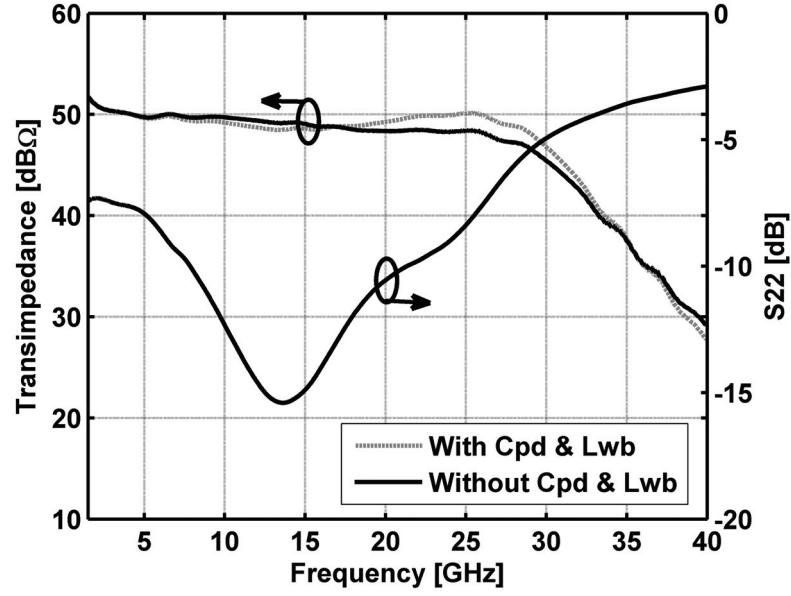


Figure 2.12: Measured transimpedance gain and output return loss (solid lines) and extracted transimpedance gain (dotted line) simulated with $C_{PD} = 50 \text{ fF}$ and $L_{BW} = 0.22 \text{ nH}$

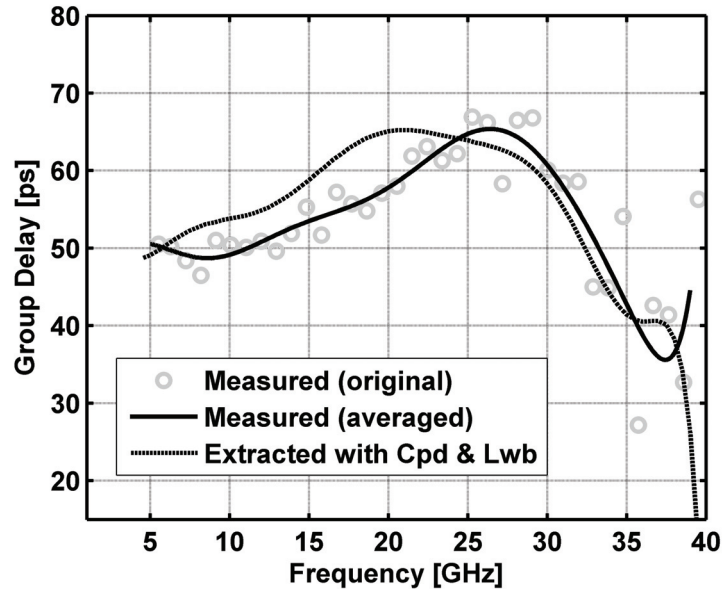


Figure 2.13: Measured transimpedance group delay variation (solid line) and extracted transimpedance group delay variation (dotted line) simulated with $C_{PD} = 50 \text{ fF}$ and $L_{BW} = 0.22 \text{ nH}$

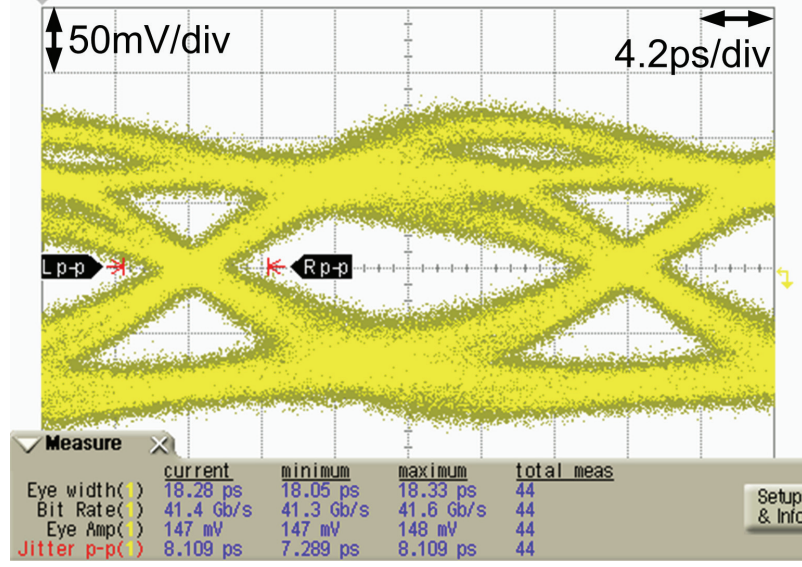


Figure 2.14: Measured eye diagram with a 40-Gb/s $2^{31} - 1$ PRBS

minimize the interconnect parasitics between the detector and the TIA. The bond-wire offers an additional inductance, L_{WB} , and contributes to the TIA matching above 10 GHz. The TIA frequency response is extracted from a simulation of the measured TIA S-parameter data and an input network comprised of a 40-Gb/s InGaAs PIN diode, $C_{PD} = 50 fF$, and a series ribbon interconnect inductance between the PIN and TIA of 0.22 nH [52]. The transimpedance 3-dB bandwidth is 29.9 GHz and the overall gain exhibits small peaking. The measured output return loss is better than 10 dB between 7.7 GHz and 22 GHz but is better than 7.5 dB below 7.7 GHz and 5.7 dB between 22 and 29-GHz. Low return losses at low and high frequencies are introduced by the output inductors L_4 and L_5 . The TIA is unconditionally stable over the entire bandwidth with a minimum K -factor of 1.8 determined from the measured S -parameters.

The group delay variation is illustrated in Fig. 2.13. The group delay is measured from S -parameters and translated to transimpedance group delay. The S -parameter group delay is lower than the transimpedance group delay because of the dependence on the input return loss in (2.20). The TIA has nominal a transimpedance group delay of 50 ps and increases to 66 ps. The overall measured group delay variation is 16 ps over the 3-dB bandwidth and matches the group

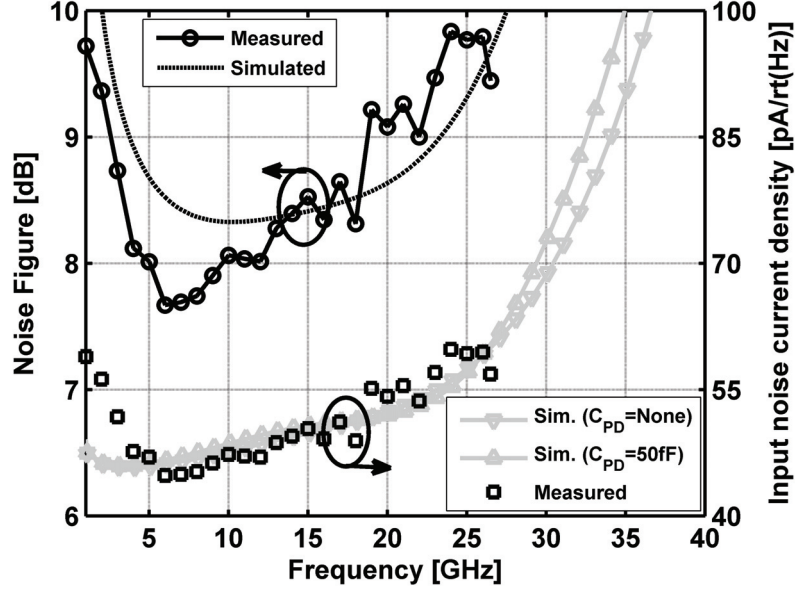


Figure 2.15: Measured noise figure and input noise current density with/without C_{PD}

delay from Spectre simulations.

The eye diagram is measured using Agilent 86100A DCA wide-bandwidth oscilloscope. A $2^{31} - 1$ pseudorandom bit sequence (PRBS) is generated from a Centellax TG1P4A pulse pattern generator. Fig. 2.14 shows the measured output eye diagram for a data rate of 40-Gb/s. With an input current swing of $460 \mu A_{PP}$, the output voltage swing is $147 mV_{PP}$.

The output eye diagram indicates that the peak-to-peak jitter is about 8.1 ps where the original input signal has the peak-to-peak jitter of 7.4 ps. Consequently, the TIA introduces a small amount of additional deterministic jitter to the signal. Some amplitude distortion occurs near the upper voltage level of the eye. Since the rising and falling responses of our measured data eye are not symmetric, this indicates slight non-linearity caused by device depletion capacitances. Additionally, some bandwidth limitation is introduced by the microwave attenuators (3.5 mm connector) and cabling that were used to reduce the input swing of the 40-Gb/s PRBS from its nominal 600mV swing.

The precise impact of the photodiode capacitance on the eye-diagram can-

not be determined experimentally with an electrical eye measurement. In [13], an on-chip capacitor is integrated with the chip to act as a surrogate for the photodiode capacitance. This is about the best way to deduce circuit performance with a photodiode capacitance but this technique does not necessarily capture the shot noise generation of the photodiode.

The measured and simulated noise figure are plotted in Fig. 2.15. The noise figure (NF) is measured using an Agilent E4440 spectrum analyzer with an Agilent 346C noise source. The minimum NF is 7.6 dB at 6 GHz and the maximum NF is 9.8 dB at 24 GHz. The input current noise density of the TIA is calculated from the measured noise figure up to 26.5 GHz and illustrates agreement with the simulations over this band with and without the photodiode capacitance. The simulations of the noise current density are shown up to twice the 3-dB bandwidth to illustrate the deviation caused by a 50 fF photodiode capacitance. The input-referred noise current is determined by integrating the simulated noise current density up to twice the 3dB bandwidth and we find an RMS input noise current of $8.82\mu A$ with $C_{pd} = 0 fF$ and $8.98\mu A$ with $C_{pd} = 50 fF$ [54]. Following the technique suggested in [13], the average input-referred noise current density is $51.8 pA/\sqrt{Hz}$.

The chip consumes 45.7 mW from a 1.5 V supply and the transimpedance-bandwidth FOM is $200.7 \Omega/pJ$ and represents the exceptional figure of merit performance compared to recent publications on 40-Gb/s TIAs in Table 2.2. While previous work was demonstrated in $0.18\text{-}\mu m$ CMOS, a severe drawback of this previous work is the dramatic group delay variation, often not reported, that is introduced with bandwidth enhancement techniques that are designed exclusively for maximum 3-dB bandwidth. This work demonstrates low group delay variation while still offering the smallest active area and power consumption compared to prior publications on 40-Gb/s TIAs in CMOS.

Table 2.2: Comparison of reported 40-Gb/s transimpedance amplifiers

Ref.	Process	Bit Rate (Gb/s)	BW (GHz)	Z_T (dB Ω)	GD (ps)	S22 (dB)	Noise (pA/ $\sqrt{Hz}$)	Supply (V)	Power (mW)	Area (mm ²)	$BW\Omega/P_{DC}$ (Ω /pJ)
[48]	DHBT $f_T=160G$	40	47	50*	–	-15	35	5.2	458	0.66	64.7**
[53]	SiGe $f_T=200G$	40	50	43*	–	-12	30	5.2	182	0.92	77.4**
[55]	0.18 μ m CMOS	40	30	48	–	—	20***	1.8	50.4	1.04	149.5
[13]	0.18 μ m CMOS	40	30.5	51	125	-10	55.7 (sim.)	1.8	60.1	0.54	180.1
This work	0.13 μ m CMOS	40	29	50	16	-7.4	51.8 (sim.)	1.5	45.7	0.4	200.7

*: single-ended gain, **: calculated with differential gain, *** up to 18GHz

2.6 Conclusions

In this paper, a series peaking π -network is discussed for optimized bandwidth enhancement with respect to group delay variation over multiple stages. A novel analysis of the maximum transimpedance with multistage post-amplifiers determines the maximum transimpedance for a given f_T . A 50 dB Ω transimpedance gain, 40-Gb/s transimpedance amplifier is implemented in 0.13- μ m CMOS process. The bandwidth of the TIA is 29 GHz and group delay variation is under 16 ps over the entire 3-dB bandwidth. The $BW\Omega/P_{DC}$ is 200.7 Ω /pJ.

Acknowledgments

Chapter 2 is in-part mostly a reprint of the material as it appears in IEEE Transactions on Circuits and Systems I: Regular Papers, 2010. Joohwa Kim; James F. Buckwalter. This dissertation author was the primary author of this material.

Chapter 3

40-Gb/s SOI Transceiver Front-ends

3.1 Circuit Design

In this chapter, a SOI process is used to reduce the power consumption of a high-speed transceiver. The circuit design consists of a high-voltage driver and low-power receiver demonstrated in a SOI technology shown in gray in Fig. 3.1.

3.1.1 50 Ω Modulator Driver

Modulator drivers require high-voltage swing ($>2V_{PP}$) to induce a 180 degree (π) phase shift in the MZM. This is at odds with highly scaled CMOS where the low breakdown voltage and high knee voltage of the device limits the drain voltage swing [20]. Fig. 3.2(a) shows the conventional cascode configuration which has been used to eliminate the effects of oxide breakdown voltage and the hot carrier degradation [56]. The common-source and common-gate transistors are connected in series to allow the use of a larger supply voltage. However, the conventional cascode configuration does not equally divide the voltage stress between the two transistors since the common-gate transistor M_2 has a constant dc voltage v_{cg2} with an ac ground. Consequently, the common-gate transistor M_2 is stressed more, severely across its drain and gate terminals since $|v_{c2} - v_{cg2}| \approx v_{c2}$. In the

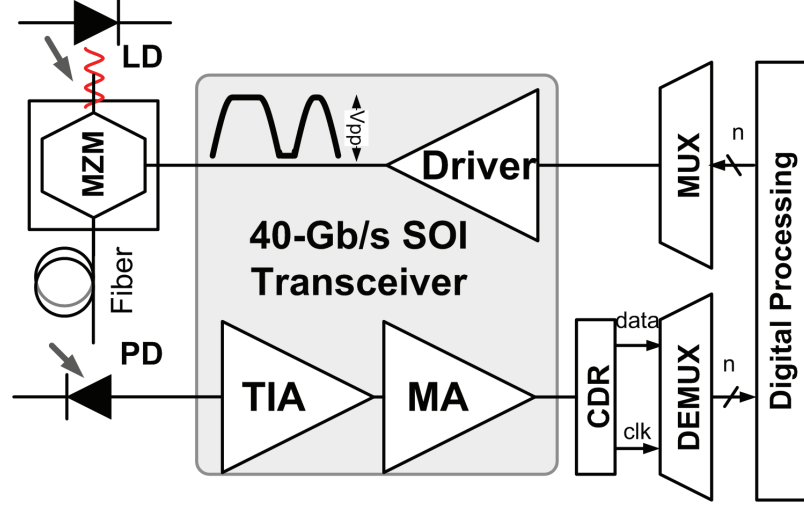


Figure 3.1: Block diagram of a typical 40-Gb/s optical transceiver.

conventional cascode configuration, the input impedance Z_{c1} is seen at the source of the cascode is

$$Z_{c1} = \frac{Z_{c2} + r_{o2} + sC_{gd2}r_{o2}Z_{c2}}{1 + g_{m2}r_{o2} + s[g_{m2}C_{gd2}Z_{c2}r_{o2} + Z_{c2}(C_{gs2} + C_{gd2})]}. \quad (3.1)$$

where g_{m2} is the transconductance of M_2 , r_{o2} is the output impedance of M_2 , and Z_{c2} is the impedance seen looking into the load.

By assuming the gate-to-drain capacitance C_{gd2} is negligible and $r_{o2} \gg Z_{c2}$, Z_{c1} can be simplified to $1/g_{m2}$.

To achieve a high output voltage swing, SOI technologies offer a unique opportunity to build broadband high-voltage drivers using FET stacking technique [57]. The stacked FET technique allows the gate, drain, and source of each transistor in the stack to swing in unison to prevent drain-source voltages that might breakdown the gate or channel of the device. SOI is chosen for this technique because the body of each FET is isolated from the bulk silicon material. Fig. 3.2(b) shows the stacked FET driver that is composed of a common-source input transistor M_1 and two stacked transistors M_2 and M_3 connected in series so that their output swings are added in phase. In contrast to the conventional cascode configuration where the gate of the common-gate transistor is a high frequency ground, relatively small external gate capacitances (C_1 and C_2) are added to allow

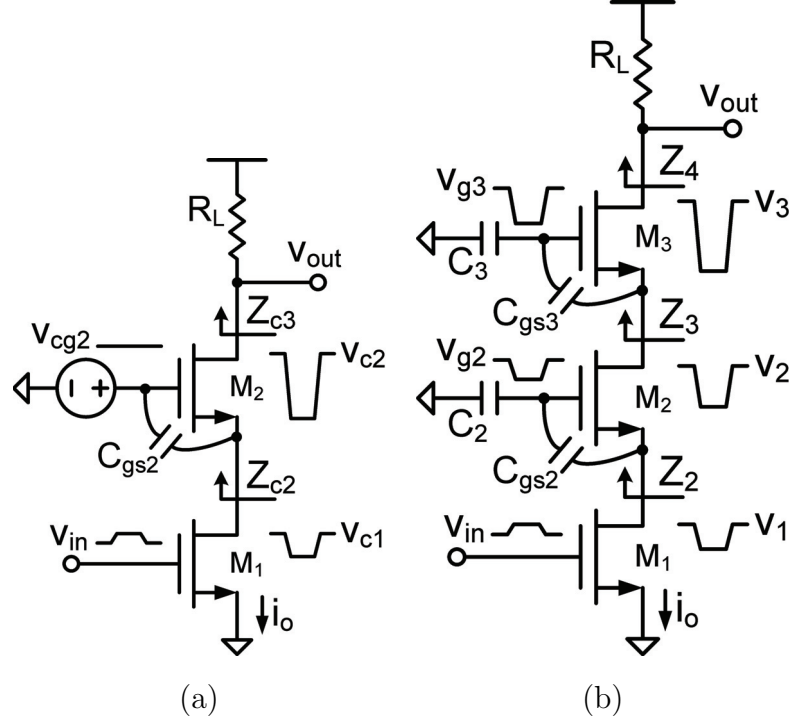


Figure 3.2: Simplified schematics of (a) conventional cascode driver and (b) stacked-FET driver.

an voltage swing at the gate of each stacked transistor. The external gate capacitances (C_1 and C_2) and the gate-to-source capacitances (C_{gs2} and C_{gs3}) create the capacitive voltage divider to produce the proper in-phase voltage swing at the gate and drain [57], *i.e.* $v_{g2} = v_1 \cdot (C_{gs2}/C_1)$.

With this modification, the impedance seen looking into the source of transistor i is

$$Z_i = \frac{C_i + C_{gs(i+1)} + C_{gd(i+1)} [1 + g_{m(i+1)}Z_{(i+1)} + sZ_{(i+1)}(C_i + C_{gs(i+1)})]}{(g_{m(i+1)} + sC_{gs(i+1)}) (C_i + C_{gd(i+1)} + sC_iC_{gd(i+1)}Z_{(i+1)})}, \quad i = 2, 3. \quad (3.2)$$

By assuming that the feedback current through the gate-to-drain capacitance C_{gd} is negligible, the equation simplifies to

$$Z_i = \left(1 + \frac{C_{gs(i+1)}}{C_i}\right) \cdot \left(\frac{1}{g_{m(i+1)}} \parallel \frac{1}{sC_{gs(i+1)}}\right), \quad i = 2, 3. \quad (3.3)$$

Notably, unlike in (3.1), given the transistor size and bias condition, the

source input impedance is determined by the external gate capacitance C_i . The values of external capacitors (C_1 and C_2) should be chosen for $Z_1 = v_1/i_o$ and $Z_2 = v_2/i_o \approx 2 \cdot Z_1$, and $Z_3 = v_3/i_o \approx 3 \cdot Z_1$ so that the voltage stress (v_{ds} , v_{dg} , and v_{gs}) is equally divided between transistors ($M_1 \sim M_3$). However, unlike in a power amplifier design [57], the choice of external capacitors (C_1 and C_2) is more restrictive in the broadband amplification. Fig. 3.4 shows that output voltage waveforms at 40-Gb/s for different values of C_1 . The values of external capacitors (C_1 and C_2) should be set such that C_1 and C_2 are C_{1opt} and C_{2opt} , respectively to avoid overshooting or undershooting in the eye-diagram, resulting in intersymbol interference (ISI) [6].

Fig. 3.3 shows the proposed differential modulator driver consisting of a common-source FETs, M_1 and M_4 , and two stacked FETs, $M_{2\sim3}$ and $M_{5\sim6}$. The gate of each stacked FET is isolated from ground to allow self-biasing of the gate

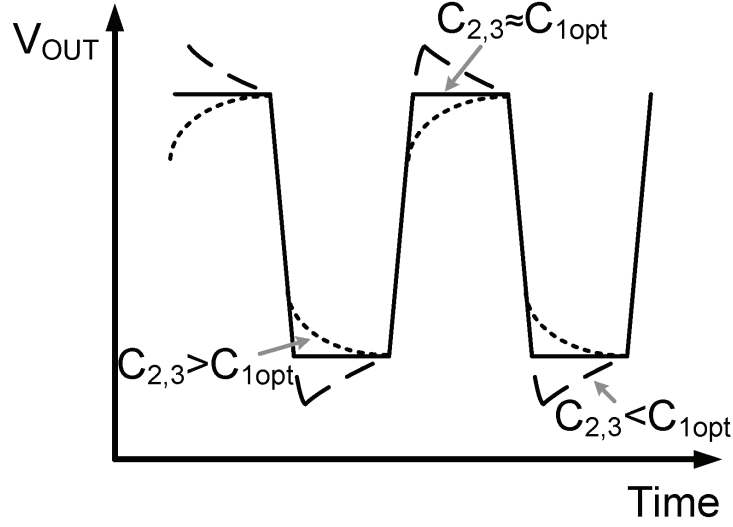


Figure 3.4: Output voltage waveforms for different values of C_1 .

and avoid the gate-to-drain and drain-to-source breakdown voltages at high drain voltages. The gate of M_2 is decoupled with a small external capacitance, C_1 to couple the drain swing v_1 into the gate of M_2 through the gate-source capacitance (C_{gs}) of M_2 [57]. The external capacitance C_2 is also used to couple the drain swing v_2 into the gate of M_3 through C_{gs3} . The external gate capacitances C_1 and C_2 are 147 fF and 68 fF, respectively, and are realized as a vertical natural capacitor (VNCAP) in the bottom metal layers with a 374 nm spacing between the metal plates. The d.c. gate bias voltages are applied using a resistive voltage divider created by R_1 , R_2 and R_3 that maintains a nominal gate-source voltage (v_{gs}) across each transistor of approximately 500 mV.

The stacked devices are connected in series to combine drain-source voltage swings from each transistor in phase and increase the intrinsic on-resistance of the stacked FET. Fig. 3.5 shows the simulated drain voltage waveforms at 40-Gb/s. The drain-source voltage swing of M_1 , V_1 , does not exceed 1.2 V. Similarly, the drain-source voltage swing of M_2 , $V_2 - V_1$, does not exceed 1.2 V. Finally, the swing at M_3 , $V_{out} - V_2$, is not more than 1.2 V and, consequently, the predicted output voltage swing is 2 V peak-to-peak.

The bandwidth required for 40-Gb/s operation is at least 28 GHz to avoid

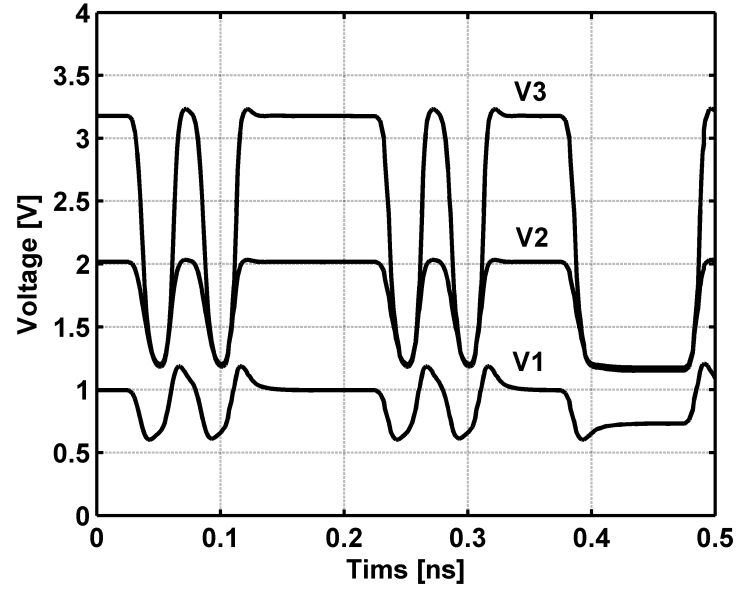


Figure 3.5: Simulated drain voltage waveforms for 40-Gb/s.

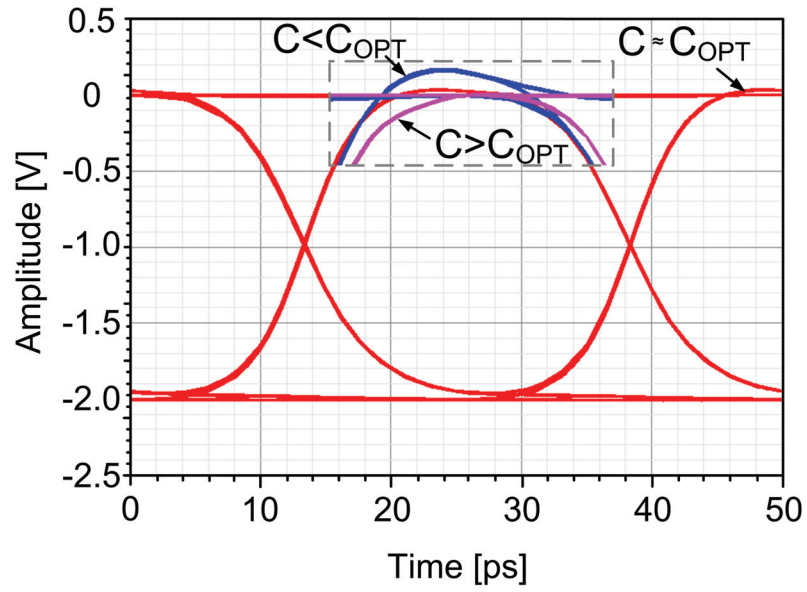


Figure 3.6: Simulated output eye diagram of modulator driver with 700mVpp input swing for 40-Gb/s.

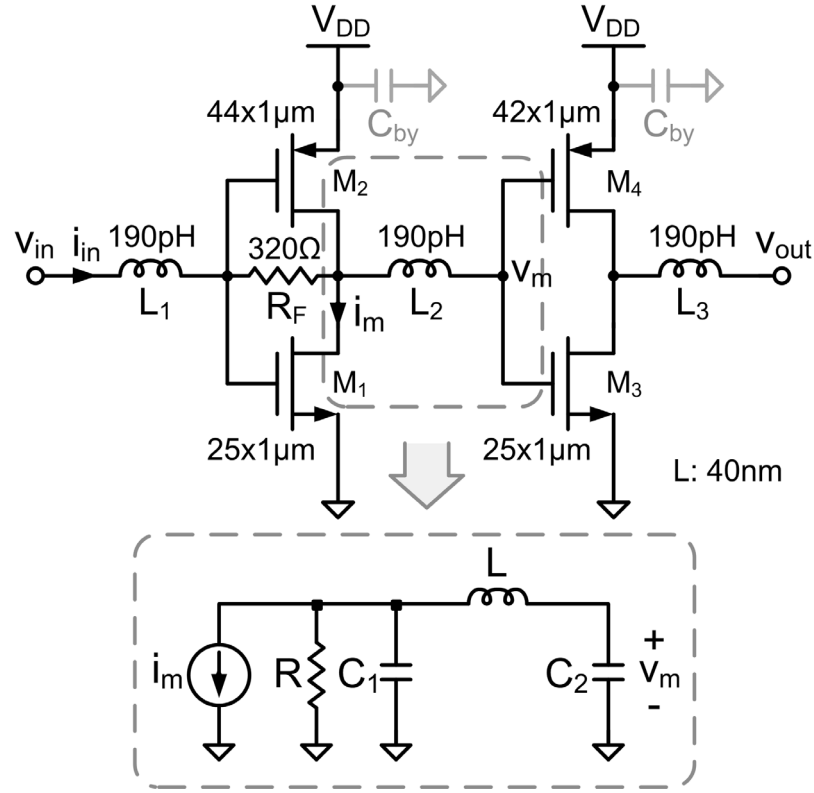


Figure 3.7: Schematic of the proposed TIA with post amplifier and series inter-stage inductance with the equivalent small-signal model.

ISI distortion [6]. A broadband matching network for the amplifier uses a parallel combination of resistors R_1 and the sum of $R_2 \sim R_4$. The output matching network is formed with the combination of the load resistor R_L and the output resistance of the stacked-FET. The response of the matching network is limited by the input and output capacitances of the stacked-FET transistors. A small inductance is introduced with coplanar waveguide (CPW) lines, 100 μm length, at the input and output ports to isolate these parasitic capacitances from the bondpads.

Fig. 3.6 shows that simulated single-ended output eye diagram of a differential modulator driver with 700mV_{pp} input swing for 40-Gb/s.

3.1.2 Transimpedance Amplifier

There are several possible TIA topologies in CMOS processes. Shunt feedback is commonly employed for TIA circuits because it offers high transimpedance

and low input impedance. Typically, a resistive load (R_L) is used to provide wide-band response but a significant voltage drop is required for high gain; *i.e.* open loop gain = $g_m \times R_L \parallel R_F$ [58]. The resistive load can be replaced with a PFET active load (r_o) to increase the gain and relax the d.c. voltage headroom problem; *i.e.* open loop gain $\approx g_m \times r_o \parallel R_F$. However, for processes with low voltage supplies, active loads reduce the achievable gain for each stage and the maximum transimpedance is limited by the load impedance at the drain of the first amplifier stage.

In highly-scaled SOI CMOS technology where the PFET device has a sufficiently high f_T , both the NFET and PFET provide transconductance as a push-pull or “inverter” amplifier with shunt resistive feedback. This is illustrated in the first stage of Fig. 3.7 where R_F is connected between the gate and drain of the NFET and PFET. The post amplifier is also realized as a push-pull amplifier and increase the transimpedance of the TIA stage.

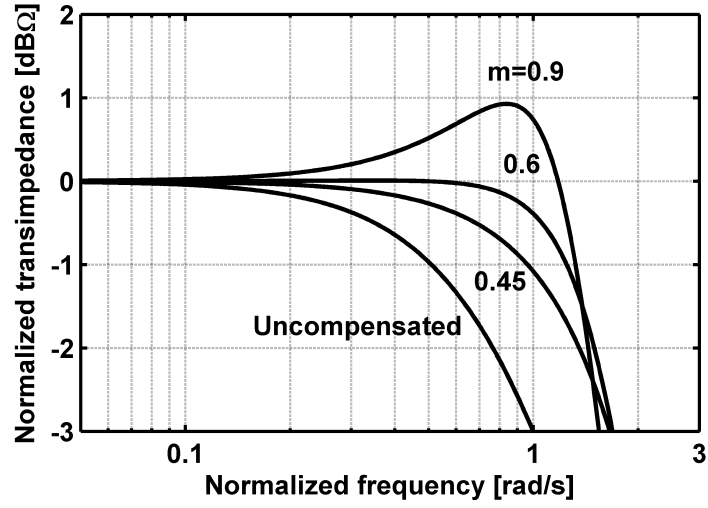
The advantage of this approach is to reuse the drain current and realize the intrinsic gain of both devices while reducing the power dissipation [59]. Since the NFET and PFET are in parallel, the PFET enhances the overall transconductance and the combination of the NFET and PFET transconductance is $g_{m,o} = g_{m,n} + g_{m,p}$. Similarly, the total channel conductance is $g_{ds,o} = g_{ds,n} + g_{ds,p}$, where $g_{ds,n}$ and $g_{ds,p}$ are respectively the NFET and PFET channel conductances and the small-signal gain of the inverter is $A = -g_{m,o}/g_{ds,o}$. Therefore, the d.c. transimpedance, R_T , and the input impedance, R_I , are

$$R_T = \frac{1 - g_{m,o}R_F}{g_{m,o} + g_{ds,o}} \approx -R_F, \quad (3.4)$$

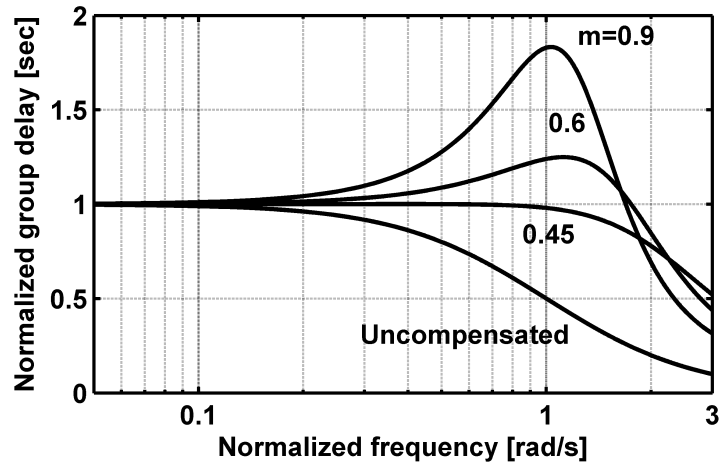
$$R_I = \frac{1 + g_{ds,o}R_F}{g_{m,o} + g_{ds,o}} \approx \frac{g_{ds,o}R_F}{g_{m,o}}, \quad (3.5)$$

where R_F is the feedback resistance. The approximations hold for large transconductances.

Fig. 3.7 shows the schematic of the proposed TIA with one post amplifier stage. The post-amplifier is also realized as a push-pull amplifier and increases the transimpedance of the TIA stage. The overall transimpedance is increased by



(a)



(b)

Figure 3.8: Normalized transimpedance response (a) and group-delay response (b) of inductive-series peaking π -network with different m values using (3.6) ($R = 1\Omega$ and $n = 7/8$).

the gain of the post-amplifier to $R_{T,o} = R_T \cdot \frac{g_{m,a}}{g_{ds,a}}$, where R_T is found from (3.19) and $g_{m,a}$ and $g_{ds,a}$ are the total transconductance and output conductance of the post-amplifier stage. All amplifier stages are self-biased using the shunt resistive feedback R_F since the transimpedance and post amplifier stages are d.c. coupled.

Each amplifier stage has additional capacitance associated with the contribution of the gate-source and drain-source capacitances of the PFET. A series inductance is inserted between the input and output nodes to form a π -network for wide bandwidth as well as low group-delay variation [8]. The transimpedance of the π -network between the drain of TIA stage and the gate voltage of the post amplifier stage with inductive series peaking behaves as a third order response,

$$\begin{aligned} Z_\pi(s) &= \frac{v_m(s)}{i_m(s)} = \frac{R}{s^3 RLC_1C_2 + s^2 LC_2 + sR(C_1+C_2) + 1} \\ &= \frac{R}{\left(\frac{s}{\omega_u}\right)^3 mn(1-n) + \left(\frac{s}{\omega_u}\right)^2 mn + \frac{s}{\omega_u} + 1}, \end{aligned} \quad (3.6)$$

where $m = L/R^2(C_1+C_2)$ and $n = C_2/(C_1+C_2)$ are dimensionless parameters and the frequency response is normalized to $\omega_u = \frac{1}{R(C_1+C_2)}$, the 3-dB bandwidth for the uncompensated transimpedance with $L = 0$. The m parameter is characterized by the product of the L/R and RC time constants while the n parameter characterizes the capacitance ratio of C_1 and C_2 and is primarily determined by the relative size of active devices and associated device parasitic capacitances. In this design, C_1 can be represented by the combination of drain-source capacitances of $C_{ds1} + C_{ds2}$ while C_2 is the combination of gate-source capacitances of $C_{gs3} + C_{gs4}$. In a SOI CMOS technology, careful parasitic extraction is required to determine parasitic capacitance accurately, because transistor intrinsic parasitic capacitance is lower due to isolation from the bulk silicon and interconnect parasitic capacitances can not be ignored.

In this design, the gate capacitances, C_1 , is four times larger than the drain capacitances, C_2 . However, since the effective capacitance at the TIA and post amplifier inputs is increased due to the Miller effect, the ratio of parasitic capacitances should be increased as well. Assuming the gate capacitances, C_1 , is seven times larger than the drain capacitances, C_2 , for devices of similar size, n is approximately 7/8. Normalizing C_1 and C_2 to 0.125 F and 0.875 F, respectively,

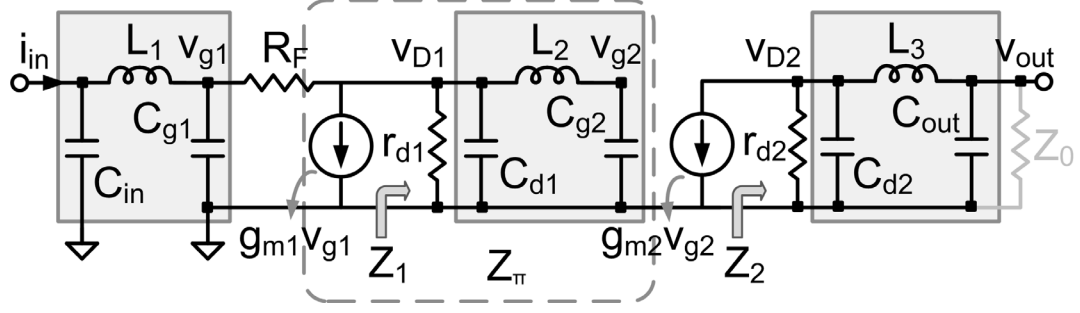
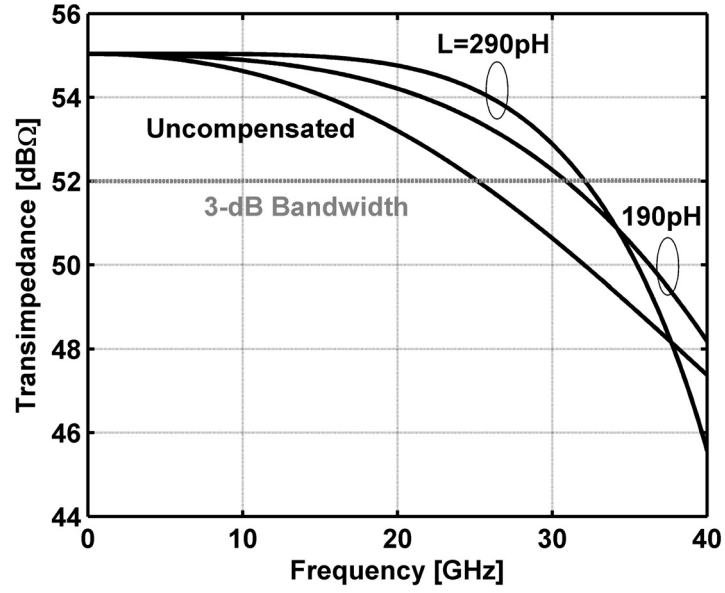


Figure 3.9: Simplified circuit schematics of each stage, including the photodetector and bondpad capacitances with equivalent small-signal model.

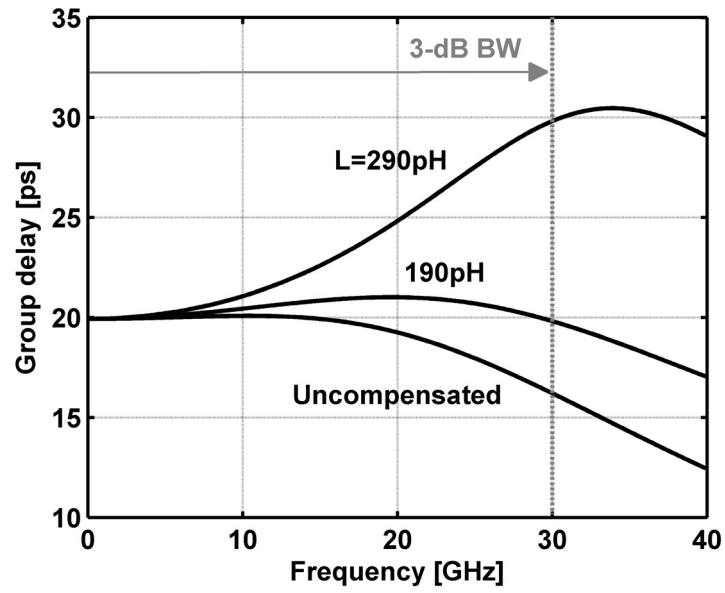
the 3-dB bandwidth of uncompensated case is unity and $R = 1\Omega$.

Fig. 3.8(a) shows the magnitude of the normalized transimpedance response and can be compared to normalized group delay response shown in (b) of the inductive-series peaking π -network for values of m . The uncompensated case, $m = 0$, provides a reference with unity 3-dB bandwidth. The 3-dB bandwidth varies as m increases and a maximum bandwidth-enhancement ratio (BWER) of 1.68 is achieved when $m = 0.6$ and in this case maximally flat magnitude is also obtained. However, the group delay variation is minimized when $m = 0.45$ and it provides BWER of 1.65. Linear phase delay is represented by a flat group delay response and large group delay variation results in DDJ which degrades the signal integrity of the data eye [8]. In this case, both the maximum transimpedance and minimum group delay variation can be achieved between $m = 0.45$ and 0.6. The response of both transimpedance and group delay variation are varies as the ratio of capacitance, n , changes. Typically, in common intermediate stage designs, the value of n is limited by the transistor size and process unless external capacitance is added. However, at the input of TIA, C_1 is represented by the combination of photodetector and/or bondpad parasitic capacitances. In this case, since the π -network is reciprocal, (3.6) is still valied except that the capacitance ratio becomes $n = C_{in}/(C_{in} + C_{g1})$, where C_{in} is the parasitic capacitance of photodetector (or combination with bondpad capacitance) and C_{g1} is the input capacitance of TIA (in this design, the combination of gate-source capacitances of $C_{gs1} + C_{gs2}$).

The finite gain of the TIA amplifier, M_1 and M_2 , creates a finite input



(a)



(b)

Figure 3.10: Analytical results of transimpedance (a) and phase response (b) using (3.11) of TIA.

impedance of the transimpedance stage, *i.e.* $R_{in} = R_F / (A + 1)$. In this design, the input impedance is matched to 50Ω for electrical measurement. The total receiver input capacitance plays an important role in determining the maximum bandwidth of the transimpedance receiver. It consist of the photodiode capacitance, the gate capacitance of the nMOS and pMOS, and the the capacitance of the bondpad. The photodiode capacitance is bounded between 50 fF and 80 fF based on commercially available 30-GHz photodiodes and the bondpad capacitance contributes around 40 fF [52]. The input pole for the TIA is

$$\omega_p = \frac{A + 1}{R_F C_T} = \frac{1}{R_{in} C_T} \quad (3.7)$$

where C_T is the total input capacitance at the input of TIA, *i.e.* $C_T = C_{in} + C_{g1}$. For 50Ω input impedance, the 3-dB cutoff is under 28-GHz if $C_T \geq 113fF$. To relax this bandwidth constraint, inductor $L_1 = 190pH$ is inserted in series between the bondpad and the transimpedance stage. Isolating the photodiode capacitance, the pole is increased to approximately $(A + 1) / (R_F C_T)$. In this case, $n = 7/8$ and $m = 0.45$ therefore the bandwidth-enhancement ratio (BWER) = 1.65 and normalized group delay variation = 0.125.

Fig. 3.9 shows the small-signal model of the proposed TIA with interstage inductive series π -networks. The transimpedance transfer function from (3.6) is expressed in terms of the circuit parameters in Fig. 3.9 as

$$\begin{aligned} Z_T(s) &= \frac{v_{D1}(s)}{i_{in}(s)} \\ &= \frac{Z_1(g_{m1}R_F - 1)}{g_{m1}Z_1 + 1} \frac{1}{s^3\tau_{t3} + s^2\tau_{t2} + s\tau_{t1} + 1} \end{aligned} \quad (3.8)$$

where $\tau_{t1} = \frac{R_F + Z_1}{g_{m1}Z_1 + 1} C_T$, $\tau_{t2} = L_1 C_{in}$, $\tau_{t3} = \frac{R_F + Z_1}{g_{m1}Z_1 + 1} L_1 C_{in} C_{g1}$, and g_{m1} is the total nMOS, M_1 , and pMOS, M_2 , small-signal transconductance. The transimpedance depends on the output impedance of the first stage, Z_1 , as well as R_F . The output impedance of each stage is

$$Z_x = \frac{s^2 C_{gx+1} L_{x+1} r_{dx} + r_{dx}}{s^3 \tau_{i3} + s^2 \tau_{i2} + s \tau_{i1} + 1} \text{ for } x = 1 \text{ and } 2, \quad (3.9)$$

where $\tau_{i1} = r_{dx} (C_{gx+1} + C_{dx})$, $\tau_{i2} = L_{x+1} C_{gx+1}$, $\tau_{i3} = r_{dx} L_{x+1} C_{gx+1} C_{dx}$, and r_{dx} is the total transistor output conductance, r_{ds} , of NFET and PFET at the bias point, *i.e.* $r_{d1} = r_{ds1} \parallel r_{ds2}$.

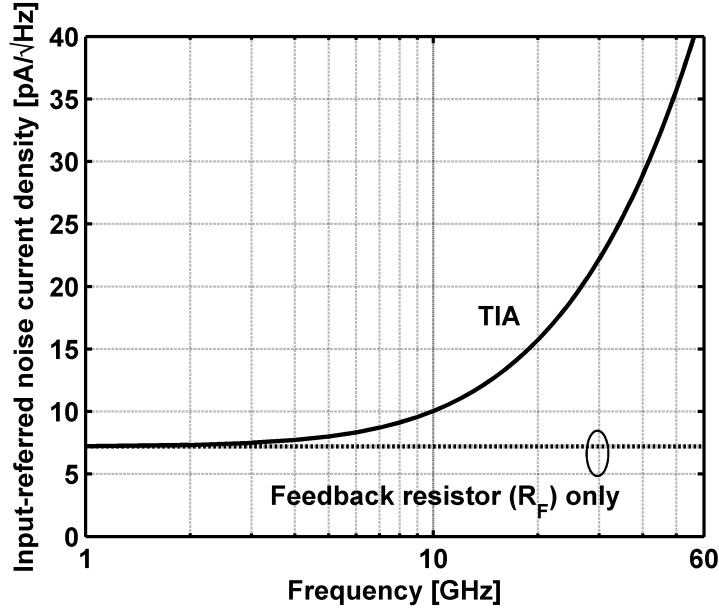


Figure 3.11: Simulated input-referred noise current density using (3.12).

The post amplifier with interstage inductive-series peaking provides voltage gain while mitigating group delay variation. The interstage voltage gain from output of TIA to the input of post amplifier is expressed as

$$\frac{v_{D2}}{v_{D1}} = g_{m2} Z_{\pi 2} \frac{Z_2}{Z_1} \approx g_{m2} Z_{\pi 2}, \quad (3.10)$$

where the output impedances for consecutive stages cancel to the extent that their impedances over the frequency response are identical. Consequently, the π -network transfer function described in (3.6) gives the frequency response and the overall transimpedance is derived as

$$Z_{T,total} = Z_T(s) \cdot g_{m2} Z_{\pi 2}(s). \quad (3.11)$$

The photodiode and bondpad capacitances are isolated from the input of the transimpedance stage with L_1 . Additionally, L_2 isolates the TIA output and post-amplifier input capacitance. Finally, L_3 isolates the output capacitance of post amplifier stage and output bondpad. In this design, L_1 , L_2 , and L_3 are 190 pH . Fig. 3.10(a) and (b) show that the analytical results of transimpedance

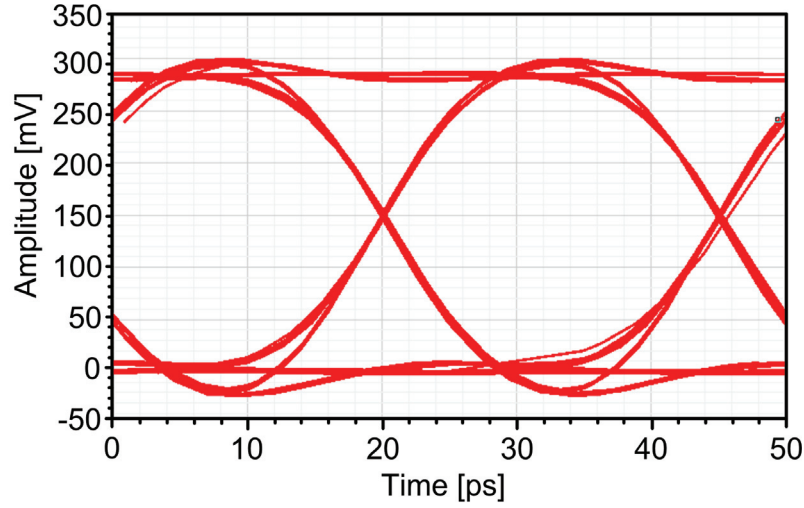


Figure 3.12: Simulated output eye diagram of TIA with $500\mu\text{App}$ input swing for 40-Gb/s.

and phase response using (3.11), respectively. The predicted 3-dB bandwidth of transimpedance is 31 GHz with $L = 190\text{ pH}$, which is 1.24 times larger than uncompensated case. The 3-dB bandwidth can be increased with higher value of series inductance, *i.e.* $BW = 32\text{ GHz}$ with $L = 290\text{ pH}$, at the price of increasing phase distortion as shown in Fig. 3.10(b).

The total input-referred noise current spectrum of a shunt feedback TIA is expressed as

$$I_{n,TIA}^2(f) = I_{n,RF}^2(f) + I_{n,Amp}^2(f) \quad (3.12)$$

where $I_{n,RF}^2(f)$ is the thermal noise of the feedback resistor and $I_{n,Amp}^2(f)$ is the input-referred amplifier noise. The first term of (3.12) is given by the well-known thermal-noise equation,

$$I_{n,RF}^2(f) = \frac{4kT}{R_F}. \quad (3.13)$$

The input-referred noise current spectrum of an amplifier is

$$I_{n,Amp}^2(f) = 2qI_l + 4kT\Gamma \cdot \frac{1}{g_{m1}R_F^2} + 4kT\Gamma \cdot \frac{(2\pi C_T)^2}{g_{m1}} \cdot f^2 \quad (3.14)$$

where I_l is the sum of the photodiode (dark current) and FET gate leakage currents and Γ is the excess channel noise factor term associated with short-channel transistors. In this noise analysis, the first and second term of (3.14) are neglected because they are small compared with the feedback-resistor noise if $g_m R_F \gg \Gamma$ [6]. Additionally, assuming the $1/f$ or flicker noise of FET is neglected. The noise sources due to the post amplifier also contribute to the input-referred TIA noise, *i.e.* $I_{n,PostAmp}^2(f) = (4kT\Gamma) / (g_{m2}R_F^2)$. However, if the gain of the TIA stage is sufficiently large, these sources can be neglected and the total input-referred rms noise current of the TIA is derived as

$$\overline{I_{n,TIA}^2(f)} = \frac{4kT}{R_F} I_2 B_0 + 4kT\Gamma \frac{(2\pi C_T)^2}{g_m} I_3 B_0^3 \quad (3.15)$$

where B_0 is the 3-dB bandwidth of the receiver, $g_m = g_{mn} + g_{mp}$, and I_2 and I_3 are the normalized Personick noise bandwidth integrals, respectively. Consequently, in (3.15) the first term can be minimized by choosing R_F as large as possible given integral values for Butterworth. However, large R_F decrease the pole frequency in (3.7) and limits the 3-dB bandwidth of the TIA.

Fig. (3.20) shows that simulated results of an input-referred noise current density of TIA. The input-referred noise current spectrum of the TIA is shown in a solid line and the contribution from the feedback resistor, R_F , is plotted with a dashed line. At low frequencies, the noise from the feedback resistor dominates and the total spectral density is about $7.2 \text{ pA}/\sqrt{\text{Hz}}$. However, at high frequencies, f^2 -noise due to the channel noise of FET's dominates and the total spectral density increases as frequency increases. Assuming that the TIA has a second-order Butterworth response, the input-referred rms noise current can be determined using (3.15) and is about $3.67 \mu\text{A}_{rms}$ with C_T of 100 fF. The optical sensitivity can be found from

$$\overline{P_{sens}} = \frac{Q \cdot i_n^{rms}}{R}, \quad (3.16)$$

where R is the responsivity of the photodetector. $Q = v_s^{pp} / (2 \cdot v_n^{rms})$ where v_s^{pp} is a peak-to-peak value of the non-return-to-zero (NRZ) signal, and v_n^{rms} is an rms value of the noise. *i.e.*, $Q = 7.035$ for bit-error rate (BER) of 10^{-12} [6].

Consequently, by assuming that the photodetector has the responsivity of 1 A/W, the receiver sensitivity is predicted using (3.16) and is about -15.88 dBm for BER of 10^{-12} at 40-Gb/s.

Fig. 3.12 illustrates the simulated output eye diagram with a peak-to-peak current of $500 \mu\text{A}$ at 40-Gb/s. The output swing is $300 mV_{pp}$ indicating a total transimpedance of $55 \text{ dB}\Omega$. The eye does not suffer from significant deterministic jitter.

3.2 Measurements

The circuits are implemented in a 45 nm SOI CMOS technology with 8 metal layers. The chip microphotographs are shown in Fig. 3.13. The single-ended modulator driver occupies $0.42 \text{ mm} \times 0.49 \text{ mm}$ (0.21 mm^2) while the differential version occupies $0.47 \text{ mm} \times 0.81 \text{ mm}$ (0.38 mm^2). However, the active area of both drivers are only less than 0.004 mm^2 . The TIA occupies $0.54 \text{ mm} \times 0.54 \text{ mm}$ (0.29 mm^2). The single-ended modulator driver chip consumes 11 mA and 30 mA from a 2.5 V and 5 V supplies, respectively, while the differential driver chip consumes 21.5 mA and 37 mA from a 3 V and 5 V supplies, respectively. The TIA chip consumes 9 mA from a 1 V supply.

3.2.1 Modulator Drivers

With a single-ended modulator driver, S -parameters are measured using the Agilent E8361A two-port network analyzer using on-chip probing with Picoprobe coplanar 67A ground-signal-ground (GSG) probes. The measured S -parameters are shown in Fig. 3.14 and can be compared to the simulated results (dotted lines). The single-ended modulator driver has a d.c. gain of 7.6 dB and a 3-dB bandwidth of 33 GHz. The measured input return loss is better than 7.6 dB across the entire 3-dB bandwidth, but remains below 10 dB below 23 GHz. The output return loss is better than 11.4 dB across the entire 3-dB bandwidth and the reverse isolation is better than 30.5 dB. Fig. 3.14 shows an excellent agreement between measured and simulated results.

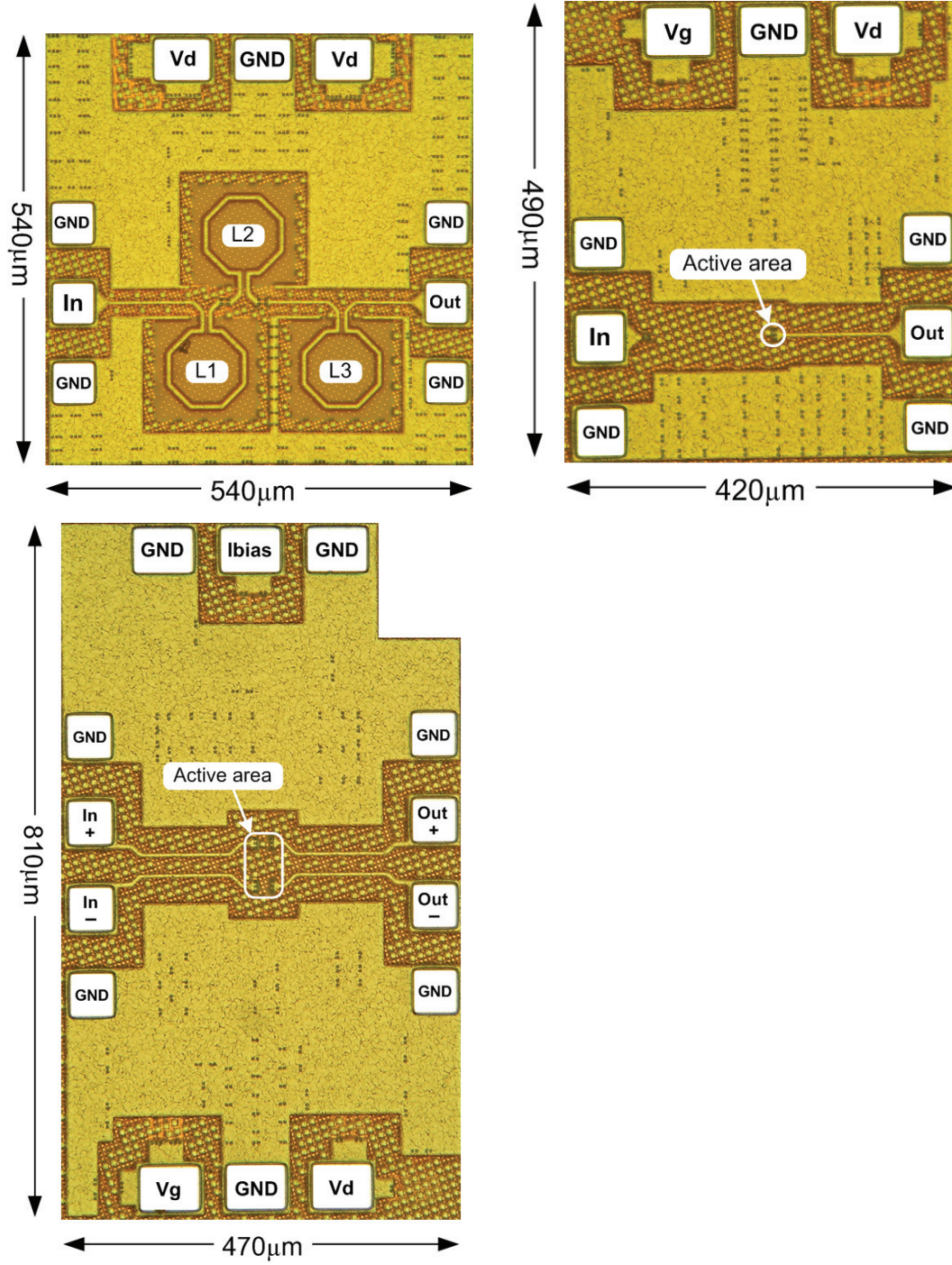


Figure 3.13: Chip microphotographs of TIA with post amplifier (left), single-ended modulator driver (right) and differential modulator driver (bottom) in 45nm SOI CMOS.

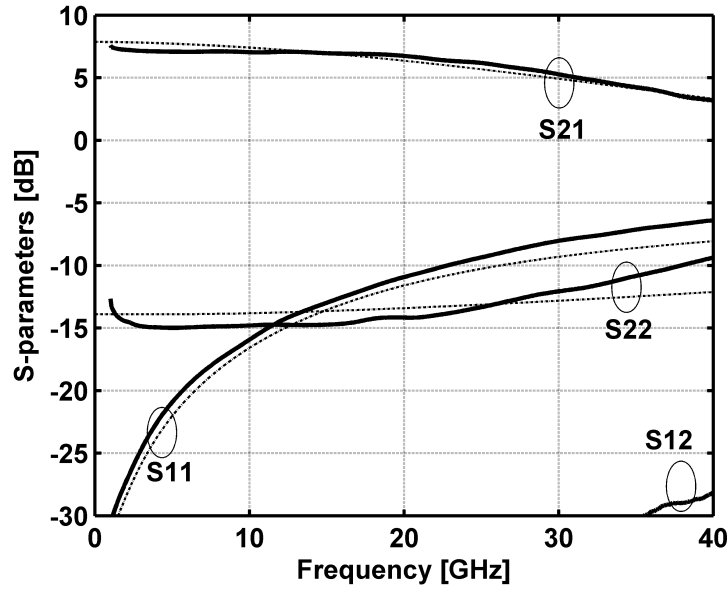


Figure 3.14: Measured (solid lines) and simulated (dotted lines) S -parameters of single-ended modulator driver.

The group-delay variation of a single-ended modulator driver is shown in Fig. 3.15. The group delay is measured from the S -parameters and the modulator driver has a nominal group delay of 2.4 ps, increases to 8.6 ps, giving an overall measured group-delay variation of ± 3.1 ps over the 3-dB bandwidth.

Fig. 3.16(a) and (b) shows the measured electrical output eye diagram of a single-ended modulator driver and one of outputs of a differential modulator driver at 40-Gb/s. The eye diagram is measured using an Agilent 86100A DCA wide-bandwidth oscilloscope. A $2^{31}-1$ non-return-to-zero (NRZ) pseudorandom bit sequence (PRBS) is generated from a Centellax TG1P4A pulse pattern generator with a Centellax OA4MVM broadband amplifier to amplify input voltage swing from the 40-Gb/s PRBS generator (nominal 5~600 mV_{PP} swing depending on cable losses). The output load for the driver is 50 Ω , and 3, 10 and 20-dB microwave attenuators are used to avoid overloading the wide-band oscilloscope and to reduce the output voltage swing from Centellax broadband amplifier (7 V_{PP} swing). With an input voltage swing of 890 mV_{PP} , the output voltage swing of a single-ended driver is about 2 V_{PP} while the single-ended output swing of a differential driver

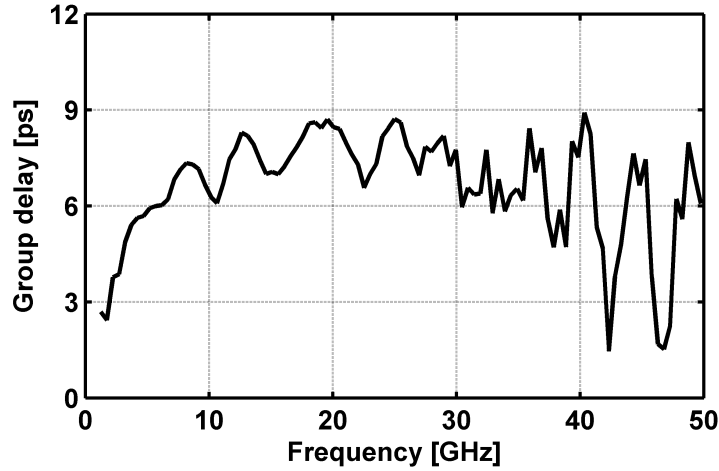


Figure 3.15: Measured group delay variation of modulator driver.

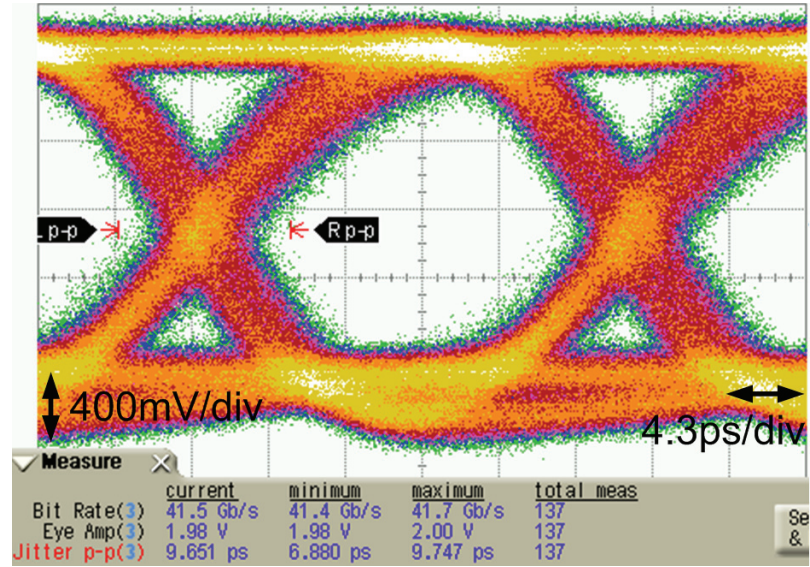
is about $2.25 V_{PP}$. The jitter of the modulated eye is less than 10 ps peak-to-peak for a single-ended driver while the input signal has 7.8 ps of peak-to-peak jitter. The differential driver has the jitter of the modulated eye of less than 10.7 ps peak-to-peak. The both eye diagrams showed good characteristics at 40-Gb/s.

3.2.2 Transimpedance Amplifier

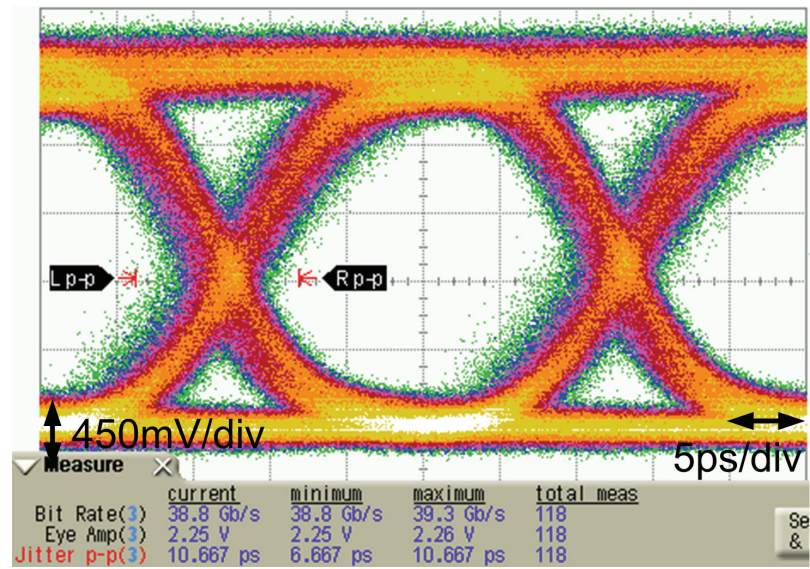
The transimpedance is derived from the S -parameters,

$$Z_T = \frac{Z_o S_{21}}{1 - S_{11}} \quad (3.17)$$

where Z_o is the load impedance of 50Ω . The measured S -parameters and transimpedance are shown in Fig. 3.17 and can be compared to the simulated results (dotted lines). The measured small-signal gain is 20 dB with a 3-dB bandwidth of 30 GHz and reverse isolation is better than 28.4 dB across the entire 3-dB bandwidth. This translates to a transimpedance of $54.7 \text{ dB} \cdot \Omega$ with a 3-dB bandwidth of 30 GHz. The measured input return loss is better than 9.5 dB across the entire 3-dB bandwidth, but remains below 14 dB below 25 GHz. The output return loss is better than 10 dB below 25 GHz. Fig. 3.17 shows an excellent agreement between measured and simulated results. The transimpedance-bandwidth figure



(a)



(b)

Figure 3.16: Measured (a)output eye diagram of single-ended driver and (b)single-ended output eye diagram of differential modulator driver with a 40-Gb/s $2^{31}-1$ PRBS.

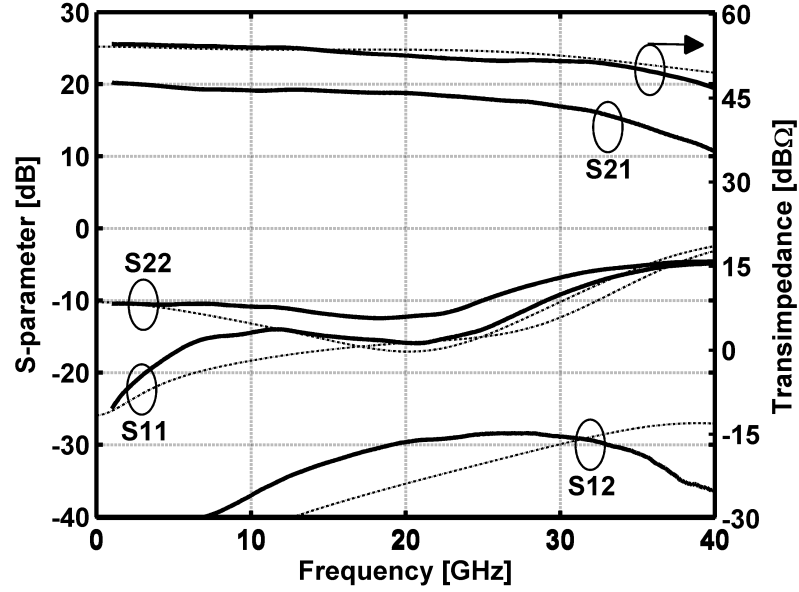


Figure 3.17: Measured (solid lines) and Simulated (dotted lines) S -parameters and transimpedance of TIA.

of merit $FOM = R_T BW / P_{DC}$ is $1874.5 \Omega/pJ$.

The group-delay variation is shown in Fig. 3.18. The group delay is measured from the S -parameters and translated to Z parameters to find the transimpedance group delay. The TIA has a nominal group delay of 17.1 ps, increases to 24.9 ps, giving an overall measured group-delay variation of ± 3.9 ps over the 3-dB bandwidth.

Fig. 3.19(a) and (b) show the measured electrical output eye diagrams of the TIA and MA at 22-Gb/s and 40-Gb/s. The eye diagrams are measured with the same setup described in Section 4.2.1. With an input current swing of $1.4mA_{PP}$, the output voltage swing is $750mV_{PP}$ at 22-Gb/s as shown in Fig. 3.19(a). Fig. 3.19(b) shows that with an input current swing of $1mA_{PP}$, the output voltage swing is $521mV_{PP}$ at 40-Gb/s. They both showed good characteristics at 22-Gb/s and 40-Gb/s, respectively. At 40-Gb/s, the output eye diagram records 6.4 ps of peak-to-peak jitter while the input signal has 5.8 ps of peak-to-peak jitter. Consequently, the low group delay variation of the TIA reflects a low deterministic jitter in the signal.

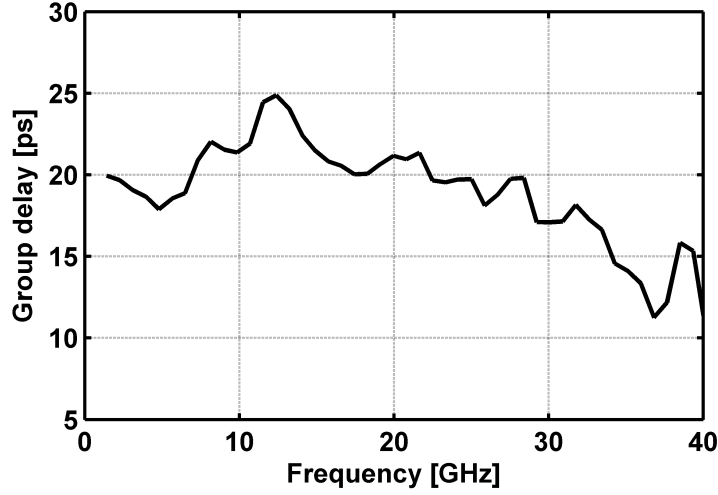


Figure 3.18: Measured group delay variation of TIA.

The integrated output noise of TIA is determined on the oscilloscope by observing the output of the TIA with no input signal source [48]. Fig. 3.20 shows the amplitude distribution obtained by the oscilloscope histogram function. The measured integrated output noise is $1.5mA_{rms}$ and the integrated input-referred noise can be calculated as

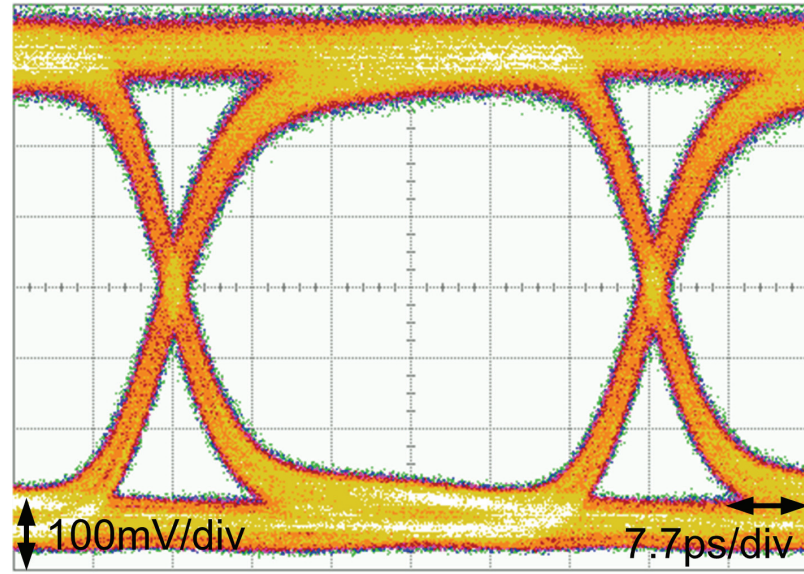
$$\begin{aligned}
 I_{n,in,tot} &= \frac{2\sqrt{(1.5m)^2 + (1.19m)^2}}{Z_T} \\
 &= 3.54\mu A_{rms}
 \end{aligned} \tag{3.18}$$

where the $1.19mA_{rms}$ noise contributed by the oscilloscope itself has been subtracted and Z_T is found from (3.19) [14]. The average input-referred noise density is

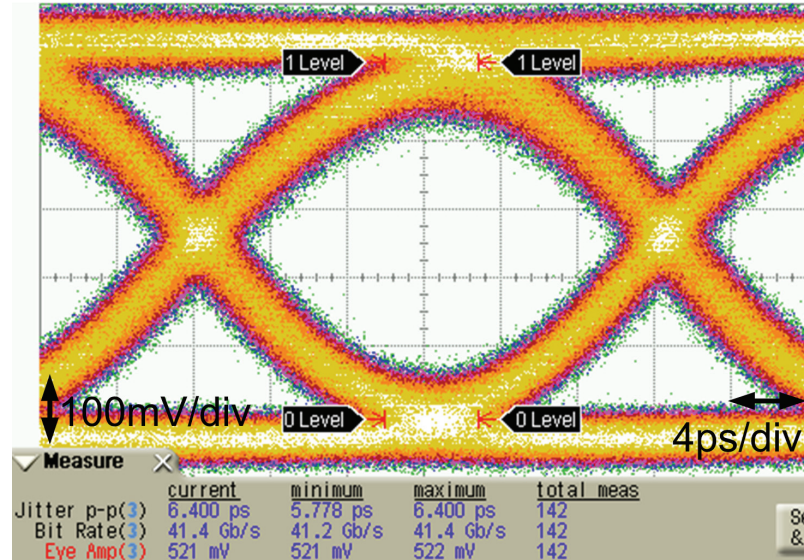
$$\begin{aligned}
 I_{n,in,avg} &= \frac{I_{n,in,tot}}{\sqrt{BW}} \\
 &= 20.47pA/\sqrt{HZ}
 \end{aligned} \tag{3.19}$$

where the BW is a 3-dB bandwidth of the TIA. Consequently, by assuming that the photodetector has the responsivity of 1 A/W and 0.8 A/W, the receiver sensitivity is predicted using (3.16) and is about -16 dBm and -15 dBm, respectively, for BER of 10^{-12} at 40-Gb/s.

The TIA is demonstrated in a 40-Gb/s optical testbed to illustrate the eye



(a)



(b)

Figure 3.19: Measured electrical output eye diagrams of TIA with (a) 22-Gb/s $2^{31}-1$ PRBS for 1.4 mA_{PP} input swing and (b) 40-Gb/s $2^{31}-1$ PRBS for 1 mA_{PP} input swing.

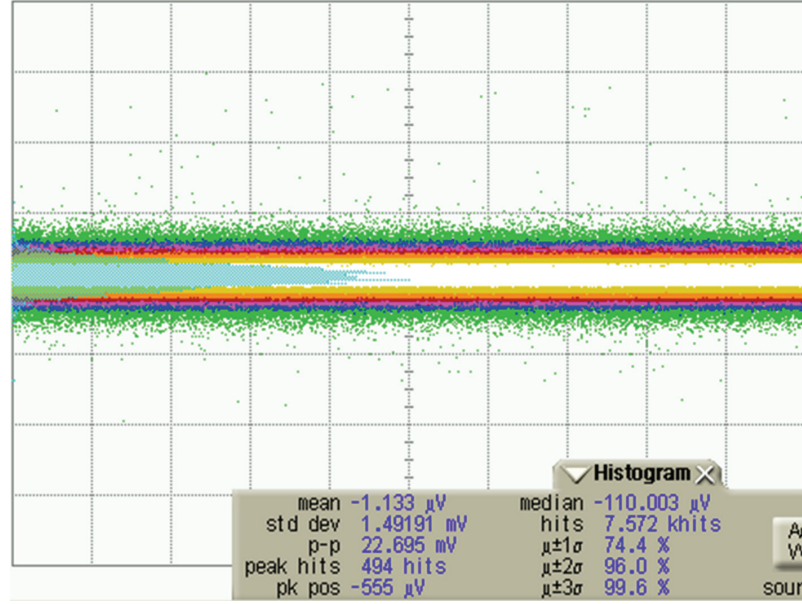


Figure 3.20: Measured integrated output noise.

diagram quality in Fig. 3.21. A 40-Gb/s, A $2^{31}-1$ PRBS is generated from a Centellax TG1P4A pulse pattern generator and amplified with a Centellax OA3MVM modulator driver. The electrical signal modulates a Mach-Zehnder modulator (JDS Uniphase, modal no. 21014025). The Santec ECL-200 tunable laser source is set to a wavelength 1555.28 nm and output power of 6 dBm. A fiber polarization controller polarizer adjusts the polarization state of the launched optical signal and E-tek MLDC-1032 multi-channel laser diode controller is connected to C-band fiber amplifier. A power monitor observes the output optical power and controls the optical power. The receiver is a Discovery Semiconductors DSC10H photodetector with a 3-dB bandwidth of 42 GHz and is connected to the 40-Gb/s device under test (DUT). The amplifier output is sampled with an Agilent DCA-J 86100C wide-bandwidth oscilloscope using a precision 20 GHz trigger generated by the TG1P4A.

The measured 40-Gb/s optical eye diagrams are shown in Fig. 3.22(a) and (b). With an input optical power of -8 dBm and -1 dBm, the output voltage swing is 91 mV_{PP} and 439 mV_{PP}, respectively. The rms jitter is 1.49 ps and 1.33 ps respectively and shows low jitter at high optical power. Note that the cable

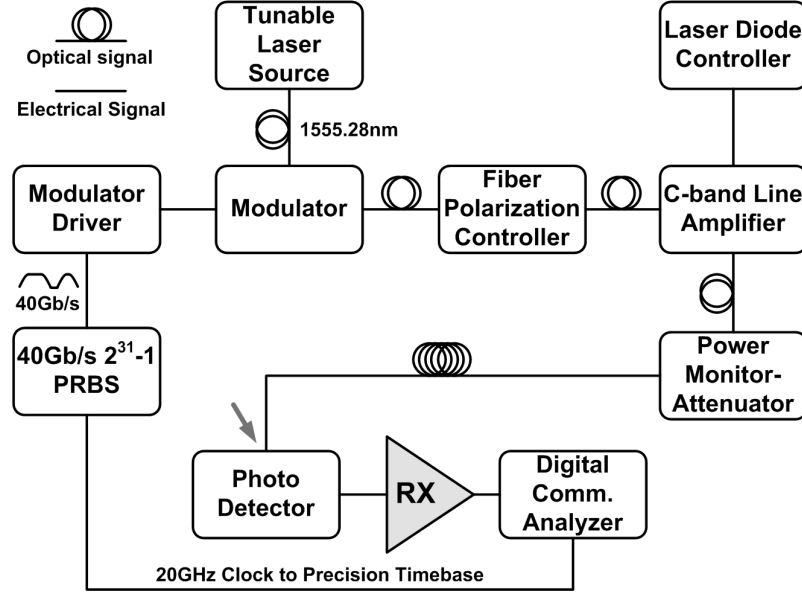


Figure 3.21: Block diagram for the optical measurement test setup.

and connector losses (~ 2.5 dB at 20 GHz) between the off-chip photodetector and DUT exist and reduce the sensitivity of the receiver.

The performance of 40-Gb/s optical transceiver front-end circuits are summarized in Table 3.1. The modulator driver represents the first effort to integrate a broadband, high voltage driver for 40-Gb/s into an SOI process.

A comparison with the recent publications on 40-Gb/s TIAs is provided in Table 3.2. The presented implementation is notable in the extremely low power consumption, group delay variation, and input-referred current noise density as well as the smallest area. The transimpedance-bandwidth FOM is $1874.5 \Omega/pJ$ and demonstrates remarkable improvement over previously published 40-Gb/s TIAs.

3.3 Conclusions

A 40-Gb/s optical transceiver front-end is implemented in a 45 nm SOI CMOS process. The TIA has a transimpedance of 55 dB $\cdot\Omega$ and group-delay variation of ± 3.9 ps over a 30 GHz bandwidth. The single-ended modulator driver has a small-signal gain of 7.6 dB over 33 GHz bandwidth and provides 2 V_{PP} voltage swing at 40-Gb/s. Finally, the differential modulator driver has an output voltage

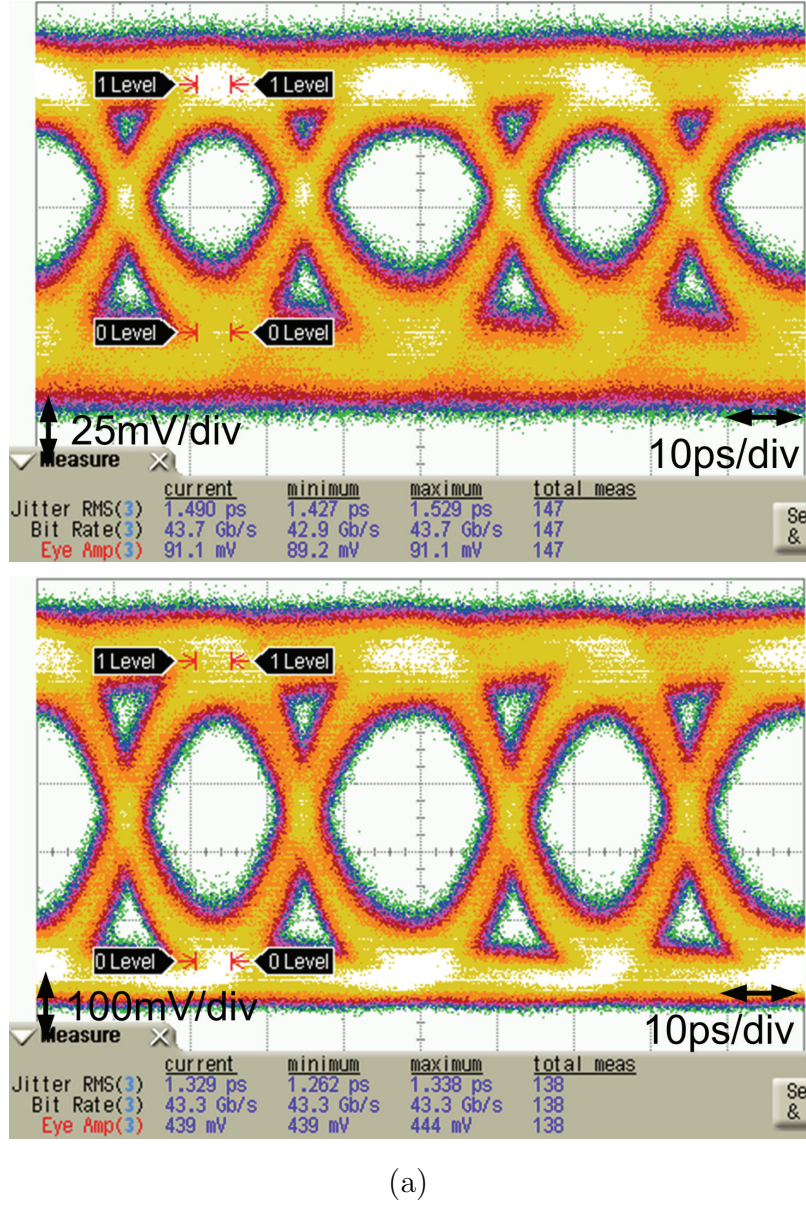


Figure 3.22: Measured optical output eye diagrams of TIA with a 40-Gb/s $2^{31}-1$ PRBS for (a) -8 dBm optical power and (b) -1 dBm optical power.

Table 3.1: Performance Summary of 40-Gb/s Transceiver

Technology	45nm SOI-CMOS (40nm L_{gate})
TX (50 Ω modulator driver)	
Die Area	0.21 mm ² (single-ended) 0.38 mm ² (differential)
Power Consumption	177.5 mW (single-ended) 437 mW (differential)
Gain	7.6 dB (single-ended)
3-dB Bandwidth	33 GHz
Group-Delay Variation	± 3.1 ps
Output Voltage	2 V_{PP} (single-ended) > 4 V_{PP} (differential)
RX (TIA with post amplifier)	
Die Area	0.29 mm ²
Power Consumption	9 mW
Transimpedance	55 dB $\cdot\Omega$
3-dB Bandwidth	30 GHz
Input-Referred Noise	20.47 pA/ $\sqrt{Hz}$
Group-Delay Variation	± 3.9 ps

swing of 4.5 V_{PP} at 40-Gb/s.

Acknowledgments

Chapter 3 is in-part mostly a reprint of the material as it appears in IEEE Custom Integrated Circuits Conference, 2010, J. Kim; J. F. Buckwalter, and in part, has been submitted for publication to IEEE Journal of Solid-State Circuits. J. Kim; J. F. Buckwalter. This dissertation author was the primary author of this material.

Table 3.2: Comparison of reported 40-Gb/s transimpedance amplifiers

Ref.	Process	Bit Rate (Gb/s)	BW (GHz)	Z_T (dB Ω)	GD (ps)	Noise (pA/ $\sqrt{Hz}$)	Supply (V)	Power (mW)	Area (mm ²)	$BW\Omega/P_{DC}$ (Ω /pJ)
[48]	DHBT $f_T=160\text{GHz}$	40	47	50*	–	35	5.2	458	0.66	64.7**
[53]	SiGe $f_T=200\text{GHz}$	40	50	43*	–	30	5.2	182	0.92	77.4**
[13]	0.18 μm CMOS	40	30.5	51	± 62.5	55.7 (sim.)	1.8	60.1	0.54	180.1
[8]	0.13 μm CMOS	40	29	50	± 8	51.8 (sim.)	1.5	45.7	0.4	200.7
[14]	90nm CMOS	40	22	60*	–	22	1.2	75	0.56	585.3**
This work	45nm SOI CMOS	40	30	55	± 3.9	20.47	1	9	0.29	1874.5

*: single-ended gain, **: calculated with differential gain

Table 3.3: Comparison of reported modulator drivers

Ref.	Process	Bit Rate (Gb/s)	BW (GHz)	Gain * (dB)	GD (ps)	Output Swing**(V)	Power ** (mW)	Area (mm ²)
[60]	0.18 μ m CMOS	10	–	14	–	8	600	0.68
[60]	0.35 μ m BiCMOS	10	–	19	–	9	1000	0.56
[61]	80-GHz HBT	40	32.2	7.6	± 6	3	1125	1.19
[62]	0.18 μ m BiCMOS	40	22	36	–	7.2	3600	3
[63]	0.25 μ m BiCMOS	40	33.7	7	–	6	1350	0.72
This work	45 nm SOI CMOS	40	33	7.6	± 3.1	4.5	437	0.38

*: single-ended, **: differential

Chapter 4

100-160 Gb/s Optical Receiver Front-ends

4.1 Cascaded Transimpedance Enhancements

The ability of silicon integrated circuits to cross the bandwidth chasm from 40-Gb/s to 160-Gb/s requires broadband amplifier design techniques that extend into the millimeter-wave design regime. Shunt feedback is commonly used to achieve high transimpedance and low input impedance. Unfortunately, the transimpedance, R_T , of the shunt feedback amplifier is inversely proportional to the square of the required 3-dB bandwidth, BW . For instance, a technology with $f_T = 200$ GHz and photodiode capacitance of $C_T = 40$ fF limits the transimpedance to 80Ω ($38 \text{ dB}\cdot\Omega$) for a 3-dB bandwidth of 100 GHz. With such a low transimpedance, the amplifier is scarcely more effective than a 50Ω termination. For this reason, silicon electronics lag alternative III-V integrated circuit options where wide bandwidths are demanded.

4.1.1 Broadband Cascade

To increase the transimpedance limit at high speeds from (1.3), additional post amplifiers with a total gain A_1 can be introduced as shown in Fig. 4.1. With n identical post-amplifier stages each with a d.c. voltage gain A_s and a second-order

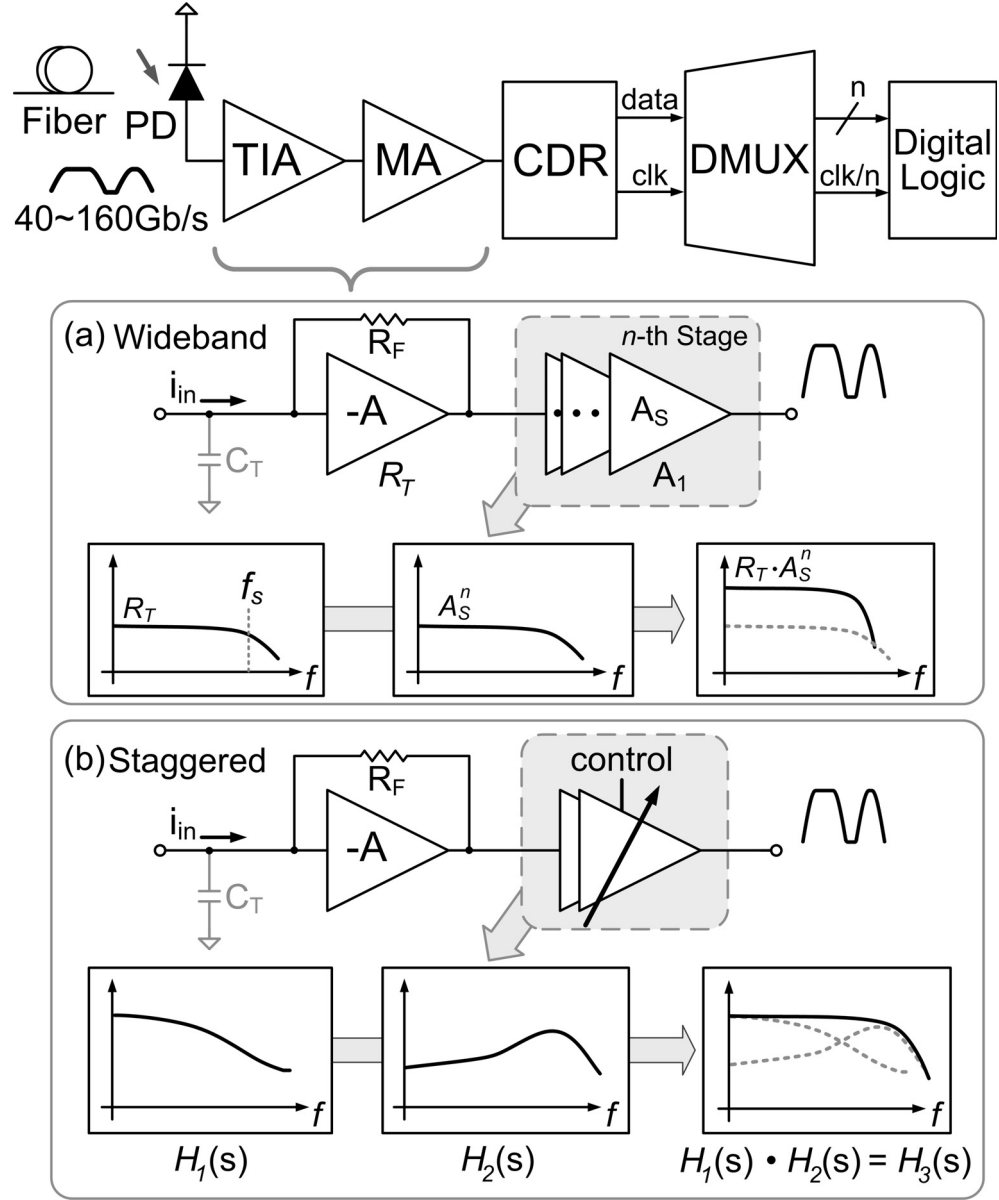


Figure 4.1: Block diagram of an optical receiver and a comparison of the wideband cascading versus staggered responses.

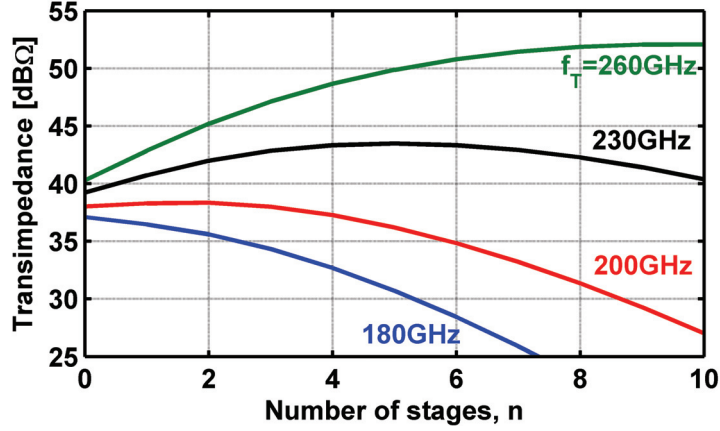


Figure 4.2: Maximum achievable transimpedance as a function of the cut-off frequency, f_T ($C_T = 40\text{ fF}$ and $\text{BW} = 100\text{GHz}$).

Butterworth response, the bandwidth of each post amplifier is f_s as determined by the maximum gain-bandwidth product (GBW), *i.e.* $\text{GBW} = A_s \cdot f_s \leq f_T$. With each additional post-amplifier more poles are added to the frequency response and the receiver bandwidth drops rapidly. If each post-amplifier has a bandwidth equal to the TIA bandwidth, f_s , then

$$\text{BW}_{total} = f_s \cdot (2^{1/(n+1)} - 1)^{1/4}. \quad (4.1)$$

Accordingly, the 3-dB bandwidth of the TIA and post-amplifiers must increase to compensate for the bandwidth lost by multistage post amplification. Consequently, the transimpedance limit with post amplifiers has been previously derived [8];

$$R_{T,total} \leq \frac{f_T^{n+1}}{2\pi C_T \text{BW}_{total}^{n+2}} (2^{1/(n+1)} - 1)^{(n+2)/4}. \quad (4.2)$$

Without post amplification ($n = 0$), the transimpedance limit in (4.2) reduces to (1.3). Fig. 4.2 shows the maximum achievable transimpedance over n stages as a function of f_T . For $f_T = 200\text{ GHz}$ and $C_T = 40\text{ fF}$, the maximum transimpedance is $38\text{ dB}\cdot\Omega$ for any number of stages greater than one. When the peak f_T is reduced by 10% to 180 GHz , the transimpedance is $36.5\text{ dB}\cdot\Omega$ - even lower than without post amplification ($n = 0$). Consequently, adding post-amplifier stages with f_T lower than 200 GHz does not improve the transimpedance.

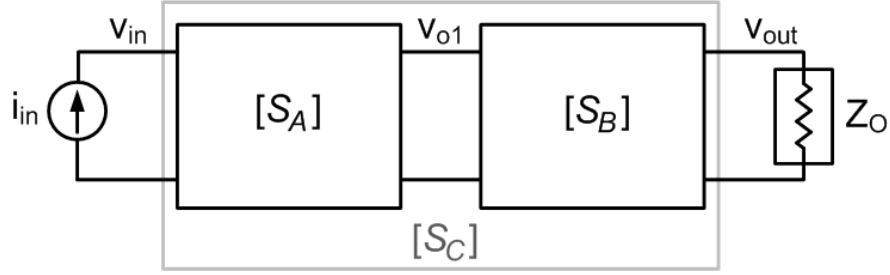


Figure 4.3: Block diagram of cascaded two-ports.

To overcome these bandwidth limitations, different design techniques have been reported. Traditional broadband SiGe HBT design is based on staggered impedance matching with cascaded emitter followers and consumes high power [64]. Distributed amplifiers achieve large bandwidth by absorbing transistor capacitances into artificial transmission lines or LC ladder filters [65–67]. However, the quality factor of on-chip passives in Silicon (Si) and Silicon-Germanium (SiGe) limit the achievable gain-bandwidth for distributed amplifier topologies [68,69]. Other bandwidth enhancement techniques are suggested based on optimal π -networks to isolate interstage capacitances with inductors [16].

4.1.2 Staggered Response

The preceding analysis assumes that each post-amplifier stage has the same bandwidth as the TIA. If staggered responses are used, the transimpedance limit in (4.3) may be relaxed. For instance, the bandwidth might be smaller at the transimpedance stage while subsequent stages provide gain at high frequency. At high-frequency, the broadband frequency response requires broadband matching between stages while compensating for the frequency response. The transimpedance, Z_T , is derived from the S -parameters;

$$Z_T = \frac{Z_o S_{21}}{1 - S_{11}}, \quad (4.3)$$

where Z_o is the load impedance [53] [14]. A broadband transimpedance response requires that both S_{21} and S_{11} satisfy low variation across the 3dB bandwidth.

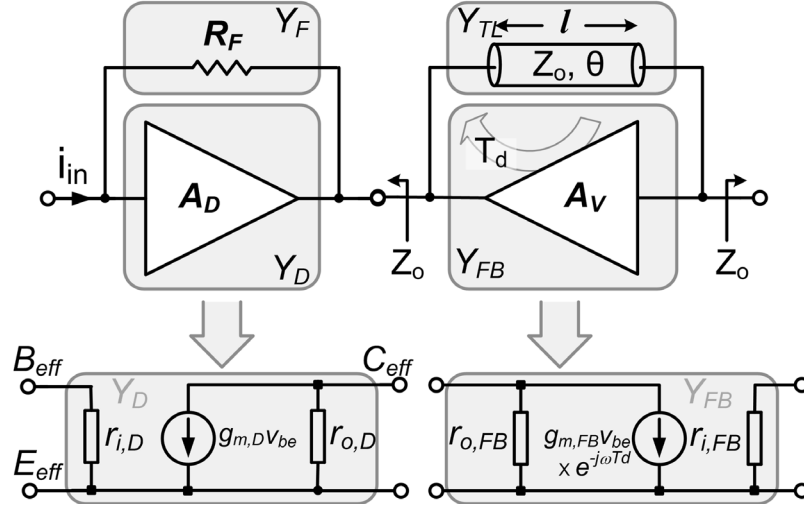


Figure 4.4: Shunt-shunt resistive feedback circuit cascaded with a constructive wave circuit. Equivalent circuits for the Darlington amplifier and feedback amplifier are shown respectively in the bottom left and right.

For a staggered response, the cascade of different frequency responses results in a broadband transimpedance response. The cascade of stages is described from the S -parameters of the individual two-port blocks shown in Fig. 4.3. If the first block is denoted S_A and the second block is denoted S_B , then

$$S_x = \begin{bmatrix} S_{x,11} & S_{x,12} \\ S_{x,21} & S_{x,22} \end{bmatrix}, \quad x = A \text{ or } B. \quad (4.4)$$

When S_A and S_B are cascaded to form a new block S_C , the forward transmission and input reflection are expressed as

$$S_{C,21} = \frac{S_{A,21}S_{B,21}}{1 - S_{A,22}S_{B,11}}, \quad (4.5)$$

and

$$S_{C,11} = S_{A,11} + \frac{S_{A,12}S_{A,21}S_{B,11}}{1 - S_{A,22}S_{B,11}}. \quad (4.6)$$

Substituting (4.5) and (4.6) into (4.3), the total transimpedance is

$$Z_{T,C} = \frac{Z_o S_{A,21} S_{B,21}}{1 - S_{A,11} - S_{B,11} (S_{A,22} - S_{A,11} S_{A,22} + S_{A,12} S_{A,21})}. \quad (4.7)$$

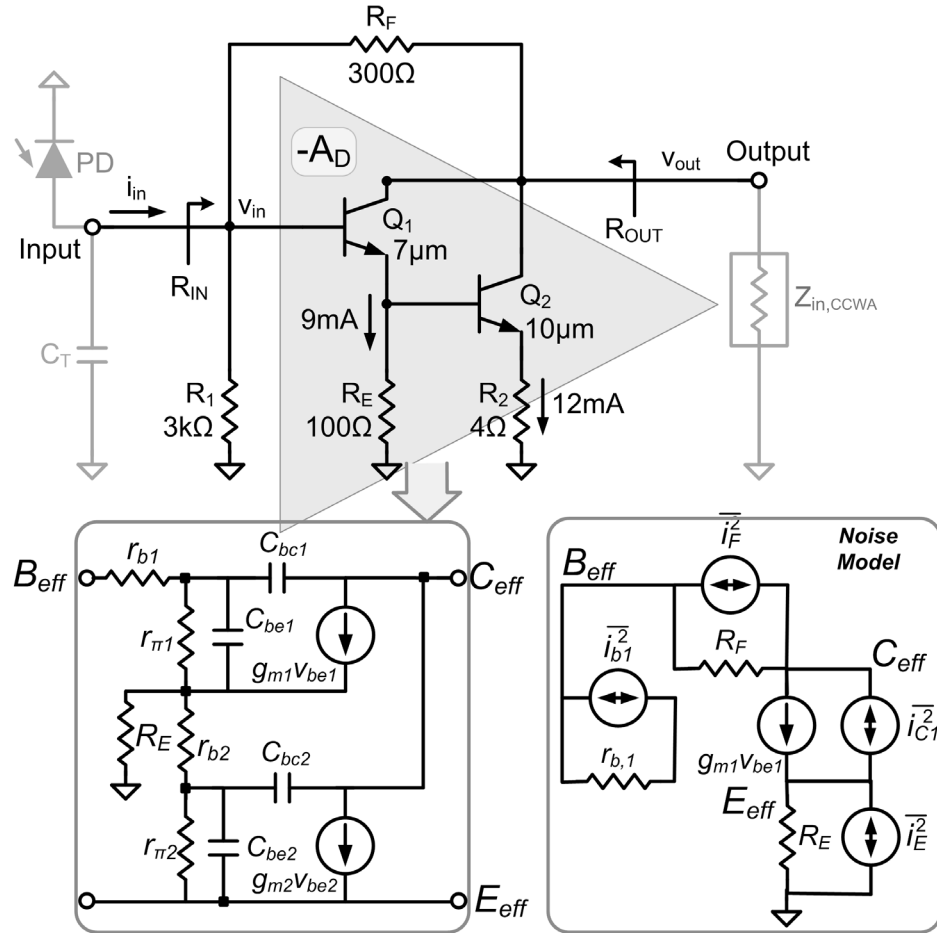


Figure 4.5: Circuit schematic of the Darlington feedback amplifier (top) and small signal model (bottom).

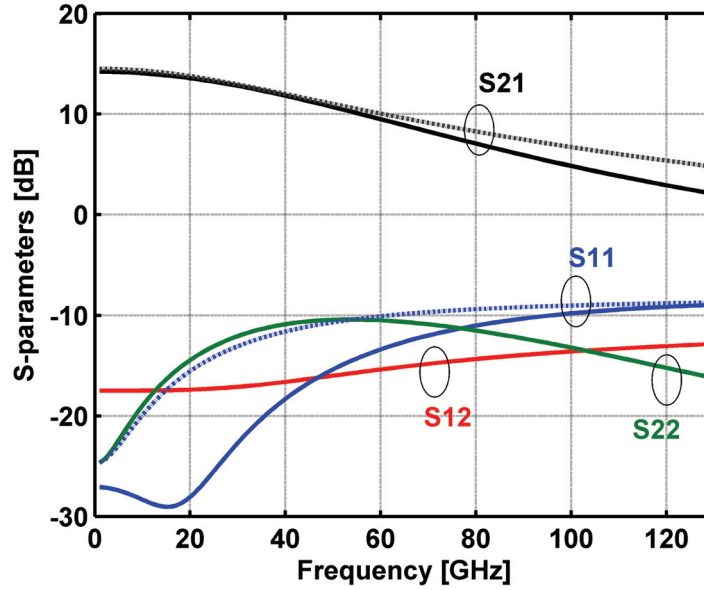


Figure 4.6: Spectre simulations (solid lines) and analytical results using (4.15) (dotted lines) of S -parameters for the Darlington feedback stage.

A staggered broadband response is possible if the product of $S_{A,21}$ and $S_{B,21}$ is constant over the 3-dB bandwidth. However, matching between the first and second stages also impacts the stagger tuning. Several conditions mitigate the frequency dependence caused by interstage matching. First, input matching of the second stage is satisfied over the 3-dB bandwidth, i.e. $S_{B,11} = 0$. In this case, no reflection occurs at the input of the second stage and, consequently, reflections do not change the cascaded frequency response in (4.5) and (4.6). In other words, these expressions reduce to $S_{C,21} = S_{A,21}S_{B,21}$ and $S_{C,11} = S_{A,11}$. Second, if the output matching of the first stage is satisfied ($S_{A,22} = 0$), the first stage must be unilateral ($S_{A,12} = 0$) to achieve a broadband response to the 3-dB bandwidth. In either case, staggered responses using resonant elements such as shunt peaking provide bandwidth enhancement but also limit matching over a broad bandwidth ($S_{A,22} = 0$ or $S_{B,11} = 0$ are not maintained for the *entire* 3-dB bandwidth). When one of these conditions is satisfied, the staggered transimpedance response shown in Fig. 4.1 is

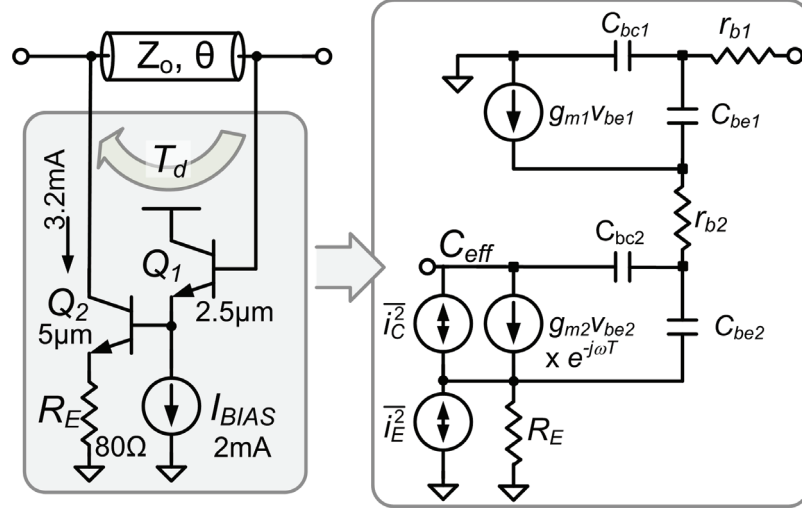


Figure 4.7: Transmission line with shunt-shunt feedback circuit without biasing circuitry (left) and small signal circuit model (right).

$$Z_{T,C} \approx \frac{Z_o S_{A,21} S_{B,21}}{1 - S_{A,11}}. \quad (4.8)$$

The proposed design approach creates a composite transimpedance, $H_3(s)$ over two stages as shown in Fig. 4.1. The first stage provides low-frequency transimpedance gain and is denoted $H_1(s)$. If the input impedance of the first stage is matched ($S_{A,11} = 0$), $H_1(s)$ is nearly identical to $Z_o \cdot S_{A,21}$. The second stage provides high-frequency gain and is denoted $H_2(s) = S_{B,21}$. Undesired peaking occurs if the two frequency responses are mismatched.

Therefore, the transimpedance limit in (1.3) applies to $H_1(s)$ only and does not necessarily apply to $H_3(s)$. A similar approach for bandwidth enhancement has previously been demonstrated using SiGe HBT technology based on staggered impedance matching with cascaded emitter followers [64]. However, the cascaded emitter followers increase power consumption and noise figure.

4.2 Circuit Design

The staggered response is demonstrated for a SiGe broadband amplifier and illustrated in Fig. 4.4. The first amplifier stage is a Darlington feedback amplifier

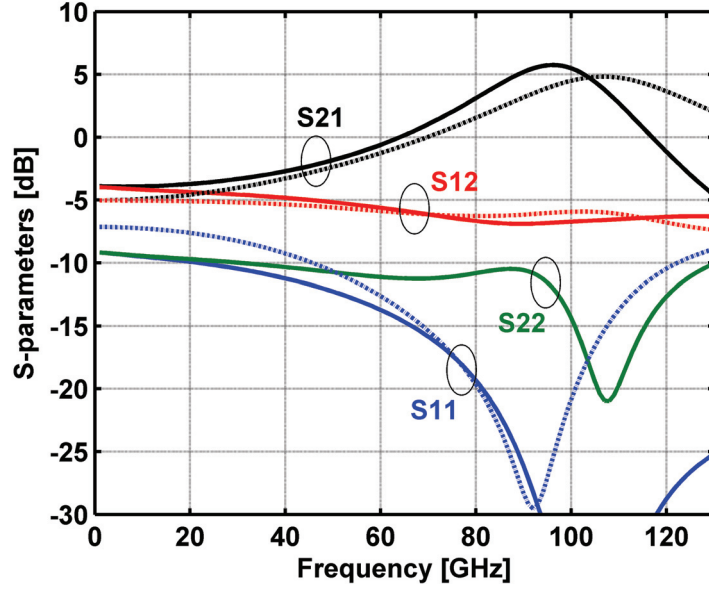


Figure 4.8: Spectre simulations (solid lines) and analytical results using (4.33)-(4.35) (dotted lines) of S -parameters for the constructive wave amplifier.

and the second stage is a constructive wave amplifier (CWA) [70]. The CWA has broadband matching with gain peaking at high frequency. In our approach, a reference impedance, Z_o exists between the Darlington feedback amplifier and CWA that defines the matching conditions described in (4.7). Input matching to a $50\ \Omega$ impedance is desirable for TIA circuits operating at this frequency range since packaged photodiodes include a $50\ \Omega$ source termination. Output matching of the Darlington stage is chosen to be $50\ \Omega$ to match the impedance of the following CWA and external testing environment. The following circuit analysis demonstrates how the frequency response of $H_1(s)$ and $H_2(s)$ interact to achieve high 3-dB bandwidth, low group delay variation, and low gain-ripple. In each section, circuit intuition about the proper design of S_{11} and S_{21} is demonstrated based on Y -parameters.

4.2.1 Darlington Stage

The Darlington stage is analyzed in terms of Y -parameters to assess the broadband matching conditions. Fig. 4.5 shows the circuit schematic of a Dar-

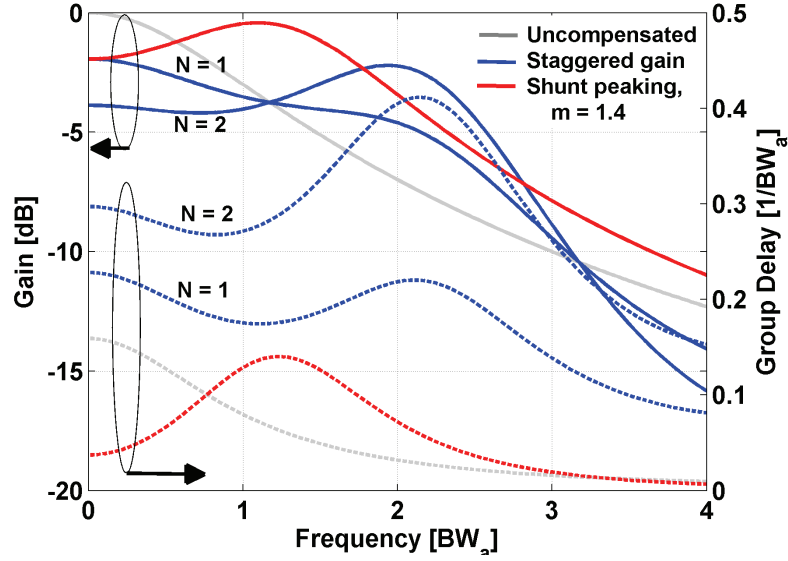


Figure 4.9: Comparison of uncompensated response with a staggered response introduced with the constructive wave amplifier and shunt peaking response.

$N = 1$ and 2 refers to the number of constructive wave amplifiers.

lington stage with resistive shunt feedback [71]. The Darlington stage offers higher unity current gain cut-off frequency, f_T , than each individual transistor and increases the maximum available transimpedance. Although a practical Darlington stage might not double the cut-off frequency, recent work has shown the effective cut-off frequency of Darlington stage in a $0.12\text{-}\mu\text{m}$ SiGe BiCMOS technology is 325 GHz, or about 1.7 times higher than the f_T of a single transistor (200 GHz) [72].

A simplified Y -parameter model, Y_D , for the Darlington stage can be found from the small-signal equivalent circuit in Fig. 4.5 under the unilateral device assumption that $C_{bc1,2} = 0$:

$$Y_{D,11} = \frac{1}{r_{i,D}} = \frac{1}{r_{b1} + r_{D1}(1 + g_{m1}r_{D2}) + r_{D2}}, \quad (4.9)$$

where $r_{D1} = \frac{r_{\pi 1}}{1 + sC_{be1}r_{\pi 1}} \approx \frac{1}{sC_{be1}}$ and $r_{D2} = \left[r_{b2} + \frac{r_{\pi 2}}{1 + sC_{be2}r_{\pi 2}} \right] \parallel R_E \approx \frac{R_E(1 + sC_{be2}r_{b2})}{1 + sC_{be2}(R_E + r_{b2})}$. Approximations for r_{D1} and r_{D2} are valid at mid-band frequency below the 3dB bandwidth.

The forward transadmittance of the Darlington stage is

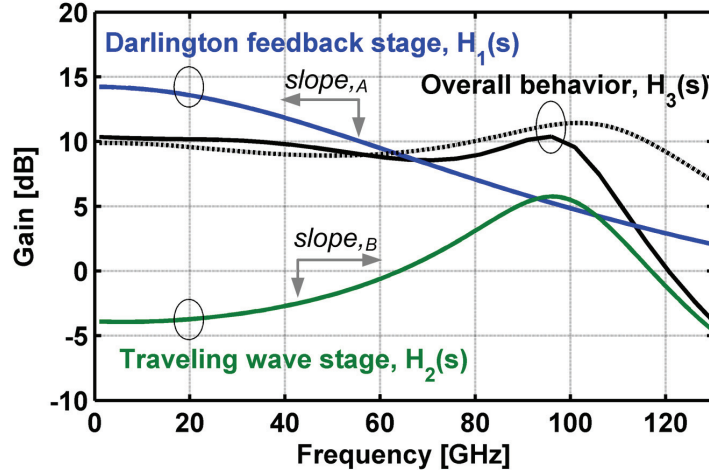


Figure 4.10: Spectre simulations (solid lines) and analytical result (dotted line) of S_{21} frequency response: Darlington feedback stage, the traveling wave stage, and overall behavior.

$$Y_{D,21} = g_{m,D} = \frac{g_{m1}r_{D1}(1 + g_{m2}r_{D2}) + g_{m2}r_{D2}}{r_{i,D}}. \quad (4.10)$$

At d.c., the transconductance of the Darlington stage is found from (4.10);

$$g_{m,D} \approx g_{m1} \frac{1 + g_{m2} \cdot (R_E \parallel (r_{b2} + r_{\pi2}))}{1 + g_{m1} \cdot (R_E \parallel (r_{b2} + r_{\pi2}))}, \quad (4.11)$$

where the approximation assumes $r_{\pi1} \gg r_{b1}$. While the current gain is approximately the product of the gains of the two transistors $\beta_{eff} \approx \beta_{Q1} \cdot \beta_{Q2}$ [73], the transconductance of the Darlington stage is to that of each transistor if $g_{m,1} = g_{m,2}$. If the output resistance from both transistors is negligible, $Y_{D,22}$ is roughly zero ($r_{o,D} \approx \infty$). Additionally, the Darlington stage is assumed to remain unilateral, $Y_{D,12} = 0$.

The schematic of the implemented circuit is shown in Fig. 4.5. The emitter lengths of Q_1 and Q_2 are $7 \mu\text{m}$ and $10 \mu\text{m}$ respectively to maximize the bandwidth of the Darlington stage. Larger emitter lengths increase the base-collector capacitance and degrade the bandwidth and stability. On the other hand, small devices provide insufficient transconductance to provide gain into a 50Ω load. In addition, smaller Q_1 increases the HBT base resistance r_{b1} , reducing the bandwidth. R_E is selected to be 100Ω to compensate for the different sizing and provide the

appropriate base bias voltage of Q_2 . The output resistance of Q_1 and Q_2 appears in a parallel combination and the emitter degeneration (R_2) increases the output resistance, i.e. $(1 + g_{m2}r_{o2}) R_2$. Simulation indicates that the effective cut-off frequency of the Darlington stage illustrated in Fig. 4.5 (inside of the triangle) is about 264 GHz which 1.33 times higher than a single transistor. Therefore, the transimpedance limit in (1.3) for 100 GHz bandwidth is increased to 40.5 dB· Ω from the original value of 38 dB· Ω .

Table 4.1: Small-Signal Parameters for a 0.12- μm SiGe HBT

	Q_1	Q_2^*
g_m (mS)	223	148
C_{be} (fF)	130	170
C_{bc} (fF)	45	50
r_b (Ω)	55	280
r_π (Ω)	1500	1500
r_o (Ω)	1700	1700

*: effective parameters with R_2 in Fig. 4.5.

4.2.2 Darlington Transimpedance Amplifier

The first stage, $H_1(s)$, of the broadband amplifier provides transimpedance to 40 GHz using resistive feedback in a Darlington amplifier. The admittance of the Darlington transimpedance amplifier, Y_A , is found from the shunt-shunt interconnection of Y_D and the feedback resistor, R_F ;

$$Y_A = Y_F + Y_D, \text{ where } Y_F = \frac{1}{R_F} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}. \quad (4.12)$$

The input impedance of a resistive shunt feedback amplifier is $R_{in} = R_F / (1 + A_D)$ where A_D is the voltage gain of the Darlington stage. For simplicity, we assume $Y_{12,D} = Y_{22,D} = 0$. By translating Y -parameters into S -parameters, the input return loss of the Darlington feedback stage is approximately

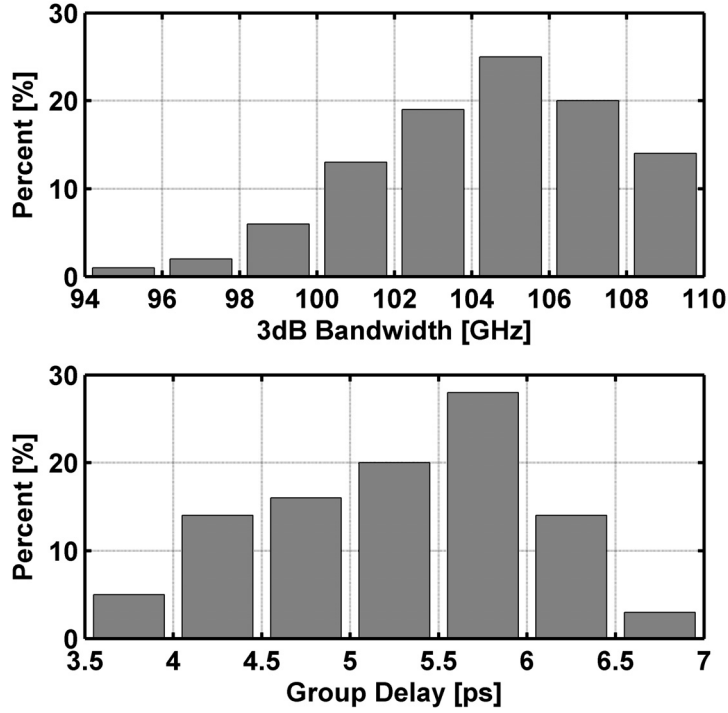


Figure 4.11: Monte Carlo realizations of the effect of process variations on the 3-dB bandwidth and group delay variation (Ibias = 3 mA).

$$\begin{aligned}
 S_{A,11} &= \frac{(R_F Y_0)^2 - 1 - Y_{A,21} R_F}{(R_F Y_0 + 1)^2 + Y_{A,21} R_F} \\
 &= \frac{R_F Y_0 - g_{m,D} Z_0}{R_F Y_0 + 2 + g_{m,D} Z_0},
 \end{aligned} \tag{4.13}$$

where $Y_o = 1/Z_o$. For input matching, we find that $R_F = g_{m,D} Z_0^2$. In the previous section, the maximum f_T for the Darlington stage is 260 GHz. Consequently, the f_T implies that a 40 GHz bandwidth limits the voltage gain to approximately 6. If the $A_D = g_{m,D} Z_o \approx 6$, then R_F is chosen to be 300 Ω for an input and output impedance of 50 Ω . This impedance is appropriate for testing in a 50 Ω environment but is not a critical design constraint. Note that the condition in the numerator of (4.13) holds as long as the $g_{m,D}$ does not change with frequency and is not necessarily dictated by the 3-dB bandwidth.

The gain is also defined by the conversion of Y -parameters into S -parameters under similar assumptions;

$$S_{A,21} = \frac{-2 \cdot Y_{A,21} R_F Z_0}{(Y_{A,11} Z_0 + 1)(Z_0 + R_F) + Y_{A,21} Z_0^2} \quad (4.14)$$

$$\approx \frac{-g_{m,D} R_F}{1 + Y_{D,11} R_F + g_{m,D} Z_0}.$$

The frequency response of $S_{A,21}$ depends on the admittance seen at the input of the amplifier stage in the denominator. If the input admittance of the Darlington stage is zero, the gain approaches $S_{A,21} = -(R_F/Z_0)$. As described in the introduction, the admittance at the input is dominated by the photodiode capacitance and the input capacitance of the amplifier stage. Under broadband matching conditions at the source and load ports ($Z_S = Z_L = Z_o$), $S_{A,21}$ is equivalent to a voltage transfer function, $S_{A,21} = v_{out}(s)/v_{in}(s)$, which is expressed as a rational polynomial;

$$H_1(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{b_0 + b_1 s}{a_0 + a_1 s + a_2 s^2}, \quad (4.15)$$

where a_n and b_n are coefficients of polynomial. The coefficients of the rational polynomial, a_n and b_n , describing the voltage transfer function of the Darlington shunt feedback amplifier are determined from the circuit model in Fig. 4.4. The polynomial coefficients in the denominator of (4.15) are

$$a_0 = x d_1 + g_{m1} Z_o d_2 \quad (4.16)$$

$$a_1 = C_{be1} ((Z_o + r_{b1} + R_E) x + Z_o (g_{m2} R_E - 1)) + C_{bc1} x d_1 (Z_o + r_{b1}) \\ + (C_{be2} + C_{bc2}) (x (R_E + r_{b2} d_1) + g_{m1} Z_o (R_E + r_{b2} d_2)) \quad (4.17)$$

$$a_2 = C_{be1} C_{bc1} R_E (Z_o + r_{b1}) x + C_{bc1} (C_{be2} + C_{bc2}) (R_E + r_{b2} d_1) (Z_o + r_{b1}) x \\ + C_{be1} (C_{be2} + C_{bc2}) [x ((R_E + r_{b2}) (Z_o + r_{b1}) + r_{b2} R_E)] \\ - C_{be1} Z_o (C_{be2} + C_{bc2}) (R_E + r_{b2} (1 - g_{m2} R_E)) \quad (4.18)$$

where $x = 2 + Y_o R_F$, $d_1 = 1 + g_{m1} R_E$, and $d_2 = 1 + g_{m2} R_E$. The polynomial coefficients in the numerator of the transfer function are

$$b_0 = d_1 - g_{m1} R_F d_2, \quad (4.19)$$

and

$$b_1 = C_{be1} (r_{b1} + R_E (1 - g_{m2} R_F)) + C_{bc1} r_{b1} d_1 + (C_{be2} + C_{bc2}) \left[R_E + r_{b2} d_1 - R_F (g_{m1} r_{b2} d_2 + g_{m2} R_E) \right]. \quad (4.20)$$

Assuming the transistors are identical and have a large transconductance, we can assume $d_1 = d_2 \gg 1$. Additionally, the input matching condition is imposed, $x \approx Y_o R_F = g_{m1} Z_o$, based on the estimation of the matching condition from (6.12a). A final approximation is that the base-emitter capacitance, C_{be} , is much larger than the base-collector capacitance, C_{bc} . Therefore, the terms in (4.16), (4.17), and (4.18) simplify to

$$a_0 \approx 2g_{m1} Z_o d_1, \quad (4.21)$$

$$a_1 \approx C_{be1} g_{m1} Z_o (Z_o + r_{b1} + 2R_E) + C_{be2} g_{m1} Z_o (2R_E + 2r_{b2} d_1), \quad (4.22)$$

and

$$a_2 \approx C_{be1} C_{bc1} g_{m1} Z_o R_E (Z_o + r_{b1}) + C_{be2} C_{bc1} g_{m1} Z_o (Z_o + r_{b1}) (R_E + r_{b2} d_1) + C_{be1} C_{be2} g_{m1} Z_o ((Z_o + r_{b1}) (R_E + r_{b2}) + 2r_{b2} R_E). \quad (4.23)$$

Similarly,

$$b_0 \approx -g_{m1} R_F d_1, \quad (4.24)$$

$$b_1 \approx - (C_{be1} g_{m2} R_F R_E + C_{be2} r_{b2} d_1 g_{m1} R_F). \quad (4.25)$$

Consequently, the first-order pole and zero of the Darlington stage are located at approximately

$$\frac{a_1}{a_0} \approx \frac{C_{be1}}{2d_1} (R_E + 2r_{b2} d_1) \quad (4.26)$$

$$\frac{b_1}{b_0} \approx \frac{C_{be1}}{d_1} (R_E + r_{b2}d_1). \quad (4.27)$$

When r_{b2} is large, the first-order time constant is approximately $C_{be1}r_{b2}$ for both terms.

The dc gain, $\left. \frac{v_{out}}{v_{in}} \right|_{j\omega=0} = b_0/a_0$, is expressed in (4.21) and (4.24) and is approximately $\frac{-g_{m,D}^2 R_F R_E}{(1+g_{m,D}Z_o)(1+g_{m,D}R_E)}$ when $g_{m,1} = g_{m,2} = R_F/Z_o^2$, and the base resistance is ignored, e.g. $r_{b,1} = r_{b,2} = 0$.

The first-order pole and zero associated with a_1/a_0 and b_1/b_0 are approximated from (4.22) and (4.25). Assuming identical device geometry, the time constant of the first-order pole and zero is approximately $C_{be}r_{b,2}$. The small-signal parameters for the proposed Darlington stage are listed in Table 4.1. From the circuit analysis of the poles, the first-order pole is located at 12.4 GHz and is canceled by the first-order zero located at 12.1 GHz. Consequently, the second-order pole at a_2/a_0 determines the 3dB bandwidth and is located at 43.5 GHz, i.e. $BW_A = 43.5$ GHz. In this case, the Darlington stage might be approximated by a first-order response,

$$H_1(s) = \frac{b_0}{a_0} \frac{1}{1 + s\tau_A}, \quad (4.28)$$

where τ_A is the time constant associated with BW_A . For a first-order response, the group delay is τ_A near d.c. and approaches zero at high-frequency. Within the 3-dB bandwidth, the group delay variation (GDV) of the first stage, GDV_A , is $0.49\tau_A$ or around 1.9 ps.

Simulated S -parameters for the Darlington transimpedance stage are shown in Fig. 4.6 using Spectre. The simulations predict a d.c. gain of 14.2 dB and a 3-dB bandwidth of 46 GHz. This gain translates into a transimpedance of $R_T = 250 \Omega$ or 48 dB $\cdot\Omega$. The input and output return losses are nominally less than 10 dB from d.c. to more than 120 GHz. In addition, the reverse isolation is better than 15 dB across the entire 3-dB bandwidth. Therefore, the conditions $S_{A,22} = 0$ and $S_{A,12} = 0$ in (4.8) are essentially satisfied. The numerical results of (4.15) and expressions for the pole and zero locations are shown in Fig. 4.6 for comparison

with circuit simulations. Both results suggest that the slope of S21 is dominated by a single pole below 100 GHz.

4.2.3 Constructive Wave Stages

The fundamental constructive wave amplifier (CWA) is presented in [69]. Briefly, a CWA stage provides high-frequency gain, $H_2(s)$, without sacrificing broadband matching. The CWA consists of shunt-shunt feedback across a transmission line as shown in the top-left of Fig. 4.7 and the response is determined from the combination of admittance parameters;

$$Y_{CWA} = Y_{TL} + Y_{FB}. \quad (4.29)$$

For a lossless transmission line of length of l ,

$$Y_{TL} = Y_o \begin{bmatrix} \cot(\beta l) & -\csc(\beta l) \\ -\csc(\beta l) & \cot(\beta l) \end{bmatrix}, \quad (4.30)$$

where β is the phase constant of the transmission line. The feedback has a small signal transconductance found from the small-signal model in Fig. 4.7;

$$Y_{FB,21} \approx g_{m,eff} \frac{1}{1 + s\tau_{FB}}, \quad (4.31)$$

where $g_{m,eff} = g_{m2}/(1 + g_{m2}R_E)$. The current bias, I_{bias} , of the emitter follower adjusts the transconductance, $g_{m,2}$ and consequently the feedback gain, $A_V = g_{m,eff}Z_o/2$. If the base-collector capacitance is ignored,

$$\tau_{FB} = (1 + g_{m2}R_E) C_{be1} + (1 + g_{m1}(r_{b2} + R_E)) C_{be2}. \quad (4.32)$$

The time delay through the active feedback is estimated to be 2 ps at 100 GHz.

If the input and output admittance is small, the Y -parameters in (4.29) are transformed into S -parameters for a single CWA stage. Assuming $Y_{FB,12} = 0$, the forward transmission is

$$S_{B,21} = \frac{e^{-j(\omega\tau_{FB} + \beta l)}}{1 + A_v e^{-j(\omega\tau_{FB} + \beta l)}} = \frac{e^{-j\omega\tau_B}}{1 + A_v e^{-j\omega\tau_B}}, \quad (4.33)$$

where $\tau_B = \tau_{FB} + \frac{l}{v_p}$ and v_p is the phase velocity along the line. The maximum gain is reached when the overall phase through the transmission line and the feedback amplifier, $\omega\tau_B$, is π -radians. Therefore, the center of the amplifier gain response is located at $f_o = \frac{1}{2\tau_B}$. Under this condition, the maximum gain per stage is $|S_{B,21}|_{max} = 1/(1 - A_v)$. However, the gain rolls-off from the center frequency of this stage. Near d.c., the gain is $|S_{B,21}|_{min} = 1/(1 + A_v)$. Consequently, the slope of each traveling wave stage is

$$\nabla_{CCWA} \approx \frac{20 \log_{10} \left(\frac{1+A_v}{1-A_v} \right)}{\text{decade}}. \quad (4.34)$$

This slope is chosen to compensate the roll-off of the Darlington transimpedance amplifier. Clearly, a larger slope is achieved using a larger A_v . Unfortunately, larger choices for A_v result in larger input return loss. From [69], the input and output return loss is

$$S_{B,11} = S_{B,22} = \frac{A_v}{1 + A_v e^{-j\omega\tau_B}}, \quad (4.35)$$

and must be constrained to roughly $A_v \leq 0.27$. This bound on the feedback gain suggests that a single CWA provides around 5 dB of compensation per decade. Consequently, two cascaded CWA (CCWA) stages offer 10-dB gain per decade to compensate the roll-off of the Darlington amplifier. The forward transmission achieves a gain of 4.8 dB and -6.3 dB of isolation at f_o .

The bandwidth of a single CWA is calculated in [69].

$$BW_B = 2f_o \left(1 - \frac{1}{\pi} \arccos \left(\frac{1}{2A_v} + \frac{A_v}{2} - 2 \right) \right). \quad (4.36)$$

As A_v increases, the bandwidth decreases. Since the matching conditions bound the gain of the CWA stage to 2.5 dB ($A_v = 0.27$), the 3-dB bandwidth is equal to f_o and the frequency response remains relatively wideband. As additional CWA stages are introduced, the bandwidth tends to narrow.

The group delay for a single CWA stage is determined from (4.33);

$$GD_{B,21} = \frac{1}{2} \tau_B \frac{1 - A_v^2}{1 + 2A_v \cos(\omega\tau_B) + A_v^2}. \quad (4.37)$$

The GDV is calculated from the maximum and minimum values of (4.37) over the 3-dB bandwidth. The minimum group delay occurs at $\omega = 0$ and the maximum group delay occurs at $\omega = \pi/\tau_B$.

$$GDV_B = 2\tau_B \frac{A_v}{1 - A_v^2} \quad (4.38)$$

Therefore, the GDV depends on the feedback gain. As the gain approaches zero, the GDV also approaches zero. If $A_v = 0.27$, $GDV_B \approx 0.25\tau_B$. In other words, a single CWA with a center frequency of 100 GHz exhibits 2.5 ps of GDV.

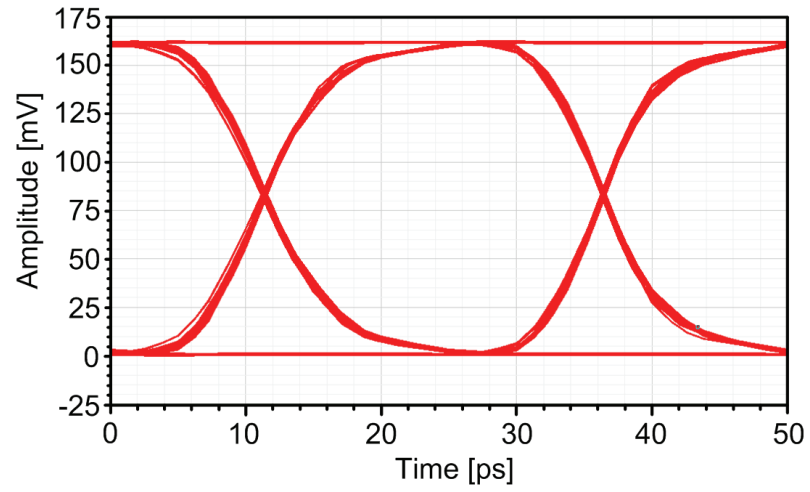
Simulated S -parameters for the two cascaded traveling wave stage are shown in Fig. 4.8. Spectre simulations indicate that a gain of 5.7 dB at 98 GHz and 4dB of attenuation at d.c. The input and output return losses are nominally less than 10 dB from a d.c. to 130 GHz. Therefore, the condition, $S_{B,11} = 0$, in (4.8) is satisfied for cascaded gain. The analytical results using (4.29) are compared to Spectre simulations and demonstrates accurate prediction of S_{21} , S_{12} and S_{11} with the hand calculations of (4.33).

4.2.4 Staggered Broadband Frequency Response

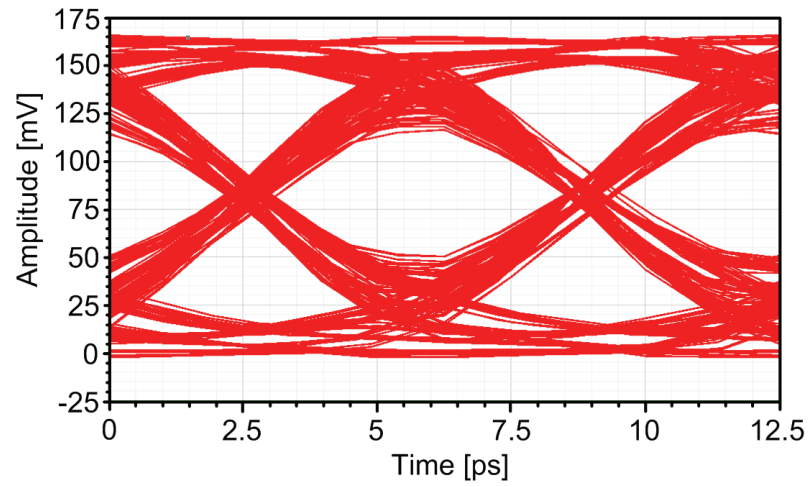
The ensemble staggered frequency response is deduced from Sections 4.2.2 and 4.2.3. If the bandwidth of the first stage, BW_A , is considered the uncompensated response, the second stage compensates through stitching the peaking in the second stage for maximum bandwidth. The lower 3-dB frequency of the bandpass response of the CWA stage is located at $f_o - \frac{1}{2}BW_B = BW_A$ where BW_B is defined from (4.36). Hence, the center frequency of the CWA stage is located at

$$f_o = \frac{\pi BW_A}{\arccos\left(\frac{1}{2A_v} + \frac{A_v}{2} - 2\right)} \quad (4.39)$$

If the CWA stage provides 2.5-dB gain, the center frequency is $2.1 BW_A$. In other words, the staggered response bandwidth can be more than 84 GHz for a 40 GHz uncompensated bandwidth. A bandwidth enhancement ratio (BWER) compares the bandwidth of compensated response to the uncompensated response. For a single CWA stage, the BWER is around 2.2.



(a)



(b)

Figure 4.12: Simulated output eyes with $800\mu A_{PP}$ input swing for (a) 40-Gb/s, and (b) 160-Gb/s.

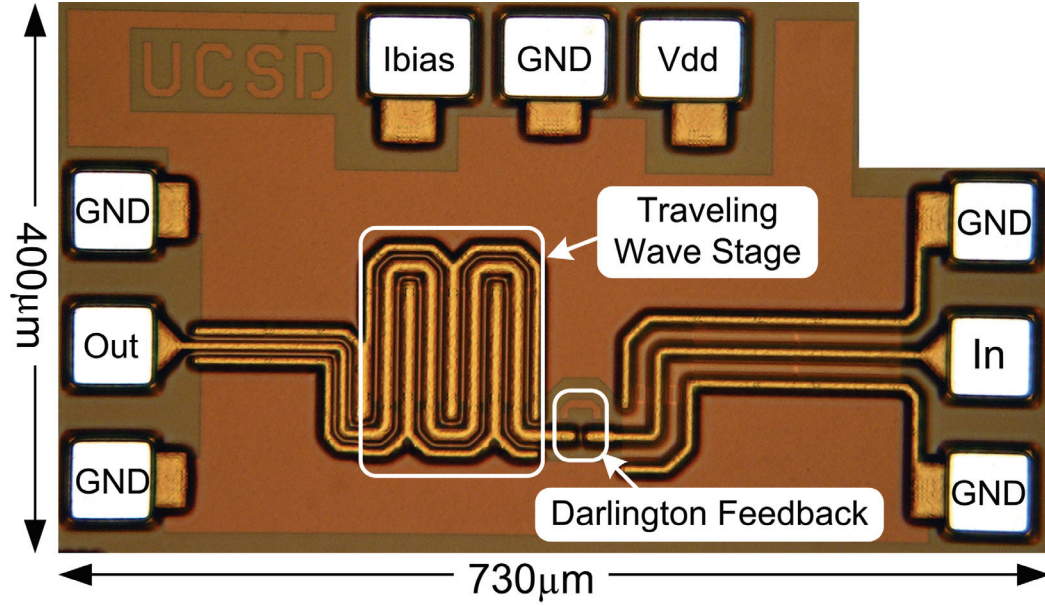


Figure 4.13: Chip microphotograph of the 100GHz transimpedance amplifier in 0.12- μm SiGe BiCMOS.

The staggered frequency response from (4.28) and (4.33) is plotted in Fig. (4.9) for one and two CWA stages and compared to the uncompensated response. A single CWA stage following the first-order response results in a BWER of $2.11 BW_A$ while the cascade of two CWA stages results in a BWER of $2.7 BW_A$.

The staggered group delay is also plotted on the right axis in Fig. (4.9). For a single CWA stage, the GDV across the compensated 3-dB bandwidth is $0.31\tau_A$ or approximately 1.3 ps for a 40 GHz bandwidth. For two CWA stages, the GDV increases nearly threefold to $0.87\tau_A$ or 3.6 ps. However, the second stage improves the gain flatness across the 3-dB bandwidth as well as reaching higher bandwidth.

4.2.5 Comparison to Shunt Peaking Techniques

Prior work has investigated BWER improvements through the introduction of resonance near the uncompensated 3-dB bandwidth [16, 47, 74]. Several approaches suggest shunt or series peaking with a single inductor or bridged circuit through coupled inductors. The general shunt-peaking frequency response is characterized by

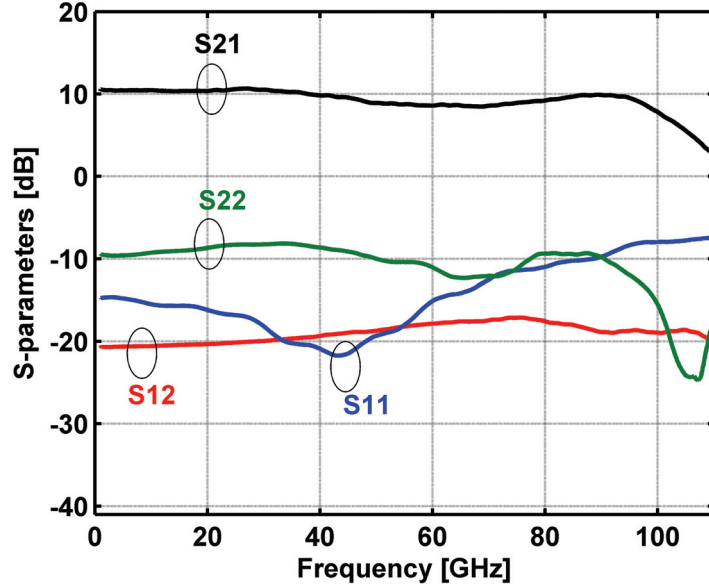


Figure 4.14: Measured S -parameters for the proposed broadband amplifier.

$$H_{shunt}(\omega) = A_0 \frac{1 + \frac{s}{m\omega_o}}{1 + \frac{s}{\omega_o} + \frac{s^2}{m\omega_o^2}} \quad (4.40)$$

and ω_o is the uncompensated bandwidth. For $m = 1.4$, the response has maximum bandwidth and results in a BWER of approximately 1.8. The GDV is approximately $0.81\tau_A$ [19]. For 40 GHz uncompensated bandwidth, the GDV of the shunt peaking response is 3.2 ps.

For comparison, the shunt peaking response is compared to the CWA approach in Fig. 4.9 where the d.c. gain reduction is incorporated into the BWER of the shunt peaking response. For $m = 1.4$ and a 2-dB gain reduction, the BWER is approximately 2.29 while the group delay variation is $0.63\tau_A$. In other words, the 40 GHz bandwidth can be improved to 91 GHz with 2.5 ps of GDV. Consequently, the addition of a single CWA stage achieves similar BWER to the second shunt peaking example but *half* of the group delay variation. Additionally, the output matching for the CWA approach is preserved over the entire 3-dB bandwidth which is not generally true for a shunt-peaking amplifier.

4.2.6 Noise Factor Analysis

The noise factor for the cascaded Darlington transimpedance amplifier and CWA is

$$F_T = F_D + \frac{F_{CWA} - 1}{G_D}, \quad (4.41)$$

where F_D and F_{CWA} are the respective noise factors of the Darlington amplifier and CWA and G_D is the Darlington amplifier gain. The roll-off of G_D at high-frequency indicates that at high-frequency the CWA noise factor more strongly impacts the overall noise factor.

The input referred noise of the Darlington feedback stage is calculated for the collector and the base shot noise sources of the first transistor (Q_1) in Fig. 4.5 [75].

$$\overline{v_{n,1}^2} = 4kT \left(r_{b,1} + \frac{1}{2g_{m,1}} + R_{E,1} \right) = 4kT \cdot R_{eq,1} \quad (4.42)$$

$$\overline{i_{n,1}^2} = 2qi_{B,1} + \frac{2qi_{C,1}}{|\beta_1(j\omega)|^2} + \frac{\overline{v_{n,1}^2}}{R_F^2} + \frac{4kT}{R_F} \quad (4.43)$$

Typically, the last term in (4.43) dominates and the noise factor for the Darlington amplifier is approximated as

$$F_D = 1 + \frac{\overline{v_{n,1}^2}}{v_{R_S,1}^2} + \frac{\overline{i_{n,1}^2}}{i_{R_S,1}^2} \approx 1 + \frac{R_{eq,1}}{R_S} + \frac{R_S}{R_F} \quad (4.44)$$

where the input referred current noise is assumed to be dominated by the $4kT/R_F$. The shunt feedback resistor should be as large as possible to minimize the input referred current noise. Based on the values in Table 4.1, the Darlington amplifier stage has a noise figure of 6.3 dB.

The noise performance of the CWA stage is predicted from the noise model shown in Fig. 4.7. The noise factor is calculated based on the series combination of the collector shot noise, $\overline{i_C^2}$, and noise generated by the emitter degeneration resistor, $\overline{i_E^2}$, e.g. $\overline{i_E^2} = \frac{4kT}{R_E} \Delta f$. The noise factor is derived from these two noise sources as

$$F_{CWA} = 1 + \frac{\left| \frac{g_m Z_o}{e^{j\omega T_d} + g_m R_e} \right|^2 \left(\bar{i}_C^2 |g_m e^{-j\omega T_d}|^{-2} + \bar{i}_E^2 R_E^2 \right)}{4kT R_{out}}, \quad (4.45)$$

For $R_E = 50\Omega$, $g_m = 10mS$, and $\bar{i}_C = \sqrt{2qI_c} = 55 \frac{pA}{\sqrt{Hz}}$, the CWA stage has a noise figure of 7 dB at low frequencies and 13 dB near $f_o = 100$ GHz. These noise figure predictions will be subsequently compared to simulation and measurement in Section 4.3.2.

4.2.7 Circuit Simulations

Fig. 4.10 compares the frequency response from the analytical predictions in the previous sections with simulations from the Spectre device models of the staggered response of the Darlington feedback and cascaded traveling wave stage. The cascaded transfer function, $H_3(s)$, in Fig. 4.10, anticipates 10-dB gain over a 3-dB bandwidth of 103 GHz. The low gain ripple results from the compensation of the S_{21} slope of $H_1(s)$ with the S_{21} slope of $H_2(s)$.

Monte Carlo simulations of the effect of process variations on the 3-dB bandwidth and group delay variation are plotted in Fig. 4.11 for a fixed bias current of the CWA stage. The mode of the 3-dB bandwidth is 104 GHz. In more than 90% of trials, the bandwidth is greater than 100 GHz indicating significant robustness of our approach to process variation. Note that the bias current of the CWA stages adjusts the 3-dB bandwidth and can compensate for these variations. Additionally the group delay variation indicates a mode of ± 6 ps and a range of 3.5 to 7 ps in 99% of the simulations. Temperature variations (not shown) can also account for bandwidth variation. At 125 C, the simulated 3-dB bandwidth drops from 106 GHz to 93 GHz.

Fig. 4.12 illustrates the simulated output eye diagrams with $800 \mu A_{PP}$ input swing for the data rates of 40 and 160-Gb/s. At 160-Gb/s, the simulated eye diagrams predicts adequate eye opening but higher jitter is observed and eye height is decreased as the data rate increases.

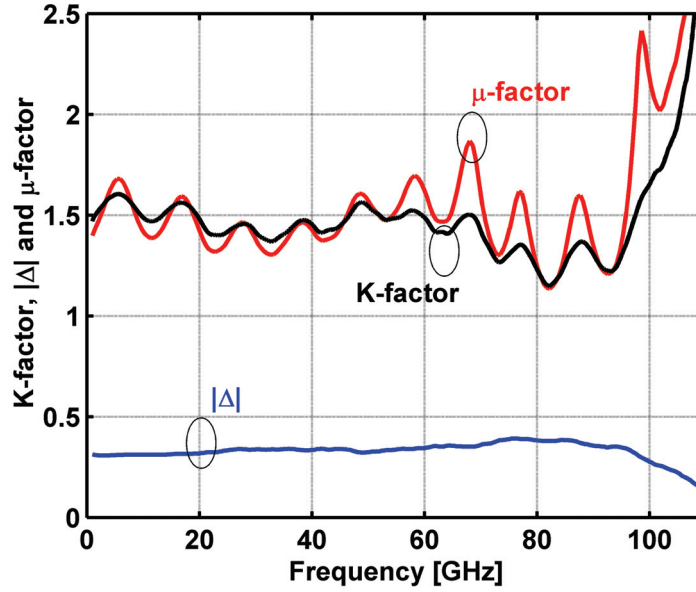


Figure 4.15: Measured stability factors indicate unconditional stability across the entire bandwidth.

4.3 Measurements

The circuit is implemented in a 0.12- μm SiGe BiCMOS technology with HBT devices ($f_T = 200 \text{ GHz}/f_{max} = 230 \text{ GHz}$). The chip microphotograph is shown in Fig. 4.13. The chip area is 0.29 mm^2 (0.73 mm by 0.4 mm), however the active circuit area is 0.02 mm^2 . The chip consumes 36.5 mA from a 2 V supply. The Darlington feedback amplifier consumes a total of 21 mA at $I_{bias} = 0 \text{ mA}$.

4.3.1 Small-Signal Measurements

S -parameters are measured with the Agilent E8361A two-port network analyzer and N5260A mm-wave controller using on-chip probing. The measured S -parameters are shown in Fig. 4.14 and can be compared to the simulated S_{21} in Fig. 4.10. The amplifier has a gain of 10.1 dB and a 3-dB bandwidth of 102 GHz. The minimum midband gain reduces to 8.6 dB at 65 GHz where gain staggering between the first and second amplifier stages results in the maximum gain ripple of 1.5 dB. The gain-bandwidth product (GBW) of this amplifier is 323 GHz. The

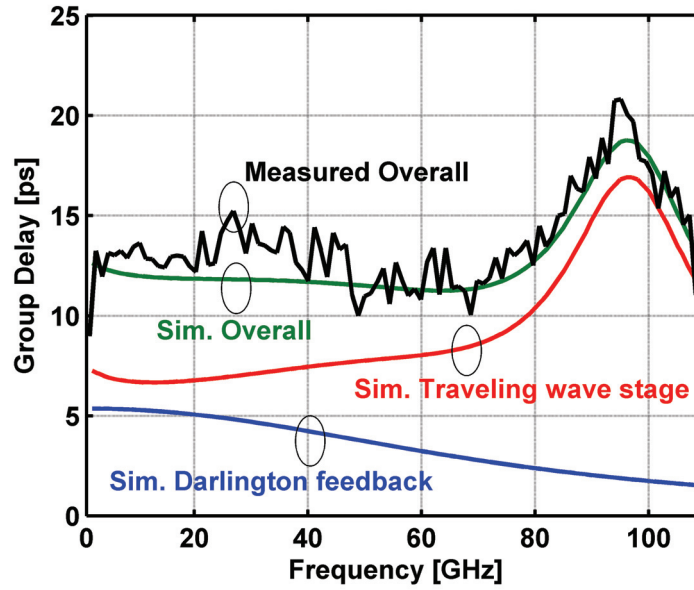


Figure 4.16: Measured and simulated group delay variation of S_{21} .

measured input return loss across the entire 3-dB bandwidth is less than 8 dB, but remains below 10 dB below 90 GHz. The output return loss is better than 9 dB over the 3-dB bandwidth. Measured reverse isolation is better than 19 dB over most of the bandwidth. The measured stability is plotted in Fig. 4.15 and indicates that the amplifier is unconditionally stable at all frequencies.

The group delay variation is measured in Fig. 4.16. The amplifier has a nominal group delay of 13 ps and group delay variation of ± 6 ps over the 3-dB bandwidth. However, the $G DV_{21}$ is only ± 2.5 ps until 85 GHz. Spectre simulations indicate that the Darlington feedback stage group delay is 5.5 ps at d.c. and decreases to 1.7 ps at 100 GHz while the group delay of the traveling wave stage increases from 6.6 ps to 17 ps.

The second stage gain is electronically tuned to compensate for the high-frequency response. The emitter follower bias of the CWA increases the gain above 70 GHz. The frequency response is plotted in Fig. 4.17. At $I_{bias} = 0$ mA, S_{21} is compared to circuit simulation and indicates that the Darlington feedback stage has 11.4-dB gain with a 3-dB bandwidth of 53 GHz. The measured gain indicates

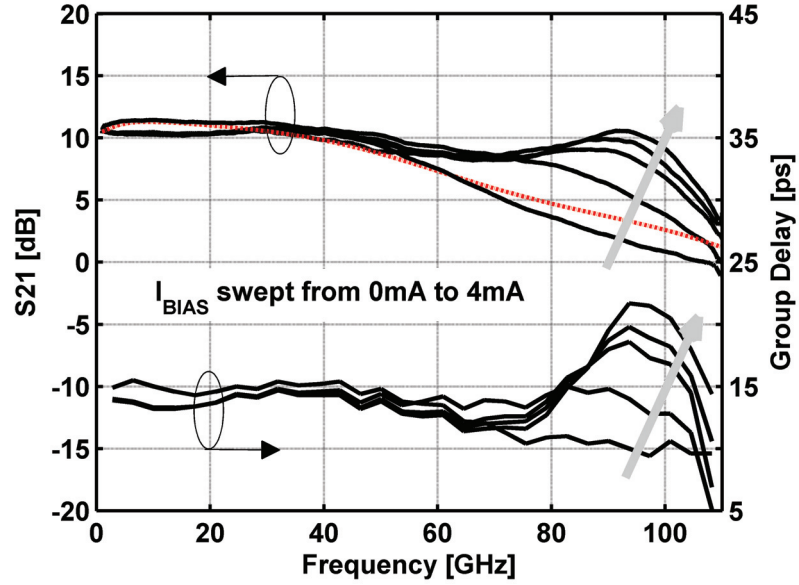


Figure 4.17: Measured S_{21} frequency response and group delay variations (solid line) as a function of the bias of the traveling wave stage for I_{bias} ranging from 0 mA to 4 mA ; simulated S_{21} at $I_{bias} = 0\text{ mA}$ bias condition (dotted line).

that the Darlington stage response rolls-off faster than simulation predicts due to the additional parasitic capacitance. For maximally flat gain, the bias current of the traveling wave stage is 3 mA . GDV_{21} is also plotted in Fig. 4.17 and indicates that the group delay increases as I_{bias} increases.

4.3.2 Noise Figure

The noise figure is measured using an Agilent E4400 spectrum analyzer with an Agilent 346C noise source for the frequency range from 1 GHz to 50 GHz and a QuinStar W -band noise source with excess noise ratio (ENR) uncertainty of $\pm 0.75\text{ dB}$ and output power flatness variation of $\pm 3\text{ dB}$. At W -band, a Pacific Millimeter Wave 75110H W -band down-converter ($G_c = -7.5\text{ dB}$ at 90 GHz) shifts the noise to an IF frequency between 4 GHz to 10 GHz . An Agilent E8257D RF synthesizer generates a subharmonic of the local oscillator (LO) and is tripled with a Pacific Millimeter W3 W -band frequency tripler and filtered with a 90 GHz to 100 GHz Pacific Millimeter MOD9010 bandpass filter. A two-stage IF amplifier provides 24 dB of

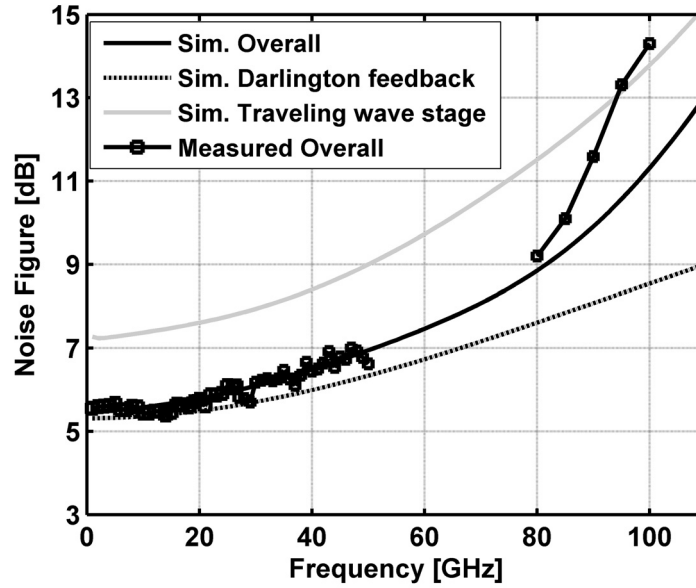


Figure 4.18: Measured and simulated noise figure.

gain to compensate the conversion loss of the mixer. The noise figure of the down-conversion stage is initially calibrated with an Agilent E4440 spectrum analyzer. Cable and probe losses are de-embedded from the noise figure measurement. The noise figure test setup is compared to a QuinStar QWL series 92-98 GHz amplifier and found to have less than 1dB error from the manufacturer specification of 6 dB at 98 GHz.

The noise figure is plotted in Fig. 4.18 and compared against Spectre simulations. The measured noise figure increases from 5.4 dB at 14 GHz to 7 dB at 50 GHz. At *W*-band, the noise figure increases from 9.2 dB at 80 GHz to 14.3 dB at 100 GHz while the simulated noise figure increases from 8.8 dB at 80 GHz to 11.3 dB at 100 GHz. The 3-dB discrepancy between the simulated and measured noise figure at *W*-band is accounted for from (4.41). Since the measured S_{21} has 2-dB less gain at 100 GHz than in simulation (Fig. 4.17) when $I_{bias} = 0$ mA, the gain of Darlington feedback amplifier is 20% lower than anticipated and the CWA noise factor contributes more strongly to overall noise factor. From (4.41), the overall noise factor increases by 3dB for a 2-dB gain reduction in the Darlington feedback amplifier and confirms the expected behavior from the analysis in Section 4.2.6.

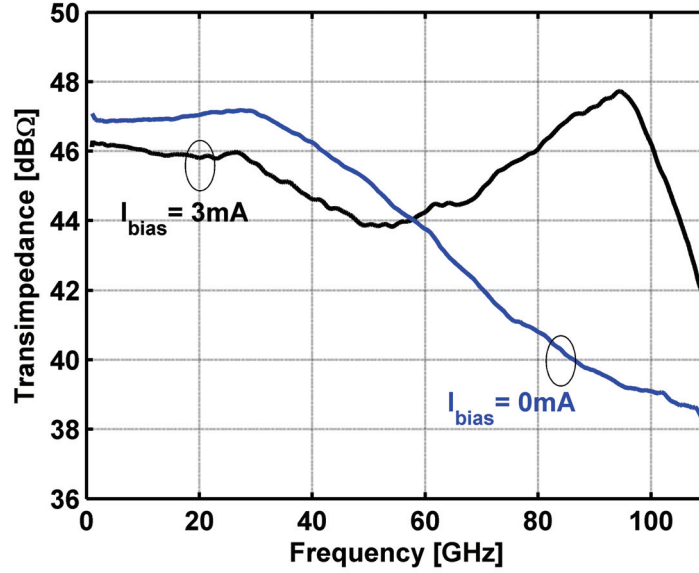


Figure 4.19: Measured transimpedance gain for 40 GHz ($I_{bias} = 0$ mA) and 100 GHz ($I_{bias} = 4$ mA) gain settings.

4.3.3 Transimpedance

The transimpedance gain and group delay variation are derived from the measured S -parameters in Section 4.3.1 using (4.3). The measured transimpedance gain is reported in Fig. 4.19 and demonstrates a transimpedance of $46 \text{ dB}\cdot\Omega$ with a 3-dB bandwidth of 108 GHz at $I_{bias} = 3 \text{ mA}$ condition. The transimpedance ripple is about $\pm 1.9 \text{ dB}\cdot\Omega$ and is reduced by controlling the bias condition, I_{bias} . However, more mid-band ripple occurs at small I_{bias} condition near 60 GHz because of gain staggering between the first and second stages. At $I_{bias} = 0 \text{ mA}$, the transimpedance is $47 \text{ dB}\cdot\Omega$ and has a 3-dB bandwidth of 53 GHz. The transimpedance group delay variation is determined from (4.3). The amplifier has a nominal transimpedance group delay of 10.2 ps and increases to 20 ps. The overall measured transimpedance group delay variation is ± 5 ps over the 3-dB bandwidth, but only ± 2.1 ps until 85 GHz.

The equivalent input noise current density is calculated from the transimpedance response and the noise figure [13]. The input referred noise current is calculated from the integration of the current noise density to twice the 3-dB

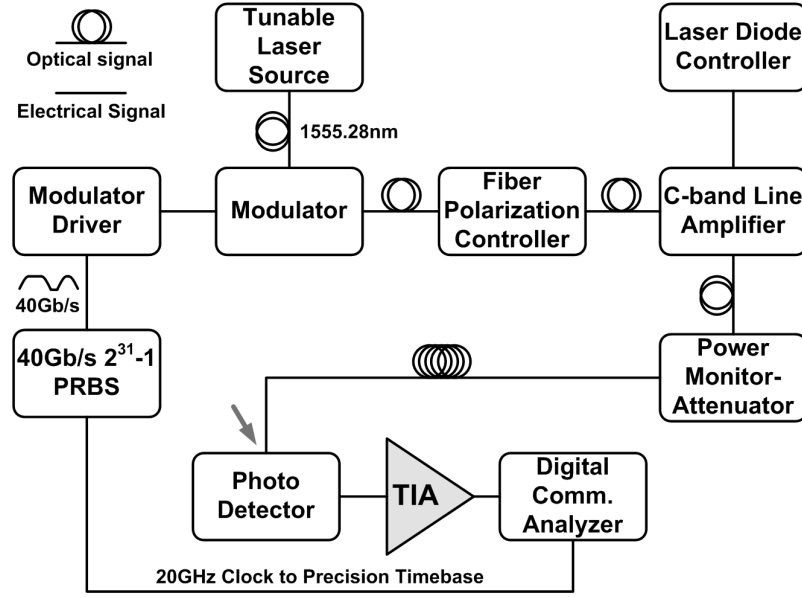
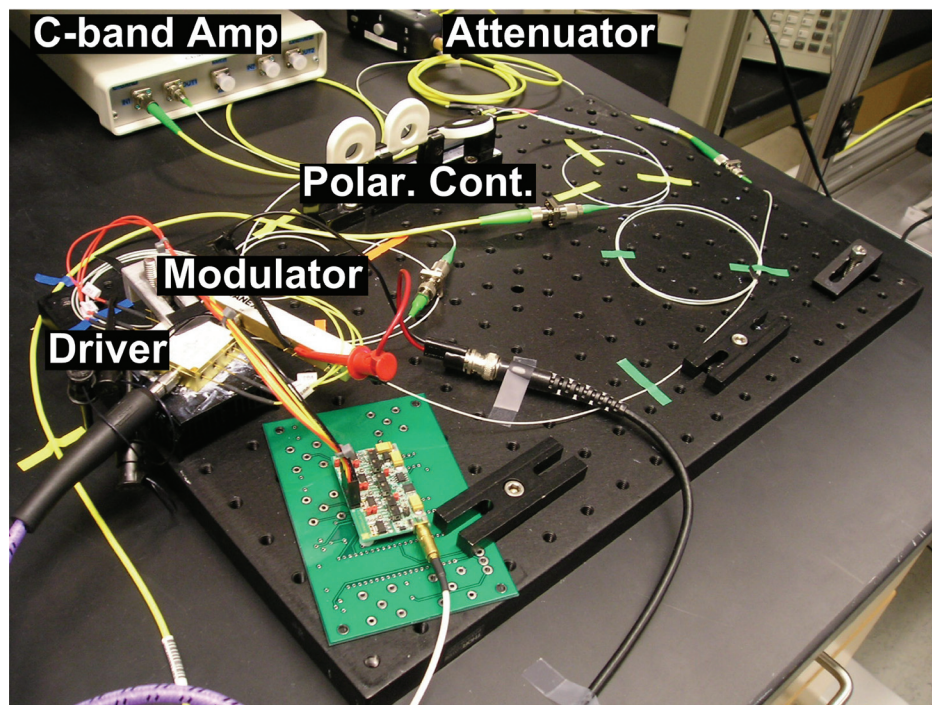


Figure 4.20: Block diagram for the optical measurement test setup.

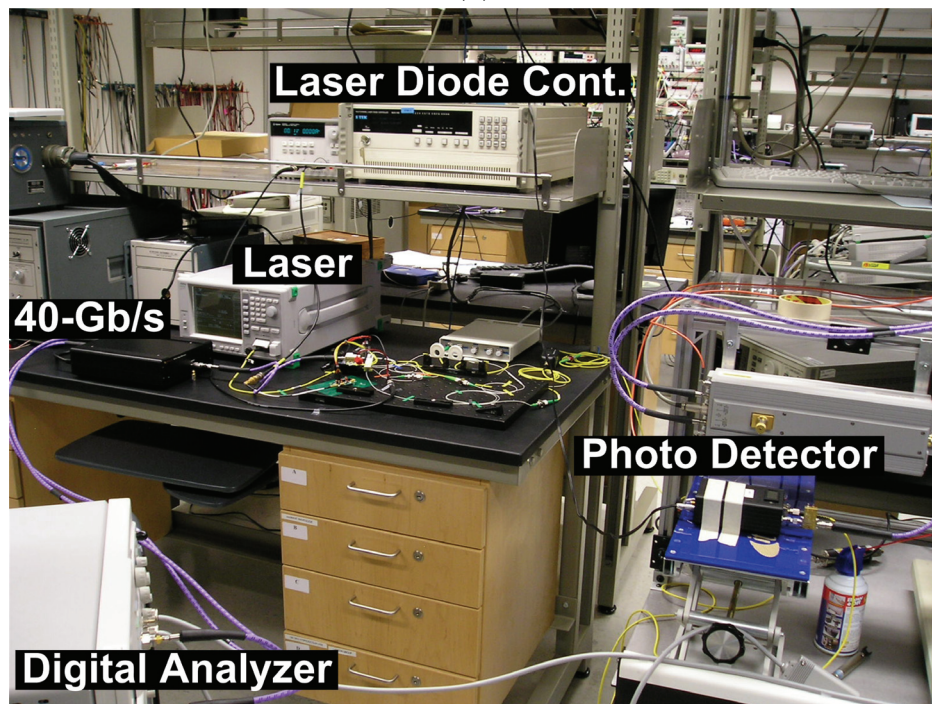
bandwidth. If the noise figure is measured to the 3-dB bandwidth, we estimate the noise current density above 110 GHz from simulation and perform the integration to find the input-referred noise current. Over a bandwidth of 100 GHz, we calculate that the rms input noise current is $17.5 \mu A$ and the average input-referred noise current density is $53.9 \text{ pA}/\sqrt{Hz}$. Therefore, the sensitivity for a receiver with a p-i-n photodetector assuming that the photodetector has a responsivity of 1 A/W is -6 dBm to achieve a BER of 10^{-12} at 160-Gb/s.

4.3.4 Time Domain Optical Measurements

The broadband TIA is demonstrated in a 40 Gb/s optical testbed to illustrate the eye diagram quality in Fig. 4.20. A 40-Gb/s, $2^{31} - 1$ pseudorandom bit sequence (PRBS) is generated from a Centellax TG1P4A pulse pattern generator and amplified with a Centellax OA4MVM modulator driver. The electrical signal modulates an Avanex PowerBit SD-40 modulator. The Anritsu MG9638A tunable laser source is set to a wavelength of 1555.28 nm and output power of 6.66 dBm. A fiber polarization controller adjusts the polarization state of the launched optical signal and E-tek MLDC-1032 multi-channel laser diode controller is connected to



(a)



(b)

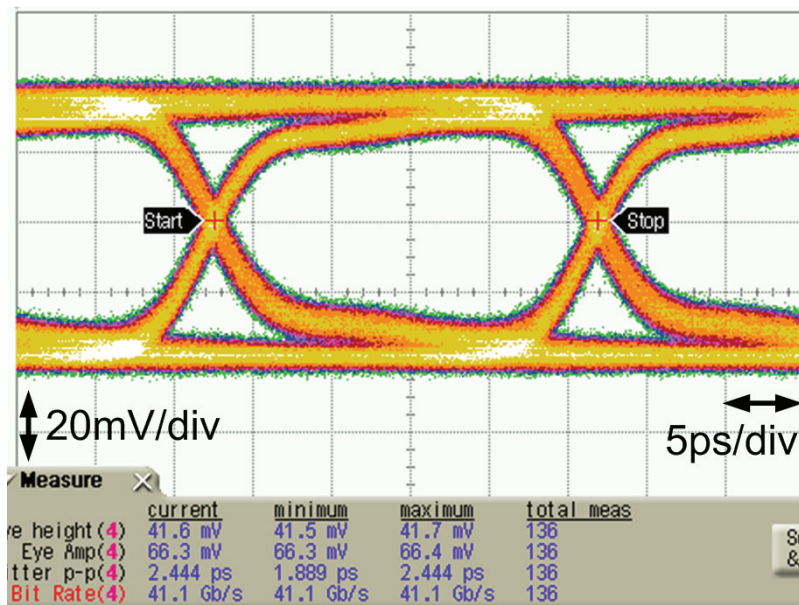
Figure 4.21: Pictures of time domain optical measurement setup.

C-band fiber amplifier.

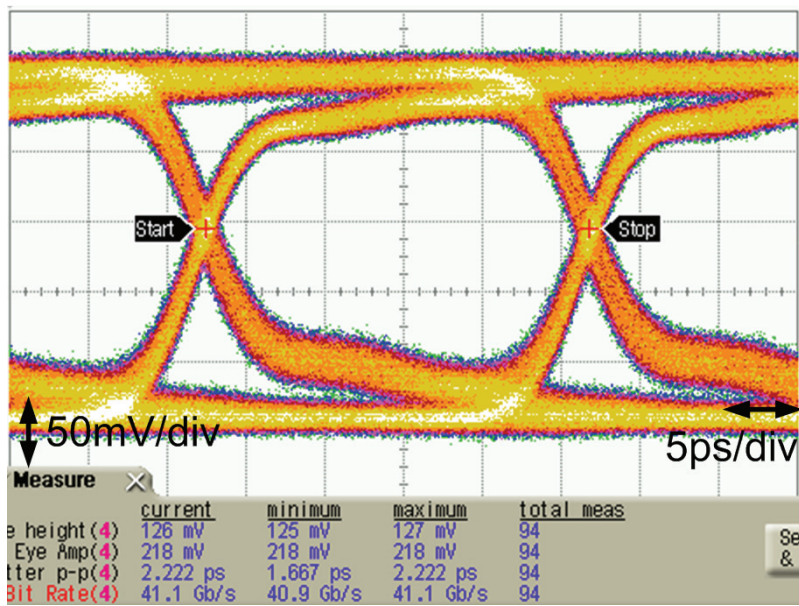
The receiver is a Discovery Semiconductors DSC10H photodetector with a 3-dB BW of 42 GHz and is connected to the 100 GHz device under test (DUT). The amplifier output is sampled with an Agilent DCA-J 86100C wide-bandwidth oscilloscope using a precision 20 GHz trigger generated by the TG1P4A. Bandwidth limitation is introduced by the combination of the photodetector (42 GHz), RF probes (67 GHz), microwave bias tees (50 GHz) and cables (50~67 GHz). Furthermore, the Agilent 86118A remote sampling head is used to measure output eye diagrams of the amplifier and has a 3-dB bandwidth of 70GHz. The measured 40-Gb/s eye diagrams are shown in Fig. 4.22(a) and (b). With an input current swing of $330 \mu A_{PP}$ and $1 mA_{PP}$, the output voltage swing is 66.3 mV and 218 mV, respectively. Based on an input referred current noise at 100 GHz of $17 \mu A$ rms, the minimum input sensitivity is $204 \mu A$ for BER better than 10^{-9} . The maximum linear input amplitude is 1.7 mA and the linear input range is around 19 dB. The peak-to-peak jitter is 2.4 ps and 2.2 ps respectively and shows low jitter at high input current. The rise and fall times of the 40-Gb/s data eye are 5 ps indicating a circuit bandwidth of 70 GHz since $BW = 0.35/t_{rise}$, which is the bandwidth limit the sampling scope. Fig. 4.21 shows that the pictures of time domain optical measurement setup.

While pulse-pattern generators operating above 40Gb/s are currently unavailable, an eye-diagram is projected from the measured amplifier S -parameter data and an input network comprising a photodiode parasitic capacitance of 40 fF in Agilent Design Systems [19]. Fig. 4.23(a)-(d) shows that the extracted output eye diagrams with 0 dBm optical input power at 40, 80, 100, and 160-Gb/s. The extracted and simulated eye diagrams at 40 Gb/s in Fig. 4.23(a) and Fig. 4.12(a), respectively, show similar eye opening as the measured eye diagram in Fig. 4.22(a). The extracted eye diagrams illustrate data rates up to 160-Gb/s at the expense of higher jitter and reduced eye height.

A comparison with similar high-speed (>100 Gb/s) circuit demonstrations is provided in Table 4.2. The presented implementation achieves the highest bandwidth reported in Silicon or Silicon-Germanium as well as the lowest gain-



(a)



(b)

Figure 4.22: Measured output eyes with a 40-Gb/s $2^{31}-1$ PRBS for (a) $330\mu A_{PP}$ input swing and (b) $1mA_{PP}$ input swing.

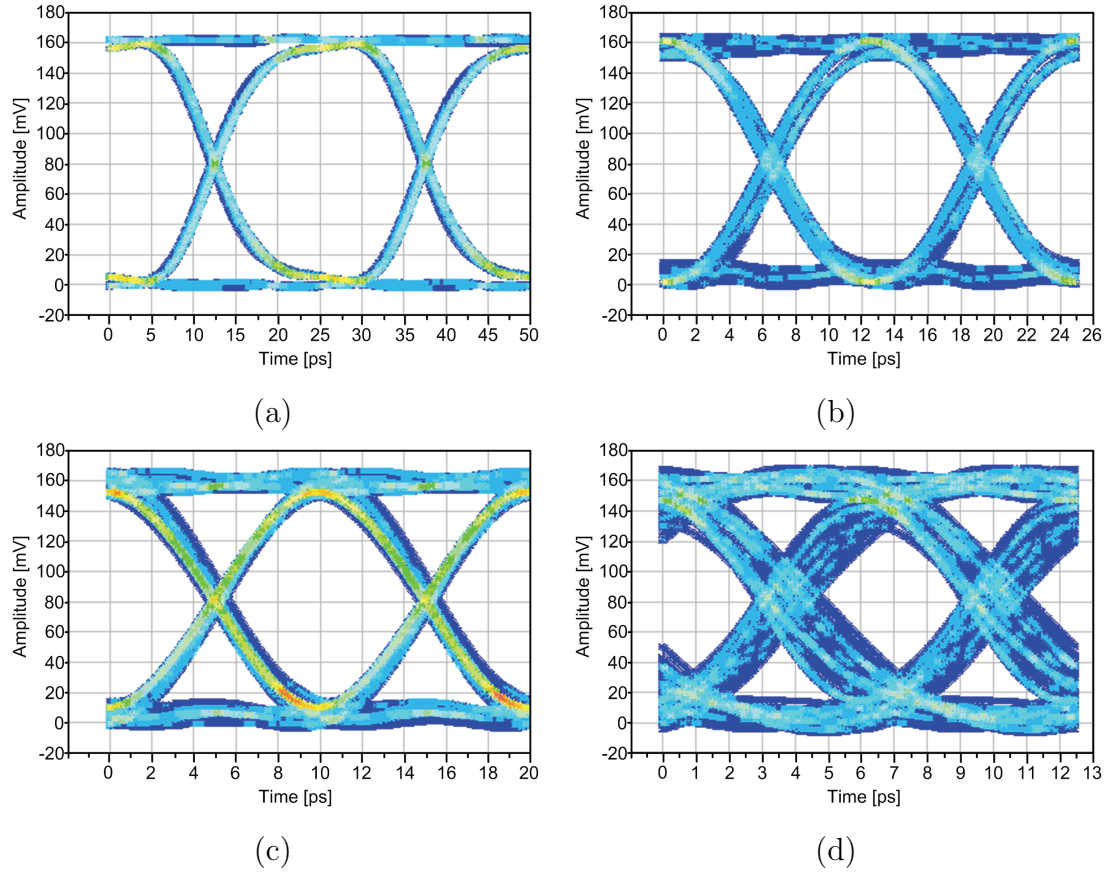


Figure 4.23: Extracted output eyes with $800\mu A_{PP}$ input swing for (a) 40-Gb/s, (b) 80-Gb/s, (c) 100-Gb/s, and (d) 160-Gb/s.

ripple, power consumption, and area. The gain-bandwidth product FOM is 4.425 GHz/mW and represents the exceptional energy efficiency when compared to recent publications in Table 4.2.

A comparison with the recent publications on 40-Gb/s TIAs is provided in Table 4.3. The presented implementation achieves the lowest group delay variation and area for this bandwidth. The transimpedance-bandwidth FOM for $I_{bias} = 3\text{ mA}$ and $I_{bias} = 0\text{ mA}$ conditions are $295.2\text{ }\Omega/pJ$ and $282.5\text{ }\Omega/pJ$ respectively. Both cases represent the exceptional figure of merit performance compared to other TIAs.

Table 4.2: Comparison to other broadband amplifiers

Ref.	Process	Gain dB	BW of S_{21} (GHz)	Gain Rip- ple(dB)	GD of S_{21} (ps)	GBW (GHz)	Supply (V)	Power (mW)	Area (mm^2)	GBW/P_{DC} (GHz/mW)
[64]	0.18 μm SiGe	14 *1	84	4	± 32	421 *1	-5.5	990	0.63	0.848 *3
[65]	SiGe $f_T=200$ GHz	13	81	> 5 *2	–	362	5.5	495	1.17	0.731
[76]	SiGe $f_T=200$ GHz	10 *1	62	> 3 *2	–	196 *1	-5	770	0.3	0.508 *3
[77]	0.12 μm SOI CMOS	11	90	2.4	–	320	2.5	210	1.28	1.524
[78]	0.13 μm CMOS	10	70.6	> 3 *2	± 12	231	1.5	79.5	0.39	2.906
[79]	90nm CMOS	7	70	> 7 **	± 10	157	–	122	0.72	1.287
[66]	90nm CMOS	7.4	80	> 3 *2	–	188	2.4	120	0.72	1.567
[67]	90nm CMOS	14	73.5	> 3 *2	± 23	369	1.2	84	1.72	4.393
This work	0.12 μm SiGe	10	102	< 2	± 6	323	2	73	0.29	4.425

*1: single-ended gain, *2: Based on S_{21} plot provided on the paper, and *3: calculated with differential gain

Table 4.3: Comparison to reported 40-Gb/s transimpedance amplifiers

Ref.	Process	Bit Rate (Gb/s)	Z_T (dB Ω)	BW of Z_T (GHz)	GD of Z_T (ps)	Supply (V)	Power (mW)	Area (mm ²)	$BW\Omega/P_{DC}$ (Ω /pJ)
[48]	HBT $f_T=160$ GHz	40	50 *1	47	–	5.2	458	0.66	64.7 *2
[53]	SiGe $f_T=200$ GHz	40	43 *1	50	–	5.2	182	0.92	77.4 *2
[55]	0.18 μ m CMOS	40	48	30	–	1.8	50.4	1.04	149.5
[13]	0.18 μ m CMOS	40	51	30.5	± 62.5	1.8	60.1	0.54	180.1
[15]	0.13 μ m CMOS	40	50	29	± 8	1.5	45.7	0.4	200.7
This work	0.12 μ m SiGe	40 (mea.) / 160 (ext.)	47 *3 / 46	53 *3 / 108	± 2.1 *3 / ± 5	2	42 *3 / 73	0.29	282.5 *3 / 295.2

*1: single-ended gain, *2: calculated with differential gain, and *3 at $I_{bias} = 0$ mA condition

4.4 92-GHz Bandwidth Distributed Main Amplifier

Fig. 4.24 shows the schematic of a three-stage distributed amplifier (DA). The NMOS gate and drain capacitances are absorbed into artificial transmission lines comprising the gate inductance and capacitance, L_g and C_g , and drain inductance and capacitance L_d and C_d that form a T -network. The characteristic impedance is approximated by $Z_o = \sqrt{L_g/C_g} = \sqrt{L_d/C_d}$. If the transmission lines are assumed lossless, the DA voltage gain is expressed as

$$G = \frac{N \cdot g_m \cdot Z_o}{2}, \quad (4.46)$$

where N is the number of stages and g_m is the transconductance of the stage, and the DA bandwidth is limited by the cutoff frequency of the transmission lines, i.e.

$$f_c = \frac{1}{\pi \sqrt{L_g C_g}} = \frac{1}{\pi \sqrt{L_d C_d}}, \quad (4.47)$$

and is independent of the N [80]. Combining (4.46) and (4.47) suggests an approximate GBW for the DA as $GBW = \frac{N}{2\pi} \frac{g_m}{C_g} \approx N f_T$. Given N , measurement of the GBW suggests the f_T of each stage. However, the quality factor of on-chip passives limits the DA GBW below the limit suggested by the NMOS [80].

4.4.1 Device Layout and Characterization

The total input capacitance of the common source NMOS, C_g , comprises the gate-source capacitance and Miller capacitance, $C_g = C_{gs} + C_{gd}(1 - A_v)$, where A_v is the small-signal voltage gain of each stage [81]. The NMOS promises extremely high f_T from transistor level simulations but the back-end-of-the-line (BEOL) gate and drain connections introduce substantial parasitic resistance and capacitance to reach the thick top metal interconnect. In this design, $Z_o \approx 50 \Omega$ and the targeted bandwidth is 100 GHz. Consequently, both the gate- and drain-line capacitance should be about 60 fF. Common source and cascode NMOS geometry is $40 \times 1\text{-}\mu\text{m}$ fingers with an effective gate length of 40 nm yields the desired capacitance

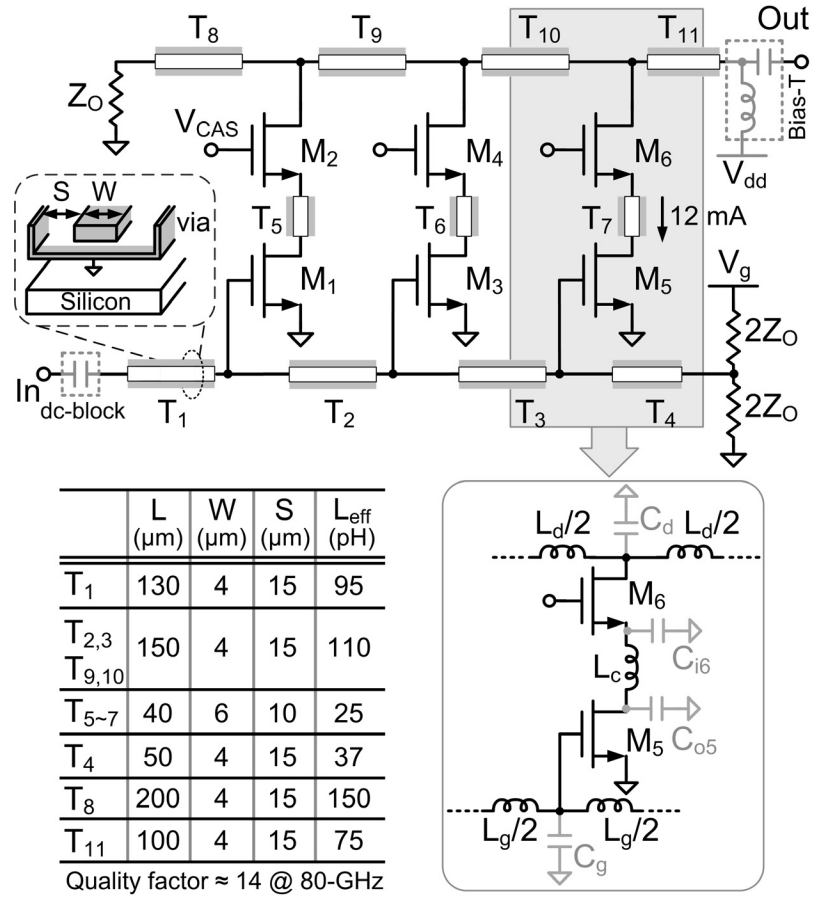


Figure 4.24: Schematic of a 3-stage cascode distributed amplifier. Note that the body of all NMOS devices is floating.

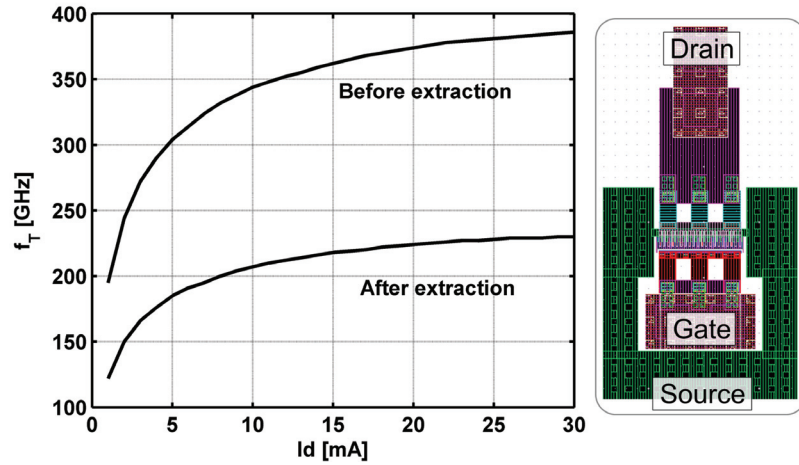


Figure 4.25: Simulated f_T for pre- and post-layout and the layout of M_1 , M_3 and M_5 .

including anticipated layout parasitics. The f_T reduction for the common source NMOS based on pre- and post-layout simulations is shown in Fig. 4.25. The peak f_T drops from 380 GHz to 230 GHz when the layout parasitics are accounted. Each cascode is biased with 12 mA to provide g_m of 48 mS for each stage.

The cascode stage reduces the input capacitance substantially since the 45-nm NMOS exhibits a relatively large $C_{gd} \approx 1/2 C_{gs}$. The cascode pole is introduced at $\omega_{cc} = g_{m,cs} / (C_{cs} + C_{cc})$ where $g_{m,cs}$ is the common source transconductance, C_{cs} is the gate-drain and drain-substrate capacitance of the common source NMOS, and C_{cc} is the gate-source and source-substrate capacitance of the cascode NMOS in Fig 4.24. The pole is pushed to higher frequencies with the series inductor L_c inserted between C_{CS} and C_{CC} . A series inductance of 25 pH extends the pole from 75 GHz to 115 GHz.

4.4.2 Interstage Inductance

Based on $C_g = 60$ fF, a characteristic impedance of $Z_o \approx 50 \Omega$ is achieved when L_g and L_d are around 110 pH ~130 pH. These inductances are realized with shielded microstrip transmission lines to isolate the signal line and prevent induced currents in the substrate ($\rho \sim 13.5 \Omega\text{-cm}$). The effective inductance is determined with the signal line width (W) and side shielding space (S). Transmission line

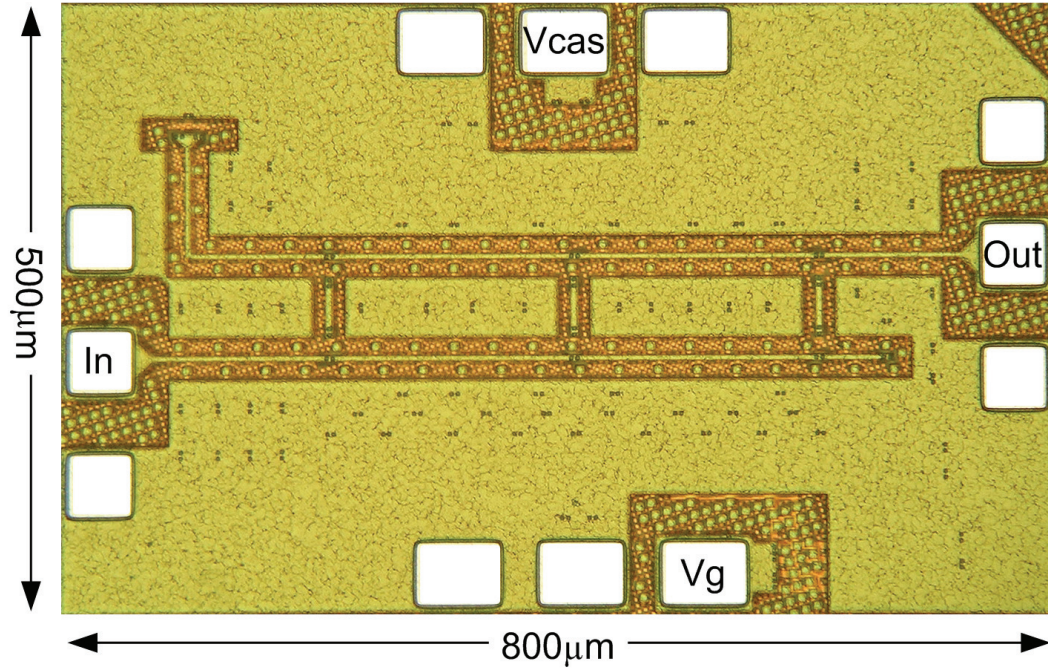


Figure 4.26: Chip microphotograph of the distributed amplifier in 45 nm SOI CMOS.

inductance and quality factor is listed in Fig. 4.24 for interstage inductance values.

The optimal number of stages in the DA is limited by the transmission lines losses. To maximize gain-bandwidth product power efficiency (GHz/mW), three-stages was found optimal based on circuit simulation. From (4.46), the predicted mid-band gain is 11 dB and bandwidth is 110 GHz.

4.4.3 Measurements

The distributed amplifier is implemented in a 45-nm SOI CMOS process and is shown in Fig. 4.26. The chip occupies an area of 0.8 mm by 0.5 mm (0.4 mm²) including pads and consumes 37 mA through the three active stages (12.3 mA per stage) and 24 mA through the 50-Ω drain termination.

S -parameters are measured on-wafer with Cascade ACP110-LW coplanar ground-signal-ground (GSG) probes and the Agilent E8361A network analyzer with the N5260A mm-wave controller. The measured S -parameters are plotted in Fig. 4.27 along with the simulated results. The amplifier has a peak gain

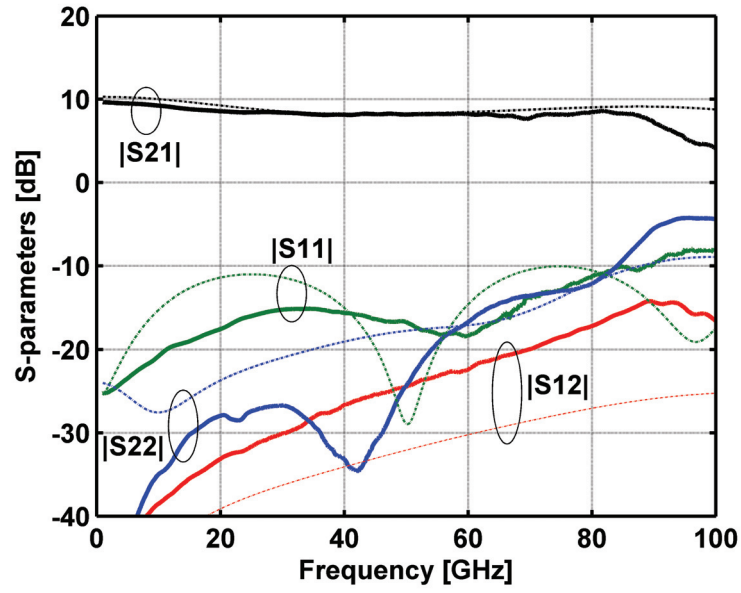


Figure 4.27: Measured (solid lines) and simulated (dotted lines) S -parameter responses.

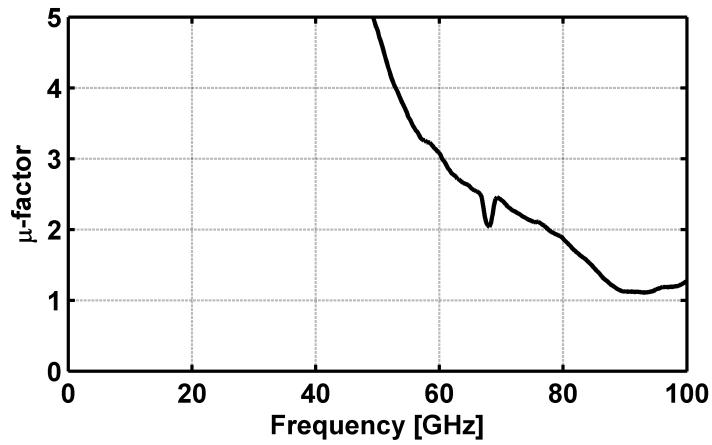


Figure 4.28: Measured stability μ -factor.

of 9 dB and a 3-dB bandwidth of 92 GHz, offering an overall gain-bandwidth product (GBW) of 259 GHz. The gain ripple is less than 1.5 dB over the 3-dB bandwidth. Circuit simulation accurately predicts the nominal gain; however, the 3-dB bandwidth is lower due to 15 fF of additional parasitic capacitance at the cascode node. The gain at 110 GHz is 4 dB indicating a unity gain frequency higher than 110 GHz. The measured μ -factor is graphed in Fig. 4.28 and indicates unconditional amplifier stability.

The measured input return loss across the entire 3-dB bandwidth is less than 10 dB, but remains below 15 dB below 70 GHz. The measured output return loss across the entire 3-dB bandwidth is less than 6 dB, but remains below 10 dB below 84 GHz. The reverse isolation is 15 dB at 88 GHz and better than 20 dB below 70 GHz.

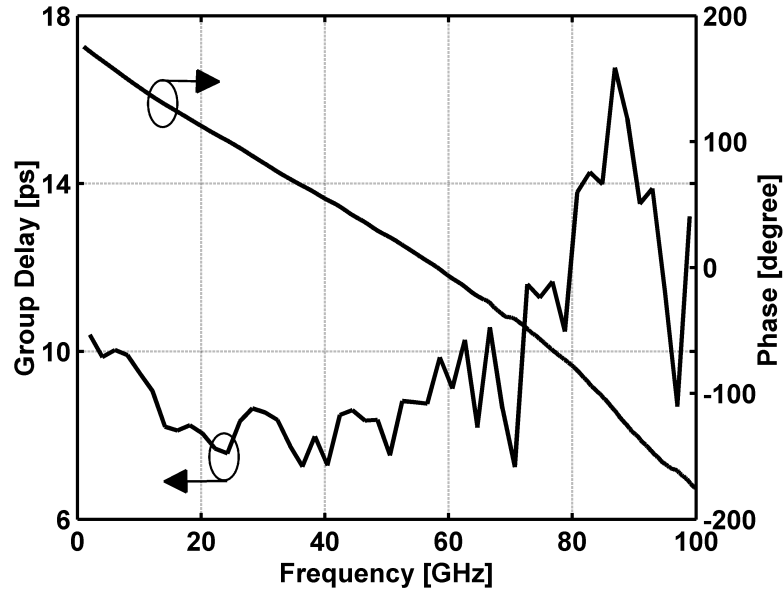


Figure 4.29: Measured group delay variation and phase of the distributed amplifier.

The phase and group delay variation (GDV) are shown in Fig. 4.29. The DA has a nominal group delay of 7.3 ps and GDV of ± 4.7 ps over the 3-dB bandwidth but only ± 2.3 ps to 80 GHz. A comparison with state-of-the-art CMOS DAs is presented in Table 4.4. The proposed implementation achieves the highest 3-dB

bandwidth, lowest gain ripple, and lowest power consumption reported in bulk or SOI CMOS processes. The GBW power efficiency figure of merit is 3.53 GHz/mW, 5.83 GHz/mW if the termination current is de-embedded, and is the best figure of merit performance compared to other technologies.

4.5 Conclusions

In this paper, a staggered broadband amplifier design is presented and demonstrated in a 10 dB gain, d.c. to 102 GHz broadband amplifier implemented in 0.12- μ m SiGe BiCMOS process. The gain features a gain ripple of 1.5 dB and group-delay variation is under ± 6 ps over the entire 3-dB bandwidth. To the authors' knowledge, this is the largest 3-dB bandwidth with low gain-ripple, group-delay variation in a Si/SiGe technology. A low-power, compact DA is also demonstrated in a 45-nm SOI CMOS process. The DA achieves a 3-dB bandwidth of 92 GHz and peak gain of 9 dB with a gain-ripple of under 1.5 dB over the 3-dB bandwidth. The group-delay variation is under ± 4.7 ps over the 3-dB bandwidth.

Acknowledgments

Chapter 4 is in part mostly a reprint of the material as it appears in IEEE Journal of Solid-State Circuits, 2011, Joohwa Kim; James F. Buckwalter, and is also in part mostly a reprint of the material as it appears in IEEE Microwave and Wireless Components Letters, 2011. Joohwa Kim; James F. Buckwalter. Additionally, chapter 4 is also in part mostly a reprint of the material as it appears in IEEE Radio Frequency Integrated Circuits Symposium, 2009, Joohwa Kim; James F. Buckwalter. This dissertation author was the primary author of these materials.

Table 4.4: Comparison to other CMOS distributed amplifiers

Ref.	Process	Gain (dB)	Ripple (dB)	BW* (GHz)	GBW** (GHz)	S11 (dB)	S22 (dB)	Supply (V)	Power (mW)	Area (mm ²)	GBW/ P_{DC} (GHz/mW)
[82]	90 nm CMOS	7	–	20–70	112	< –7	< –10	–	122	0.72	0.92
[66]	90 nm CMOS	7.4	–	5–80	176	< –10	< –8	2.4	120	0.72	1.47
[81]	130 nm SOI CMOS	7	1	1–43	94	< –8	< –6	1.8	75.6	1.5	1.24
[77]	120 nm SOI CMOS	11	2.4	5–90	302	< –5	< –7	2.5	210	1.28	1.44
[83]	120 nm SOI CMOS	4	2.4	4–91	138	< –7	< –7	2.6	91	0.8	1.52
[84]	90 nm SOI CMOS	9.7	3.2	10–59	260	< –5	< –12	2	132	0.3	1.97
This work	45 nm SOI CMOS	9	1.5	dc–92	259	< –10	< –10	1.2	73.5	0.45	3.53

*: 3-dB bandwidth and **: Gain $\times$ BW

Chapter 5

Cascaded Constructive Wave Amplification

5.1 Constructive Wave Amplification

A wideband, high-frequency amplifier technique is introduced based on traveling wave amplification at W -band. To provide high-gain and broadband-matching, the constructive wave amplification is proposed. As opposed to distributed amplifiers, the proposed CCWA amplifies forward traveling waves while attenuating backward traveling waves through a single transmission line. A CCWA topology is ideal for a direct-detection imaging applications since high-gain is achieved with comparable noise performance.

The input traveling wave is amplified as it propagates along a *single* transmission line. Several advantages are realized in this design. First, the use of a single transmission lines implies an overall area reduction for the amplifier. Second, the phase matching between the input and output lines of a conventional distributed amplifier is unnecessary. Finally, conventional distributed amplifiers have a limitation on the number of stages that can be distributed due to the inherent losses of the artificial transmission line. This prevents using more than six to eight stages in the conventional distributed amplifier.

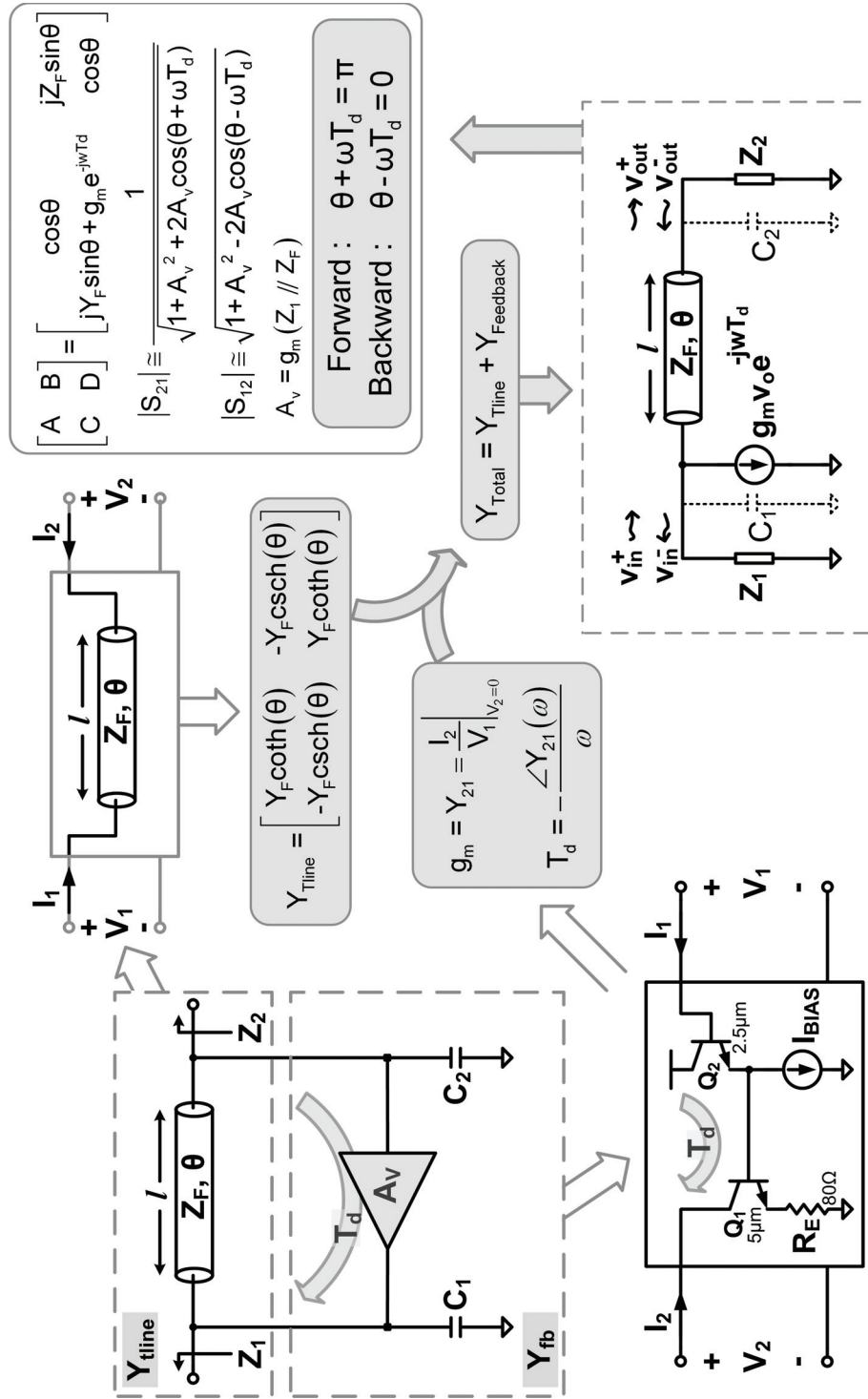


Figure 5.1: Analysis summary of CCWA using transmission line with shunt-shunt feedback

The proposed approach obviates any limitation on the number of cascaded stages since the amplifier can compensate for any losses along the transmission line. This chapter will illustrate how the appropriate feedback network unilaterally amplifies a traveling wave along a transmission line. The general concept considers an active feedback path that constructively contributes energy to the wave traveling in one direction while canceling the wave traveling in the opposite direction.

5.1.1 Traveling Wave Stage Analysis

The proposed approach consists of shunt-shunt feedback across a transmission line as illustrated in Fig. 5.1. For this shunt-shunt interconnection, Y -parameters of the transmission line and the feedback stage are analyzed separately and combined to determine the response of a single stage. The general Y -parameters for a transmission line are

$$Y_{tline} = \begin{bmatrix} Y_f \coth(\gamma l) & -Y_f \operatorname{csch}(\gamma l) \\ -Y_f \operatorname{csch}(\gamma l) & Y_f \coth(\gamma l) \end{bmatrix}, \quad (5.1)$$

where $\gamma = \alpha + j\beta$ is the propagation constant consisting the attenuation and phase constant along a transmission line of length, l , with characteristic admittance of Y_f .

A transconductor is introduced in the shunt-shunt feedback network which samples the output of the stage at port two and feedbacks current to the input of the stage at port one. The transconductor is represented as

$$Y_{fb} = \begin{bmatrix} sC_1 & g_m e^{-sT_d} \\ 0 & sC_2 \end{bmatrix}. \quad (5.2)$$

Here, the transconductance is g_m while C_1 and C_2 are the input and output capacitive loading of the feedback contributed by the transconductor. Additionally, a time delay through the feedback path is considered, T_d . This is modeled as a true time delay corresponding to some fraction of the finite transit time of the transconductor but could be alternatively considered as a frequency-dependent delay through the feedback. The response of a single stage determined from the interconnection of (5.1) and (5.2);

$$Y_{total} = Y_{tline} + Y_{fb} = \begin{bmatrix} sC_1 + Y_f \coth(\gamma l) & g_m e^{-sT_d} - Y_f \operatorname{csch}(\gamma l) \\ -Y_f \operatorname{csch}(\gamma l) & sC_2 + Y_f \coth(\gamma l) \end{bmatrix} \quad (5.3)$$

To simplify the following derivations, the transmission line will be assume lossless ($\alpha = 0$), the transmission line impedance is equal to the source and load impedance, ($Y_f = Y_o$), and the input and output capacitive loading of the feedback stage is ignored, ($C_1 = 0$ and $C_2 = 0$). These assumptions allow general observations about the mechanism of the constructive wave amplification.

5.1.2 Single Stage S -parameters

The wave transmission and reflection for a single stage are determined through conversion of the Y -parameters in (5.3) into S -parameters;

$$S = \begin{bmatrix} \frac{A_v e^{-j(\omega T_d + \theta)}}{1 + A_v e^{-j(\omega T_d + \theta)}} & \frac{e^{-j\theta} + j A_v e^{-j\omega T_d} (1 - e^{-j2\theta})}{1 + A_v e^{-j(\omega T_d + \theta)}} \\ \frac{1}{1 + A_v e^{-j(\omega T_d + \theta)}} & \frac{A_v e^{-j(\omega T_d + \theta)}}{1 + A_v e^{-j(\omega T_d + \theta)}} \end{bmatrix}, \quad (5.4)$$

where a feedback voltage gain is defined as $A_v = g_m Z_o / 2$. The magnitude of each of these element in the matrix is

$$\begin{aligned} |S_{11}| &= \frac{A_v}{\sqrt{1 + A_v^2 + 2A_v \cos(\theta + \omega T_d)}} \\ |S_{21}| &= \frac{1}{\sqrt{1 + A_v^2 + 2A_v \cos(\theta + \omega T_d)}} \\ |S_{12}| &= \frac{\sqrt{1 + 4A_v^2 \sin^2(\theta) - 4A_v \sin(\theta) \sin(\omega T_d)}}{\sqrt{1 + A_v^2 + 2A_v \cos(\theta + \omega T_d)}} \\ |S_{22}| &= \frac{A_v}{\sqrt{1 + A_v^2 + 2A_v \cos(\theta + \omega T_d)}} \end{aligned} \quad (5.5)$$

From this first-order analysis, the S -parameters depend on the voltage gain through the shunt feedback as well as the phase through the transmission line, θ , and delay through the feedback path, T_d . Constructive interference of the forward traveling wave and destructive interference of the backward traveling wave occur when

$$\theta + \omega T_d = \pi \quad \theta - \omega T_d = 0. \quad (5.6)$$

In other words, the phase through the transmission line and the feedback path should be 90° at the amplifier center frequency. Under this phase condition, the scattering matrix reduces to

$$S = \begin{bmatrix} \frac{A_v}{1 - A_v} & \frac{1 - 2A_v}{1 - A_v} \\ \frac{1}{1 - A_v} & \frac{A_v}{1 - A_v} \end{bmatrix}. \quad (5.7)$$

The backward transmission, S_{12} , is cancelled completely if $A_v = 1/2$ while the forward transmission, S_{21} , is 2. Hence, the forward wave is amplified while providing isolation of the backward traveling wave. The phase conditions in (5.6) and resulting S -parameters in (5.7) indicate that the stage amplifies through positive feedback of the wave from the output to the input of the stage. However, the input and output return loss, S_{11} and S_{22} are equal to 1 for $A_v = 1/2$ but are reduced for smaller values of A_v . In the limit that the feedback voltage gain approaches zero, the response in (5.7) resembles an ideal lossless transmission line.

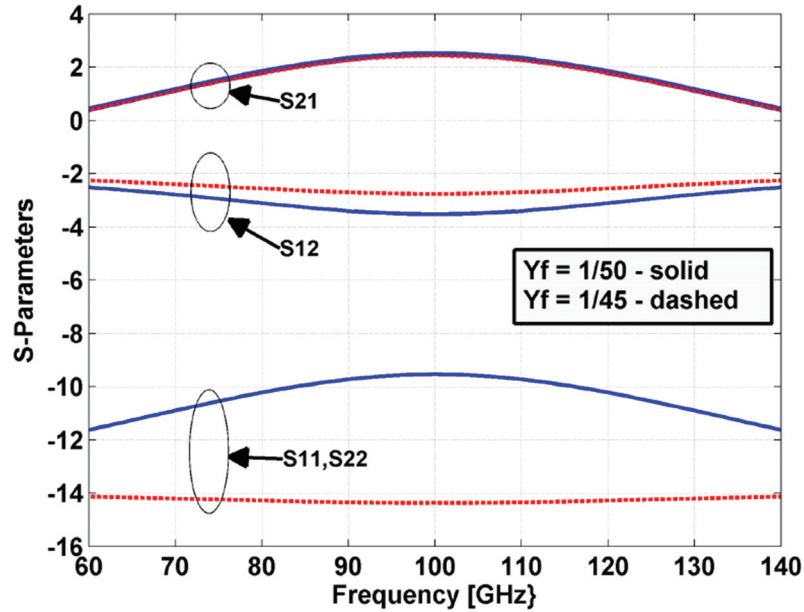


Figure 5.2: Analytical single stage S -parameters with $g_m = 10 \text{ mS}$, $\theta = \pi/2$, and $T_d = 2.5 \text{ ps}$

The S -parameters are plotted in Fig. 5.2 for $g_m = 10 \text{ mS}$ or an effective voltage feedback gain of $1/4$ under two different transmission line impedances to

offer acceptable input and output return loss conditions and ensuring stability. The first condition is $Z_f = 50\Omega$ based on our initial assumptions. The forward transmission reaches a maximum of 2.2 dB at the center frequency of 100 GHz while the backward transmission reaches a minimum of -4 dB. With no capacitive loading the input and output return loss is identical, *i.e.* $S_{11} = S_{22}$, and increases to around -9.5 dB. To explore the subjectivity of the initial assumptions, the S -parameters are also determined for $Z_f = 45\Omega$. Notably, S_{21} does not change appreciably while S_{12} increases to -2.5 dB. However, the primary benefit of reducing the transmission line characteristic impedance is a reduction of S_{11} and S_{22} to -14 dB across the entire frequency range. Notably, the constructive wave amplification results in broadband matching of the stage. This is a benefit that is not common in traditional cascaded lumped element amplifier designs.

5.1.3 Input and Output Matching

A notable feature of the constructive wave stage is the broadband matching as shown in Fig. 5.2. The input and output admittances are determined from (5.3);

$$\begin{aligned} Y_{in} &= Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22}+Y_o} = Y_o \left(1 + 2A_v e^{-j(\omega T_d + \theta)} \right) \\ Y_{out} &= Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11}+Y_o} = Y_o \left(1 + 2A_v e^{-j(\omega T_d + \theta)} \right) \end{aligned} \quad (5.8)$$

The input and output impedances are identical in the extent that the impedance at the input and output is identical. Both the input and output admittance trace a circle of radius $1 + 2A_v$ around the ideal matching condition. As might be anticipated, the matching is improved by reducing the voltage feedback gain.

5.2 Cascaded Constructive Wave Amplification

The chain matrix representation of the stage presented in Section 5.1 is employed to study the interaction of a cascade of uniform stages. Converting (5.3) into a chain matrix under the simplifying assumptions of Section 5.1.1, each stage contributes

$$T_{stage} = \begin{bmatrix} \cosh(\gamma l) & Z_f \sinh(\gamma l) \\ \frac{1}{Z_f} \sinh(\gamma l) + g_m e^{-j\omega T_d} & \cosh(\gamma l) \end{bmatrix}. \quad (5.9)$$

The chain matrix determines the important features of the cascaded constructive traveling wave stages to amplify the forward traveling wave and isolate the backward traveling wave over multiple stages.

5.2.1 Cascaded Gain

The cascade of N traveling wave stages is determined from the chain matrix multiplication.

$$T_{amp} = T_{stage}^N \quad (5.10)$$

Unfortunately, straightforward substitution of (5.5) into (5.10) does not provide simple analytical results but is manageable numerically. For simplicity, the interaction of the stages under the condition $\theta = \omega T_d = \pi/4$ is

$$T^N = \begin{cases} \begin{bmatrix} 0 & jZ_o(2A_v - 1)^{(N-1)/2} \\ \frac{j}{Z_o}(1 - 2A_v)^{(N+1)/2} & 0 \end{bmatrix} & \text{if } N \text{ odd} \\ \begin{bmatrix} (2A_v - 1)^{N/2} & 0 \\ 0 & (2A_v - 1)^{N/2} \end{bmatrix} & \text{if } N \text{ even} \end{cases} \quad (5.11)$$

Therefore, the resulting cascaded gain in the forward direction is

$$|S_{21}| = \begin{cases} \frac{1}{(1-A_v)(1-2A_v)^{(N-1)/2}} & \text{if } N \text{ odd} \\ \frac{1}{(1-2A_v)^{N/2}} & \text{if } N \text{ even} \end{cases} \quad (5.12)$$

From the earlier condition on the feedback voltage gain in (5.5), the cascade illustrates that $A_v < 1/2$ is necessary for stability. The forward transmission gain depends on whether the number of stages is even or odd and generally it can be found that an even number of stages produces slightly higher overall gain. Fig. 5.3 shows that the analytical results of cascaded stage S -parameters for $N=1$ and

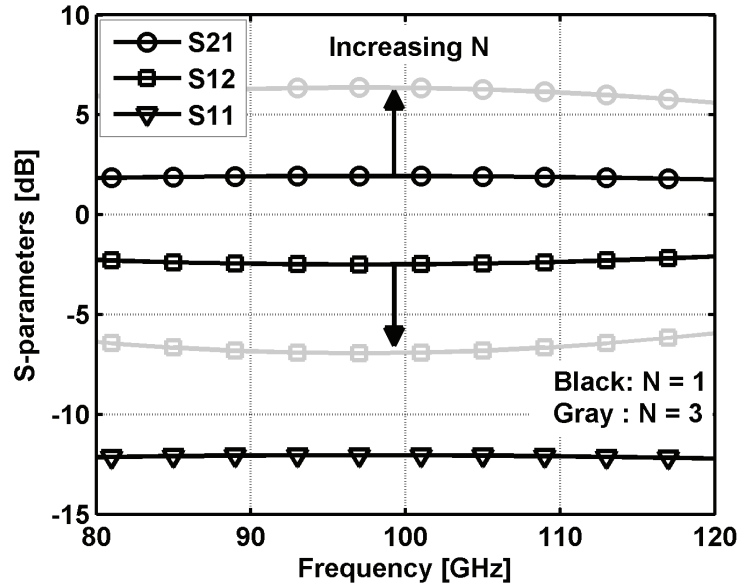


Figure 5.3: Analytical cascaded stage S -parameters for $N=1$ and $N=3$

$N=3$, where N is the number of stage. As the number of stage increases, the forward gain (S_{21}) is increased while the backward wave (S_{12}) is isolated. The matching performance (S_{11}) remains below -10 dB for both $N=1$ and $N=3$.

5.3 SiGe Circuit Design

The shunt-shunt active feedback is implemented with HBT devices in a $0.12\text{-}\mu\text{m}$ SiGe BiCMOS technology and consists of an emitter follower followed by a common emitter amplifier with resistive emitter degeneration as illustrated in Fig. 5.1. As has been determined from the analysis, the feedback circuit should be designed to provide high input and output impedance to prevent loading of the transmission line. An HBT implementation offers high impedance and high transconductance with f_T of 200 GHz and f_{max} of 280 GHz. Consequently, the feedback amplifier can satisfy the desired delay requirements through the feedback path.

5.3.1 Small Signal Transconductance

For the active feedback, the small-signal equivalent circuit in Fig. 5.4 is used to determine Y -parameters Y_{Act} and Y_{21} can be found as

$$Y_{21Act} = \frac{g_{m1}g_{m2}}{(1 + g_{m2}R_E)g_{m1} + t_1s + \dots} \quad (5.13)$$

where

$$\begin{aligned} t_1 = & (1 + g_{m2}R_E)C_{be1} + (1 + g_{m2}R_E)g_{m1}r_{b1}C_{bc1} \\ & + (1 + g_{m1}r_{b2} + g_{m1}R_E)C_{be2} \\ & + (1 + g_{m2}R_E + g_{m1}r_{b2} + g_{m1}g_{m2}r_{b2}R_E)C_{bc2}. \end{aligned}$$

In (5.13), the input resistance, r_π , and the output resistance, r_o , for both Q_1 and Q_2 is assumed to be infinite for simplifying equation. From (5.13), the current bias condition, I_{bias} , of the emitter follower provides a convenient method to adjust the feedback gain and the transconductance, $g_{mAct}|_{mb}$, at mid-ban frequency is determined as

$$g_{mAct}|_{mb} = \frac{g_{m2}}{1 + g_{m2}R_E}. \quad (5.14)$$

The time delay, T_d , through the active feedback is also found from (5.13) and is about 2 ps at 100GHz. The active feedback is assumed to be unilateral in this analysis ($Y_{12Act} = 0$) and the input impedance at low frequency is determined by $1/Y_{B,11}$

$$\begin{aligned} r_{iAct}|_{mb} = & r_{b1} + r_{\pi1} + (1 + g_{m1}r_{\pi1})(r_{b2} + r_{\pi2}) \\ & + (1 + g_{m1}r_{\pi1})(1 + g_{m2}r_{\pi2})R_E. \end{aligned} \quad (5.15)$$

Clearly, the feedback gain is chosen by degeneration through R_E . In this design, Q_1 is biased for g_m of 60mS while R_E is 70 Ω .

5.3.2 Input and Output Impedance

Maintaining high impedance at the input and output of the active feedback stage is critical to reducing loading on the transmission line. The input impedance at the bast of the common emitter stage is

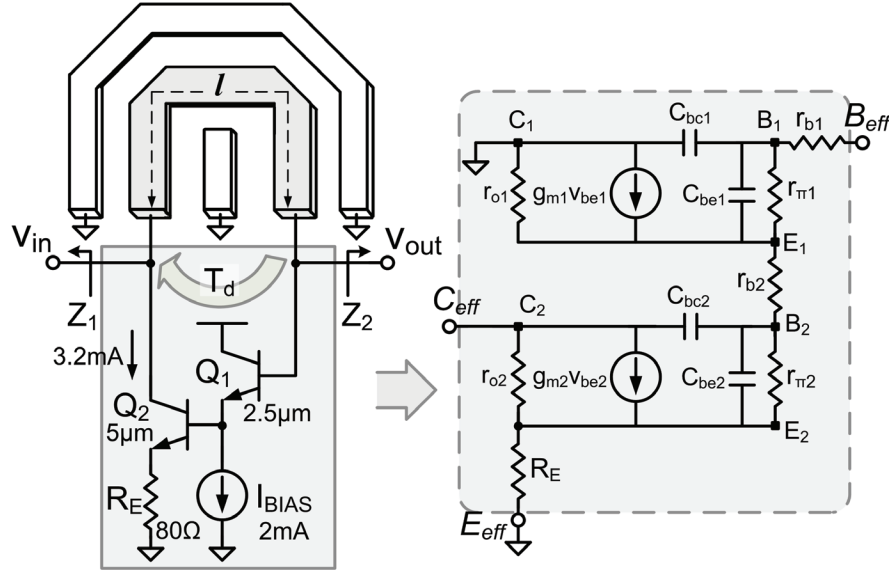


Figure 5.4: SiGe HBT implementation of active feedback

$$Z_{in,1} = r_{b1} + \frac{(1 + sC_{bc,1}\frac{Z_o}{2})(1 + sC'_{be,1}R_E)}{s(C'_{be,1} + C_{bc,1}(1 + g'_{m,1}\frac{Z_o}{2})) + s^2C_{bc,1}C'_{be,1}(R_E + \frac{Z_o}{2})}, \quad (5.16)$$

where $C'_{be,1} = C_{be,1}/(1 + g_m R_E)$ and $Z_o/2$ is estimated as the impedance at the collector of the transistor. Similarly, the impedance at base of the emitter follower stage is

$$Z_{in,2} = r_{b2} + \frac{1}{sC_{be,2}} + Z_{in,1}(1 + \frac{g_{m,2}}{sC_{be,2}}). \quad (5.17)$$

Substituting (5.16) into (5.17), the total feedback input impedance at output port of the amplifier stage is

$$Z_{in,2} \approx r_{b1} + r_{b2} + R_E \left(1 + \frac{g_{m,1}g_{m,2}}{s^2C_{be,1}C_{be,2}} + \frac{g_{m,1}}{sC_{be,1}} + \frac{g_{m,2}}{sC_{be,2}} \right) + \frac{1}{sC_{bc,2}}. \quad (5.18)$$

The impedance consists of resistive and capacitive components. The capacitance at the emitter of the emitter follower stage contributes to negative resistance at the input impedance port. However, the input resistance remains positive because of the relatively high base resistance.

The output impedance of the feedback stage is

$$Z_{out} = (1 + g_{m,1}r_{o,1}) R_E + \frac{1}{sC_{bc,1}}. \quad (5.19)$$

The output impedance has a relatively large output resistance because of the emitter degeneration and the capacitance seen at this node is limited to the base-collector capacitance of the common emitter transistor.

5.3.3 Non-uniform CCWA Implementation

As opposed to the approach in the first version of CCWA [69], the implementation of the CCWA in this chapter is non-uniform and the current consumption of each stage is significantly lowered. The schematic of the CCWA is shown in Fig. 5.5 and comprises fourteen cascaded amplifier stages.

Each stage is represented by the small-signal circuit model in Fig. 5.5. The non-uniform design considers this gain-matching trade-off. The design of the stages is split between matching at the first and last stage of the amplifier while providing gain in the middle amplifier stages. An A_v of 0.11 ($|S_{21}| = 1$ dB) provides input and output return loss of better than 18 dB while A_v of 0.23 ($|S_{21}| = 2.3$ dB) provides return loss better than 10 dB. At the first and last stages, g_m is reduced to improve the matching characteristics. The feedback gain is controlled with emitter resistance R_E and reduces the transconductance, e.g. $g_m \approx g_{m,Q2}/(1 + g_{m,Q2}R_E)$. The current bias is $I_c = 0.6$ mA at the first and last stage and a large emitter resistance is included to degenerate the device. The transmission line length is 230 μm which is shorter than the theoretical quarter-wave transmission line because of the capacitive loading of the active circuit.

In the middle amplifier stages, the ratio of gain to the d.c. power consumption can be improved substantially with respect to [69]. Since the transconductance is related to the collector current and thermal voltage, i.e. $g_m \simeq I_c/V_T$, the gain-to-power ratio can be expressed in terms of the feedback voltage gain,

$$\frac{|S_{21}|}{P_{dc}} = \frac{1}{2V_{cc}V_T} \cdot \frac{Z_o}{A_v(1 - A_v)} \left(1 - 2A_v \frac{R_E}{Z_o} \right). \quad (5.20)$$

Since A_v is fixed, smaller R_E improves this ratio by requiring less transconductance.

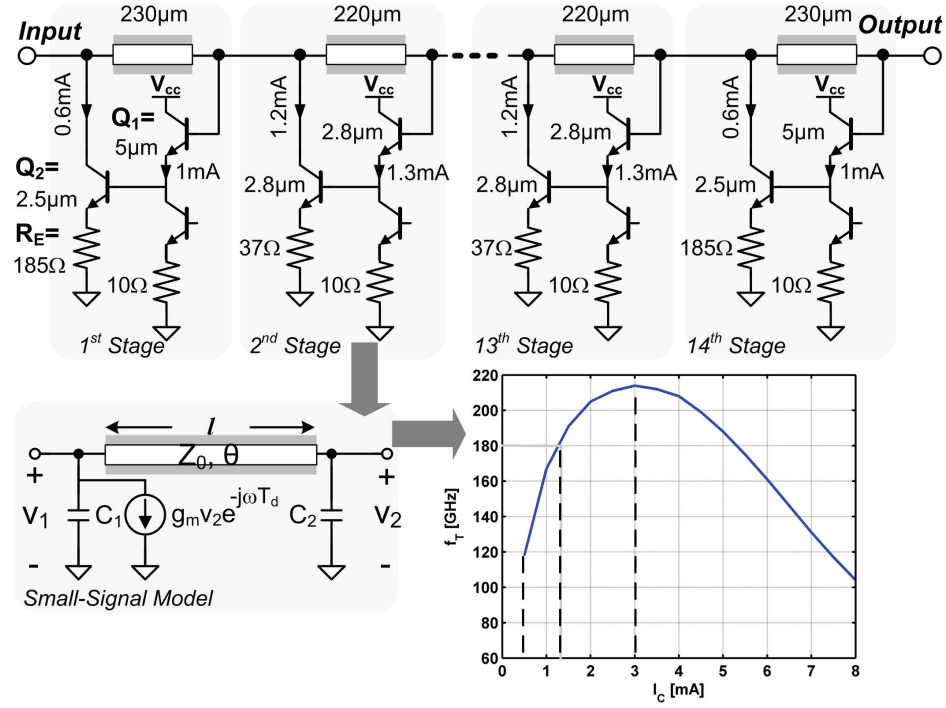


Figure 5.5: Schematic of 14-stage CCWA with small-signal model and f_T versus collector current for $L_e = 2.8 \mu m$.

In the limit that $R_E \rightarrow 0$, g_m should be around 10 mS and suggests a relatively small HBT for peak f_T ($W_E = 0.4 \mu m$). However, this device has process variations of around 50%. Robustness to process, voltage, and temperature variations are improved by re-introducing the negative feedback through R_E at the expense of the ratio in (5.20). The sensitivity to transconductance variations can be expressed as

$$\frac{\partial A_v}{\partial g_m} = \frac{Z_o}{2} \left(1 - 2A_v \frac{R_E}{Z_o} \right)^2. \quad (5.21)$$

For a 50% reduction in the sensitivity of the gain to the g_m variations, $R_E = 30 \Omega$. From (5.20), this degeneration degrades the gain-to-power ratio by 30%. Mismatch is also reduced by 25% when the emitter length is $L_e = 2.8 \mu m$. In this work, R_E is 37Ω for the common emitter HBT. Each HBT is nominally biased at 1.2 mA for f_T of 180 GHz. To compensate for the higher capacitance in the middle stages, the transmission line length is decreased to $220 \mu m$.

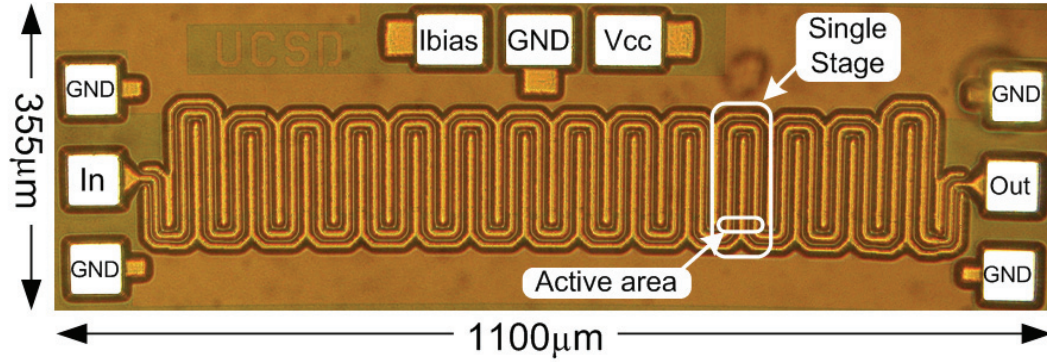


Figure 5.6: Chip microphotograph of the W -band amplifier in $0.12\text{-}\mu\text{m}$ SiGe BiCMOS.

5.4 Measurements

The chip microphotograph is shown in Fig. 5.6. The implemented chip occupies an area of 1.1 mm by 0.36 mm including the pads.

On-wafer probing with Cascade ACP110-LW coplanar ground-signal-ground (GSG) probes is used to measure the S -parameters with the Agilent E8361A two-port network analyzer and N5260A mm-wave controller. The measured S -parameters at the nominal bias conditions are shown in Fig. 5.7. The gain has a 3-dB bandwidth of 17.5 GHz between $80.8\text{--}98.3\text{ GHz}$. The measured gain is compared to circuit simulation over fourteen stages and demonstrates accurate prediction of the nominal gain and bandwidth. At the nominal bias, the GBW is 553 GHz . The measured input and output return losses are better than 11 dB and match the simulated results. Measured reverse isolation is 35 dB at 80 GHz and better than 40 dB above 88 GHz . Fig. 5.7 shows that the simulated noise figure is as low as 10.8 dB at 83 GHz and increases to 12.1 dB at 98 GHz . The gain compression is recorded in Fig. 5.8 under the nominal biasing conditions using an Agilent E4419B power meter with a W8486A power sensor. The measured output-referred 1-dB gain compression point for the amplifier is -5.5 dBm .

Higher bias conditions maximize the GBW of the amplifier in Fig. 5.9 subject to unconditional stability. The amplifier has a 3-dB bandwidth of 14.6 GHz between $84.1\text{--}98.7\text{ GHz}$ and a peak gain of 37.5 dB at 87 GHz with the gain ripple of less than 2 dB . The GBW of the amplifier is $1,095\text{ GHz}$. The

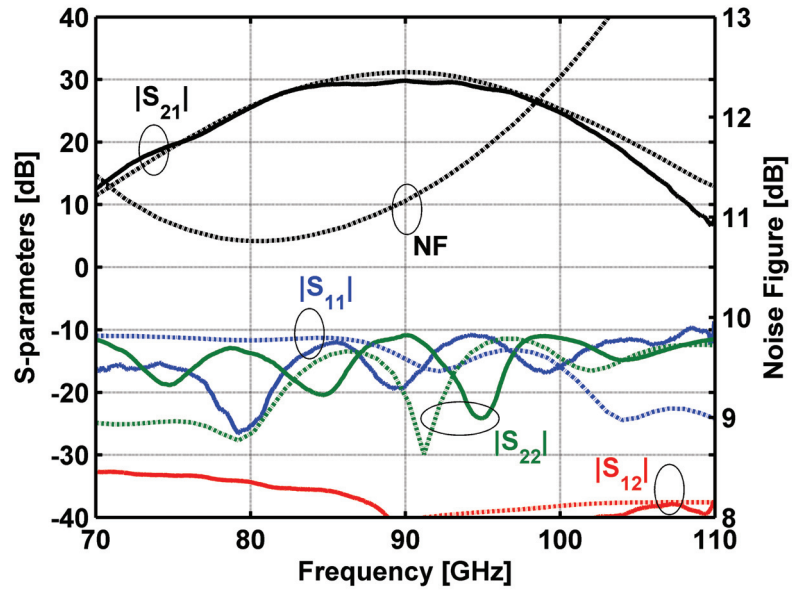


Figure 5.7: Measured (solid lines) and simulated (dotted lines) S -parameters and noise figure for a nominal bias condition (V_{cc} , $V_{bias} = 1.8$ V and $I_{bias} = 1.6$ mA).

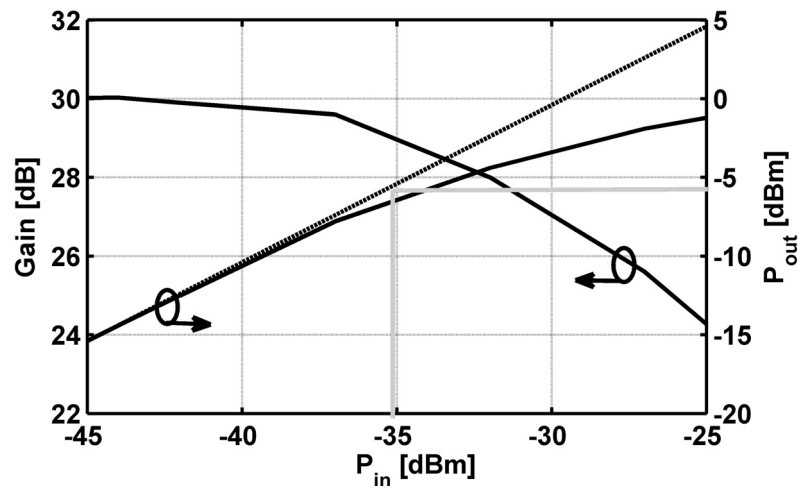


Figure 5.8: Measured gain compression of 14-stage amplifier.

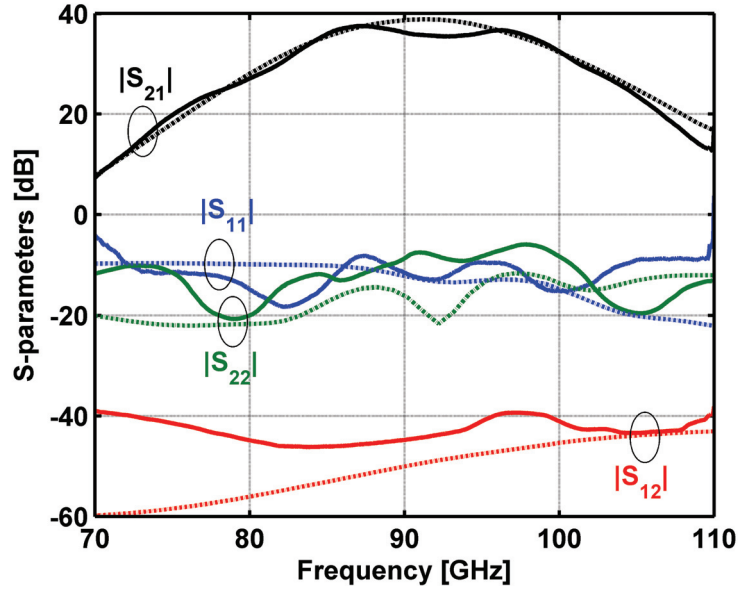


Figure 5.9: Measured (solid lines) and simulated (dotted lines) S -parameters for a high gain bias condition (V_{cc} , $V_{bias} = 2$ V and $I_{bias} = 1.4$ mA).

measured input return loss across the entire 3-dB bandwidth is better than 8.3 dB and remains below 10 dB over the most of the frequency range. The measured input return loss is 7.5 dB at 91 GHz and better than 10 dB below 89 GHz. The measured reverse isolation is at most 46 dB and decreases to 39.5 dB at 98 GHz. The amplifier noise figure increases to 12.4 dB.

The stability is illustrated in Fig. 5.10. At the nominal bias, μ -factor is greater than one, indicating unconditional stability for the amplifier. At the high bias, the minimum μ -factor is 0.98 at 97.5 GHz and the amplifier is entering a conditionally stable regime.

The GBW doubles between the two biases and induces a proportional increase in the power consumption. The chip consumes 65 mW from the 1.8-V supply and 130 mW from the 2-V supply. The power consumption has been reduced by around 40% from previous work and is unconditionally stable at higher values of gain [69]. A comparison with state-of-the-art W -band amplifiers is provided in Table 5.1. The proposed implementation achieves the highest gain and gain-bandwidth product reported in silicon or silicon-germanium. The GBW effi-

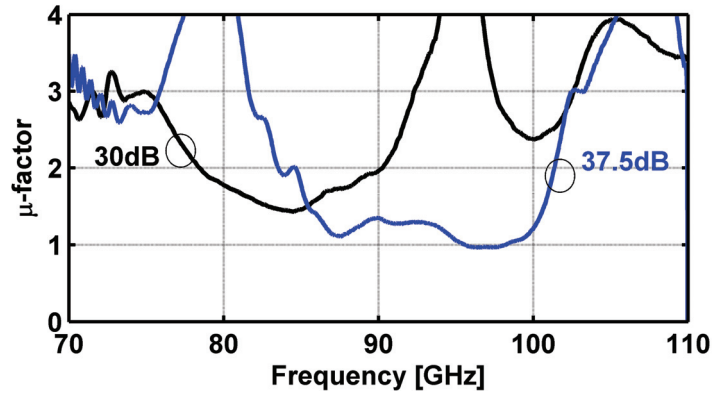


Figure 5.10: Measured stability factor.

ciency figure of merit (FOM) is 8.51 GHz/mW for the nominal biasing conditions and 8.43 GHz/mW for the high biasing conditions.

5.5 Conclusion

A wideband, millimeter wave amplifier topology is presented based on constructive wave amplification. An analysis of the cascaded constructive wave amplification is presented and theoretical gain, matching, group delay and noise figure is studied and compared with circuit simulation and measured results. A fourteen-stage cascaded constructive wave amplifier is demonstrated in a 0.12- μm SiGe BiCMOS process with a gain-bandwidth product exceeding 1 THz. To the author's knowledge, this represents a record for an amplifier demonstrated in silicon/silicon-germanium processes. A maximum 37.5-dB gain over a bandwidth of 14.6 GHz is demonstrated with a total power consumption of 130 mW.

Acknowledgments

Chapter 5, is in part mostly a reprint of the material as it appears in IEEE Microwave and Wireless Components Letters, 2011, J. Kim; J. F. Buckwalter. The dissertation author was the primary author of these materials. In chapter 5,

some figures are similar or same to the figures in the paper IEEE Transactions on Microwave Theory and Techniques, 2009, J. F. Buckwalter; J. Kim. I thank Professor James Buckwalter for providing me with the material.

Table 5.1.1: Comparison to other W-band amplifiers

Ref.	Process	Gain (dB)	BW (GHz)	GBW (GHz)	S11 (dB)	S22 (dB)	NF (dB)	OP1dB (dBm)	Supply (V)	Power (mW)	GBW/P_{DC} (GHz/mW)
[29]	65nm CMOS	13	21	94	< -6	< -10	7.5	6	1.2	86	1.09
[85]	90nm CMOS	17	22	155	< -7	< -3	-	2	2.5	54	2.87
[32]	90nm CMOS	9.4	2	17	< -9.5	< -5	-	-	1	22	0.77
[30, 86]	0.12 μ m SiGe	23	17	240	< -5	< -8	8-10	-3	1.2	28	8.57
[69]	0.12 μ m SiGe	26	13	260	< -15	< -12	10.8	0	2.2	113	2.3
[69]	0.12 μ m SiGe	35	13	740	< -7	< -4.5	13	0	2.2	181	4
This work	0.12 μ m SiGe	30	17.5	553	< -11	< -11	10.8 *	-5.5	1.8	65	8.51
This work	0.12 μ m SiGe	37.5	14.6	1,096	< -8.3	< -7.5	12.4 *	-5 *	2	130	8.43

*: simulation

Chapter 6

Switchless Bidirectional Transceiver Architectures

6.1 System Considerations Based on Switched Amplifiers

Fig. 6.1 shows that the block diagram of the traditional half-duplex transceiver and the proposed bidirectional transceiver. To reduce the number of off-chip interconnects required for the transmitter and receiver, the antenna is shared by the transmitter and receiver with a switch that isolates the transmit and receiver paths. However, a single-pole double-throw (SPDT) switch introduces intrinsic limitations for this traditional architecture. First, the switch has high insertion loss at mm-wave frequencies. The performance of the state-of-the-art SPDT switches are summarized in Table 6.1. Typical value of the insertion loss is about 2 dB to 5 dB above Q-band. This insertion loss reduces the front-end sensitivity; the receiver noise factor using SPDT switches is expressed as

$$F_{eq} = L_{sw1} + L_{sw1} (F_{LNA} - 1) + \frac{L_{sw1} (L_{sw2} - 1)}{G_{LNA}} + \dots \quad (6.1)$$

where L_{sw1} and L_{sw2} are the insertion losses of the switches before and after the LNA, F_{LNA} is the noise factor of LNA, and G_{LNA} is the gain of LNA. For example, if the LNA has a noise figure of 3 dB and each switch has an insertion loss of 3

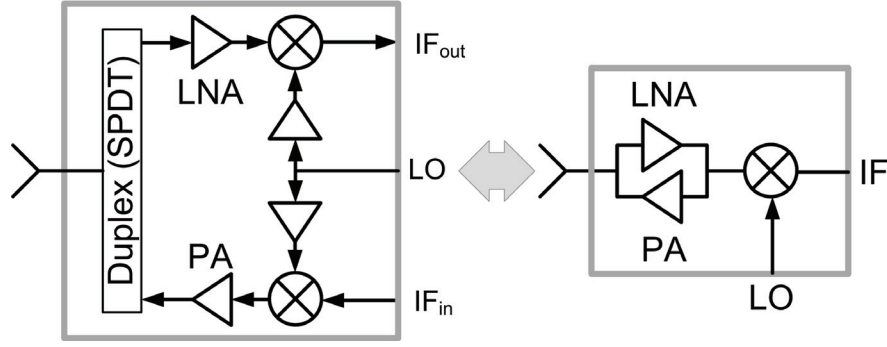


Figure 6.1: Architecture of a conventional half-duplex front-end and bidirectional front-end

Table 6.1: Performance Summary of the state-of-the-art SPDT switches

Ref.	Process (CMOS)	Frequency (GHz)	Loss (dB)	Isolation (dB)	P1dB (dBm)
[87]	90 nm	50	3.4	13.7	14
[88]	65 nm	70–94	4.2	25	–
[89]	90 nm	50–94	2.7	27	15
[90]	130 nm	45–70	2	30	13
[91]	130 nm	57–60	4.5	24.1	4.1
[92]	45 nm	50–94	5	20.5	11

dB, the total receive noise figure must be greater than 6 dB.

Additionally, the insertion loss between the PA and antenna reduces the output power of PA. The power-added efficiency (PAE) of a traditional transmitter using SDPT switches in Fig. 6.1 is

$$PAE_{eq} = \frac{P_{out}}{L_{sw1}P_{dc}} \cdot \left(1 - \frac{L_{sw2}}{G_{PA}}\right) \quad (6.2)$$

where G_{PA} is the gain of PA. For instance, if the PA has 20 dB of gain at $P_{out} = 10$ dBm and consumes 65 mW, then the total PAE is 15.23%. Once the switch loss of 3 dB is incorporated, the total PAE drops to 7.5 %. Additionally, the FET-based switches have a limited P1dB, typically between 11 dBm and 15 dBm in Table 6.1. Consequently, the switch may limit power handling.

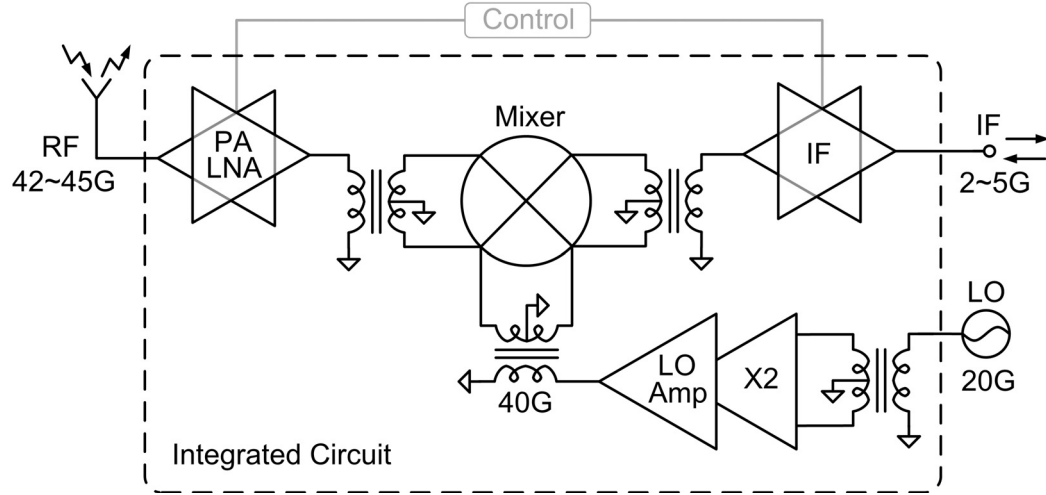


Figure 6.2: Architecture of the Q -band bidirectional transceiver.

6.2 A Fully Integrated Switchless Q -band (45-GHz) Bidirectional Transceiver

A switchless Q -band bidirectional front-end is introduced as shown in Fig 6.2. The bidirectional transceiver is a three-port network that is biased to amplify from the RF to IF port in the receive mode or from IF to RF port in the transmit mode. The third port is provided for the LO signal. The transceiver is consisting of five main blocks. The first stage is the PALNA (Power amplifier and low noise amplifier) which eliminates the need for transmit and receive switches. The second block is a double-balanced resistive mixer for bidirectional frequency conversion. The next stage is a IF bidirectional amplifier which compensates the conversion loss of the mixer. Finally, the frequency doubler and LO amplifier generate a 40-GHz LO signal from the 20-GHz input carrier. The PALNA design imposes circuit and system design constraints which are explored in this section.

6.2.1 Power Amplifier/Low Noise Amplifier (PALNA)

To eliminate the need for a T/R switch, the output of the power amplifier and input of the low noise amplifier are connected through an isolation network

shown in Fig. 6.3. To operate in transmit or receive mode, the base biasing is adjusted for the PA or LNA transistors to make one of these amplifiers active. As will be shown here, the properties of the isolation network change when the LNA bias is switched from an on (or active) state to an off (or cutoff) state. The impedance seen from both sides of the isolation network is determined by the transistor parameters for the LNA device (Q1), C_{b1} and r_{b1} , and the PA device (Q2), C_{c2} and r_{o2} . First, we investigate the small-signal behavior of the PALNA.

Receive Mode

In receive mode, the LNA is active and the PA is off. The bias of the Q1 is set for minimum noise. Ideally, the base resistance, r_{b1} , and the capacitance, C_{b1} , are used for matching to port one. The impedance seen looking into the input of the LNA is $Z_1 = \frac{1}{sC_{b1}} + r_{b1}$, where $C_{b1} = C_{be1} + C_{\mu1}$ is the combination of the base-emitter capacitance and the Miller capacitance which exaggerates the base-collector capacitance. The impedance looking from port one into the PALNA is

$$Z_A = \frac{1}{sL_1} \parallel Z_1 \parallel Z_B \approx \frac{1}{sL_1} \parallel Z_1. \quad (6.3)$$

The inductor is used to provide noise matching of the LNA at 44 GHz. The isolation network should keep Z_B from loading the input matching circuit.

In receive mode, the output resistance, r_o , of the PA is large allowing it to be ignored since the current bias on the common-emitter device is zero and only the collector capacitance, C_{c2} , loads the transmission line. Since the PA collector remains biased to the voltage supply, the collector-base junction remains reverse-biased. The isolation network is constructed with the transmission lines, T_1 and T_2 , each of lengths l_1 and l_2 and characteristic impedances Z_{o1} and Z_{o2} . The impedance seen looking into the isolation network is

$$\begin{aligned} Z_B &= Z_{o1} \frac{\frac{1}{sC_{c2}} \parallel jZ_{o2} \tan(\beta l_2) + jZ_{o1} \tan(\beta l_1)}{Z_{o1} + j \tan(\beta l_1) \left(\frac{1}{sC_{c2}} \parallel jZ_{o2} \tan(\beta l_2) \right)}, \\ &= jZ_o \frac{\tan(\beta l_1) + \tan(\beta l_2)(1 - \omega C_{c2} Z_o \tan(\beta l_1))}{1 - \tan(\beta l_2)(\tan(\beta l_1) + \omega C_{c2} Z_o)} \end{aligned} \quad (6.4)$$

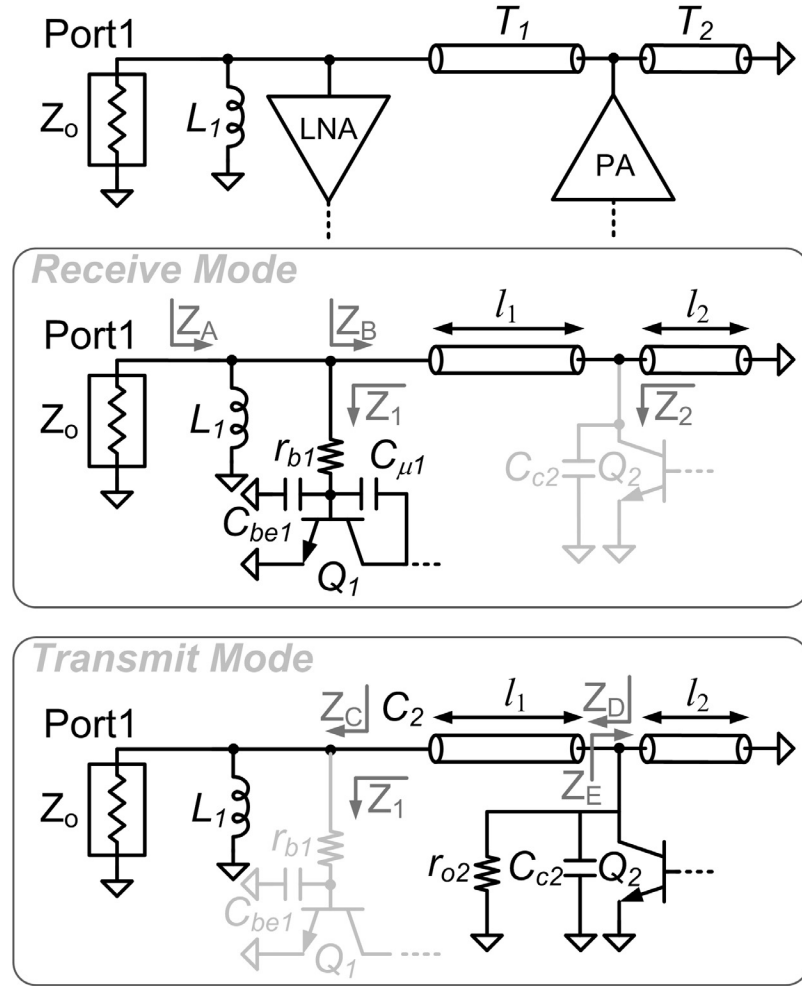


Figure 6.3: Schematic of PALNA matching network for receive and transmit mode at port one.

where C_{c2} is the collector capacitance of Q_2 and β is the propagation constant along the lines. The second equality assumes the characteristic impedance of the transmission lines are the same, i.e. $Z_{o1} = Z_{o2} = Z_o$. If $C_{c2} = 0$, (6.4) reduces to $jZ_o \tan(\beta(l_1 + l_2))$. To prevent received signal power from being absorbed in the power amplifier network, this impedance should be open at the receive frequency f_o . If the denominator of (6.4) is zero, the length of the first transmission line segment is

$$l_1 = \frac{1}{\beta} \arctan \left(\frac{1}{\tan(\beta l_2)} - \omega_o C_{c2} Z_o \right). \quad (6.5)$$

Larger PA devices have a larger capacitance, C_{c2} , which impacts the transmission line length, l_1 . However, the proper proportion between l_1 and l_2 will require additional constraints suggested by the transmit operation.

The Q of the isolation impedance network is defined by $Q_{IN} = \beta/2\alpha$, i.e. the quality factor of the transmission line. Therefore, series resistance, r_s , of the isolation network transmission line is characterized with a shunt resistance

$$R_{PA} = Q_{IN}^2 r_s. \quad (6.6)$$

The impact of this shunt resistance due to the isolation network on the noise figure is defined by

$$F = 1 + \frac{R_s}{R_{PA}} + \frac{\overline{i_n^2} + \overline{v_n^2} |Y_C + G_s + G_{PA}|^2}{4kTR_s}, \quad (6.7)$$

where the noise factor of the LNA is defined by the input referred voltage, $\overline{v_n^2}$, and current, $\overline{i_n^2}$, noise contributions, the correlation admittance, Y_C , and source conductance $G_s = 1/R_s$. When the isolation network is removed, $F_{LNA} = 1 + \frac{\overline{i_n^2} + \overline{v_n^2} |Y_C + G_s|^2}{4kTR_s}$. Therefore, the noise factor degradation is approximately $\frac{R_s}{R_{PA}}$ as long as the conductance G_{PA} is small.

Transmit Mode

In transmit mode, the PA is active and two changes occur to the isolation network with respect to receive mode. First, the load resistance, r_o , of the PA becomes finite ($r_o \sim 5 - 40\Omega$) when the PA is biased to handle high-power. Second, the base bias current of the LNA transistor is reduced to zero. As the bias substantially changes, the impedance seen at the input of the LNA, Z_1 , increases. Notably, the base capacitance is reduced since the transistor in cut-off has no gain, i.e. $C_{b1} \approx C_{be1}$. Second, the base resistance of the transistor is reduced since the intrinsic base resistance is isolated from the network. The impedance seen looking into port one is

$$Z_C \approx sL_1 \frac{sr_{b1}C_{be1} + 1}{s^2L_1C_{be1} + sr_{b1}C_{be1} + 1} \parallel Z_o. \quad (6.8)$$

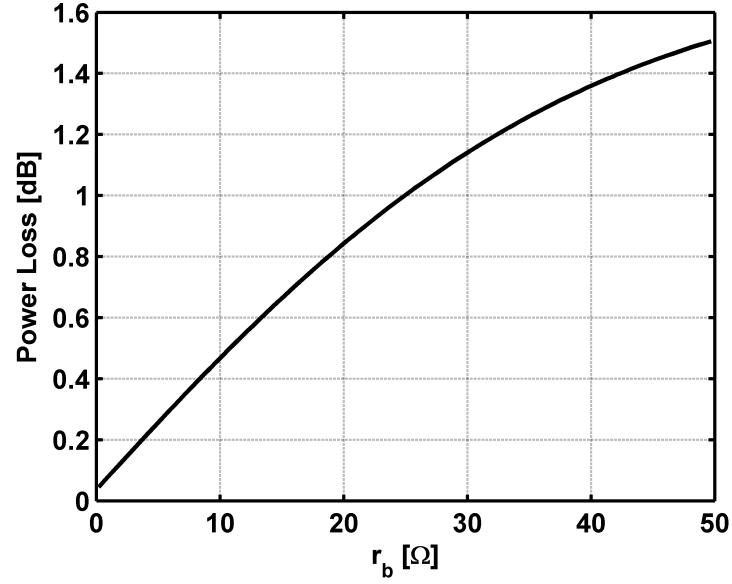


Figure 6.4: Simulated insertion loss of the output matching network in transmit mode at 44-GHz versus the base resistance of Q_1 ($C_{b1} = 50\text{fF}$).

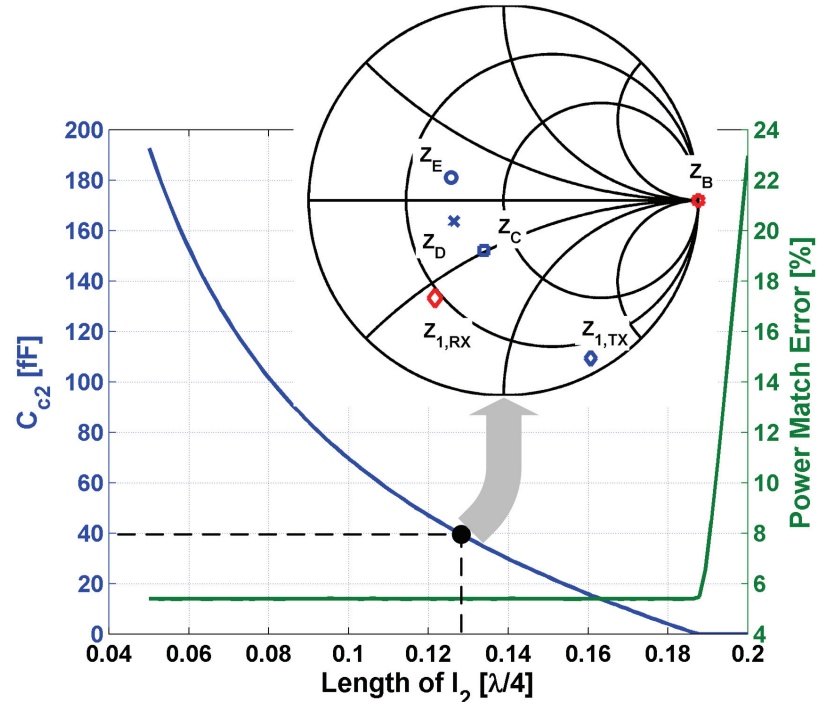


Figure 6.5: Impedance of the PALNA matching network in Fig. 6.3 at 44-GHz ($C_{b1} = 150\text{fF}$, $r_{b1} = 15\Omega$, and $r_{o2} = 40\Omega$).

When the base resistance is very small, then Z_C simplifies to a parallel resonance, i.e. $[sL_1/(1 - \omega^2 L_1 C_{be1})] \parallel Z_o$, and the output of the PA should not be absorbed into the LNA base. Since r_{b1} cannot be completely neglected, the Q of the parallel resonance of the LNA network introduces a shunt resistance of $R_{LNA} = Q_1^2 r_{b1}$ where $Q_1 = (\omega_o C_{be1} r_{b1})^{-1}$. Fig. 6.4 shows the insertion loss of the isolation network in the transmit mode at 44 GHz as a function of the base resistance r_{b1} . To reduce power loss in the transmit mode, smaller base resistance of LNA is desirable which comes at the expense of larger emitter length and higher current consumption. Nonetheless, the power loss is extremely low compared to the insertion loss of an integrated microwave switch.

To achieve a power match, the isolation network should provide impedance matching. The impedance seen at the output of the PA looking towards the LNA is

$$Z_D = Z_o \cdot \frac{Z_C + jZ_o \tan(\beta l_1)}{Z_o + jZ_C \tan(\beta l_1)}. \quad (6.9)$$

Power matching at the collector of the power transistor requires $Z_D^* = Z_E \parallel r_{o2}$. The impedance seen looking into transmission line T_2 is

$$Z_E = \frac{1}{sC_{c2}} \parallel jZ_o \tan(\beta l_2). \quad (6.10)$$

Since the transmission line segment with length l_2 behaves as a load for the PA, this poses an additional design constraint on l_1 and l_2 in conjunction with (6.5). Applying the power match condition, the relationship between the collector capacitance, C_{c2} and transmission line length l_2 is plotted in Fig. 6.5. With knowledge of l_2 and C_{c2} , l_1 is implicitly determined. As C_{c2} is increases, more of the overall quarter wavelength transmission line length is absorbed into l_1 since l_2 becomes smaller. At each of these choices for C_{c2} , the power matching condition is satisfied to within 5% of the ideal impedance match.

For example, if $C_{c2}=40$ fF, the choice of transmission line length is $l_1 = l_2 = \lambda/8$. The impedance conditions corresponding to the design of the isolation network are shown in the Smith chart in Fig. 6.5. The capacitance, C_{b1} , is reduced in transmit mode due to the lower base-collector and base-emitter capacitance.

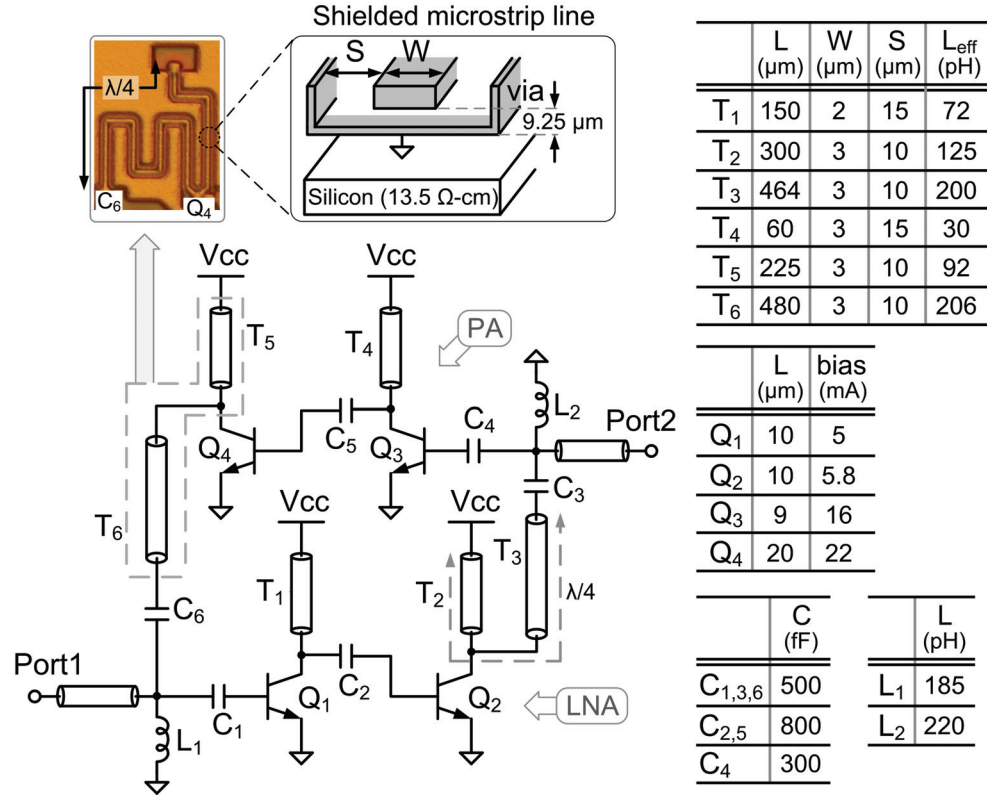


Figure 6.6: Schematic of power amplifier low noise amplifier (PALNA) without biasing circuitry and shielded microstrip line structures.

When the circuit enters receive mode, the base capacitance increases by nearly four times due to the diffusion capacitance of the base and the Miller effect - this is a particular feature of the SiGe HBT technology. Additionally, the base resistance is reduced by a factor of one-half compared to the receive mode. The variation of the input impedance, Z_1 , is assumed to be $15 - j25$ in the receive mode and $7.5 - j75$ in the transmit mode at 44 GHz. The impedance Z_1 shifts from the outside of the Smith chart to an improved match when the operation is switched to receive mode. Applying these assumptions and the choice of C_{c2} , the Smith chart indicates that the transmit mode impedances are conjugately matched, i.e. $Z_D^* = Z_E \parallel r_{o2}$. In receive mode, Z_B is very large indicating significant isolation of the power amplifier.

6.3 Circuit Implementations

The Q -band bidirectional transceiver consists of an integrated PA/LNA, passive ring mixer, frequency doubler with a LO amplifier, and IF amplifiers implemented in a $0.12\ \mu\text{m}$ SiGe BiCMOS process as illustrated in Fig. 6.2. All HBT devices use minimum emitter width. Transmission lines are realized using shielded microstrip-mode lines to isolate the signal line from the substrate coupling ($\rho_{sub} = 13.5\ \Omega\text{-cm}$) which lends to slightly higher Q and improved stability limitations. To minimize transmission line area, side shields are shared between neighboring cells as shown in Fig. 6.6. Characteristic impedance is chosen with the line width (W) and shielding spacing (S) in Fig. 6.6. All capacitors are implemented using metal-to-metal (MIM) capacitors. All inductors are custom designs that use the top aluminum metal (thickness = $4\ \mu\text{m}$ and sheet resistance = $7\ \text{m}\Omega/\square$). Passive structures are simulated in SONNET, extracted as S -parameters, and included in the Spectre simulations.

6.3.1 PALNA

Fig. 6.6 shows the schematic of PALNA without biasing circuitry. Both the PA and LNA are designed using two cascaded common-emitter stages with the inductive transmission line loads. Device sizing is provided in the table accompanying the figure.

PA Stage

The first stage of the PA is designed for maximum gain. To achieve a peak f_T of 165 GHz, the emitter length (l_E) of the common-emitter transistor Q_3 is $l_E = 9\ \mu\text{m}$ and the stage is biased at 16 mA, i.e. $1.7\ \text{mA}/\mu\text{m}$. The capacitor C_4 provides d.c. blocking as well as the input impedance matching to the PA stage. Transmission line T_4 has a length $l_4 = 60\ \mu\text{m}$ ($L_{eff} = 30\ \text{pH}$) to provide shunt loading for the first PA stage. The peak gain of the first amplifier stage is 15 dB. Interstage matching between the first and second PA stage is realized using capacitor C_5 .

The final PA stage is Q_4 ($l_E = 20 \mu\text{m}$) and is designed to deliver at least 12 dBm to the output port in Class-A operation. A nominal d.c. bias of 22 mA reduces the average current density to $1.1 \text{ mA}/\mu\text{m}$. The output load impedance of PA is $Z_D = 55.1 + j16.9 \Omega$ at 44-GHz. Transmission line T_5 is $225 \mu\text{m}$ long ($L_{eff} = 92 \text{ pH}$).

The isolation network between the PA and LNA is formed with transmission line T_6 . From (6.5), l_6 is $480 \mu\text{m}$ long and the transmission line has a characteristic impedance of 60Ω . When the first stage of the LNA (Q_1) is unbiased, the impedance seen looking into the LNA is $Z_1 = 7.2 - j77.4$ at 44-GHz and constitutes the external capacitance C_1 , the base resistance r_{b1} and the base capacitance $C_{be1} + C_{bc1}$. A shunt inductance (L_1) of 185 pH resonates the series combination of these capacitances to generate an impedance $Z_C = 45.6 - j1.2 \Omega$ determined from (6.3) that is matched to 50Ω . The impedance seen looking into the PALNA in transmit mode is $Z_A = 57.7 + j12.5 \Omega$ at 44-GHz and also indicates impedance matching to 50Ω over 38–53 GHz ($|S_{11}| < -10 \text{ dB}$). The finite quality factor of the output matching network due to the base resistance r_{b1} introduces an insertion loss of 0.35 dB at 44 GHz. Nonetheless, compared to the insertion loss of SPDT switches (Table 6.1) this loss is much lower.

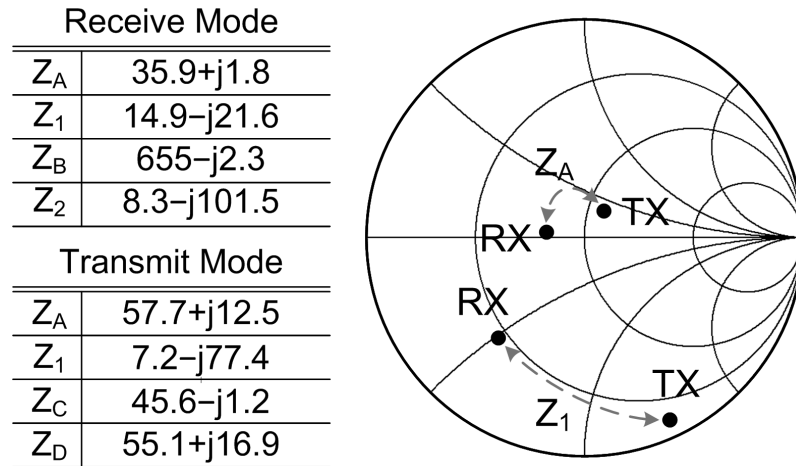


Figure 6.7: Circuit simulation of PALNA circuit impedance matching in a $0.12 \mu\text{m}$ SiGe process.

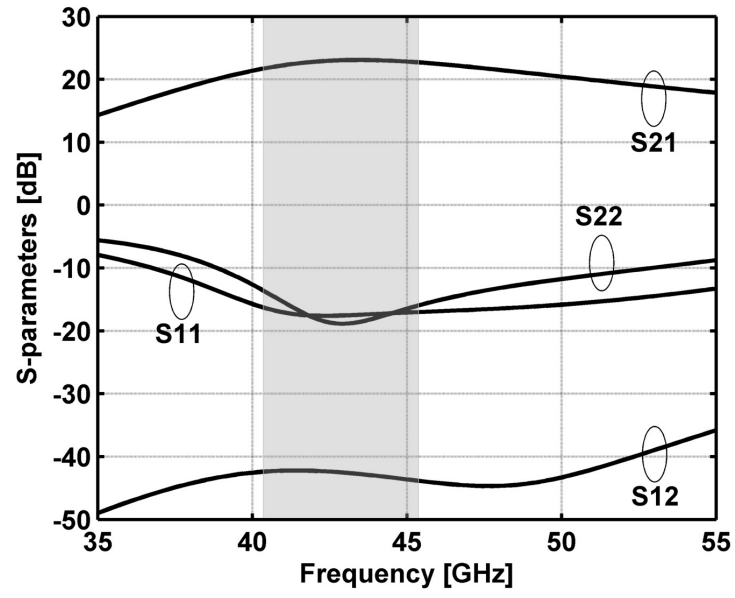
LNA Stage

For low noise operation, transistor Q_1 in the first stage is biased at a lower current density of $0.5 \text{ mA}/\mu\text{m}$ ($f_T = 163 \text{ GHz}$). For an emitter length of $10 \mu\text{m}$, the first stage consumes 5 mA . The input noise match of the LNA is achieved with the shunt inductor $L_1 = 185 \text{ pH}$. Additionally, the capacitor C_1 is used for dc blocking as well as the input impedance matching. Transmission line T_1 has length $l_1 = 150 \mu\text{m}$ and acts as an inductive shunt load ($L_{eff} = 72 \text{ pH}$) for Q_1 . Since transmission line lengths, $T_5 + T_6$, are a effective quarter wavelength at the operating frequency, capacitor C_6 is added for dc blocking adjusts the impedance of Z_B . The impedance of Z_B is $655 - j2.3 \Omega$ at 44 GHz and suggests excellent isolation of the signal path from the power amplifier.

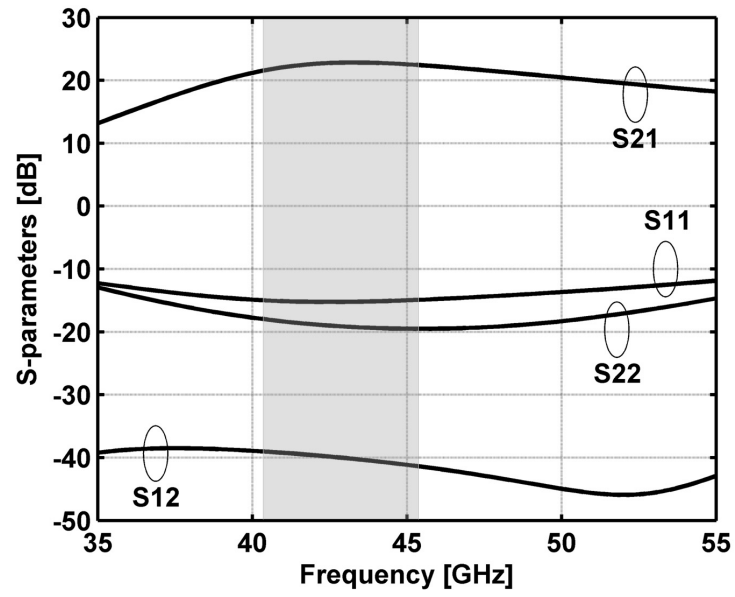
The input impedance of LNA in receive mode is $Z_A = 35.9 - j1.8 \Omega$ at 44 GHz and provides an acceptable match to 50Ω over a range from $35\text{--}55 \text{ GHz}$ ($|S_{11}| < -10 \text{ dB}$). If the PA is removed and isolation network is removed completely the input impedance shifts to $Z_A = 36.3 - j3.6 \Omega$ at 44 GHz . The second stage of the LNA is designed for a high gain and the emitter length of the transistor Q_2 is $l_E = 10 \mu\text{m}$ which is biased at 5.8 mA to achieve a peak f_T of 171 GHz . The interstage matching between stages is realized using the capacitor C_2 . The isolation network formed at the output of the LNA and the input of the PA follows a similar design method. The transmission line T_2 has a length of $300 \mu\text{m}$ to load the second stage of LNA as well as the part of the quarter wave isolation network based on the transmission line T_3 .

PALNA Simulations

The supply of the PA circuit is 1.8 V for high output power while the supply for the LNA is 1 V . Fig. 6.8(a) and (b) show the simulated S -parameters of PALNA. In the transmit mode, the amplifier has a small-signal gain of 23 dB with a 3-dB bandwidth of 11.5 GHz ($39\text{--}50.5 \text{ GHz}$). Input and output matching are better than -13 dB and -16 dB , respectively, over the 3-dB bandwidth while isolation is better than 42 dB . In the receive mode, the amplifier has a gain of 23 dB with a 3-dB bandwidth of 12 GHz ($39\text{--}51 \text{ GHz}$). Input and output return losses



(a)



(b)

Figure 6.8: Simulated S -parameters of PALNA in (a) TX mode and (b) RX mode.

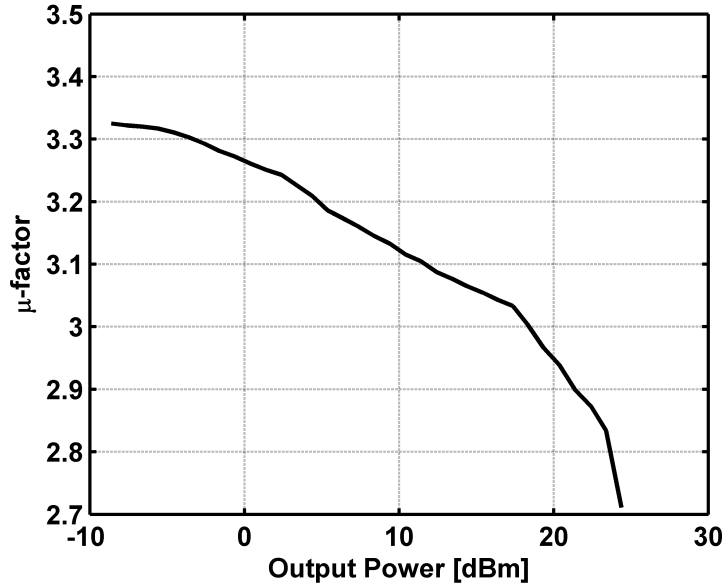


Figure 6.9: Simulated μ -factor of PALNA in transmit mode at 45-GHz versus the output power.

are better than 15 dB and 17 dB, respectively, over the 3-dB bandwidth while isolation is better than 39 dB. Fig. 6.9 shows the simulated stability μ -factor of PALNA as a function of the output power at 44 GHz. The μ -factor is greater than 3 at low power levels and begins to reduce as the output power increases. This degraded stability occurs because the output power of the PA begins to turn-on the LNA base. Nonetheless, the stability is guaranteed to more than 20 dBm. The amplifier remains unconditionally stable in both TX and RX modes from d.c. to more than 100 GHz.

Fig. 6.10 shows that the simulated noise figure of PALNA with the isolation network (Z_B in Fig. 6.3) (solid line) in RX mode is 4 dB at 45 GHz. The minimum noise figure (NF_{min}) of the 0.12- μ m HBT device is also shown in Fig. 6.10 for the same emitter length. The NF_{min} at 45 GHz is about 2.8 dB indicating that our noise figure is degraded by around 1.2 dB. This compares favorably to an alternative design where SPDT switches with insertion loss of 3 dB are implemented. In this case, the minimum noise figure of receiver is bounded to 5.8 dB. In Fig. 6.10, the noise figure without the isolation network (dotted line) is also plotted and the

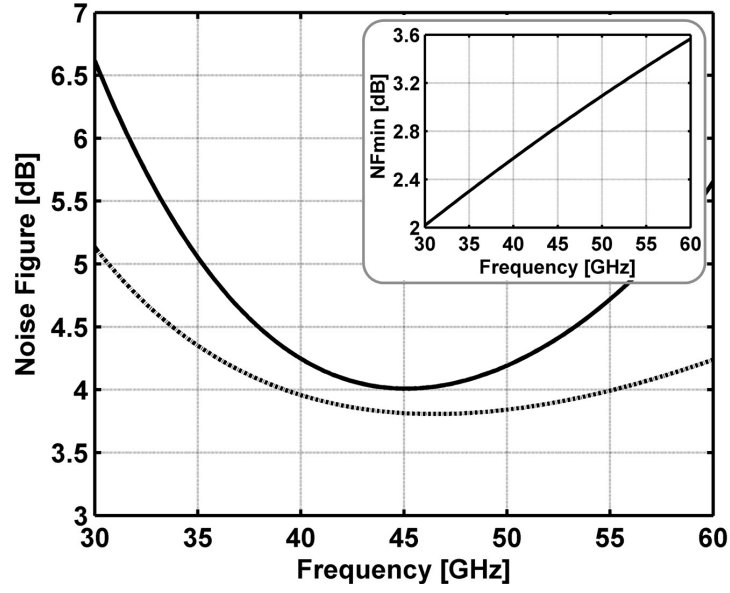


Figure 6.10: Simulated noise figure of PALNA in RX mode with the isolation network (Z_B in Fig. 6.3) (solid line) and without the isolation network (dotted line).

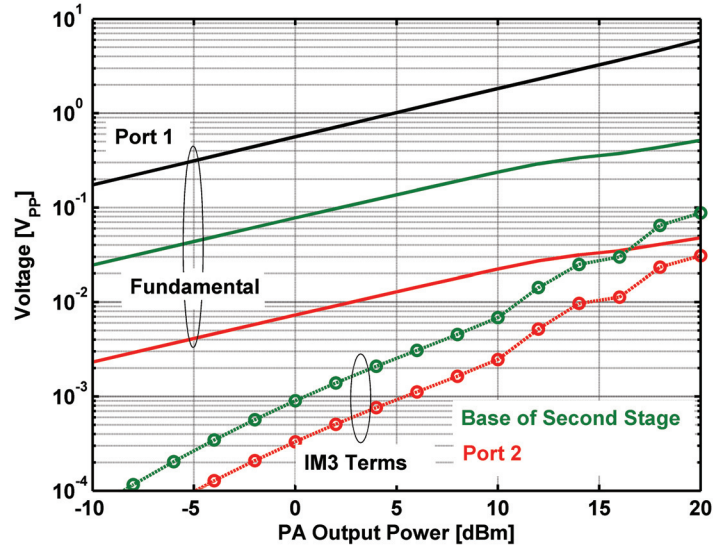


Figure 6.11: Distortion generation of the output network in the transmit mode.

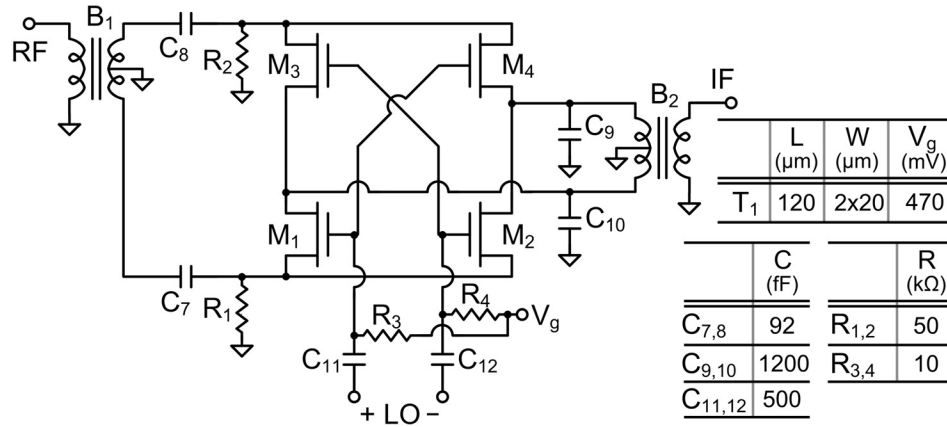


Figure 6.12: Schematic of resistive ring mixer without biasing circuitry.

noise figure degradation is only less than 0.2 dB at 45 GHz due to the isolation network as expressed in (6.7).

Finally, the nonlinear capacitance of the LNA base is a source of distortion in the transmit mode since high power can generate intermodulation products which propagate through the subsequent LNA stages and impact the input of the PA. Fig. 6.11 investigates the IM3 terms after the first LNA stage and the second LNA stage. At an output power of 10 dBm, the IM3 products are more than 40 dB below the fundamental output power.

6.3.2 Double-balanced Resistive Mixer

The double-balanced resistive mixer consists of four 120-nm NFETs in a ring configuration as shown in Fig. 6.12. A passive mixer is chosen because it is inherently bidirectional and offers high linearity. The double-balanced structure also offers high isolation between RF, LO and IF ports and cancellation of the even-order harmonics. The FET gates are biased near the threshold voltage, *e.g.* $V_g \approx 470$ mV, and driven with a 40 GHz LO signal. The transistor width is 2×20 - μm for a combination of low conversion loss and one-dB compression. At the RF port, the series capacitors C_7 and C_8 are used with the on-chip balun B_1 to provide matching to 50 Ω . Shunt resistors R_1 and R_2 of 50 k Ω are included to prevent

eliminate any floating nodes. At the LO port, series capacitors C_{11} and C_{12} isolate the dc bias on the NFET gates from the supply of the LO driver (described in the next section). Shunt capacitors C_9 and C_{10} short LO and RF harmonics at the IF port to improve the LO-to-IF and RF-to-IF isolation.

To provide differential signals, on-chip 180° spiral baluns are implemented at the RF, LO and IF ports. The RF balun B_1 is shown in Fig. 6.13(a) and realized using two top aluminum metal layers with a $4\text{-}\mu\text{m}$ spacing between metal plates. The one-turn primary inductor with $4\text{-}\mu\text{m}$ width is implemented using the top aluminum metal and the port one is matched to the $50\ \Omega$ output port impedance of PALNA in Fig. 6.6. The two-turn secondary inductor is implemented using the second top aluminum metal (thickness = $1.25\ \mu\text{m}$ and sheet resistance = $23\ \text{m}\Omega/\square$) and is oriented in the opposite direction of the primary inductor. The secondary coil has a width of $6\ \mu\text{m}$ and spacing of $2\ \mu\text{m}$. The impedance of the secondary coil matches the input impedance of the resistive ring mixer ($\approx 21.5 - j56.5$ single-ended). The RF balun requires a maximum area of $82\ \mu\text{m} \times 82\ \mu\text{m}$ and demonstrates a self-resonance above 90 GHz. Consequently, no output magnitude imbalance due to a notch response occurs at the frequencies of interest. Additionally, capacitors (C_7 and C_8) adjust the input impedance of the ring mixer to minimize the phase and magnitude imbalances. EM simulations indicate that B_1 has a minimum conversion loss of 1.1 dB, a gain imbalance of 0.1 dB and a phase imbalance of less than 1 degree over the 3-dB bandwidth. Port one of B_1 is matched to $50\ \Omega$ over 40–50 GHz ($|S_{11}| < -10\ \text{dB}$) and the band-pass behavior isolates out-of-band frequency components around 44 GHz.

The IF balun B_2 is shown in Fig. 6.13(b) and is implemented using only the top aluminum metal with $4\ \mu\text{m}$ width and $5\ \mu\text{m}$ spacing between lines. B_2 measures $210\ \mu\text{m}$ by $210\ \mu\text{m}$ and has a resonant frequency of around 25 GHz. The low self-resonance eliminates coupling of the single-ended LO (at 40 GHz) or RF (at 44 GHz) to couple into the IF port. Port one and two is matched to $50\ \Omega$ over 1.5–10 GHz ($|S_{11}| < -10\ \text{dB}$). EM simulations indicate that B_2 has a minimum conversion loss of 1.53 dB, a gain imbalance of 0.15 dB and a phase imbalance of less than 1 degree over the 3-dB bandwidth. isolations. Deep trench isolation is

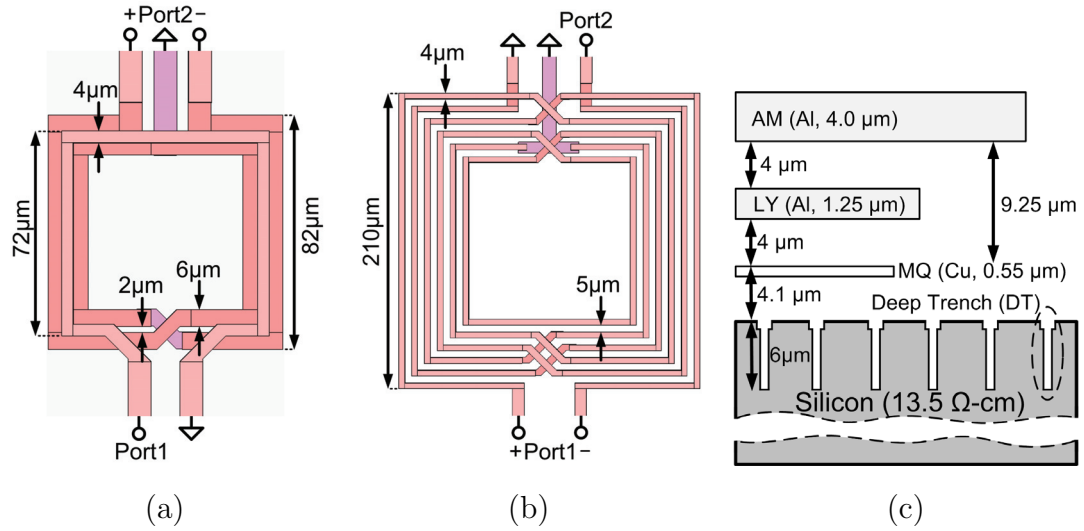


Figure 6.13: Layout of the (a) RF balun (B_1) and (b) IF balun (B_2) as shown in Fig 6.12 and (c) the cross-section of SiGe BiCMOS process.

place beneath the on-chip baluns to reduce substrate coupling as shown in Fig. 6.13. Spectre simulations indicate that the conversion loss and input-referred 1-dB compression point are 9 dB and 8 dBm in both TX and RX modes at 42 GHz with an LO power of 4 dBm at 40 GHz. Isolation between ports is simulated to be better than 50 dB for both TX and RX modes.

6.3.3 Frequency doubler with LO amplifier

Fig. 6.14 illustrates the schematic of a balanced Q -band frequency doubler and LO amplifier. At the LO port, series capacitors C_{15} and C_{16} and shunt capacitors C_{13} and C_{14} are used for input matching at 20 GHz to the on-chip balun B_3 . The balun design is similar to the RF balun B_1 . The LO balun measures 92 μm by 92 μm for the one-turn primary inductor and 102 μm by 102 μm for two-turn secondary inductor. EM simulations indicate that LO spiral balun B_3 has a minimum conversion loss of 1 dB, a gain imbalance of 0.1 dB and a phase imbalance of less than 1 degree at 20 GHz. The LO return loss is 30 dB at 20 GHz.

The common-emitter transistors Q_5 and Q_6 are the doubling stage followed by a cascode stage, Q_7 that amplifies the $2f_o$ signal and reduces the Miller effect

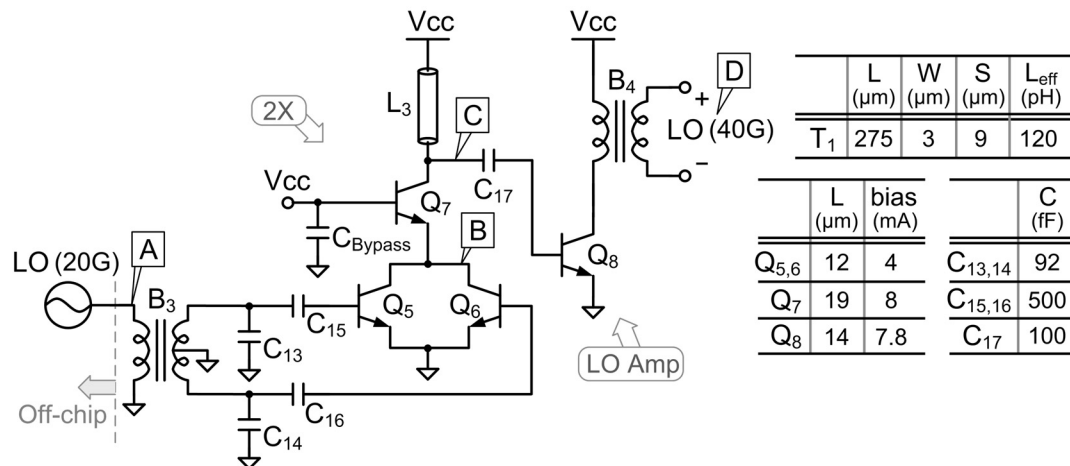


Figure 6.14: Schematic of doubler with LO amplifier without biasing circuitry.

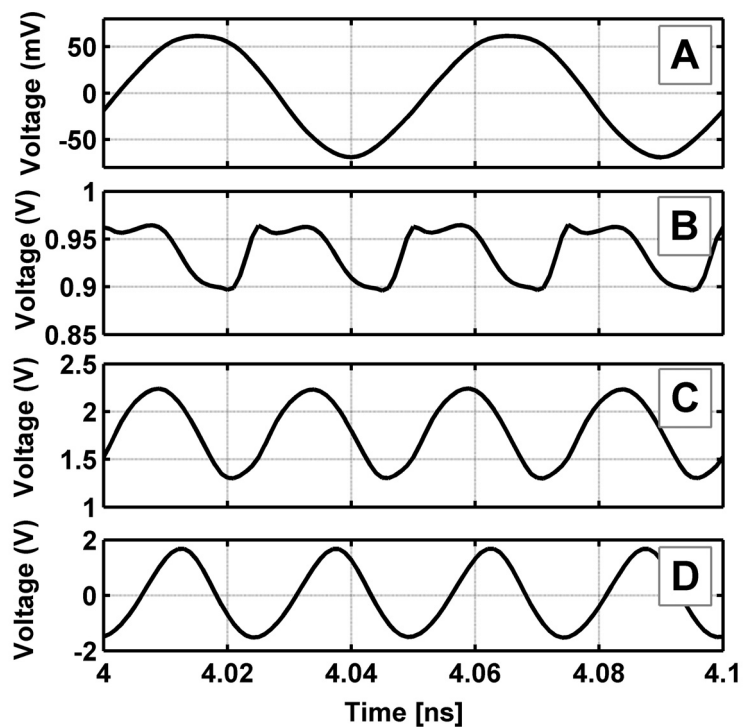


Figure 6.15: Voltage waveforms at each node in Fig. 6.14.

of Q_5 and Q_6 . Both doubling and cascode stages are biased in the forward-active region and consume 8 mA from a 1.8 V supply. Inductor L_3 resonates with the cascode device Q_3 at the $2f_o$ to increase the output LO power and is realized using a transmission line of length $275 \mu\text{m}$.

The output power at $2f_o$ (40 GHz) is amplified using a single LO amplifier Q_8 ($l_E = 14 \mu\text{m}$) biased at 7.8 mA. Interstage matching between frequency doubler and LO amplifier is realized using the capacitor C_{17} to provide d.c. isolation. The LO amplifier is loaded with B_4 to convert from a single-ended to differential LO at the double-balanced mixer in Section 6.3.2. B_4 measures $56 \mu\text{m}$ by $56 \mu\text{m}$ for the one-turn primary inductor and $66 \mu\text{m}$ by $66 \mu\text{m}$ for two-turn secondary inductor. EM simulations indicate that LO spiral balun (B_4) has a minimum conversion loss of 1 dB, a gain imbalance of 0.1 dB and a phase imbalance of less than 1 degree at 40 GHz.

Fig. 6.15 shows that the voltage waveforms at multiple stages in Fig. 6.14. At input LO port (A), the input power of the 20 GHz LO is around -13 dBm (or $0.13 V_{PP}$ into 50Ω). After the doubling stage (node B), the 20 GHz LO is converted to a 40-GHz LO with amplitude of $60 mV_{PP}$ along with strong 4th harmonic content. However, the cascode stage eliminates these other harmonics and provides a spectrally clean 40 GHz signal with an amplitude of $80 mV_{PP}$ at node C. The LO amplifier boosts the signal swing to generate a $3.1 V_{PP}$ differential signal at node (D) with B_4 .

6.3.4 IF amplifiers

Fig. 6.16 shows the schematic of the bidirectional IF amplifiers. The bidirectional IF amplifiers are less sensitive to input and output matching at the IF frequency. The IF amplifiers for both TX and RX modes consist of two cascaded common-emitter stages with the resistor loads. In TX mode, the first amplifier Q_{11} is biased at 4 mA while the second amplifier Q_{12} is biased at 10.5 mA for maximum IF output power. The load resistors $R_1 \sim R_4$ are 60Ω and are realized using tantalum nitride resistors.

In RX mode, the first amplifier stage Q_9 is designed for minimum noise

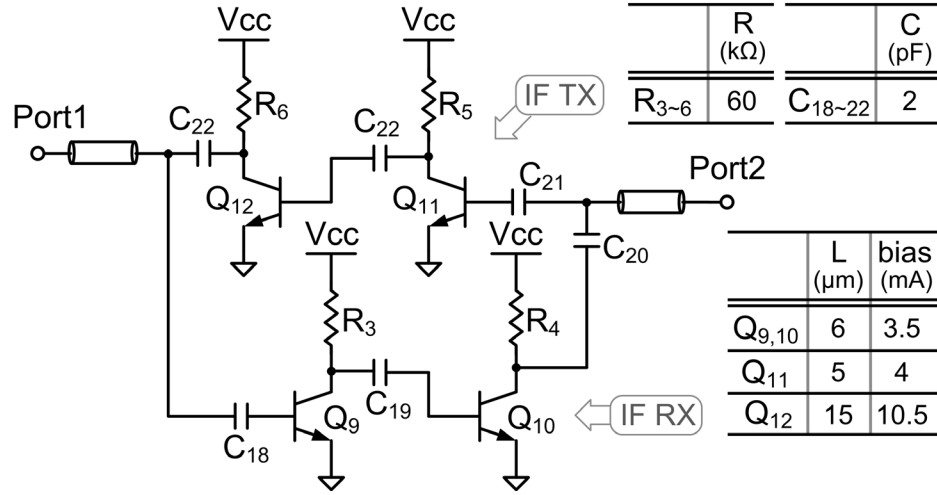


Figure 6.16: Schematic of IF amplifiers without biasing circuitry.

figure and biased at 3.5 mA. The second amplifier stage Q_{10} is biased at 6.5 mA. Spectre simulations indicate a small signal gain of more than 25 dB at nominal bias conditions for both TX and RX IF amplifiers. Additionally, the IF amplifier in RX mode has a noise figure of 6 dB over the 3-dB bandwidth. In contrast to PALNA, the alternate signal path (C_{22} and R_6) is not isolated in receive mode, the noise contributed by the R_6 is directly added to the input of IF amplifier. However, since the total noise performance is dominated by the input stage (PALNA) of the system, the noise penalty due to IF amplifier is about 0.4 dB. The supply for the TX IF and RX IF amplifiers are 1.8 V and 1.5 V, respectively.

6.4 Experimental Results

The Q -band transceiver is implemented in a 0.12- μm SiGe BiCMOS technology ($f_T = 200 \text{ GHz}/f_{max} = 230 \text{ GHz}$). The chip microphotograph is shown in Fig. 6.17. The transceiver occupies 1.6 mm x 0.8 mm (1.28 mm²). At nominal bias conditions, the chip consumes 119.4 mW and 54 mW in transmit and receive modes from 1 V, 1.5 V, and 1.8 V supplies.

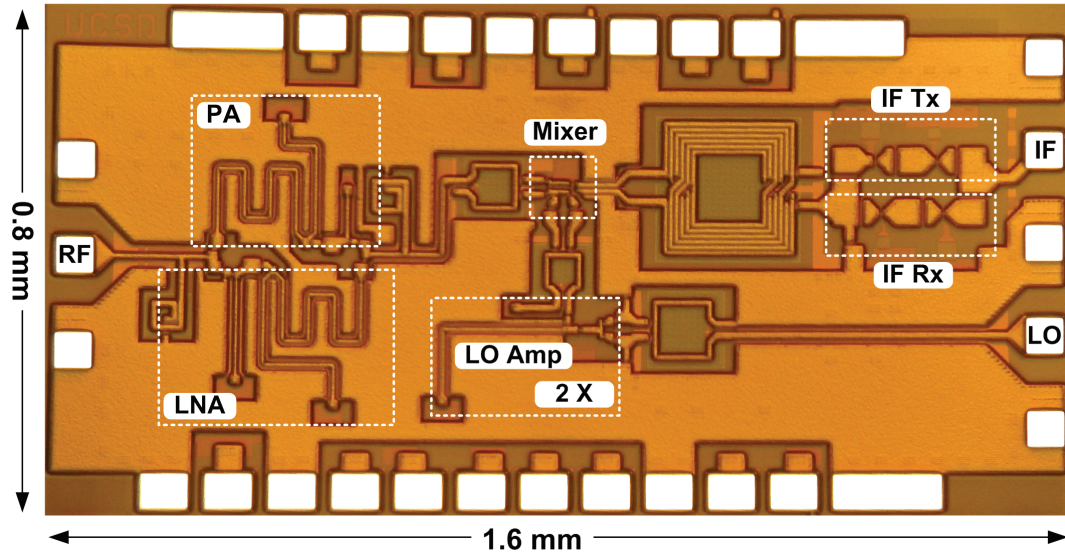


Figure 6.17: Chip microphotograph of Q -band transceiver in $0.12\text{-}\mu\text{m}$ BiCMOS technology.

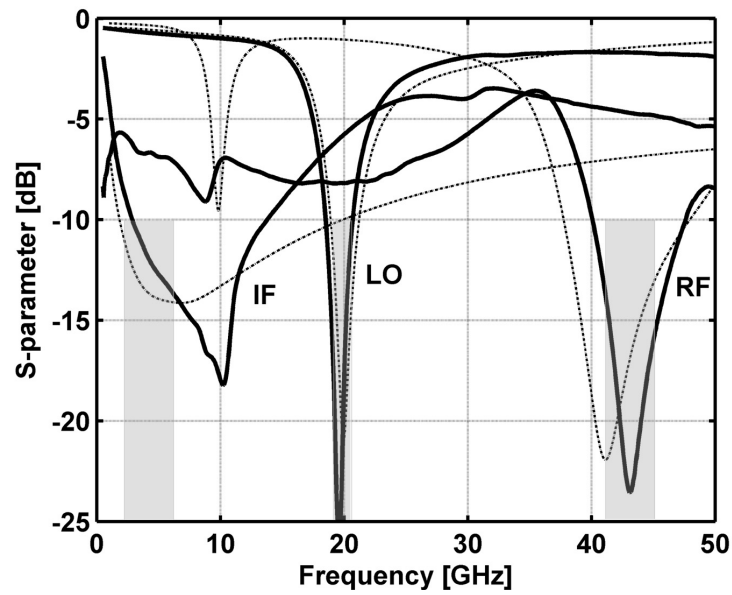


Figure 6.18: (Solid lines) Measured input matching and (dotted lines) simulated input matching in TX mode.

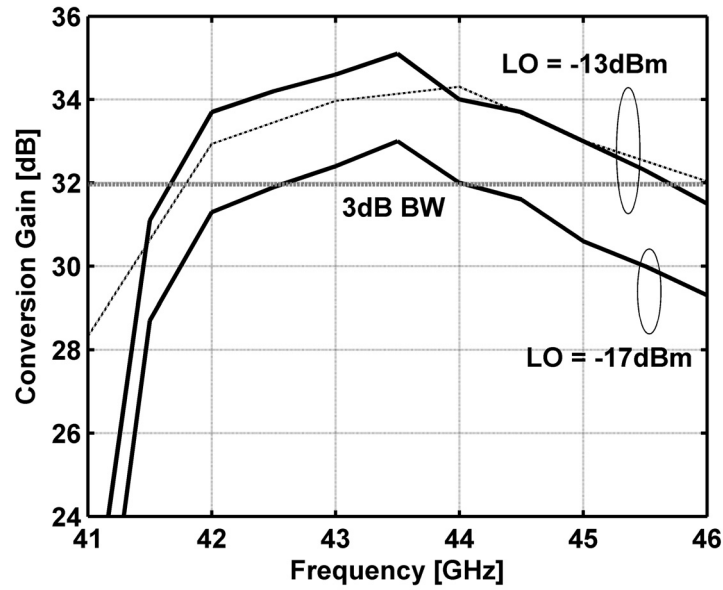


Figure 6.19: (Solid line) Measured conversion gain and (dotted line) simulated conversion gain in TX mode.

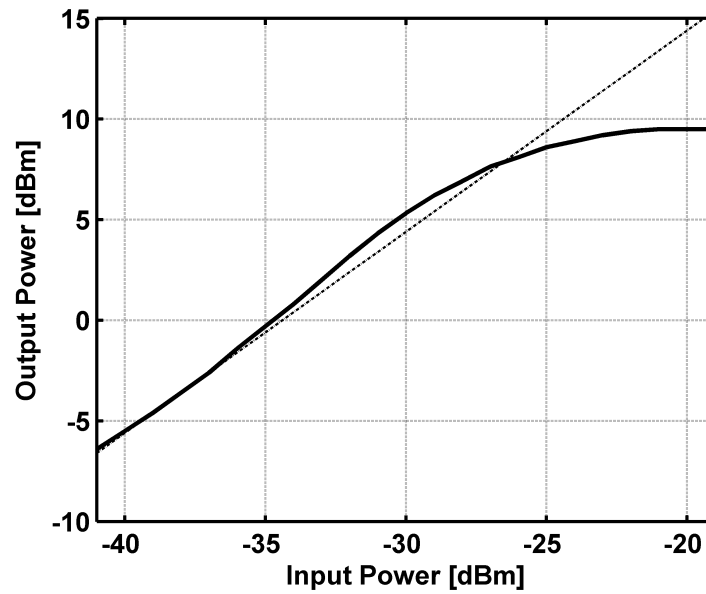


Figure 6.20: Measured output power at RF = 42 GHz in TX mode at nominal bias conditions (V_{PA} and V_{IF} = 1.8 V).

6.4.1 Transmit mode

S -parameters are measured using the Agilent E8361A two-port network analyzer using on-chip probing with Picoprobe coplanar 50A GSG probe at the RF port and 40A GSGSG probe at LO and IF ports. The measured S -parameters for TX input matching are shown in Fig. 6.18 and compared against Spectre simulations (dotted lines). The measured RF and IF input return losses are better than 15 dB and 10 dB, respectively, over the frequency band of interest. The measured LO input return loss is 17 dB at 20 GHz and is better than 10 dB from 18.5 GHz to 20.8 GHz. Excellent agreement between simulation and measurement results results from the use of SONNET models of all passives in the design.

The TX and RX conversion gains are measured using an Agilent E4400 spectrum analyzer and Agilent E4419B power meter with 8487A 50 GHz power sensor. An Agilent E8257D RF synthesizer generates the local oscillator at 20 GHz as well as IF or RF signals for the TX or RX measurements, respectively. The measured TX conversion gains are shown at nominal bias conditions with an LO power of -13 and -17 dBm in Fig. 6.19. The simulation result with an LO power of -13 dBm (dotted line) is also provided for comparison. The TX conversion gain is 35 dB with a 3-dB bandwidth of 4 GHz ($41.7 \sim 45.7$ GHz) and is better than 33 dB for LO power as low as -17 dBm. The simulation results agree with the experimental data. The measured S -parameters and frequency spectrum indicate that all TX port-to-port isolations are better than 45 dB.

Measured gain compression at RF = 42 GHz is recorded in Fig. 6.20 at the nominal bias condition (V_{PA} and $V_{IF} = 1.8$ V). The output-referred 1-dB compression point ($OP1dB$) in TX mode is 8.5 dBm and the saturated output power (P_{sat}) is 9.5 dBm with LO power of -13 dBm. This represents that the PALNA in TX mode has a power-added-efficiency (PAE) of 13.7 %.

To experiment the performance the double-balanced resistive ring mixer was fabricated as a stand-alone. Fig. 6.21 shows the chip microphotograph of a mixer with on-chip baluns (B_1 and B_4 in Fig 6.12 and 6.14). Measured results of output power compression and single-side-band (SSB) noise figure are also shown in Fig. 6.21. Off-chip IF balun was used to test the mixer. The mixer has a

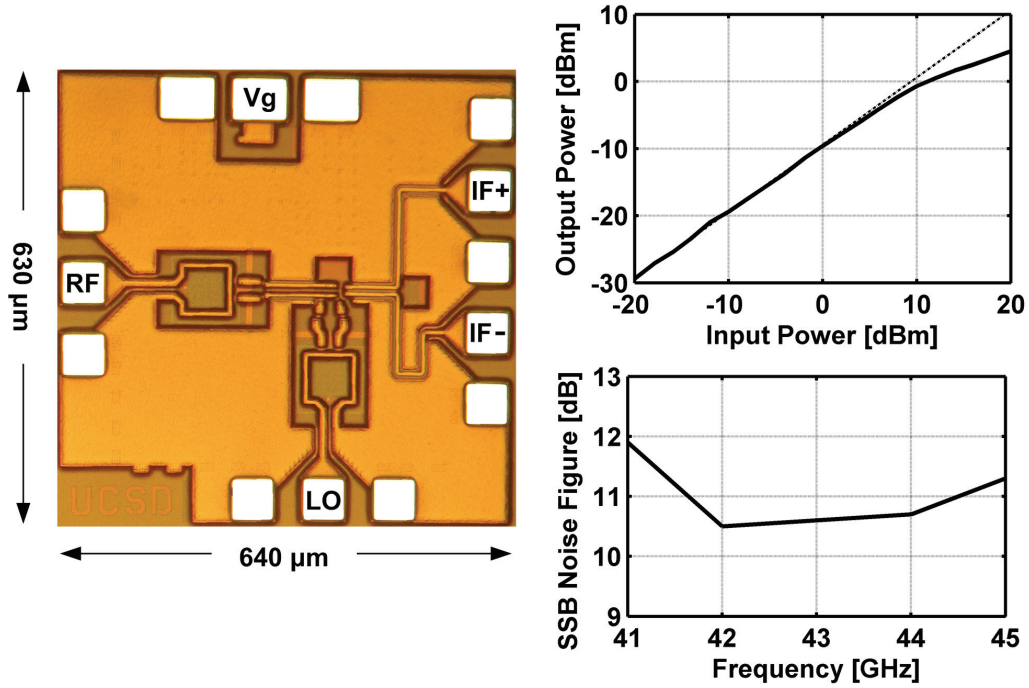


Figure 6.21: Chip microphotograph of a mixer with on-chip baluns and measured results of output power and SSB noise figure.

conversion loss of 9.4 dB at 43 GHz with LO power of 6 dBm. Measured input-referred 1-dB compression point is 8.5 dBm. Measured SSB noise figure is 10.5 dB and less than 11 dB over the frequency band of interest.

6.4.2 Receive mode

Fig. 6.22 shows the measured S -parameters for RX input matching with comparison to simulated results. The measured RF and IF input return losses are better than 15 dB and 17 dB, respectively. The measured LO input return loss is 20 dB at 20 GHz and is better than 10 dB from 18.5 GHz to 21.2 GHz. The measured RX conversion gain is shown at nominal bias conditions with an LO power of -13 and -17 dBm in Fig. 6.23. The RX conversion gain is 34 dB with a 3-dB bandwidth of 3 GHz (41.8 $\sim$ 44.8 GHz) and is better than 31 dB for LO power as low as -17 dBm. Additionally, the RX conversion gain is increased to more than 39 dB for $V_{LNA} = 1.5$ V and $V_{IF} = 1.8$ V of the RX amplifiers. The simulation results agree with the experimental data. The measured S -parameters

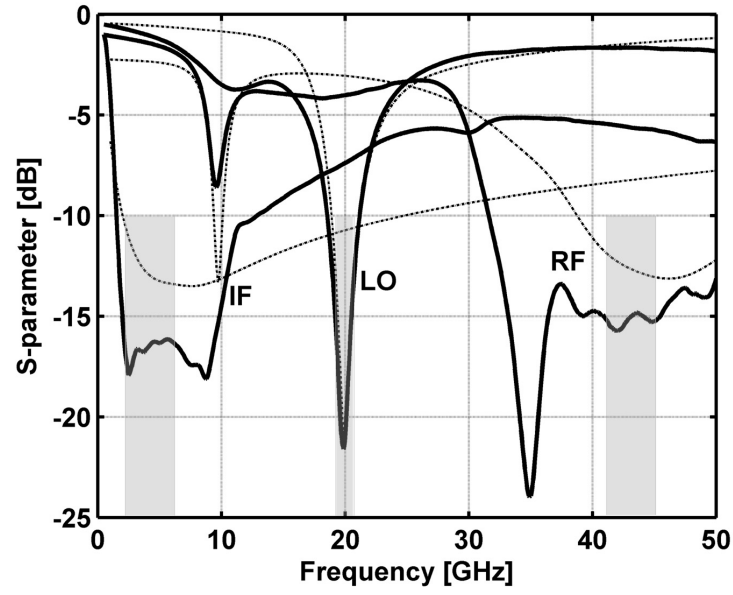


Figure 6.22: (Solid lines) Measured input matching and (dotted lines) simulated input matching in RX mode.

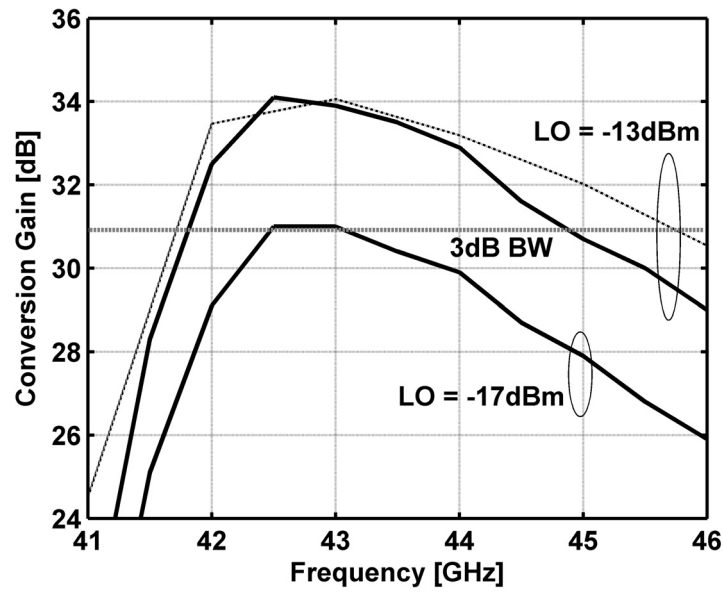


Figure 6.23: (Solid line) Measured conversion gain and (dotted line) simulated conversion gain in RX mode.

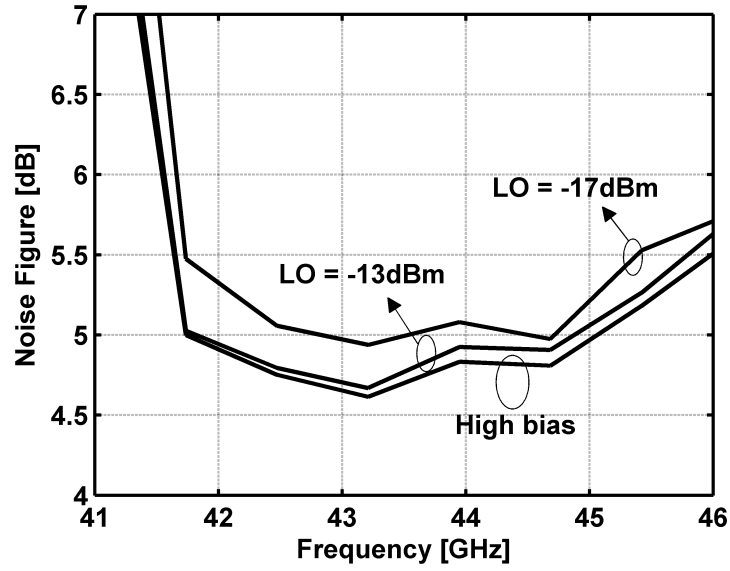


Figure 6.24: Measured noise figure in RX mode in the Q -band transceiver in $0.12\text{-}\mu\text{m}$ BiCMOS technology.

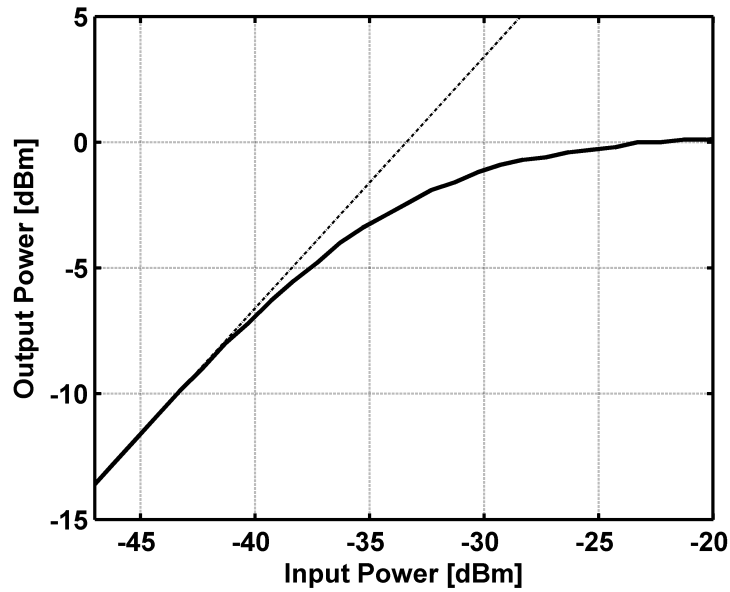


Figure 6.25: Measured output power at $\text{RF} = 43\text{ GHz}$ in RX mode at nominal bias conditions ($V_{LNA} = 1\text{ V}$ and $V_{IF} = 1.5\text{ V}$).

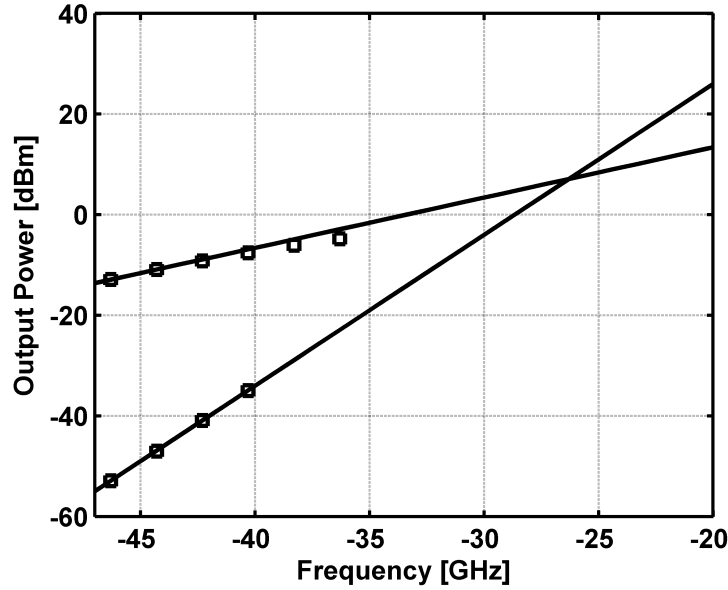
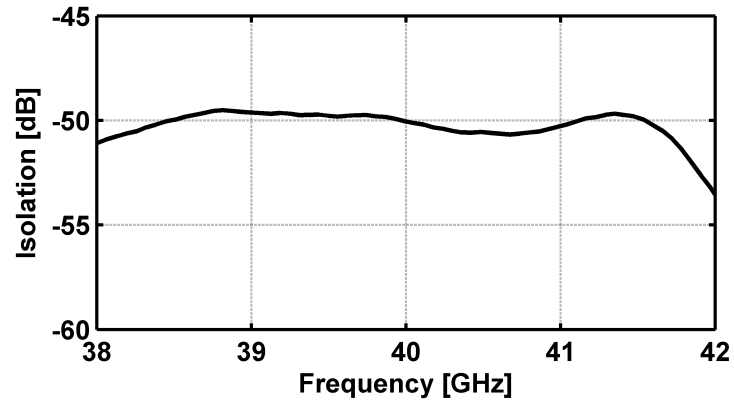


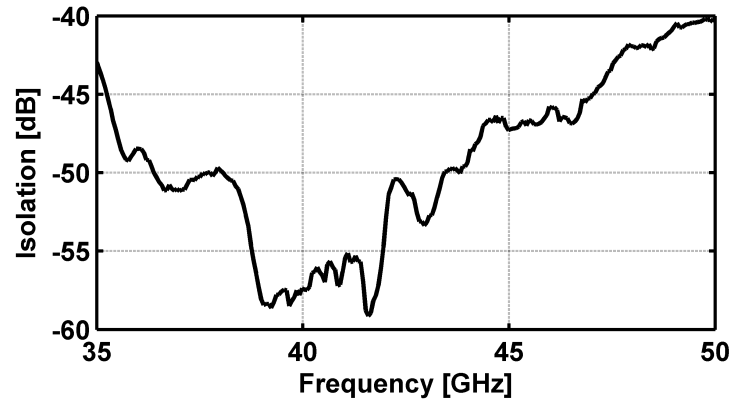
Figure 6.26: Measured input-referred 3rd order intercept point at RF = 43 GHz in RX mode at nominal bias conditions ($V_{LNA}=1$ V and $V_{IF}=1.5$ V).

and frequency spectrum indicate that all RX port-to-port isolations are better than 47 dB. The noise figure is measured using an Agilent E4400 spectrum analyzer with an Agilent 346C-K01 noise source. The noise figure is initially calibrated with an Agilent E4440 spectrum analyzer and cable and probe losses are de-embedded from the measurement. Fig. 6.24 shows the measured noise figure in RX mode with an LO power of -13 and -17 dBm as well as the high bias condition ($V_{LNA} = 1.5$ V and $V_{IF} = 1.8$ V of the RX amplifiers). The measured noise figure with an LO power of -13 dBm is 4.7 dB at 43.3 GHz and better than 5 dB over the 3-dB bandwidth. At lower LO power (-17 dBm), noise figure is slightly increased to 5 dB.

The gain compression is recorded in Fig. 6.25 at the nominal bias condition. The output-referred 1-dB compression point ($OP1dB$) at RF = 43 GHz in RX mode is -5 dBm. Fig. 6.26 shows the measured input-referred 3rd order intercept point (IIP_3) at RF = 43 GHz in RX mode at nominal bias conditions. The measured IIP_3 in RX mode is -26 dBm. The performance of the Q-band transceiver including the power consumption for each of the blocks is summarized



(a)



(b)

Figure 6.27: Isolations of (a) LO-to-RF in TX mode and (b) RF-to-IF in TX mode.

Table 6.2: Performance Summary of *Q*-band Bidirectional Transceiver

Transmit Mode		
Conversion Gain	35 dB	
3-dB Bandwidth	4 GHz (41.7~45.7 GHz)	
Matching	RF	< -15 dB
	LO	< -17 dB
	IF	< -10 dB
OP1dB	8.5 dBm	
PAE	13.7% (PA)/ 7.5% (Sys)	
Power Consumption	PA	65.3 mW
	Mixer	0 mW
	Doubler	14.4 mW
	LO Amp	14 mW
	IF Amp	25.7 mW
	Total	119.4 mW

Receive Mode		
Conversion Gain	34 dB	
3-dB Bandwidth	3 GHz (41.8~44.8 GHz)	
Matching	RF	< -15 dB
	LO	< -20 dB
	IF	< -17 dB
Noise Figure	4.7 dB	
OP1dB/IIP3	-5 dBm/ -26.3 dBm	
Power Consumption	LNA	10.8 mW
	Mixer	0 mW
	Doubler	14.4 mW
	LO Amp	14 mW
	IF Amp	14.6 mW
	Total	54 mW

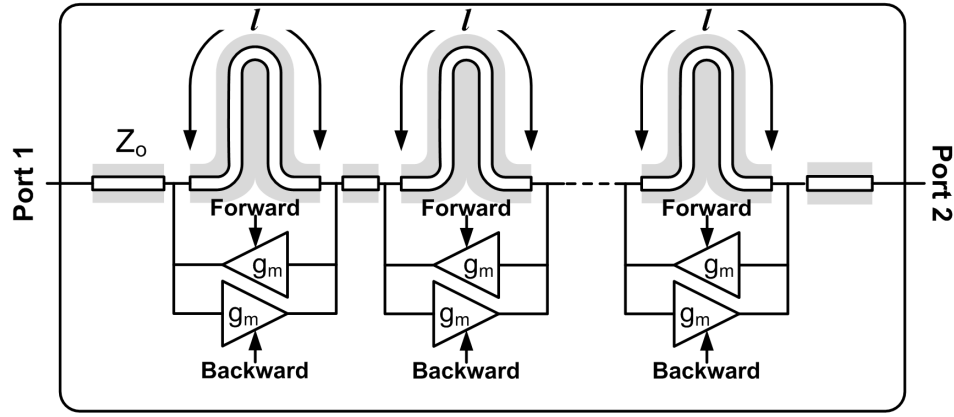


Figure 6.28: Schematic of the Bidirectional Constructive Wave Amplifier

in Table I. PAE of the transceiver in TX mode is 7.5 %.

The isolation between RF and LO ports is better than 50 dB as shown in Fig. 6.27. The excellent isolation occurs because the LO frequency is one-half of the frequency used for frequency conversion and the balun networks indicate excellent gain and phase matching. At 43 GHz, the RF to IF isolation is 50 dB.

6.5 Bidirectional Constructive Wave Amplifier

Using the constructive wave amplifier technique discussed in Chapter 5, a W -band, bidirectional constructive wave amplifier is demonstrated to allow amplification in one of two directions. The proposed bidirectional constructive wave amplifier is shown in Fig. 6.28. The architecture is based on the recently proposed cascaded constructive wave amplifier [70]. The prior work incorporated only one feedback amplifier to amplify the traveling wave in only one direction. Here, we demonstrate a bidirectional constructive wave amplifier circuit that incorporates two anti-parallel feedback amplifiers sharing a common transmission line. Only one of the feedback amplifiers operates at a time which obviates the need for a switch between the LNA and the PA.

Each amplifier stage consists of a transmission line of length, θ , with a feedback amplifier modeled as a transconductance, $g_m e^{-j\omega T_d}$, that is modulated

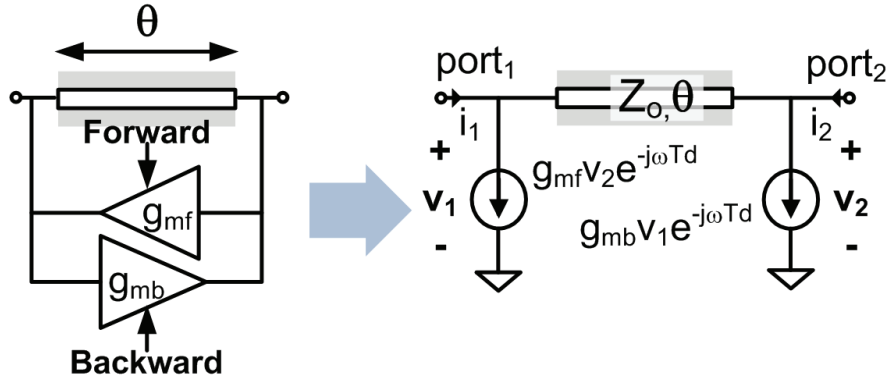


Figure 6.29: Small-signal model for a single stage.

by the traveling wave at the output of the stage [69]. The small-signal model is illustrated in Fig. 6.29. The local feedback at each stage injects current into the traveling wave at the input of the stage. The forward amplifier, A_F , is activated to amplify the forward traveling wave ($|S_{21}| > 1$). In this case the backward amplifier is nulled ($A_B = 0$). The backward amplifier, A_B , is activated to amplify the backward traveling wave ($|S_{12}| > 1$) and the forward amplifier is nulled ($A_F = 0$).

6.5.1 Gain/Isolation Analysis

The frequency response of this amplifier depends on the relative phase through the transmission line, θ , and the time delay through the feedback circuit, T_d . Constructive interference of the forward traveling wave and destructive interference of the backward traveling wave occurs when $\theta + \omega T_d = \pi$ and $\theta - \omega T_d = 0$ [69]. This condition is satisfied at the center frequency of the amplifier defined by $f_o = \frac{1}{4T_d}$. For a center frequency of 92 GHz, the feedback delay amounts to around 2.7 ps of delay.

The feedback voltage gain is determined by the product of the transconductance and the transmission line impedance. The forward feedback voltage gain is defined as $A_F = 0.5 \cdot g_{mf} Z_o$ and the backward feedback gain is $A_B = 0.5 \cdot g_{mb} Z_o$, where g_{mf} and g_{mb} are shown in Fig 6.29. At the center frequency f_o , the forward and backward S -parameters are simply expressed as a function of the forward and

backward feedback amplifier gains;

$$S_{21} = \frac{(1 - 2A_B)}{1 - (A_F + A_B)} \quad (6.11a)$$

$$S_{12} = \frac{(1 - 2A_F)}{1 - (A_F + A_B)}. \quad (6.11b)$$

To select the direction of amplification the feedback amplifiers are exclusively turned on. For forward wave amplification, the feedback amplifier, A_F , is active ($A_F > 0$) and A_B is nulled ($A_B = 0$). Therefore, $S_{21} = \frac{1}{1-A_F}$ and $S_{12} = \frac{(1-2A_F)}{1-A_F}$. If we assume that $A_F = \frac{1}{4}$, the forward traveling wave is amplified by 2.5 dB while the backward traveling wave is attenuated by 3.5 dB.

For backward wave amplification, A_B is active and A_F is nulled and the prior arguments are symmetric. By cascading multiple stages of the simple traveling wave amplifier stage in Fig. 6.29, the overall gain and attenuation can be quite large. For a 10-stage amplifier, the amplification can be 25 dB while the isolation can be 35 dB. Consequently, the bidirectional amplifier can be shown to be unconditionally stable in a half-duplex front-end.

6.5.2 Return Loss Analysis

A final critical feature of the bidirectional constructive wave amplifier is input and output matching under both modes of operation. At the center frequency of the response f_o , the input and output return loss is expressed in terms of the feedback voltage gain;

$$S_{11} = \frac{A_F + A_B}{1 - (A_F + A_B)}. \quad (6.12a)$$

$$S_{22} = \frac{A_F + A_B}{1 - (A_F + A_B)}. \quad (6.12b)$$

Interestingly, the expressions for the input and output matching are identical because the forward and backward feedback gains sum together. Consequently, a unique feature of the bidirectional constructive wave amplifier is the matching of the amplifier should be nearly identical in the forward and backward direction.

Notably, the value of the feedback gain sets the minimum return loss. If, for instance, the feedback gain is $A_F = \frac{1}{4}$, the input return loss 9.5 dB. Consequently, the feedback gain cannot be set to a larger value than one-quarter to maintain acceptable input and output matching [69].

6.6 Circuit Design

Fig. 6.30 illustrates the schematic for a single bidirectional constructive wave amplifier stage in the BiCMOS technology as well as common biasing circuits. The circuit implementation consists of ten identical cascaded bidirectional amplifier stages. Each stage has an emitter follower, Q_1 , and current source consisting of Q_4 and R_E . The emitter width of Q_1 is $1.5 \mu\text{m}$. The emitter follower feeds the signal to both the forward and backward amplifiers consisting of HBTs, Q_2 and Q_3 , and NMOS transistors, M_2 and M_4 , respectively. The NMOS devices are biased in the triode region to provide a voltage controlled degeneration resistance for the common emitter HBTs. Two separate current mirrors are provided to bias the gate of M_2 and M_4 independently from an off-chip current source for testing.

The proposed approach requires twice the transmission line length to distribute the forward and backward amplifiers but reduces parasitic loading from the active devices by distributing these amplifiers. Each transmission line is implemented as a shielded microstrip to prevent interstage coupling and is $200 \mu\text{m}$ long. The characteristic impedance of the transmission line is 45Ω for improved input and output return losses [69].

Simulations of the proposed circuit response are shown in Fig. 6.31 for forward amplification. The peak gain is predicted to be 22 dB at 94 GHz. The isolation is 28 dB at 94 GHz. The input return loss is better than 9 dB from 60 to 120 GHz and the output return loss is better than 13 dB over the same frequency range. Simulation of the backward amplification produces symmetric results with similar performance.

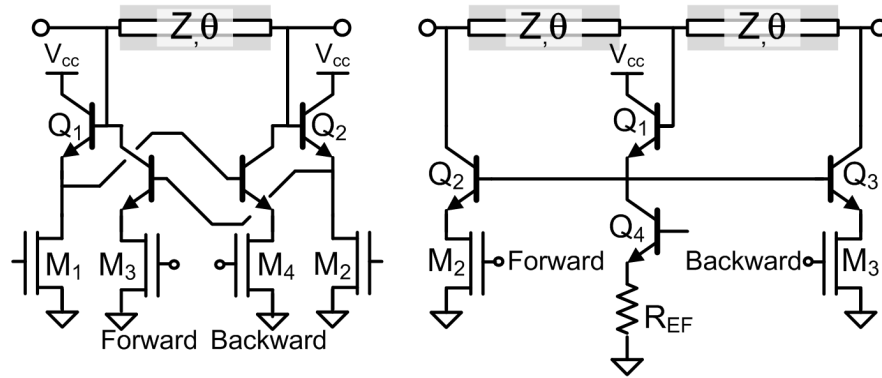


Figure 6.30: BiCMOS circuit implementation of the bidirectional amplifier cell.

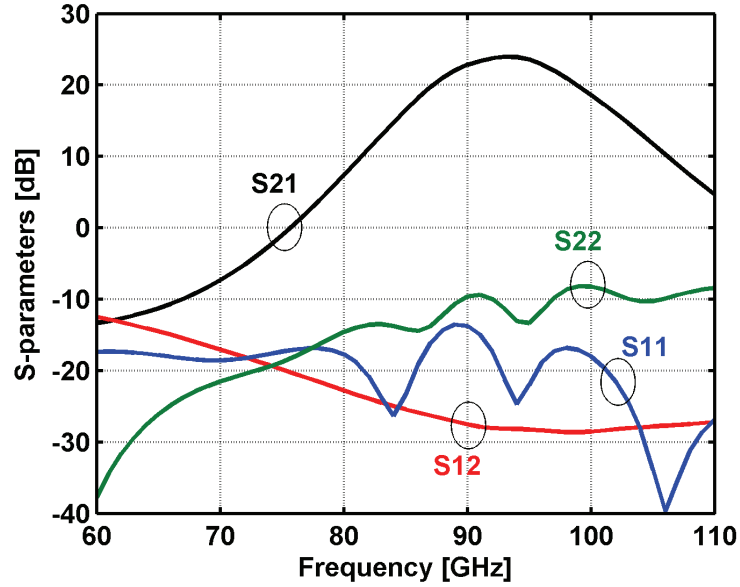


Figure 6.31: Spectre Simulations of the S -parameters for Forward Amplification.

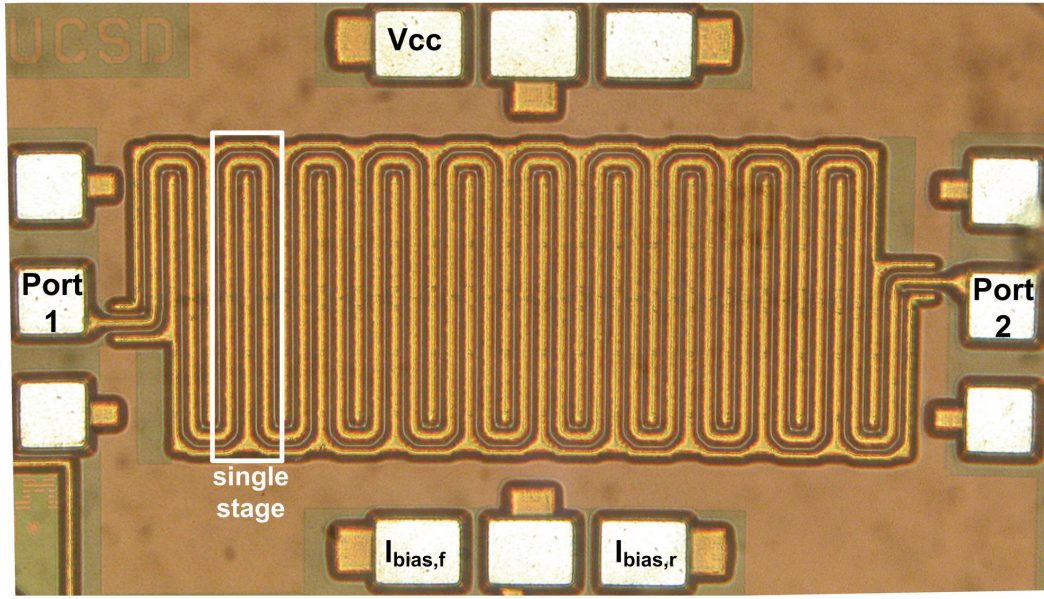


Figure 6.32: Microphotograph of the BCWA implemented in a 0.12- μm SiGe BiCMOS process.

6.7 Measurement Results

The BCWA is fabricated in a 0.12- μm SiGe BiCMOS ($f_T = 200$ GHz) process and the microphotograph is shown in Fig. 6.32. The circuit measures 520 μm by 905 μm including pads for a total area of 0.47 mm^2 .

The nominal bias conditions are $V_{cc} = 2$ V, $V_{bias} = 2$ V, $I_{bias} = 2$ mA, $I_{bias,f} = 1.86$ mA, and $I_{bias,r} = 0$ mA for forward amplification. The current consumption through the ten emitter followers is 15.9 mA from the 2 V supply (approximately 1.6 mA per stage) and the current consumption for the ten common emitter stages is 17 mA from the 2 V supply. The total power consumption under nominal conditions is 65.8 mW.

Small signal characteristics of the BCWA are measured at room temperature. The measurement are performed with Cascade ACP110-LW GSG probes and the Agilent E8361A two-port network analyzer with N5260A mm Wave controller. The measured S -parameters for forward and backward amplification are plotted in Figures 6.33 and 6.34.

For forward amplification, the measured S_{21} demonstrates a peak gain of

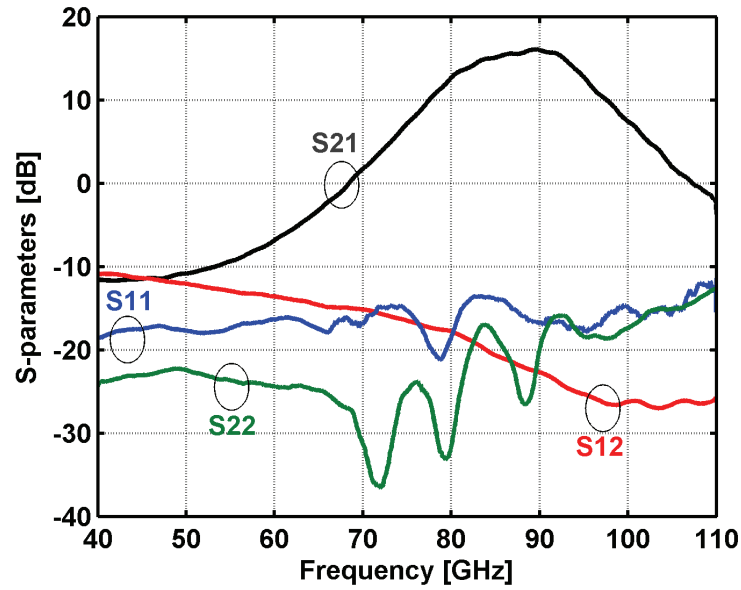


Figure 6.33: Measured S -parameters for Forward Amplification in the BCWA implemented in the BCWA implemented in a 0.12- μm SiGe BiCMOS process.

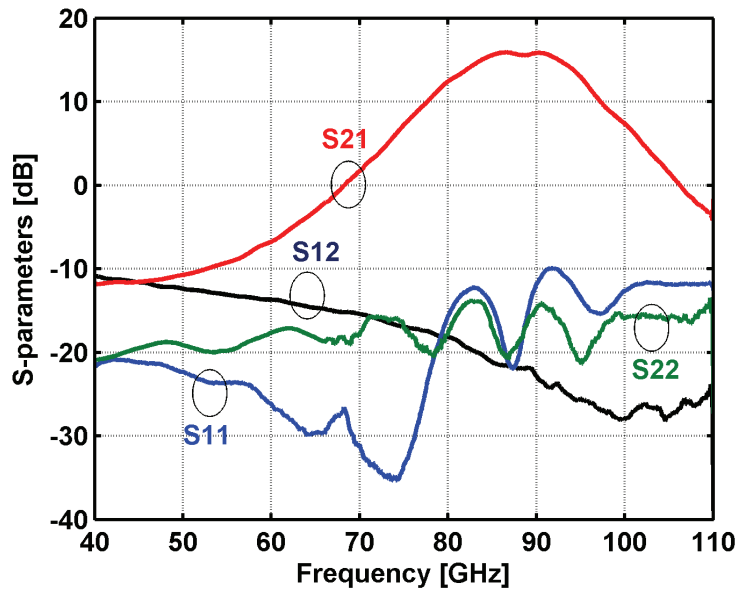


Figure 6.34: Measured S -parameters for Backward Amplification in the BCWA implemented in a 0.12- μm SiGe BiCMOS process.

16 dB at 90 GHz. The 3-dB bandwidth of the response is 14.5 GHz. The measured isolation (S_{12}) is 22 dB at 90 GHz. The input return loss (S_{11}) is better than 13 dB from 40 to 110 GHz and output return loss (S_{22}) is better than 16 dB over the same range.

For backward amplification at the similar bias conditions, the measured S_{12} demonstrates peak gain of 16 dB at 90 GHz and the measured isolation (S_{21}) is 22 dB at 90 GHz and the isolation (S_{21}) is 22 dB at 90 GHz. The output return loss (S_{11}) is higher but remains below 10 dB from 40 to 110 GHz. The input return loss (S_{22}) is better than 15 dB over the same frequency range. Therefore, symmetric performance has been demonstrated for both forward and backward amplification.

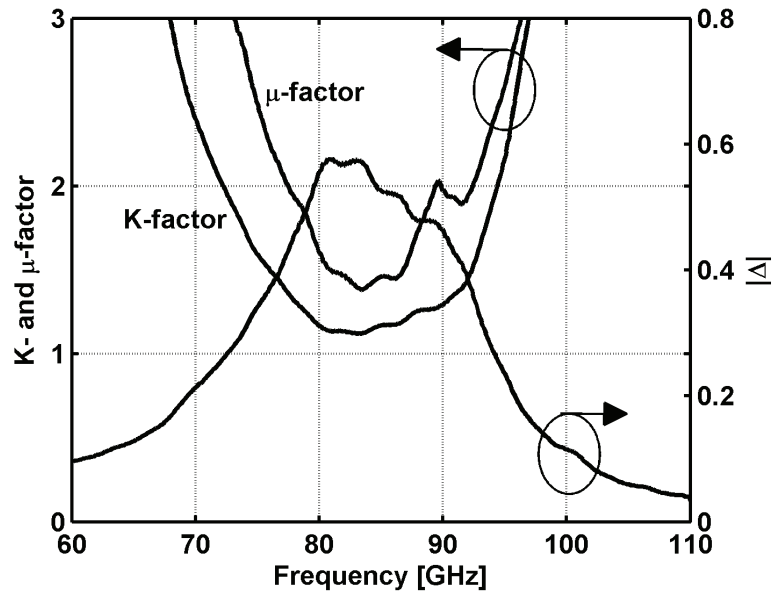


Figure 6.35: Measured stability factors of the TCWPA

Fig. 6.35 shows the stability of the proposed BCWA and indicates unconditional stability over the entire W -band.

An additional feature of the implemented circuit is that the passband of the frequency response is tuned with the bias voltage of the NMOS emitter degeneration. By increasing the bias current, $I_{bias,f}$, the gate-source voltage of the diode connected reference NMOS in Fig. 6.30 increases and reduces the channel resis-

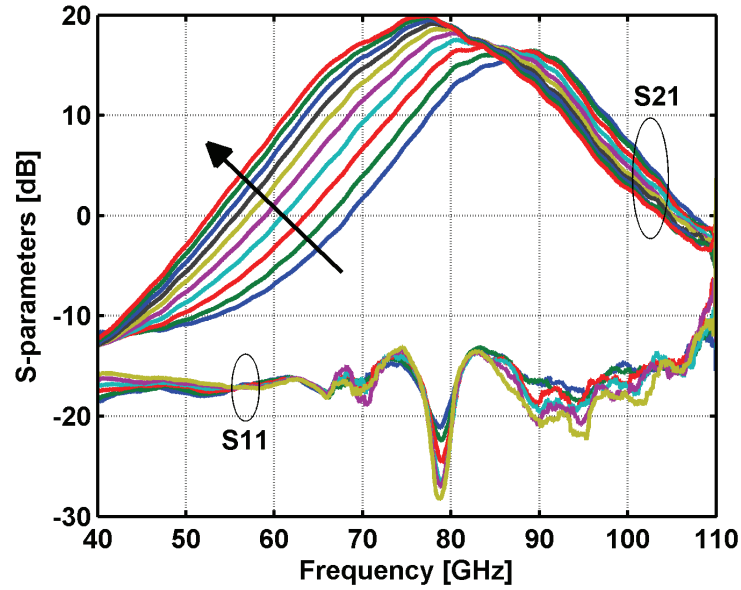


Figure 6.36: Tunable Response of the Forward Path

tance of the NMOS device. The reduced channel resistance increases the feedback voltage gain of each stage and the forward gain increases to 20 dB.

However, the reduced emitter degeneration introduces more delay through the feedback path and the center frequency of the amplifier moves to a lower frequency. The tunable frequency response is plotted in Fig. 6.36. From the nominal bias at $I_{bias,f} = 1.86$ mA, increasing the bias current to 7.39 mA shifts the center frequency down to 77 GHz while the peak gain increases to 20 dB. The increasing bias current is only changing the gate source voltage of the NMOS degeneration and does not significantly change the power consumption of the stage of the circuit. The input return loss is also plotted in Fig. 6.36 under the bias current variation. The input return loss is relatively insensitive to the changes in the bias current and remains better than 13 dB from 40–110 GHz regardless of the location of the peak gain.

The power consumption through the emitter follower is 15.9 mA from a 2 V supply (approximately 1.6 mA per stage) and 17 mA from a 2 V supply for the common emitter stages. The total power consumption under nominal operating

conditions is 65.8 mW.

6.8 Conclusions

A switchless, bidirectional millimeter-wave (40–45GHz) transceiver circuit has been demonstrated in 0.12- μm SiGe BiCMOS. The bidirectional behavior is realized using an integrated PALNA circuit that can realize better sensitivity and power handling than an integrated millimeter wave switch. The TX and RX conversion gain is better than 34 dB, the RX noise figure is 4.7 dB, and the TX saturated output power is better than 9.5 dBm.

A 77- to 90-GHz bidirectional constructive wave amplifier is demonstrated in a 0.12- μm SiGe HBT process. The amplifier demonstrates a peak gain of 16 dB and 3-dB BW of 14.5GHz and can be electronically controlled to offer similar performance in the forward and backward directions. The chip occupies an area of 0.47 mm^2 , achieving a significant size advantages for *W*-band front-ends. To the author's knowledge, this represents the first fully integrated bidirectional amplifier demonstrated at *W*-band.

Acknowledgments

Chapter 6 is in part mostly a reprint of the material as it appears in IEEE Bipolar / BiCMOS Circuits and Technology Meeting, 2010, Joohwa Kim; James F. Buckwalter, and is in part mostly a reprint of the material as it appears in IEEE Custom Integrated Circuits Conference, J. Kim, M. Parlak, and J. F. Buckwalter, and in part, also has been submitted for publication of the material as it will appear in IEEE Journal of Solid-State Circuits, 2011, Joohwa Kim; James F. Buckwalter. The dissertation author was the primary author of these materials.

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Chapter 7

Conclusions

This dissertation presented 40-Gb/s to 160-Gb/s low power receivers and transmitters using 0.13- μm CMOS, 0.12- μm SiGe BiCMOS and 45 nm SOI CMOS technologies. First, a compact low group-delay 40-Gb/s TIA with post amplifier was demonstrated. A transimpedance limit for multistage TIAs was derived, and a bandwidth-enhancement technique while avoiding large group-delay variation using inductive-series π -networks was analyzed. Next, low power 40-Gb/s SOI CMOS transceiver was presented. To overcome circuit design issues for high-speed optical front-ends described in Section 1.1.2 several design techniques are explored that can enable the implementation of both 40-Gb/s receiver and transmitter in highly scaled CMOS technology. A new bandwidth enhancement scheme was proposed in the later part to achieve 100–160-Gb/s optical data rate and the 3-dB bandwidth of 102-GHz with a gain ripple of less than 1.5 dB was achieved. A 92-GHz distributed amplifier was also demonstrated and can be used for 100-Gb/s main amplifier.

In the second part of this dissertation, the new high-frequency amplifier topology (CCWA) was introduced based on traveling-wave amplification and it provides high- and broadband-gain and broadband-matching performances. The millimeter-wave bidirectional transceiver architecture was proposed to improve the performance of the conventional half-duplex transceiver. A fully integrated Q -band switchless bidirectional transceiver was demonstrated using 0.12- μm SiGe BiCMOS technology. Additionally, CCWA topology was also used to demonstrate

the bidirectional operation scheme at W -band.

Chapter 2 described the transimpedance limit which is a powerful concept revealing the tradeoffs between transimpedance, bandwidth, and technology of a transimpedance amplifier (TIA). A 40-Gb/s TIA with post amplifiers was presented using multistage inductive-series peaking for low group delay variation. Next, A bandwidth enhancement technique using inductive-series π -networks was analyzed. A design method for low group delay constrained to 3 dB bandwidth enhancement was suggested. The TIA was demonstrated in a 0.13 μm CMOS process and achieved a 3-dB bandwidth of 29 GHz. The transimpedance gain was 50 dB Ω and the transimpedance group delay variation was less than 16 ps over the 3-dB bandwidth. The chip occupied an area of 0.4 mm² including the pads and consumes 45.7 mW from a 1.5 V supply. The measured TIA demonstrated a transimpedance figure of merit of 200.7 Ω/pJ .

Chapter 3 presented a low-power 40-Gb/s SOI tranceiver front-ends which include TIA, main amplifier and single-ended/differential 50 $\cdot\Omega$ modulator drivers. A modulator driver uses floating body devices to realize differential voltage swing of more than 4.5 V_{PP} with a single-ended small-signal gain of 7.6 dB over 33 GHz. The optical receiver consisted of a TIA and post-amplifier with 55-dB $\cdot\Omega$ of transimpedance over 30 GHz. The group-delay variation is ± 3.9 ps over the 3-dB bandwidth and the average input-referred noise density is 20.47 $\text{pA}/\sqrt{\text{Hz}}$. The TIA consumed 9 mW from a 1 V supply for a transimpedance figure of merit of 1874.5 Ω/pJ .

Chapter 4 presented low-power 100–160-Gb/s receivers. 160-Gb/s receiver was realized with cascaded stagger-tuned stages that are equalized for high bandwidth and low gain ripple. The staggered frequency response was demonstrated to improve the transimpedance limit of active circuits. The staggered response was demonstrated with a Darlington feedback amplifier and a constructive wave amplifier, which achieves low group delay. The broadband amplifier was demonstrated in a 0.12- μm SiGe BiCMOS process and achieved a 3-dB bandwidth of 102 GHz. The gain was 10 dB with 1.5 dB gain-ripple and group-delay variation under ± 6 ps over the entire 3-dB bandwidth. The chip occupied an area of 0.29

mm² including the pads and consumes 73 mW from a 2 V supply. In addition, a low-power cascode distributed amplifier was demonstrated in a 45-nm SOI CMOS process. The amplifier was suitable for more than 100-Gb/s main amplifier. The amplifier achieved a 3-dB bandwidth of 92 GHz. The peak gain was 9-dB with a gain-ripple of less 1.5 dB over the 3-dB bandwidth. The group-delay variation was under ± 4.7 ps over the 3-dB bandwidth. The amplifier consumed 73.5 mW from a 1.2 V supply and results in a gain-bandwidth efficiency figure of merit of 3.53 GHz/mW. The chip occupied an area of 0.45 mm² including the pads.

In chapter 5, a wideband, high-frequency amplifier technique was introduced based on traveling wave amplification. The behavior of the CCWA was analyzed in terms of gain, bandwidth, stability, and noise figure. Using CCWA topology, the *W*-band (75-111GHz) amplifiers were demonstrated in a 0.12- μ m SiGe BiCMOS process with multi cascaded amplification stages achieved 37.5-dB gain at 90 GHz with a 3-dB bandwidth of 14.6 GHz. Consequently, this amplifier demonstrated a gain-bandwidth product as high as 1,095 GHz. At nominal bias condition, input and output return losses were better than 11 dB over the entire 3-dB bandwidth and the amplifier consumes 65 mW from a 1.8 V. The chip occupied an area of 0.39 mm² including the pads. The amplifiers can potentially be used for medical and security imaging, as well as high capacity wireless communications at *W*-band frequencies. To the author's knowledge, this represents a record for an amplifier demonstrated in silicon/silicongermanium processes.

In chapter 6, a fully integrated *Q*-band (40~45 GHz) bidirectional transceiver was demonstrated in a 0.12- μ m SiGe BiCMOS technology. The RF front-end design eliminated the need for transmit/receive switches by demonstrating a novel PA/LNA circuit. The transceiver had a transmit conversion gain of 35 dB with a 3-dB bandwidth of 4 GHz. The OP1dB was 8.5 dBm and Psat was 9.5 dBm. The transceiver had a receive conversion gain of 34 dB with a 3-dB bandwidth of 3 GHz. The noise figure was 4.7 dB and OP1dB was -5 dBm at 43 GHz. The chip consumed 119.4 mW when transmitting and 54 mW when receiving, and overall chip size was 1.6 mm $\times$ 0.8 mm including pads. To the author's knowledge, this work represents the first switchless millimeter-wave bidirectional transceiver in a

CMOS or BiCMOS processes.

In this chapter, a *W*-band, bidirectional constructive wave amplifier was also demonstrated in a $0.12\text{-}\mu\text{m}$ SiGe BiCMOS technology. The amplifier allowed symmetric amplification in one of two directions. The amplifier had a peak gain of 16 dB and bandwidth of 14.5 GHz. The center frequency was electronically controlled between 77 and 94 GHz. The amplifier was illustrated to remain stable over all operating conditions. The circuit operated from a 2 V supply and consumes approximately 32 mA under nominal conditions. The full integrated circuit occupies an area of 0.8mm^2 . To the author's knowledge, this represents the first bidirectional amplifier at *W*-band in a CMOS or BiCMOS processes.

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