Title

Shielded piezoresistive cantilever probes for nanoscale topography and electrical imaging

Journal

Journal of Micromechanics and Microengineering, 24(4)

ISSN

0960-1317

Authors

Yang, Yongliang
Yue, Eric
Cui, Yong-Tao
et al.

Publication Date

2014-04-01

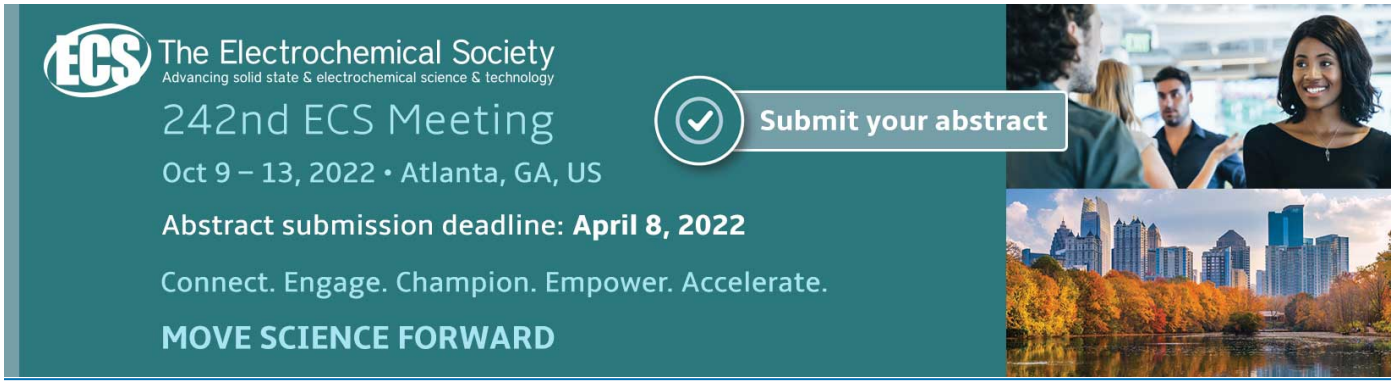
DOI

10.1088/0960-1317/24/4/045026

Peer reviewed

PAPER

Shielded piezoresistive cantilever probes for nanoscale topography and electrical imaging



IOP Publishing Journal of Micromechanics and Microengineering
J. Micromech. Microeng. **24** (2014) 045026 (7pp) doi:10.1088/0960-1317/24/4/045026

Shielded piezoresistive cantilever probes for nanoscale topography and electrical imaging

Yongliang Yang[1], Eric Yue Ma[1], Yong-Tao Cui[1], Alexandre Haemmerli[2], Keji Lai[1,3], Worasom Kundhikanjana[1,4], Nahid Harjee[2], Beth L Pruitt[2], Michael Kelly[1] and Zhi-Xun Shen[1]

[1] Department of Applied Physics and Geballe Laboratory for Advanced Materials, Stanford University, Stanford, CA 94305, USA
[2] Mechanical Engineering, Stanford University, Stanford, CA 94305, USA
[3] Department of Physics, University of Texas at Austin, Austin, TX 78712, USA
[4] School of Physics, Institute of Science, Suranaree University of Technology, Nakron Ratchasima, 30000, Thailand

E-mail: zxshen@stanford.edu

Received 18 December 2013, revised 12 February 2014
Accepted for publication 24 February 2014
Published 25 March 2014

Abstract

This paper presents the design and fabrication of piezoresistive cantilever probes for microwave impedance microscopy (MIM) to enable simultaneous topographic and electrical imaging. Plasma enhanced chemical vapor deposited Si_3N_4 cantilevers with a shielded center conductor line and nanoscale conductive tip apex are batch fabricated on silicon-on-insulator wafers. Doped silicon piezoresistors are integrated at the root of the cantilevers to sense their deformation. The piezoresistive sensitivity is 2 nm for a bandwidth of 10 kHz, enabling topographical imaging with reasonable speed. The aluminum center conductor has a low resistance (less than 5 Ω) and small capacitance (∼1.7 pF) to ground; these parameters are critical for high sensitivity MIM imaging. High quality piezoresistive topography and MIM images are simultaneously obtained with the fabricated probes at ambient and cryogenic temperatures. These new piezoresistive probes remarkably broaden the horizon of MIM for scientific applications by operating with an integrated feedback mechanism at low temperature and for photosensitive samples.

Keywords: MEMS, cantilever, probe

(Some figures may appear in colour only in the online journal)

1. Introduction

Microwave impedance microscopy (MIM) is now established as an indispensable tool to study nanoscale dielectric and conductive properties of materials [1]. As shown in figure 1, GHz microwave signals are guided to a conductive tip and interact with the materials beneath the tip apex. The reflected signals, which contain local electrical information of the sample, are amplified and demodulated to form MIM-Im (imaginary component) and MIM-Re (real component) images. This technique enables direct visualization of the nanoscale complex permittivity [2, 3] under ambient [4] or low temperatures [5]; it has already found application in the study of fundamental problems in electron physics [6–8] and material science [9].

Height control feedback is essential for scanning probe microscopy (SPM) because it regulates the tip–sample interaction, prevents tip crash, and provides topographic information of the sample surface. The room temperature MIM is usually implemented on a commercial atomic force microscope (AFM) to take advantage of the conventional laser beam feedback [1–4, 9]. A major drawback of laser feedback is the influence of stray light on photo-sensitive materials. In addition, height control feedback inside cryogenic chambers

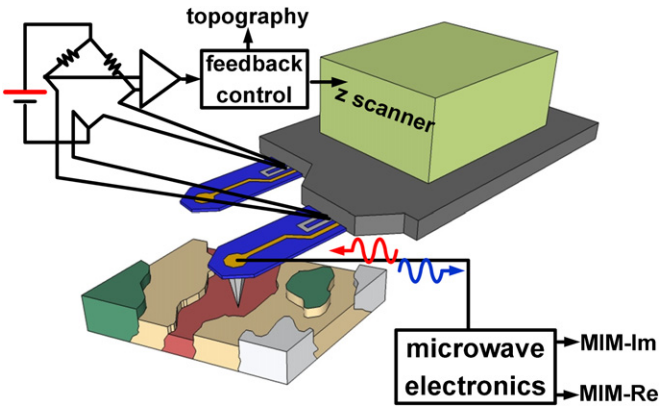


Figure 1. Schematic of MIM setup and designed piezoresistive cantilever probe. Two on-chip heavily doped Si piezoresistors, one on the cantilever and the other as a background reference, are connected into a Wheatstone bridge circuit for the detection of cantilever deformation that provides feedback to the z-scanner. Microwave electronics connected to the heavily doped silicon tip detect tip–sample impedance and output it as MIM-Im (imaginary-component) and MIM-Re (real-component).

is not trivial due to limited setup space. Here, we implement a non-optical feedback scheme to provide topographic information during the MIM measurement and to minimize tip crashes, thus preserving tip sharpness.

Piezoresistive sensing is an established feedback mechanism for contact mode SPM [10]. However, integration of a piezoresistor on MIM probes is a challenging task. First, the fabrication of a piezoresistive element should be compatible with batch process of sharp conductive tip apex, which sets the MIM spatial resolution [4]. Second, a low-resistance metallic path from the bonding pad (for signal input/output) to the tip apex is needed to minimize the loss. The background capacitance between this signal line and the ground should also be kept small for better electrical sensitivity. Third, the signal line should be electrically shielded to reduce the stray fields and noise pickup. In other words, the center conductor should be surrounded by dielectrics and then shield metals. Finally, such a sandwich structure with stacking metal/dielectric layers is highly susceptible to bimorph bending [11]. Thus, the stresses and thermal expansions of different layers must be balanced such that the cantilever remains straight over the variable temperature range. The MIM probes produced so far show good electrical and mechanical performance but no piezoresistive element [12, 13]. We previously reported piezoresistive probes with doped n-type silicon piezoresistors on p-type silicon device layer of SOI wafers. Those probes exhibited a vertical displacement resolution of 3.5 nm at 10 kHz bandwidth. The un-optimized center conductor and dielectric layers resulted in large resistance (32 Ω) and capacitance (9.5 pF), which were unfortunately too large for the MIM [14].

In this work, we report novel batch-processed low impedance, well-shielded piezoresistive cantilever probes. SOI wafers with low resistive n-type silicon are used as starting material. Piezoresistors fabricated by thinning the n-type silicon device layer are integrated on plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 cantilever to detect the deformation due to tip–sample contact force. Capsulated by SiO_2, the piezoresistors show low noise and the height resolution is 2 nm in a 10 kHz band, which enables high quality topographic imaging. A shielded aluminum center conductor connects the sharp silicon tip to a bond pad on the die handle. With the optimized center conductor and dielectric layers, the resistance of the center conductor is less than 5 Ω and the capacitance between the center conductor and outer shield is 1.7 pF. These low resistance and capacitance values are critical for high sensitivity MIM imaging. The optimized cantilever structure also ensures the cantilever to be flat at variety temperatures. Using these new piezoresistive microwave probes, high quality topographic and MIM images are simultaneously obtained under both ambient and cryogenic temperatures.

2. Probe design and fabrication

A schematic of the designed piezoresistive cantilever microwave probe is shown in figure 1. The main body of the cantilever is made of PECVD Si_3N_4. A heavily doped

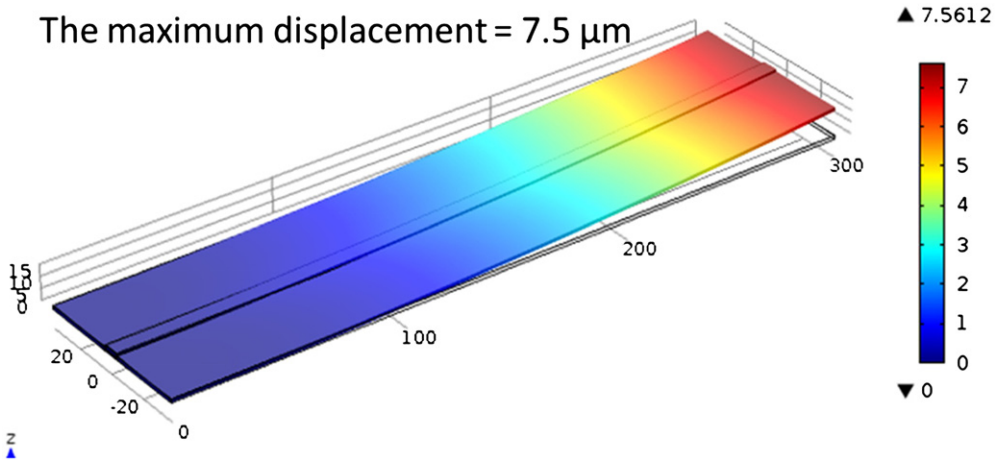


Figure 2. Simulated displacement of the cantilever when the temperature drops from 20 °C to −196 °C. The cantilever free end only moves 7.5 μm, which is small enough to meet the requirement for low temperature scanning.

n-type silicon tip is integrated on the cantilever free end. The aluminum center conductor connects the tip to a wire bond pad to guide microwave signals to and from the tip. The cantilever front side (tip side) is covered by an Al shield layer, which is electrically grounded in the microwave measurements to suppress noise pickup. Two on-chip heavily doped Si piezoresistors, one on the cantilever and the other as a background reference, are connected into a Wheatstone bridge circuit for the detection of cantilever deformation that provides feedback to the z-scanner.

In the probe design, we minimized both the series resistance (R_s) of the center conductor and its capacitance (C_{tip}) to ground. The small R_s decreases the loss in the signal line and increases the sensitivity. In our case, the thick center conductor (1 μm Al) and optimized conductor path width (6 μm on the cantilever and 15 μm on the chip) keep the R_s small. In MIM, the tip–sample interaction is essentially a tiny modulation to the tip capacitance. We have used a sufficiently thick dielectric (1.5 μm Si_3N_4) and optimized conductor path width to minimize C_{tip}.

For a cantilever with multiple layers and different materials, it is important to balance the mechanical and thermal stresses to keep it straight at variable temperatures. In our design, Al metal and Si_3N_4 with low stress are used to minimize the internal stress at the room temperature. The shape and thickness of Al center conductor and Si_3N_4 dielectric layers are optimized for small resistance and capacitance. The only tunable layer is the metal shield. We used COMSOL finite element modeling (FEM) simulation to optimize the shield metal thickness. A 100 nm Al shield was chosen to obtain low thermal stress and with conformal electrical shielding capability. Figure 2 shows the simulated displacement of cantilever when the temperature drops from 20 °C to −196 °C. The cantilever free end only moves 7.5 μm, which is small enough to meet our requirements for low temperature scanning.

The probes are fabricated on (1 0 0) SOI wafers with an 8 μm device layer, 2 μm buried silicon dioxide (BOX), and 400 μm handle layer. The device layer and handle wafer are heavily doped n-type silicon with a resistivity of 0.001–0.0015 Ω•cm for low resistance and good Ohmic contact with Al. During the process, the wafers were rotated 45° to make the piezoresistors along ⟨1 0 0⟩ crystal direction and maximize the piezoresistive coefficient in n-type silicon [15].

The detailed fabrication processes are shown in figure 3. The starting material was SOI wafer (figure 3(*a*)). A 100 nm thermal SiO_2 was grown on the wafer and patterned with 15 μm × 15 μm square tip etch masks. The wafer was then etched in 45% KOH at 60 °C for about 30 min. Tall tips of 7 μm with uniform height were created by undercutting the oxide mask, with about 1 μm left in the remaining device layer (figure 3(*b*)). A second 100 nm SiO_2 layer was grown in a wet atmosphere at 950 °C to sharpen the tip apex. After patterning the SiO_2, the wafer was again etched in 45% KOH at 60 °C for about 5 min to form a stage around the tip and the piezoresistors. The thickness of the stage and piezoresistor is in the range of 0.5 to 1.5 μm due to the inhomogeneity of SOI device layer (figure 3(*c*)). The tips were further sharpened by growing a 200 nm thick oxide at 950 °C in a wet atmosphere (figure 3(*d*)), followed by the removal of the oxide on piezoresistor contact holes and the stage by buffered oxide etch (BOE). The oxide on the tip was kept to protect the apex during the following processes (figure 3(*e*)). A layer of 1 μm Al was deposited on the wafer and patterned into the center conductor, which connects the tip stage and bond pad on the chip to guide microwave signals. The dummy trace on the other side of the cantilever balances the lateral structure. Electrodes for the piezoresistors were also formed at the same process (figure 3(*f*)). A dielectric layer of 1.5 μm PECVD Si_3N_4 was then deposited and patterned as the cantilever body by reactive-ion etching (figure 3(*g*)). The front layer of 0.1 μm Al served as the shield was sputtered and patterned (figure 3(*h*)). Note

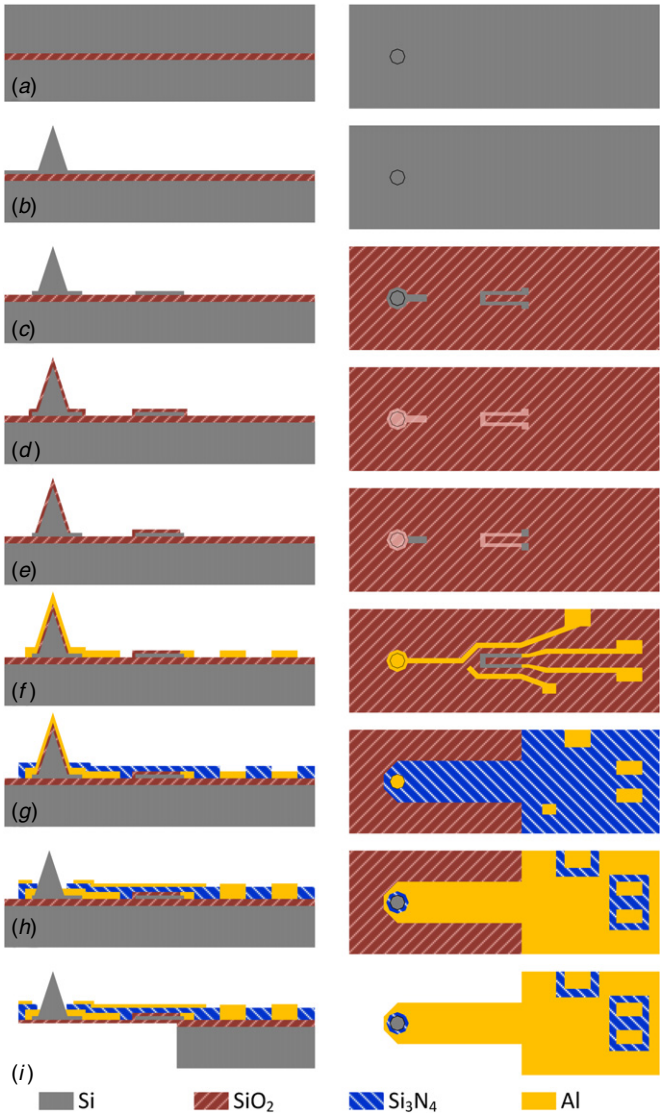


Figure 3. Fabrication processes. (*a*) Starting SOI wafer. (*b*) KOH etching to form the tip. (*c*) Pattern the piezoresistors. (*d*) Sharpen the tip by thermal oxidation at 950 °C in a wet atmosphere. (*e*) Open contact holes for piezoresistors and silicon tip. (*f*) Fabricate the center conductor and piezoresistor electrodes. (*g*) Deposit and pattern the Si_3N_4 to form the cantilever main body. (*h*) Deposit and pattern the shield. (*i*) Release the cantilever with DRIE and pad etching.

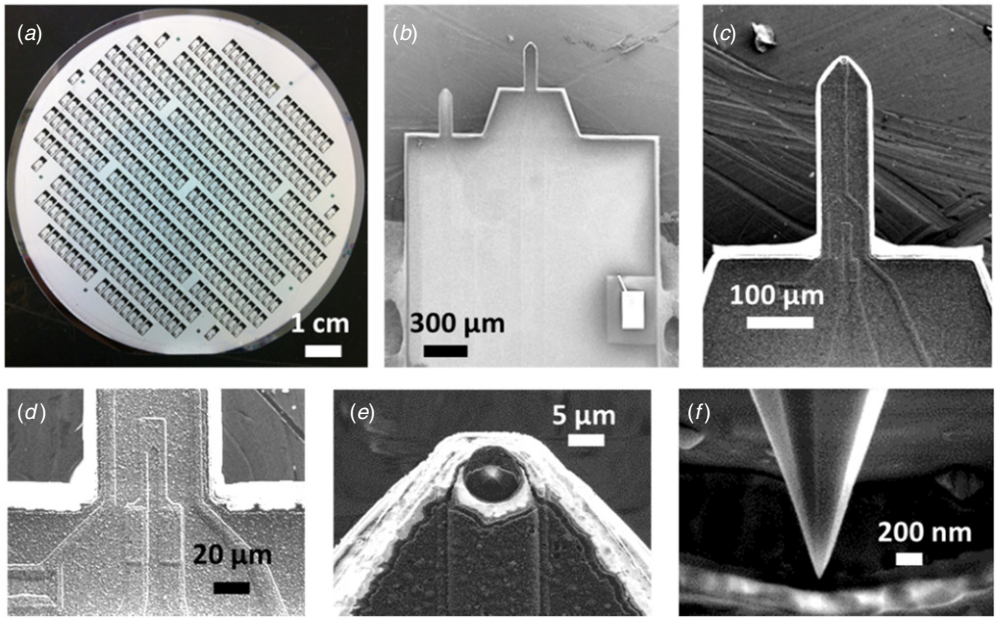


Figure 4. SEM images of the fabricated probe. (*a*) Finished 4″ wafer with hundreds of probes. (*b*) SEM image of the chip shows active and reference cantilevers, as well as the bond pad. (*c*) Full view of the MIM cantilever. (*d*) The piezoresistor at its root. (*e*) and (*f*) Close-up views of the tip demonstrate a sharp tip apex with a diameter less than 50 nm.

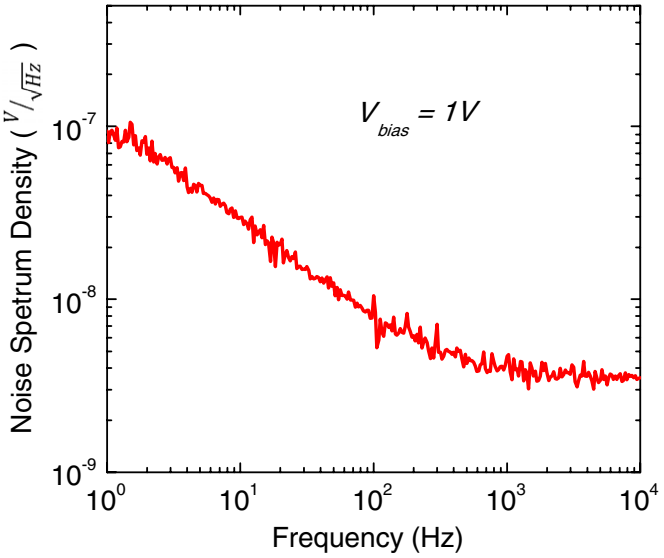


Figure 5. Measured noise spectrum of piezoresistors. The integrated noise is 428 nV from 1 Hz to 10 kHz is 428 nV at 1 V dc bias.

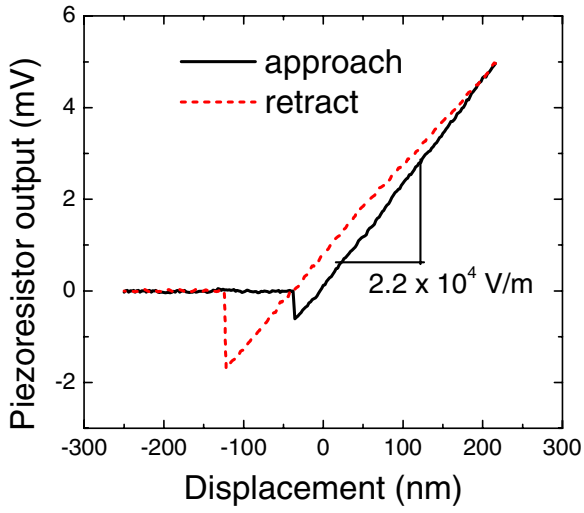


Figure 6. Piezoresistor output versus AFM z-scanner displacement in an approach–retract circle. The slope gives a sensitivity of 2.2 × 104 V m^{-1} with an amplifier gain of 100 and 1 V dc bias.

that the via–hole through the dielectric layer is to electrically ground the dummy wire to the shield, which is shown in the top views of figures 3(*f*)–(*h*). We then removed the Al and SiO_2 on the tip to expose the tip apex by Al etchant and pad etchant (SiO_2 etch rate = 35 nm min^{-1}), respectively. To release the cantilever probes, we spin coated both sides of the wafers with 7 μm photoresist, then patterned the back side and etched away the silicon underneath the cantilever by deep reactive ion etching (DRIE). The BOX layer was removed by pad etchant to complete the cantilever release (figure 3(*i*)). Finally, the probes are annealed in forming gas at 450 °C for 30 min to form Ohmic contacts between the heavy doped silicon and the Al center conductor. In the fabrication, 1 μm spin-coated photoresist was used during the patterning of tip etch masks (figure 3(*b*)) and 7 μm spin-coated photoresist was used after the tip formation by KOH etching, which created 7 μm steps on the wafer (figure 3(*c*)).

As shown in figure 4, hundreds of probes are batch fabricated on a 4 inch wafer (figure 4(*a*)). The dimensions are 3.4 mm × 1.6 mm for the chips and 300 μm × 75 μm for the cantilever. A scanning electron micrograph (SEM) in figure 4(*b*) displays active and reference cantilevers, as well as the bond pad. Figure 4(*c*) is a full view of the MIM cantilever and figure 4(*d*) shows the piezoresistor at its root. Close-up views of the tip in figures 4(*e*) and (*f*) demonstrate a sharp tip apex with a diameter less than 50 nm. The reference cantilever

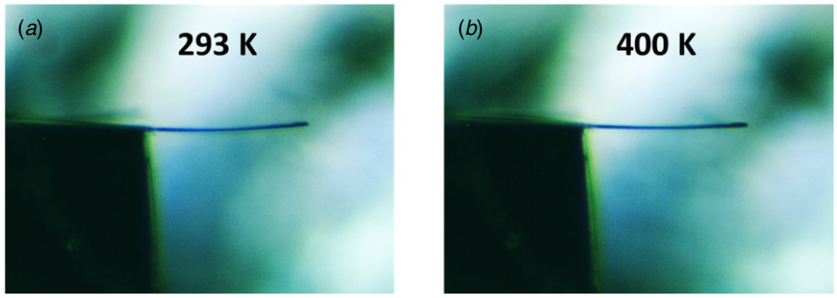


Figure 7. Side views of the cantilever at (*a*) room temperature (20 °C) and (*b*) 127 °C. The cantilever is reasonably flat at the room temperature and maintains its shape when heated to 127 °C.

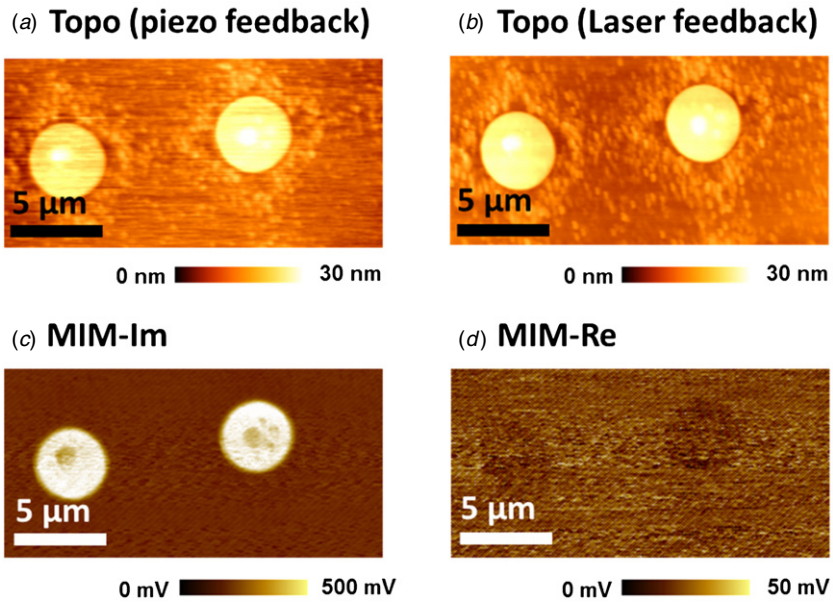


Figure 8. Testing results at the room temperature. The sample contains 10 nm tall Al dots on a silicon substrate with 100 nm SiO_2. Piezoresistive bridge outputs were used as feedback to control the displacement of the z-scanner and the topography image was obtained from the position of the z-scanner. (*a*) Topography obtained with piezoresistive feedback has the same quality as that obtained with traditional laser feedback in (*b*). (*c*) and (*d*) MIM images simultaneously recorded by microwave electronics show clear MIM-Im contrast between the conducting Al and insulating SiO_2.

has the same structure as the sensing cantilever except that it has no tip on the free end.

3. Testing results

The two on-chip piezoresistors were connected with two metal film resistors to form a Wheatstone bridge configuration. A 1 V dc bias was applied on the bridge and the output was amplified with an instrumentation amplifier, which has the bandwidth of 800 kHz and a very low noise that can be negligible during the testing. The amplified signal was then sent to the control circuit to provide feedback to the z-scanner. The piezoresistor on the reference cantilever balances the environment induced fluctuation and drift. The low frequency noise spectrum was measured by a signal analyzer HP3562A and the results are shown in figure 5. Bandwidth of 1 Hz to 10 kHz was chosen to match the AFM feedback loop bandwidth, which generally is around 10 kHz. The integrated noise from 1 Hz to 10 kHz at 1 V dc bias is:

$$V_{\text{noise}} = \sqrt{\int_{f=1\text{ Hz}}^{10000\text{ Hz}} [V(f)]^2\,\mathrm{d}f} = 428\text{ nV} \qquad (1)$$

where $V(f)$ is the measured noise spectrum density in figure 5.

To measure the displacement sensitivity, the probe was mounted on a Park XE-70 AFM system to approach a hard sample surface. The amplified bridge output versus AFM z-scanner displacement was measured, which shows a typical approach–retract curve (figure 6). The slope gives a sensitivity of 2.2×10^4 V m^{-1} with an amplifier gain of 100 and 1 V dc bias. The vertical resolution of the piezoresistive probe for a bandwidth of 10 kHz can be calculated:

$$\text{Res} = \frac{V_{\text{noise}}}{\text{Sensitivity}} = 2\text{ nm} \qquad (2)$$

Thanks to the optimized parameters of Al center conductor and Si_3N_4 dielectric, our probes show small R_s (measured less than 5 Ω) and C_{tip} (measured about 1.7 pF), much better than the doped Si trace in other reports [13]. The optimized cantilever structure not only minimizes the noise pickup and the topographic artifact, but also balances

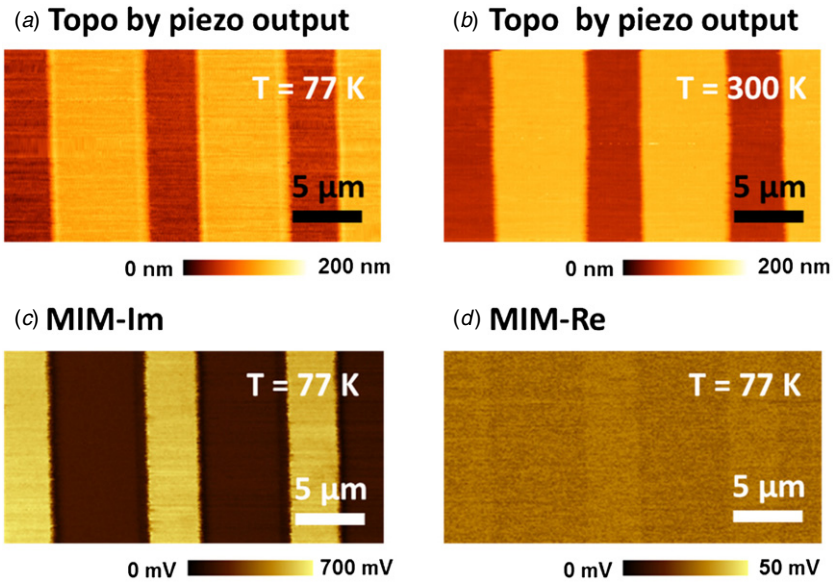


Figure 9. Testing results at low temperature. The sample is a 100 nm SiO_2/Si wafer, with the SiO_2 etched in a stripe pattern. (*a*) The topography image at −196 °C was directly recorded from the piezoresistive output and was comparable to that at room temperature in (*b*). (*c*) MIM-Im contrast reflects the tip–sample capacitance change between the 100 nm SiO_2 layer and native oxide on the etched regions. (*d*) No contrast is observed in the MIM-Re image, as expected for the insulating SiO_2 surface.

the stresses to keep the cantilever straight under variable temperatures. It is difficult to optically observe the cantilever shape at low temperature due to the complicated cryogenic system. So we heated the cantilever to be 127 °C to prove it. As shown in figure 7, the cantilever is reasonably flat at the room temperature and maintains its shape when being heated to 127 °C.

Results of simultaneous topographic and MIM imaging at the room temperature are shown in figure 8. The sample contains 10 nm tall Al dots on a silicon substrate with 100 nm SiO_2. In the scanning, we used piezoresistive bridge output as feedback to control the z-scanner displacement and the topography is obtained from the z-scanner position. The topography obtained by piezoresistive feedback (figure 8(*a*)) has the same quality as that obtained with traditional laser feedback (figure 8(*b*)). The MIM images (figures 8(*c*) and (*d*)) were simultaneously recorded by microwave electronics, showing clear MIM-Im contrast between the conducting Al and insulating SiO_2. Details about the analysis of MIM images can be found in [2–4, 13].

Figure 9 shows the results at cryogenic temperature (−196 °C). The scanning was done in Janis cryogenic cryostat based MIM setup, which is the sample as that in [4] except for the piezoresistive probe. The tip, sample as well as the scanners were placed in a vacuum tube with helium exchange gas. Then the tube was immersed in liquid nitrogen to reach −196 °C. The sample is a 100 nm SiO_2/Si wafer, with the SiO_2 etched in a stripe pattern. Here the topography, shown in figure 9(*a*), was directly recorded from the piezoresistive output. The MIM-Im contrast reflects the tip–sample capacitance change between the 100 nm SiO_2 layer and native oxide on the etched regions. No contrast is observed in the MIM-Re image, as expected for the insulating SiO_2 surface.

4. Conclusions

We have demonstrated piezoresistive cantilever MIM probes integrated with low impedance, electrical shield and sharp tips for simultaneously topographical and electrical SPM. The piezoresistive displacement resolution is 2 nm in a band from 1 Hz to 10 kHz. The resistance of the center conductor is less than 5 Ω and the tip-to-ground capacitance is 1.7 pF. The small resistance and capacitance, as well as the shielded structure ensure the excellent electrical performance. The probes show good piezoresistive topographic and MIM capability at both room and cryogenic temperatures. These novel piezoresistive probes broaden MIM applications in scientific and engineering studies of new materials and electronic devices.

Acknowledgments

Fabrication work was performed in part at the Stanford Nanofabrication Facility (a member of the National Nanotechnology Infrastructure Network) supported by the NSF under grant ECS-9731293, its lab members, and the industrial members of the Stanford Center for Integrated Systems. This work is supported by National Science Foundation (NSF) under grant no DMR-130573, Center of Probing the Nanoscale (CPN) grant no PHY-0425897 and the Gordon and Betty Moore Foundation through grant GBMF3133 to ZXS. The authors would like to thank the Stanford Nanofabrication Facility staff for their advice and help.

References

[1] Lai K, Kundhikanjana W, Kelly M and Shen Z-X 2011 Nanoscale microwave microscopy using shielded cantilever probes *Appl. Nanoscience* **1** 13–8

[2] Lai K, Kundhikanjana W, Kelly M A and Shen Z X 2008 Calibration of shielded microwave probes using bulk dielectrics *Appl. Phys. Lett.* **93** 123103
[3] Lai K, Kundhikanjana W, Kelly M and Shen Z X 2008 Modeling and characterization of a cantilever-based near-field scanning microwave impedance microscope *Rev. Sci. Instrum.* **79** 63703–6
[4] Lai K, Ji M B, Leindecker N, Kelly M A and Shen Z X 2007 Atomic-force-microscope-compatible near-field scanning microwave microscope with separated excitation and sensing probes *Rev. Sci. Instrum.* **78** 63702
[5] Kundhikanjana W, Lai K, Kelly M A and Shen Z-X 2011 Cryogenic microwave imaging of metal- insulator transition in doped silicon *Rev. Sci. Instrum.* **82** 33705
[6] Lai K, Nakamura M, Kundhikanjana W, Kawasaki M, Tokura Y, Kelly M A and Shen Z-X 2010 Mesoscopic percolating resistance network in a strained manganite thin film *Science* **329** 190–3
[7] Lai K, Peng H, Kundhikanjana W, Schoen D T, Xie C, Meister S, Cui Y, Kelly M A and Shen Z-X 2009 Nanoscale electronic inhomogeneity in In_2Se_3 nanoribbons revealed by microwave impedance microscopy *Nano Lett.* **9** 1265–9
[8] Kundhikanjana W, Lai K, Wang H, Dai H, Kelly M A and Shen Z 2009 Hierarchy of electronic properties of chemically derived and pristine graphene probed by microwave imaging *Nano Lett.* **9** 3762–5
[9] Kundhikanjana W, Yang Y, Tanga Q, Zhang K, Lai K, Ma Y, Kelly M a, Li X X and Shen Z-X 2013 Unexpected surface implanted layer in static random access memory devices observed by microwave impedance microscope *Semicond. Sci. Technol.* **28** 025010
[10] Harjee N, Haemmerli A, Goldhaber-Gordon D and Pruitt B L 2010 Coaxial tip piezoresistive scanning probes with sub-nanometer vertical displacement resolution *IEEE Sensors (2010)* pp 1962–6
[11] Chut W, Mehreganyt M and Robert L 1993 Analysis of tip deflection and force of a bimetallic cantilever microactuator *J. Microelectromech. Syst.* **4** 3–7
[12] Yang Y, Lai K, Tang Q, Kundhikanjana W, Kelly M a, Zhang K, Shen Z and Li X 2012 Batch-fabricated cantilever probes with electrical shielding for nanoscale dielectric and conductivity imaging *J. Micromech. Microeng.* **22** 115040
[13] Yang Y L, Lai K J, Tang Q C, Kundhikanjana W, Kelly M, Shen Z X and Li X 2011 A shielded cantilever-tip microwave probe for micro/nano surface imaging of conductive properties *IEEE 24th Int. Conf. on Micro Electro Mechanical Systems (MEMS 2011)* pp 79–82
[14] Haemmerli A J, Nielsen R T, Kundhikanjana W, Harjee N, Lai K, Yang Y L, Goldhaber-Gordon D, Shen Z X and Pruitt B L 2012 Low-impedance shielded tip piezoresistive probe enables portable microwave impedance microscopy *IEEE 25th Int. Conf. on Micro Electro Mechanical Systems (MEMS)* pp 277–80
[15] Bao M 2005 *Analysis and Design Principles of MEMS Devices* (Amsterdam: Elsevier)