UNIVERSITY OF CALIFORNIA

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A 300-GHz 52-mW CMOS Receiver with On-Chip LO Generation

A dissertation submitted in partial satisfaction

of the requirements for the degree

Doctor of Philosophy in Electrical and Computer Engineering

by

Onur Memioglu

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ABSTRACT OF THE DISSERTATION

A 300-GHz 52-mW CMOS Receiver with
On-Chip LO Generation

by

Onur Memioglu
Doctor of Philosophy in Electrical and Computer Engineering
University of California, Los Angeles, 2021
Professor Behzad Razavi, Chair

A 300-GHz heterodyne receiver downconverts the input to an IF of 27 GHz and performs quadrature separation, thereby avoiding the need for power-hungry couplers and phase splitters. The LO generation consists of a 270-GHz fundamental-mode subsampling PLL with offset mixing driven by a 108-GHz PLL and a 54-GHz PLL. Fabricated in 28-nm CMOS technology, the receiver provides a voltage gain of 18 dB with a noise figure of 20 dB with I/Q gain mismatch of 1.2 dB and phase mismatch of 5.4 degrees.

The dissertation of Onur Memioglu is approved.

Gregory J. Pottie

Aydin Babakhani

Yuanxun Wang

Behzad Razavi, Committee Chair

University of California, Los Angeles

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To my family

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VITA

2011-2015	B.Sc. in Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey
2015-2018	M.Sc. in Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey
2019	Ph.D. Candidate in Electrical and Computer Engineering, University of California, Los Angeles

CHAPTER 1

Introduction

Development of integrated millimeter-wave (mm-Wave) and THz systems in the recent years have found many applications in various areas like wireless communication at 60-GHz, automotive radars at 77-GHz [1–3], THz high speed communication links [4–8], gas spectroscopy [9–13] and biomedical imaging [14–21]. Ongoing demand for higher data rates greater than 20 Gb/s requires highly stable low phase noise local oscillators to improve bit error rate (BER) of these communication systems. These phase locked oscillators were previously developed with BiCMOS [22–24] or III-V semiconductor technologies like InP [25–27]. With the continuous scaling of CMOS technology, CMOS transistors can reach a unit gain frequency (f_t) of 350 GHz and more. Therefore, it is more attractive to build a compact system in the CMOS technology with reduced area, cost and power consumption. However, near ft operation, low quality factor value for inductors creates a very low phase noise performance for the VCO's around sub-THz frequency which requires the use of very high PLL bandwidth to reduce the VCO phase noise.

Data communication in the 300-GHz band has also found renewed interest in the past few years. Rising demands for high data rate wireless communication, still pushes the boundaries for the available frequencies. The idea of getting a high bandwidth communication and the unallocated frequency band from 252 GHz to 322 GHz makes a suitable candidate for next generation communications. The IEEE 802.15.3d standard, which was established in 2017 for radios in the 300 GHz frequency band, is currently trying to determine feasible standards for high bandwidth communication in 300 GHz [28]. In addition to the IEEE task force, a number of researchers have demonstrated the viability of such radios in a range of semiconductor technologies like SiGe BiC-

MOS, InP HEMT and with CMOS [4–8, 26, 29–36].

For 300-GHz transceivers to serve as an attractive complement to WiFi and WiGig, they should perform extensive beam forming so as to overcome the path loss. This point underscores the importance of low power consumption per element. Moreover, high order modulation schemes require a local oscillator (LO) signal with very low phase noise. Unfortunately, the generation and distribution of LO phases proves extremely power hungry.

A receiver architecture in these frequencies started with simple modulations like OOK/ASK modulations. These modulations allows much simpler designs for both transmitters and receivers [37–39]. First of all, these types of receivers do not require a locked local oscillator for up/down-conversion. With the limited speed of the transistors, these type of transmitters/receivers are the most common ones. Unfortunately, these systems do not offer much advantage in terms of data bandwidth. The inefficient modulation schemes lead to lower data rates and high bit error rates.

With further advances in the semiconductor technologies and f_{max} values reaching frequencies of 500 GHz and more, the quadrature transmitters and receivers became feasible for 300 GHz. These systems offer robust performance and better data rates when compared to OOK/ASK however they have some challenges in terms of design. First of all, these systems require a local oscillator that is phase locked to a reference to generate stable clocks. Without phase locked LOs, the quadrature modulations would be highly inefficient due to high phase noises and low frequency stability of oscillators. Traditionally, these PLLs are designed at lower frequencies and the harmonic of the VCO is extracted to be the local oscillator [23, 26, 40, 41]. This method offers better power consumption but suffers from the low power of the desired signal at the output. Another approach is to use frequency multipliers to go to the desired frequencies [30, 42–44]. By using different numbers of frequency multipliers, these types of circuits consume too much power to get a modest swing at the desired frequency. Use of injection locked multipliers can also cause the output signal to be at a different frequency than the desired signal. Therefore, additional tracking loops are needed to be used for correct operation [24]. Again, these multipliers have very low efficiency in terms of power output. In [22], a frequency stabilization technique is proposed for

frequencies between 302-330 GHz. This proposed system doesn't use a reference frequency and hence cannot be reliable to be used in a transceiver chain.

Second problem is to obtain a quadrature clocks to drive mixers in the chip. Some design examples typically include a lossy on chip quadrature hybrid [4, 30, 35, 43]. These hybrids, since passive, introduce a direct 3-dB reduction in the LO power due to the nature of the hybrid. In addition, on chip lossy metals introduce additional losses since these designs must be at quarter wavelength.

The problem of LO generation at frequencies of several hundred gigahertz has generally entailed two facets: (1) it has been considered difficult to design VCOs that achieve such speeds, especially in view of the low varactor Q's, and (2) it is also difficult to develop dividers for these frequencies.

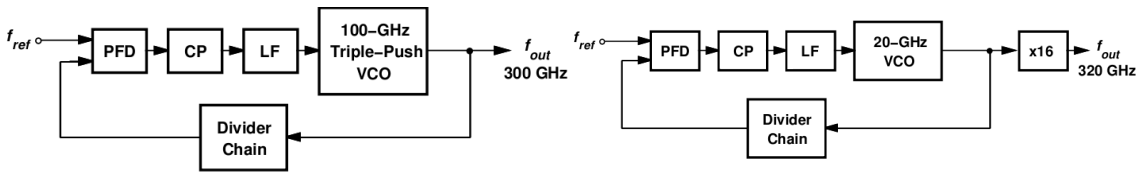
A third issue related to terahertz generation is the reference phase noise. Even a reference frequency of hundreds of MHz with a phase noise of -160 dBc/Hz places an upper bound of about -100 dBc/Hz at 300 GHz if all other noise are neglected. Indeed, typical PFDs and charge pumps also suffer from these levels of noise. To reduce these contributions, one can reduce the PLL bandwidth, but the VCO noise then dominates. Thus, a single PLL is not an attractive choice for our purpose.

In this paper, we will propose an efficient clock generation scheme with a quadrature receiver at 300-GHz for low power and high performance downconversion of the 300-GHz signal to lower bands. In the first parts of the paper, we will go into the details of the 300-GHz LO generation circuit. In the next parts we will explain the quadrature receiver in detail and combine both of these architectures to achieve a 300-GHz receiver with excellent performance and low power consumption.

CHAPTER 2

Overall PLL Architecture

A fundamental generator at THz frequencies is still a difficult challenge although the transistors f_T reaches greater than 300-GHz. Most commonly used technique is to extract the harmonic of the VCO to reach THz frequencies. An example is to use a 100-GHz PLL and use a triple push VCO at 100 GHz to obtain 300 GHz output as shown in Fig. 2.1(a). As we are extracting the harmonic of the VCO, the output power of the extracted signal will be inherently low. Another common approach is to synthesize a low frequency and use frequency multipliers to go to THz frequencies. A sample approach is given in Fig. 2.1(b) where we have a x16 frequency multiplier which uses four x2 multipliers. This approach is also very power inefficient as the output swing of the multipliers are low. Each multiplication stage needs a driver in between to fully drive the preceding stage to achieve maximum output power.



(a) (b)

Figure 2.1: A 300-GHz LO generator with 100-GHz VCO at the PLL (a), A 320-GHz LO generator with integrated x16 frequency multiplier (b)

As seen from the Fig. 2.1, all the generators use a PLL loop at a much lower frequency than the output frequency. We would like to retain the amplitude and power benefits of a fundamental oscillator as they would yield higher output swings and consume less power when compared to the

frequency multiplication techniques. Let's set up the PLL circuit in Fig. 2.2(a) with a fundamental oscillator at 300-GHz. Assuming that we have a VCO at this frequency and a reference frequency of 500-MHz, we would need a divide-by-600 circuit.

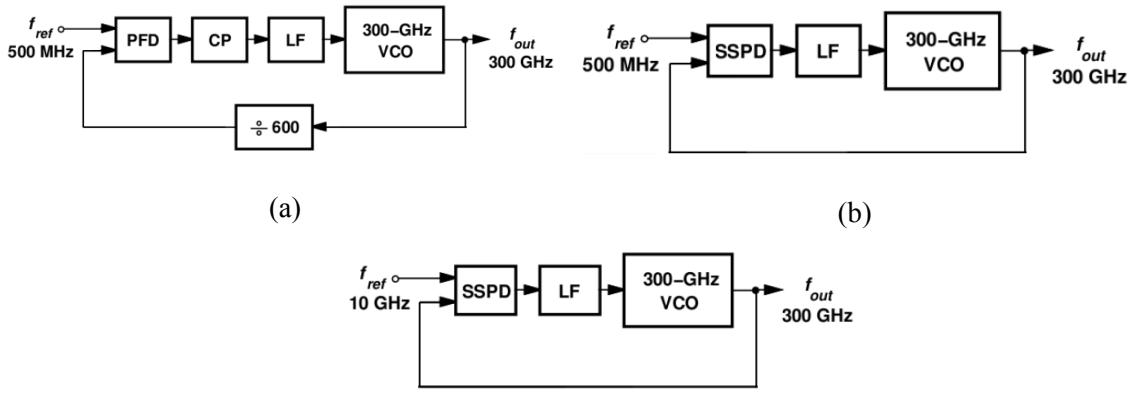


Figure 2.2: A standard PLL design with 300 GHz VCO, a phase detector, charge pump, loop filter and a divide-by-600 circuit (a), Subsampling PLL with 500 MHz reference (b), Subsampling PLL with 10 GHz reference (c)

Most critical part in this design is the first divider in the chain. Only an injection locked frequency divider would be able to divide this input as conventional dividers would lack the necessary speed to overcome such high frequencies. For an ILFD, we must make sure that the output swing at the VCO is able to lock to the divider. Eq. 2.1 describes the injection locking range of the divider. In order to maximize the injection locking range, the injection current must be maximized which means that we need to push a large current from 300-GHz VCO to create a viable locking range.

$$\omega_L = \frac{\omega_0}{2Q} . \frac{I_{inj}}{I_{osc}} \tag{2.1}$$

A VCO at 300 GHz may not sufficiently carry a large current due to limited transistor sizes. Moreover, pulling too much current out of the oscillator can reduce the Q factor of the tank eventually damping the oscillation. Even though if we manage to divide 300-GHz into some reasonable

frequency like 100-GHz we may still need to employ another ILFD to go into the ranges for standard divider circuits like D-flipflop dividers. Additionally, these ILFDs need to tuned by external means as in [24] to check whether the ILFD locked to the correct frequency. Otherwise, the PLL wouldn't lock.

Another option is to remove the divider chain completely from the loop and use a subsampling phase detector to directly sample the VCO signal at the input with 500-MHz reference signal as shown in Fig2.2(b). Apart from sampling problems, which will be discussed later, the lack of divider in the subsampling PLL may lead to false lock conditions. Since the reference frequency is 500-MHz, this PLL may lock to 299.5-GHz or 300.5-GHz or any other integer multiple of 500-MHz. In order to achieve proper lock, we need to monitor the output frequency with a frequency locked loop or with a secondary coarse PLL to correct the output frequency. It would be again difficult to build a PLL with a divider to detect the correct frequency so this idea is also not feasible.

In order to lock to the correct frequency, we can use a higher reference frequency than 500-MHz as in Fig 2.2(c). Let us assume that we have a reference of 10-GHz and the VCO at 300 GHz can oscillate between 295-GHz and 305-GHz. In this case, even with subsampling, the oscillator can only lock to 300-GHz because VCO cannot oscillate at any integer multiple of 10 GHz. For the subsampling phase detector, we can use a capacitor and a single MOSFET as a switch to sample 300-GHz with 10-GHz reference as in Fig. 2.3(a).

Now with the simple sampling circuit, let's see what happens when we try to sample 300-GHz signal with 10-GHz. For the sake of simplicity let us start the analysis of SSPD with an ideal switch instead of transistor and perfect square waveform for 10-GHz as in Fig. 2.3(b). When the switch turns on, 300-GHz signal will be on the capacitor and when the switch turns off, the capacitor will maintain its charge and hence the current phase information. With ideal switch and sampling waveform, we can extract phase information from the 300-GHz signal without any loss.

For the next part of analysis, we keep the waveform same but change the ideal switch to a MOSFET as in Fig. 2.3(c). A transistor has finite on and off resistance when compared to an ideal switch. When the transistor turns on, we will be forming an RC low pass filter at the SSPD. Since

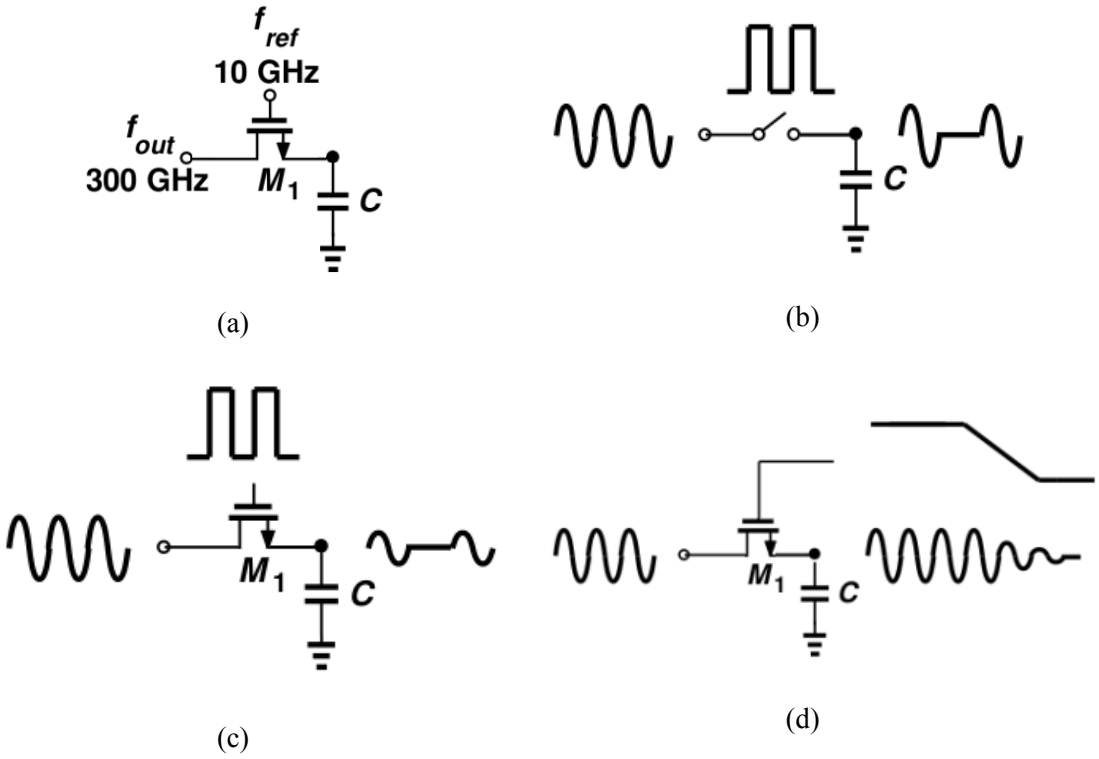


Figure 2.3: Subsampling phase detector with an NMOS and a capacitor (a) an ideal sampler with square wave reference waveform (b), sampling transistor with square-wave reference (c), sampling with finite rise-fall time signal (d)

we have $f_{ref} \ll f_{VCO}$, input will reach steady state until switch turns off. As a result, we can say that 300-GHz sees an RC low pass filter at the input. In this case, we will lose some of the signal amplitude during sampling due to filtering effect formed by the RC circuit. The effective phase detector gain, when compared with the previous case will be reduced by the factor in Eq. 2.2.

$$V_{out} = \frac{1}{\sqrt{1 + \omega^2 R_{on}^2 C^2}} \tag{2.2}$$

The bandwidth of the sampler needs to be adjusted to accommodate higher input frequencies so that K_{PD} remains intact. One can increase the size of the switch transistors to reduce the on resistance but this will also increase the load capacitance on the 300-GHz VCO due to the transistor parasitics.

What would happen if the reference signal is not a perfect square wave but has some rise and fall time? Now we know that during on time, the signal will experience filtering effect and during off time, the phase information will be preserved. Now if the on resistance increases slowly due to finite fall time, the filter's bandwidth will start to reduce slowly. Fig. 2.3(d) shows the output signal during a transition period. Slow decrease in bandwidth would result in the reduction of the amplitude of sampled signal, in this case phase information. When the rise/fall time becomes comparable with the period of the sampled signal, SSPD gain reduces drastically, leading to lock failure in an actual PLL.

As a result, in order for the SSPD to operate correctly, we need very short rise and fall times. In other words, we need a high frequency reference signal so that we would maintain a substantially high phase detector gain and the loop operates correctly. By simulations, we can show that for a 60-GHz sinusoidal reference signal, we can show that for 300-GHz input, we have a gain 1.2-mV/rad, for 180-GHz input, we have a gain of 32-mV/rad.

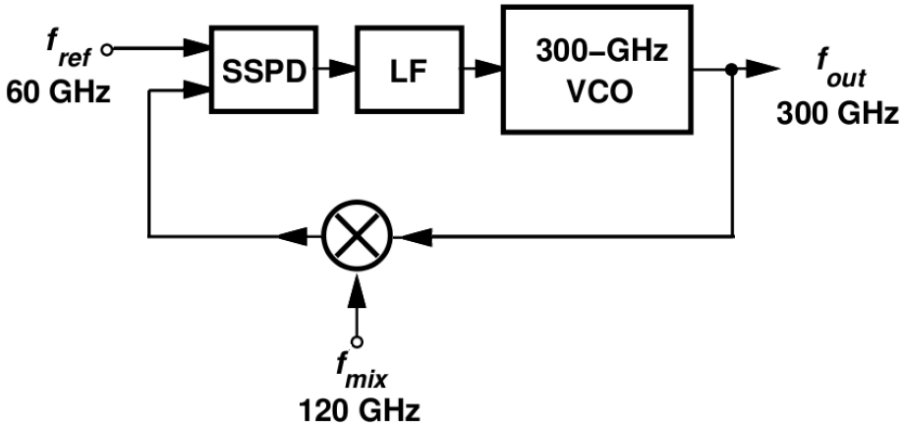


Figure 2.4: 300-GHz PLL employing a mixer to reduce frequency input to SSPD and uses a 60-GHz reference

We can improve the gain of the phase detector by reducing the frequency coming from the VCO. As discussed earlier, a frequency divider wouldn't be easy to design at 300 GHz due to the very high frequency. Fig. 2.4 shows a simple structure which can solve our needs and achieve phase locking for 300 GHz input. Rather than using a divider, we employ a mixer at the feedback

path with 120 GHz LO signal. By this way 300 GHz signal is reduced to 180 GHz which has sufficiently higher phase detector gain.

CHAPTER 3

Proposed System Design

Fig. 2.4 shows that we need to have two signals, one at 60-GHz and the other at 120-GHz to drive such a PLL. As we need a very low phase noise reference for 300 GHz generation, we must generate 60 GHz signal from a crystal reference at a much lower frequency, and we can have another PLL that can generate 120-GHz from the existing 60 GHz.

Fig. 3.1 shows the proposed LO generator architecture. It consists of a 60-GHz PLL, a 120-GHz PLL, and a 300-GHz PLL that receives the former PLLs' outputs. A 60-GHz PLL (PLL_1) is used to generate a 60-GHz output by using a 500-MHz crystal oscillator reference. This output is shared by the 300-GHz PLL (PLL_3)and 120-GHz PLL (PLL_2). PLL_2 generates 120-GHz output which is used by the offset mixer in the PLL_3 to downconvert 300-GHz output to 180-GHz. From 180-GHz, PLL_3 locks to 60 GHz reference and generates an output of 300-GHz.

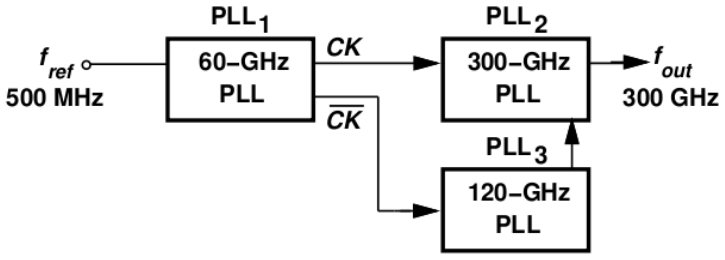


Figure 3.1: Proposed system architecture including a PLL at 60 GHz, 120 GHz and 300 GHz

The architecture of Fig. 3.1 merits five remarks. First, to lower the reference phase noise contribution, we select a relatively narrow bandwidth, about 50-MHz, for PLL_1, but design the 60-GHz VCO for very low phase noise, about -117 dBc/Hz at 1 MHz offset. On the other hand, we choose wide bandwidths for PLL_2 and PLL_3, 400 MHz and 700 MHz, respectively, so as to attenuate the

phase noise of their VCOs.

Second, to minimize power consumption and simplify the routing of signals, we avoid high-frequency inductor-hungry buffers: the output of PLL_1 directly drives its own feedback divider and the phase detectors (PDs) in PLL_2 and PLL_3, the 120-GHz signal generated by PLL_2 is directly applied to PLL_3, and the output of PLL_3 directly switches the input transistors of the mixer. The cost is extensive iteration between design and layout. Third, another benefit of avoiding buffers is the small area of the overall generator, about 185 μm x 220 μm, which proves useful if multiple beam-forming transceivers are to be integrated on the same chip. Fourth, we exploit the line inductances associated with the distribution of the waveforms to create series peaking and slightly enlarge the voltage swings. Fifth, the generator's frequency planning affords great flexibility in direct-conversion or heterodyne transceiver design and coverage of numerous bands from 60 GHz to 420 GHz.

3.1 300-GHz PLL Design

300-GHz PLL consists of a subsampling phase detector, an amplification denoted as G_m , a VCO at 300-GHz and a mixer shown in Fig. 3.2. Rather than employing a power hungry injection locked divider, we simply use a double balanced active mixer to downconvert 300-GHz output to 180-GHz, with the help of 120-GHz signal generated from an additional PLL.

One of the important question that needs to be answered is that whether this PLL locks to 300-GHz with the given configuration. Let us consider the simplified phase equivalent diagram of the 300-GHz PLL in Fig. 3.3.

A mixer in time domain can be considered as a multiplier circuit. If we multiply two cosines of different frequency and phases, we would obtain:

$$cos(\omega_1 + \theta_1).cos(\omega_2 + \theta_2) = \frac{cos[(\omega_1 + \omega_2)t + (\theta_1 + \theta_2)] + cos[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)]}{2} \quad (3.1)$$

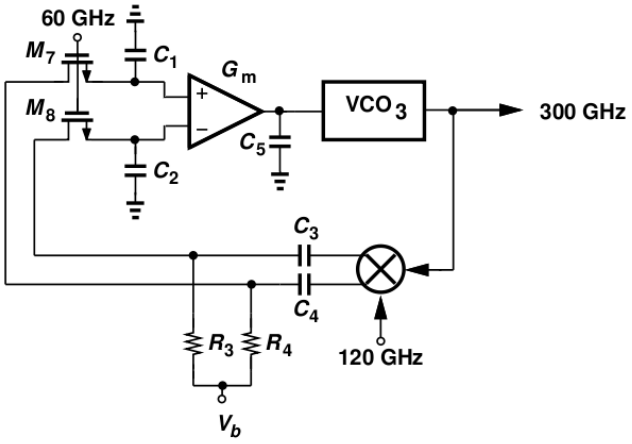


Figure 3.2: Proposed 300-GHz PLL architecture

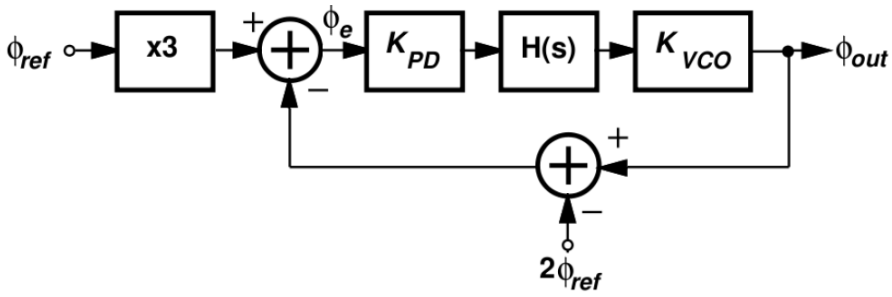


Figure 3.3: Small signal phase equivalent of 300-GHz PLL

In phase domain, the mixer adds phases for the upconversion, and subtracts phases for the downconversion. Since we are using the downconverted output, this mixer can be approximated as a subtractor in phase domain.

Secondly, now the frequency at the input of the SSPD is reduced to 180-GHz, we have x3 subsampling at the input, therefore the reference phase at the input is multiplied by 3. At 120-GHz input side, we assume that the input is $2\Phi_{ref}$ because this signal is generated using another PLL from 60-GHz.

Let us start analyzing the PLL. If we write the phase error:

$$\phi_e = 3\phi_{ref} - (\phi_{out} - 2\phi_{ref}) \tag{3.2}$$

$$\phi_e = 5\phi_{ref} - \phi_{out} \tag{3.3}$$

$$\phi_{out} = K_{PD}.H(s)\frac{K_{VCO}}{s}\phi_e \tag{3.4}$$

$$\phi_{out} = K_{PD} * H(s)\frac{K_{VCO}}{s}.(5\phi_{ref} - \phi_{out}) \tag{3.5}$$

$$\frac{\phi_{out}}{\phi_{ref}} = A_\phi(s) = \frac{5K_{PD}H(s)\frac{K_{VCO}}{s}}{1 + K_{PD}H(s)\frac{K_{VCO}}{s}} \tag{3.6}$$

$$\frac{\phi_{out,open}}{\phi_{ref,open}} = T(s) = 5K_{PD}H(s)\frac{K_{VCO}}{s} \tag{3.7}$$

where $A_\Phi(s)$ is the closed loop response and T(s) is the open loop response.

When we analyze the open loop gain, which is given in Eq. 3.7 we find an interesting resulting. Although it is a x3 subsampling stage, the overall system can be approximated as a x5 subsampling stage without mixer and 120-GHz input as in Fig. 3.4. This gives us a clear image why this is a viable structure for a PLL to lock.

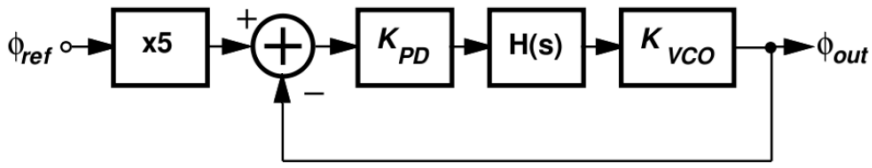


Figure 3.4: Approximate x5 subsampling phase model for 300-GHz PLL

3.1.1 Subsampling Phase Detector

The SSPD in 300-GHz PLL is a differential sampling stage which has 180-GHz input coming from the mixer. As discussed in the previous chapter, we need to reduce the input frequency to maximize the phase detector gain. From simulation results, direct sampling of 300 GHz signal by 60 GHz has a phase detector gain of 1.2-mV/degree whereas, direct sampling of 180-GHz signal by 60-GHz reference has a phase detector gain of 32-mV/deg.

A phase detector which consists of only a single NMOS as a switch and a capacitor C as in Fig. 3.5 is chosen as a simple structure to perform phase detection. The switch size is chosen as 2 μm and capacitor is chosen as 5 fF. These values give a bandwidth of 360 GHz including the parasitics, which is 2 times the input signal frequency.

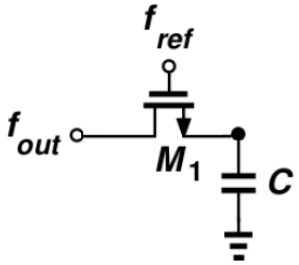


Figure 3.5: Subsampling stage in 300-GHz PLL

Reference signal in this case is a sinusoidal signal at 60-GHz. One way to improve the phase detector gain is to improve rise and fall time of the reference. By making a square wave, we would be able to sample more effectively thus increasing our K_{PD}. Given that the signal's high frequency we would need power hungry buffers in order to decrease signal transition times by around 1 ps according to the simulations, which is not feasible to do. With reduced input frequency and 60-GHz reference frequency, we can get substantially high gain and as a result achieve phase lock.

3.1.2 300-GHz VCO Design

For an oscillator at 300-GHz, typical approach is to extract harmonic from an existing oscillator. However, these approaches prove to be very power inefficient and the output doesn't have sufficient swing at the output in most of the cases. In this design we propose a fundamental oscillator that can oscillate at 300-GHz and that has a sufficient swing at its output to drive a mixer in the receive path.

As a fundamental oscillator, a simple cross-coupled oscillator can be used as a THz oscillator as long as we can have a tank with high enough Q-factor. However, this approach falls short for 2 reasons. Firstly, in order to get the oscillation frequency, we need to select very low transistor sizes

to reduce parasitic capacitances and also to keep the inductance as high as possible. The output swing of a cross coupled pair is:

$$V_{out} = \frac{4}{\pi} I_b R_p \tag{3.8}$$

Choosing low inductances, will eventually reduce the output swing of the transistor because as illustrated in (3.8), the output swing heavily depends on the R_p formed by the inductor and its quality factor. Secondly, this oscillator will be susceptible to any load connected to its output, reducing oscillation frequency drastically.

As illustrated in [45], the addition of transformer and buffer to the XCO, which is referred as buffer feedback oscillator (BFO) entails some advantages over the XCO alone. The schematic is given in Fig. 3.6(a) which shows a cross coupled pair is connected to common source stages M_3 and M_4. Through the coupling action, some of the power couples back into the XCO, enabling special properties.

Fig. 3.6(b) shows a simplified small signal analysis of the structure. The frequency of oscillation can be calculated using the small signal analysis. If we assume L_1=L_2=L and C_1=C_2=C, this oscillator would yield two modes of oscillation:

$$\omega_1^2 = \frac{1}{(L+M)C} \tag{3.9}$$

$$\omega_2^2 = \frac{1}{(L-M)C} \tag{3.10}$$

Equation (3.10) is obtained when the transformer currents are out of phase and yields a much higher oscillation frequency. However this mode of oscillation is not observed in this configuration. Equation (3.9) is observed when the transformer currents are in phase and can be obtained if used in the current configuration.

This structure uses 3 μm transistors in the cross-coupled pair with 25-pH inductance in the L_1 to create oscillation in the BFO structure. According to simulation results, we would need a

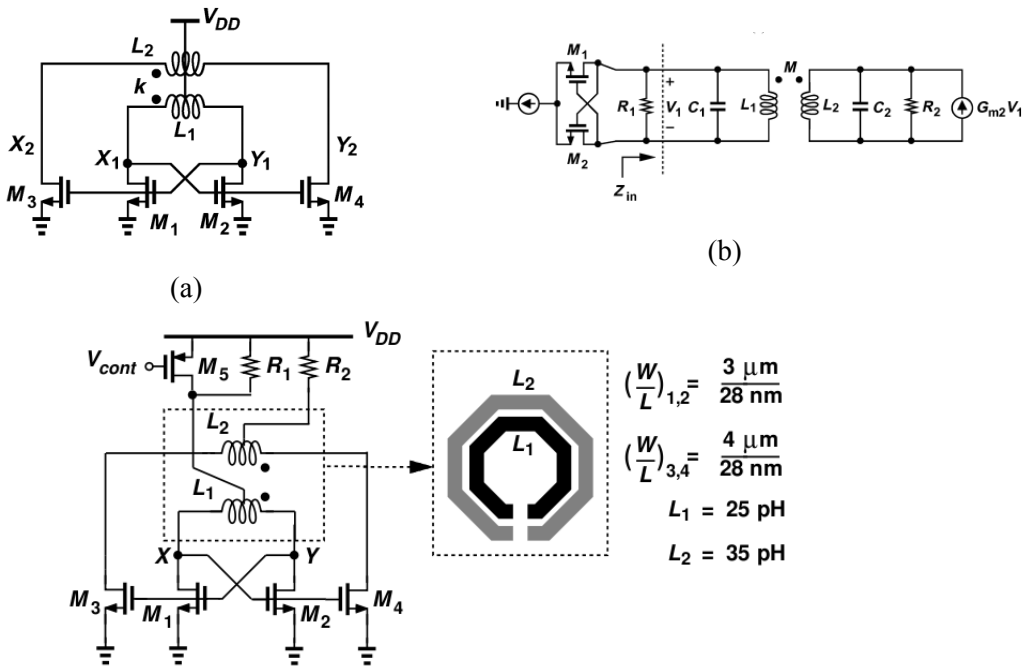
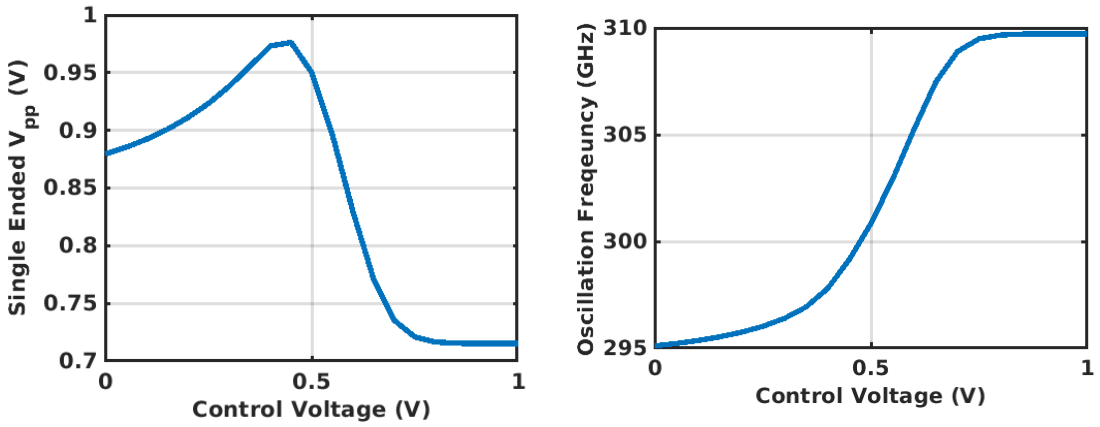


Figure 3.6: Buffer feedback oscillator (a), simplified small-signal analysis (b), BFO converted into a VCO with the help of M_5 and physical implementation of transformer (c)

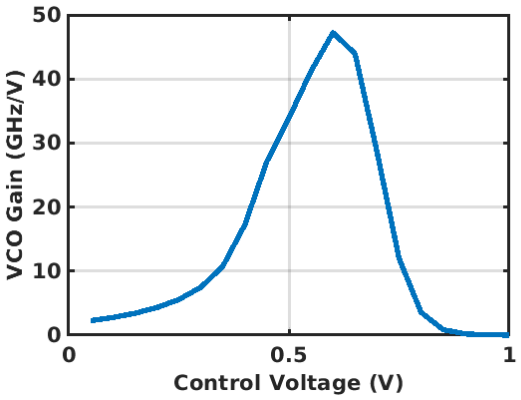
transistor size around 2.2 µm transistors to get the same oscillation frequency with only a simple cross-coupled pair.

Creating a VCO is another challenge at these frequencies. Lack of varactor models at these frequencies, we propose a tuning technique that adjusts the CM level at X and Y by M_5 in Fig. 3.6(c). At lower CM levels, M_1-M_4 spend more time in the off region, exhibiting a smaller average gate capacitance and hence providing a greater oscillation frequency. R_1 ensures oscillator startup even if V_{cont} is near V_{DD} at the beginning of operation. R_2 establishes an output CM level around $0.75*V_{DD}$ and suited to the offset mixer. Change in VDD voltage also results in the change of the amplitude swing, where swing is maximized when V_{ctrl} is around 0.45 V whereas the VCO gain is maximized when V_{ctrl} is at 0.6 V. Fig. 3.7(a) shows how the amplitude varies with the V_{ctrl}. This oscillator consumes 2.5 mA from a 1 V source when it oscillates at 300-GHz.



(a)

(b)



(c)

Figure 3.7: Single ended peak to peak swing with respect to control voltage (a), VCO frequency with respect to control voltage (b), VCO gain with respect to control voltage (c)

This tuning approach doesn't load the oscillator directly so that we can choose the size of M_5 very large without affecting oscillation frequency. However one major drawback of this approach is that the flicker noise of M_5 directly modulates the oscillator leading to phase noise. Due to large bandwidth of 300-GHz PLL, this additional noise is suppressed by the PLL bandwidth. In addition, large size of PMOS transistor also effectively reduces the noise contribution coming from this transistor. This method allows the transistor to be tuned between 295 GHz to 310 GHz leading to a K_{VCO} of 47 GHz/V when V_{cont} is 0.6 V. Fig. 3.7(b) shows the oscillation frequency and Fig. 3.7(c)

shows the VCO gain with respect to V_{ctrl}.

3.1.3 Offset Mixer Design

The offset mixer is used to simply reduce 300 GHz to 180 GHz with the help of 120-GHz LO signal coming from 120-GHz PLL.

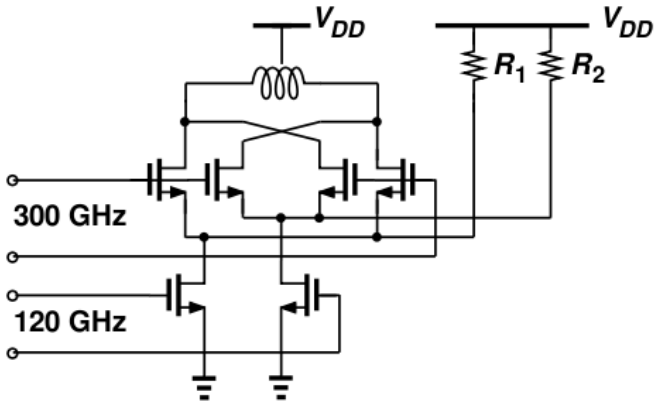


Figure 3.8: 300-GHz offset mixer

The schematic of this offset mixer is given in Fig. 3.8. This mixer uses a double balanced active mixer topology. LO transistors have a width of 4 µm and 300-GHz transistors have a size of 1 µm. Low transistor size for 300-GHz is chosen to minimize the effect on the oscillation frequency and amplitude of the VCO. The gain of this mixer is given in Eq. 3.11 assuming that the RF transistors can fully switch the current from one transistor to the other.

$$V_{out} = \frac{4}{\pi} g_m . V_{LO} . \omega L Q \tag{3.11}$$

In order to maximize the gain of the mixer, we need to ensure that transconductance, LO swing and Q-factor of the inductor in Fig. 3.8 is maximized. 120-GHz LO swing comes directly from a VCO which has a swing around 1 V_{pp}. The inductor at the load allows the structure to resonate at 180-GHz, maximizing the voltage swing at the output. The swing value depends on the R_p value

of the inductor at 180-GHz. The designed inductor has 200 pH with a Q-factor of 18. In order to maximize g_m, we need to push current through the LO transistors. Current passing through the RF transistors are limited hence in order to get more current to those transistor additional resistors are employed as in Fig. 3.8. Resistors R_1 and R_2 are used to provide 40% of the bias current to the 120-GHz LO transistors boosting the overall gain of the structure.

There are two benefits associated with this mixer. Firstly, offset mixer seperates 300-GHz VCO from the subsampling phase detector. Due to the capacitances being switched on and off for some time in the SSPD, it is possible that direct connection to the subsampling phase detector would create a modulation in the oscillation frequency at the VCO. However, by inserting the mixer, we ensure that the VCO sees a fixed capacitance and hence do not change its oscillation frequency. Secondly, this mixer does not generate spurs because its output components can be expressed as 120n ± 300m GHz, where n and m are integers, which are harmonics of the 60-GHz reference and map to dc after the PD.

3.1.4 Gain Stage

In order to compensate some of the loss in the phase detector, an additional g_m stage is added to the PLL loop as depicted in Fig. 3.2. This amplifier consists of two stages of amplification. First stage is a fully differential PMOS pair with resistive loads and the second stage is consists of 5 transistor OTA as in Fig. 3.9(a).

Due to the finite loop gain and first order loop characteristics, the loop may be unable to lock to the reference frequency. The oscillation frequency must be close enough to be able to lock to the reference frequency. The DC bias at the output of the gain stage determines the control voltage of the VCO and hence determines the VCO's output frequency. By manipulating the output DC level, we can establish a close enough VCO frequency so that the PLL locks.

The DC bias of the output stage is modified by inserting a DC current at the positive and negative output of the fully differential amplifier. By adding small DC offset at the input of second stage,

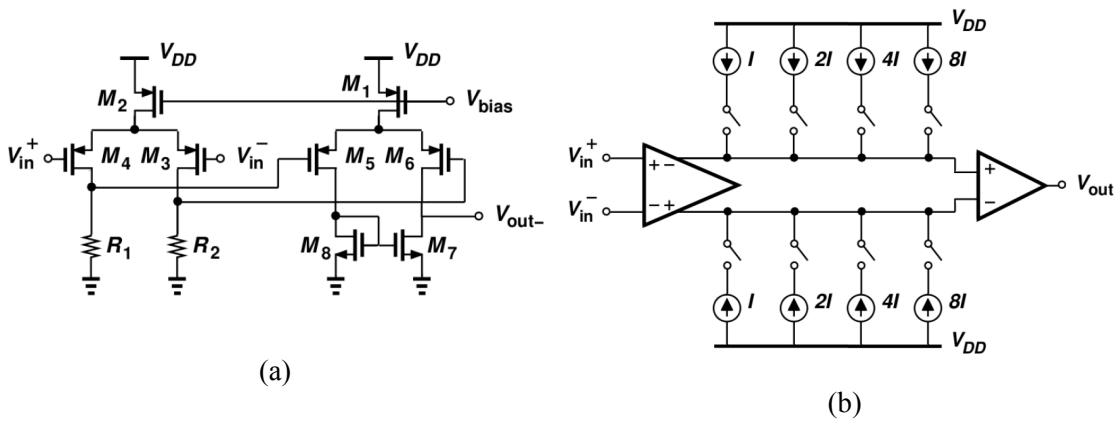


Figure 3.9: Gain stage design (a), programmable currents added to control output DC level (b)

the output voltage can be controlled. Fig. 3.9 (b) shows the amplifier with the programmable DC bias controller. The current sources are switched externally and has a step of 10μA with a total of 160μA. This gives the output DC range from 150 mV to 650 mV which is the desired range for the VCO. This amplifier generates a maximum of 16 dB gain with a bandwidth of 1 GHz. The output This large DC bias adjustment covers all of the VCO range where K_{VCO} is greater than 5 GHz/V. At maximum K_{VCO} point, the loop may become unstable due to the excessive gain as simulations show. As a result, a gain switch is added to the fully differential amplifier to reduce overall gain to 10 dB, such that the loop remains stable.

3.2 Phase Noise Analysis for 300-GHz PLL

In the previous sections, we showed that this PLL acts as an equivalent of x5 subsampling PLL. By using this approximation, we could still get a fairly good approximation of the exact phase noise for 300-GHz signal. For the full analysis, let us use diagram in Fig. 3.10 for phase noise analysis.

Firstly, let's start by analyzing VCO noise and calculate its contribution at the output.

$$\phi_{n,out} = (\frac{1}{1+T(s)})^2 \phi_{n,VCO} \tag{3.12}$$

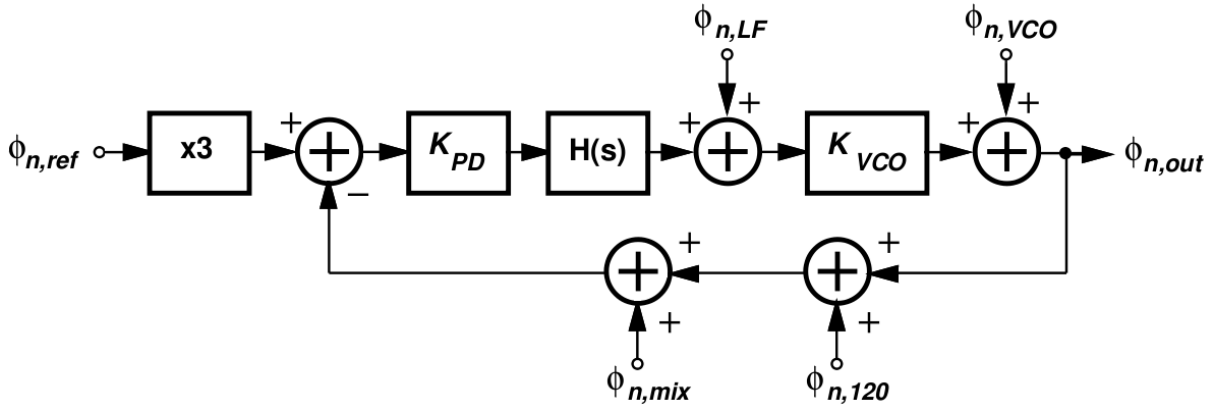


Figure 3.10: Small signal model for phase noise analysis

Secondly, let's calculate SSPD and gain stage noise contribution at the output.

$$\phi_{n,out} = (\frac{A_\phi(s)}{K_{PD}H(s)})^2\phi_{n,K_{PD}} \tag{3.13}$$

Both of these contributions can be approximated like we have a x5 subsampling PLL.

Let's calculate the effect of reference and 120-GHz PLL at the same time.

$$\phi_{n,out} = 9\phi_{n,ref}\frac{A_\phi(s)^2}{25} + \phi_{n,120}\frac{A_\phi(s)^2}{25} + H^2_{n,refn,120}(\phi n, ref\phi_{n,120}) \tag{3.14}$$

We know that VCO, SSPD and gain stage noises are uncorrelated with each other so we can utilize superposition to simplify our analysis. However, 60-GHz reference noise and 120-GHz noise are correlated to each other. In fact, in this case we can approximate that they are fully correlated within the loop bandwidth of 120-GHz PLL. We will analyze 120 GHz PLL phase noise in the following sections and we will see that the major noise contribution is coming from the 60-GHz reference for 120-GHz signal. Now assuming full correlation, the correlation term in Eq. 3.14 becomes:

$$\phi_{n,out} = 9\phi_{n,ref}\frac{A_\phi(s)^2}{25} + \phi_{n,120}\frac{A_\phi(s)^2}{25} + 6\frac{A_\phi(s)^2}{25}\phi_{n,ref}\phi_{n,120} \tag{3.15}$$

From 120 GHz PLL, we can relate output noise to the reference as:

$$\phi_{n,120} = 2\phi_{n,ref} \tag{3.16}$$

When we substitute this in Eq. 3.15, this will yield:

$$\phi_{n,out} = 9\phi_{n,ref}\frac{A_\phi(s)^2}{25} + 4\phi_{n,ref}\frac{A_\phi(s)^2}{25} + 12\phi_{n,ref}\frac{A_\phi(s)^2}{25} \tag{3.17}$$

$$\phi_{n,out} = A_\phi(s)^2\phi_{n,ref} \tag{3.18}$$

in which we can assume that this PLL acts like a x5 subsampling PLL.

An interesting question in here is that what would happen if the noises are uncorrelated? If we can generate 60-GHz using two different PLL's and one of them is used as a reference for 300-GHz PLL and the other is used as a reference for 120-GHz PLL as denoted in Fig. 3.11.

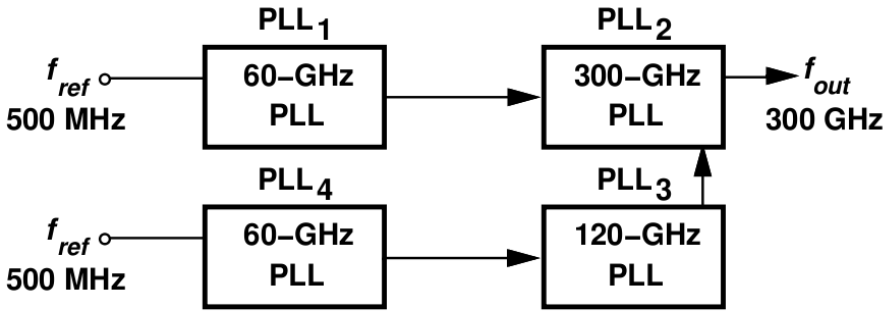


Figure 3.11: A system proposition for uncorrelating phase noise

Since the noises are uncorrelated, we can neglect the correlation term in Eq. 3.14. The overall phase noise becomes:

$$\phi_{n,out} = 9\phi_{n,ref}\frac{A_\phi(s)^2}{25} + \phi_{n,120}\frac{A_\phi(s)^2}{25} \tag{3.19}$$

$$\phi_{n,out} = 9\phi_{n,ref}\frac{A_\phi(s)^2}{25} + 4\phi_{n,ref}\frac{A_\phi(s)^2}{25} \tag{3.20}$$

$$\phi_{n,out} = \frac{13}{25}A_\phi(s)^2\phi_{n,ref} \tag{3.21}$$

which is approximately half of the phase noise that we get when we use single 60-GHz PLL.

Utilizing 2 60-GHz PLLs would significantly increase the power budget and complexity of the entire system and the gain would be only 3 dB given that both 60-GHz PLLs and crystals are at the

same phase noise level with each other. Any noise mismatch in these components would reduce the noise benefit from additional circuitry, therefore it is not implemented in this design.

3.3 120-GHz PLL Design

120-GHz PLL design is very similar to the 300-GHz PLL with a few changes. The most notable change for this PLL is the direct connection of the VCO to the SSPD stage. Since the VCO is frequency is 2 times the reference frequency, SSPD would have sufficient gain to lock the loop. The schematic of this PLL is given in Fig. 3.12.

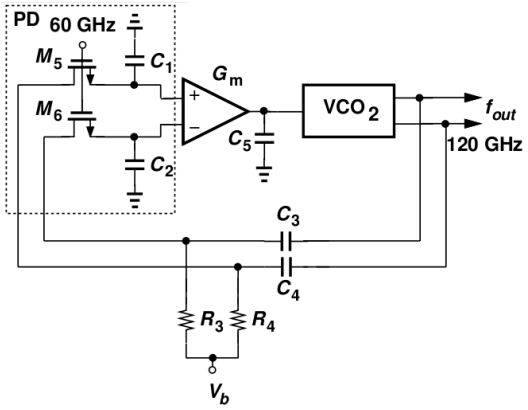


Figure 3.12: 120-GHz PLL

VCO in this loop has some small modifications. First of all, although, it uses the same architecture with 300-GHz VCO as seen in Fig. 3.12(b). The values of the inductors and transistors are modified to better accommodate the lower frequency.

For the PLL system to work, all of the frequencies, 60-GHz, 120-GHz, 300-GHz PLLs must be aligned so that we can achieve a locking at 300-GHz PLL. 300-GHz VCO has a frequency change from 295 GHz to 310 GHz. This means that if we want to lock the PLL system for this entire range, 120-GHz VCO must oscillate between 118 GHz to 124 GHz. Unfortunately the frequency change of 120-GHz VCO in this case is eventually limited to 1.5 GHz as shown from simulations in Fig. 3.15(a). Recalling Eq. 3.10, the oscillation frequency depends on the inductance, mutual

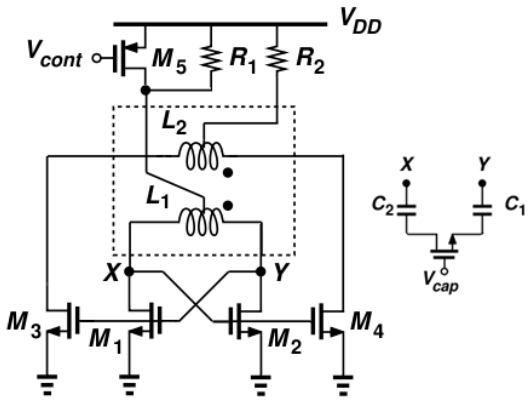


Figure 3.13: 120-GHz VCO schematic

inductance and the parasitic capacitance. Rather than changing transistor sizes to match oscillation frequency, the inductances are increased to get the maximum output swing from the VCO, limiting capacitance change from VDD variation. Combined with increased capacitance from large inductor size, CM level change leads to a very narrow change in oscillation frequency.

In order to boost the frequency range of this PLL to cover more than the 300-GHz VCO, 3 capacitor banks with a load of 4 fF in Fig. 3.13 are added. The resulting oscillation frequency coverage with capacitor banks is given in Fig. 3.15(a) where it covers a range from 115 GHz to 121.2 GHz. Although, this VCO exhibits a smaller K_{VCO}, this PLL can lock much better than the 300-GHz. With high VCO swing and lower frequency, SSPD has a higher phase detector gain and eventually compensating the low gain from the VCO.

Due to the absence of the mixer, the output of this VCO is directly connected to the subsampling phase detector. As seen in the Fig. 3.14, this capacitor switching operation would create a modulation in the VCO frequency, causing spurs at 120 GHz ± 60 GHz at a level as high as -30 dBc according to simulation results. Fortunately, upon driving the offset mixer in Fig. 3.8, these components translate to integer multiples of 60 GHz, producing no additional spurs in the 300-GHz output.

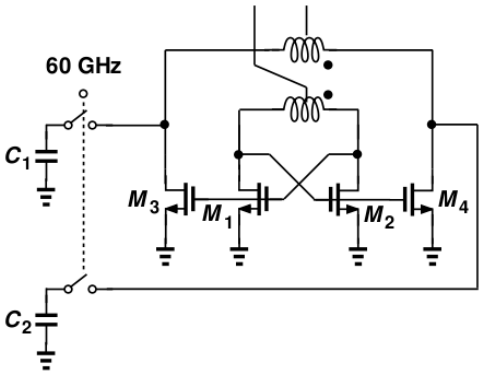
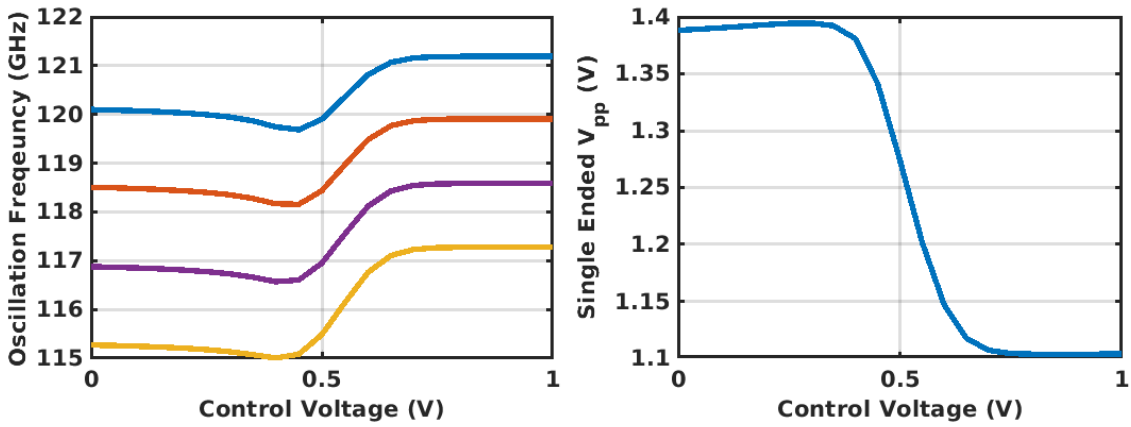


Figure 3.14: Modulation of 120-GHz VCO with 60-GHz VCO



(a) (b)

Figure 3.15: 120 GHz VCO oscillation frequency with respect to control voltage and capacitor banks (a), single ended peak-to-peak swing (b)

3.4 60-GHz PLL Design

The purpose of this PLL is divided in 2 parts. First of all, it should be able to have a rail to rail swing at 60 GHz such that it can drive the subsampling switches at both high frequency PLLs and secondly, to generate a 60-GHz signal from 500-MHz crystal reference with lowest noise as possible. The loop bandwidth is chosen as 50-MHz to limit the reference noise and VCO noise contributions.

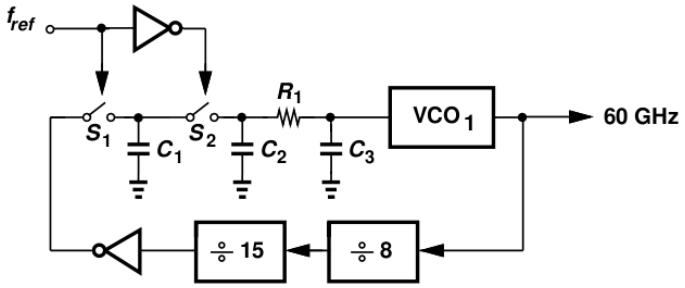


Figure 3.16: 60GHz PLL schematic

The PLL architecture is given in the Fig. 3.16. In this PLL rather than using a subsampling architecture, we employ dividers to go down all the way down to 500 MHz. As discussed in previous sections, it would be still hard not to use dividers in this case because, without dividers, this PLL can lock to any integer multiple of 500 MHz. To avoid using extra complex circuitry for a second loop, we have dividers at this circuit to divide 60 GHz down to 500 MHz.

After the division, the signal is sampled using master slave sampling phase detector. Previous sections extensively used a single stage sampling compared to this one. These switches are driven by complimentary inputs from the 500 MHz crystal.

After sampling the signal, it is only filtered with the low pass filter formed by the C_3 and R_1, forming the control voltage. No amplifiers are necessary at this loop because the divided signal is more like a square wave such that the sampler acts like a bang-bang phase detector. This generates enough loop gain to achieve phase locking. This was not the case in the previous PLLs because the SSPD gain was sufficiently low so we need some boost at the loop itself.

3.4.1 60-GHz VCO Design

Being at a lower frequency than both 120-GHz and 300-GHz, we don't use the buffer feedback oscillator as an oscillator for 60-GHz. This VCO is formed by complimentary cross coupled pair as seen in Fig. 3.17. This oscillator uses 15 µm width both NMOS and PMOS transistors and 60 pH inductance as L_1. Low frequency enables us to use the varactor models existing in the process

library with enough confidence. Fine tuning of this VCO is established with the varactors. In order to get a large tuning range for this VCO, 7 capacitor banks each consisting of 8 fF are added to increase the coarse tuning range of the frequency.

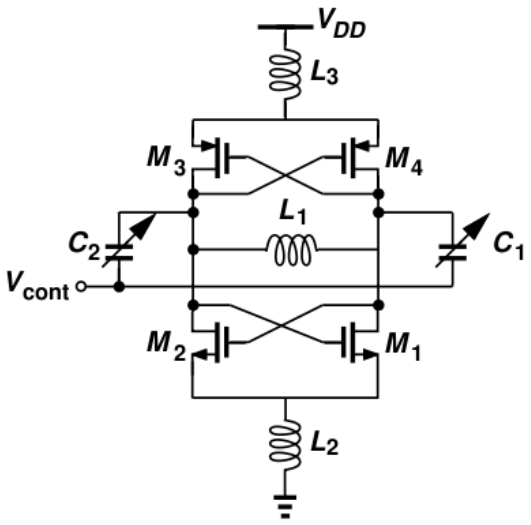


Figure 3.17: 60 GHz VCO schematic

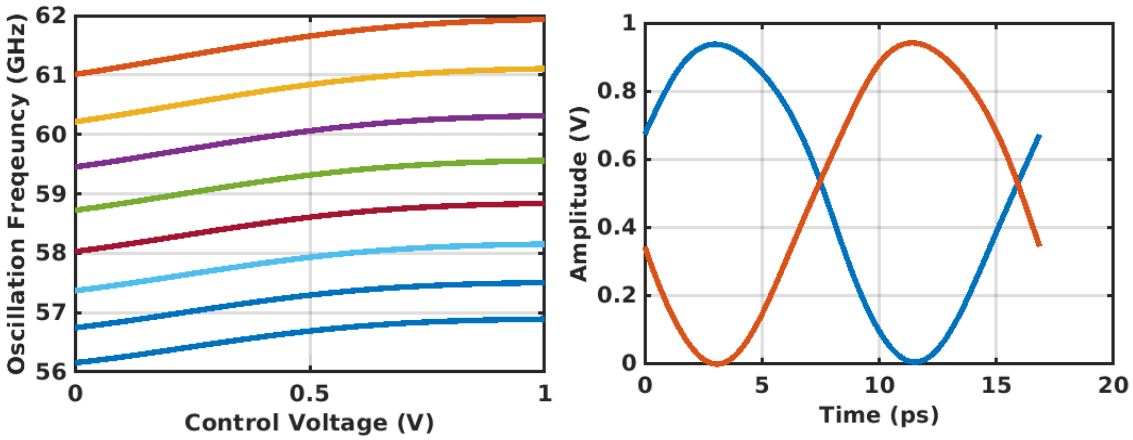
Varactors in this oscillator provide a frequency change of 900 MHz. With the additional capacitor banks, this oscillator oscillates from 56 GHz to 62 GHz as in Fig. 3.18(a). With this range, this PLL covers 280 GHz to 310 GHz in the higher frequency regime, overlapping with the 300 GHz VCO frequency.

The amplitude of the oscillation is provided in Fig. 3.18 (b), swinging from 0 to 950 mV.

3.4.2 Divide-by-8 Circuit

A critical difference in 60-GHz PLL is the use of frequency dividers in the feedback path. As discussed earlier, with a very low reference frequency at 500 MHz, it is possible that this loop might lock to any integer multiplier of 500 MHz. In order to prevent this, either an additional frequency tracking loop or a frequency divider must be used.

For 60-GHz divider, it is possible to design a divider as transistors have enough gain. However



(a) (b)

Figure 3.18: 60 GHz VCO oscillation frequency with respect to control voltage and capacitor banks (a), output swings in time domain (b)

it is still a tedious task to design a divider that can operate at 60 GHz. That is why in order to achieve a divide-by-120 in total, we employ two different divider stuructures in the loop. The first divide-by-8 structure is responsible for bringing the frequency down to 7.5 GHz and the divide-by-15 brings the frequency down to 500 MHz.

The first divide-by-8 structure consists of 3 cascaded divide-by-2 circuits. A sample divide-by-2 circuit is given in Fig. 3.19. In this structure, we have 3 inverters connected back to back with two switches inserted in between two inverters. These switches are driven with complimentary inputs such that only one of the switches remains on at the same time. This maintains the loop to be open at all times with non-overlapping clocks.

An inverter and a switch structure can be viewed as a single latch. When the switch turns on, the inverted input is at the output and when the switch turns off, the output doesn't change relative to the input. This divider uses two latches in series which acts as a D-flipflop. The extra inverter at the output is used to generate complementary output for the divider operation. Equivalently it is a D-flip flop based divide-by-2 structure as in Fig. 3.20.

Circuit in Fig. 3.19 still lacks the speed to successfully divide 60 GHz into 30 GHz. Although

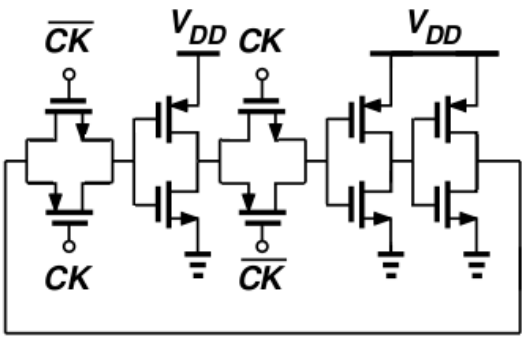


Figure 3.19: Simple divide-by-2

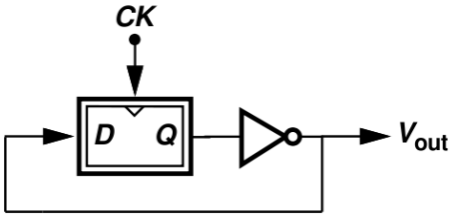


Figure 3.20: D-flip-flop divide-by-2 circuit

it is the simplest form of a latch, it still cannot keep up to speeds like 60 GHz. The inverters need to drive a switch and an additional inverter. As a result, inverters cannot fully pull up and down their outputs with the 60 GHz clock inputs. In order to boost the speed of the divider, a few modifications are made to that circuit. Firstly, The PMOS side of the switch is removed to reduce the inverter load. Since PMOS pair is removed, in order to pull up the voltage at the output of the switch, the input clock DC level is boosted to 1 V. The output of 60-GHz VCO is AC coupled to the divider and 1 V DC level is supplied from a 4 kΩ resistor. Secondly an additional feedforward path is added to boost the speed of the circuit. The feedforward path helps the latch to prepare the output for the second stage. As the input is ready for the next latch, the circuit can operate at faster speeds. The complete circuit diagram for 60 GHz divider is given in the Fig. 3.21.

Two feedforward paths can be used to achieve more symmetrical response from the loop and an increased speed for the divider. The extra feedforward path, however, can complete a loop with three inverters, resulting in an oscillation like a ring oscillator.

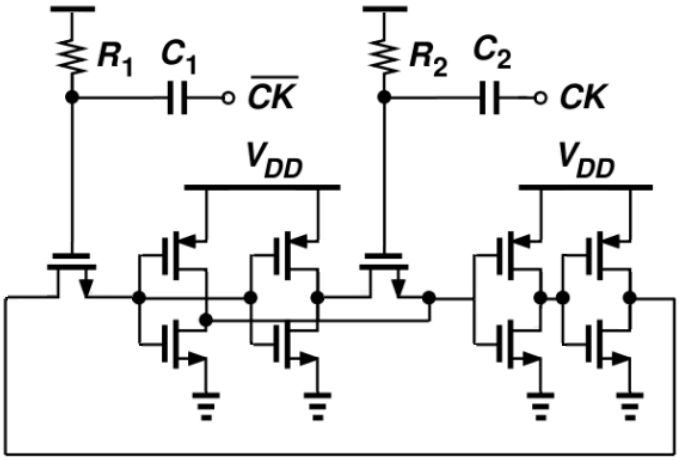


Figure 3.21: Modified divide-by-2 circuit for 60 GHz input

For a single feedforward path, the size of the feedforward inverter must be chosen such that, it wouldn't disrupt the operation on the main path. If the feedforward path gets too strong, then one of the latches will operate like a buffer and as a result, this structure wouldn't divide the input frequency. Fig. 3.22 shows the divide-by-2 structure with a dominant feedforward path. We can see that the output of latch is buffered and connected to the input of itself. This can be problematic with the fast-fast corner in the chip when the feedforward path gets stronger. The structure might even start oscillating when the switch turns on. Extensive corner simulations are required to verify that the divider can successfully cover the frequency range of our 60-GHz VCO without any possible oscillations.

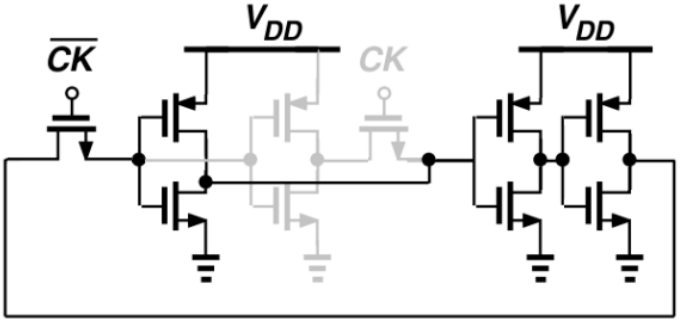


Figure 3.22: 60-GHz divider with a strong feedforward path

Fig. 3.23 shows the response of the divider cells outputs with 60-GHz input driven by the VCO at nominal conditions. At the first divider successfully divides 60-GHz into 30-GHz, second divider takes 30-GHz input and produces 15-GHz output and finally last divider takes 15-GHz input and returns 7.5 GHz output.

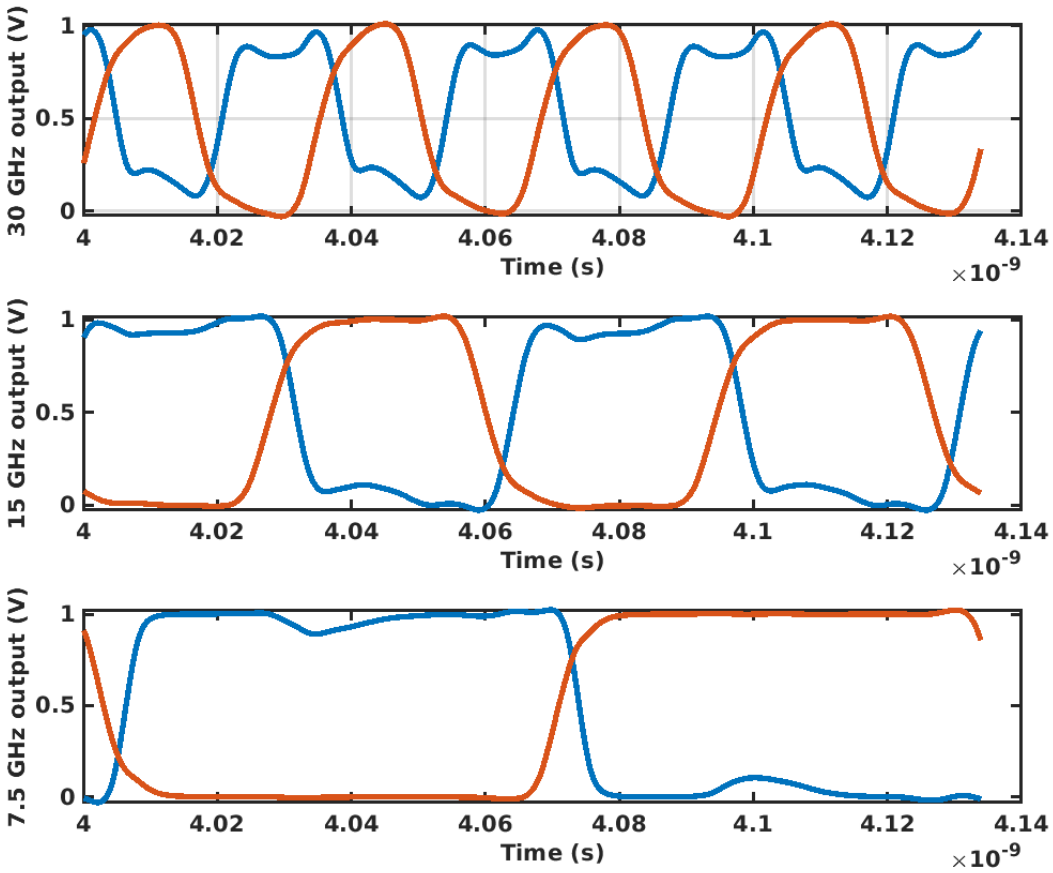
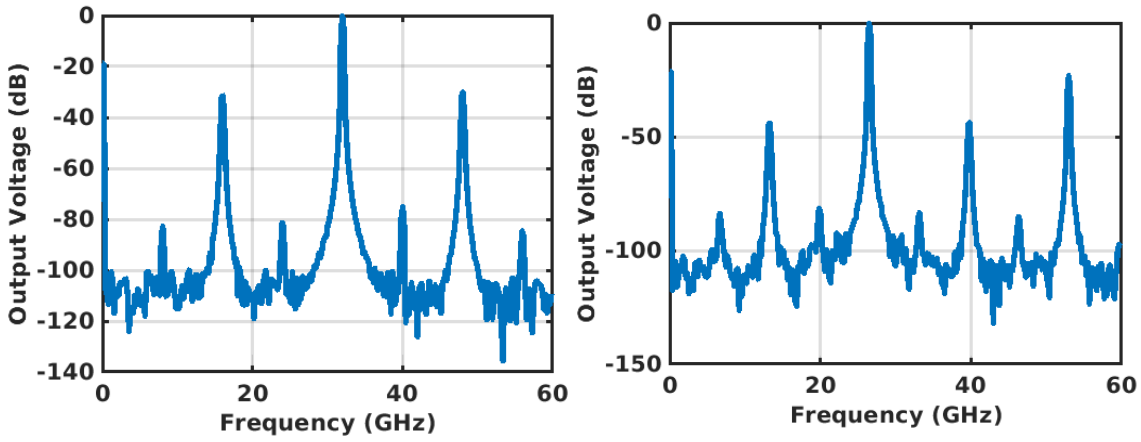


Figure 3.23: 60-GHz divide-by-8 outputs at each step

Fig. 3.24 shows the DFT results of the divider in slow-slow and fast-fast corners. From the SS corner in Fig. 3.24(a), we can divide a maximum of 64 GHz without any problems. From the FF corner in Fig. 3.24(b), we can divide a minimum of 53 GHz without any problems.



(a) (b)

Figure 3.24: Maximum divider frequency at SS corner (a), minimum divider frequency at FF corner (a(b)

3.4.3 Divide-by-15 Circuit

This divide-by-15 stage is used to divide 7.5 GHz input from the previous divide-by-8 to 500 MHz. The output of this circuit will drive the phase detector of the 60-GHz PLL. Unlike the previous divider, it has relaxed requirements in terms of speed.

As the divider architecture, the modular programmable divider from [46] is chosen. Fig. 3.25 shows the overall structure which is composed of 2/3 divider cells cascaded together with a modulus feedback. The operation is as follows. When the divider cell in 2/3 divider is in a division period, the previous cell generates the mod_{n-1} signal. This signal moves to the left side of the chain and throughout this movement it is clocked again in each cell along its way. With the p_n inputs, 2/3 divider cells decide the division ratio of each cell. If p_n is zero, the divided signal propagates through the chain from left to right without an additional period. If p_n is one, then the divider cell adds an extra period to the signal. With this operation, the output period can be calculated as:

$$T_{out} = 2^n.T_{in} + 2^{n-1}.T_{in}.p_{n-1} + 2^{n-2}.T_{in}.p_{n-2} + ... + 2^1.T_{in}.p_1 + 2^0.T_{in}.p_0 \qquad (3.22)$$

Alternatively, the division ratio ”N” can be expressed as:

$$N = 2^n + 2^{n-1}.p_{n-1} + 2^{n-2}.p_{n-2} + ... + 2^1.p_1 + 2^0.p_0 \tag{3.23}$$

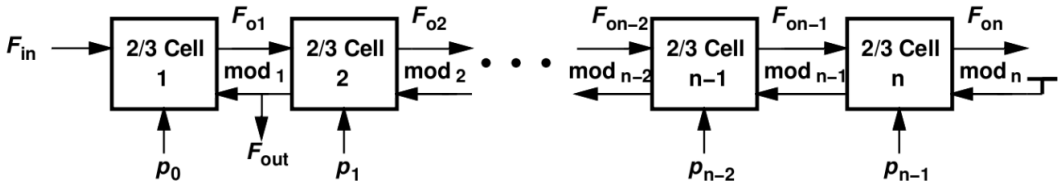


Figure 3.25: Modular programmable divider architecture

Since we need a divide-by-15 design in our PLL configuration, we would need 3 stages of dividers. By using the equation in 3.23, we can see that all p_n values must be equal to 1. In other words, each 2/3 divider cell must add an extra period to the divided signal.

A 2/3 divider cell consists of two blocks. The first block, where the signal propagates, is a divide-by-2 circuit which consists of 2 latches to form a d-flipflop divider as in Fig. 3.20. Second part of the circuit is called as ”end-of-cycle” logic which takes in the mod input from the preceding stage and with p input decides the division ratio of the cell. If the p value is 0, then end-of-cycle logic doesn't affect the division ratio and 2/3 cell divides the input frequency by 2. If p=1, then end-of-cycle logic forces the top divider to absorb an extra period. Logic circuit for 2/3 divider is shown in Fig. 3.26.

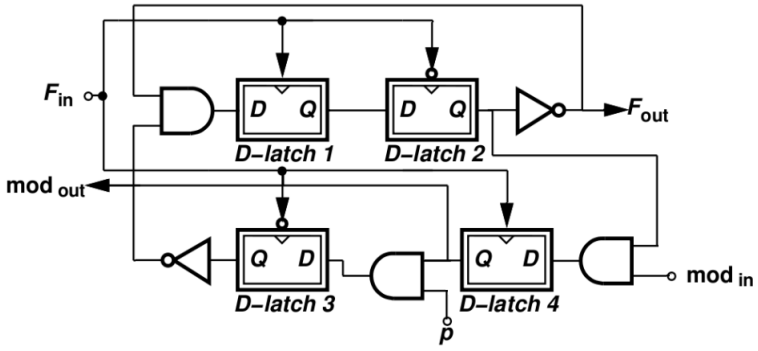


Figure 3.26: 2/3 divider cell logic diagram

All of the 2/3 divider cells consists of TSPC stages. It is an ideal choice for reduced clock loading and power consumption for the logic cells. Due to the reduced clock loading, it also benefits the circuit in terms of speed. A circuit diagram for 2/3 divider cell implemented with TSPC logic is given in the Fig. 3.27. The overall circuit divides the input clock from 7.5 GHz to 500 MHz with a total power consumption of 1 mW.

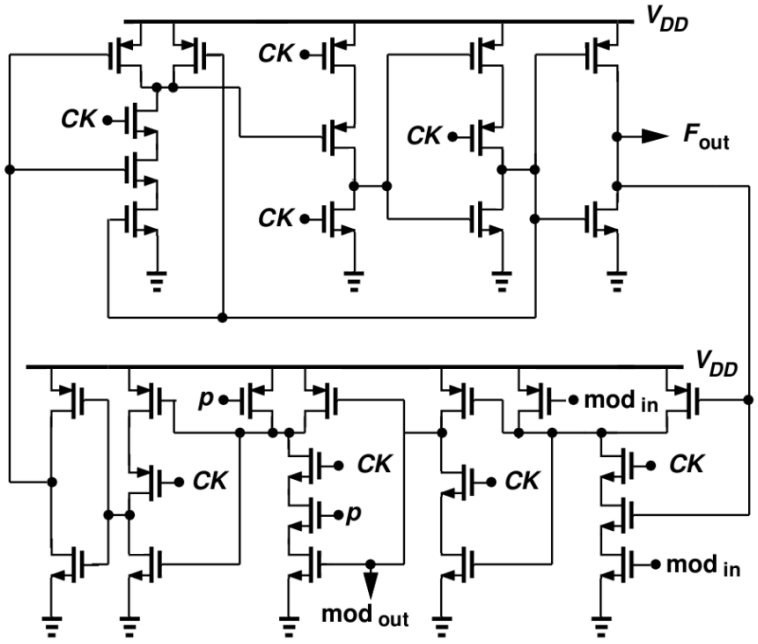


Figure 3.27: 2/3 divider cell circuit diagram implemented with TSPC logic

The timing diagram is given in the Fig. 3.28. When we look at the timing diagram for all of the outputs, F_{o1}, F_{o2} and F_{o3}, when the signals are high, there is an additional period where the signal remains high in all 2/3 divider cell outputs.

3.4.4 Master Slave Sampling Phase Detector

60-GHz PLL also uses a sampling phase detector to determine the phase difference between input and the reference. Unlike its higher frequency counterparts, this PLL uses a master-slave sampling stage as depicted in Fig. 3.16.

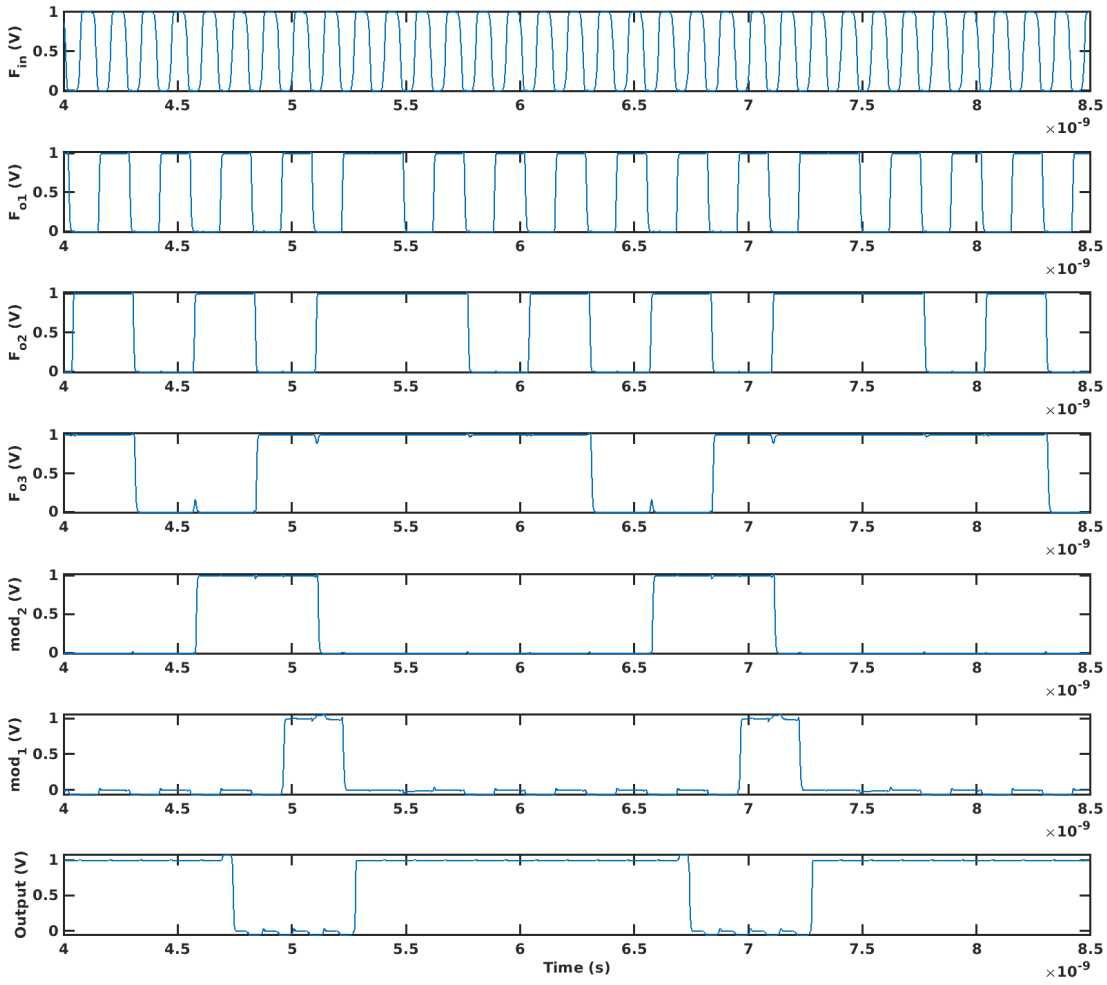
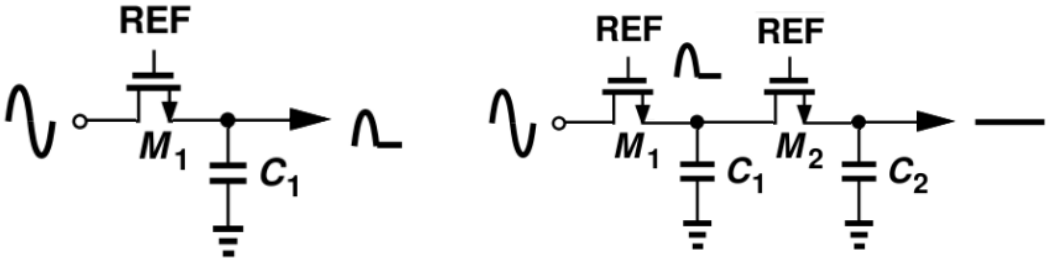


Figure 3.28: Simulation result for the divide-by-15 circuit with all 2/3 divider cell and mod outputs

A master slave sampling is more advantageous than a single stage sampling. Simply by sampling the signal at 2 different stages, we get a pure DC signal at the output. Fig. 3.29 shows a comparison of output signals when there is single stage sampling and when there is master slave sampling. With a single stage sampling, when the switch is on, we have a sinusoidal signal on the sampling capacitor. When the switch turns off, we sample the phase of the signal on the capacitor resulting in a pure DC as seen in Fig. 3.29(a).

For MSSPD sampling in Fig. 3.29(b), the DC part of the initial signal is sampled on the capacitor. This results in an output with a pure DC and a higher phase detector gain.



(a) (b)

Figure 3.29: Single stage sampling for phase detector (a), master slave sampling for phase detector (a(b)

In order to prove the increase in phase detector gain, let's start by analyzing single stage sampling. We would like to calculate the first fourier coefficient of the resulting signal in order to find the DC power, which is our phase detector gain, we can write the following equation:

$$a_0 = \frac{1}{T}[\int_0^{T/2} A.cos(\omega t + \theta)\, dt + \int_{T/2}^{T} A.cos(\theta + \pi)\, dt] \tag{3.24}$$

$$a_0 = \frac{1}{T}[\frac{A.sin(\omega t + \theta)}{\omega}\Big|_0^{T/2} - A.cos(\theta)\Big|_{T/2}^{T}] \tag{3.25}$$

$$a_0 = \frac{-Asin(\theta)}{\pi} - \frac{cos(\theta)}{2} \tag{3.26}$$

For small phase difference, $\theta = 0$, we can further calculate the phase detector gain as:

$$K_{PD} = \frac{-Asin(\theta)}{\pi} \tag{3.27}$$

$$K_{PD} = \frac{-A\theta}{\pi} \tag{3.28}$$

where the phase detector gain is scaled by $1/\pi$.

If we sample the phase using a MSSPD, we would directly sample the phase without any loss in voltage, assuming ideal sampling. Fig. 3.29(b) illustrates MSSPD sampling and the output signal. In this case, phase detector gain will be:

$$a_0 = K_{PD} = Asin(\theta) \tag{3.29}$$

For small phase difference, $\theta = 0$, we can further calculate the phase detector gain as:

$$K_{PD} = A\theta \tag{3.30}$$

which is π times higher than the single sampling stage.

The major reason why this is not used in the higher frequency PLLs is that MSSPD needs complementary clocks to operate and for those PLLs, the clock frequency is at 60 GHz. These switches are driven by the same 60-GHz VCO. In order to reduce the loading on the 60-GHZ VCO, we only use single stage sampling at those PLLs.

With a rail to rail swing coming from the divider and reference buffers, this phase detector is very ideal as it has high phase detector gain, pretty low power consumption and excellent phase noise performance. Due to its high phase detector gain, 60 GHz PLL doesn't have an additional amplifier at the output of this circuit.

3.5 Loop Performance for 60 GHz PLL

60-GHz PLL is a type 1 PLL like the previous PLLs as it contains only a single integrator at the loop. To analyze it more closely, let's take a look at the system diagram of the 60-GHz PLL in Fig. 3.30.

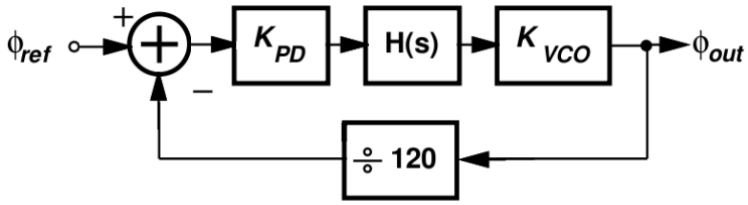


Figure 3.30: 60 GHz PLL system diagram

MSSPD acts as both a phase detector and a low pass filter in the loop due to its sampling nature. A sampling circuit in Fig. 3.31 can be approximated as an RC circuit at frequencies much lower than the sampling frequency with an equivalent R_s of $1/Cf_{ref}$. With a gain of K_{PD}, we can write

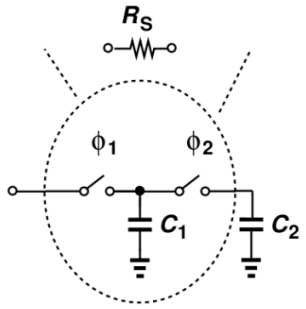


Figure 3.31: Equivalent circuit for an MSSPD

the transfer function of MSSPD as:

$$H_{PD}(s) = \frac{K_{PD}}{1 + sRC} \tag{3.31}$$

Equivalently,

$$H(s)_{PD} = \frac{K_{PD}}{1 + \frac{s}{f_{ref}}} \tag{3.32}$$

The open loop transfer function would be

$$\frac{\phi_{out,open}}{\phi_{ref,open}} = T(s) = 120H(s)\frac{K_{VCO}}{s} \tag{3.33}$$

The closed loop transfer function can be calculated as

$$\frac{\phi_{out}}{\phi_{ref}} = A_\phi(s) = \frac{120H(s)\frac{K_{VCO}}{s}}{1 + H(s)\frac{K_{VCO}}{s}} \tag{3.34}$$

For the phase noise analysis, we need to take a look at the phase noise contributions. Fig. 3.32 shows the phase noise contributions for this PLL. For each contribution, we can write the following equations to determine the total phase noise contribution of this PLL using superposition.

$$\phi_{n,out,VCO} = (\frac{1}{1 + T(s)})^2\phi_{n,VCO} \tag{3.35}$$

$$\phi_{n,out,lf} = (\frac{A_\phi(s)}{K_{PD}H(s)})^2\phi_{n,K_{PD}} \tag{3.36}$$

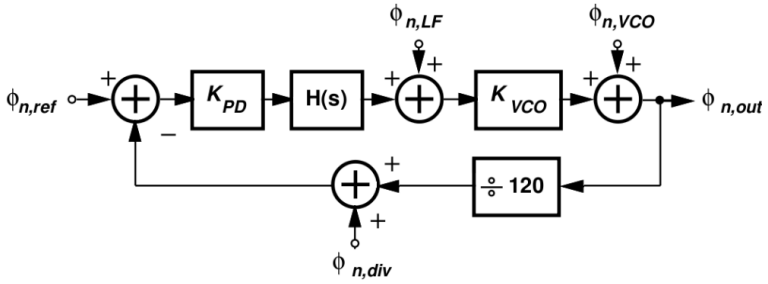


Figure 3.32: 60 GHz PLL noise contributors

Unlike high frequency PLLs, the noise contributions in this PLL contributes the most of the phase noise in the overall system. Once the reference is multiplied by 120, 120-GHz PLL and 300-GHz PLL components' noise contribution is negligible compared to the reference noise as we will prove later throughout simulations.

CHAPTER 4

Layout and Floorplanning

A crucial part of the design is the layout of the PLLs. Without correct layout and placement, it would be hard to correctly operate the system in harmony especially at 300 GHz. Since the frequency is very high, we need to be very careful about the placement as it may lead to a shift in frequencies or create high losses in the oscillation amplitudes, which would result in the loop not to lock.

First major concern is the design of the 300 GHz loop. From Fig. 3.2, we can see that 300 GHz VCO is driving the 180-GHz mixer from the output of the VCO. As the most vulnerable part of circuit in terms of oscillation frequency and amplitude, the mixer must be placed very close to the 300-GHz VCO to load the VCO with the least amount of parasitic capacitance. In terms of inductor radius, 300-GHz VCO radius is 16.75 μm and the mixer inductor radius is 27.5 μm . According to these dimensions, 300-GHz VCO and mixer inductors can be placed as in Fig. 4.1.

Fig. 4.1 reflects a very idealized picture in terms of the placement. 300-GHz VCO inductor is placed on the top side with mixer inductor is placed on the bottom side. As the transistors are placed very closely, this type of arrangement would provide the best swing from the 300-GHz VCO and at the output of the mixer. Another concern for a placement like this is the coupling between inductors.

Here we see another advantage of using a BFO. We have two inductors in the VCO that is coupled to each other. These inductors due to their strong coupling wouldn't couple with the neighboring inductors. Simulation results for a placement like in Fig. 4.1 would only result in a change of 300-GHz VCO frequency by 3.3 GHz and its amplitude by 62 mV even though when the bottom edges of the inductors are placed 10 μm apart.

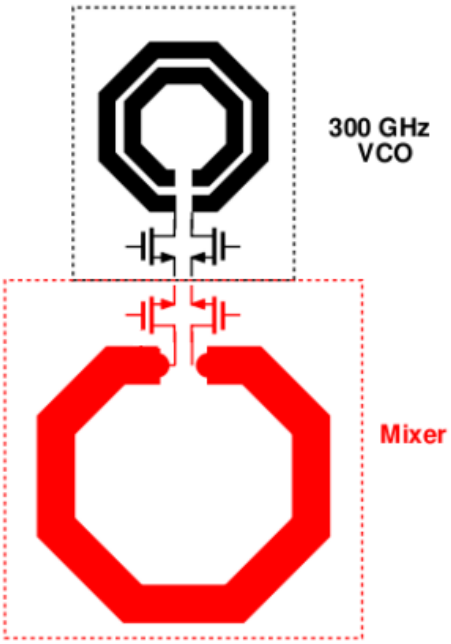
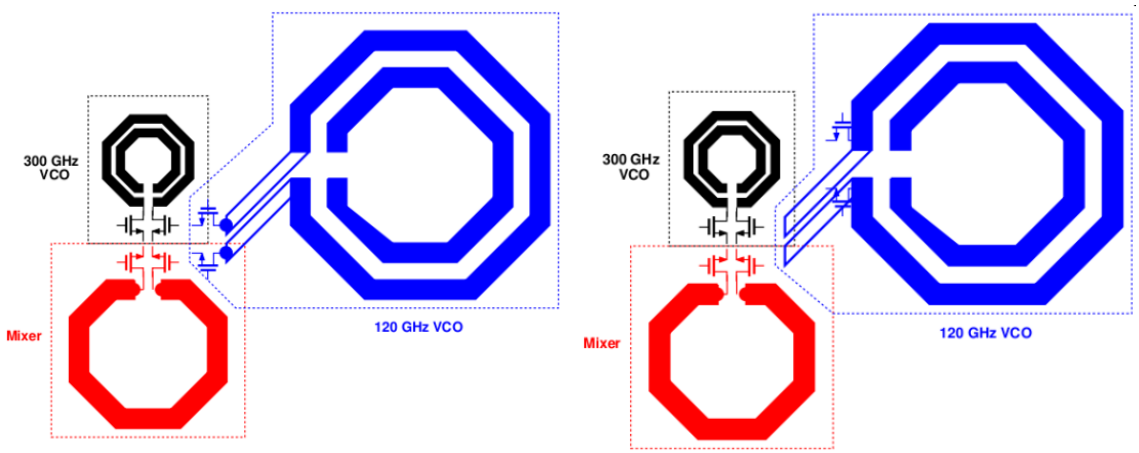


Figure 4.1: An idealized placement for VCO inductor and mixer inductor in 300 GHz PLL loop

For the remaining part of the 300-GHz loop, we can place the sub-sampler and the amplifier very close to the mixer, reducing the routing losses. The only long path is from the output of the amplifier driving the PMOS control transistor to adjust VCO frequency. However, due to the low frequency nature of that specific line, we can afford to a very long line as it wouldn't create much loss terms of the control voltage.

When we go to the next critical loop in our PLL design, we have 120-GHz PLL. In this PLL, we have a 120-GHz VCO again driving the mixer and differently from the other PLL, this VCO is driving its own subsampling stage. Building on top of our previous floorplan in Fig. 4.1, we can add the 120-GHz VCO inductors, which have an outer radius of 45.8 μm, right next to the small 300-GHz VCO inductors as in the Fig. 4.2 VCO transistors are directly connected to the sub-sampler without any extra routing. This type of arrangement brings some different challenges to the layout design. First of all, although not as vulnerable as 300-GHz VCO, 120-GHz oscillator is still prone to parasitic capacitances which can largely impact its oscillation frequency and amplitude.



(a) (b)

Figure 4.2: 120 GHz VCO inductor on the right side of 300 GHz VCO inductor and mixer inductor. 120 GHz VCO transistors are close to the other transistors (a), 120 GHz VCO transistors are at the VCO inductor (b)

A possible floorplan is to place the transistors away from the VCO inductor and closer to the mixer transistors as in Fig. 4.2(a). In this case, VCO transistors will be able to drive the mixer transistors however, due to significant distance from the inductor and the use of low level metals for routing from inductors to the transistors results in a high inductor resistance. This effectively reduces the Q factor of the VCO inductors and reduces the output swing of the VCO. When compared with ideal conditions (when the routing is minimum) from simulation results, it leads to a loss of 200 mV (1.6 dB loss).

Second option is to place the transistors close to the inductor have some routing from the transistors to the input of the mixer. This type of arrangement as in Fig. 4.2(b) would eventually lead to better VCO characteristics in terms of amplitude. Now since the inductor is directly connected to the transistors, this wouldn't reduce the Q value of the inductor. However extra routing using the lower metal layers from the output would lead to some resistive loading from the mixer combined with the gate resistance of mixer transistors. From the simulation results, although it is a better alternative from the previous routing, it still has a loss around 150 mV (1.16 dB loss). This amount

of loss might seem pretty small and manageable but unfortunately it has a large impact on the loop performance. The mixer, in order to operate properly, the transistors must be switched from on to off fully in a 8.33 ps. A switching like this requires a very large 120-GHz swing as the transistors suffer from speed degradation at such large frequencies. A reduction of 1.2 dB in amplitude results in a loss of 3.6 dB in the overall mixer gain at 180 GHz. A reduction of 1.6 dB in amplitude results in a loss of 4.8 dB in the overall mixer gain at 180 GHz.

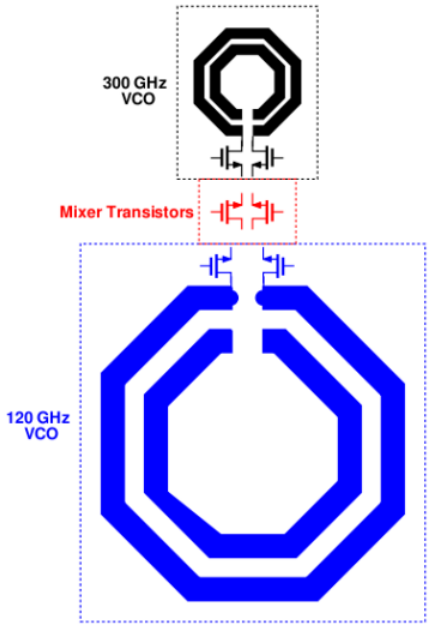


Figure 4.3: Layout placement for VCO inductors and transistors

We cannot afford to such a high loss at the mixer output. This may eventually lead to very small lock ranges or may prohibit the loop to lock. As a result, we propose the floorplan in the Fig. 4.3 where on the top side, we have 300 GHz VCO inductors directly connected to the 300-GHz VCO transistors, on the bottom side we have 120-GHz VCO inductors that is directly connected to 120-GHz VCO transistors. In order to minimize the routing to mixer transistors, we place those transistors right in the middle of two VCOs. With a routing like this, we would minimize the loading on both of the VCOs and get the best performance out of the them. There is still one question remains. Where should we place the mixer inductors?

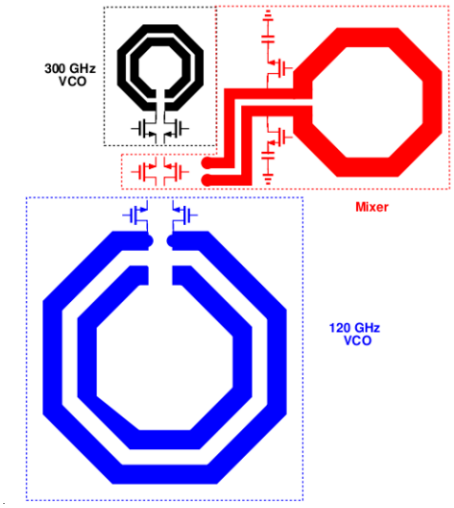


Figure 4.4: Layout placement for inductors and transistors

Since the center area is occupied by the VCO inductors, we need to place the mixer inductor to the side as in the Fig. 4.4. In order to reach to the inductor, we now need to travel some distance from the mixer to its inductor. One might say that this arrangement would again result to a lower mixer gain. In order to prevent the loss, we would offer some modifications to the layout.

First of all, we need to use thick metal layers to route the output of the mixer to its inductors. This would minimize the loss by the line resistances. It is true that these lines would add some inductance and slightly lower the Q-factor of the overall inductor. Second modification is the placement of the sub-sampler in the loop. Where is the correct location for the the sub-sampler? In order to answer this question, let's take a look at the Fig. 4.5.

According to Fig. 4.5(a), the sub-sampler is placed right at the mixer output. According to this scheme, the mixer output will experience the full reduction in Q-factor of the inductor. In addition to this, sub-sampler capacitance is directly contributing to the mixer load, reducing the resonance point. With reduced inductance and Q-factor, this leads to a decrease in output voltage by 0.9 dB.

Let's take a look at Fig. 4.5(b). In this case, the sub-sampler is connected right at the output of the extra routing inductance. The series inductor results in a shunt peaking of the voltage, given that we have the correct inductance value, ultimately boosting the voltage at the input of the sampler.

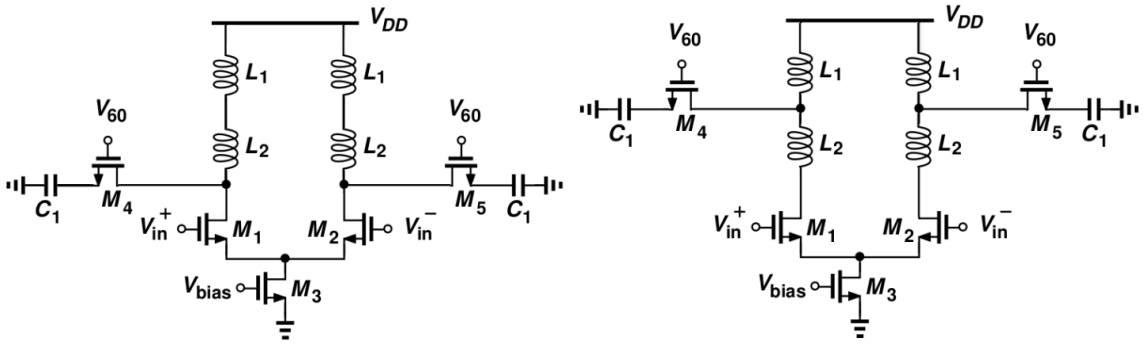


Figure 4.5: Different placements for the sub-sampler, right at the transistors (a), after travelling through some path (b)

In return, from the simulation results, this approach leads to a voltage gain of 0.1 dB at the input of the sub-sampler.

To summarize, by using a floor planning as in Fig. 4.4, we were able to get the best performance out of our PLL design. We preserved the best output voltage from our VCOs and mixer with minimal loss.

After the placement of high frequency PLLs, the only remaining block is the 60 GHz PLL. Now this PLL is generating a reference clock for the 120-GHz and 300-GHz PLLs so it is also an important block in the floorplanning. This VCO has 3 inductors in it, and in order to minimize coupling with other inductors, it needs to be placed on a separate empty area. Furthermore, the routing to the subsamplers must be minimized so that we would induce minimal loss to the 60-GHz signal.

60-GHz VCO uses a complementary cross coupled oscillator to get the desired oscillation as seen in Fig. 3.17. Inductor L1 has a value of 42 pH and inductors L_2 and L_3 have a value of 22 pH. In terms of inductor sizes, The radius of L1 is 20 µm. and the radius for L_2 and L_3 is 12 µm. With the given radii, the area of L1 is almost 4 times of L_2 or L_3. For the placement of the inductors of this VCO, we used the floorplan as in Fig. 4.6. The main inductor is placed at the top whereas the small inductors are placed at the bottom side. This layout gives us a modular layout for the 60 GHz

VCO.

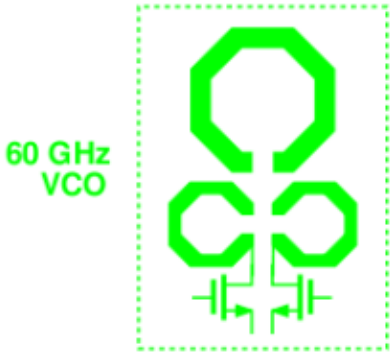


Figure 4.6: Layout placement for VCO inductors in 60 GHz VCO

Once the dimensions of the 60-GHz VCO are known, the next step is the placement of this VCO as close as possible to the sub-sampler of both of the PLLs. A nice and close placement might seem on the left hand side of the 300-GHz VCO as in Fig. 4.7. Since there are no inductors occupying that space, it seems like a fitting choice. However there is a one major concern in this placement. Although the VCO is very close to 120 GHz sub-sampler, it is not close to the sub-sampler of 300-GHz PLL. As explained before, the sub-sampler of 300-GHz PLL is placed closer to the mixer inductor to get a slight voltage boost at the input of the sampler. Since 300 GHz PLL is more critical than the 120-GHz PLL, we need to place 60 GHz VCO closer to the mixer inductors.

Fig. 4.8 shows the final placement of the 60 GHz VCO. Rather than placing the VCO to the left side of the 300 GHz PLL, we placed it closer to the mixer inductor. By this way, it is much closer to the 300-GHz sub-samplers. Now again, the question becomes whether we suffer losses due to the long lines coming from the VCO to the sampling transistors. Here we see the advantage of designing the sampling stages with only a single transistor sampling. This directly reduces the load on the VCO by half. Secondly, we do not have to drive 120-GHz and 300-GHz PLL with the same clock phase. Since both of them are different PLLs, we can actually use in phase output to drive 300-GHz PLL and complementary output to drive 120-GHz PLL simultaneously. This will also allow us to symmetrically distribute the loading to the VCO. For the voltage swing, we again

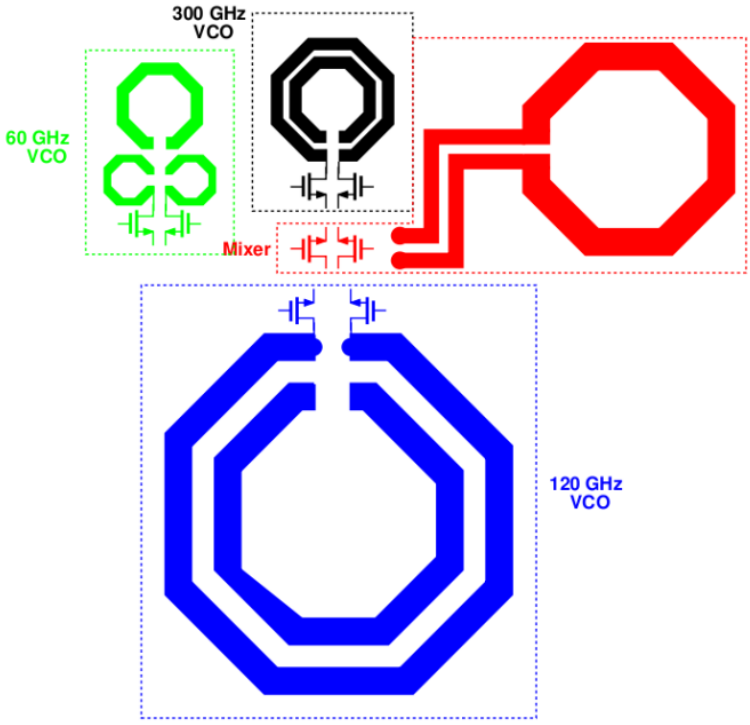


Figure 4.7: Layout placement for 60 GHz VCO inductors in the whole floorplan

try to use the shunt peaking effect explained previously to prserve the swing at the gates. Although the lines are lossy, due to the added inductance, the voltage at the gates of the switches, get a slight voltage boost of 32 mV peak-peak.

Due to high frequency nature of these circuits, we cannot rely on using simple component models to actually model our routings and inductors. We require a simulation method with a high accuracy with taking into account every coupling and electromagnetic effect in our design. These simulations are performed with HFSS which is a full 3D finite element method electromagnetic simulator. After the HFSS simulation, a valid spectre circuit model is created and used in Cadence to model all electromagnetic effects. For the VCOs' transistor routing, we relied on the parasitic extraction tool in cadence to extract correct capacitance and inductance. Simulating the parts, which include transistor routing, in HFSS requires high memory and high simulation times due to the small feature sizes, which is not feasible. Also small simulations for transistor routing both in

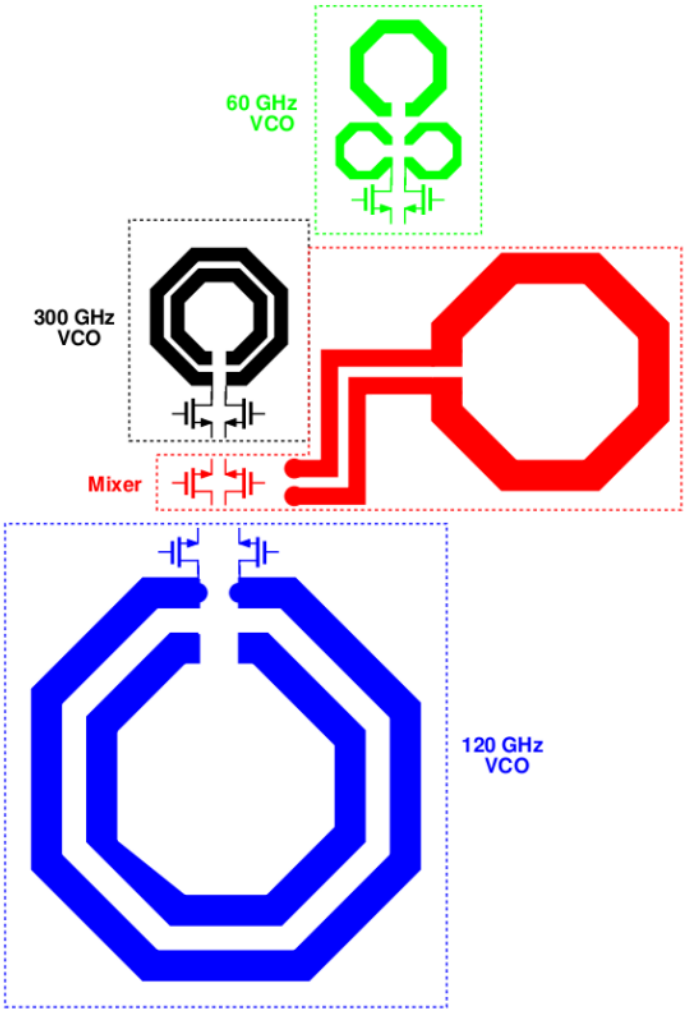


Figure 4.8: Final layout placement for 60 GHz VCO inductors in the whole floorplan

HFSS and parasitic extraction has the same results and as a result HFSS is used in the simulations of inductors and long routing, whereas parasitic extraction is used for transistor routing and smaller routings.

CHAPTER 5

Circuit Simulations and Results

Achieving a complete lock with the PLL system requires step by step locking. Firstly, 60 GHz PLL locks to the 500-MHz input reference and generates a 60-GHz signal at the output. Secondly, 120-GHz PLL takes in 60-GHz reference and generates 120-GHz at its output. Finally, with both 60-GHz reference and 120-GHz LO signal, 300-GHz PLL locks to 60-GHz. Fig. 5.1. shows the control voltages for all of the PLLs and sequential locking.

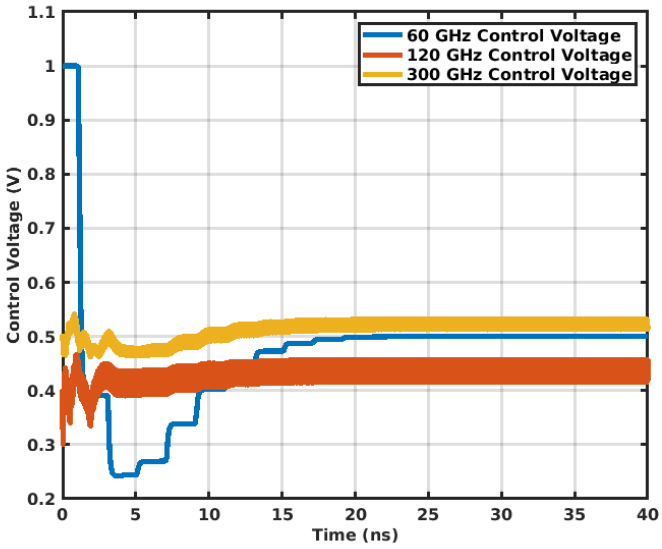


Figure 5.1: Control Voltages for different PLL's when locking

For the phase noise simulations, we have the results in Fig. 5.2 from the simulations. For 60-GHz PLL we can see different contributions from the existing sources. Firstly, we can see that the major noise contributor is the divider noise. Next, the major noise contributor is the sampling phase

detector combined with the loop filter. Reference crystal noise and buffer noise takes the 3rd major contributor for the overall phase noise. Last but not least, we can see the VCO noise contribution especially forming the majority of the PLL phase noise after the loop bandwidth.

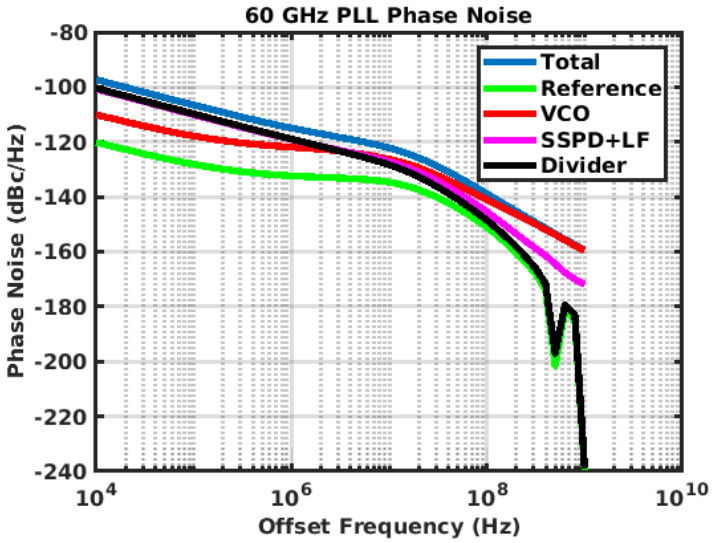


Figure 5.2: 60-GHz PLL's output phase noise and its noise contributors

120 GHz phase noise and its contributors are given in the Fig. 5.3. We only have VCO, subsampler and amplifier in this loop contributing to the phase noise. From the simulations, we can clearly see that other circuits have very small contributions for the phase noise when compared to the reference noise that is coming from the 60 GHz.

300 GHz phase noise and its contributions are given in Fig. 5.4. The phase noise contributors of this loop is very similar to the 120-GHz loop, with the dominant contributor is the 60-GHz reference noise. The mixer noise, subsampler noise and amplifier noise are all well below the reference noise where they can be ignored as a noise contributor.

5.1 On-Chip Downconversion Mixer

300-GHz output is a very high frequency to be measured using standard ways. Due to high frequency nature, transporting this signal to outside the chip would result in tremendous amount of

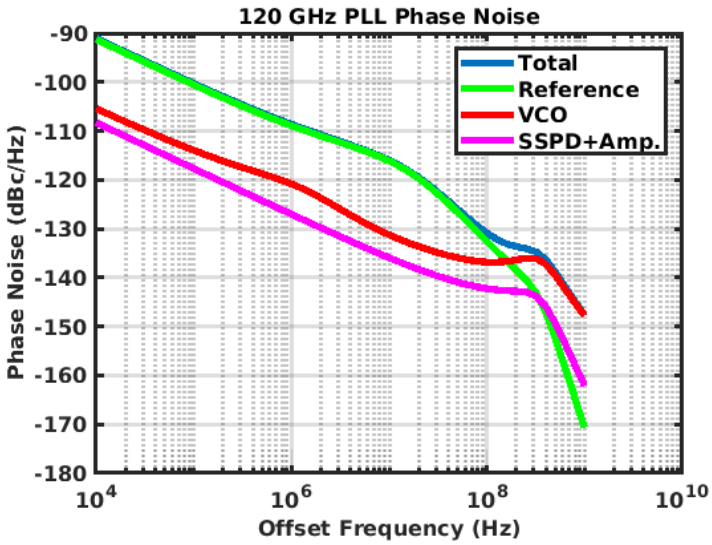


Figure 5.3: 120-GHz PLL's output phase noise and its noise contributors

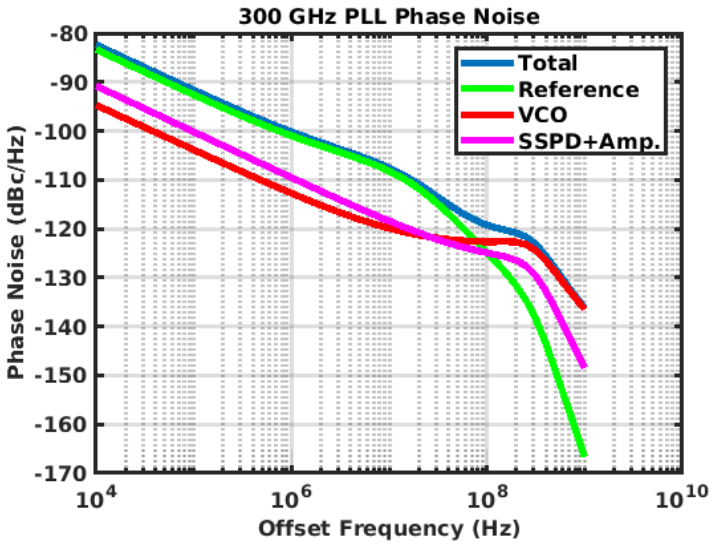
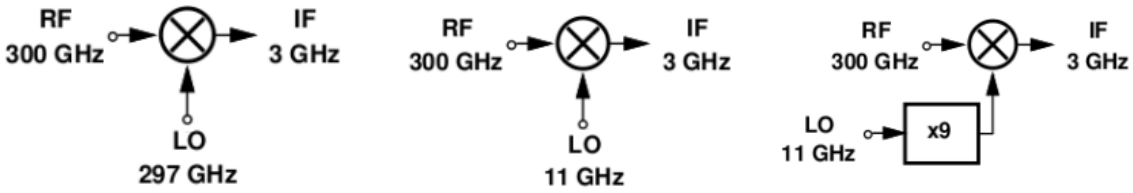


Figure 5.4: 300-GHz PLL's output phase noise and its noise contributors

losses. With the lack of amplifiers at these frequencies, this power loss could not be compensated. In addition to this, the lack of spectrum analyzers and phase noise analyzers at this frequency creates an additional challenge for the measurement.

We need to downconvert the signal to analyze it using conventional spectrum analyzers. This

downconversion can be done in a few ways. Firstly, we can use a mixer, that takes in 300-GHz as an LO, to perform the downconversion. Fig. 5.5(a) shows a downconversion scenario. With a high enough LO level, this would be an ideal downconversion scenario as it would provide the least amount of loss. The major problem with this scenario is the lack of the external high powered 300-GHz LO signal and also there are no fundamental mixers to do the downconversion.



(a) (b) (c)

Figure 5.5: Fundamental mixer with 297-GHz LO input to generate 3 GHz IF output (a), harmonic mixer which uses 27th harmonic with 11-GHz LO input to generate 3 GHz IF output (b), harmonic mixer which uses 3rd harmonic and x9 frequency multiplier to move input frequency from 11 GHz to 99 GHz to generate 3 GHz IF (c)

A second scenario, is to use a harmonic mixer to downconvert 300-GHz signal. With a harmonic mixer using 27th harmonic, we can eventually use regular high powered signal generators as LO and use it to downconvert 300-GHz output for measurements. Fig. 5.5 (b) summarizes the downconversion scenario. Only downside is the high loss of the mixer which is typically more than 60 dB.

A third scenario, is to use a high frequency source and combine it with a harmonic mixer of lesser order. This scenario is depicted in Fig. 5.5(c). Let's suppose we have a signal generator input of 11 GHz. We use a frequency multiplier by 9 and hence generate a high powered signal at 99 GHz. In the next step we connect this to the LO of the harmonic mixer. When the mixer downconverts using 3rd harmonic of LO, we would get 3 GHz as IF output which can be simply analyzed using conventional spectrum analyzers. In addition to this, we would get lesser conversion loss due to the low harmonic order of the mixer.

Now the second question that remains is how to get this signal out of the chip. An simple idea is to design an on chip antenna, that is connected to the output of the 300-GHz PLL. With a very high gain antenna, it would be possible to transfer the signal to another antenna which is connected to the test setup. Fig. 5.6 shows the test setup for transferring 300-GHz out of the chip.

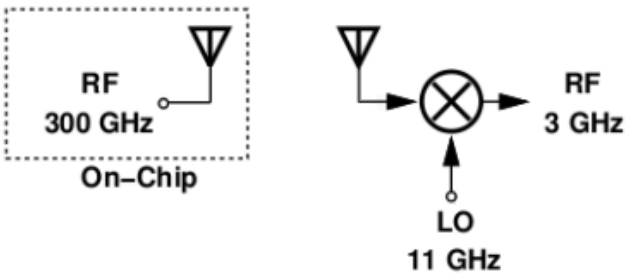


Figure 5.6: Measurement setup with an on-chip antenna

A high gain 50 Ω antenna at 300-GHz is not a simple task to do in a standard bulk CMOS process. Especially with lower channel lengths, the substrates have very high surface conductivity which lowers the on-chip antenna's efficiency and gain. High gain CMOS antenna designs at these frequencies often rely on backside radiation and employs a silicon lens at the backside to enhance radiation as in Fig. 5.7. Resulting antennas can have gain values more 10 dBi at 300-GHz [47–49].

The main problem of the on-chip antenna is that it needs to be at 50 Ω to be a very good radiator. Inside the chip, we only have the output of the VCO at 300-GHz. If we connect this antenna to the output of the VCO, we would eventually lower the quality factor of the resonator and hence significantly drop the output swing value. Eventually the oscillator might not even start since, as discussed before, the VCO needs 1/gm as the startup condition. Increasing transistor sizes, would help us in terms of gm but eventually reduce our oscillation frequency which is not a good tradeoff. Due to the being unable to drive 50 Ω with the current VCO, we cannot implement an on-chip antenna to transfer our signal to outside.

Another idea is to use a waveguide probe to take the signal directly out of the chip. But unfortunately, this method also falls short for the reasons previously listed. In order to take the signal

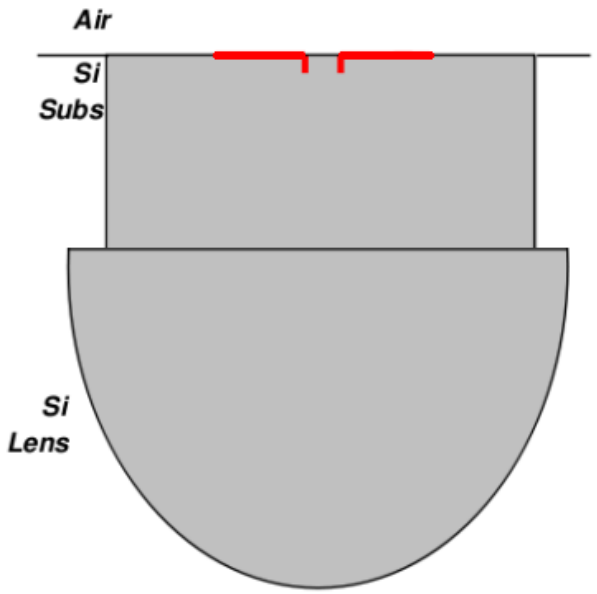


Figure 5.7: On-chip antenna with silicon lens to enhance gain

to the pads, we would need a 50 Ω transmission line on the chip taking signal from VCO to the 50 Ω probe. Transmission line would have lower loss when compared to the antenna setup when taking into account the path loss of the 300-GHz signal in the air. Unfortunately, the VCO would not be able to drive 50 Ω probe to transfer the signal out of the chip.

Since, it would be hard to take 300-GHz signal out of the chip directly, we should attempt to directly downconvert 300-GHz on the chip and take out the low frequency IF as an output. For the downconversion, we would use a structure in Fig. 5.8 where we generate a high frequency signal external signal and feed it inside the on-chip harmonic mixer for the downconversion. While getting the LO from outside, we should also make sure that we need the lowest loading on the VCO to minimize the mixer's effect on the VCO performance. In the Fig. 5.8, we simply take an LO frequency of 99 GHz and use an on-chip harmonic mixer which uses 3rd harmonic for downconversion.

We propose the structure in Fig. 5.9 as a harmonic mixer to downconvert 300-GHz to an IF frequency which can be detected and measured by the conventional spectrum analyzers. The har-

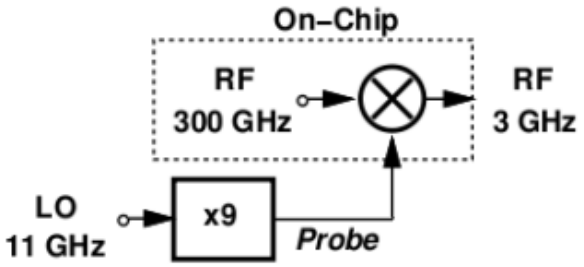


Figure 5.8: On-Chip harmonic mixer and external frequency multiplier for the test setup

monic mixer consists of only 2 transistors. M_1 is connected to the external LO input and the gate of M_2 is connected to the VCO. Size of M_2 is chosen as 400 nm to minimize the loading effect on VCO.

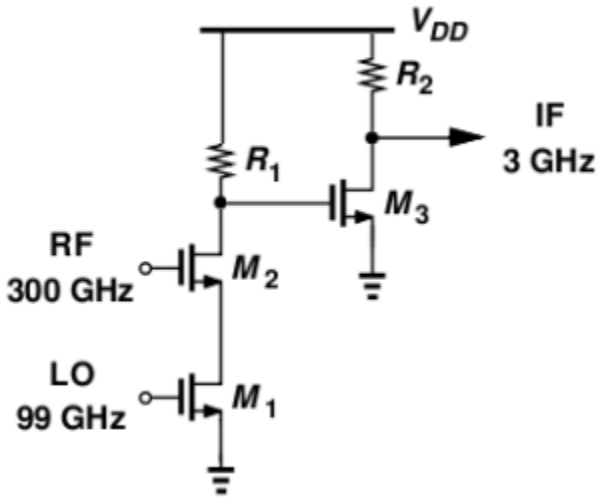


Figure 5.9: Harmonic mixer and output buffer

The transistors on the on-chip harmonic mixer is driven with high levels of voltage swings at their inputs. This gives an advantage in terms of minimizing the loss at the output of the mixer. In addition to this, we also added an open drain common source stage to drive the 50 Ω load at its output. There is only one missing element remains in the mixer design. How do we specify the DC current in the mixer?

The output of the frequency multiplier is a waveguide which means it is an open circuit at DC.

Therefore, we can provide on chip DC bias at the desired current level that would maximize our conversion gain. We connect a current mirror at the gate of the M2 to provide adequate bias and use 50 Ω as an isolation resistance. This 50 Ω resistance would also serve as a proper termination for the outside frequency multiplier, minimizing losses due to reflection. The full schematic of the on-chip mixer is given in Fig. 5.10.

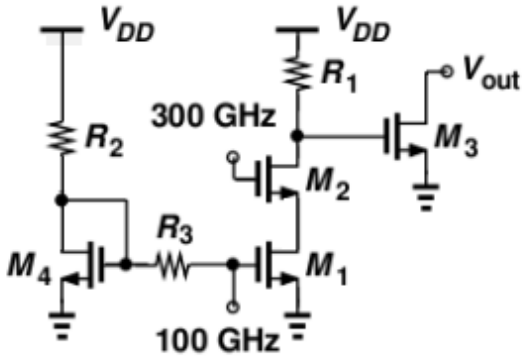


Figure 5.10: Harmonic mixer and output buffer and the current mirror

This on-chip harmonic mixer would deliver a -55 dBm output at IF frequency assuming 0 dBm swing at the LO input and 800 mV peak-to-peak VCO swing according to the simulation results. Fig. 5.11 shows a simulation result with 99 GHz as external input and 3 GHz as the IF frequency at the output of the mixer.

5.2 Measurement Setups and Results

The 300-GHz PLL is designed with 28-nm bulk CMOS process and manufactured by TSMC. The active area is 180 μm x 220 μm. Fig. 5.12 shows the die micrograph.

In order for the system to system to work, firstly 60-GHz PLL needs to lock to 500 MHz reference crystal, then 120-GHz PLL locks to 60-GHz reference. Finally, after these two PLLs lock, 300-GHz PLL can lock. As a result, we must firstly make sure that 60-GHz PLL locks. We do not have direct access to the 60-GHz VCO check the frequency of the oscillation, however, we have

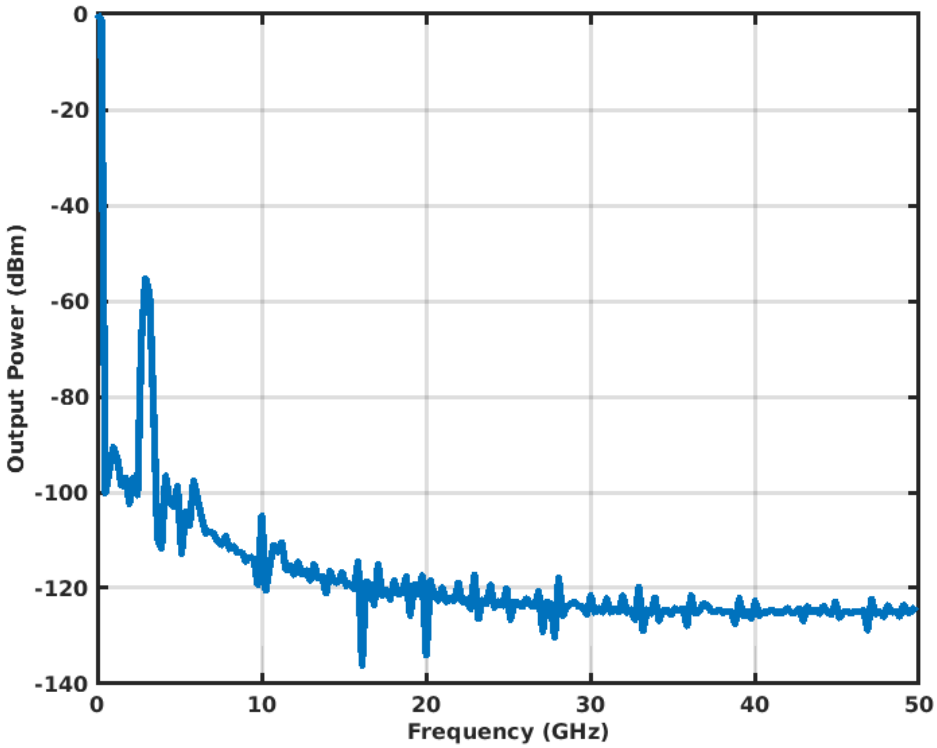


Figure 5.11: Downconverted output at 3 GHz with -55 dBm output power

access to the divider output. Since the output frequency is low, we can use a buffer to connect it to the spectrum analyzer to monitor its phase noise and frequency. Fig. 5.13 shows the 60-GHz circuit and the measurement setup for divider frequency. For the spectrum analysis, Fig. 5.14(a) shows the unlocked 500-MHz divider output, and Fig. 5.14(b) shows the locked waveform. Unlocked waveform has more noise when compared to the locked waveform.

The phase noise measure for this output is also trivial. The frequency is low and there is sufficient power at the output to measure the phase noise. The phase noise is measured by Agilent E5052A and Fig. 5.15 shows the phase noise result of this output.

Once 60-GHz PLL is locked, the next step is to lock 120-GHz PLL. Now this PLL has some challenges in terms of locking. The main problem for this PLL is that we do not have definitive output from the VCO itself and since it is operating as a subsampling PLL, it doesn't have any

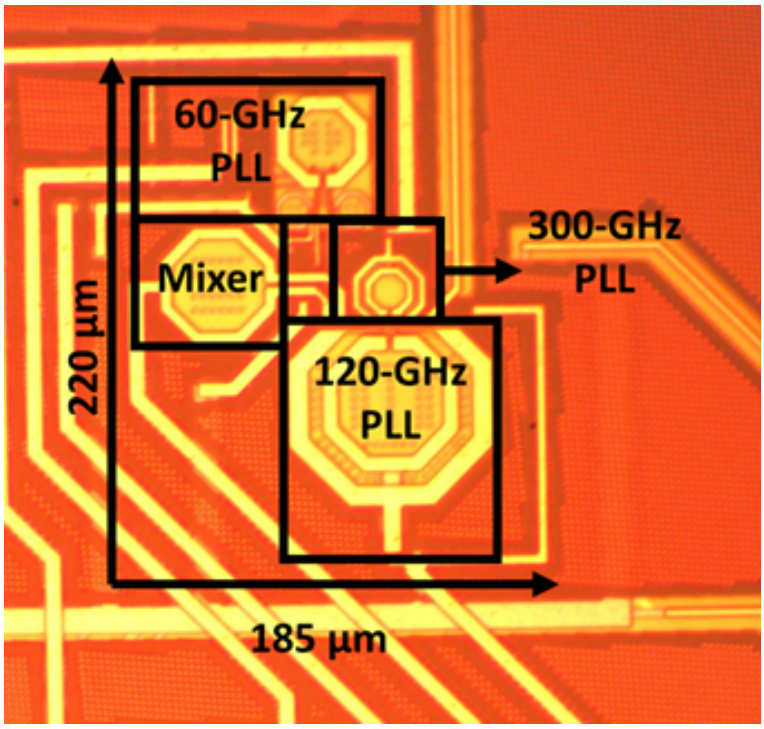


Figure 5.12: 300 GHz PLL chip micrograph. The active area is 180 µm x 220 µm

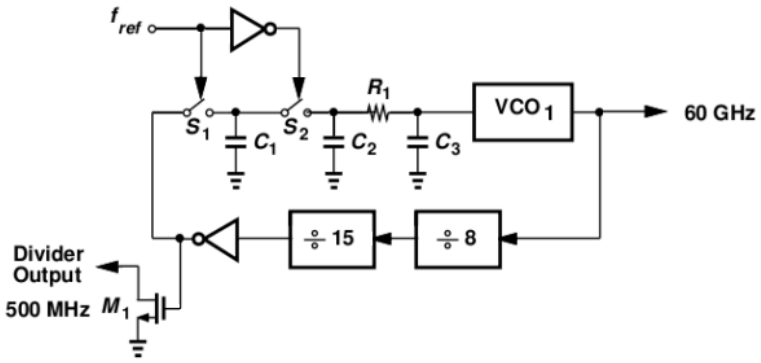
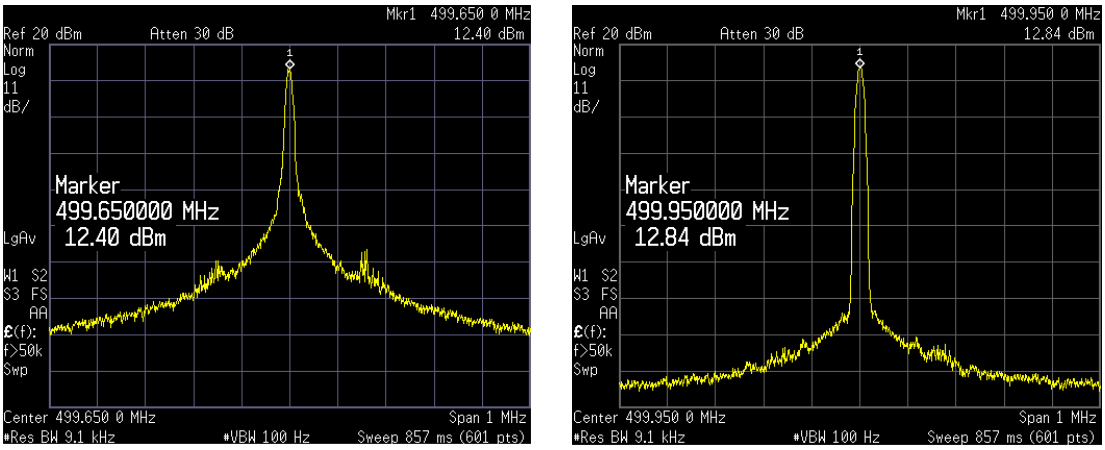


Figure 5.13: 500-MHz divider output measurement setup

divider output. Basically, there is no way for us to directly determine the frequency of oscillation in the VCO. In 120-GHz VCO, we have three capacitor banks and ability to change control voltage of the VCO for fine control of frequency.

Next question is since we don't know 120-GHz VCO output frequency, how can we determine whether 300-GHz PLL locks? We have an harmonic mixer at the output of the 300-GHz VCO.



(a) (b)

Figure 5.14: Spectrum of unlocked (a) and locked (b) 500-MHz divider outputs (b)

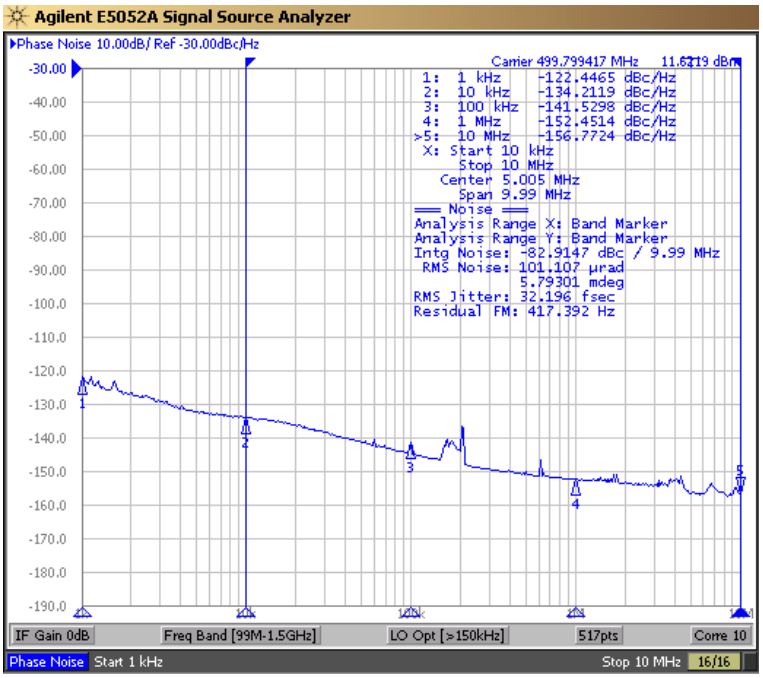


Figure 5.15: 500 MHz locked signal phase noise

Fig. 5.8 shows the measurement setup for this VCO. With the downconverted output, we can precisely determine the output frequency. We also have fine tuning methods as in the case of 120-GHz VCO. This PLL can only be locked if 120-GHz and 60-GHz PLLs are locked at the same time. So

the idea is we can precisely bring the output frequency of VCO to 300-GHz and search for correct 120-GHz PLL settings, to correctly adjust it to 120-GHz.

For measuring 300-GHz VCO output frequency, we use the setup in Fig. 5.16. Agilent E8257D signal generator generates us a frequency around 11 GHz and next this signal is fed into x9 frequency multiplier from Virginia Diodes WR9.0M-SGX module. This modules multiplies our frequency input by 9. Assuming the input is 11 GHz, this module will have an output of 99 GHz and this output will be transferred into the chip by a probe. The on-chip harmonic mixer will downconvert using the 3rd harmonic of the LO frequency and hence we would get 3 GHz IF output which can be measured using conventional spectrum analyzers. By only monitoring 500-MHz output frequency and 300-GHz output frequency, we can monitor the whole PLL operation.

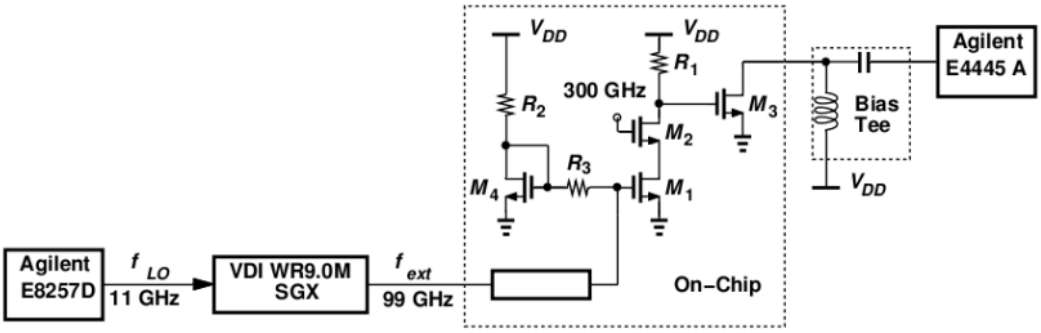
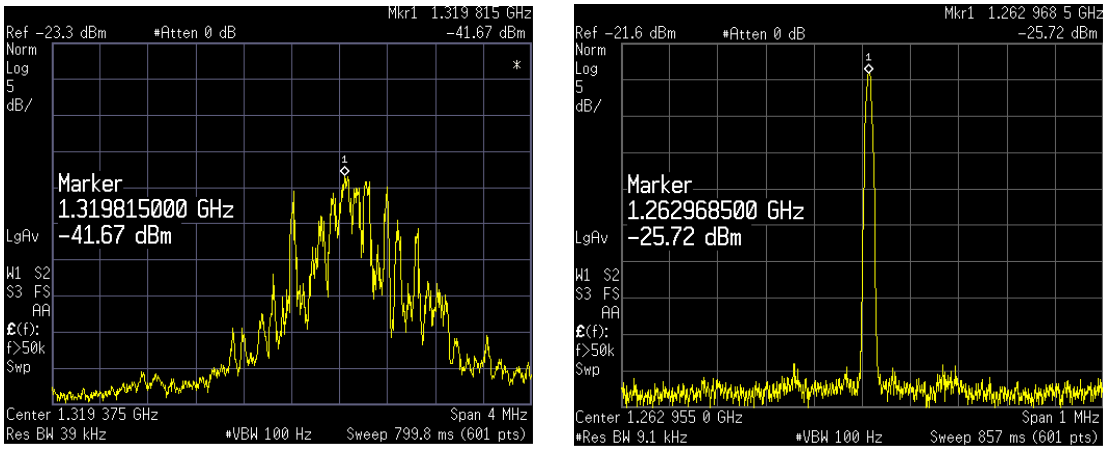


Figure 5.16: 300 GHz PLL output measurement setup for spectrum analysis

Extreme care has been taken to ensure that the measured output is a downconverted copy of the 300-GHz signal rather than a harmonic of f_{ext}. This is verified by three methods: (1) we change f_{ref} by Δf and observe that f_{out} changes by $600\Delta f$, (2) to ensure that $f_{IF} = f_{out} - 3f_{ext}$, we change f_{ext} by Δf and observe that f_{IF} changes by $3\Delta f$, and (3) we intentionally drive 120-GHz PLL or 300-GHz PLL out of lock and compare the resulting downconverted spectrum with that in the locked case. Fig. 5.17(a) shows the unlocked 300-GHz signal and Fig. 5.17(b) shows the locked signal at 300-GHz.

Once we achieve lock at 300-GHz, the next step is to measure the phase noise of the 300-



(a) (b)

Figure 5.17: Spectrum of unlocked (a) and locked (b) 300-GHz PLL outputs (b) For both cases f_{ext}= 99.54 GHz

GHz output. The harmonic mixer's output power is around -55 dBm and hence we need some amplifiers to raise the output power such that the signal analyzer can perform a good phase noise measurement. Fig. 5.18 shows the measurement setup for the phase noise analysis. We added 2 additional amplifiers to move the input signal from -55 dBm to 0 dBm. Agilent E5052A is capable of measuring the phase noise of the signals when the input power is more than -20 dBm. Fig. 5.19 shows the phase noise of the 300 GHz signal along with its jitter. According to these results, we have a phase noise of -100 dBc/Hz at 1 MHz offset.

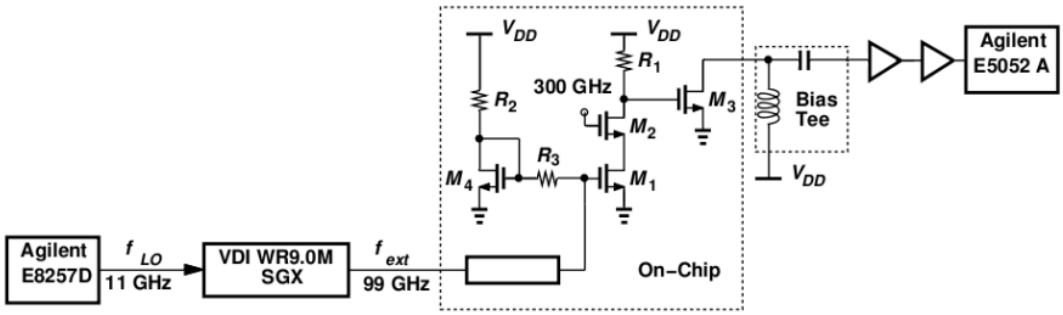


Figure 5.18: 300 GHz PLL output measurement setup for phase noise analysis

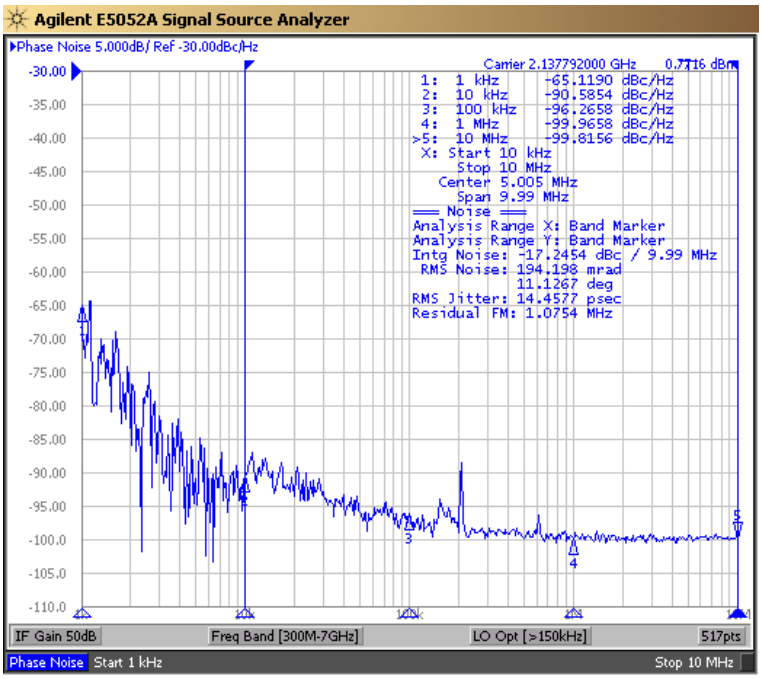


Figure 5.19: 300 GHz PLL downconverted phase noise. f_{ext}= 99.288 GHz

In addition to the phase noise performance, the PLL achieves a total locking range of 9.6 GHz starting from 298.2 GHz up to 307.8 GHz. This number corresponds to a tuning range of 3.2% while consuming 32 mW from 1-V supply (with reference buffers included) at 300 GHz. When the entire locking range is considered, the chip consumes between 30.8 mW to 35.1 mW.

The phase noise of the reference is measured by another phase noise analyzer because, the noise floor of Agilent E5052A is not adequate enough to measure this low noise. We used Rohde Schwarz FSWP 26 and measured the following for the phase noise of the crystal. At 500 MHz, the crystal has the phase noise depicted in Fig. 5.20. Total rms jitter integrated from 10 kHz to 10 MHz is 7.37 fs.

Table 5.1 summarizes the performance of our prototype and compares it with that of prior art for frequencies near 300 GHz. We point out that (1) our work targets communication links, hence the need for phase-locking, and (2) this LO generator is suited to drive upconverters and downconverters, but it does not act as a radiator. For a fair comparison, therefore, only phase-

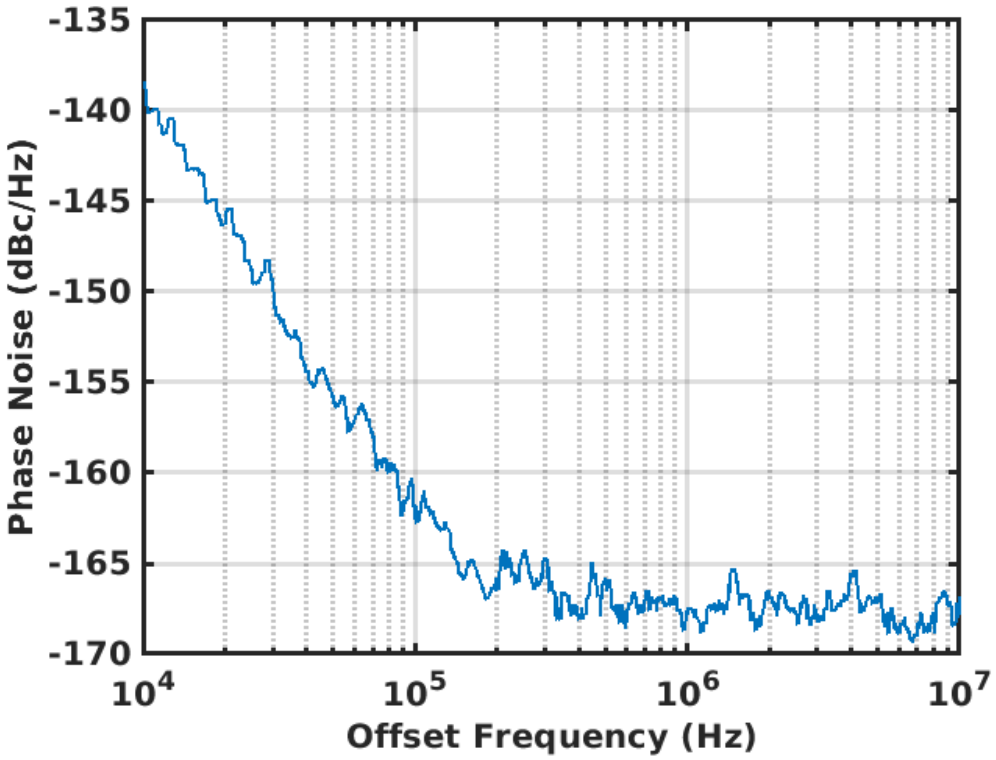


Figure 5.20: Phase noise of the crystal oscillator

locked generators containing on-chip VCOs are included in the comparison table.

	This Work	JSSC'14 []	IMS'11 []	JSSC'20 []	TTST'18 []
f_{min} (GHz)	297.3	280.3	300.7	198.0	282.3
f_{max} (GHz)	300.9	303.4	301.1	274.0	283.7
VCO Type	Fund.	3rd harm	Fund.	ILFM	3rd harm
Lock. Range	3.4%	7.9%	0.1%	29.3%	0.5%
Power (mW)	32	376	301	49	114
PN @ 1 MHZ (dBc/Hz)	−100.0	−82.5	−78.0 (@100 kHz)	−85.7	−78.6 (@10 MHz)
Tech. (nm)	28−nm CMOS	90−nm BiCMOS	InP HBT	65−nm CMOS	65−nm CMOS

Table 5.1: Comparison for state-of-the-art PLL's at 300 GHz

CHAPTER 6

Overall Receiver Architecture

The main challenge in the receiver architecture is to get a quadrature 300-GHz downconversion. A simple homodyne quadrature receiver is given in Fig. 6.1. Here, we assumed that we have a set of quadrature clocks at 300 GHz. If we would like to generate quadrature phases at 300-GHz, we can use quadrature hybrid as given in the Fig. 6.2.

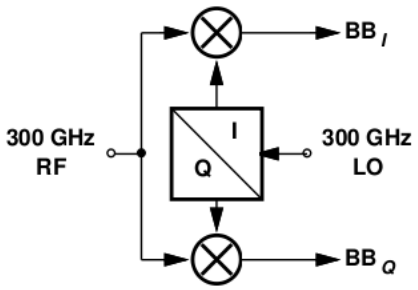


Figure 6.1: Homodyne receiver with IQ seperated clocks

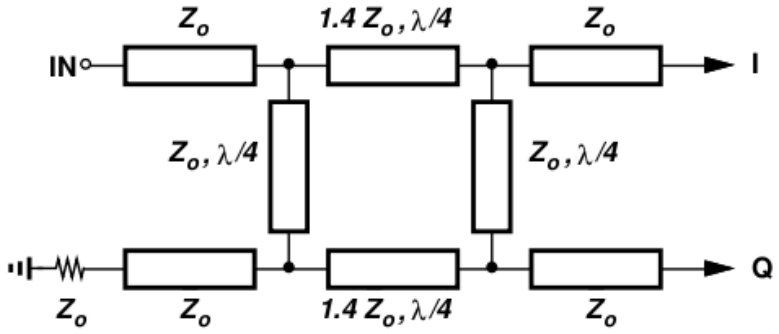


Figure 6.2: Quadrature coupler with quarter wavelength transmission lines

Unfortunately, as previous works, we cannot attempt to integrate a quadrature hybrid at 300-GHz to generate the necessary clocks. These quadrature hybrids must have 50 Ω input and output resistances so that it can be tuned to exact quadrature phases. However, our VCO cannot drive a 50 Ω load quadrature hybrid. With the VCO driving the quadrature hybrid, another issue is tuning the VCO frequency. Ideally, we would expect a quadrature hybrid to be 50 Ωat every frequency however real implementation with transmission lines as in Fig. 6.2 we can tune it to be 50 Ω at 300-GHz however, it will have a reactive component at other frequencies effectively lowering tank resonance frequency. Even if the VCO frequency is tuned out, the structure may not be tuned to the correct quadrature phase generation.

Secondly, assuming we have proper quadrature LOs at 300-GHz, we need to drive 2 mixers at the RF input. When the input is matched to 50 Ω, the RF path would suffer additional losses due to matching network and ultimately decreasing receiver performance.

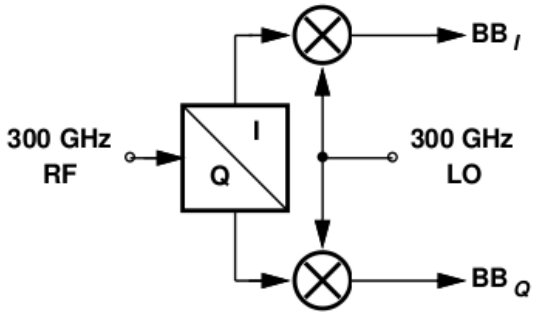


Figure 6.3: Homodyne receiver with IQ seperated input

Another approach for quadrature downconversion is to rather than the LO, we would convert the RF input. One possible advantage of this idea is that the RF input is already at 50 Ω and it is not connected to the VCO directly so there won't be any driving issue. However, since the hybrid is at the input, the loss of this network will directly be added to the noise figure of the entire receiver. An increase of more than 5 dB noise figure is not desirable in the receive chain. In addition to the noise figure, this quadrature hybrid must provide a wide bandwidth of phase and amplitude balance or otherwise it would lead to poor EVM and BER in the quadrature modulation.

Here, we would like to take advantage of the clock generation scheme. Firstly, we convert 450 MHz to 54 GHz using a PLL, and from this PLL we generate 108 GHz and 270 GHz. By adopting a heterodyne approach rather than homodyne approach in the receiver we can possibly achieve a quadrature receiving. Fig. 6.4 shows a simplified heterodyne approach. The first RF mixer mixes with 270 GHz, bringing down 300 GHz input down to 30 GHz. Secondly quadrature IF mixer, uses quadrature 27 GHz LO to bring 30 GHz down to 3 GHz baseband. This approach solves 3 issues. First, we keep only a single input mixer, reducing input load and effectively the noise figure. Secondly, we do not attempt to generate quadrature LO at 270-GHz which would be very hard with the current VCO structure, therefore preserving current VCO. Thirdly, by also not using quadrature conversion at the RF path, we avoid from additional loss and noise figure that this path might suffer due to quadrature conversion.

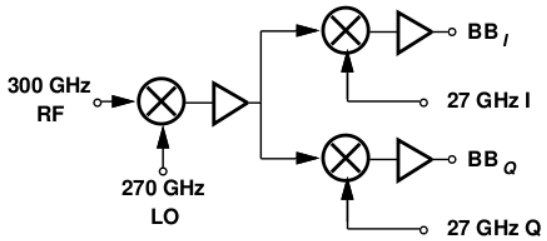


Figure 6.4: Heterodyne quadrature receiver

Due to the clock generation scheme, we have these signals locked and available from the PLL. If we look closely to the clock generator in Fig. 6.5 we can see that 270 GHz is available at the output of the PLL. For quadrature outputs, we add additional 2 divide-by-2 circuits at the output of 54 GHz PLL, giving us the necessary quadrature clocks. As a result, this the receiver architecture in Fig. 6.4 becomes feasible.

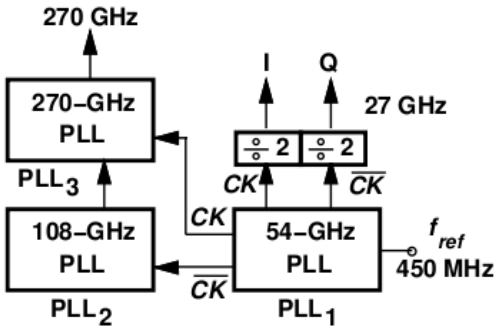


Figure 6.5: Clock generator for the heterodyne receiver

6.1 RF Mixer Design

The mixer constitutes the most important part of the receiver since we cannot afford to place a low noise amplifier at the input of the receive chain, we need to use a good mixer with the lowest noise figure and lowest loss available.

We can start analyzing the receive chain with the passive single balanced mixer in Fig. 6.6 (a) loaded with capacitors. In order to calculate the conversion gain, we will make a few assumptions. Let us assume that the transistors are ideal switches, and swings are sharp enough to fully switch the transistors. Fig. 6.6 (b) shows the approximate circuit to calculate the conversion gain.

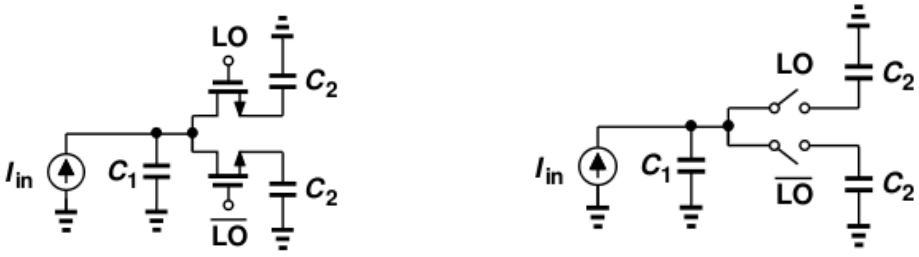


Figure 6.6: RF mixer simplified (a), approximate structure to model gain (b)

Now in this circuit we assume that we have a current source at the input. We will come to the point why we can approximate the input as a current source. Let us analyze the current waveform on the capacitor. When the switch is on, the current charges the capacitor, leading to output voltage tracking the input. When the switch turns off, all the current is steered to the other side. Assuming we have a capacitor connected to the input as in Fig. 6.7, we can assume the current waveform on the capacitor becomes like in Fig. 6.7 where it involves an impulsive current going from one side to the other side.

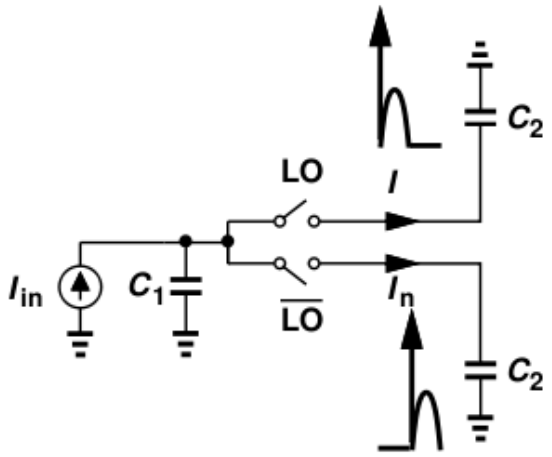


Figure 6.7: Mixer current waveforms going into the load capacitors

At half of the LO period, the current I_C charges the capacitor. and at the second half of the period, the current becomes zero as the switch turns off. When the switch turns on, an impulsive current immediately charges the load capacitance, up to the desired level. We can analyse the two behaviours separately and add both of the results together to find the conversion gain of the structure.

Let's start with the analysis of the voltage using the regular waveform. For $(n-1)T < t < nT-T/2$, we have current I_C charging the capacitor and current becomes 0 when we go to $nT-T/2 < t < nT$.

When we take the fourier transform of this current waveform, we get:

$$V_C = \frac{I_C.cos(\omega_{RF}t).rect(\omega_{LO}t)}{j\omega_{RF}C_2} \tag{6.1}$$

Which gives a conversion gain of:

$$V_C = \frac{I_C * 2}{j\omega_{RF}\pi C_2} \tag{6.2}$$

For the impulsive part of the current, the analysis is not as straightforward as this part. The impulsive current is formed due to charge sharing between C_1 and C_2 which are at different voltage levels. We will analyze the total current by writing the initial and final voltages on the capacitors as illustrated in Fig. 6.8

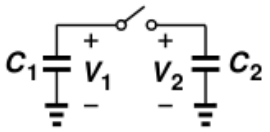


Figure 6.8: Charge sharing between transistors

With the voltages and capacitances in Fig. 6.8, the final voltage on the capacitors can be written as:

$$V_f = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} \tag{6.3}$$

By the initial voltage values depicted in Fig. 6.8 and Eq. (6.3), we can derive the final voltage on the capacitor as:

$$V_f = \frac{\frac{C_1I_C(nT)}{j\omega_{RF}C_2} + \frac{I_C(nT - T/2)}{j\omega_{RF}}}{C_1 + C_2} \tag{6.4}$$

With this final voltage, we can derive the impulsive current I_{imp} as:

$$I_{imp} = (\frac{\frac{C_1I_C(nT)}{j\omega_{RF}} + \frac{C_2I_C(nT - T/2)}{j\omega_{RF}}}{C_1 + C_2} - \frac{I_C(nT - T/2)}{j\omega_{RF}})\delta(t - nT) \tag{6.5}$$

$$I_{imp} = (\frac{C_1I_C(nT)}{j\omega_{RF}(C_1 + C_2)} + \frac{C_2I_C(nT - T/2)}{j\omega_{RF}(C_1 + C_2)} - \frac{I_C(nT - T/2)}{j\omega_{RF}})\delta(t - nT) \tag{6.6}$$

$$I_{imp} = (\frac{C_1 I_C(nT)}{j\omega_{RF}(C_1+C_2)} - \frac{C_1 I_C(nT-T/2)}{j\omega_{RF}(C_1+C_2)})\delta(t-nT) \tag{6.7}$$

With the impulsive current found, we need to determine the fourier coefficient of the downconverted signal. Here we assume $I_C(t) = Icos(\omega_{RF}t)$. The impulsive current becomes:

$$I_{imp} = (\frac{C_1 Icos(\omega_{RF}nT)}{\omega_{RF}(C_1+C_2)} - \frac{C_1 Icos(j\omega_{RF}(nT-T/2))}{j\omega_{RF}(C_1+C_2)})\delta(t-nT) \tag{6.8}$$

$$I_{imp} = \frac{C_1}{j\omega_{RF}(C_1+C_2)}(Icos(\omega_{RF}nT) - Icos(\omega_{RF}(nT-T/2))\delta(t-nT) \tag{6.9}$$

By using addition formula in cosine, we can further simplify this equation:

$$I_{imp} = \frac{C_1}{\omega_{RF}(C_1+C_2)}[Icos(\omega_{RF}nT).(1-cos(\omega_{RF}T/2)) - Isin(\omega_{RF}nT).sin(\omega_{RF}T/2)]\delta(t-nT) \tag{6.10}$$

We can convert all these equations to time domain, since impulse function has non-zero values at $t = nT$.

$$I_{imp} = \frac{C_1}{\omega_{RF}(C_1+C_2)}[Icos(\omega_{RF}t).(1-cos(j\omega_{RF}T/2)) - Isin(\omega_{RF}t).sin(\omega_{RF}T/2)]\delta(t-nT) \tag{6.11}$$

Let's take a look at the multiplication of cosine with infinite impulses at time domain. However, in Fourier domain, we can use convolution to find the frequency response of the term $Icos(\omega_{RF}t).\delta(t-nT)$.

The Fourier transform of cosine equals to two impulses:

$$F(\omega) = 0.5[\delta(f-f_{RF}) + \delta(f+f_{RF})] \tag{6.12}$$

The Fourier transform of the impulse train is again an impulse train:

$$H(\omega) = \frac{1}{T}\sum_{n=-\infty}^{\infty}\delta(f-n/T) \tag{6.13}$$

If we write the convolution integral in the fourier domain:

$$\int_{-\infty}^{\infty}\frac{1}{2T}\sum_{n=-\infty}^{\infty}\delta(\tau-n/T)[\delta(f-\tau-f_{RF}) + \delta(f-\tau+f_{RF})]d\tau \tag{6.14}$$

By using the sifting property of the impulse function and use the equality $f_{LO} = 1/T$, we can get the following:

$$\frac{f_{LO}}{2}[\sum_{n=-\infty}^{\infty} \delta(f - f_{RF} - nf_{LO}) + \sum_{n=-\infty}^{\infty} \delta(f + f_{RF} - nf_{LO})] \tag{6.15}$$

We are only interested in the downconverted waveform for the mixer problem where n=1 and n=-1. As a result, we get:

$$\frac{f_{LO}}{2}[\delta(f - f_{RF} + f_{LO}) + \delta(f + f_{RF} - nf_{LO})] \tag{6.16}$$

Going back to the time domain:

$$I_{imp,cos} = f_{LO}cos(\omega_{IF}t) \tag{6.17}$$

We can apply the same for the sine part of the impulsive current and get the downconverted waveform as:

$$I_{imp,sin} = f_{LO}sin(\omega_{IF}t) \tag{6.18}$$

When both of the currents are combined, we can simply obtain the downcconverted current as:

$$I_{imp} = \frac{C_1}{j\omega_{RF}(C_1 + C_2)}[I.f_{LO}.cos(\omega_{IF}t).(1 - cos(\omega_{RF}T/2)) - I.f_{LO}.sin(\omega_{IF}t).sin(\omega_{RF}T/2)] \tag{6.19}$$

The current would have both a sine and a cosine part which creates a real and imaginary part for the impedance although we haven't assumed any resistance in the circuit. Final step is to calculate the total current gain in this mixer.

$$I_{IF} = I_{rect} + Iimp \tag{6.20}$$

$$I_{IF} = \frac{C_1}{j\omega_{RF}(C_1 + C_2)}[I.f_{LO}.cos(\omega_{IF}t).(1-cos(\omega_{RF}T/2))-I.f_{LO}.sin(\omega_{IF}t).sin(\omega_{RF}T/2)]+I\frac{2}{\pi} \tag{6.21}$$

For current I, we also need another equation to represent it in terms of input current and capacitors. The term $sin(\omega_{RF}T/2)$ term is close to zero because $f_{RF} = 1.1f_{LO}$ We will assume that the input almost sees the total capacitance of C_1 and C_2. The current value I can be simply approximated as

$$I = I_{in}\frac{C_2}{C_1 + C_2} \tag{6.22}$$

The mixer has the following trade-offs. Firstly, the conversion gain must be maximized. Secondly, noise figure of the receiver must be minimized. We need to see how these numbers are traded with each other and take some precautions accordingly.

Now to answer why we are using a current source to approximate the input, we use an additional inductor at the input. This inductor forces the current passing through it remain ideally constant. The only question that remains is to maximize the current that is going into the circuit.Let's take a look at 2 different circuits. In Fig. 6.9(a), we have 50 Ohm source directly connected the RF mixer. C_1 represents the input capacitance coming from the mixer parasitics and C_2 represents the load capacitance. In Fig. 6.9 (b) we have an additional inductor to resonate this capacitance. We have shown that the mixer input impedance can be approximated as a capacitance of $C_1 + C_2$.

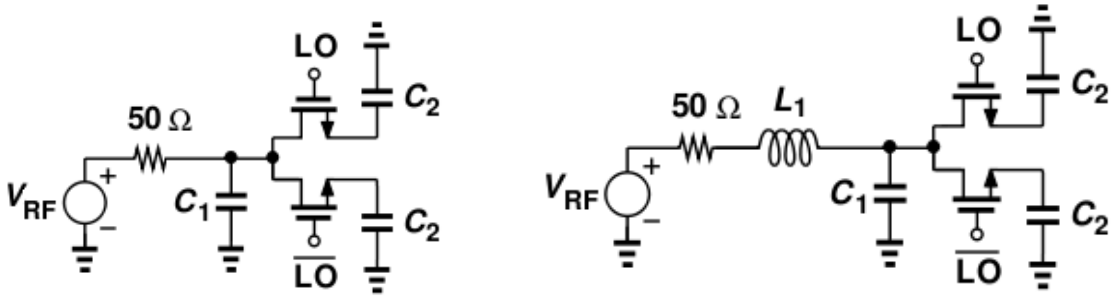


Figure 6.9: Mixer directly connected to 50 Ω input (a), mixer connected to input with a resonating inductor (b)

When we look back to the circuit in Fig. 6.9, we can now clearly see why the inductive resonance provides us a better gain for the mixer. Let's assume that we have a lossless inductor at the input of the mixer and neglect the upconverted resistance due to being very large when compared to the input capacitance. With 50 Ω input source, we can get the following input current:

$$I_{in} = \frac{V_{RF}}{50 + j\omega L - \frac{1}{\omega C}} \tag{6.23}$$

At resonance, this equation simplifies to:

$$I_{in} = \frac{V_{RF}}{50} \tag{6.24}$$

At resonance, the value of C_1 determines how much current goes into the capacitor C_2. Another benefit is that due to resonance, we can get a higher voltage swing at the input, which would in return reduce the noise figure and increase receiver gain.

This input capacitance depends mainly on the mixer transistor sizes because transistor parasitics like C_{gs} is directly added as a capacitance between input and ground.

Transistor size is a major determining factor for the performance of the mixer. Increasing transistor size would decrease the on resistance of the transistors, eventually increasing gain and decreasing noise contribution from the mixer. It would also increase the total capacitance seen at the input, leading to a decrease in the voltage gain of the receiver. By keeping input capacitance low, we can get some voltage gain at the input with the help of the inductor. This voltage gain would suppress the mixer noise contribution too, effectively reducing the overall noise figure more than the change in on resistance.

Output capacitance is also a major factor in determining the mixer performance. Mixer gain would decrease with increasing capacitance. Also, the output noise would decrease with increasing capacitance due to the kT/C nature of the output noise. The output capacitance overall needs to be optimized for the best gain and lowest noise figure possible. When the load capacitance decreases, mixer gain increases, the input referred capacitance decreases. Overall gain increases, the voltage gain from source to mixer input increases. This voltage increase increase counters some of the noise figure increase due to kT/C noise increase however there is an optimum point in the NF according to simulations where the NF is minimum and gain is maximum.

Fig. 6.10 shows the final mixer schematic with component values. The load capacitances are generated by the IF amplifier's input transistors. With these values, the resulting receiver gain and noise figure are given in Fig. 6.11(a) and Fig. 6.11(b) respectively. These numbers do not include the pad and transmission line losses at the input. When we look at the gain vs. frequency graph

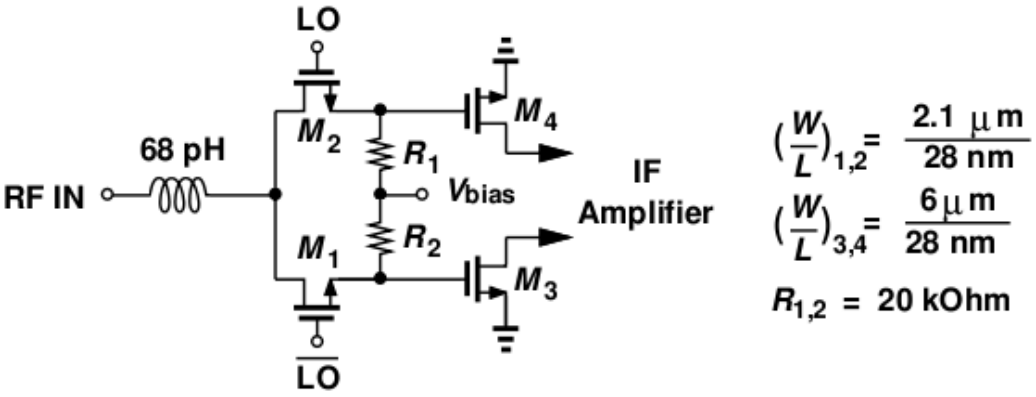
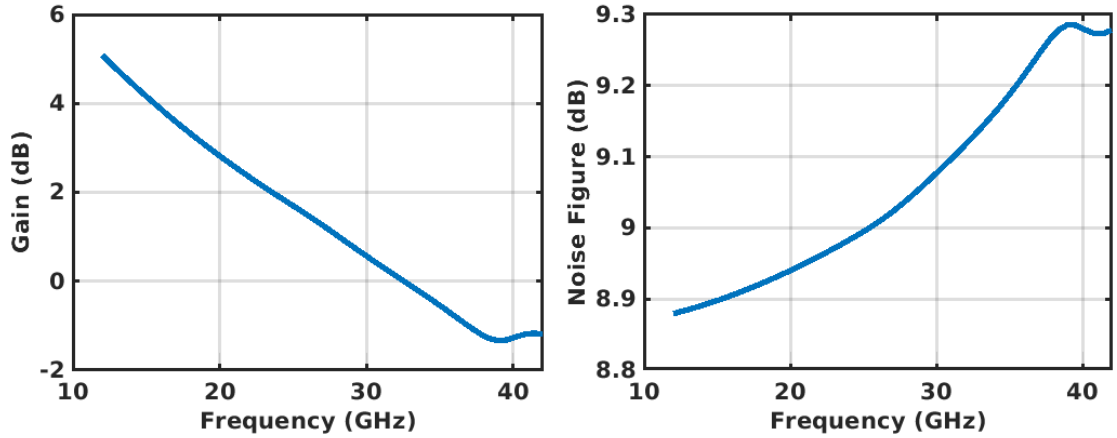


Figure 6.10: RF mixer schematic with component values

in Fig. 6.11(a), we notice that the gain goes down with a slope due to the load capacitance. At 27 GHz, we get 1.26 dB gain and 9 dB NF.



(a) (b)

Figure 6.11: RF mixer gain(a) and noise figure for downconverted signal (b)

6.2 IF Amplifier

This amplifier is the first amplification stage in the receiver stage. The input frequency from the mixer is around 27 GHz and this amplifier must have a large bandwidth to accompany the high

bandwidth around 20 GHz. We would like to get an amplification of more than 10 dB with only a single stage amplifier.

A simple differential amplifier can be suitable enough to generate the gain necessary for the IF amplification. Let's consider the IF amplifier as shown in Fig. 6.12. With resistive loads, it is possible to get extra bandwidth from the output of the amplifier. When we look at the gain profile of this simple amplifier, we would get a single pole at 22.9 GHz which would result in a gain of 8.8 dB assuming transistor size of 6 μm and R_D as 650 Ω.

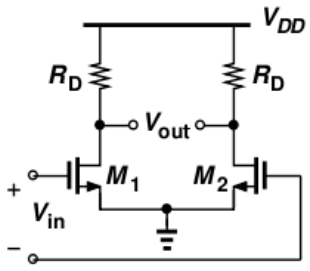


Figure 6.12: Basic differential as IF amplifier

This type of gain profile, with 10 dB/decade slope, is not highly desirable in the receiver because same type of profile is also observed at the output of the mixer. This would mean that at low frequencies, the receiver would have high gain but at 37 GHz, this gain would be reduced by 3 dB. This problem must be addressed in this amplifier such that it doesn't propagate the next stages.

Shunt peaking at the amplifier would help us to get some gain at the high frequency part and also extend the bandwidth of the amplifier. Fig. 6.13 shows the shunt peaking with inductors and the simulation results for such an amplifier. The low frequency gain of the amplifier is determined by R_D and at high frequency, the gain is determined by the inductor Q and R_D resulting in a higher gain. This amplifier yields a low frequency gain of 8.4 dB and peaked gain of 9.8 dB at 39 GHz.

This gain although good, is not high enough to suppress the noise figure of the remaining stages in the receiver chain. We can add additional amplifiers with the same configuration which would increase our gain and also power consumption. Besides, due to the stability concerns in multistage

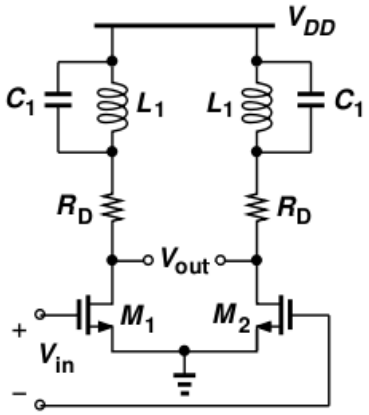


Figure 6.13: IF amplifier with shunt peaking

amplification, we would like to get an amplification more than 10 dB in single stage.

We propose this small modification to our amplifier. A small PMOS cross coupled pair added to the output of the amplifier would provide additional gain at the expanse of some power dissipation. This power dissipation wouldn't be as high as the main amplifier so that it would still remain a feasible choice.

IF amplifier is directly loading the RF mixer, which places some constraints in terms of input transistor size. In order to increase the gain and decrease the noise, we would like to increase the size of the input transistors. However, the mixer places a limit on the size of the transistor because we also need to minimize the load capacitance for the RF mixer so that gain is maximized and noise is minimized.

Final schematic with component values are also given in Fig. 6.14. 6 μm transistors are selected that would present an input capacitance of 5 fF to the RF mixer. Resulting structure has a gain of 10 dB at 27 GHz and 11.2 dB in 37 GHz. Fig. 6.15(a) and Fig. 6.15(b) shows the gain and NF of the IF amplifier and the combined system respectively. This amplifier draws 1.85 mA from the supply with cross coupled pair only drawing 0.3 mA of this total power.

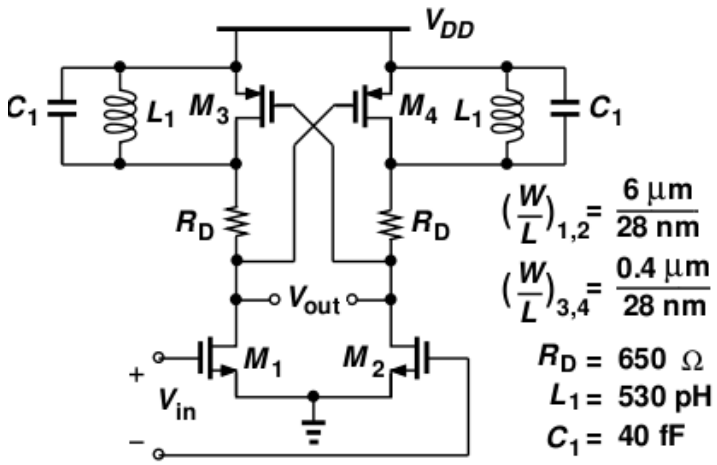
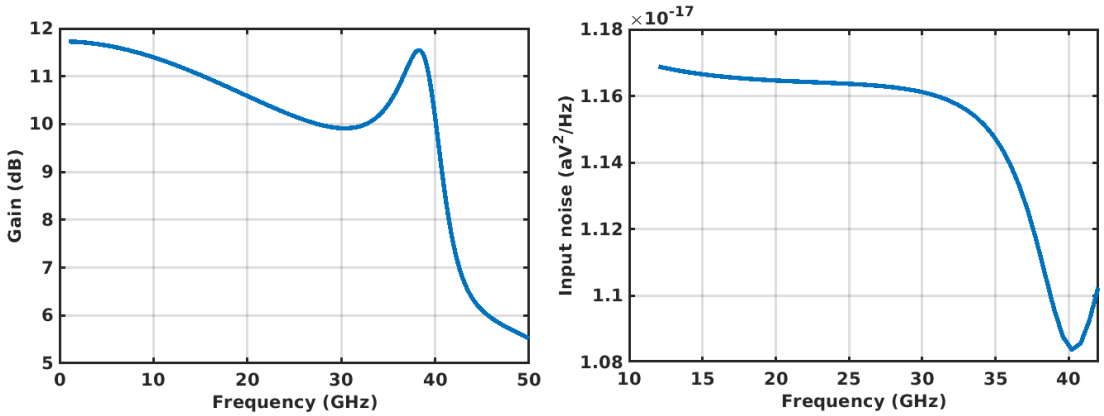


Figure 6.14: IF amplifier with shunt peaking and PMOS cross-coupled pair



(a) (b)

Figure 6.15: IF amplifier gain(a) and input referred noise (b)

6.3 Quadrature Clock Generation

The quadrature clocks are generated using the same divider that was used to divide 54-GHz into 27-GHz. The divider schematic is given in Fig. 3.21. Now the single divider unfortunately fails to provide quadrature phases from its output. Since it is composed of inverter stages, the delay between each element causes the phase shift around each stage to be larger than 90 degrees.

In order to overcome this problem, we propose to add 2 more additional dividers to 54-GHz VCO. One of the divider would get the nominal phase and the second divider would get the differential phase as illustrated in Fig. 6.16. When divided with 2 separate dividers, dividers would provide quadrature phases at their outputs.

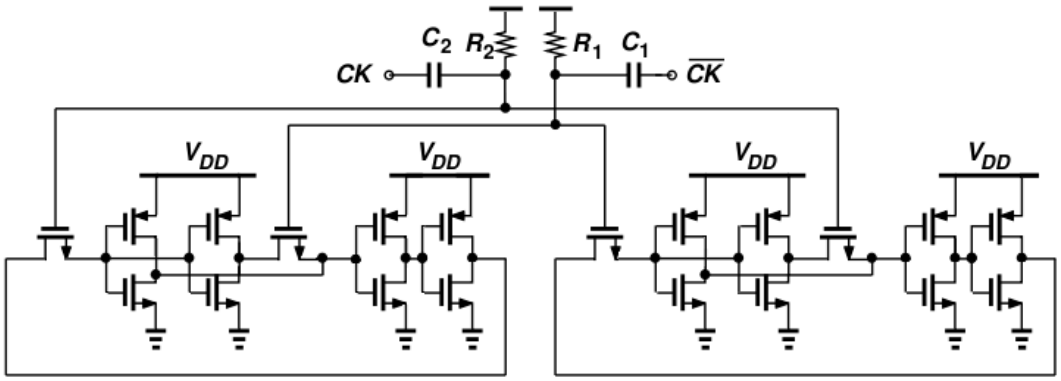


Figure 6.16: Complete divider schematic for quadrature separation

The simulation results for the divider is shown in Fig. 6.17. The results also indicate a quadrature waveform from the output with a very small phase and amplitude imbalance. At 27 GHz, the total phase mismatch is 2.3 degrees and amplitude mismatch is 2.8 dB.

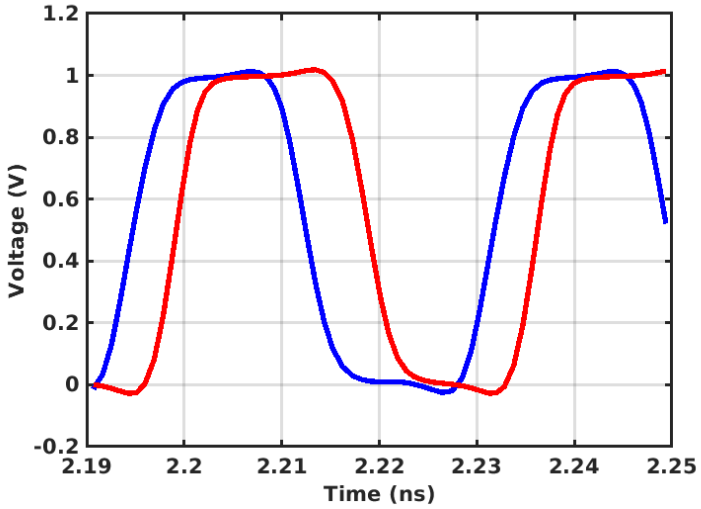


Figure 6.17: Transient waveforms for quadrature divider

6.4 IF Mixer

IF mixer is the 3rd stage in the receiver chain as in the Fig. 6.4. Its main function is to convert the IF frequency down to baseband. This mixing stage uses quadrature clocks.

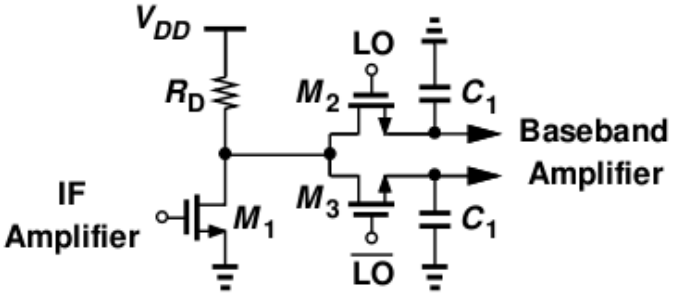


Figure 6.18: IF mixer schematic

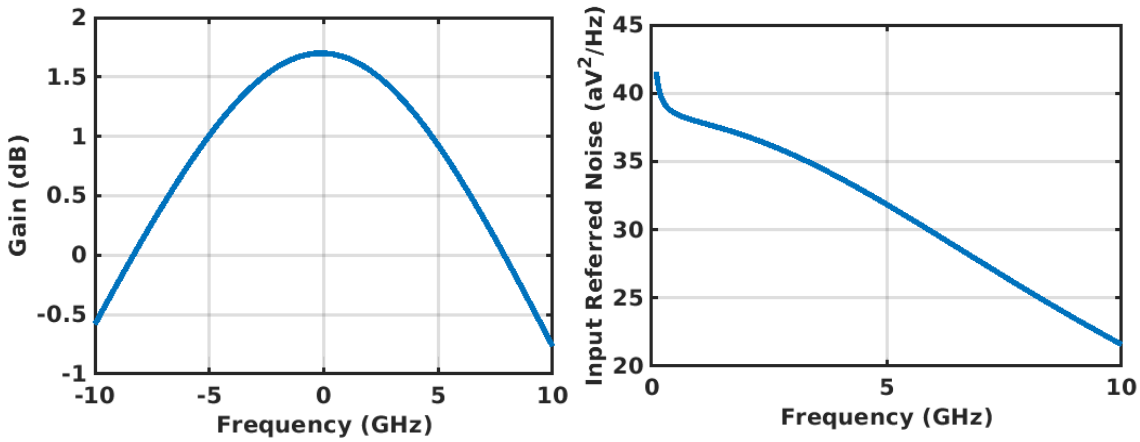
The mixer is given in Fig. 6.18. At its input, it has a common source driving stage, followed by a passive mixer loaded with capacitors. The amplification stage is required to get extra driving capability for the mixer and also reduce the load of the IF stage to main its bandwidth.

Since this mixer again has a capacitive load, similar kind of analysis in the RF mixer conversion gain calculation. However, when we have a homodyne stage, at DC we would expect a gain:

$$\frac{V_{out}}{V_{in}} = \sqrt{\frac{1}{\pi^2} + \frac{1}{4}} \tag{6.25}$$

The switch transistors are driven by the outputs from the divide-by-2 stage in Fig. 3.21. This divider provides rail-to-rail swing at 27 GHz to these transistors which is enough to switch these from on to off. The only concern for the divider is that the switch size still needs to be small so that the divider is not loaded with a high capacitance.

The amplifier and mixer combination provides a total of 1.2 dB gain and 40 aV/Hz^2 output noise at the baseband. The conversion gain for the mixer and output noise is given in Fig. 6.19 (a) and Fig. 6.19(b) respectively.



(a) (b)

Figure 6.19: IF mixer gain(a) and output noise (b)

6.5 Baseband Amplifier

The baseband amplifier has to perform 2 operations. Firstly, it should be able to amplify a wide-bandwidth signal from 0 to 10 GHz with a sufficiently high gain. Secondly, it should be able to drive 50 Ω load at its output.

Typically, these passive mixers are terminated with trans-impedance amplifiers (TIAs) for low bandwidth signals. However since we need a bandwidth of at least 10 GHz, the design constraints on a TIA would be challenging.

Instead of TIAs, we again employ differential amplifiers in Fig. 6.20 to get a voltage amplification at the output. In order to get the bandwidth, we use shunt peaking technique to enhance the bandwidth and a small cross coupled pair to boost the gain.

For driving 50 Ω transmission line, we have an open-drain NMOS devices. As these devices need to drive a 50 Ω load, they sizes should be large and uses a lot of current. In order to exclude the power consumption of these transistors, we use an open drain NMOS where their voltage is supplied with an external bias-tee.

This baseband amplifier provides a total gain given in Fig. 6.21 (a) with an additional input

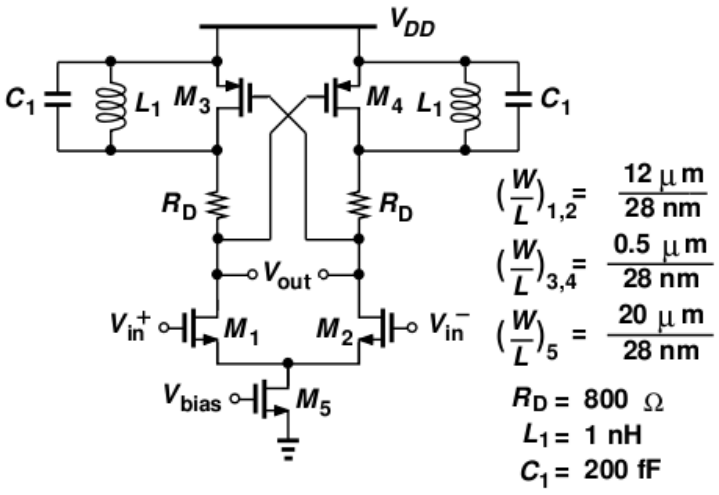
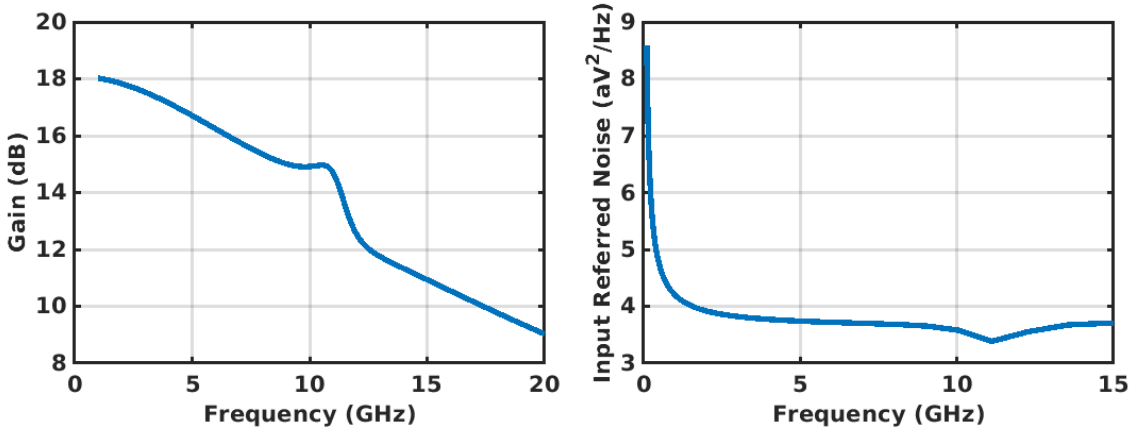


Figure 6.20: Baseband amplifier schematic

referred noise given in Fig. 6.21 (b).



(a) (b)

Figure 6.21: Baseband amplifier gain(a) and input referred noise (b)

6.6 Measurement Setup and Results

The 300-GHz receiver is designed with 28-nm bulk CMOS process and manufactured by TSMC. The active area is 200 µm x 300 µm. Fig. 6.22 shows the die micrograph.

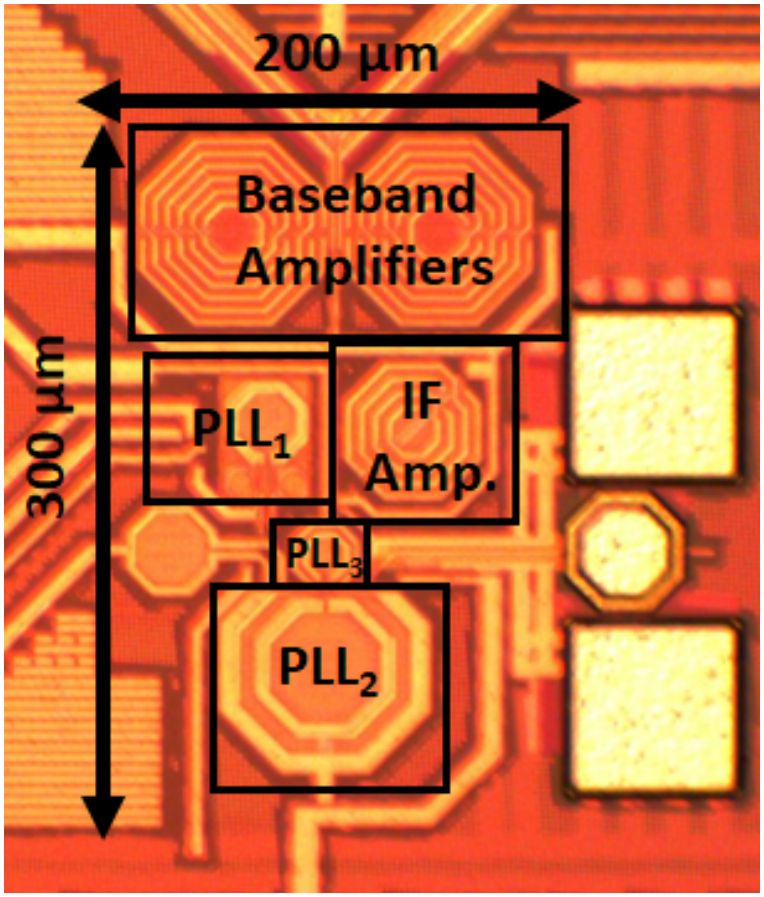


Figure 6.22: Chip photo for 300-GHz receiver

The measurement setup for this chip is more complex than the LO generator. In LO generator, we only had to measure the output frequency at 300-GHz and adjust operating points inside the chip to lock the PLLs. In this chip, we also need to measure the receiver performance with all the PLLs locked.

For locking PLLs, firstly we have to measure whether the 54-GHz PLL is locking. In this chip, we also have access to the divider output. By monitoring divider output and adjusting proper

capacitor banks, we can lock 54-GHz PLL.

Secondly, we need to lock 108-GHz PLL to 54-GHz input signal. We again do not have a direct access to the output of 108-GHz VCO. However, in the receiver scenario, we have another way to monitor this VCO output. RF input path crosses very close to the 108-GHz VCO, where some of the signal at 108-GHz VCO couples to this line. When the RF input is close to VCO frequency, these mix due to the nonlinearity of the transistors of RF mixer. Fig. 6.23 indicates the mechanism for the mixing of these signals. According to the simulations, this path would have a conversion loss of 70 dB, leading to a reasonable amount of power above the noise floor to be able to determine the frequency of oscillation and check whether the VCO is locked or not.

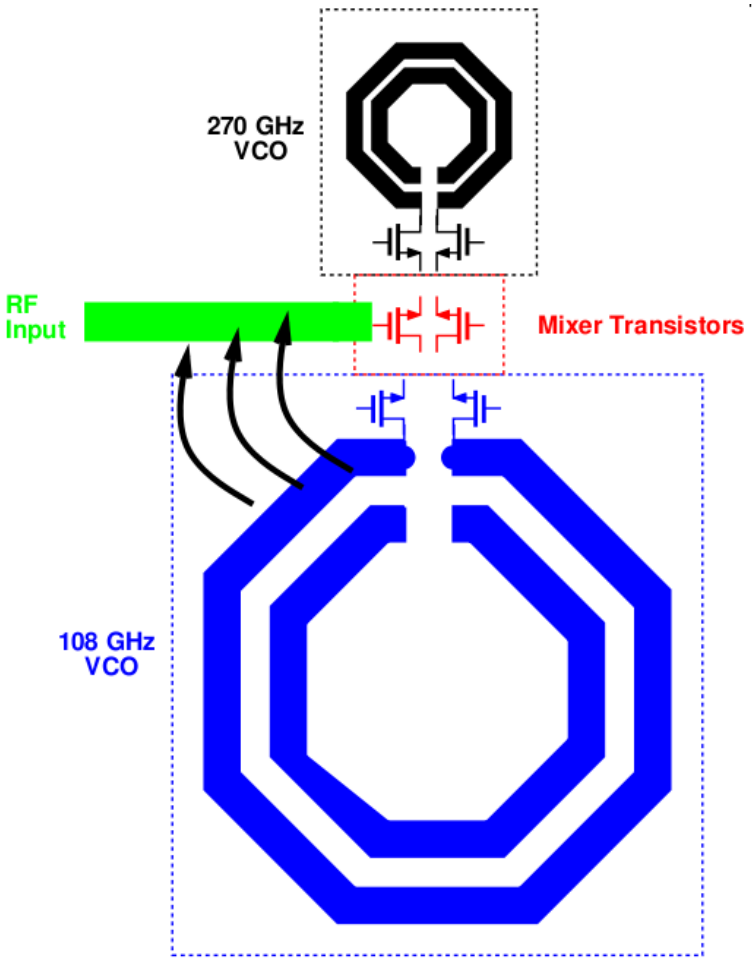


Figure 6.23: Coupling path for 108-VCO

Finally, once 108-GHz VCO is locked, we need to lock 270-GHz VCO. Since we are working on the reception of 300-GHz, We would give an input of 300-GHz and from the output of the receiver, we would get a downconverted waveform with a substantial power to determine the 270-GHz VCO frequency. Assuming high side injection, the baseband frequency can be calculated as:

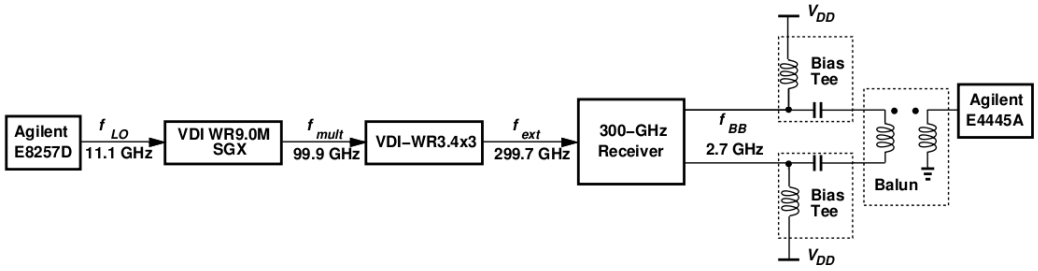
$$f_{vco} = f_{in} - f_{out} - 27 \tag{6.26}$$

After the PLLs lock, we need to measure the gain and noise figure of the system. First of all, we need to find an adequate 300-GHz source as an input for our receiver. Since we do not have commercial fundamental 300-GHz generators, we need to use some frequency multipliers which takes in reasonable frequency input like 12-18 GHz and multiplies it up to 300 GHz. Virginia Diodes VDI-WR10M-SGX module takes in a frequency between 12-18 GHz and generates output around 70-110 GHz. Even this output still stays short of 300 GHz. With the addition of another Virginia Diodes multiplier, VDI-WR3.4x3, we can triple this input to 220-330 GHz with a waveguide output. This multiplier should have an output of 6 dBm with nominal operation.

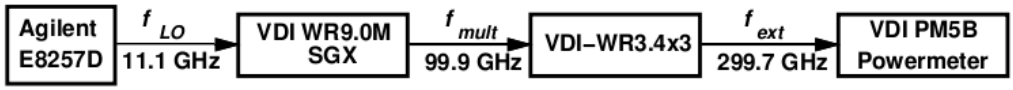
For the gain measurement, we need to perform the following measurements. Firstly, with 287 GHz to 307 GHz input, we need to measure the output power from the receiver, as in Fig. 6.24(a). Next step is to measure the power output from the signal generator. In this measurement step, we connect the output of VDI-WR3.4x3 to PM5B Erickson powermeter from Virginia Diodes, as in Fig. 6.24(b). Last step is to subtract the loss of cables and other baseband external components as in Fig. 6.24(c). The probe loss cannot be calibrated in these measurements so we are using the manufacturer data sheet to get an average loss of 2.2 dB from the probes. Total gain would be

$$Gain = P_{out} - P_{in} + P_{loss} + 2.2 \tag{6.27}$$

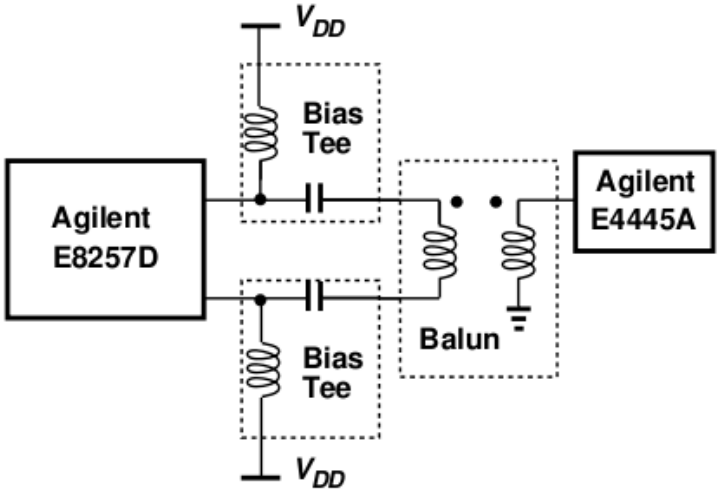
As soon as we obtain the gain, the next step is to find the noise figure of the receiver. Again at these frequencies, there are no commercial calibrated noise sources. A y-factor noise measurement



(a)



(b)



(c)

Figure 6.24: Measurement setups for gain measurement (a) and input power measurement (b) and loss calibration (c)

would be highly accurate since it is a measurement with different calibrated noise states. Unfortunately due to lack of this noise source, we have to rely on the gain method. This method calculates the noise figure according to the formula:

$$NF = P_{N,out} - (-174dBm + 10log(BW) + Gain) \tag{6.28}$$

When we have high gain and high noise figure, gain method is a viable method to measure noise figure. High gain is required such that the noise floor of the spectrum analyzer is suppressed by the receiver noise. In order to increase the gain, we add an additional external low noise amplifier to generate a gain more than 30 dB. The gain method also assumes that the input is matched to 50 Ω such that the total noise at the input is -174 dBm which is kT_0.

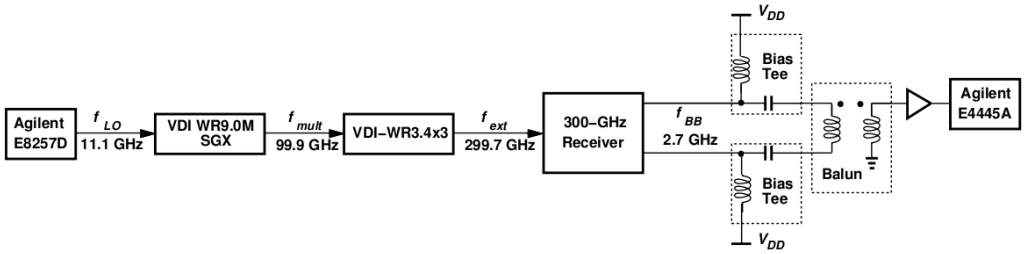
The input needs to supply -174 dBm noise to the receiver. Since this noise is coming from the 50 Ω source, we turn off the multiplier however, the receiver is still connected to the turned down source. This measurement would give us the output noise $P_{N,out}$, which is required to calculate the noise figure.

It is important to maintain a high accuracy between the measurements. Firstly, the gain of the receiver is measured using the setup in Fig. 6.25(a). Then, the noise floor is measured by turning off the signal generators in Fig. 6.25(a). By this way, the test setup remains intact between the measurements. After these two measurements are done, we need to measure the input power using powermeter in the Fig.6.24(b) and we need to characterize the gain and noise figure of the cable and additional amplifiers using the setup in Fig. 6.25(b).

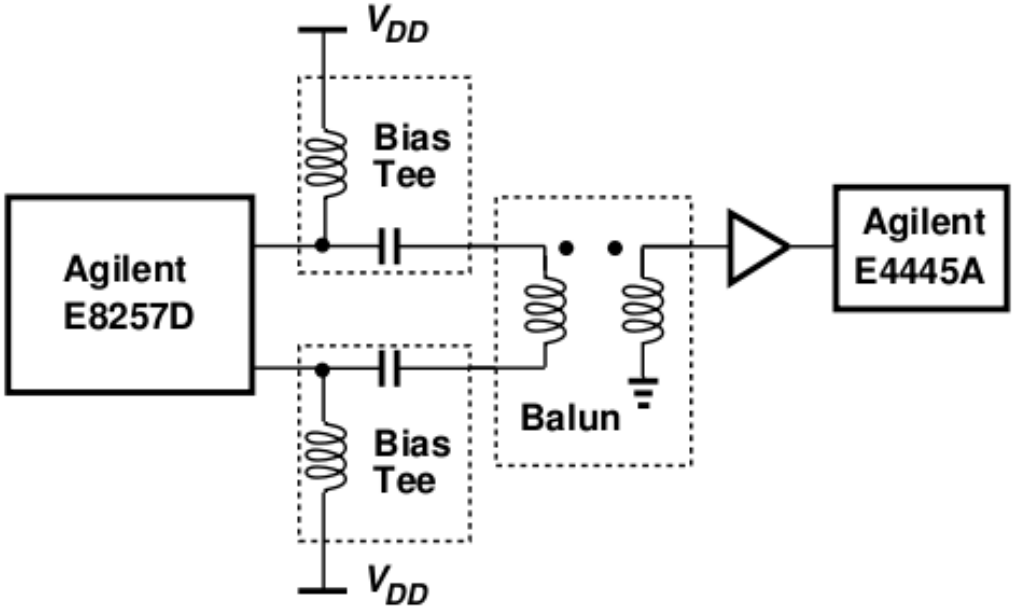
According to these measurements, the receiver Gain and Noise figure are given in Fig. 6.26 (a) and Fig. 6.26 (b) respectively. The overall gain is around 20 dB in a 16 GHz bandwidth with a overall noise figure less than 22 dB around the entire bandwidth.

At 500 MHz baseband frequency, the measured IQ mismatch is 1.2 dB and 5.4 degrees.

For compression point measurement, we just swept the input power from the source and measured the output power level. The test setup is the same in Fig. 6.24(a). and rather than using an amplifier at the output, the output of the chip connected to the spectrum analyzer to eliminate the nonlinearity associated with the additional amplifier in the chain. Next step is to sweep the source power and measure the input power using the powermeter as in Fig. 6.27.

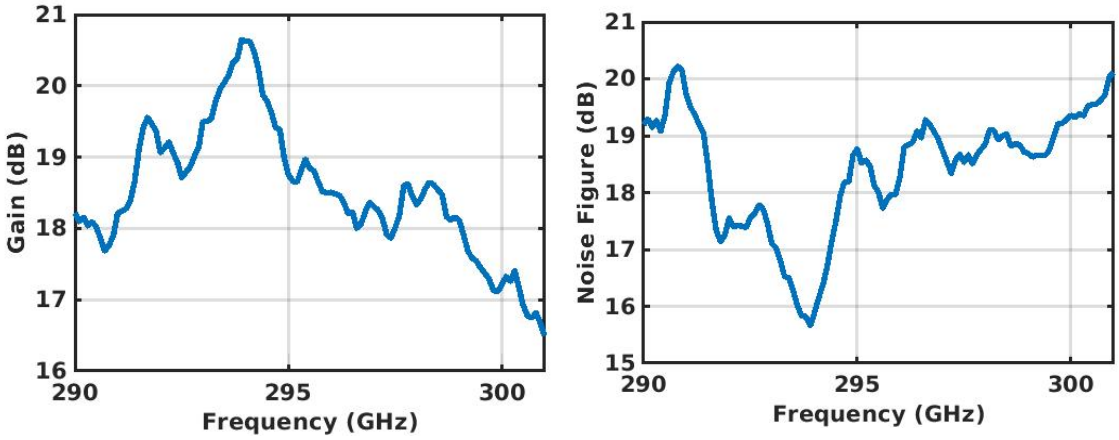


(a)



(b)

Figure 6.25: Measurement setups for noise figure measurement, gain measurement (a) and loss calibration (b)



(a) (b)

Figure 6.26: Gain (a) and noise figure (b) measurement results

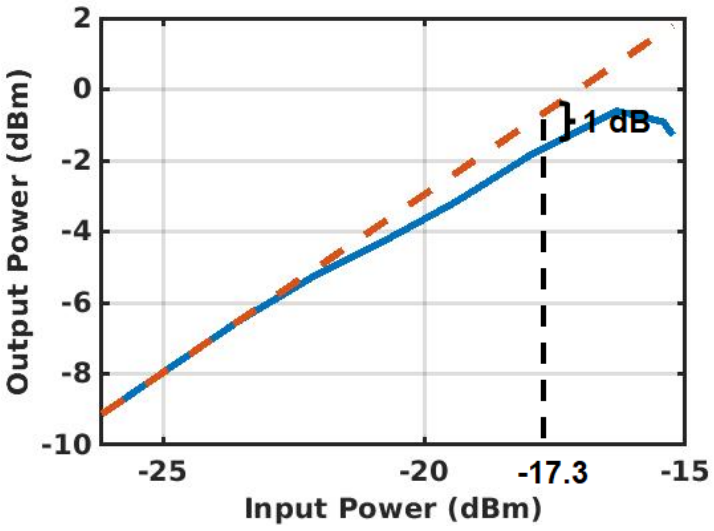


Figure 6.27: P_{1dB} measurement at 1 GHz

CHAPTER 7

Comparison with state-of-the-art and Conclusion

Table 7.1 summarizes the performance of our prototype and compares it with that of the state of the art. In comparison to [31], which requires an external 40GHz LO, the conversion gain is improved by 36dB and the power is reduced by a factor of 2.6. In comparison to the RX in [30], which uses an external 44GHz LO, the conversion gain is improved by about 15dB and the power is reduced by a factor of 17.

	This Work	JSSC'19 [1]	MTT-S'20 [2]	APMC'18 [3]	RFIT'17 [4]
f_{min} (GHz)	289	255	278	286.5	287
f_{max} (GHz)	305	275	304	313.5	320
Gain (dB)	18	3	−16.5	−19.5	−18
Noise Fig. (dB)	20	22.9	NA	27	25.5
Power (mW)	52	897*	140*	650*	416*
Chip area (mm^2)	0.72	NA	1.9	NA	2.29
Tech. (nm)	28-nm CMOS	40-nm CMOS	65-nm CMOS	40-nm CMOS	40-nm CMOS

*with external LO

Table 7.1: Comparison with other state-of-the-art 300-GHz receivers

The clock generation in the receiver allows us to drive the mixers with a very low loss and low noise figure, allowing us to downconvert 300-GHz to an IF level with high gain and low noise. The previous clock generators use power hungry multipliers and require substantially very high powered input clocks to fully drive their resistive mixers. However, with internally generated clocks, the clock swings are high enough such that they can drive a switch based mixer with very high efficiency.

With the following receiver and clock generation, we have achieved substantial gain and re-

duced noise figure at 300-GHz with a highly reduced power consumption. Furthermore, high input P_{1dB} and very low quadrature mismatch proves that the prototype is suitable for quadrature modulations like 64-QAM.

REFERENCES

[1] J.-H. Song, C. Cui, S.-K. Kim, B.-S. Kim, and S. Nam, "A Low-Phase-Noise 77-GHz FMCW Radar Transmitter With a 12.8-GHz PLL and a $\times 6$ Frequency Multiplier," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 7, pp. 540–542, 2016.

[2] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A Single-Chip Dual-Band 22–29-GHz/77–81-GHz BiCMOS Transceiver for Automotive Radars," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, 2009.

[3] J. Powell, H. Kim, and C. G. Sodini, "SiGe Receiver Front Ends for Millimeter-Wave Passive Imaging," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 11, pp. 2416–2425, 2008.

[4] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A 16-QAM 100-Gb/s 1-M Wireless Link With an EVM of 17% at 230 GHz in an SiGe Technology," *IEEE Microwave and Wireless Components Letters*, vol. 29, no. 4, pp. 297–299, 2019.

[5] H. Hamada, T. Fujimura, I. Abdo, K. Okada, H.-J. Song, H. Sugiyama, H. Matsuzaki, and H. Nosaka, "300-GHz. 100-Gb/s InP-HEMT Wireless Transceiver Using a 300-GHz Fundamental Mixer," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, pp. 1480–1483, 2018.

[6] I. Dan, G. Ducournau, S. Hisatake, P. Szriftgiser, R.-P. Braun, and I. Kallfass, "A Superheterodyne 300 GHz Wireless Link for Ultra-Fast Terahertz Communication Systems," in *2019 49th European Microwave Conference (EuMC)*, pp. 734–737, 2019.

[7] S. Hara, K. Takano, K. Katayama, R. Dong, K. Mizuno, K. Takahashi, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "300-GHz CMOS Receiver Module with WR-3.4 Waveguide Interface," in *2018 48th European Microwave Conference (EuMC)*, pp. 396–399, 2018.

[8] S. Lee, R. Dong, T. Yoshida, S. Amakawa, S. Hara, A. Kasamatsu, J. Sato, and M. Fujishima, "9.5 An 80Gb/s 300GHz-Band Single-Chip CMOS Transceiver," in *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, pp. 170–172, 2019.

[9] D. Van Der Weide, F. Keilmann, V. Agrawal, and J. Murakowski, "Gas absorption spectroscopy with electronic terahertz techniques," in *1998 IEEE Sixth International Conference on Terahertz Electronics Proceedings. THZ 98. (Cat. No.98EX171)*, pp. 117–119, 1998.

[10] P. F.-X. Neumaier, K. Schmalz, J. Borngräber, and H.-W. Hübers, "Application of multivariate analysis to gas-phase spectroscopy at 245 GHz," in *2014 39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, pp. 1–2, 2014.

[11] D. Kissinger, N. Rothbart, K. Schmalz, J. Bornzraber, and H.-W. Hübers, "Sensitive Millimeter-Wave/Terahertz Gas Spectroscopy Based on SiGe BiCMOS Technology," in *2018 43rd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, pp. 1–2, 2018.

[12] A. Tekawade, T. E. Rice, M. A. Oehlschlaeger, M. W. Mansha, K. Wu, M. M. Hella, and I. Wilke, "Towards Industrial THz Wave Electronic Gas Sensing and Spectroscopy," in *2019 44th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, pp. 1–2, 2019.

[13] N. Rothbart, K. Schmalz, J. Borngräber, D. Kissinger, and H.-W. Hübers, "Gas detection with sub-ppm sensitivity based on a 245 GHz SiGe BiCMOS transmitter and receiver," in *2017 42nd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, pp. 1–2, 2017.

[14] M. Hosseini and A. Babakhani, "A Fully Integrated 20-500-GHz Coherent Detector with 2-Hz Frequency Resolution," in *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, pp. 1–4, 2020.

[15] B. Jamali and A. Babakhani, "A Fully Integrated 50–280-GHz Frequency Comb Detector for Coherent Broadband Sensing," *IEEE Transactions on Terahertz Science and Technology*, vol. 9, no. 6, pp. 613–623, 2019.

[16] S. Razavian and A. Babakhani, "A Fully Integrated Coherent 50–500-GHz Frequency Comb Receiver for Broadband Sensing and Imaging Applications," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 231–234, 2020.

[17] S. van Berkel, E. S. Malotaux, C. De Martino, M. Spirito, D. Cavallo, A. Neto, and N. Llombart, "Wideband Double Leaky Slot Lens Antennas in CMOS Technology at Submillimeter Wavelengths," *IEEE Transactions on Terahertz Science and Technology*, vol. 10, no. 5, pp. 540–553, 2020.

[18] J. Shi, Y. Wang, D. Xu, C. Yan, L. Tang, P. Duan, Y. He, H. Liu, T. Chen, H. Feng, and J. Yao, "Biomedical diagnosis of cerebral ischemia with continuous-wave THz imaging," in *2016 41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, pp. 1–2, 2016.

[19] K. Sengupta, D. Seo, L. Yang, and A. Hajimiri, "Silicon Integrated 280 GHz Imaging Chipset With 4×4 SiGe Receiver Array and CMOS Source," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 3, pp. 427–437, 2015.

[20] R. Han, C. Jiang, A. Mostajeran, M. Emadi, H. Aghasi, H. Sherry, A. Cathelin, and E. Afshari, "25.5 A 320GHz phase-locked transmitter with 3.3mW radiated power and 22.5dBm EIRP for heterodyne THz imaging systems," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 1–3, 2015.

[21] K. Sengupta, D. Seo, and A. Hajimiri, "A terahertz imaging receiver in 0.13μm SiGe BiCMOS technology," in *2011 International Conference on Infrared, Millimeter, and Terahertz Waves*, pp. 1–2, 2011.

[22] C. Jiang, M. Aseeri, A. Cathelin, and E. Afshari, "A 301.7-to-331.8GHz source with entirely on-chip feedback loop for frequency stabilization in 0.μm BiCMOS," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pp. 372–374, 2018.

[23] R. Han, C. Jiang, A. Mostajeran, M. Emadi, H. Aghasi, H. Sherry, A. Cathelin, and E. Afshari, "A SiGe Terahertz Heterodyne Imaging Transmitter With 3.3 mW Radiated Power and Fully-Integrated Phase-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2935–2947, 2015.

[24] X. Liu and H. C. Luong, "Fully Integrated 0.27-THz Injection-Locked Frequency Synthesizer With Frequency-Tracking Loop in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1051–1063, 2020.

[25] M. Seo, M. Urteaga, M. Rodwell, and M.-J. Choe, "A 300 GHz PLL in an InP HBT technology," in *2011 IEEE MTT-S International Microwave Symposium*, pp. 1–4, 2011.

[26] M. Seo, M. Urteaga, A. Young, J. Hacker, A. Skalare, R. Lin, and M. Rodwell, "A single-chip 630 GHz transmitter with 210 GHz sub-harmonic PLL local oscillator in 130 nm InP HBT," in *2012 IEEE/MTT-S International Microwave Symposium Digest*, pp. 1–3, 2012.

[27] M. Seo, A. Young, M. Urteaga, Z. Griffith, M. Rodwell, M.-J. Choe, and M. Field, "A 220-225.9 GHz InP HBT Single-Chip PLL," in *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1–4, 2011.

[28] "IEEE Standard for High Data Rate Wireless Multi-Media Networks–Amendment 2: 100 Gb/s Wireless Switched Point-to-Point Physical Layer," *IEEE Std 802.15.3d-2017 (Amendment to IEEE Std 802.15.3-2016 as amended by IEEE Std 802.15.3e-2017)*, pp. 1–55, 2017.

[29] P. Rodríguez-Vázquez, J. Grzyb, B. Heineman, and U. R. Pfeiffer, "Optimization and Performance Limits of a 64-QAM Wireless Communication Link at 220-260 GHz in a SiGe HBT Technology," in *2019 IEEE Radio and Wireless Symposium (RWS)*, pp. 1–3, 2019.

[30] S. Lee, S. Hara, T. Yoshida, S. Amakawa, R. Dong, A. Kasamatsu, J. Sato, and M. Fujishima, "An 80-Gb/s 300-GHz-Band Single-Chip CMOS Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, 2019.

[31] I. Abdo, T. Fujimura, T. Miura, K. K. Tokgoz, H. Hamada, H. Nosaka, A. Shirane, and K. Okada, "A 300GHz Wireless Transceiver in 65nm CMOS for IEEE802.15.3d Using Push-Push Subharmonic Mixer," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, pp. 623–626, 2020.

[32] S. Hara, K. Takano, K. Katayama, R. Dong, S. Lee, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "300-GHz CMOS Transceiver for Terahertz Wireless Communication," in *2018 Asia-Pacific Microwave Conference (APMC)*, pp. 429–431, 2018.

[33] S. Hara, K. Katayama, K. Takano, R. Dong, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "A 416-mW 32-Gbit/s 300-GHz CMOS receiver," in *2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pp. 65–67, 2017.

[34] K. Takano, S. Amakawa, K. Katayama, S. Hara, R. Dong, A. Kasamatsu, I. Hosako, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "17.9 A 105Gb/s 300GHz CMOS transmitter," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 308–309, 2017.

[35] M. Elkhouly, Y. Mao, S. Glisic, C. Meliani, F. Ellinger, and J. C. Scheytt, "A 240 GHz direct conversion IQ receiver in 0.13 μm SiGe BiCMOS technology," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 305–308, 2013.

[36] S. Lee, S. Hara, R. Dong, K. Takano, S. Amakawa, T. Yoshida, and M. Fujishima, "A 272-GHz CMOS Analog BPSK/QPSK Demodulator for IEEE 802.15.3d," in *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, pp. 415–418, 2021.

[37] S. Moghadami, F. Hajilou, P. Agrawal, and S. Ardalan, "A 210 GHz Fully-Integrated OOK Transceiver for Short-Range Wireless Chip-to-Chip Communication in 40 nm CMOS Technology," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 5, pp. 737–741, 2015.

[38] A. Standaert and P. Reynaert, "A 410 GHz OOK Transmitter in 28 nm CMOS for Short Distance Chip-to-Chip Communications," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 240–243, 2018.

[39] Z. Wang, P.-Y. Chiang, P. Nazari, C.-C. Wang, Z. Chen, and P. Heydari, "A 210GHz fully integrated differential transceiver with fundamental-frequency VCO in 32nm SOI CMOS," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 136–137, 2013.

[40] Y. Zhao, Z.-Z. Chen, Y. Du, Y. Li, R. Al Hadi, G. Virbila, Y. Xu, Y. Kim, A. Tang, T. J. Reck, and M.-C. F. Chang, "A 0.56 THz Phase-Locked Frequency Synthesizer in 65 nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 3005–3019, 2016.

[41] P.-Y. Chiang, Z. Wang, O. Momeni, and P. Heydari, "14.7 A 300GHz frequency synthesizer with 7.9% locking range in 90nm SiGe BiCMOS," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 260–261, 2014.

[42] Z. Ahmad and O. Kenneth, "0.4-THz wideband imaging transmitter in 65-nm CMOS," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pp. 99–102, 2017.

[43] N. Sarmah, P. R. Vazquez, J. Grzyb, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A wideband fully integrated SiGe chipset for high data rate communication at 240 GHz," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 181–184, 2016.

[44] B. Khamaisi, S. Jameson, and E. Socher, "A 0.58–0.61THz single on-chip antenna transceiver based on active X30 LO chain on 65nm CMOS," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 97–100, 2016.

[45] B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 894–903, 2011.

[46] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-/spl mu/m CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, 2000.

[47] H. Sherry, R. Al Hadi, J. Grzyb, E. Öjefors, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "Lens-integrated THz imaging arrays in 65nm CMOS technologies," in *2011 IEEE Radio Frequency Integrated Circuits Symposium*, pp. 1–4, 2011.

[48] H. Jalili and O. Momeni, "23.2 A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 64, pp. 326–328, 2021.

[49] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77GHz 4-Element Phased Array Receiver with On-Chip Dipole Antennas in Silicon," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, pp. 629–638, 2006.