UNIVERSITY OF CALIFORNIA

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Process Development of Power Delivery Through Wafer Vias for Silicon Interconnect Fabric

A thesis submitted in partial satisfaction

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in Materials Science and Engineering

by

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ABSTRACT OF THE THESIS

Process Development
of Power Delivery Through Wafer Vias
for Silicon Interconnect Fabric

by

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Master of Science in Materials Science and Engineering
University of California, Los Angeles, 2019
Professor Subramanian Srikantes Iyer, Chair

At UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), we have been developing a fine pitch heterogeneous wafer-scale platform with a single level of hierarchy called the silicon interconnect fabric (Si-IF). The Si-IF is a platform for heterogeneous integration of different bare dies at fine pitch (2 to 10 µm) and close proximity (<100 µm die spacing). The Si-IF platform can accommodate an entire 50 kW data center on a single 300 mm diameter wafer. Power delivery and heat extraction are fundamental challenges. To minimize the overhead of power conversion, current at mission voltage is planned to be delivered directly to the assembly; this requires a uniform delivery of tens of kA. Our approach is to deliver the current from the back of the Si-IF, using cooled Cu fins and through wafer vias (TWVs), to the front side of the wafer, where the

dies are assembled facedown. TWVs are a key component of this power delivery system and are required to penetrate through the entire thickness of the Si-IF (500 – 700 µm). A process for fabrication of large-sized (100 µm diameter) TWVs for the Si-IF is described in this paper. The TWVs are etched in 500 µm Si wafer (aspect ratio of 1:5) and are designed to enable back-side power delivery to the integrated system. Each TWV exhibits a resistance of 1.1 mΩ with an extracted resistivity of 1.73·10-8 Ω·m. The scale and performance of these large-sized TWVs supports high current density for power delivery applications.

The thesis of Meng-Hsiang Liu is approved.

Dwight C. Streit

Jenn-Ming Yang

Subramanian Srikantes Iyer, Committee Chair

University of California, Los Angeles

2019

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Last but not least, I would like to thank my mother as well as all my family members for their constant support and help.

CHAPTER 1

Introduction

1.1 Silicon Interconnect Fabric (Si-IF) Technology

Reducing communication power and latency, drives the need for both, high performance devices and improved integration (*i.e.*, high interconnect density and fine spaced die assembly) [1]. Conventional packaging and integration technologies, however, are based on solder attachment of chips to printed circuit boards (PCBs). In this approach, the large interconnect pitch on the PCB, typically 0.4 to 1 mm, significantly limits the data bandwidth [1-3].

We have developed the silicon interconnect fabric (Si-IF), a heterogeneous integration wafer-scale platform with a single level of hierarchy. The Si-IF supports fine pitch and solder-less metal-metal integration. In the Si-IF technology, bare dies are attached to the Si wafer [2] using thermal compression bonding (TCB) [1]. The Si-IF supports heterogeneous integration of bare dies at fine pitch (2 to 10 μm) and high proximity (<100 μm spacing), as compared to the large pitch and spacing on PCBs [1,3], leading to reduces communication energy and latency [4]. The Si-IF platform is expected to accommodate an

entire 50 kW data center on a single 300 mm diameter wafer. Heat dissipation and power delivery are, therefore, key challenges of the Si-IF approach. Our approach is to deliver the current from the back side of the Si-IF using cooled copper (Cu) fins and through-wafer vias (TWVs) to the front side of the wafer, where the dies are assembled facedown. To ensure high quality of power delivered to the front side of the Si-IF, a process for TWVs within a full thickness Si wafer (500 µm) is developed. A schematic of the Si-IF construct including TWVs is shown in Figure 1.

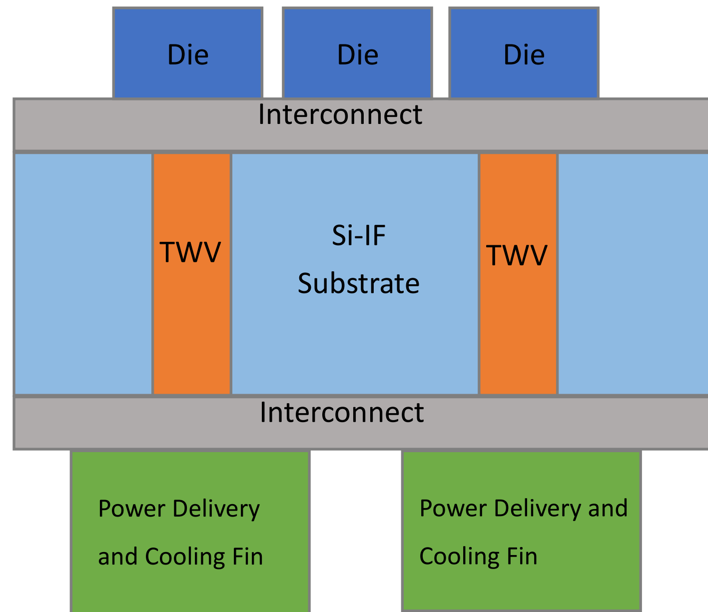


Figure 1. Schematic of TWVs supporting back-side power delivery within the Si-IF [9]. Power is delivered to the back side of the Si-IF using large Cu fins that double as thermal conduits to remove heat away from the Si wafer.

1.2 Three-Dimensional Integration and Through Silicon Via (TSV)

The development of through-silicon vias (TSVs) originated from the evolution of three-dimensional (3D) integration, which shows the potential to ensure the cost-efficient scaling of the next generation electronic devices [5-7]. In the 3D integration scheme, two or more layers of active electronic components are integrated vertically using TSVs enabling reduced delay and increased bandwidth [6]. Since thermal management of 3D integrated systems can limit the application space, TSVs also double as thermal conduits for heat extraction. Nowadays, TSV-based 3D integration techniques have been widely-accepted to improve system performance and reduced form factor [8].

As TWVs are used for full-thickness wafers, they are much deeper as compared to TSVs fabricated in thinned silicon substrates. TWV holes can be formed using several methods, including laser etch, wet etch, and dry etch. Deep reactive-ion etching (DRIE) is distinguished from other etching or ablation techniques [10], since this anisotropic etch provides the least pattern alignment mismatch and deformation, the highest aspect ratio, and, comparatively, a better sidewall profile of TWVs. In addition, different profiles of sidewalls within the substrate can be achieved by adjusting the amount of etchant gases, such as vertical or tapered sidewalls [11]. Cu is chosen as the fill material of the TWV due

to higher conductivity in the target dimension (~100 μm), higher melting point, and superior electromigration resilience as compared to aluminum. The preferable characteristics of Cu led to a wide adoption of Cu electroplating by the industry, as a method to fill up large via holes (>50 μm).

Cu electroplating setups require a Cu anode, and the target wafer coated with a Cu seed layer to serve as the cathode. Both anode and cathode are immersed in a solution containing Cu cation (Cu^{2+}), originating from a Cu sulfate ($CuSO_4$) electrolyte solution, to form a closed circuit [12]. We then apply a direct current to the system reducing the Cu^{2+} in the solution to Cu that is plated unto the target wafer, meanwhile, Cu atoms on the anode are oxidized and become Cu^{2+} that dissolve into the solution to maintain electrical neutral.

In the following sections (Chapter 3), we present the entire TWV process flow, recipe development, and scanning electron microscope (SEM) images of the fabricated TWVs. We also discuss the results of the electrical characterization, annealing and temperature cycling tests (Chapter 4). Moreover, we will show the measured capacitance, inductance, and IR-drop of the TWVs. (Chapter 5)

1.3 Contribution of the Work

The primary objectives of the work are to develop and optimize TWVs, a technological enabler for Si-IF, along with physical and electrical characterization. The contributions of the work are as follows.

(1) Develop and optimize the Si etch (Bosch etch) recipe for TWV etching profile on 500 μm thick Si wafer.

(2) Setting up a lab owned high performance Cu electroplating system.

(3) Develop and optimize Cu electroplating profile and quality for TWV on 500 μm thick Si wafer.

(4) Top view and cross section sample preparation, with optical microscope and scanning electron microscope (SEM) images taken.

(5) Electrical characterization of several properties of TWV are measured and extracted, including resistance, self-inductance, capacitance and IR-drop.

(6) Reliability examinations of TWVs are demonstrated, including current stressing test and temperature cycling test.

1.4 Organization of the Thesis

The organization of the thesis is as follows. In Chapter 2, the setup, operation and maintenance of lab-owned Cu electroplating system are introduced. Chapter 3 presents the process flow of full scale (500 μm thick Si wafer) TWV fabrication in UCLA NRF and ISNC. Chapter 4 presents cross section and top view figures of TWV before and after process optimization. Chapter 5 demonstrates the electrical characterization of TWVs and simple integration with an LED. The conclusions are drawn in Chapter 6.

CHAPTER 2

The Setup and Operation of Lab-Owned Copper Electroplating System

2.1 Overview and Setting Up of Cu Electroplating System

The lab-owned electroplating system, shown in Figure 2, is a portable tabletop wafer plating module measures 16 inch long, 12 inch wide, 14 inch deep constructed from 0.5 inch thick natural polypropylene with flange. The unit has one (1) anode rod as required for single side plating and one (1) cathode rod of 1/4 x 1 inch stainless steel with holders.

The module features cathode rod knife-edge agitation, complete with variable speed motor, 0-16 RPM, motor mount, cam and connecting arm. The main purpose of the agitation is securing uniformity of Cu deposition on the wafer during electroplating. The tank is heated by a 1000 watts L-type derated heater (10 watts/sq. in.) with integral thermal overload protection, digital readout temperature control (in variation of 0.25%) and a low solution level shut-off. The module also features a filter system for continuous filtration and separate agitation pump assembly, complete with natural polypropylene dispersion line with valve. Agitation pump along with The plating tank, filter pump, agitation pump,

etc. is mounted on a common polypropylene base with integral safety tray approximately 30 inch x 36 inch.

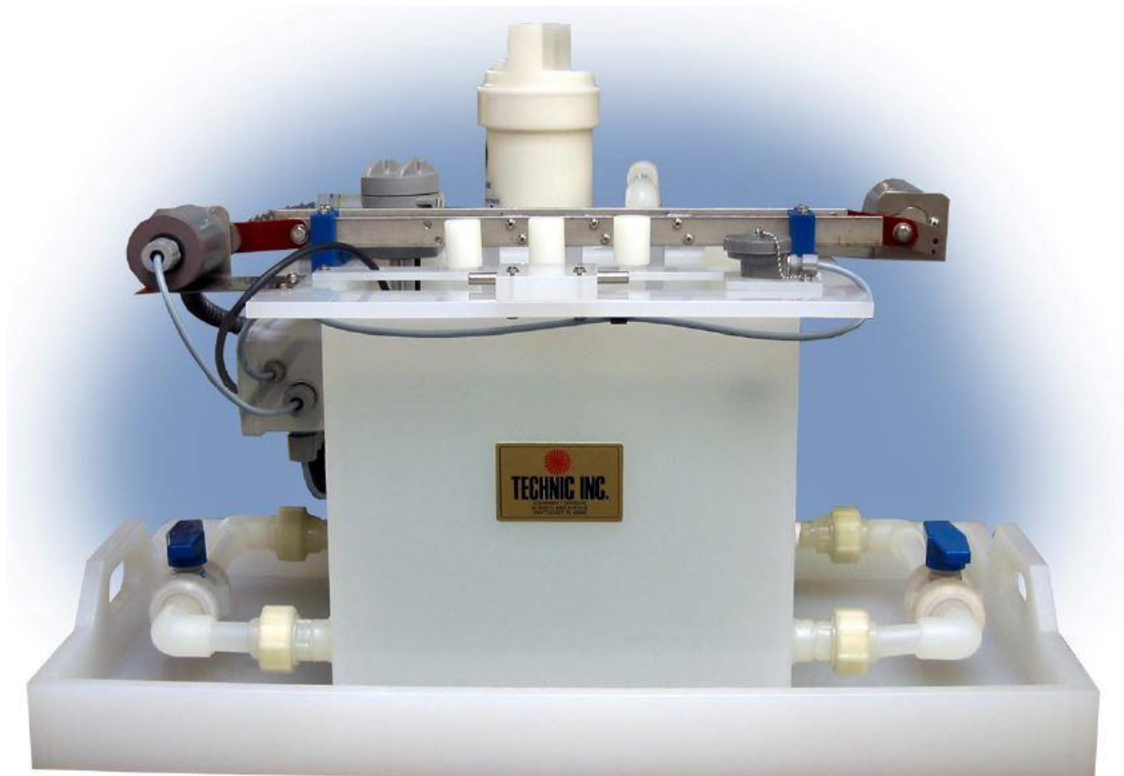


Figure 2. The setup of lab-owned Cu electroplating system

The heater, pumps and agitation system are pre-wired to a chemical resistant NEMA 4X fiberglass enclosure with the necessary fuses and circuit breakers. The temperature control and necessary switches for the pumps and agitation system are mounted in a separate fiberglass enclosure. The rectifier (provided separately) plugs into the enclosure. Input voltage 110 V/1ph/60Hz.

Chemicals for this setup provide damascene (and dual-damascene) electroplating [13]. Aside from $CuSO_4$ electrolyte, we utilize brightener and carrier as additives. Brighteners, typically organic-sulfates such as 3-mercapto-1-propanesulfonate (MPS) or bis(3-sulfopropyl) disulfide (SPS) [19], enable a uniform current density at the interface of CuSO4 electrolyte and the sidewall of via. Whereas carriers, such as polyethylene glycol (PEG) or Polyalkylene Glycol (PAG), create and maintain a defined diffusion layer at the Cu anode to control (slow down) the electroplating rate.

To set up the system, first, we must clean the sink. Leaching and cleaning are the very first step. We use a 3% potassium hydroxide (KOH) solution for leaching, this process takes away all dusts and organics, then another 3% sulfuric acid to clean up the remaining KOH and create acid environment for electroplating. The following steps are the detail of tank cleaning for chemical makeup:

(1) Drain and rinse tank and all plumbing with tap water.

(2) Fill the tank approximately two-thirds full with tap water. Dissolve 2-4 oz per gallon of tank volume (570g for entire tank) of KOH.

(3) Fill to tank volume with tap water and stir well.

(4) Allow the solution to leach the tank for a minimum of 24 hours with pumping.

(5) Drain the leach solution and rinse the tank, including plumbing and pumps with tap water.

(6) Fill the tank to approximately two-thirds full with tap water.

(7) Slowly add, with stirring, enough Sulfuric Acid to make a 3% by volume solution.

(8) Fill to tank volume with water and stir well.

(9) Allow the solution to leach the tank for a minimum of 24 hours. Be sure to activate the pumps to circulate the solution through the system.

(10) Drain the solution and rinse the tank and plumbing system 2-3 times with water. Final rinse with deionized water. Be sure to run the pumping system. Check the pH of the rinse water. The pH should be 5.5-7.5. If the pH is below 5.5, rinse the system again with deionized water.

After KOH leaching and sulfuric acid cleaning, we pour 28 liters of CuSO4 electrolyte into the tank. We then add brightener and carrier in a 1000:7:7 ratio of volume comparing with electrolyte, and switch on solution sparger for an hour to stir well the solution to reach uniform concentration of all chemicals. Finally, the electroplating system is ready for operation with a 4 μm/hr electroplating rate under 250 mA of current.

2.2 Operation Manual of Electroplating System

The entire Cu electroplating system contains:

(1) Cu electroplating tank, control panel and accessories.

(2) High current power supply, replenisher and pipettes

(3) Deionized (DI) water filter

Part (1) and (2) are stored inside a fume hood for chemical protection. Part (3) are installed beside the sink for tap water source. The figures of entire system are presented in Figure 3, 4 and 5.

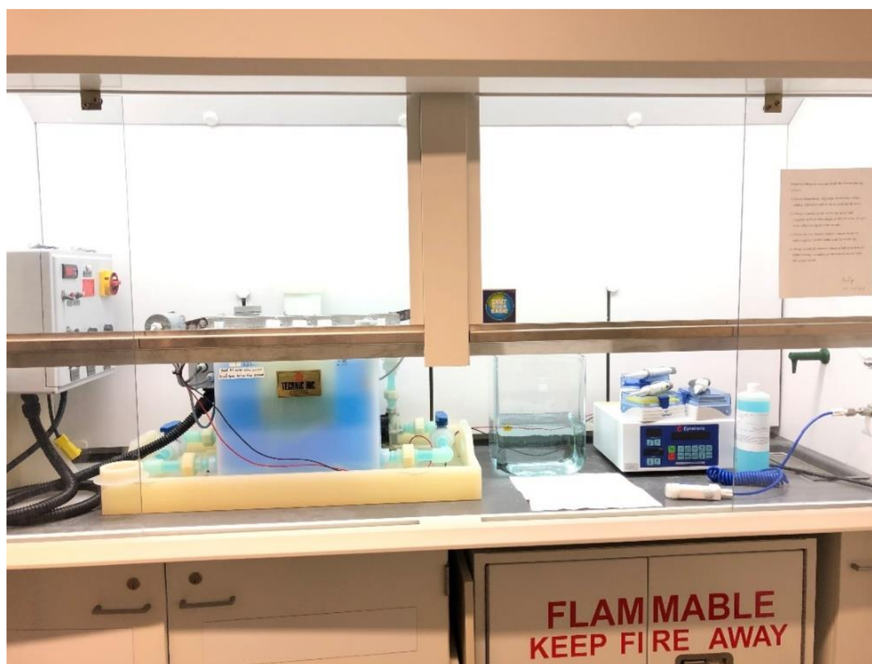


Figure 3. The overview of Cu plating system (except DI water filter). Including (from left to right) control panel, electroplating tank, DI rinsing tank, power supply, pipettes, nitrogen gun and replenisher.

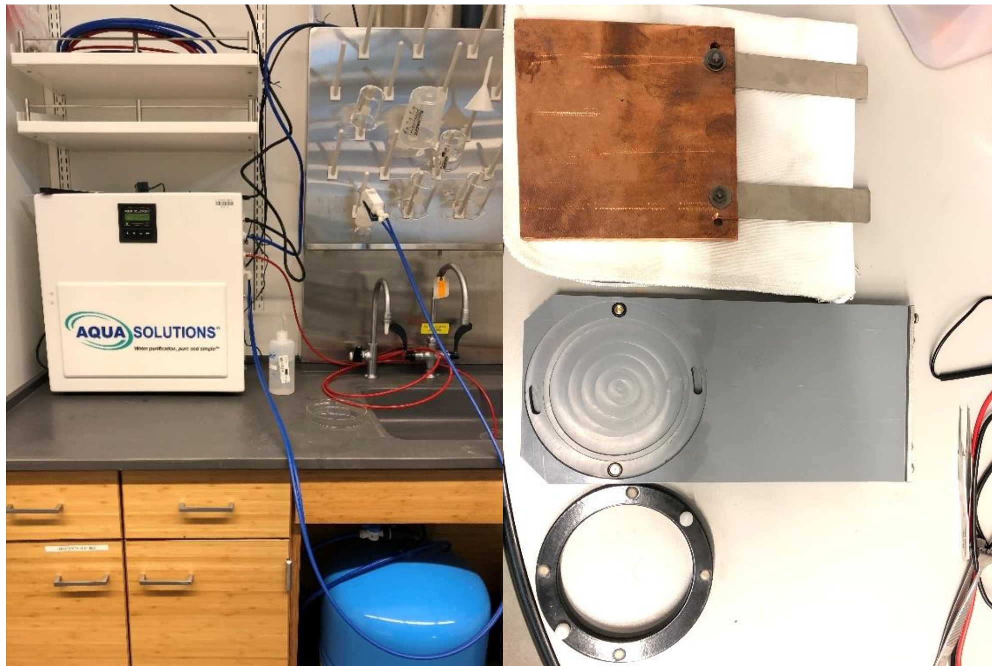


Figure 4. (left) DI water filter system, water tank and sink.

Figure 5. (right) Accessories for Cu electroplating. (top to bottom) Cu anode, a 4-inch wafer jig and magnetic wafer holder.

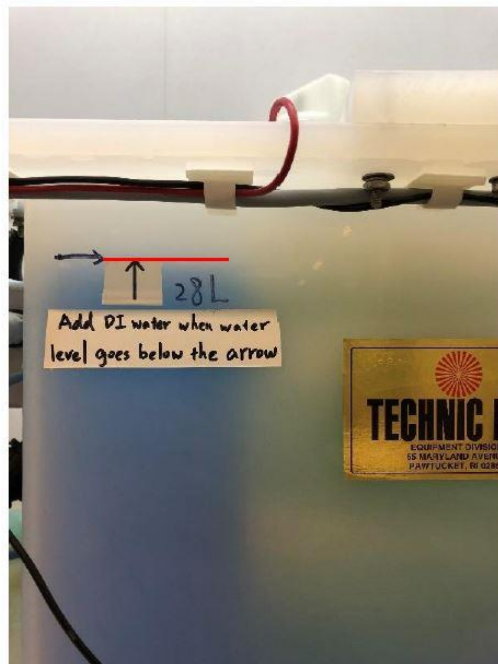


Figure 6. The water level of Cu electroplating tank should be higher than the red line to sustain the correct chemical concentration.

The detailed operating flow are as follows:

(1) Make reservation from CHIPS google calendar “electroplating”, there’s no time limitation for tool usage. Write the date and user’s name on CHIPS log sheet upon using.

(2) Check the water level of electrolyte. If it goes below the arrow (red line), see Figure 6, add DI water into the wank until it reaches the tip of arrow to keep the concentration of electrolyte.

(3) Switch on the red main power switch of plating station controlling panel. Figure 6 provides detail description of the control panel.

(4) Turn on the main power, located at top-left on back side of power (current) supply. (Figure 7)

(5) Press “ENTER” on the supply once to set the current you want. There is a formula to help user set up desired plating current: Plating current / 0.6 = Forward current to set. (leave rev. current zero)

(6) Use the arrows under the current display to set the current. (See Figure 7)

(7) Place your sample on the gray wafer jig, put on the black magnetic holder to fix your wafer.

(8) Check the conduction from your sample to the top of wafer jig. (See Figure 8)

(9) Hang the wafer jig on the metal bar of plating station.

(10) Write down all information user should provide on CHIPS log sheet.

(11) Switch up “solution agitation” and then press “OPR” (green) button on power supply to start plating.

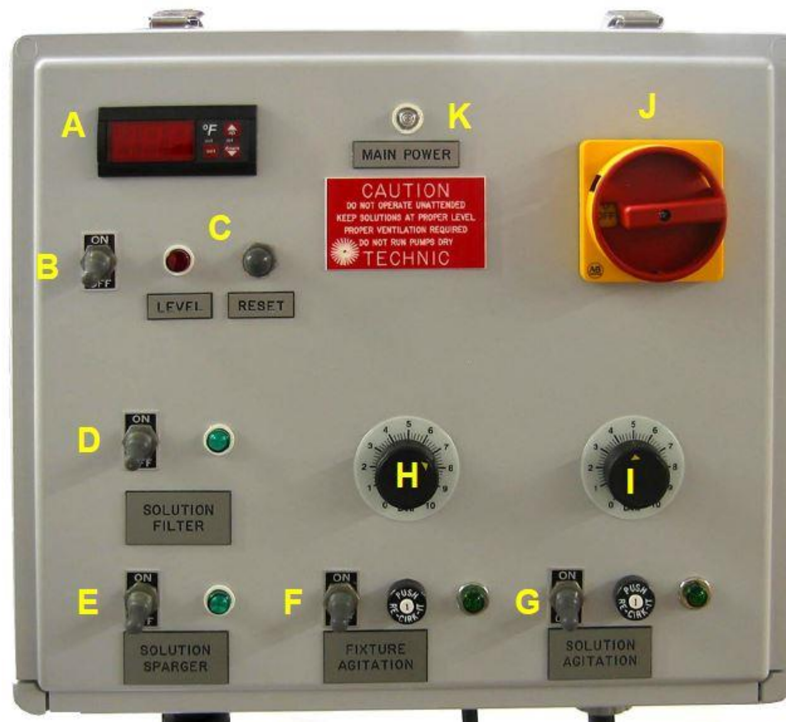


Figure 7. Control Panel of Technic Cu electroplating. (A) Digital Temperature Control (B) Temperature Control (ON, OFF) (C) Low Level Indicator Light & Reset (D) Solution Filter Pump (ON,OFF) & Indicator Light (E) Solution Sparger Pump (ON, OFF) & Indicator Light (F) Fixture Agitation (ON, OFF) Circuit Breaker & Indicator Light (G) Solution Agitation (ON, OFF) Circuit Breaker & Indicator Light (H) Fixture Agitation Motor Speed Control (I) Solution Agitation Motor Speed Control (J) Main Disconnect (Main power) 120V/20A/1Ph/60Hz (K) Main Power Indicator Light.

(12) Write down the voltage, current and time on the log sheet.

(13) Before stopping Cu plating, switch on the valve of nitrogen cylinder in gas cylinder room if you need nitrogen (important for Si-IF daisy chain process).

(14) Press “STBY” (red) button on power supply to stop plating, and then switch off “solution agitation”.

(15) Write down the end time, voltage and current on log sheet.

(16) Take out the wafer jig and immerse your sample into DI water tank for 20 sec.

(17) Take wafer jig to water sink and rinse it with DI water in water tank to remove corrosive electrolyte. For Si-IF process, rinse the wafer for at least 1 min.

(18) Move the wafer holder out from hood to sink with beaker or tray holding under it, since remaining electrolytes can erode the marble floor around hood (Figure 8).

(19) Release sample from wafer jig and dry it with nitrogen or compressed air to prevent further oxidation.

(20) Turn off the main power of power (current) supply and switch off the main power of plating station controlling panel.

(21) Add replenisher to plating station using the right pipette and tips. The formula $\mathbf{0.08 \times _mA \times _hr = _\mu l}$ on the log sheet can help calculate the amount of

replenisher to add. Then discard the tip after adding replenisher.

(22) Rinse with DI and clean up the wafer jig. Especially the magnetic wafer holder. Use the scrub and acetone (or tweezer) to remove all Cu that plated on the magnetic holder. Poor cleanliness condition results poor plating uniformity in the future.

(23) Switch the nitrogen main valve to closed to prevent gas leakage.

Figure 8. Desirable methods to transfer wafer jig from fume hood to sink after electroplating. Either using a glass beaker (left) or a plastic tray (right).

2.3 Electroplating Recipes Design for Different Projects in CHIPS

In CHIPS, multiple projects are highly relying on this lab-owned Cu electroplating system. We have designed and customized different recipes for individual process. For high aspect ratio TWVs, the ideal electroplating current ranges from 50-70 mA, and we will further discuss this process in Chapter 3. For all projects related to Si-IF, including Daisy Chain and Universal Digital Signal Processor (UDSP), are using 250 mA high current electroplating due to large plating area and lower aspect ratio. 350 mA recipe is also testified for Si-IF projects testing wafers with a 6 μm/hr electroplating rate. Besides, the plating thickness for Si-IF samples should be less than 6 μm considering the process time of CMP. Finally, for FlexTrate projects, a range of 70-100 mA is desirable because of their complex substrate surfaces or pattern design. Table 1 presents the desirable electroplating current, time and thickness for various projects.

Table 1. Electroplating recipes for projects in CHIPS

Project	Current	Plating Time	Cu thickness	Reason
TWV	50-70 mA	27 hr	500 μm	High aspect ratio
Si-IF	250 mA	1-1.5 hr	3.5-6 μm	Large plating surface
FlexTrate	70-100 mA	0.5-1.5 hr	Depends on design	Substrate

2.4 Management of Electroplating System and Chemicals in Wet Bench

Lab-owned Cu electroplating system requires weekly, annual maintenance along with chemical storage and managements. The necessity of annual maintenance is because the system is located inside a fume hood. Fume hood protects hazardous vapors from electroplating solution, mostly water. For weekly maintenance, we should add DI water into the tank to keep the water level at certain level (discussed in Chapter 2.2). Since the fume hood also evaporates little amount of electrolyte and additive day by day, to keep the tool in high electroplating quality, annual maintenance is suggested. We pump out all electrolyte (~30 liters) to empty waste bottles, and rinse (with agitation and filter pumps on) the tank with DI water twice for 1 hour each. Then follow step (7) to (10) in leaching process (Chapter 2.2) to complete annual maintenance, the entire process takes about 5 days.

Annual maintenance creates dozens of acidic chemical waste bottles. Formic acid, copper etchant and organic solvents with less hazard are also frequently used in CHIPS, therefore the storage and management are crucial for users' safety. Figure 9 shows all acids are stored in plastic storage cabinet, while organic (flammable) solvents are stored in metal cabinet. During operation of acidic chemicals, personal protection equipment (PPE) are

required (see Figure 10). Users can only pour sulfuric acid to beakers/glass wares (and dilute it) at the hood, sink, or the white plastic tray to prevent spill.

Figure 9. (left) Acid bottles with labels are stored in plastic corrosion-free cabinet, and organic ones are stored in steel cabinet.

Figure 10. PPEs. (left to right) Blue chemical-proof coveralls, black nitride gloves, and face mask.

CHAPTER 3

Process Flow Design and Physical Structures of Through Wafer Vias

In this chapter, we will introduce the process flow of TWVs with detailed description for the deep silicon etching and plating processes. Using tools in UCLA NRF and ISNC, also the lab-owned Cu electroplating system. After showcasing the process development, we will also present metrology results from an optical microscope and an SEM. The process flow for fabricating TWVs is presented in Figure 11. Table 2 lists all tools be used for processing TWVs, and further discussion will also be made in this chapter.

Table 2. Tools for TWV process development

Deposition	Lithography	Etch	Metalization	Others
STS PECVD	Carls Suiss mask aligner	STS AOE (oxide etch)	Denton Sputter	Oxide furnace
Fiji G2 PEALD	Matrix asher	FDRIE (silicon etch)	Lab-owned Cu electroplating	Vacuum oven

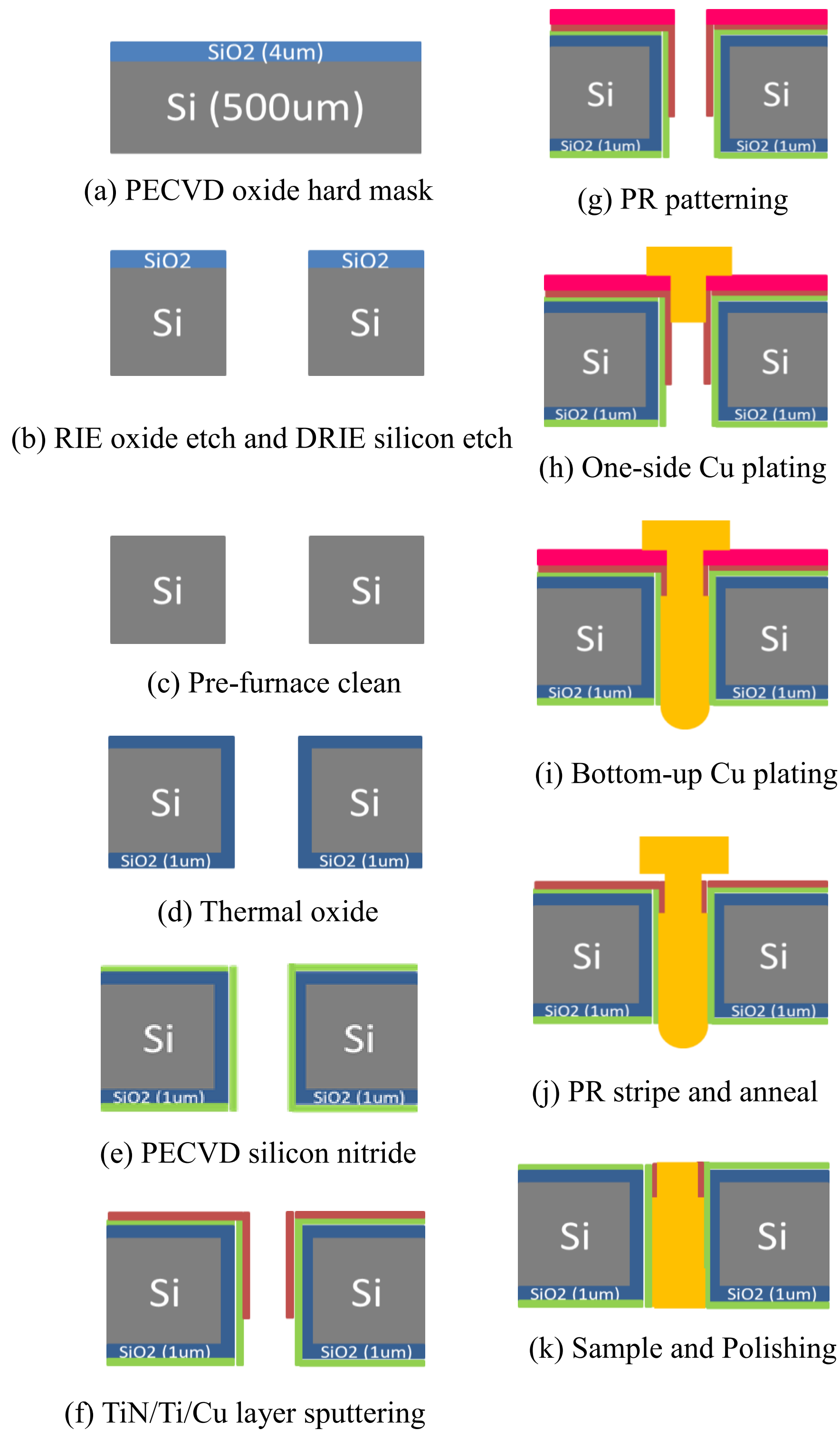


Figure 11. TWV fabrication process.

3.1 Through Wafer Via Etch

The TWV process begins with a standard p-type single-side polished 100 mm (4 inches) wafer with a <100> orientation, 500 µm in thickness, and resistivity of 10-20 Ω·cm. To optimize for power delivery, we design 100 µm diameter TWVs to support large currents and as efficient heat extraction tools.

Before silicon etch, we use plasma-enhanced chemical vapor deposition (PECVD) to deposit 4 µm of silicon oxide serve as a hard mask. A thick silicon oxide hard mask is required to achieve a good sidewall profile during the etching process of 500 µm of silicon. The via holes are formed by using dry reactive ion etch (DRIE), similar to the Bosch process [14,15]. The Bosch process includes cyclic isotropic etching and fluorocarbon-based protection film deposition by quick gas switching. The SF_6 plasma (gas etchant) cycle etches silicon, and the C_4F_8 plasma cycle creates a protection layer as passivation [16]. By controlling the number of cycles, i.e., etching time, we can also control the depth of the silicon trench. During DRIE etching, we begin with a low etch rate DRIE recipe (~5 µm/min) to etch through the first 100 µm of the Si substrate. Then, a second recipe is selected with a faster etch-rate (11 µm/min) to etch out the rest of the TWV hole leading to a cumulative taper angle of ~2 degrees. The low and high etch rate DRIE recipes include

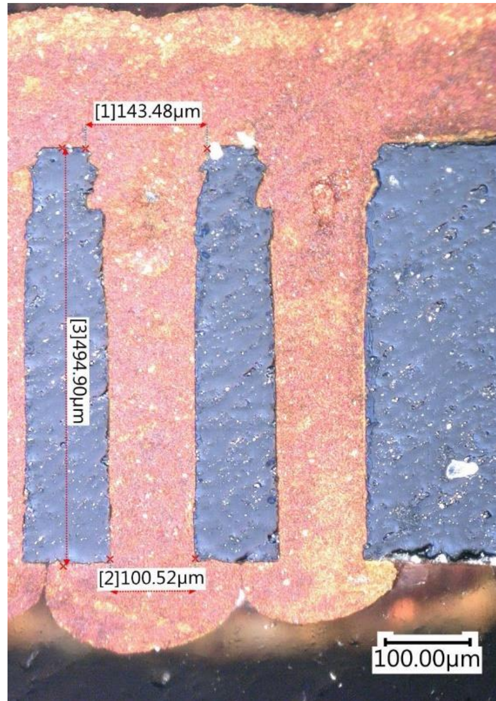


Figure 12. TWVs fabricated using a single DRIE step exhibit poor sidewall profile after Cu electroplating.

a similar flow rate of C_4H_8 and SF_6 etching gases, but different deposition time (15 vs. 80 minutes), plasma power (2,500 W vs. 3,000 W), applied voltage bias (550 V vs. 450 V) and, oxide/silicon etching selectivity (1:180 vs. 1:250). The low etch rate recipe exhibits a smaller tapering effect, but also lower selectivity as compared to the high etch DRIE recipe. The two processes are optimized to significantly reduce tapering of the 500 μm-deep TWV profile. An example of a poor TWV profile, fabricated using a single DRIE step process is shown in Figure 12, which shows significant pattern distortion during the first 100 μm of the TWV etching, and a tapered profile throughout the entire via hole.

3.2 Barrier Layer Deposition and Copper Electroplating

RIE lag [17], which is a slowdown in the etch rate at greater depth, is also observed during processing. For example, the theoretical (without considering the RIE lag) two-step DRIE process time for 500 μm etching is approximately 50 minutes, whereas in practice, in our experiments, it takes approximately 80 minutes to etch the 500 μm TWV holes. In addition, the etch rate varies at different locations of the wafer. The etch time is roughly 12% longer (70 vs. 80 minutes) at the edge of the wafer than at the center, which does not affect the quality of the center vias due to the protection provided by the thick oxide hard mask.

Prior to seed layer deposition, 1 μm of wet thermal oxide is formed as an electrical isolation layer for the TWVs. Next, a 400 nm of silicon nitride polish stop layer is deposited using PECVD on both sides of the wafer. Then a 30 nm titanium nitride (TiN) layer is deposited using atomic layer deposition, serving as a diffusion barrier [18]. The diffusion barrier is used to prevent Cu and Ti from diffusing into the silicon substrate and the thermal oxide, during high temperature processing and high current propagation. A 50 nm seed layer of Ti is deposited using DC bias sputtering on the top side of the substrate, as illustrated in Figure 2(f), serving as the adhesion layer [19] between the TiN diffusion

barrier and the Cu. Another 250 nm of Cu seed layer is sputtered on the same side (top). The Cu seed layer reaches deep along the TWV side walls, enabling the Cu electroplating process to deposit metal on the side walls.

The TWVs are electroplated using a Cu damascene electroplating process that utilizes brightener and carrier as additives. Brighteners, typically organic-sulfates such as 3-mercapto-1-propanesulfonate (MPS) or bis(3-sulfopropyl) disulfide (SPS) [20], enable a uniform current density at the interface of $CuSO_4$ electrolyte and the sidewall of via. Whereas carriers, such as polyethylene glycol (PEG) or Polyalkylene Glycol (PAG), create and maintain a defined diffusion layer at the Cu anode to control (slow down) the electroplating rate.

The electroplating of the vias, is performed in two steps. The first electroplating step is a damascene electroplating process with a layer of semi-additive AZ 4620 photoresist (PR) [21]. The AZ 4620 PR has a sufficient thickness of 10 μm to both protect the Cu seed layer from electroplating and prevent erosion of the PR within the acidic Cu electroplating setup. PR covers most of the Cu seed layer that was previously sputtered throughout the wafer. Then, the through holes are lithographically patterned, enabling electroplating of Cu only at the opening and sidewalls of the TWVs, as depicted in Figure 13. During this

first electroplating step, a low electroplating current of 70 – 100 mA is applied to ensure deposition of high-quality Cu. Cu is deposited on both the substrate surface (top side where the Cu seed layer was deposited), and the via hole sidewalls, simultaneously, with a faster electroplating rate at the substrate surface. The result of electroplating using a high current (150 mA) is shown in Figure 14. The electroplating rate is faster on the substrate side (with the seed layer), leading to voids inside the TWV.

During the second electroplating step, the wafer is flipped (top side down), and a bottom-up electroplating process is used to fill the remaining volume of the TWV. After electroplating, the wafer is annealed at 250°C for one hour in a nitrogen ambient. Finally, CMP is performed to remove the excess copper overburden, and reduce the surface

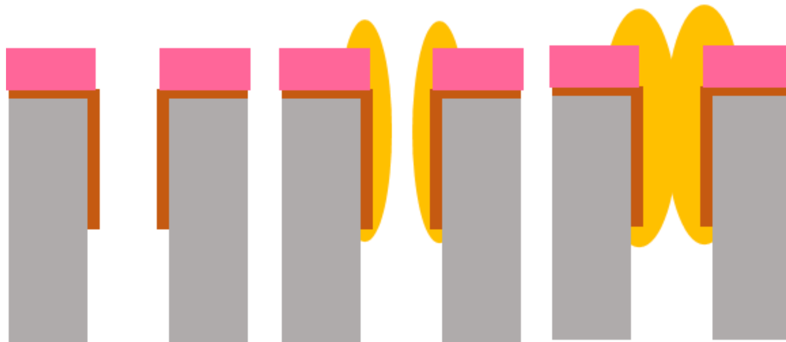


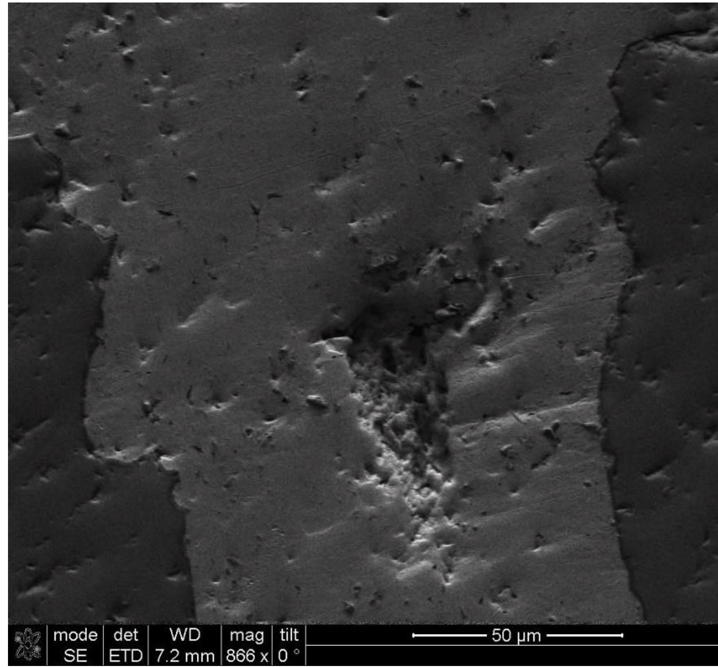
Figure 13. Schematic of the Cu electroplating process [17]. Electroplating begins (left) with a Cu seed layer (brown). Electroplated Cu (yellow) extends along the width and the length of the TWVs (center). Finally, one side of the TWV hole is sealed by the Cu (right). Note, photoresist is in pink and silicon is in gray.

roughness of the TWV.

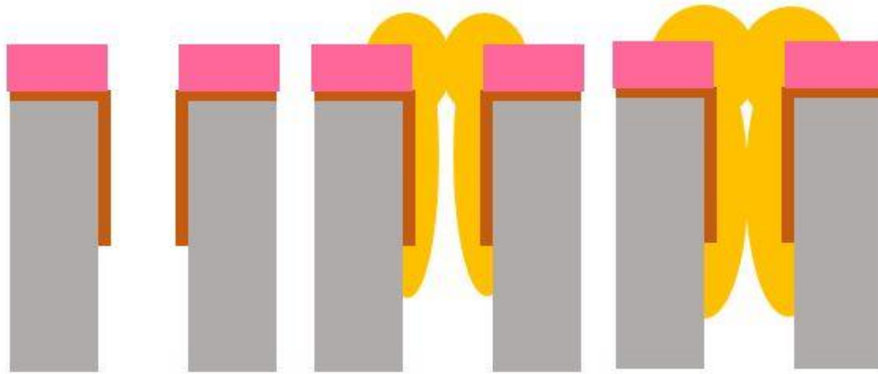
3.3 Physical Structure and Characterization

By using scanning electron microscope (SEM), we have discovered voids inside TWVs when we elevate electroplating current up to 150 mA or more. Figure 5 presents schematic Cu plating at high plating current and the SEM image of void. Higher current increases the plating rate at wafer surface even faster. The non-uniform electroplating rate between the top side and sidewall eventually causes voids inside TWVs. Moreover, large voids lead to TWV breakdown at high power delivery, we will later discuss in the section of TWV reliability analysis.

The profile from our proposed two-step DRIE is shown in Figure 15(a) with a tapering angle of 0.34 degrees, which is an improvement over the profile of the one-step DRIE from Figures 12 and 15(b) (tapering angle of 2.5 degrees). A top-view SEM image of a TWV (Figure 16) shows the distinct layers of Cu, liner oxide, and Si.

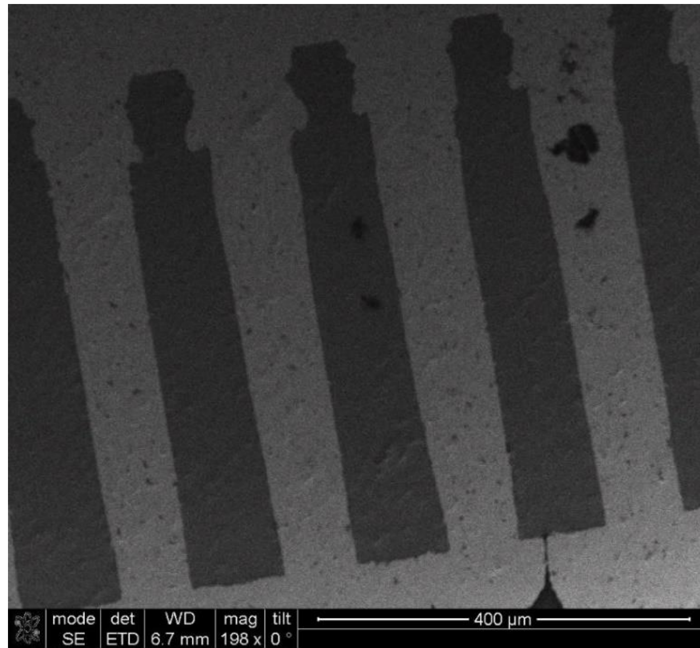


(a)

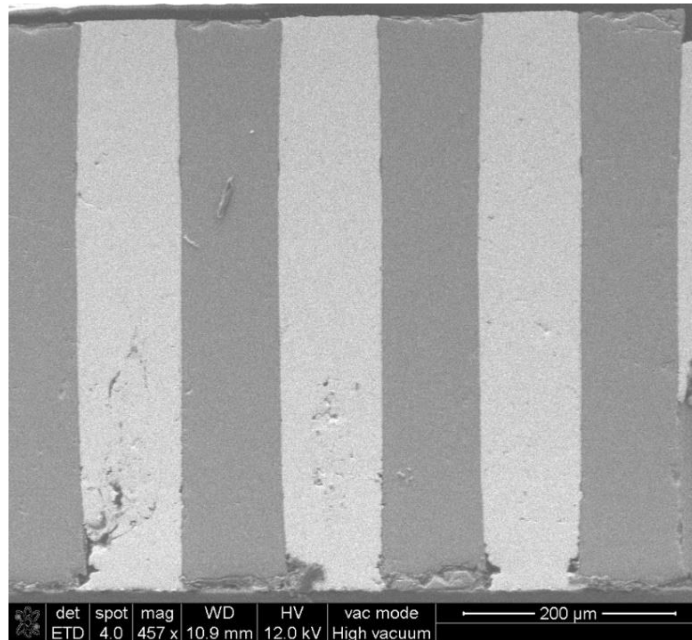


(b)

Figure 14. (a) A 10 µm x 40 µm void is identified within the TWV after using a 150 mA electroplating current. (b) Schematic of Cu electroplating at high current (≥150 mA). The electroplating rate is faster on the substrate side (with the seed layer), leaving a large void within TWV.

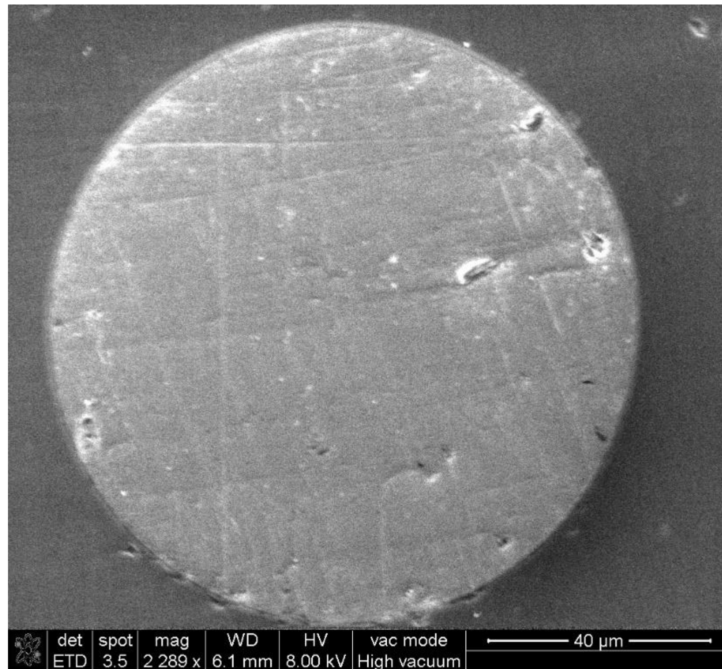


(a)

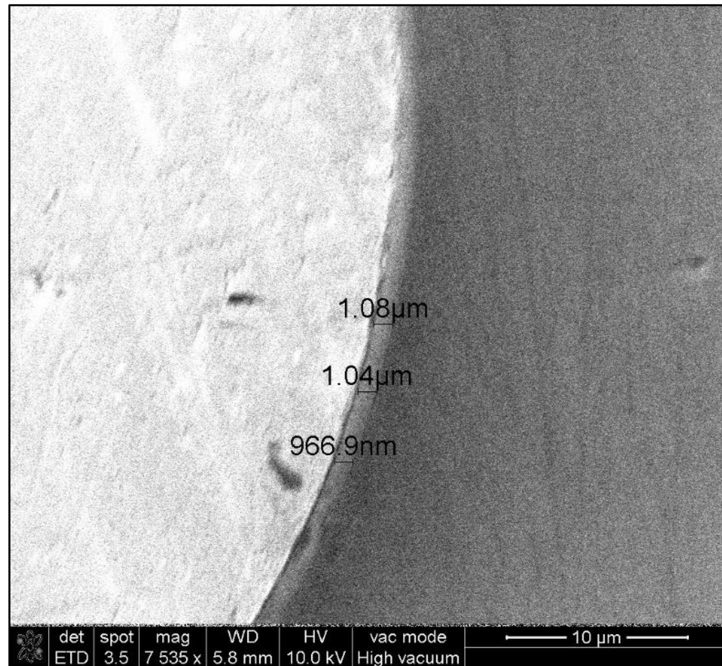


(b)

Figure 15. Cross section SEM images of TWVs with different process condition. (a) 2-step DRIE using low current (50 mA) electroplating, and (b) 1 step DRIE using medium current (100 mA) electroplating.



(a)



(b)

Figure 16. A top-view SEM image of a TWV. (a) A circular profile of the TWV, and, (b) zoom-in on the 1 μm thermal oxide isolation layer between the silicon and the copper.

CHAPTER 4

Results of Electrical and Reliability Characterization

In this chapter, we show characterization results for the TWVs, including resistance, inductance, and coupling capacitance, by using a Keysight E4980A precision LCR meter with a four-point probe setup. In addition to electrical characterization, we also examine the reliability of the TWVs using temperature cycling testing, and electrical stressing by passing a large current (>2 A) through the via.

4.1 Resistance and Resistivity of Electroplated Copper TWVs

Due to the difficulty in simultaneously accessing both sides of the TWV during electrical characterization, pairs of TWVs are shorted from the bottom side using the large overburden created during the electroplating. The TWVs are separated by a 1 µm oxide isolation and 100 µm of Si substrate, as shown in Figure 8. The shorted part at the bottom, is 250 µm in height and 4 mm in width (perpendicular to the cross section in Figure 17). The resistance of this Cu short is significantly lower (~8 µΩ) than the resistance of the TWV and can, therefore, be neglected. A four-point probe measurement of the two adjacent TWVs (connected in series) is performed, and electrical parameters of a single TWV are

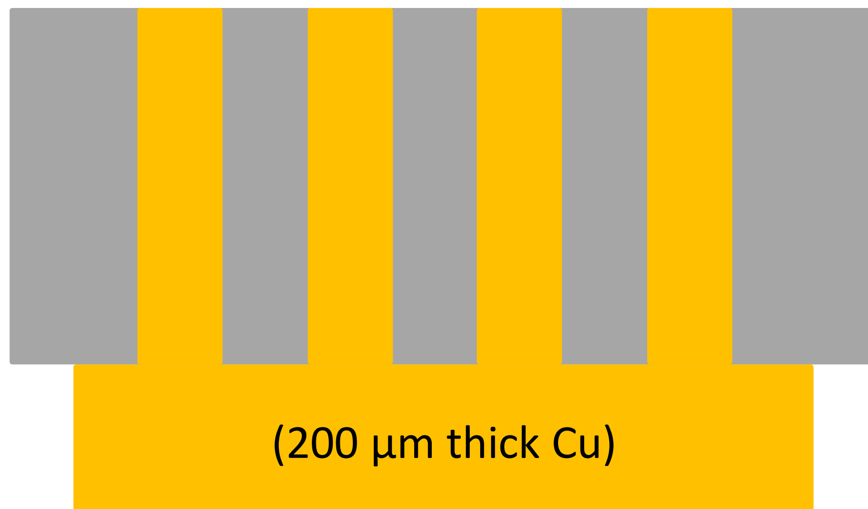


Figure 17. A schematic of two TWVs shorted on the back side of the test structure (orange). The TWVs are isolated by a 1 µm thermal oxide (blue) along with 100 µm of Si (gray). Note that the Cu thickness at the bottom is 200 µm with a width of 4 mm (perpendicular to the cross section).

extracted. After measuring 20 pairs of shorted TWVs (40 TWVs), we extract the average measured resistance of the TWV to be 1.25 mΩ, and the smallest resistance is 1.05 mΩ. The extracted smallest resistivity of TWV Cu is $1.73 \cdot 10^{-8}$ Ω·m, less than 3% higher than the theoretical resistivity of Cu ($1.68 \cdot 10^{-8}$ Ω·m), indicating a high quality of electroplated metal. Post annealing (at 250°C) resistance measurement shows negligible change as compared to the measurement before annealing (Figure 18), indicating the high-quality of the electroplated metal, and the excellent protection of TiN/Ti diffusion barrier.

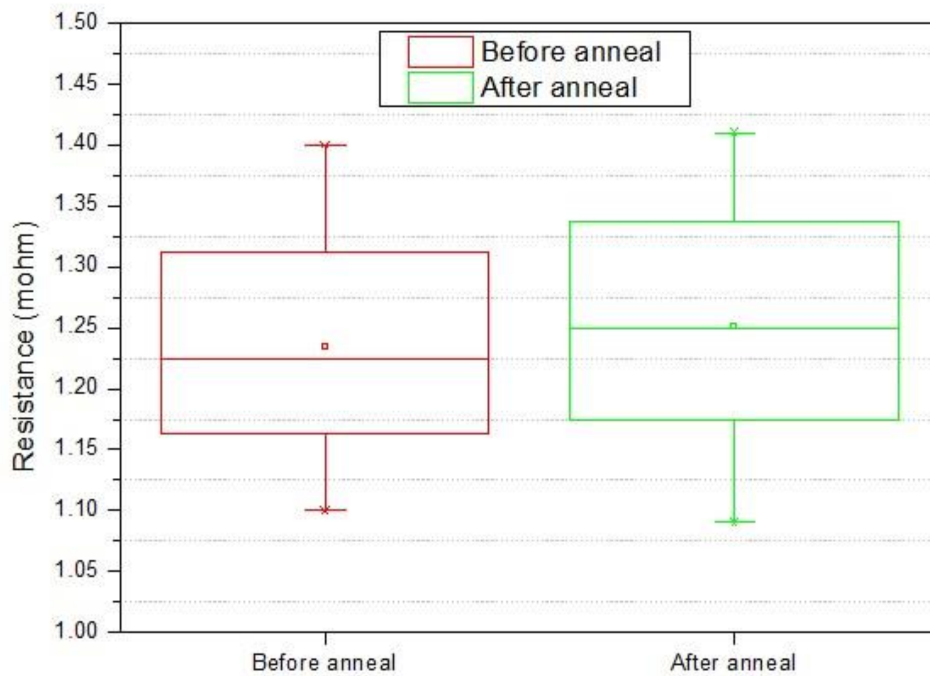


Figure 18. A statistic bar graph of extracted TWV resistance before and after annealing at 250°C.

4.2 Self-Inductance of Electroplated Copper TWVs

The inductance of the fabricated TWVs was also measured on a similar set up (Figure 8), using the same LCR meter. The measured self-inductance of the two TWVs in series is 1.7 nH at 10 kHz, 194 pH at 1 MHz, and 205pH at 2 MHz, with a minimum of 13 pH at 0.47 MHz. The data is shown in Figures 19 and 20.

At the low frequency region (<1 kHz), shown in Figure 11, the inductance of the TWV-pair (connected in series) decreases with increasing frequency. Compatible with the semiconductor physics of a large-scale MOS capacitor. Alternatively, at the higher frequency range (0.1 to 2 MHz), the inductance is approximately constant (from 0.1 to 0.5 MHz).

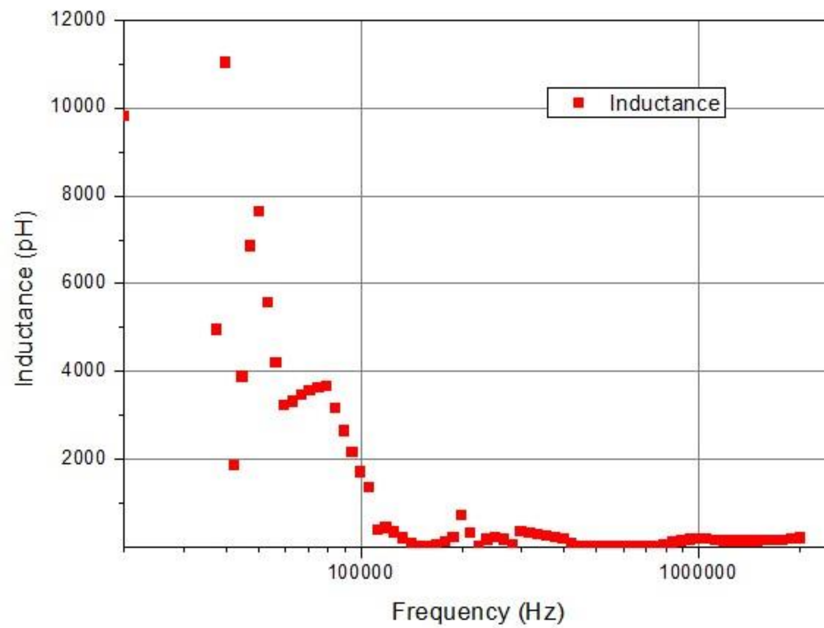


Figure 19. The inductance of two TWVs connected in series versus frequency.

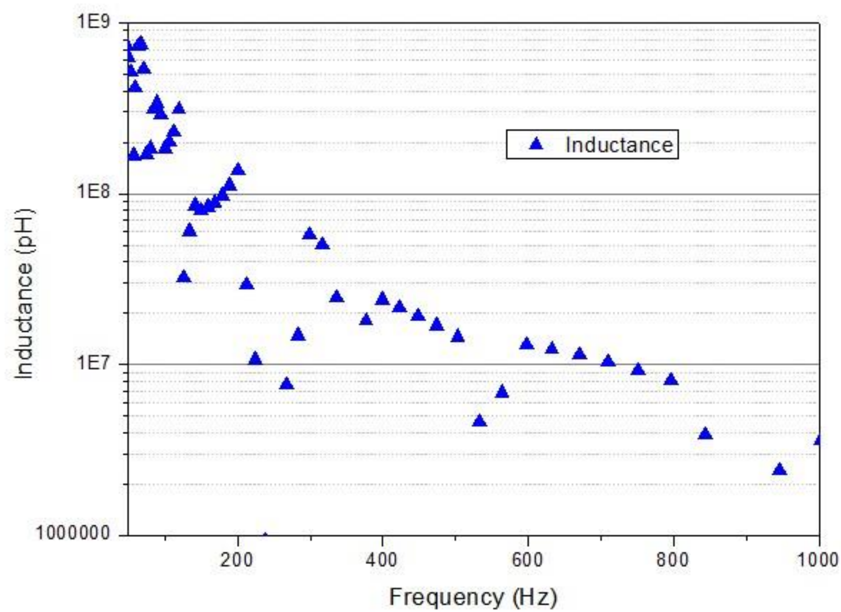


Figure 20. The inductance of two TWVs connected in series versus frequency. Zoom-in on the very low frequency region (<1 kHz)

4.3 Coupling Capacitance of Electroplated Copper TWV Pairs

The measured capacitance of the TWVs is extracted form a pair of TWVs in parallel using a TWV-dielectric-substrate model [22]. The theoretical capacitance of a pair of TWVs is 2.73 pF. To experimentally verify the capacitance of the TWVs, the excess of Cu on the bottom of the test structure was removed, resulting in two isolated TWVs (Figure 21). The measured capacitance of the TWV pairs is 2.8 pF (at 20 Hz) and 1.7 pF (at 1 MHz), with a minimum of 1.4 pF (at 0.54 MHz). The capacitance, plotted in Figure 22, decreases with increasing frequency, exhibiting concord with device physics of MOS capacitors. The measurement results agree well with the simulated values that are based on the model from [22], exhibiting a low parasitic effect.

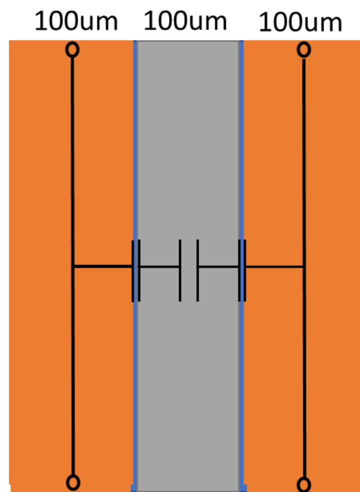


Figure 21. A simplified schematic figure of two isolated TWVs (orange) for capacitance measurement [20]. Vias are separated by a 1 μm thermal oxide (blue) and a 100 μm Si (gray).

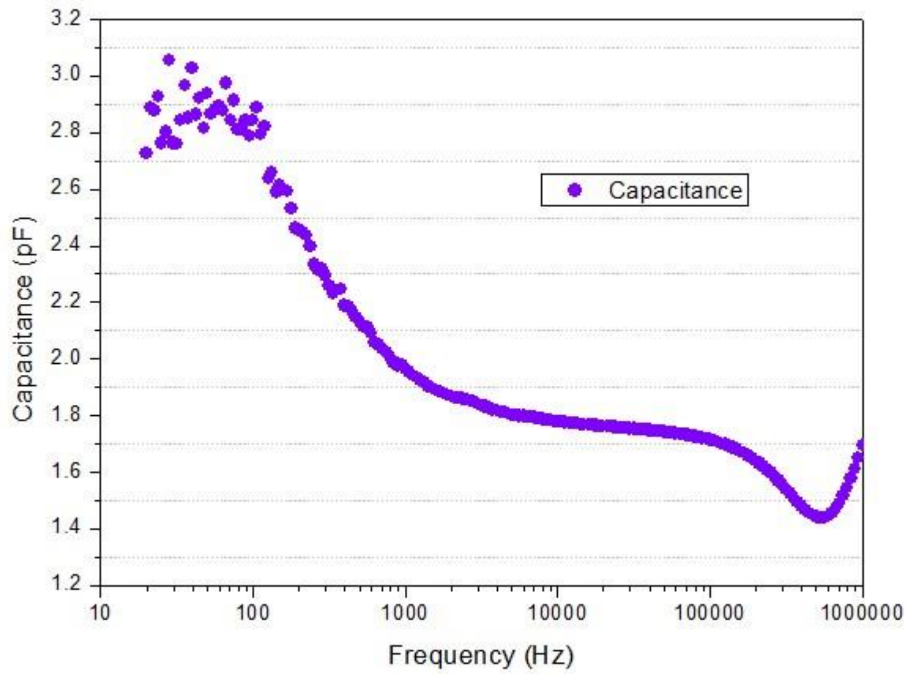


Figure 22. Capacitance measurement versus frequency between two isolated TWVs.

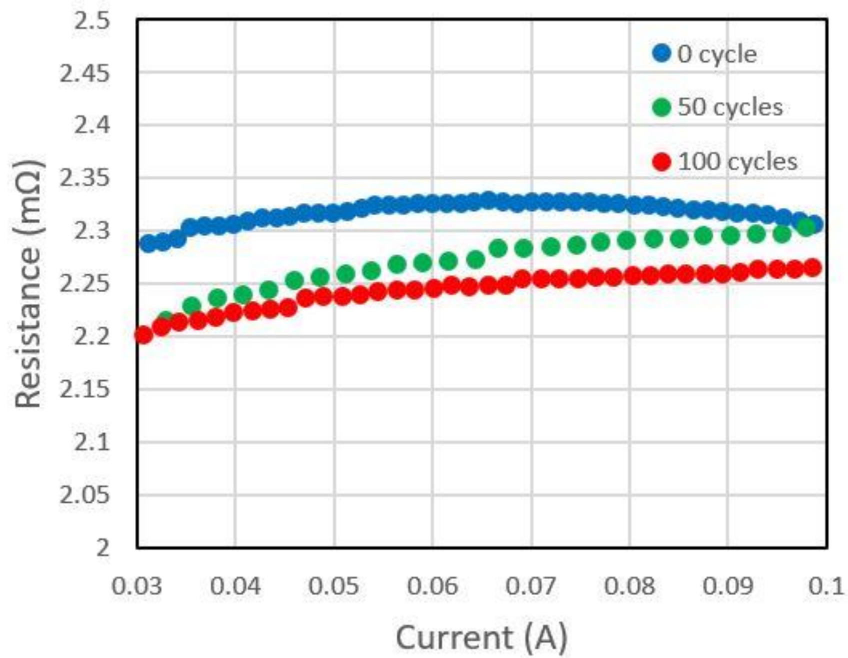


Figure 23. Resistance measurement of two shorted TWVs after temperature cycling tests.

4.4 Current Stressing and Temperature Cycling Tests

The fabricated TWVs were subjected to reliability testing. Current carrying capacity of the TWVs was evaluated using the TWV-pair test structure (Figure 7). The result shows that each TWV is capable of carrying at least 2.5 A of current at DC (limited by experiment equipment) without degradation, corresponding to a current density of 318 A/mm^2. In addition, temperature cycling test (TCT) from -40°C to 125°C (conforming to the JESD22-A104D standard) with 0, 50, and 100 cycles are performed, showing stable resistance under different current. Because the coefficient of thermal expansion (CTE) is very different between air (3690ppm/°C) and copper (16.5ppm/°C), voids within via increase the probability of TWV breakdown under TCT. The TCT results are provided in Figure 23. It can be observed that TWV resistance remains stable after the TCT, indicating that the vias have been filled up with high quality copper. In summary, TCT and large current test show good reliability of the TWVs made from our process.

4.5 IR-Drop and Integration in Simple Circuit for TWVs

In addition to the electrical characterization, a small circuit is designed to showcase the power delivery of the fabricated TWVs. A green LED is connected to two isolated arrays of TWVs using tin solder. Each leg of the LED is connected to a separate TWV

array. Due to the large size of the solder, all of TWVs in each of the arrays are connected, but arrays are still isolated from each other, through the LED. An image of the setup is shown in Figure 24. Using this simple circuit, the IR drop and power dissipation within the TWVs are also measured [23]. We have measured an IR-drop of 1.8 mV across the wafer with 20 TWVs. The extracted IR drop of a single TWV is therefore 90 μV. This experiment demonstrates that the TWV arrays (20 TWVs) dissipate only 36 μW of power (1.8 μW per TWV) in this circuit.

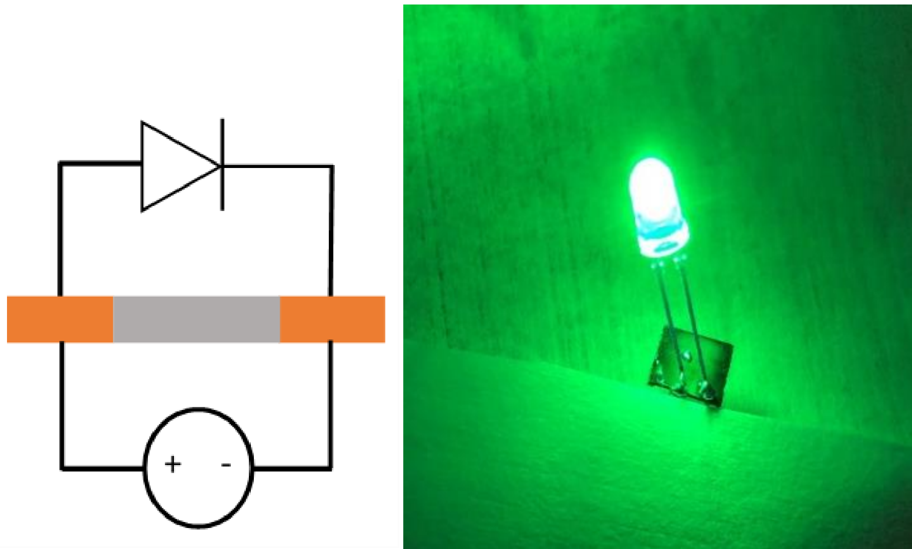


Figure 24. A schematic (left) and a photograph (right) of a green LED operating at the front side of the silicon substrate. The current is supplied from the back side of the substrate and delivered to the LED using TWVs. Note that the orange color (in schematic) stands for a set of 20 TWVs, and the gray color is the silicon wafer.

CHAPTER 5
Conclusions and Future Work

In this thesis, we have presented (1) the entire setup of lab-owned Cu electroplating system, and maintenance of wet bench with chemical storage and deposition (2) process flow of through-wafer vias for high quality power delivery across a full thickness Si wafer. The dry etch process is optimized to reduce the tapering angle from 2.5 degrees to 0.34 degrees. Moreover, reliability tests of the fabricated TWVs are performed using high current and temperature cycling testing and exhibit promising results. We measured a resistance of 1.1 mΩ, an inductance of 97 pH at 1 MHz, and a capacitance of 1.7 pF at 1 M Hz, for a single TWV, indicating a high-quality of the electroplated copper and excellent device performance. Finally, we fabricated a simple circuit using an LED and TWVs to show the functionality of the TWVs for power delivery. An IR-drop of 1.8 mV was measured, and the power dissipated in a single TWV is 1.8 µW. In conclusion, the power delivery TWVs within the Si-IF platform, exhibit good performance and reliability.

In the future, we will advance to full wafer scale TWV process development. We also plan to integrate TWVs with Si-IF and PowerTherm to show high power delivery and heat

dissipation. For characterization aspect, we plan to conduct experiments on conductance and electro-migration measurement, which the electro-migration test is a key examination for TWV reliability under high temperature. After entire wafer scale TWV process development is established, wafer scale characterization will be conducted, including process variation throughout the wafer and yield measurement.

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