UNIVERSITY OF CALIFORNIA,
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2.4 GHz Heterodyne Receiver for Healthcare Application

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical Engineering and Computer Engineering

by

Wei Cai

Thesis Committee:
Professor Frank Shi, Chair
Professor Henry Lee
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DEDICATION

To

my parents and friends

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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ABSTRACT OF THE THESIS

2.4 GHz Heterodyne Receiver for Healthcare Application

By

Wei Cai

Master of Science Sciences in Electrical and Computer Engineering

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Professor Fran Shi, Chair

Over the past 30 years, research on CMOS radio-frequency (RF) front-end circuits has progressed extremely quickly. The ultimate goal for the wireless industry is to minimize the trade-offs between performance and cost, and between performance and low power consumption design. The design is simulated with cadence tool, the design kit is from IBM 130nm.

In this thesis, the basic 2.4 GHz heterodyne receiver was designed on a 130um CMOS process. In the first part, a low noise amplifier (LNA), which is commonly used as the first stage of a receiver, is introduced and simulated. LNA performance greatly affects the overall receiver performance. The LNA was designed at the 2.4 GHz ISM band, using the cascode with an inductive degeneration topology. The design reaches the NF of 2 dB, has power consumption of 2.2 mW, and has a gain of 20dB.

The second part of this thesis presents a low power 2.4GHz down conversion Gilbert Cell mixer. The obtained result shows a conversion gain of 14.6dB and power consumption of 8.2mW at a 1.3V supply voltage.

In the third part, a high-performance LC-tank CMOS VCO was designed at 2.4 GHz. The design uses using PMOS cross-coupled topology with the varactor for wider tuning range topology. The final simulation of the phase noise is -128 dBc/Hz, and the tuning range is 2.3GHz- 2.5GHz while the total power consumption is 3.25mW. The performance of the receiver meets the specification requirements of the desired standard. In future work, a more compactly designed topology will be presented.

Chapter 1: Introduction

1.1 Motivation

Currently, remote monitoring applications are extremely important mobile technologies, because they can detect and prevent the illness. Thus, they could reduce hospital readmission rates, saving hospital resources. Remote monitoring systems help patients effectively be aware of their physical conditions, and commute more efficiently get in touch with their physicians [1].

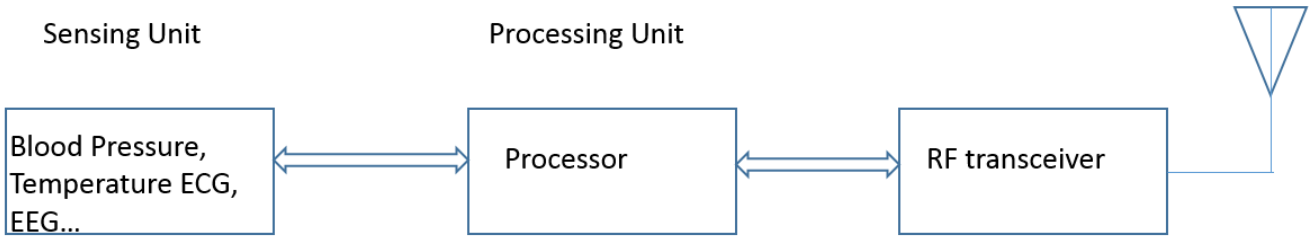


Figure 1.1 block diagram of a typical sensor node.

Fig. 1.1 shows that the basic sensing unit can collect physiological signals (e.g.: such as electroencephalography (EEG), electrocardiography (ECG), body temperature, blood pressure etc.), when individual sensors are attached to the human body [2]. The processing unit processes all the sensed signals, then processes all the data based on the communication protocols. All the processed data will be transmitted through a wireless link to a portable personal base-station.

The main challenge of such remote monitoring systems is the high power consumption of portable devices. A solutions to this challenge is the integration of the portable devices' digital part and the RF part onto one chip.

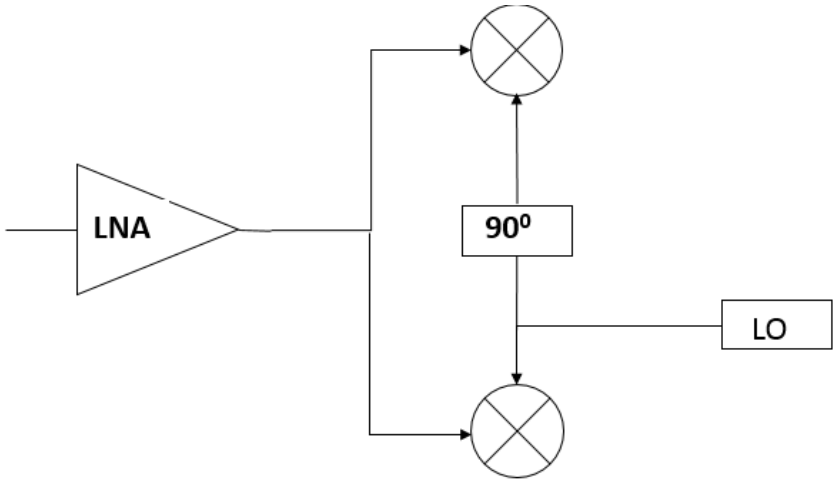


Figure 1.2: Receiver topology design

When the data is sent out by the transmitter, the receiver will pick up the signal and will also perform DSP processing [2]. The requirement of this transmitter and receiver is that both should have low power. For the front-end receiver, the major objectives are 1) receiving the RF signals and 2) recovering the biosignal classification.

This thesis proposes a low power receiver design. This system can be used in wireless ECG acquisition systems. In order to meet the standards, the system is designed as shown in Table 1.1.

Table 1.1 System Design Requirements

	NF	Gain	Power
LNA	3dB	15dB	<5mW
mixer	16dB	5dB	<10mW

VCO	Oscillation frequency	Phase noise	power
	2.4GhZ	-100dBc/Hz	<5mW

1.2 Objective and Major Contributions

The objective of this research is to build a 2.4GHz Heterodyne receiver, which consists of an LNA, a mixer and a VCO. In this thesis, LNAs use cascode inductor degeneration topology, mixers use gilbert cells, and VCOs use LC tank topologies. All of these components use 2.4 GHz.

First, the LNA has a cascode topology and an input matching network with a series inductor to achieve a high gain of the LNA. This is shown by our simulation, which consumes only 1.7 mA with a 1.3 V power supply and achieves a gain of 20 dB and NF of 1.9 dB.

Second, the mixer is a double balanced active mixer using gilbert cell topology, which has a high conservation gain. Again our simulation results show that the mixer consumes only 6.3 mA with a 1.3 V power supply and achieves a gain of 5 dB and NF of 15 dB.

Lastly, the VCO has a cross-coupled PMOS pair to achieve negative resistance, and it has a LC tank which be use to reach a resonant frequency of 2.4GHz. Simulation results show that, the VCO consumes only 2.5mA with a 1.3 V power supply and achieves a phase noise of -129dBc/Hz, KVCO is around 3MHz/V.

1.3 Thesis Organization

The thesis is organized into six chapters. Chapter 1 provides an introduction of the wireless standards. In Chapter 2, I introduce the receiver architectures and modulation of the QPSK communication system. Chapter 3 introduces basic LNA topology and presents the results of LNA simulation. Chapter 4 gives an introduction mixer topology and mixer simulation results. Chapter 5 describes VCO topology and VCO design. Chapter 6 draws conclusions.

Chapter 2: Background Introduction

2.1 Introduction to Wireless Communication

Wireless Local Area Networks (WLANs) are everywhere in our daily life, like air or water. During the last 40 years, companies have been busy with implemented WLAN infrastructures into offices to provide more convenience and better data communication across their LAN. For the sake of the interoperability, most WLAN infrastructure use WLAN standards is 802.11a and primarily 802.11b [3]. The 802.11 standard is used to provide solutions for business, home, and "hot spot" WLAN needs [3].

The 802.11b standard was an expansion of the IEEE 802.11 standard. 802.11b can support bandwidths up to 11Mbps and uses the same radio signaling frequency (2.4 GHz) as 802.11. However, interference can incur from appliances such as microwaves and cordless phones that the same 2.4 GHz range [4]. The pros of the 802.11b standard are lower costs and improved signal range. The cons are slower maximum speed fewer simultaneous users, and appliances can interfere with the frequency band.

The 802.11a standard is another extension of the original 802.11 standard. What many people do not know is that 802.11a was created at the same time as 802.11b. This is

due to the fact that 802.11b is more popular than the 802.11a. While 802.11b targets the home market, 802.11a standard is more suitable for the business market because of its higher cost. The pros of the 802.11a are faster speeds to support more users at the same time and the use of specific frequencies which can prevent devices from interfering with each other. The cons are higher cost, a shorter range than 802.11b, and that it can be easily blocked.

A new standard is 802.11g, which also has a speed of 54Mbps, similar to 802.11a. It is important to note that 802.11g is more attractive because it operates in the lower 2.4GHz unlicensed radio band, while 802.11a operates in the higher 5GHz unlicensed radio band. In other words, compared to 802.11a, 802.11g throughput drops slower over distance [5]. On the other hand, sometimes the 802.11a standard is preferred, because the 5GHz band provides many more channels than 802.11g [4].

With an 802.11g access point, 802.11b and 802.11g network interface cards (NICs) can operate together. This makes transition 802.11g smooth for existing 802.11b networks because NICs can still work with the newer 802.11g access points. [5].

Bluetooth is another wireless technology that has a different purposes comparable to WLAN [5]. It is designed to functioning in personal area networks (PANs) where a few devices are carried by a person around their desk [4]. The pros of bluetooth are its lower cost, lower battery consumption, and the fact that it provides application profiles, which are application-layer standards that are designed to allow users to work together spontaneously, with little intercession [4].

In contrast, the cons associated with bluetooth include its rated speed, distance, number of devices, and scalability. Bluetooth provides 722 kbps with a back channel of 56

kbps which it may increase. However, it is much slower than 802.11 standards. Also, its maximum coverage is only 10 meters. Bluetooth scalability is poor compared to 802.11, because 802.11 has more multiple access points [4].

The problem that bluetooth has is that it can interfere with 802.11b networks because they both operate in the 2.4GHz band. People are currently working to reduce transmission interference between these two networks but they still have some problems [11].

2.2 Receiver Architecture

Heterodyne and homodyne receivers are the two main architectures for the radio communication system. In order to find a proper architecture, one needs to consider the complexity, cost, power dissipation and the number of external components [15].

2.2.1 Heterodyne Receiver

The heterodyne receiver is probably the most popular receiver architecture and it has been widely implemented in many radio applications.

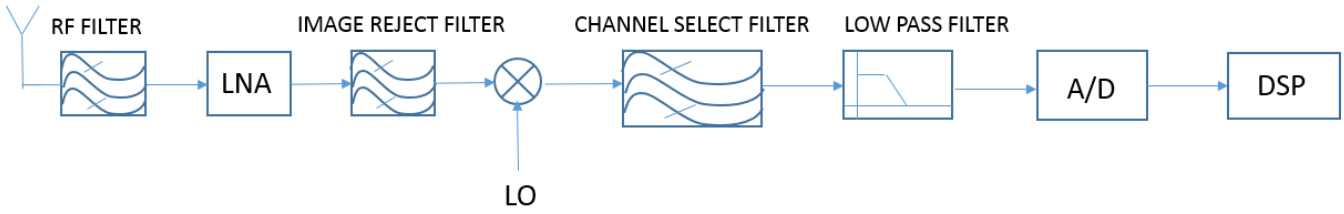


Figure 2.1 Heterodyne receiver

As seen in Fig. 2.1, RF filters can filter out unwanted out-of-band signals of the incoming signal. Then the signal goes in to a low noise amplifier, which applies it. The

signal is then filtered by the image-reject (IR) filter to further reduce the power level of undesired signals. A mixer can convert this RF signal to the intermediate frequency (IF) by its down-conversion. After passing through a narrow-band IF filter, a signal is converted to a baseband signal for further processing in subsequent stages. Intermediate frequency (IF) is a critical parameter in heterodyne receiver design [8]. When it comes to choosing a fundamental IF frequency, there is always a tradeoff between image rejection and channel selection or sensitivity. Specifically, when image frequency is far away from the desired frequency, a higher IF should be chosen. Therefore, a lower IF leads to a higher rejection rate of the interference of adjacent channels. Fig. 2.2 shows two cases that correspond to high and low values of IF so as to illustrate the trade-offs. Therefore, to choose proper IF depends on three parameters: the image noise, the distance between the desired band and the image, and the loss of the image reject filter. To minimize the image, one can either increase the IF or tolerate losses in the filter while increasing its quality factor [15].

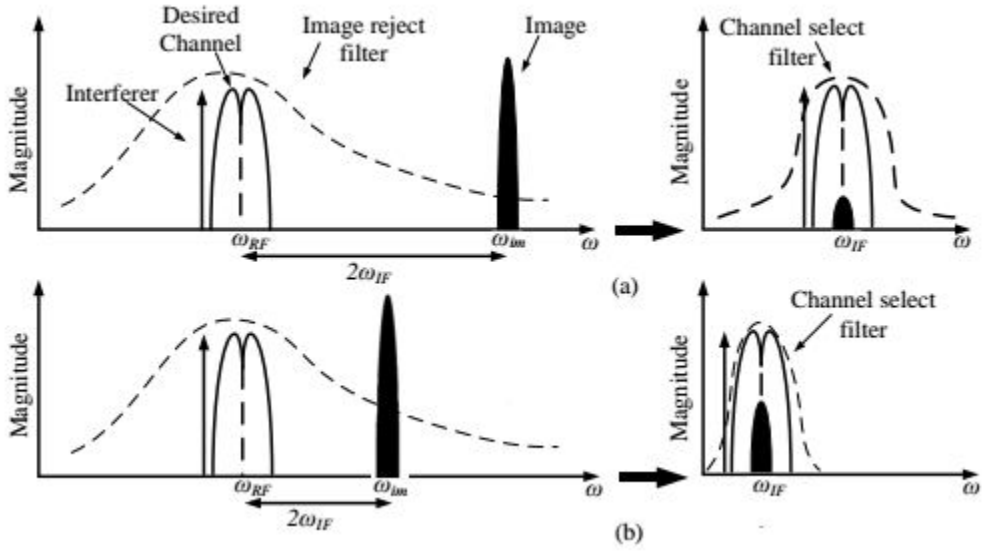


Figure 2.2 Rejection of image versus suppression of interferers for (a) high IF and (b) low IF [13]

2.2.2 Homodyne Receiver

A homodyne receiver is also called a zero-IF or direct conversion receiver. For double-sideband amplitude modulated signals, it can be down converted by simple mixers. For frequency and phase modulated signals, down conversion must be performed with quadrature mixers so as to avoid loss of information due to the overlap positive and the negative spectra after down-conversion [16]. The block diagram of a homodyne or direct conversion receiver architecture is illustrated in Fig. 2.3.

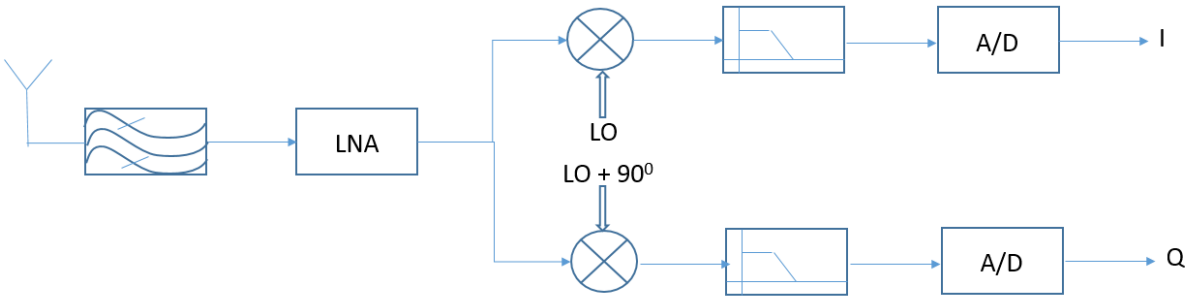


Figure 2.3 Homodyne receiver

A homodyne receiver structure is very similar to a low-IF receiver. The main difference is that it down-converts RF signal frequencies directly to base band frequencies. One major advantage of the homodyne architecture is that the image is circumvented because it is equal to zero [16]. As a result, no IR filter is required, and the LNA does not to drive a 50 Ω impedance of an off-chip IR filter, which reduces the overall power consumption. Secondly, low-pass filters and baseband amplifiers are substituting IF filters

and subsequent down-conversion stages, so they can integrate on a single chip [19]. However, issues with the homodyne receiver that would degrade the system performance [19]. The main disadvantage is the DC offset problem, because DC offset can easily corrupt the desired baseband signal and saturate the following stages. The isolation between the LO port, the input of the mixer, and the LNA is not perfect. There is a finite amount of feed-through from the LO port to the LNA and mixer inputs. This leakage signal is then mixed with the LO signal, thus generating a dc component. This phenomenon is called "self-mixing". Another serious problem with homodyne receivers is that mismatch between I/Q amplitude and phase mismatch can cause degraded SNR performance. Due to the quadrature mixing requirement, either the RF signal or the LO output must be shifted by 90^0 to fix this I/Q mismatch. But since shifting the RF signal generally causes severe noise-power-gain trade-offs, it is more plausible to use the topology in Fig. 2.3 to shit LO output.

2.3 Modulation

Many communication standards are widely used in our current daily life in applications, such as cellular networks, personal area networks (PAN), wireless local area networks (WLAN), and the upcoming wireless metropolitan area networks (WiMAX). These wireless standards include Bluetooth, IEEE802.1 Ix, and Zigbee, and are suitable for covering short distances at a low cost. Using a receiver and transmitter in one Si chip is more reasonable for maintaining low costs. Insufficient power consumption is another concern for wireless devices implementing these standards. The device's low power can be achieved by the specific architecture, but this can reduce its flexibility. Additionally, due to the limited available bandwidth of the FCC, new standards for higher

data rates will require the use of non-constant envelope modulation techniques which introduce even great power consumption by the device [5].

Modulation is the process of transforming a baseband signal into a passband signal, and this passband signal can be transmitted. The modulation types usually includes analog, digital types, and pulse modulation. Analog modulation is the transfer of an analog signal over an analog bandpass channel of a different frequency [6]. On the other hand, digital modulation the transfer of digital bits over an analog band pass channel. Additionally, the pulse modulation is the transfer of a narrowband analog signal over a wideband baseband channel.

QPSK (Quadrature Phase Shift Keying) is one type of pulse shaping modulation. QPSK sends two bits of digital information at a time, without the use of another carrier frequency [11]. The benefit of the QPSK is that the transfer of a QPSK signal is reliably half of that required for BPSK signals, which in turn makes room for more users on the channel. QPSK is thus widely used in the wireless communication [7].

The basic ideas of QPSK generation is shown in the Fig. 2.4. To do this, two BPSK signals are first added together for transmission, and then transmitted to the carrier frequency [6]. Thus, the signals occupy the same portion of the radio frequency spectrum. In other words, the basic idea is that the two groups of signals are irretrievably mixed, which requires 90^0 of phase shift between the carriers, allowing the receiver to separate the two sidebands.

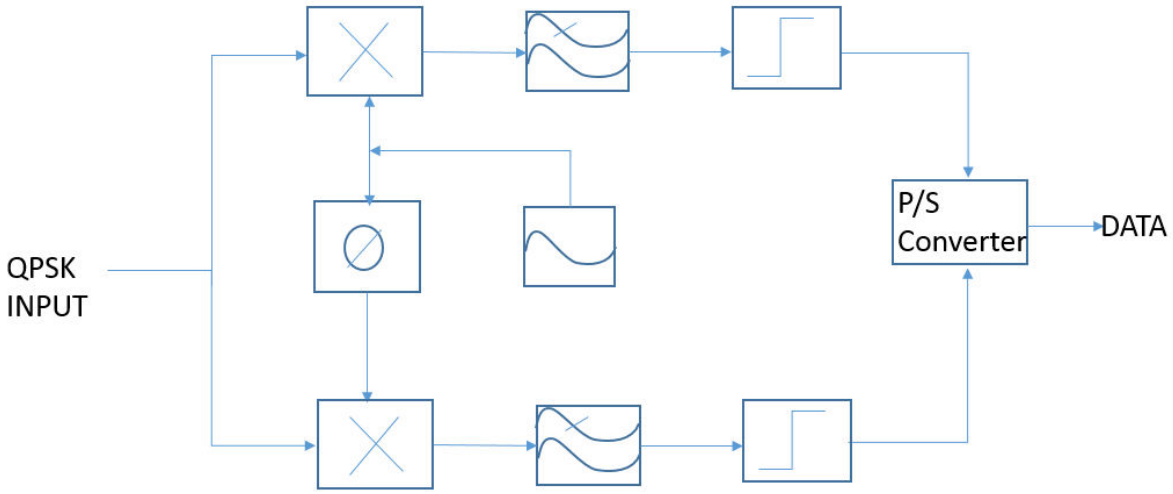


Figure 2.4 block diagram of the mathematical implementation of QPSK demodulation

Chapter 3: LNA design

3.1 LNA Design Parameters

When the signal comes from antenna, the desired RF signal is weak and surrounded by noise and interferences. Thus, the receiver design involves many issues and considerations. LNA is the first critical block in the receiving chain. Noise Figure (NF) and gain play significant roles in the overall performance of the LNA. Since the overall NF of the receiver system is dominated by the first stage, the NF of the LNA has to be as low as possible. Furthermore, the gain of the LNA needs to be high enough to reduce the noise contributions of the following stages; however, it should be not high enough to degrade the overall system's linearity [9].

The linearity of a system determines the maximum allowable input of the signal. Since all systems have nonlinear characteristics, signal distortion is a way to measure the

nonlinear circuits. The common parameters are the 1-dB compression point (P1dB) and the third-order intercept point (IP3) [8].

3.1.1 The 1-dB Compression Point

A sinusoid is applied to a nonlinear system, and the output waveform then has components that are integer multiples of the input frequency. The equation will be:

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2 cos^2\omega t + \alpha_3 A^3 cos^3\omega t + \cdots \approx \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{\alpha_3 A^3}{4})\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\,\omega t + \frac{\alpha_3 A^3}{4}\cos 3\,\omega t \quad (3.1)$$

Where A is the amplitude of the input signal.

In Eq. (3.1), the $\alpha_1 A\cos\omega t$ term includes the input frequency that is the "fundamental" and the other terms with higher-order frequencies are the "harmonics". Based on the equation, the gain is a decreasing function of A (amplitude). When increasing the input power, the circuit then becomes saturated and this distorts the linear input [8].

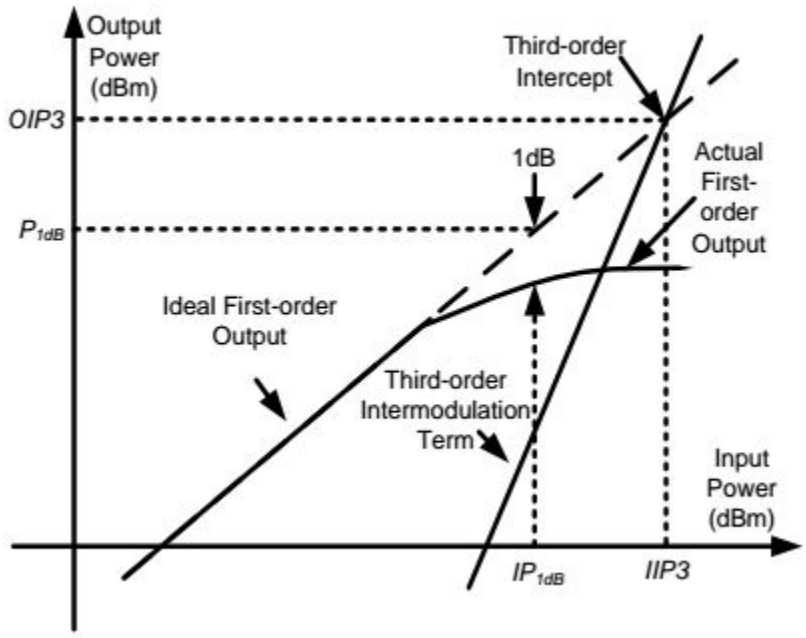


Figure 3.1 Illustrations of P1dB and IP3 [13]

Fig. 3.1 shows the gain compression due to nonlinearities in the system. The 1 dB point is the point at which the power gain begins to drop 1dB from the ideal curve. The input power is usually referred to as IP1dB. The 1-dB compression point can be calculated as [19]:

$$IP_{1dB} = 20\log_{10}\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{3.2}$$

3.1.2 The 3rd Order Intercept Point

In RF systems, the other parameter of nonlinear behavior is called the “third order intercept point”, which is done by a “two-tone” test [9].

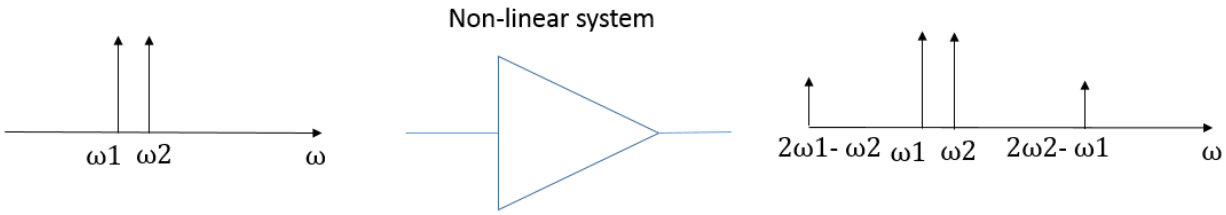


Figure 3.2 Two-tone test

When two signals with different frequencies are applied to a nonlinear system (Fig. 3.2), the output waveform has some components that are not input frequencies but are instead harmonics. This is called intermodulation (IM), and is caused by two signals "mixing" (multiplication) [9]. Assuming that the input signal is $(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, then the output through the system will be:

$$(t) = \alpha_1(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 + \alpha_3(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \quad (3.3)$$

3.1.3 Noise Figure

Noise factor (F) is a parameter of the noise performance of a circuit. It is frequently expressed in decibels (dB) and commonly referred to as a noise figure (NF) [8]:

$$NF = 10 \log_{10} F \quad (3.4)$$

Where F is defined as:

$$F = \frac{SNR_{in}}{SNR_{out}} \quad (3.5)$$

And SNR_{in} and SNR_{out} are the signal-to-noise ratio at the input and output, per unit bandwidth. It follows that:

$$P_{sig} = P_{RS} \cdot F \cdot SNR_{out} \tag{3.6}$$

For a cascade system with N stages, the total noise factor [19] can be expressed by the Friis equation:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{P1}} + \frac{F_3 - 1}{A_{P1}A_{P2}} + \cdots + \frac{F_N - 1}{A_{P1}A_{P2}\cdots A_{P(N-1)}} \tag{3.7}$$

Based on this Eq. (3.7), each stage contributes to noise, while each stage noise will decrease as the gain of the preceding stage increases. Thus, the first stage is the most critical stage in the cascode stage [9]. Generally, for the receiver, the LNA is the first active block after the antenna. Therefore, LNA NF would directly contribute to the whole system's NF. An ideal LNA should offer large gain in order to overcome the noise contribution of the following stages and add little noise [12].

3.2 LNA Topologies

Input matching architectures in LNAs can be classified into four types: Common Source (CS) with resistive termination, Common Gate (CG), CS with shunt feedback and CS with inductive source degeneration [13]. Each of these architectures can be implemented in either single-ended or differential form.

3.2.1 Common-Source Stage with Resistive Termination LNA

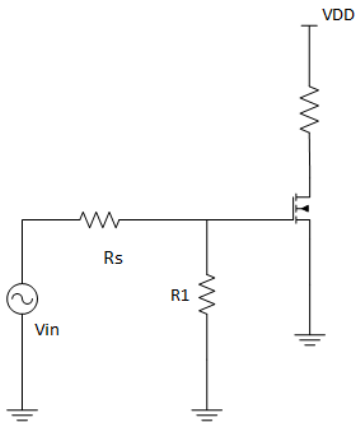


Figure 3.3 Common-source with resistive termination

This technique uses resistive termination in the input port to provide 50 input impedance, as shown in Fig. 3.3. This resistor R_1 is 50Ω which is placed in parallel with the input, in order for the input to match. However, this termination resistor generates noise. The noise factor of the circuit can be calculated as

$$F = \frac{\overline{v_{n,out}^2}}{\overline{v_{n,o,Rs}^2}} = \frac{\overline{v_{n,o,Rs}^2} + \overline{v_{n,o,R1}^2} + \overline{v_{n,o,M1}^2}}{\overline{v_{n,o,Rs}^2}} = \frac{4kT(R_s//R_1)g_m^2R_L^2\,\Delta f + \overline{i_{n,d}^2}R_L^2}{\frac{1}{4}g_m^2R_L^2}\frac{1}{4kTR_s\Delta f} \quad (3.8)[13]$$

where $\overline{v_{n,out}^2}$ represents the total output noise;

$\overline{v_{n,o,Rs}^2}$, $\overline{v_{n,o,R1}^2}$ and $\overline{v_{n,o,M1}^2}$ are the output noise due to R_s, R_1 and M1, respectively.
k is the Boltzmann's constant and T is the absolute temperature.

Transistor M1 has various noise sources. Here, we only consider the channel thermal noise for simplicity. Eq. (3.8) can be further simplified to:

$$F = \frac{4(R_s\,//\,R_1)}{R_s} + \frac{4\gamma}{\alpha g_m R_s} = 2 + 4\frac{\gamma}{\alpha}\frac{1}{g_m R_s} \quad (3.9)\ [13]$$

Where g_m is the transconductance of the input device,
and α is the ratio of g_m to the zero V_{DS} channel conductance.

There are two reasons why the NF of this structure is very high. First of all, the added resistor R_1 contributes a lot noise, and R_s contribute the same amount of the noise as R_1 [18]. This results in a factor of 2 in the first term of Eq. (3.9). Secondly, the input is attenuated, leading to a factor of 4 in the second term of Eq. (3.9) [13]. Because of the poor NF, this architecture is not popular for applications. Thus, a low noise as well as a good input matching is required.

3.2.2 Common-Gate LNA

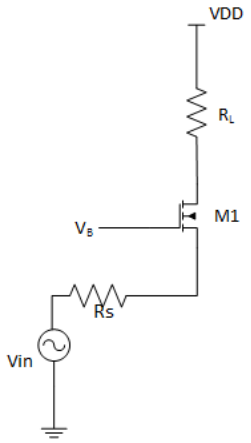


Figure 3.4 simplified common gate LNA.

Such a topology as shown in Fig. 3.4 is well known for wideband applications [14]. The input impedance and voltage gain of a common gate LNA are:

$$Z_{in} = \frac{1}{g_m} \tag{3.10}$$

$$A = g_m R_L \tag{3.11}$$

For the purpose of input matching, the g_m value is fixed at $1/R_s$. As a result, only the load impedance R_L remains as a design variable. But the transconductance of the input transistor cannot be arbitrarily high, as this it would cause a high noise factor. Through derivation, the total noise factor [13] of common gate LNA can be simplified as:

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_S} \tag{3.12}$$

The noise factor simply becomes $1+\gamma/\alpha$ after input matching [13]. This noise factor is reasonable for communication systems. However, other noise sources are from gate induced noise and substrate noise, as well as biasing circuits.

3.2.3 Common-Source Stage with Shunt Feedback LNA

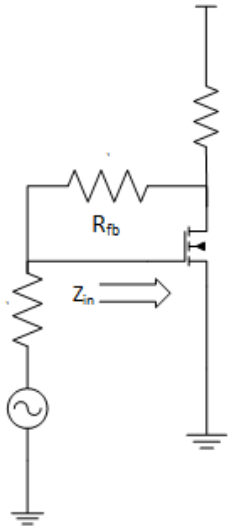


Figure 3.5 Common- source input stage with shunt feedback

Fig. 3.5 illustrates the common source stage with feedback topology. The input impedance [8] can be expressed as:

$$Z_{in} \approx R_{fb}/(1 + |A_v|) \tag{3.13}$$

Where R_{fb} is the feedback resistor,

And A_v is the corresponding voltage gain.

The noise factor for this configuration can be expressed as follows:

$$F = 1 + \left(\frac{G_s+G_{fb}}{g_m+G_{fb}}\right)^2 R_s(G_L + \gamma g_{d0}) + (\frac{G_s+G_{fb}}{g_m+G_{fb}})^2 R_s G_{fb} \tag{3.14}[13]$$

Where g_{d0} is the zero V_{DS} channel conductance, and G_s, G_{fb} and G_L is the conductance of the resistors R_s, R_{fb} and R_L, respectively.

This topology is commonly used for wideband applications. It normally can achieve a lower NF than the conventional common gate LNA. The disadvantage of this topology is, first, the input impedance Z_{in} is highly dependent on R_{fb} and A_v. . And these parameters are highly sensitive to process variations, which would cause many uncertainties. Second, the feedback signal may contain substantial noise, and thus would affect the output NF. Lastly,

the total phase shift in the loop may create instability for certain source and load impedances [18].

3.2.4 Common Source Input Stage with Source Inductive Degeneration LNA

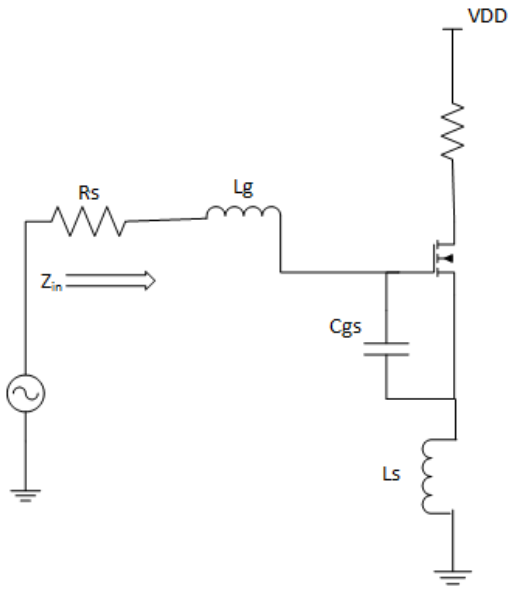


Figure 3.6 Common source input stage with source inductive degeneration

Fig. 3.6 shows the topology of a common source input stage with source inductive degeneration. The input impedance [8] is

$$Z_{in} \approx \left(\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\right) + \frac{g_m L_s}{C_{gs}} \tag{3.15}$$

In the Eq. (3.15), the resistive term is directly proportional to the inductance value. Reactance is noiseless, so it does not generate thermal noise, and it not will contribute any NF [9]. The greatest advantage of this is that it can provide the specified input impedance without adding noise to the amplifier. To get the 50Ω input impedance, the real part should be equal to 50 and the imaginary part should be zero at the frequency of interest.

Based on the analysis, the CS topology with source inductive degeneration can provide a low NF, and a comparable gain. Additionally, this topology is widely used in the

design of CMOS narrow-band LNAs [8]. The disadvantage of this topology is that the low quality factor of an inductor in the CMOS process, results in a large parasitic resistance, which would considerably degrade the NF of the LNA.

3.3 LNA Design and Simulation Results

3.3.1 LNA Design

In Figure 3.7, there is a cascode common-source with inductive degeneration. The M1 and M2 consisted of cascode opamp and the tank circuit consisted of by C_d and L_d. The transistor M3 was used for amplifier biasing. The purpose of inductors L_g, L_s and capacitor C_{gs} was to match to the 50Ω input. The degeneration inductor L_s had better linearity at the cost of lower gain for linearity. R was used to isolate the RF biasing signals. Other capacitors were used to block DC signals.

The design methodology chosen is divided into the following:

Step 1: This design was based on a LNA with a 2.4GHz frequency. The approximated input impedance expression is

$$Z_{in} \approx \left(\omega L_g + \omega L_s - \frac{1}{\omega C_{gs}}\right) + \frac{g_{m1} L_s}{C_{gs}} \tag{3.16}$$

The inductive degeneration L_s will modify the real part of the input impedance, as can be seen in (3.16). Thus, there is a value L_s that corresponds to R $\{Z_{in}\}$ = 50Ω

L_s is in series with the gate so that the imaginary part of the input impedance is zero.

Step 2 : Current density is based on the minimum noise figure (NF). Different current densities would generate different noise figures, so finding the right current density is

critical. This project used the IBM 130nm node, in order to calculate the noise figure based on the process parameters.

Below is the noise power at the output of the common-source amplifier for noise due to gate resistance, drain channel noise and gate induced noise, respectively [13].

$$v_{nO,r_g}^2 \approx 4kTr_g g_{m1}^2 R_L^2 \tag{3.17}$$

$$v_{nO,i_d}^2 \approx 4kT\gamma g_{m1} R_L^2 \tag{3.18}$$

$$v_{nO,i_g}^2 \approx \frac{4}{5} kT\delta\omega^2 C_{gs1}^2 g_{m1} R_L^2 \tag{3.19}$$

where r_g is the gate resistance,

T is the temperature,

k is the Boltzmann constant,

R_L is the amplifier load,

γ is the excess-noise factor, its value is $2/3$ for long channel transistors in strong inversion,

ω is the angular frequency of the signal and

δ is a correction factor, its value is $4/3$ in strong inversion.

The signal power is given by $P_{out} = \frac{v_{out}^2}{R_L} = g_m^2 v_{in}^2 R_L$

$$NF = P_{in}/P_{out} \tag{3.20}$$

This equation represents the relationship between the NF and I_d. Based on Eq. (3.17), the noise due to gate resistance is proportional to the current, based on the Square Law Model ($g_m \propto \sqrt{I_d}$) [13]. Since the output power is proportional to g_m^2 , the NF is not sensitive when I_d changes. Like gate resistance noise, Eq. (3.18) and (3.19), are proportional to$\sqrt{I_d}$. Thus, increasing the current reduces the NF. The increase in NF for higher I_d was

observed due to effects that were not considered, such as the increase of γ with bias current [5].

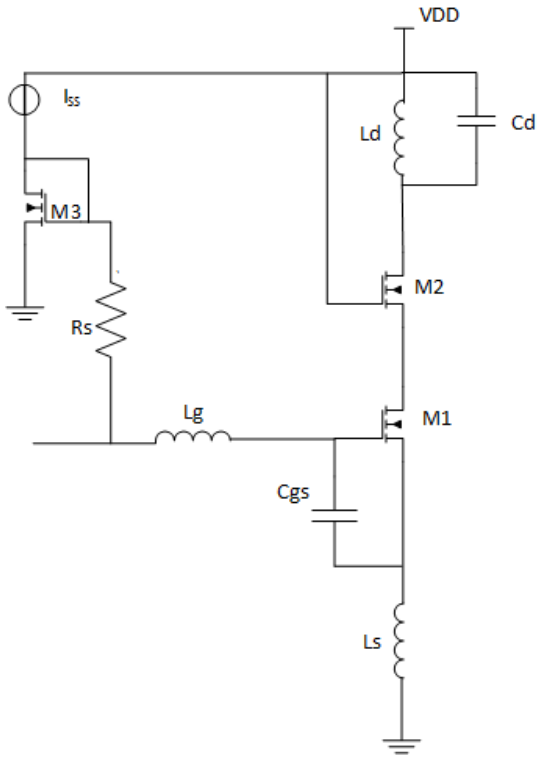


Figure 3.7 2.4GHz LNA design schematic

All the values are presented in Table 1.

Table 3.1 2.4 GHz LNA components values

Parameter	Sizes (unit)
M1, M2	W/L=10 um/180 nm
M3	W/L=2.5 um/180 nm
L_s	500 pH (Q=20)
L_g	30 nH (Q=20)
L_d	8 nH(Q=20)
C_{gs}	120 fF
C_d	440 fF

R_s	10K

3.3.2 LNA Simulation Results

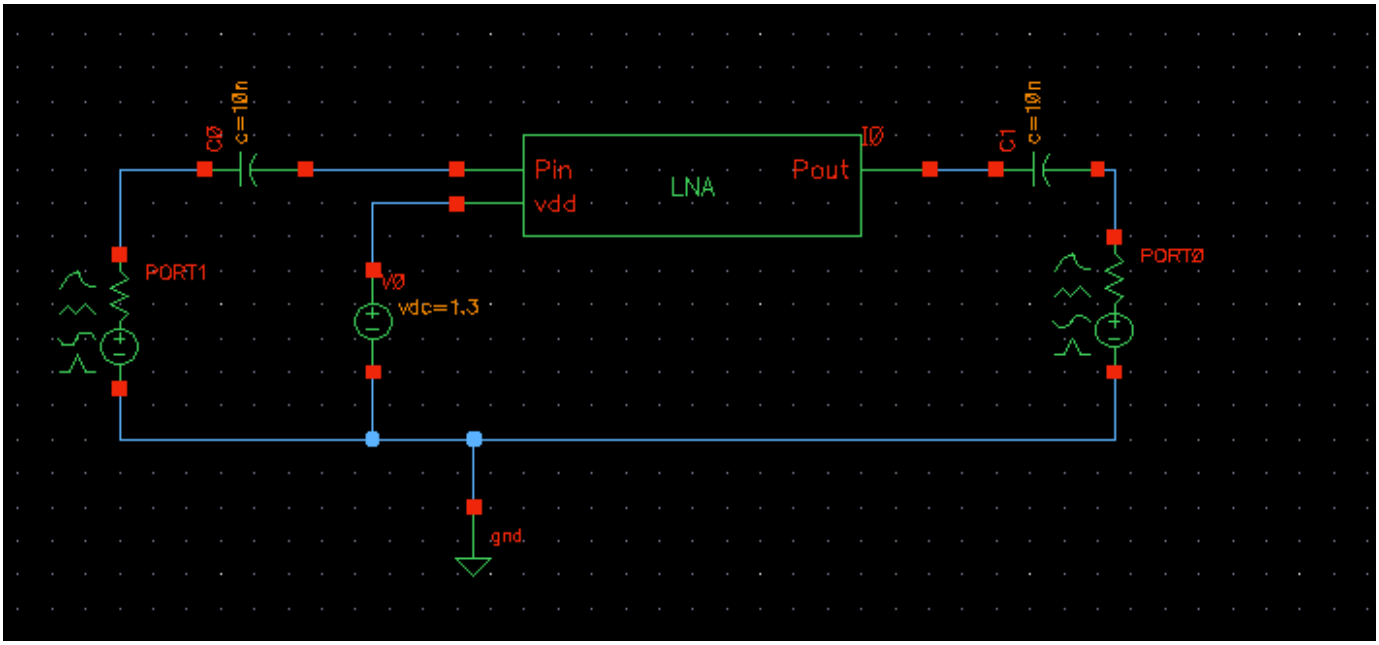


Figure 3.8 LNA test bench setup

Fig 3.8 is the test bench setup for the LNA. Here is the cadence Periodic Steady State Analysis (PSS), S- Parameter (SP) and Phase Noise (PNOISE) simulation results.

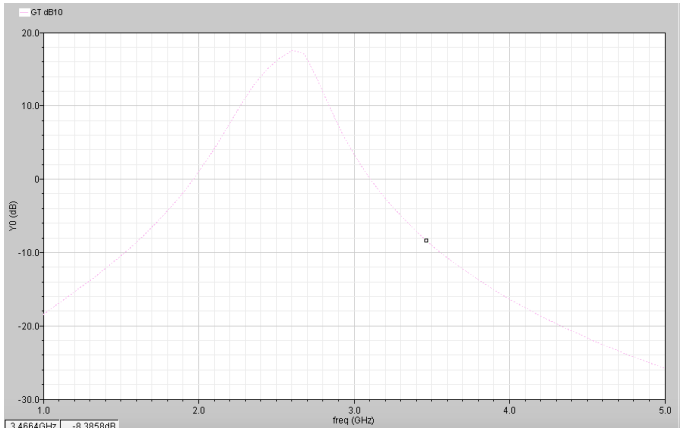
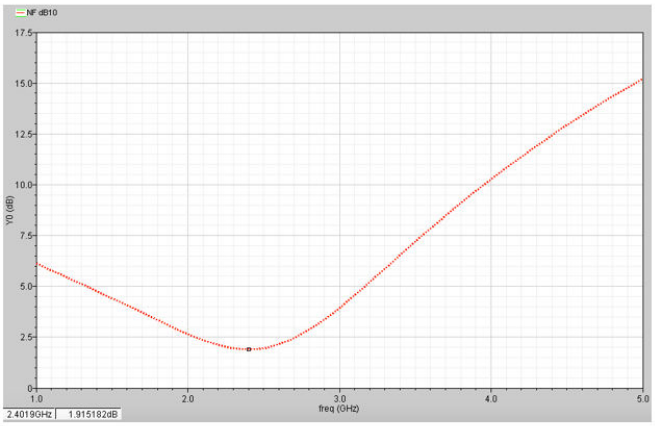


Figure 3.9: Gain plot

As seen in Fig 3.9, the gain is 20 dB at 2.4GHz. Based on the previous design procedure, the equation



(a)

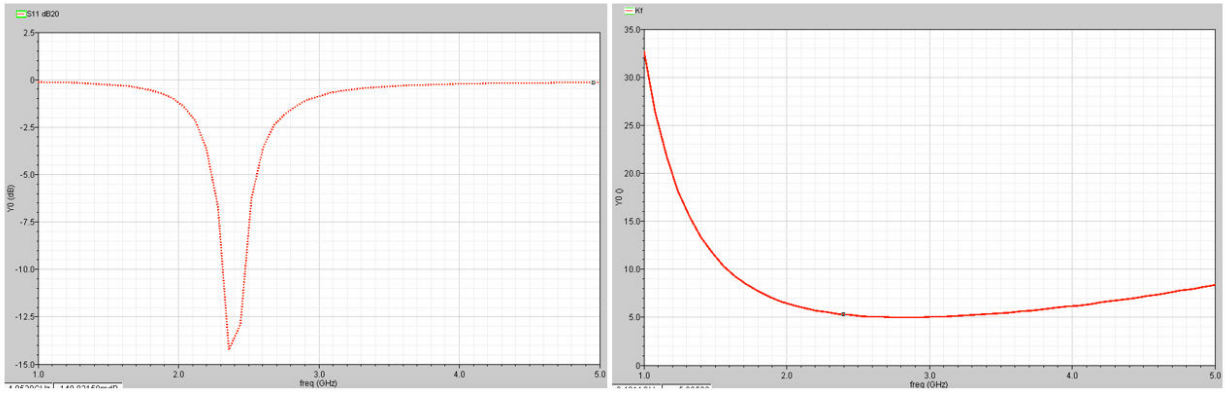
Device	Param	Noise Contribution	% Of Total
/PORT1	rn	2.05645e-16	63.77
/IO/L2	rn	9.45314e-17	29.31
/IO/M1	id	1.51644e-17	4.70
/PORT0	rn	2.87195e-18	0.89
/IO/L0	rn	1.39505e-18	0.43
/IO/L1	rn	1.21525e-18	0.38
/IO/R0	rn	9.36978e-19	0.29
/IO/M0	id	6.76366e-19	0.21
/IO/M2	id	4.63583e-20	0.01
/PORT1	ext_file_noise	0	0.00
/PORT0	ext_file_noise	0	0.00
/IO/R0	fn	0	0.00
/IO/M2	rd	0	0.00
/IO/M2	rs	0	0.00
/IO/M2	fn	0	0.00
/IO/M1	rd	0	0.00
/IO/M1	rs	0	0.00
/IO/M1	fn	0	0.00
/IO/M0	rd	0	0.00
/IO/M0	rs	0	0.00
/IO/M0	fn	0	0.00
/IO/L2	fn	0	0.00
/IO/L1	fn	0	0.00
/IO/L0	fn	0	0.00

Spot Noise Summary (in V^2/Hz) at 2.40 Hz Sorted By Noise Contributors
Total Summarized Noise = 3.22483e-16
No input referred noise available
The above noise summary info is for sp_noise data

(b)

Figure 3.10 (a) NF simulation (b) noise summary

As seen in Fig 3.10, the NF in (a) is around 1.9dB at 2.4 GHz, and (b) shows that the major contribution of the noise is from M1 and Ls. Also, the total power of the LNA is 2.2 mW. In this case, the simulation results consisted with the results too.



(a) (b)

Figure 3.11 (a) Kf simulation (b) S11 simulation

As seen in Fig. 3.11, the S11 at the 2.4G frequency in (a) is less than -10dB. Kf is larger than 1 for all frequencies from 1 to 5 GHz, so this circuit is totally stable, as seen in

(b). Based on the simulation, the LNA can be achieved for the low power as long as low noise.

Chapter 4: Mixer Design

4.1 Introduction to Mixers

An ideal mixer, as seen in Fig. 4.1, is usually translating one specific modulated carrier frequency into another specific carrier frequency. Mixers can be implemented either by time varying or nonlinear circuits [19]. A regular mixer is a three-port device, consisting of a local oscillator (LO), a radio frequency input (RF) and intermediate frequency output ports (IF) [20]. The LO port is driven by a local oscillator, which is a fixed amplitude large signal.

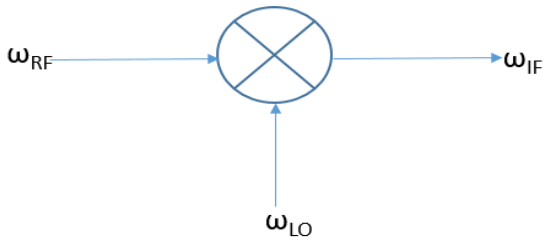


Figure 4.1 Ideal mixer

The multiplier circuit multiplies the two input signals A and B, and generates frequency product terms. Multiplication in the time domain is equivalent to the convolution in the frequency domain [6]. The following mathematical expression shows the generation of the sum and the difference between frequency products [7].

$$A = A_1 \cos \omega_1 t \tag{4.1}$$

$$B = A_2 \cos \omega_2 t \tag{4.2}$$

$$A \cdot B = \frac{A_1 A_2}{2} \cos(\omega_1 - \omega_2)t + \frac{A_1 A_2}{2} \cos(\omega_1 + \omega_2)t \tag{4.3}$$

4.2 Mixer Type

4.2.1. Up & Down Conversion Mixers

From the Eq. (4.3), we can see that the mixer produces two frequency components at the output, the sum ($\omega_{RF} + \omega_{LO}$) and the difference frequencies ($\omega_{RF} - \omega_{LO}$) as well as unwanted spurious frequencies. The main difference between the down and up conversions is dependent on their output signal frequencies. In the upconversion mixer, the output signal frequency is usually several GHz higher than the input signal, whereas in the downconversion mixers, the output signal frequency is usually several MHz lower.

4.2.2 Unbalanced Mixer

The unbalanced mixer, which is called a Square Law Mixer, is the simplest kind of mixer with the lowest noise figure. The single unbalanced mixer is shown in Fig. 4.2; the rule of mixing is to use the nonlinear square law characteristic of the MOS transistor. The conversion gain is independent of the biased current and can be expressed by Eq. (4.4) [21].

$$G_C = \frac{\mu C_{ox} W}{2L} V_{LO} \tag{4.4}$$

Another configuration of an unbalanced mixer is depicted in Fig.4.3, which is a dual gate unbalanced mixer configuration. The drain-source voltage V_{ds} of M1 can be modulated by the LO signal, and thus it can verify the transconductance of M1. In addition, to get maximize transconductance, M1 is biased between triode and saturation regions [19].

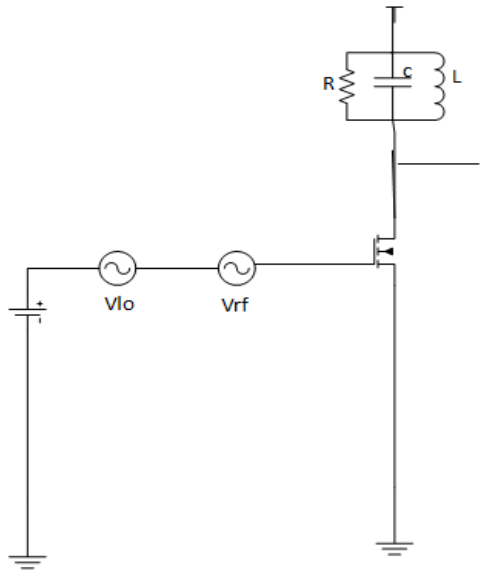


Figure 4.2 Single unbalanced mixer

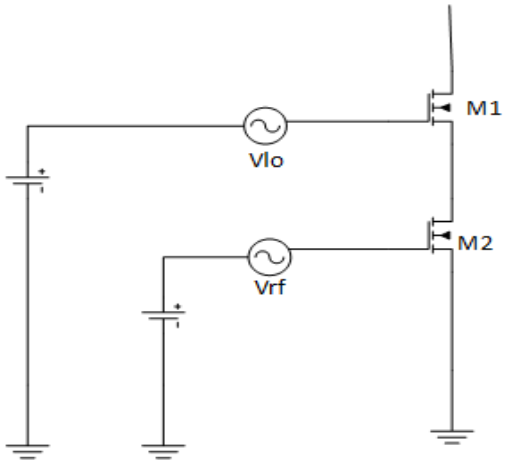


Figure 4.3 Dual gate unbalanced mixer

The disadvantage of this structure is that it has very poor port to port isolation. Feed through between different ports, (i.e. LO-to-RF, LO-to-IF, RF-to-IF ports) could degrade the Tx or Rx performance. Furthermore, noise at the IF can mix with the dc component of the LO signal, and thus increase the noise power at the IF output port. The best way to reduce this noise is by adding capacitive degeneration at the driver stage M1[19].

4.2.3 Balanced Mixer

This type of mixer consists of a single transconductance stage and a differential switching pair, as shown in Fig. 4.4. The function of the transconductance stage is to convert RF to current, and after which multiplication is made in the current domain. Specifically, the tail current is multiplied by the large LO signal. Thus the output is the sum and the difference of two frequency components. Because the output is differential, RF feedthrough can be cancelled out [24]. The circuit has a lower noise figure than the double balanced mixer due it having less MOS components. Source degeneration would have great benefits for linearity.

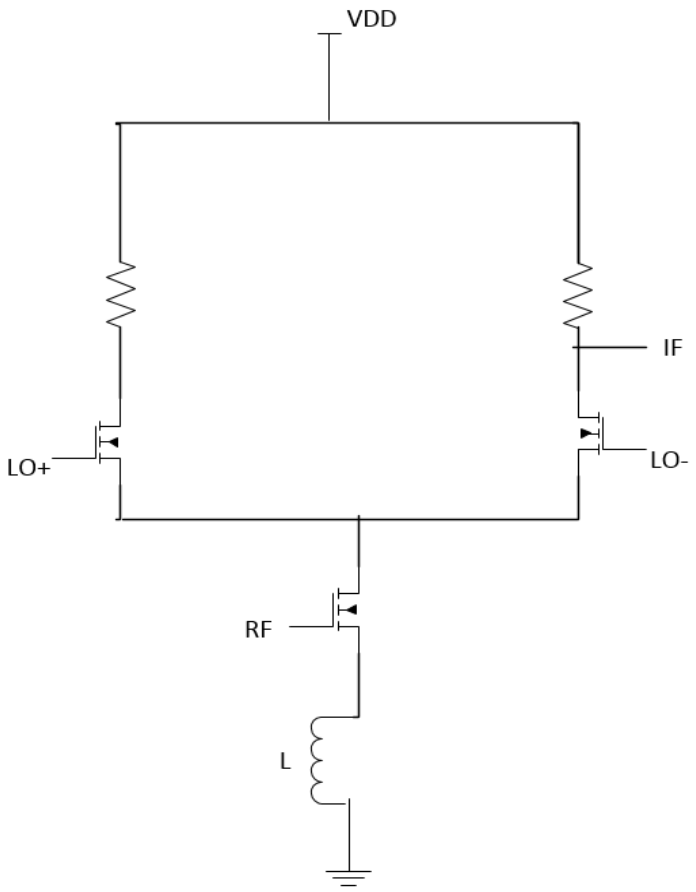


Figure 4.4 Single balanced mixer

A double balanced mixer, also known as a Gilbert mixer, is the most commonly used type of mixer. This mixer is suitable for both upconversion and downconversion. Based on the name, we know this mixer consists of a differential transconductance stage and a differential switching stage. Because of the fully differential structure, the cancellation and isolation of feedthrough between the LO-IF and RF-IF ports is greatly developed. However, due to mismatches in the differential structure, feedthrough may also exist. As mentioned before, a double balanced mixer will still have feedthrough of the RF-LO and LO-RF. The switching stage causes attenuation, but the transconductance stage provides a gain to compensate for this side effect [23]. A double balanced Gilbert mixer is shown in Fig. 4.5.

M1 and M2 form the transconductance stage, and M3 through M6 form the differential switching stage. The size of transistors M3 to M6 is much smaller than that of M1 and M2 which permits switching. The resistive load is suitable for good broadband operation at the cost of the voltage headroom. For a large output swing, the LC tank circuit could replace the resistive load, which should be tuned at the mixer output frequency. A side effect of replacement is that it limits the broadband operation of the mixer. When the output frequency is high, the tuned LC tank is used for upconversion. For downconversion mixers, it will be difficult, because the large inductor is difficult to implement on-chip.

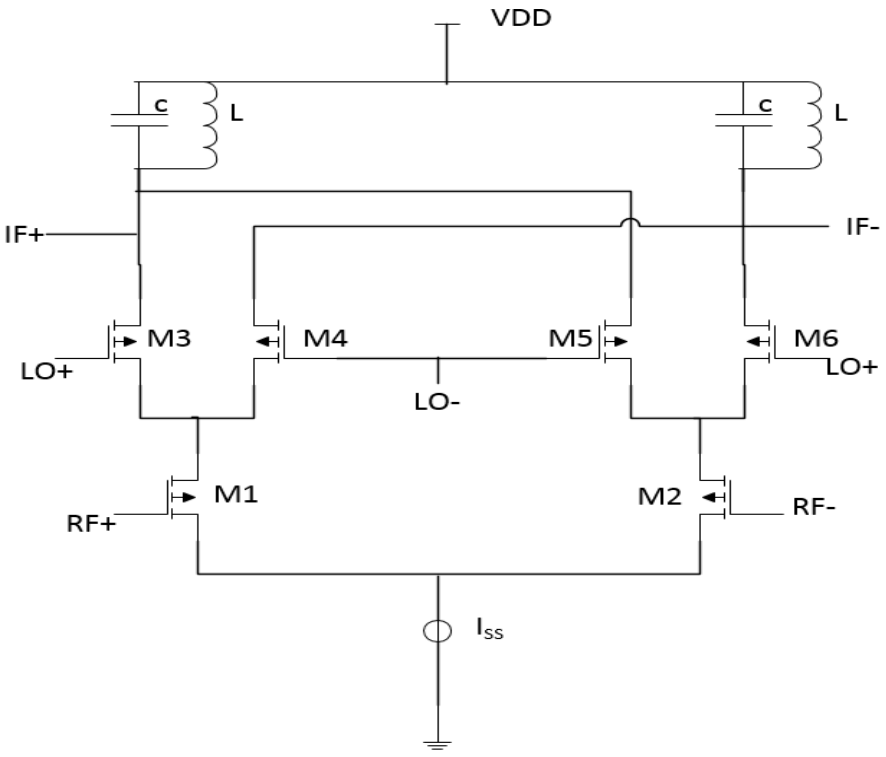


Figure 4.5 Double balanced Gilbert mixer

For improving the linearity of a double balanced mixer, source degeneration is the most common technique used today. Degeneration can be implemented in different forms,

such as a resistor, capacitor, or inductor. Usually, reactive source degeneration has a lower NF than resistive degeneration [24].

4.2.4 Passive Mixers

Passive mixers are also known as switching mixers, because these mixers do not consume dc power. These mixers usually have a conversion loss instead of a conversion gain. Passive mixers, like other mixers, also perform a multiplication between the RF signal and the LO signal, ideally represented by a square wave switching between +1 and -1, as seen in Eq. (4.6).

$$\cos(\omega_{RF}t) \cdot \cos(\omega_{LO}t) = \frac{1}{2}\cos(\omega_{RF}t + \omega_{LO}t) + \frac{1}{2}\cos(\omega_{RF}t - \omega_{LO}t) \qquad (4.6)$$

In order to reduce the conversion loss, the passive mixers should have minimum on-resistance for precise switches. For good isolation, the switch requires a maximum high resistance when off. One disadvantage for this type is that it requires a large LO drive signal to turn the MOS switches on/off. Passive mixers are opting for high frequency applications.

When the MOS is at the triode region, the transistor is on, and when off it is in the cut-off region. For accurate switching, ideally, the transistor should be biased at the threshold voltage (V_T) of the transistor. The lower the on resistance (R_{on}), the less the conversion loss. The mixers are biased with specific V_{DS} to attain optimum conversion loss as well as improved intermodulation distortion performance [19]. Fig. 4.6 shows a single balanced passive mixer. The transistors alternate on for the period of the positive and negative LO cycles.

Double balanced topology is preferred since it provides higher port-to-port isolation. Fig. 4.7 shows a passive double balanced mixer. The transconductance stage is the major non-linearity source. Since there is no transconductance stage in this type of the mixer, passive mixers provide excellent linearity. For improving port-to-port isolation and even order nonlinearity rejection, the transmission gate can replace a single NMOS transistor [24].

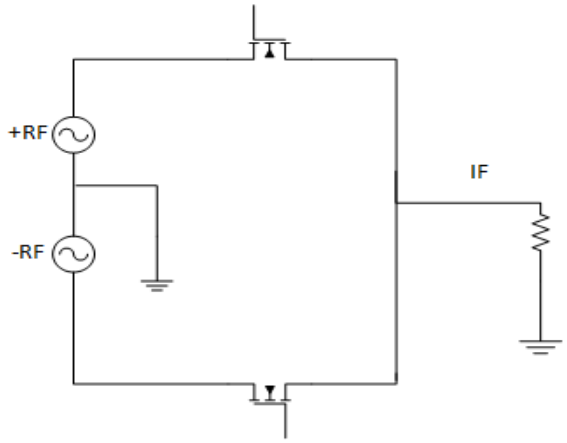


Figure 4.6 Single balanced passive mixer

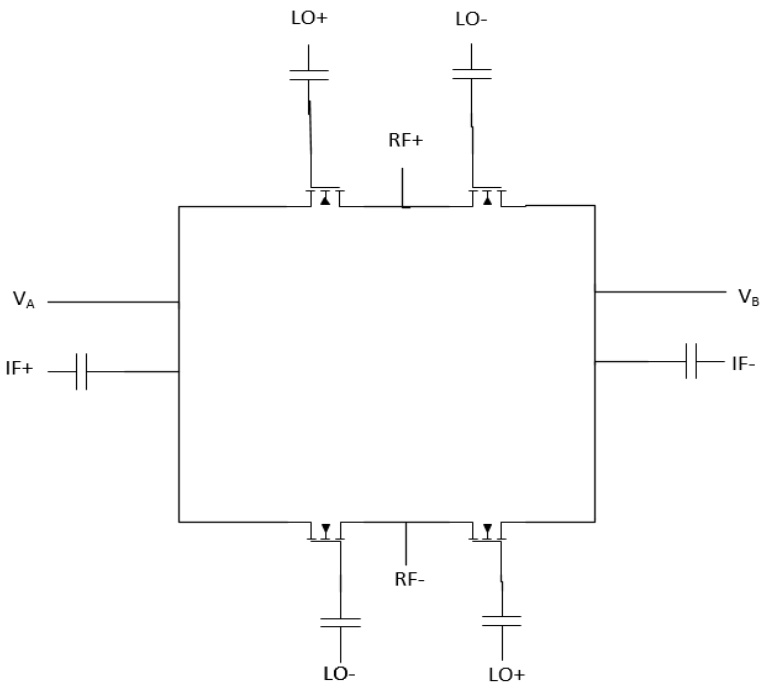


Figure 4.7 Double balanced passive mixer

To improve port-to-port isolation and even order nonlinearity rejection, a balanced transmission gate may be a better choice [8]. A transmission gate, also known as pass gate, consists of NMOS and PMOS transistors in parallel. A balanced transmission gate is depicted in Fig. 4.8 [9].

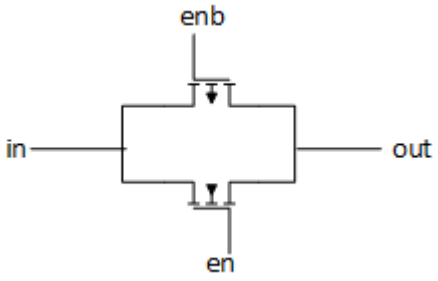


Figure 4.8 Balanced transmission gate switch

4.2.5 Active Mixers

The active mixers have two stages, a switching stage and a transconductance stage, and hence consume static power. Active mixers can also be either single ended or double ended. The most commonly used active mixer is the standard Gilbert cell mixer. The transconductance stage provides voltage gain at the cost of increasing NF and non-linearity. Therefore, researchers are coming up many ideas about improving the linearity of the transconductance stage. The switching stage performs current commutation. The topologies based on these techniques have their own advantages and disadvantages in terms of power consumption, area consumption, conversion gain and noise figure. When designing a mixer with high linearity, the tradeoff between conversion gain and NF is an important design consideration.

4.3 Mixer Design and Simulation Results

4.3.1 Gilbert Cell Mixer Design Procedure

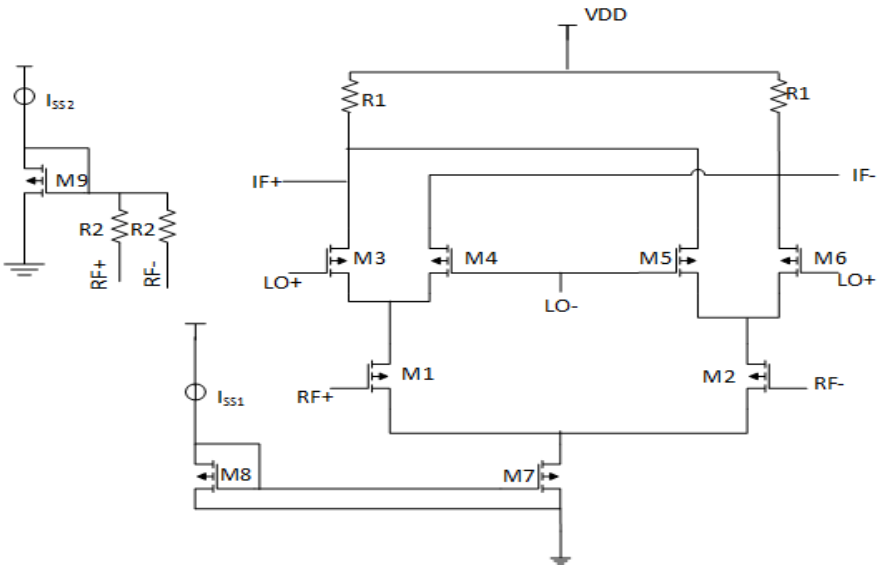


Figure 4.9 2.4 GHz Gilbert mixer schematic

Gilbert mixer provides good port-to-port isolation with some conversion gain [8]. The M1 and M2 are the input stages operating in the saturation region. The gain of this stage is proportional to gm, and

$$g_m = k_n' \frac{W}{L}(V_{GS} - V_T) \tag{4.7}$$

It is obvious from the above equation that a higher overdrive voltage provides a higher gain. Increasing the width W, while keeping the length L at minimum also results gain enhancement.

LO signals need to make the M3, M4, M5 and M6 transistors full switch, which means which transistor M3 M5 and M4 M6 are turning on alternately. In other words, LO signals must be kept at an appropriate large magnitude to ensure transistors switching accurately. Linearity is the greatly contributed decided by the trans-conductance stage.

The basic structure Gilbert cell mixer is often used in down conversion. Since transistors are operating at a saturation region, I can obtain higher gain and make the current less dependent on the changing voltage across the transistors. When I tried to bias the gain stage transistors, I needed consider whether I put enough margin of the head-room swing to make sure the transistors still working at the saturation region. The LO voltage level should be large enough to make the conversion gain insensitive to the LO amplitude. However, if the LO is too large, it will reduce the switching speed and increases the LO feed through. If two switching pair transistors conduct at the same time, noise increases. Therefore the overdrive voltage for switching pairs should be as close to zero as possible.

The transistors components values can be seen in table 4.1.

Table 4.1 Mixer components values

Parameter	Size (Unit)
M1, M2	W/L=10um/180nm
M3,M4,M5,M6	W/L=10um/180nm
M7	W/L=60um/180nm
M8	W/L=30um/180 nm
M9	W/L=12um/180nm
R1	5K
R2	3K

4.3.2 Simulation Results

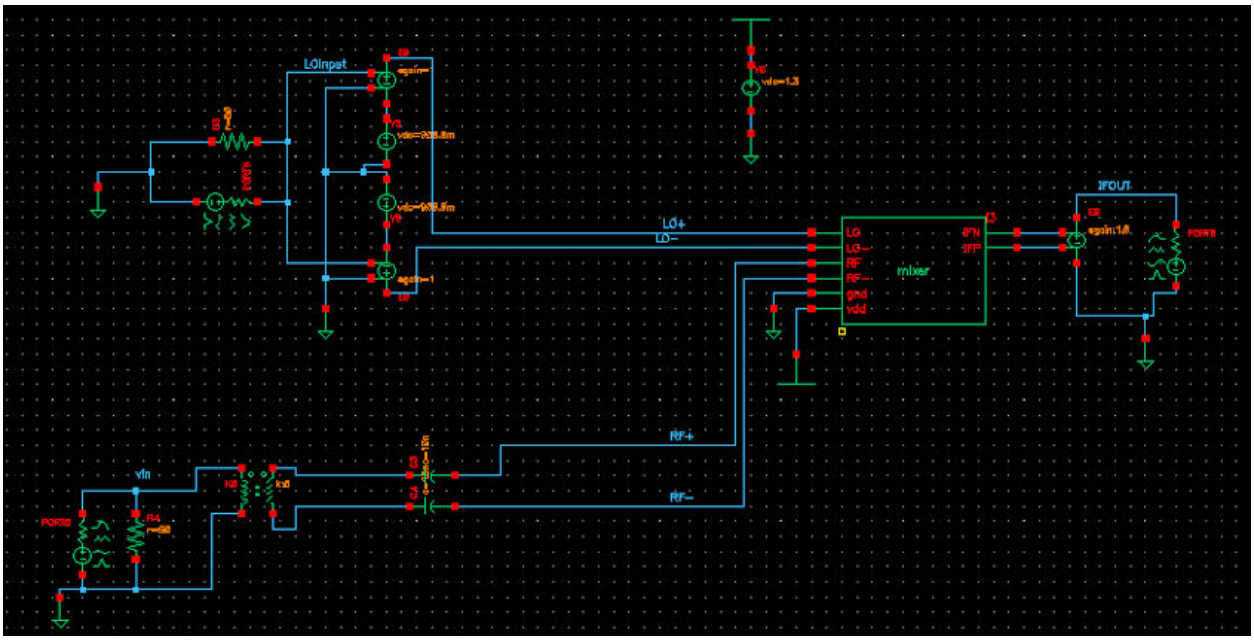


Figure 4.10 Mixer test bench setup

Fig. 4.10 is the mixer test bench, here it uses the cades tool PSS and PNOISE, PAC to run the simulations, the same tool used to run the LNA.

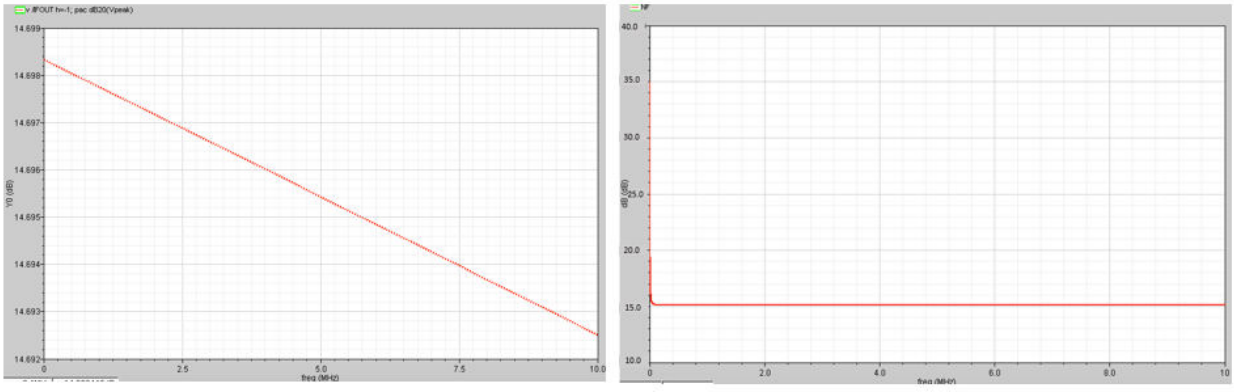


Figure 4.11 (a) Mixer conversion gain VS RF frequency (b) NF

As seen Fig. 4.11 (a), based on the PSS simulation, the conversion gain VS RF power at 2.4GHz is 14.6 dB, which is also consistent with the conversion gain $\frac{2}{\pi} g_m R_D$, and can totally

meet the design performance. Also, (b) NF is 15dB while the power consumption is 8.2mW. Based on the simulation results, which is also consisted with the design spec.

Chapter 5: VCO Design

5.1 Introduction to VCOs

Oscillators are a critical component in communication systems, and provide clean timing which means that low phase noise, periodic signals in digital circuits, and radio frequency (RF) circuits are the keys for the whole system [25]. Frequency translation purpose, an oscillator is usually referred to as the local oscillator (LO). For mixer purposes, the LO is used for frequency translation and channel selection.

The Fig. 5.1 is the typical front-end. The intermediate frequency (IF) can be downconvert to the lower frequency, or to upconvert the IF signal to a higher RF frequency. Since the IF frequency is usually fixed, the interest channel can be chosen by changing the LO frequency [16].

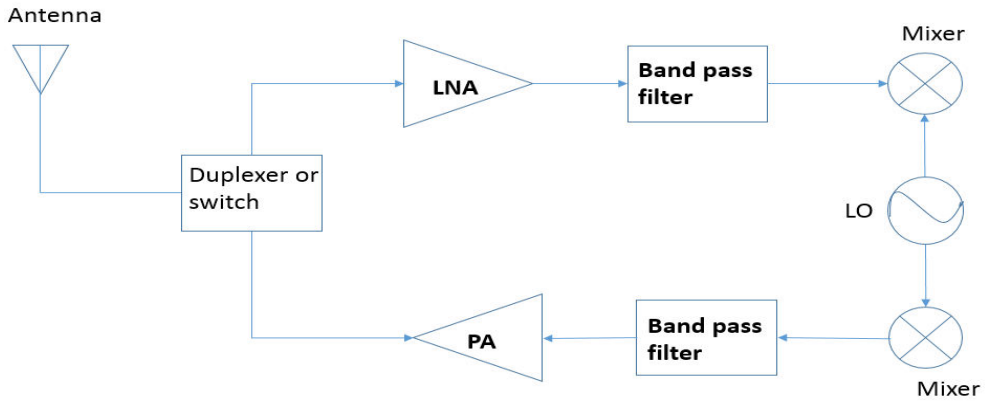


Figure 5.1 RF front-end transceiver chain

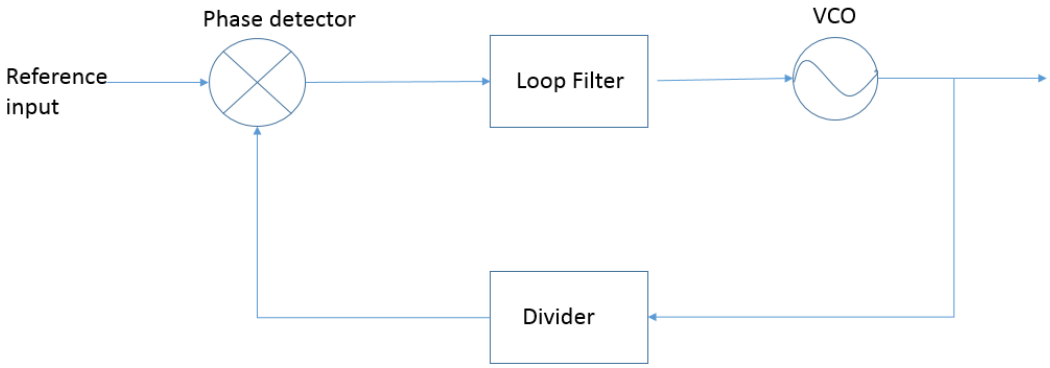


Figure 5.2 PLL block diagram

The LO can be implemented as a phase-locked loop (PLL), which contains a high-stability voltage-controlled oscillator (VCO). A typical PLL is made up of a phase detector, a low-pass loop filter, a VCO, and a frequency divider, as shown in Fig. 5.2. Because the PLL usually used for frequency translation and channel selection, the spectral purity of PLL can highly impacts the overall wireless system performance [26]. Within the loop bandwidth of

the PLL, the noise output characteristics are totally dependent on the reference signal, the phase detector, the loop filter, the divider, and the VCO. Outside the loop bandwidth, the output noise characteristics still depend on the VCO. Therefore, the output waveform of the PLL heavily depends on the VCO. The PLL spectral purity is usually referred to as the amount of phase noise [26].

Since there are increasing numbers of wireless users and a high demand for more efficient frequency usage, the frequency spectrum has become the most critical resource in wireless communications. Because wireless transceivers rely deeply on PLL, the spectral waveform of both the receiver and transmitter weighs all the number of available channels and users. In the receiver, the LO phase noise limits the system's ability to detect a weak signal when there is a strong signal in an adjacent channel. Therefore, the LO phase noise largely determines the sensitivity and dynamic range of the wireless receiver system. In the transmitter, due to the phase noise, the desired energy will be transmitted outside of the desired band. For these reasons, a clean output waveform (i.e. low phase noise) is required for the LO in a wireless transceiver [1]. There are several VCO parameters need to be simulated, such as oscillation frequency, power consumption, tuning range, and phase noise. Phase noise is the most critical spec among these parameters. Usually a resonator is commonly used for a VCO design. The resonator frequency is usually referred to as the oscillation frequency. A resonator is composed of an inductor and a capacitor, which is often referred to as an LC-tank. For frequency tuning, a voltage-controlled capacitor, such as a varactor, makes the variation of the oscillation frequency possible.

Phase noise is generally characterized in the frequency domain [29]. The output of an ideal oscillator may be expressed as

$$V_{out}(t)=V_0 \cos[\omega_0,t+\varphi_0] \tag{5.1}$$

where V_0 is the amplitude, ω_0 is the frequency, and φ_0 is the phase reference, all three values are all constants.

An ideal oscillator spectrum is shown in Fig. 5.3 (a), which consists of an impulse at ω_0. However, the output for the practical oscillator is [28]

$$V_{out}=V_0(t) \cdot f\,[\omega_0\, t+\varphi_0\,(t)] \tag{5.2}$$

where $V_0(t)$ and $\varphi_0(t)$ are functions of time, and f represents the steady-state output waveform of the oscillator. The output spectrum has power around ω_0 if the waveform, f, is not sinusoidal, as shown in Fig. 5.3 (b).

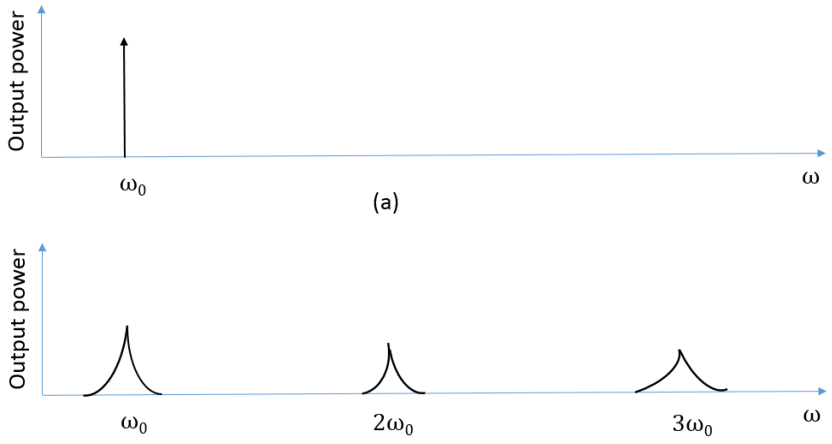


Figure 5.3 Spectral of (a) an ideal oscillator and (b) a real oscillator

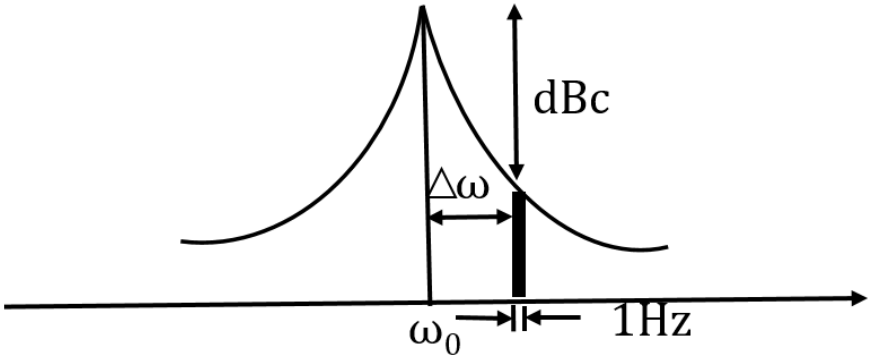


Figure 5.4 Phase noise in an oscillator output spectrum

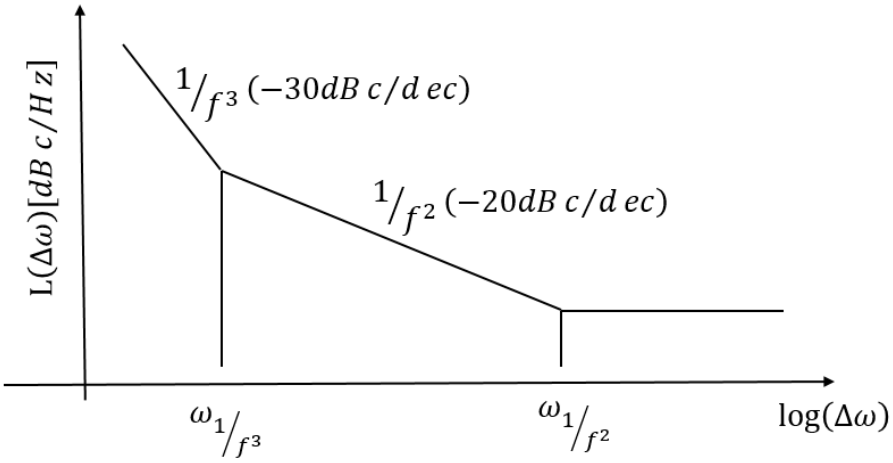


Figure 5.5 typical phase plot for a free running oscillator

Because of the random fluctuations happening around V_0 (t) and φ_0 (t), the spectrum will have sidebands, that are close to the oscillation frequency; we call these sidebands as "phase noise" [26], as shown in Fig. 5.4. Phase noise is quantified by a unit bandwidth (1Hz) at an offset Δω from the carrier, calculate the noise power in the band, and divide this result by the carrier power. The single-sided spectral noise density can be represented in units of dBc/Hz as

$$L(\Delta\omega) = 10 \cdot \log[\frac{noise\ power\ in\ a\ 1Hz\ bandwidth\ at\ frequency\ \omega_0+\Delta\omega}{carrier\ power}] \qquad (5.3)$$

Spectral density is usually specified at one or a few offset frequencies. For a free-running oscillator, when $L(\Delta\omega)$ is plotted on a logarithmic scale $\Delta\omega$, different regions have different slopes, as shown in Fig. 5.5. When far away from the offset frequencies, the noise floor is a flat. For small offset frequencies that are close to the resonant frequency, slopes of –30 dB/dec and –20 dB/dec can be observed [26].

In a wireless system, the Local Oscillator (LO) provides the carrier signal for both the receiver and the transmitter. If the LO has high phase noise, the output signal at the receiver and transmitter would be corrupted, which make it unusable [27].

In an ideal case, an impulse would convolve with a signal, both would be translated to a lower frequency without any signal distortion. However, the desired signal may be adjust to a large interferer in an adjacent channel in real life, as shown Fig. 5.6. In the receiver, when these desired signal and large interference signals are mixed with the LO output, the down-converted signal will result in overlapping spectra. The desired signal suffers because of the tail of the interferer, and this effect is called reciprocal mixing [28].

While a transmitter generates a signal at the specific frequency ω_1 with certain phase noise, a noiseless receiver would detect another frequency signal at frequency ω_2. The wanted signal will be corrupted because of the phase noise [1].

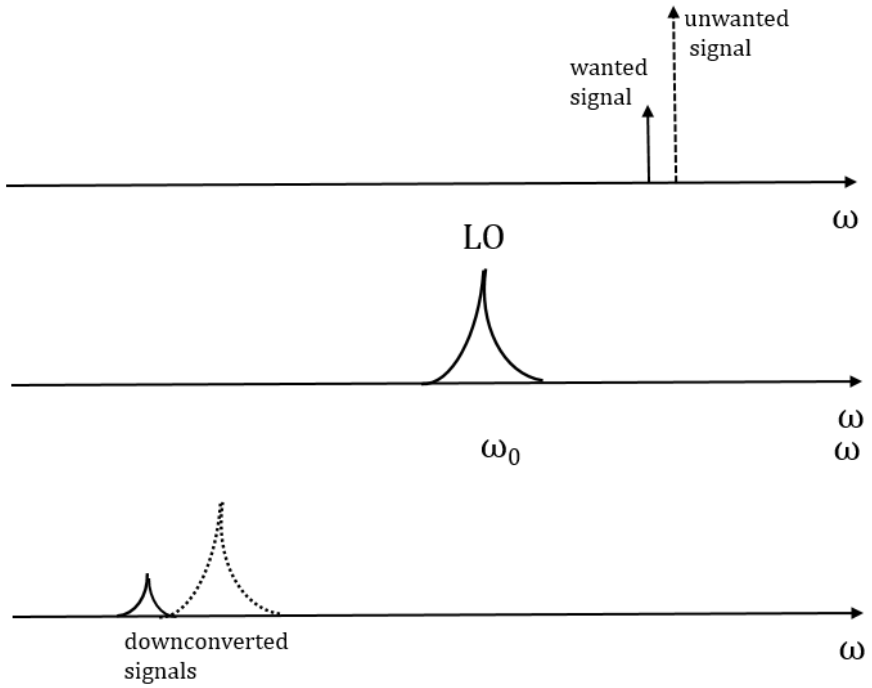


Figure 5.6: Effect of oscillator phase noise in a receiver

5.2 LC tank VCO topology

The first reason is still valid, the second reason is out of the date. In this section, oscillator topology is discussed. One-transistor oscillator topology and cross-coupled differential topology, which is also called the negative-gm oscillator are introduced. After several comparisons, a VCO should be implanted by a differential topology to obtain common-mode noise rejection. Here it will introduce all types of the cross-coupled differential topology.

One transistor VCO usually is a discrete device, for two reasons. One reason is mainly for minimizing noise; the other one is to reduce its cost. Since technology nodes are shrinking, the LC tank one transistor topology is not widely used.

5.2.1 One Transistor VCO Topology

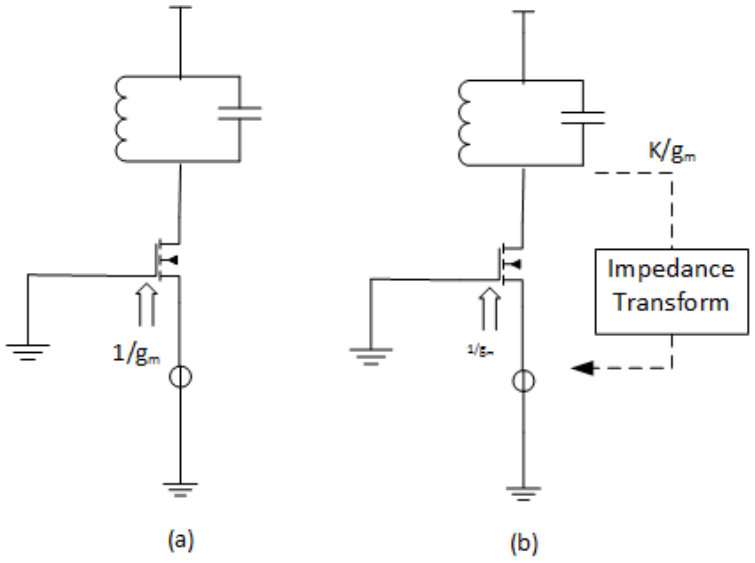


Figure 5.7 (a) Direct feedback from drain to source (b) feedback with an impedance transformer

In Fig. 5.7, LC oscillators with one transistor are shown, the configuration of Fig. 5.7 (a) has direct feedback from the drain to the source. In contrast, Fig. 5.7(b) shows the source impedance transformed to a higher value [8]. Capacitive or inductive dividers can be used for impedance transformation, as shown in Fig. 5.8. A colpitts oscillator uses a capacitive divider, and a Hartley oscillator uses an inductive divider. The equivalent resistance in the tank can be expressed as $(1+C_1/C_2)^2/g_m$ in Fig. 5.8 (a) and $(1+L_2/L_1)^2/gm$ in Fig. 5.8 (b), this impedance transformation enhances the loaded resonator Q. The colpitts oscillator contains one inductor, while a Hartley oscillator contains two, so the colpitts oscillator is more commonly used [8].

The resonance frequency can be written as $\omega r = 1/ (L_{eq} \cdot C_{eq})^{1/2}$, (5.3)

where L_{eq} is the equivalent inductance and C_{eq} is the equivalent capacitance in the parallel tanks of Fig. 5.8. The tank capacitance has some uncertainties due to inductor parasitics,

which means it hard to control the VCO oscillation frequency by adding a variable capacitor.

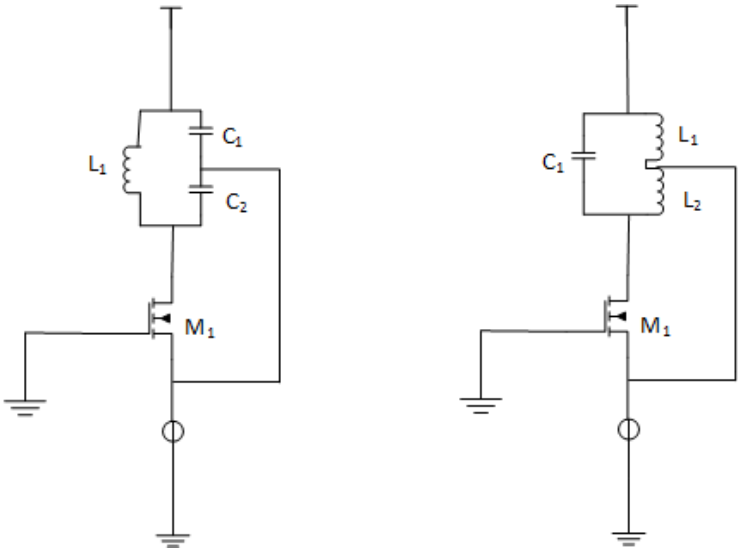


Figure 5.8 (a) Colpitts (b) Hartley Oscillator

Since VCO has only a transistor M1, the transistor design should be optimized in terms of its size and its biasing. There are two ways to reduce the gate and the drain thermal noise, one way is increasing device size, and the other one is decreasing the bias current [8]. However, there are always tradeoffs. Larger sizes usually have more parasitic capacitance, and the smaller current usually reduce the voltage swing.

These topologies have several disadvantages. One issue is that the ratio of the capacitors and inductors needs to be large, so that parasitics would have less effect on the Q. A second problem is that these topologies are single-ended outputs, which is not suitable for the wireless transceiver systems. And a third drawback is that the phase noise can be greatly affected by the common-mode noise from the supply and the substrate when the VCO is integrated in one single chip. Therefore, the differential oscillator is widely used in current industrial practice.

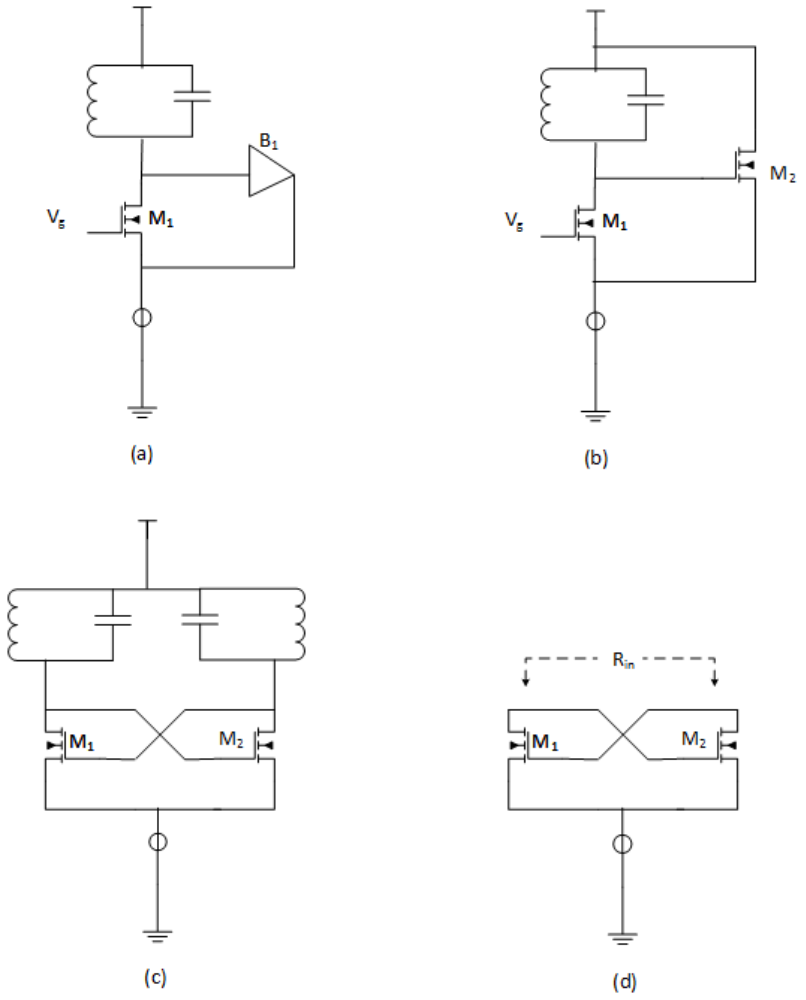


Figure 5.9: (a) A one-transistor oscillator with an active buffer (b) oscillator with a source follower (c) cross-coupled differential topology (d) Negative resistance of cross-coupled pair

Colpitts and Hartley oscillators concluded a passive divider network that is transforms the impedance to a higher value. Fig. 5.9 (a) represents a high impedance active buffer (B1) in a passive network. Fig. 5.9(b) is the same as Fig. 5.9(a) except that it shows a source follower instead of a buffer. Fig. 5.9(c) represents the cross-coupled differential oscillator configuration, are also called a negative-gm oscillator [28]. The configuration referred to in Fig. 5.9(c) can operate differentially more LC-resonators. Fig.

5.9 (d) shows negative resistance at the drain of M1 and M2, which is expressed by [9]

$$R_{in} = -2/g_m \tag{5.5}$$

Thus, if R_{in} is less than or equal to the equivalent parallel resistance of the tank, the circuit oscillates.

5.2.2 NMOS or PMOS Core Cross-Coupled Differential Topology

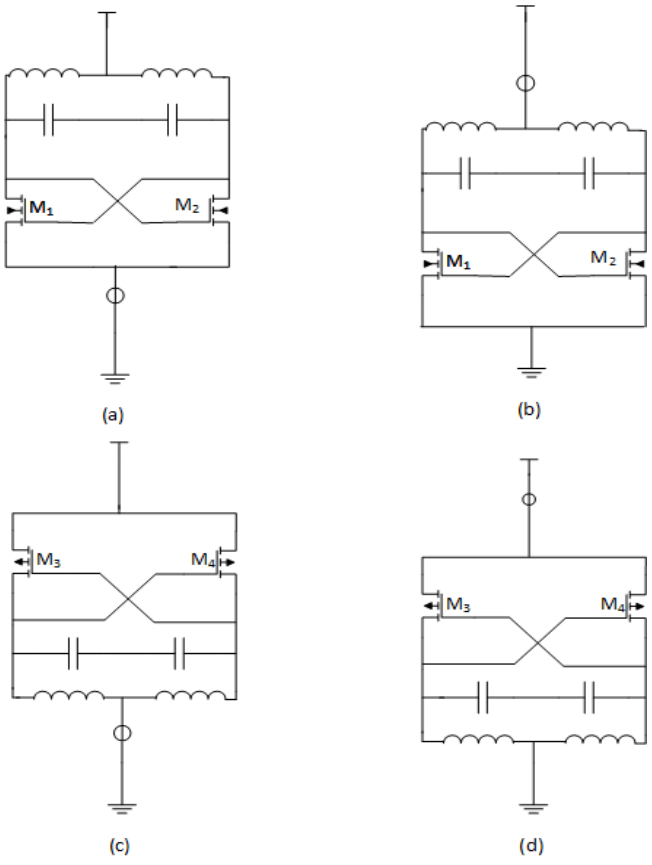


Figure 5.10 cross-coupled differential topology (a) NMOS pair and a tail current at the source (b) NMOS pair and tail current at the drain (c) PMOS pair and a tail current at the drain (d)PMOS pair and a tail current at the source

Usually, there are four versions of a cross-coupled differential configuration. Fig. 5.10 (a) and (b) are the differential oscillators with a cross-coupled NMOS pair and a tail current. Fig. 5.10 (c) and (d) are the differential oscillators with a cross-coupled PMOS pair and a tail current. A tail current can be either at the source or at the drain terminal.

PMOS cross-coupled pairs have been widely used in the VCO design because they have low noise relative to NMOS pairs [25]. The reason PMOS have less hot carrier effect is that they have less of the hot carrier effect [28]. In a CMOS process, hot electron noise is significant. Additionally, when a PMOS has same dimensions as a NMOS, PMOS flicker noise is 10 times smaller than that of the NMOS. PMOS transistors have a lower mobility than NMOS transistors. As a result, the flicker noise of a PMOS would also be lower. For these reasons, I designed a VCO using a cross-coupled PMOS pair [23].

5. 3 VCO Design and Simulation Results

5.3.1 VCO Design

The VCO schematic as shown in Fig. 5.10 was chosen for several reasons. The reasons are discussed in part 5.2. The oscillation amplitude of this structure is determined by the PMOS pair, which would also be beneficial to the low phase noise. The cross-coupled MOS pair would get a negative resistance as shown in Fig. 5.11. The negative resistance cancels the LC element's parasitic resistance [25].

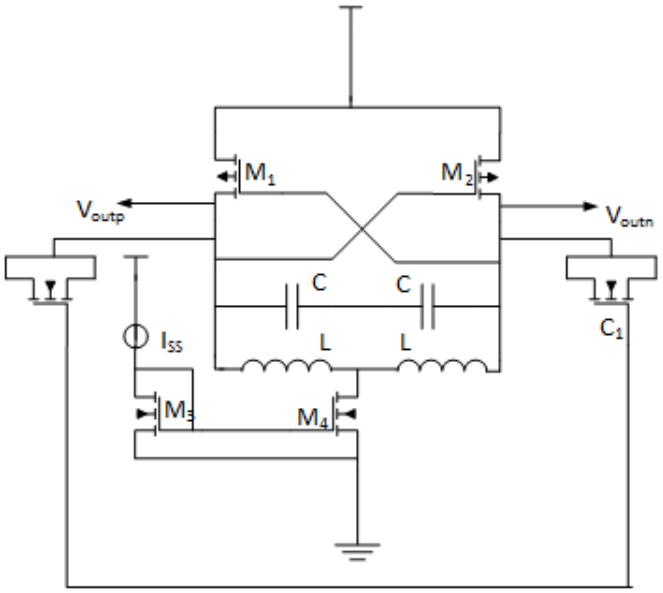


Figure 5.11 2.4 GHz VCO schematic

Table 5.1 VCO components values

Parameters	Sizes (units)
M1, M2	W/L=10um/130nm
M3	W/L=1um/130nm
M4	W/L=4um/130nm
C	700fF
L	6nH
C1	W/L=10um/130nm

A 2.4 GHz voltage controlled oscillator designed in 0.13µ CMOS process is presented. The simulation results have shown that the tuning range was from GHz 2.3- 2.5 GHz, output swing was 1.3 V while consuming 3.25mW of power.

5.3.2 Simulation Results

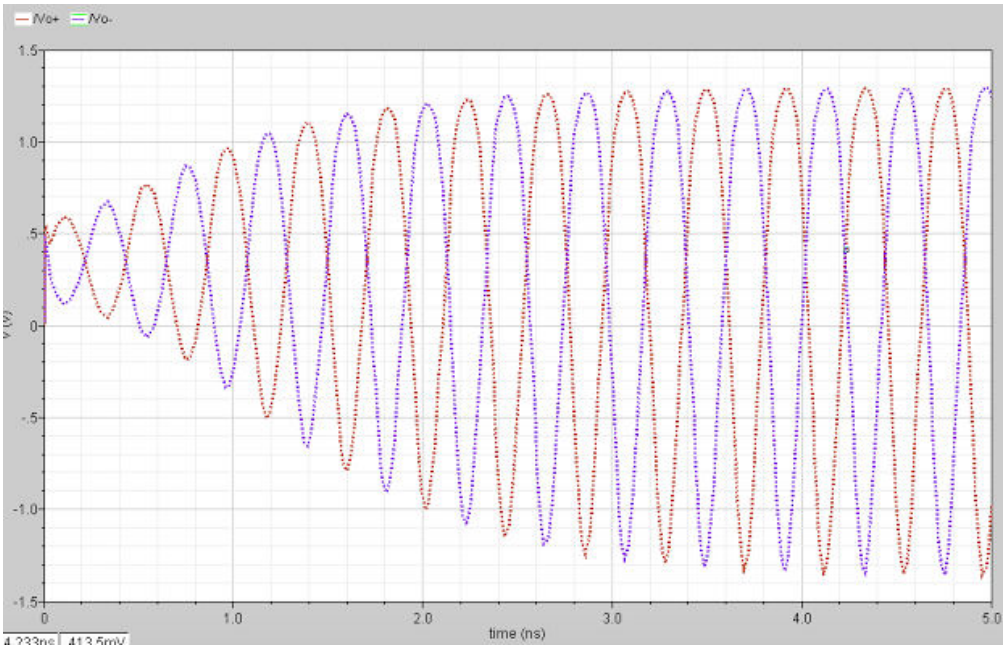


Figure 5.12 VCO (a) oscillation frequency

As we can see from the Fig 5.12, the oscillation frequency is around 2.4GHz. The simulation result is consisted with the (5.4). The L and C can be seen on the Fig 5.1.

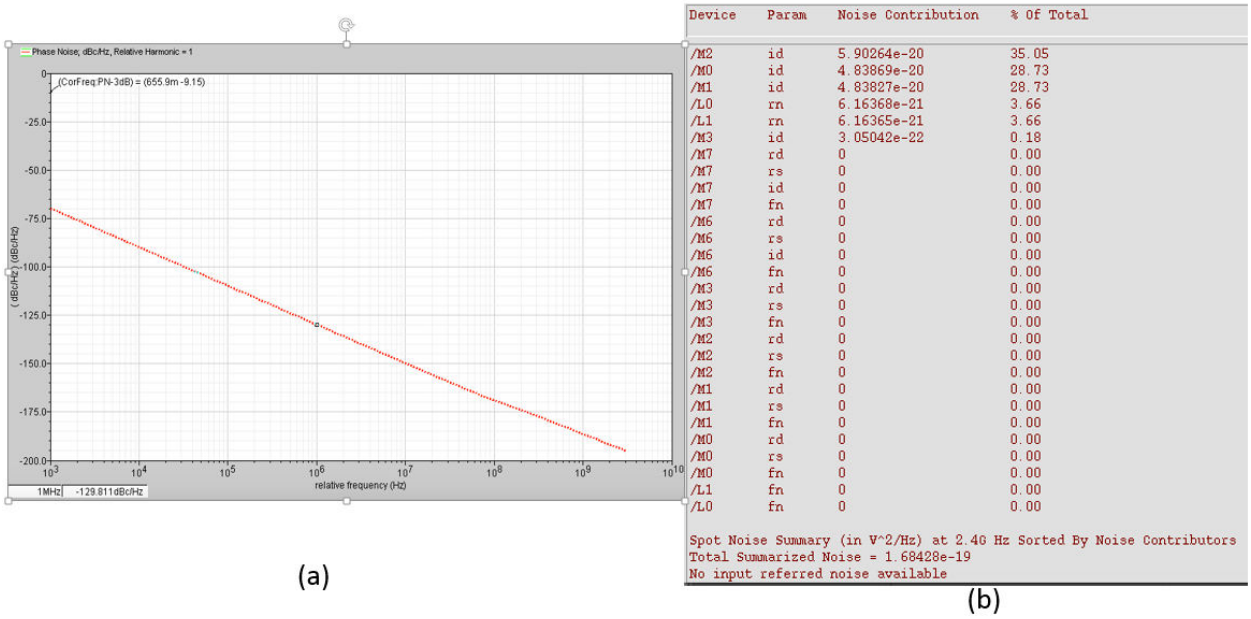


Figure 5. 13VCO (a) phase noise (b) noise summary

As we can see Fig. 5.13 (a) phase noise at 1MHz offset frequency is 129dBc/ Hz, the major noise source is the current source and the two differential pair which can see from (b).

When designing a VCO, a lot of trade-offs need to be considered. The first trade-off is between tuning range and harmonic distortion. Usually, the bigger the MOS capacitor, the wider the tuning range. However, bigger MOS capacitors usually cause non-linearity and harmonic distortion.

Chapter 6: Conclusion and Future Works

6.1 Conclusion

In this thesis, the design includes LNAs, mixers and VCOs that build a low-power, compact, reliable and fully-integrated 2.4GHz heterodyne receiver. I discuss such issues, as design trade-offs, input matching, output matching, and tuning techniques.

Performance analyses with simulation results are presented at chapters 3, 4, 5. In Table 6.1, I combine all my work simulation results that achieve all the design requirements. All the designs include bias circuits.

Table 6.1 Designed receiver simulation results

	Noise Figure	Gain	Power
LNA	1.9dB	20dB	2.21mW
mixer	15dB	14.6dB	8.2mW
VCO	Oscillation frequency	Phase noise	power
	2.4GhZ	-128dBc/Hz	3.25mW

The LNA was optimized for high gain and low NF, and was designed by combining the merits of CSLNA and the CGLNA. The LNA possesses a great trade-off between NF and power consumption. Mixers were designed to achieve better linearity and low power consumption. The VCO used the LC tank instead of the ring oscillator, because of the low phase noise and low power issue. The design simulation fully achieved the system performance specification.

6.2 Future Works

A heterodyne receiver usually has many blocks, such as filters, ADCs, and frequency synthesizers. In order to build a complete receiver, these blocks are not enough, and more

blockers should be done. Also, more work can be done to improve the performance, such as better LNA topology. I can cover and explore more deeply on this topic if time permitted. I believe power consumption is very important for healthcare applications. In order to achieve an ultra- low power system, system and circuit design both need improvements.

Secondly, since the technology nodes are becoming smaller and smaller, technology creates more challenges for analog/RF designers. For low supply voltage, it is not easy to design a very linear mixer. Besides, accurate device modeling is needed, due to the leakage and process variations.

REFERENCES

[1] Stults BM, "Preventive Health Care for the Elderly," *Western Journal of Medicine*, vol.141, pp 832-845,1984.

[2] Hatem Trabelsi, et al.,"A 3–5 GHz FSK-UWB transmitter for Wireless Personal Healthcare applications", *International Journal of Electronics and Communications*, pp 262-273, 2015

[3]Jia-Hua Hong, et al., "A Wireless ECG Acquisition and Classification System for Body Sensor Networks",*35th Annual International Conference of the IEEE EMBS*, Osaka, Japan, 3 - 7 July, pp 5183-5186, 2013

[3] Young B. Choi, "Systems recent wireless LAN management technologies: trends and outstanding issues",*331 Issues in Information*, Volume VI, No. 2,, http://iacis.org/iis/2005/Choi_Park_Fernandez_Kim.pdf ,2005

[4] J. M. Rabaey, et al., "PicoRadios for wireless sensor networks: The next challenge in ultra-low-power design," *IEEE ISSCC Dig. Tech. Papers*, 2002, pp 200–201.

[5]Horlin, F,"*The Generic Transmission scheme for Fourth Generation Wireless Systems*," Retrieved November 19, from [online http://www.imec.be/wireless/sdr/publications/WWRF_2004_generic.pdf],2004.

[6] Frenzel, Louis E., *Principles of Electronics Communication Systems*, 3rd edition, McGraw Hill, 2008.

[7] Kolimbiris, Haorld, *Digital Communications Systems*, Prentice Hall, 2000.

[8] B. Razavi, *RF Microelectronics*, Prentice-Hall, 1998.

[9]Thomas Lee, *The Design of CMOS RF Integrated Circuits*, 2011

[10] Bailey, D., Wireless Access Report: Security issues dog hotspots. *Network Week*, 26, Aug 2004.

[11] Kai Chang, *RF and Microwave Wireless Systems*, JOHN WILEY & SONS, INC, 2000.

[12] Wai-Kai Chen, *The VLSI Handbook*, by CRC press, 2000.

[13] Tran Thi Thu Nga, PhD thesis, Ultra low-power low-noise amplifier designs for 2.4 GHz ISM band applications, [online:http://www3.ntu.edu.sg/home/eccboon/pub/Thesis_ThuNga.pdf], 2012.

[14] J. A. M. Jarvinen, et al., " 2.4 GHz receiver for sensor applications", *IEEE Journal of Solid-State Circuits*, vol. 40, no. 07, p. 1426 - 1433, Jul. 2005.

[15] E. P. Hong,et al., "A Low Power Folded RF Front-end with Low Flicker Noise for Direct Conversion Receiver", *IEEE Conference on Electron Devices and Solid-State Circuits*, pp 453-456, 2007.

[16] I. Nam, et al., " A 2.4-GHz Low-Power Low-IF Receiver and Direct-Conversion Transmitter in 0.18um CMOS for IEEE 802.15.4 WPAN Applications", *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 4, p. 682-689, 2007.

[17] N. Won et al., " Direct-conversion RF receiver design", *IEEE Transactions on Communications*, vol. 49, no. 3, p. 518-529, 2001.

[18]Behzad Razavi, "RF Transmitter Architectures and Circuits", pp.197-204, *IEEE Custom Integrated Circuits Conference*, 1999.

[19] Ghulam Mehdi, MS thesis "Highly Linear Mixer for On-Chip RF Test in 130nm CMOS", [online: http://www.diva-portal.org/smash/get/diva2:22903/FULLTEXT01.pdf], 2007.

[20] Keng Leong Fong, et al., "Monolithic RF Active Mixer Design", *IEEE Transactions on Circuits and Systems*, vol.46, no.3, pp.231-239, Mar. 1999.

[21]Jacob Phil, et al., "Direct Downconversion with Switching CMOS Mixer", *IEEE ISCAS*, pp.117-120, 2001.

[22] Payam Heydari, "An Analysis High Frequency Noise in RF Active CMOS Mixers", *Analog Integr Circ Sig Process*, vol.48, pp.199-209, 2006.

[23] Hooman Darabi, et al., "Noise in RF-CMOS Mixers: A Simple Physical Model", *IEEE Transactions on Solid State Circuits*, vol.35, no.1, pp.15-25, Jan 2000.

[24]Manolis T. Terrovitis,et al., "Intermodulation Distortion in Current Commutating CMOS Mixers", *IEEE Journal of Solid State Circuits*, vol.35, no.10, pp.1461-1473, Oct. 2000.

[25] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE Journal of Solid State Circuits*, vol. 31, pp. 331-343, Mar. 1996.

[26] A. Hajimiri,et al., "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 179-194, Feb. 1998.

[27] B. De Muer,et al., "A 1.8GHz highly-tunable low phase-noise CMOS VCO," *IEEE Proc. Custom Integrated Circuits Conf*erence, pp. 585-588, 2000.

[28] Sangwoong Yoon,"*LC-tank CMOS Voltage-Controlled Oscillators using High Quality Inductors Embedded in Advanced Packaging Technologies*", PhD thesis, [online: https://smartech.gatech.edu/bitstream/handle/1853/4887/yoon_sangwoong_200412_phd.pdf], 2004.