High-Frequency CML Clock Dividers in 0.13-μm CMOS Operating Up to 38 GHz

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***Abstract*—The analysis and design of two novel high-speed CMOS clock dividers is discussed. The realizations of these circuits in a 0.13-μm CMOS process show a significant improvement in high-frequency operation compared to a conventional D flip-flop-based divider. Measured sensitivity curves of these dividers give maximum frequency of operation ranging from 20 to 38 GHz with power consumption of 12 mW from a 1.8-V supply voltage.**

***Index Terms*—Broadband communication, CMOS analog integrated circuits, CMOS integrated circuits, frequency conversion, high-speed integrated circuits.**

I. Introduction

HIGH-SPEED frequency dividers are one of the key elements in integrated circuits designed for broadband communication systems. Indeed, the frequency dividers used to divide down the internal high-speed clock in such circuits often determine the maximum operating speed of the overall circuit. In practice, GaAs and bipolar technologies [1]–[3] have been employed to make such high-speed circuits. With the aggressive scaling of MOS transistors, it is now possible to implement these circuits in CMOS technology. High-speed frequency dividers operating at frequencies greater than 20 GHz have been reported in [4]–[7].

In this paper, we present two novel clock divider circuits and compare their performance to a conventional D flip-flop (DFF)-based divider.

This paper is organized as follows. In Section II, we give a general discussion of the behavior of high-speed clock dividers based on a D flip-flop and then analyze the operation and design of the two new frequency dividers. In Section III, circuit implementation and measurement results are shown. Conclusions are given in Section IV.

II. High-Speed CML Frequency Dividers

A conventional clock divider often used in broadband communication systems is shown in Fig. 1. This circuit is simply a D flip-flop, realized using CML blocks, with feedback applied from its differential outputs *OUTP/N* back to its inputs. The inductors are used to reduce the rise and fall times, hence

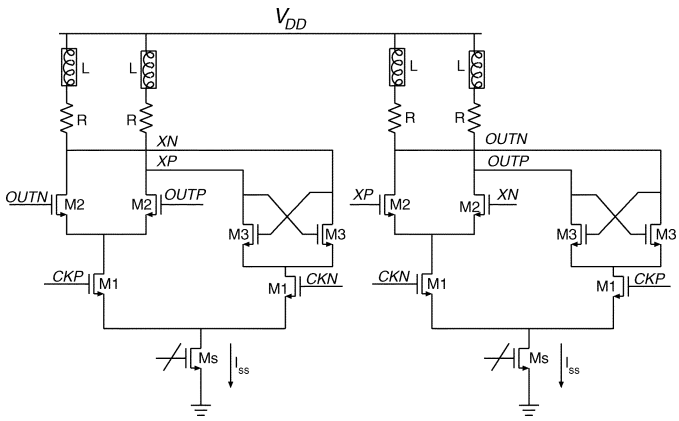

Fig. 1. DFF-based CMOS clock divider.

enhance the high-frequency operation. Conceptually, the operation of such a divider seems simple: when the differential clock signal *CKP/N* makes a high-to-low transition, the output signal should change state. Although it is convenient to analyze a clock divider based on standard digital circuit behavior, in reality, such circuits used at high frequencies behave more like complex dynamic systems. As discussed in [9], a clock divider can be accurately characterized by its sensitivity curve. The simulated sensitivity curve corresponding to the Fig. 1 circuit realized in the TSMC 0.13-μm CMOS process is shown in curve (*i*) of Fig. 2. From the sensitivity curve, it can be seen that the DFF-based frequency divider exhibits a large frequency range and can operate down to a very low input frequency. It can also be observed that this divider self-oscillates—that is, if the clock amplitude is set to zero, the output will oscillate at frequency $f_{\rm so} = 9.1$ GHz. This is a desirable characteristic since the divider will operate correctly with very low clock amplitude at input frequencies near $2f_{\rm so}$. The problem with this divider is that the output nodes *OUTP/N* see a large output capacitance from its internal feedback; outside loading adds even more capacitance. This limits the maximum frequency of operation. The cross-coupled transistor pair used in the latch is one of the largest contributors to the output capacitance. The function of these transistors is to provide negative resistance (it is this negative resistance that allows self-oscillation to occur) and to maintain a particular logic state at the appropriate clock phase. We will show that replacing the cross-coupled latch structure with well-characterized delay stages, realized by CML buffers, reduces the capacitive loading at each node while still allowing self-oscillation and locking behavior, thereby enabling it to operate at significantly higher frequencies.

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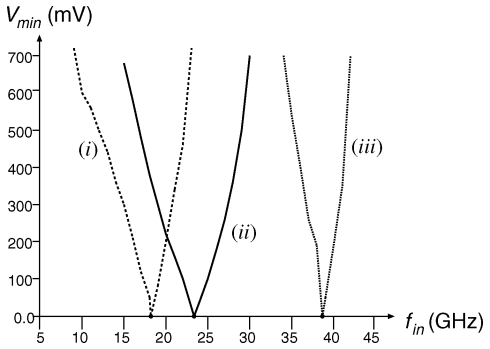

Fig. 2. Simulated sensitivity curves for: (*i*) Fig. 1, (*ii*) Fig. 4, and (*iii*) Fig. 5.

A. New Circuits for High-Speed Clock Dividers

In this section, two new high-speed frequency divider circuits are discussed. The first circuit is derived as variant of the well-known regenerative frequency divider [11], based on a mixer with feedback. The second circuit is based on injection locking.

1) Modified Regenerative Divider: The concept of a regenerative frequency divider using a mixer with feedback to perform clock division has been described in [10]–[12]. A block diagram of this divider is shown in Fig. 3(a). Given inputs with frequencies $f_{\rm in}$ and f_{out}, the mixer generates an output signal with frequency components $f_{\rm in} - f_{\rm out}$ and $f_{\rm in} + f_{\rm out}$. If the cut-off frequency of the filter is such that frequency $f_{\rm in} + f_{out}$ is filtered out then the frequency component which persists in the loop is one which satisfies the relation $f_{\rm out} = f_{\rm in} - f_{\rm out}$; i.e., $f_{\rm out} = f_{\rm in}/2$.

A CMOS realization of this divider is shown in Fig. 3(b), where the mixer used is a standard Gilbert cell and two CML buffers function as both low-pass filter and amplifier. It can be observed that this circuit does not self-oscillate—that is, if the input clock amplitude is set to zero, the divider output will have zero amplitude. This is due to the fact that the loop gain is nearly zero in the absence of the clock input signal since the signal *OUTP/N* is fed back to both mixer inputs (transistors M_2 and M_3) with opposite phases. A simple modification of this circuit can be made by feeding back intermediate outputs *YP/N* to transistors M_3 as shown in Fig. 4. Using a loop analysis similar to that given in [8], it can be shown that the difference in delays between *XP/N* and *YP/N* for the circuit in Fig. 4 allows self-oscillation to occur. The simulated sensitivity curve for this circuit is shown in curve (*ii*) of Fig. 2. Compared to the Fig. 1 sensitivity curve [curve (*i*) of Fig. 2], the self-oscillation frequency is higher while the frequency range is approximately the same.

2) Injection-Locked Frequency Divider: A different approach can be used to design a divider that operates at an even higher frequency than the previous versions. Consider once again the DFF divider shown in Fig. 1. At frequencies near self-oscillation, this circuit's behavior does not resemble that of a digital circuit. By eliminating the latches, the capacitance at each pair of nodes could be reduced, thereby allowing higher speed. The latches in the static frequency divider of Fig. 1 can be replaced by CML buffers as shown in Fig. 5. (This topology is similar to that in [13].) The resulting circuit is simply a ring oscillator with the full-rate clock injected at two of the

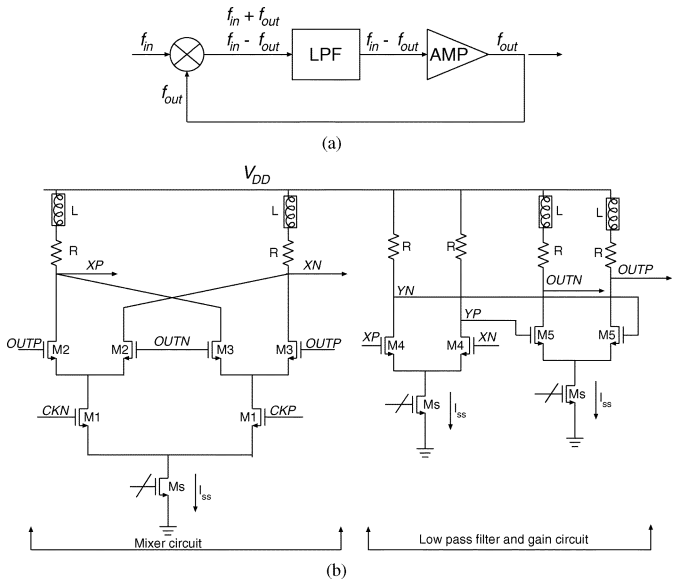

Fig. 3. Schematic of regenerative frequency divider.

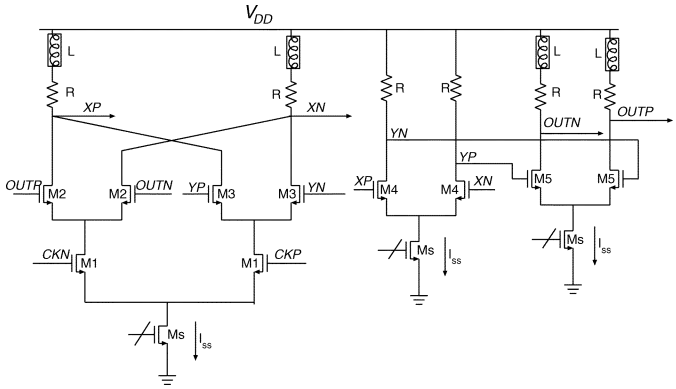

Fig. 4. Schematic of modified regenerative frequency divider.

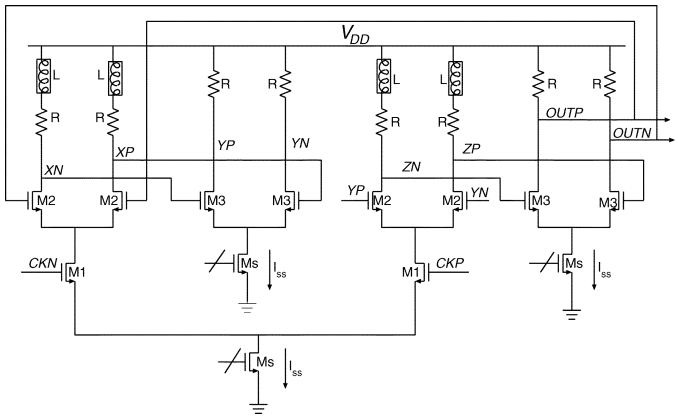

Fig. 5. Schematic of injection-locked divider.

delay cells. Injection locking a ring-oscillator instead of an LC-oscillator [8] offers the following advantages:

1) Since the ring oscillator is resistively loaded, it has a lower Q and thus exhibits a larger frequency range of operation compared to a frequency divider based on a narrowband LC-oscillator. (Simulations indicate that an LC-based divider designed using the same technology and using an

TABLE I
COMPARISON OF DIFFERENT DIVIDERS

Divider	$2f_{so}$	f_{min}	f_{max}	$f_{max} - f_{min}$	$(f_{max} - f_{min})/2f_{so}$
D-FF based	16.74 GHz	10 GHz	20 GHz	10 GHz	59%
Modified regenerative	22.14 GHz	17.4 GHz	27 GHz	9.6 GHz	43%
Injection-locked ring oscillator	36.76 GHz	34.5 GHz	38 GHz	3.5 GHz	9.5%

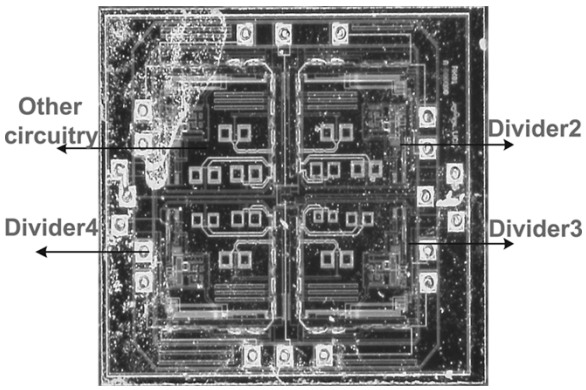

Fig. 6. Chip SEM photograph.

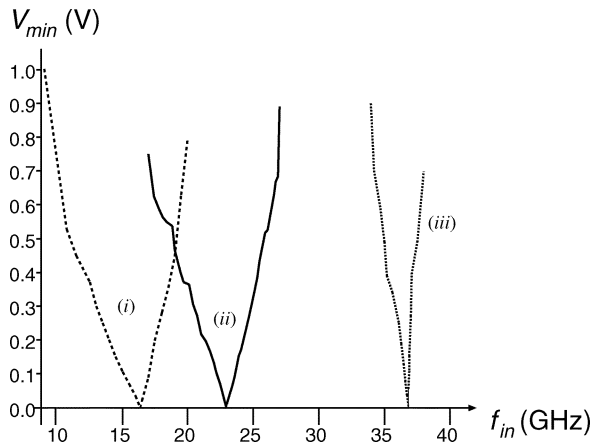

Fig. 7. Measured sensitivity curves of: (*i*) conventional frequency divider, (*ii*) modified regenerative frequency divider, and (*iii*) ring-oscillator-based frequency divider.

inductor with a Q of 5 would exhibit a frequency range that is 23% lower than that of the ring-based divider.)

2) Since the ring oscillator has more than one stage in cascade, the full-rate clock signal can be injected at various stages. If the phase relation of the full-rate clock at various injection points is selected carefully, then the range of operation can be increased significantly compared to injecting signal in only one point as described in [13]. For the circuit of Fig. 5, the signal is injected at two points, with 180° phase difference to realize divide-by-two operation.

III. CIRCUIT DESIGN AND MEASUREMENT RESULTS

The two new types of clock dividers described in the previous section (Figs. 4 and 5) as well as the conventional DFF-based frequency divider were implemented in a 0.13-μm standard CMOS process. The purpose of this experiment was to compare the performance of the different dividers by measuring their sensitivity curves. Each of the dividers under test was designed to dissipate 12 mW and drive the same capacitive load. To simplify the measurements the output of each divider under test was further divided by 32, corresponding to five additional dividers, each realized using a DFF with feedback. It was verified by simulations over process corners that at all frequencies correct divider operation was limited by the divider under test. The output buffer was designed to drive a 50-Ω load, and the input was also terminated with 50 Ω. Although in 0.13-μm the supply voltage that is recommended is 1.2 V, 1.8 V was used for more robust operation. This causes no reliability problem, as long as we ensure that the the junction voltages of all transistors are less than or equal to 1.2 V. To allow more efficient layout, the transistors were designed using parallel combinations of unit-sized transistors. For all circuits in the test chip, the unit-sized transistor used in the current sources were $5\ \mu\text{m}/0.5\ \mu\text{m}$, all others were $2\ \mu\text{m}/0.13\ \mu\text{m}$.

This chip has been fabricated and the SEM photograph is shown in Fig. 6. The size of the chip is about 1 mm $\times$ 1 mm. An Anritsu 69 367B signal generator was used to provide the input clock signal.

A comparison of the measured sensitivity curves of the dividers is shown in Fig. 7. From the figure it can be concluded that the injection-locked divider (curve *iii*) operates at very high frequency, but with a relatively narrow range (approximately 3.5 GHz). The modified regenerative frequency divider (curve *ii*) has almost the same range of operation as the conventional frequency divider (curve *i*) but operates at higher frequency. The measured self-oscillation frequency, range of operation, and maximum frequency of operation for each divider are tabulated in Table I.

IV. CONCLUSION

In this paper, two different CMOS frequency divider circuits operating at frequencies higher than those achievable by conventional dividers have been presented. These dividers are based on feedback delay realized using CML buffers. Eliminating latches reduces the capacitance at various nodes, thereby giving the required speed advantage. Unlike the DFF-based divider, all of the dividers presented are dynamic in their operation and therefore have a strict lower bound on operating frequency. The modified regenerative frequency divider exhibits a substantial increase in the maximum frequency with nearly the same range of operation as a static frequency divider. The injection-locked divider exhibits the highest frequency of operation of 38 GHz.

REFERENCES

[1] W. D. Kasperkovitz, "Frequency-dividers for ultra-high frequencies," *Philips Tech. Rev.*, vol. 38, pp. 54–68, 1978–79.

[2] K. Ishii *et al.*, "Very-high-speed Si bipolar static frequency dividers with new T-type flip-flops," *IEEE J. Solid-State Circuits*, vol. 27, no. 1, pp. 19–24, Jan. 1995.
[3] R. B. Nubling *et al.*, "25 GHz HBT frequency dividers," in *Proc. Gallium Arsenide Integrated Circuit (GaAs IC) Symp.*, Oct. 1989, pp. 125–2128.
[4] M. Wetzel *et al.*, "A 26.5 GHz silicon MOSFET 2:1 dynamic frequency divider," *IEEE Microw. Guided Wave Lett.*, vol. 10, pp. 421–423, Oct. 2000.
[5] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18 μm CMOS technology," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2003, pp. 259–262.
[6] J.-O. Plouchart *et al.*, "A power-efficient 33 GHz 2:1 static frequency divider in 0.12 μm SOI CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2003, pp. 329–332.
[7] H. Knapp, H.-D. Wohlmuth, M. Wurzer, and M. Rest, "25 GHz static frequency divider and 25 Gb/s multiplexer in 0.12 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2002, pp. 302–468.
[8] S. Verma, H. R. Rategh, and T. H. Lee, "A unified model for injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1015–1027, Jun. 2003.
[9] U. Singh and M. M. Green, "Dynamics of high-frequency CMOS dividers," in *Proc. ISCAS*, vol. 5, May 2002, pp. 26–29.
[10] H. Knapp *et al.*, "A 79 GHz dynamic frequency divider in SiGe bipolar technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2000, pp. 208–209.
[11] M. Kurisu *et al.*, "A Si bipolar 28-GHz dynamic frequency divider," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1799–1804, Dec. 1992.
[12] R. H. Derksen and H.-M. Rein, "7.3-GHz dynamic frequency dividers monolithically integrated in a standard bipolar technology," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 3, pp. 537–541, Mar. 1988.
[13] R. J. Betancourt-Zamora, S. Verma, and T. H. Lee, "1-GHz and 2.8-GHz CMOS injection-locked ring oscillator prescalers," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2001, pp. 47–50.

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