LBL-21929
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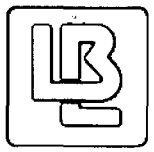

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QUAD DELAY GATE GENERATOR (LBL #21X6691 P-2)

R.J. McDonald, M.R. Maier, D.A. Landis,
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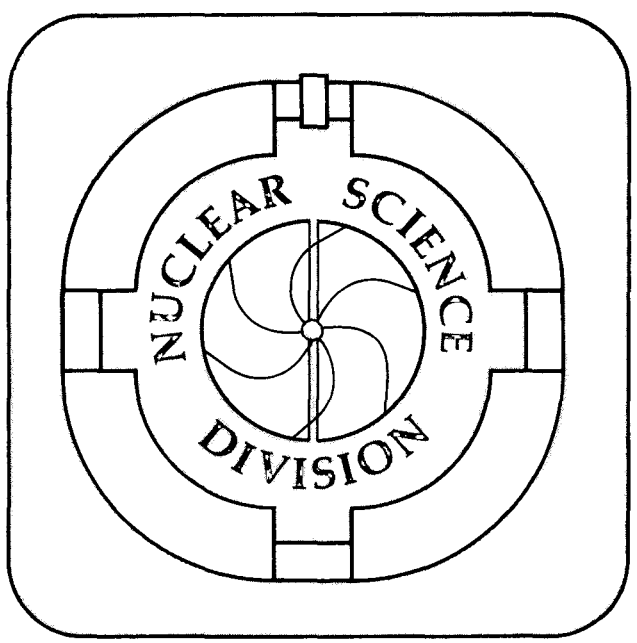
August 1986



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DISCLAIMER

Quad Delay Gate Generator (LBL #21X6691 P-2)*

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Abstract

A quad delay gate generator has been designed and packaged in a single-width NIM module. Both delay times and gate widths may be set continuously from 25 ns to 120 μsec. In normal operation, the gate follows the delay time unless a "stop" pulse cuts it short. Alternatively, the module may be operated in a bipolar mode, where the delay time is set by the input "start" pulse and reset by the input "stop" pulse. Modes and coarse time ranges are set via an octal DIP switch on the front panel. Fine adjustments of the delay and gate width are made via two twenty-turn potentiometers. Stability over a several day period was measured at ~250 ps on the 120 ns full scale range. LEDs gives a visual indication of both the input rate and the dead time.

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1.) Introduction:

Experiments in nuclear and atomic physics now require increasing numbers of detectors and channels of electronics, often on the order of tens to a hundred. In addition, set-ups are constantly changing; so flexible, rugged, modular components are essential. Typically, the number of detectors is large enough that the packing density is important, but not critical. Although many modules for these applications now exist in octal (8 channel) configurations, the front panel "real estate" becomes too crowded for the convenient use of controls and connectors. Thus, in our specifications for new modules, we have settled on quad (4 channel) configurations as being the best compromise between packing density and convenience.

Among the most common needs for nuclear and atomic physics experiments is the "delay gate" function, that is, the ability to delay a logic signal for some period of time and then regenerate a logic signal of preset width to be used in other parts of the logic circuitry. Since detectors have different response times, from fractions of nanoseconds to several microseconds, and because one typically wants to require a coincidence between different detectors, each channel of electronics will require a delay gate generator to adjust the relative timing between detectors. Even for the cases where all the detectors are fast, i.e. ~1 ns, different transit times from the experimental area to the counting area can cause these signals to differ in time by tens of nanoseconds. In order to align these signals for fast coincidences, not only must the delay gate generator have a range on the order of tens of nanoseconds, but it must be stable at the level of a fraction of a nanosecond for periods of several days. Furthermore, ADC and TDC strobes and computer interrupt signals often require delays 1000 times as long. The quad delay gate generator (QDGG) described herein spans these ranges and fulfils these needs.

2. Operation:

The general theory of operation of a delay gate generator is as follows: The input pulse generates a delay pulse **X** whose width is continually adjustable over a time range D. In this module, the delay may be adjusted over a range of ~20 ns to ~120 µsec via coarse adjust switches and a fine adjust potentiometer. A **Y** (gate) pulse of width W is generated on the trailing edge of the **X** (delay) signal. The width is similarly adjustable over the ~20 ns to ~120 µsec range. This module has an additional mode of operation in which the length of the **X** (delay) signal is determined by the time difference between the **ST** (start) and the **SP** (stop) pulse. In this mode, the time difference may exceed the normal maximum delay range of 120 µsec.

The two modes of operation of this QDGG are selected by the switch "D" of the octal DIP switch on the front panel: In mode 1, the module operates as a normal delay and gate in which an output pulse of width W is generated at a delay time D after an input **ST** (start) signal. Switch "D" must be in the "out" (fully left)

position. In mode 2, the unit operates as a bi-stable device where the **X** (delay) signal is reset only by an additional **SP** (stop) signal. Switch "D" must be in the "in" (fully right) position. Table 1 lists the modes of operation and the switch settings to activate these modes.

Several possibilities exist for each mode and they will be discussed below: The user should become familiar with these modes by repeating the examples shown in figures 3-6.

Mode 1a: The module is most frequently used in this mode. In its simplest configuration, all of the switches are in the "out" (fully left) position. Following an input **ST** pulse, the module will generate an output **Y** (gate) pulse of width W following a delay of time D where both W and D are within the range of ~20-120 ns as adjusted via the twenty-turn potentiometers on the front panel. Figure 3a shows such a case with D=80 ns and W=40 ns. The **X** (delay) outputs (2 NIM and 1 TTL) give the delay time D and the **Y** (gate) outputs (2 NIM and 1 TTL) give the gate time W. Figure 3b shows these signals with minimum delay and gate widths. Times longer than ~120 ns for both D and W may be selected by changing the ranges via switches on the front panel. Switches A, B, and C extend the ranges of the delay time and switches E, F, and G extend the ranges of the gate time respectively by factors of 10, 100, and 1000. Table 2 lists the range for each switch. If more than one delay or gate range switch is in the "in" (fully right) position, the range is the sum of the ranges selected. Note that there is an inherent delay of ~10 ns from the leading edge of an input **ST** or **SP** signal until an **X** or **Y** signal is generated. The **Y** signal is generated on the trailing edge of the **X** signal.

Mode 1b: This mode operates exactly the same as mode 1a except that an **SP** (stop) signal may interrupt the delay time and prevent the output gate signal from occurring. This is best seen by demonstration. In figure 4a, the **SP** signal occurs after the delay time D plus the gate time W and has NO effect on the **X** or **Y** signals. In figure 4b, the **SP** signal occurs before the end of the delay time D and both cuts short the delay period and eliminates the output pulse. Neither the coarse nor fine range adjusts have been changed between these two figures. Thus, the **SP** signal may be used as a "clear" or "veto" of the output. **Caution:** If the **SP** signal occurs after the delay time D but before the end of the gate time W; W will be terminated early by the **SP** signal. This is shown occurring in figure 4c. Note the 10 ns latency.

Mode 1c: This mode operates the same as mode 1b except that switch "H" is in the "in" position and thus causes a output **Y** (gate) pulse to be generated when the delay is terminated by the **SP** signal. Figures 5a and 5b show this difference. Again, neither D nor W have been changed from the previous examples. In figure 5a, the **SP** signal occurs after the delay time D plus the gate time W and again has NO effect on the **X** and **Y** signals. In figure 5b, the **SP** signal causes the delay time D to be terminated early, and since the H switch is "in", an output of width W is generated, where W is set by the coarse switches E, F, or G and the twenty-turn fine-adjust potentiometer on W.

Mode 2a: When switch D is in the "in" position , there must be an **SP** signal to terminate the delay time. The delay time D is governed solely by the difference in time between the **ST** and the **SP** signal as shown in figure 6a. The **X** (delay) signal thus operates in a bipolar mode in which it is "set" by the **ST** pulse

and "reset" by the **SP** pulse. This mode is useful for generating a "veto" signal of varying width (**X**) where the width is determined by the time difference between the **SP** and **ST** signals. In mode 2a, the switch "H" is in the "out" position so that no output **Y** (gate) signals are generated.

Mode 2b: This mode operates the same as mode 2a except that switch H is in the "in" position and this causes a output **Y** (gate) pulse to be generated when the delay signal is "reset" by the **SP** signal as shown in figure 6b. The width of the output **Y** (gate) pulse is determined by the W coarse and fine range settings.

Note that in mode 2, the **X** (delay) is determined solely by the time difference between the **ST** and **SP** input signals and may exceed the normal maximum delay range of 120 μsec. This may be useful in generating "busy" signals, as when a computer is busy processing events.

3. Summary:

One of the most important functions in nuclear instrumentation electronics is the "delay-gate" function where a logic pulse of set width is generated after some preset delay time. These delays may be used to align signals in time. Stability is of critical importance particularly if one wants to use this electronic delay instead of a cable delay for signals input to a time to amplitude converter (TAC). This QDGG has a range short enough (~20 - 120 ns) to be useful for aligning detector signals from fast detectors as well as a full-scale range long enough (~120 μsec) to generate strobes for read-out electronics. Additionally, this module has a bi-stable mode, in which the delay is governed by the time difference between two input signals and that time difference may exceed the normal maximum delay range of 120 μsec. This is useful in providing "busy" signals.

4. Footnotes:

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5. Specifications:

Inputs: **ST** (start) and **SP** (stop) : Fast negative NIM logic.

Outputs: **X** (delay) : Two NIM, one TTL. The **X** output pulses are generated ~10 ns after the leading edge of the input **ST** signal.
Y (gate) : Two NIM, one TTL. The **Y** output pulses are generated on the trailing edge of the **X** pulse and are delayed a minimum of ~25 ns from the leading edge of the **ST** pulse.

Latency: There is ~10 ns of latency between the leading edge of an input **ST** or **SP** pulse and its effect on the **X** (delay) or **Y** (gate) signals.

Operating Modes: 1a: Delay gate generator. The W (gate) signal is generated at the end of the delay time D.
1b: An **SP** signal occurs before the end of the delay time D. This terminates the **X** (delay) signal and NO **Y** signal is generated. See **Caution** in the text.
1c: An **SP** signal occurs before the end of the delay time D. This terminates the **X** (delay) signal and a **Y** signal of width W is generated.
2a: **X** is bi-stable. It is set by the **ST** signal and reset by the **SP** signal. No **Y** output is generated.
2b: **X** is bi-stable. It is set by the **ST** signal and reset by the **SP** signal. An output signal **Y** of width W is generated on the trailing edge of the **X** signal when **X** is reset.

Ranges: Mode 1: Ranges of ~20-120 ns, 0-1.2 μsec, 0-12 μsec, and 0-120 μsec on both D and W.
Mode 2: D is determined by the time difference between the **ST** and **SP** signals and W has the same adjustable ranges as in mode 1.

Indicator lights: A LED on the input indicates the rate. A bi-colored LED glows red or green depending on whether the delay D or the gate W is the major source of dead time.

Power: +6V (300 mA), -6V (1000 mA)

Table 1

MODES OF OPERATION

MODE	INPUTS	SWITCH "D"	SWITCH "H"
1a	ST only	out	out
1b	ST and SP	out	out
1c	ST and SP	out	in
2a	ST and SP	in	out
2b	ST and SP	in	in

Table 2

TIME RANGES

SWITCH	IN	OUT
A (delay)	100 ns - 1.2 µsec	10 ns - 120 ns
B (delay)	1 µsec - 12 µsec	10 ns - 120 ns
C (delay)	10 µsec - 120 µsec	10 ns - 120 ns
E (gate)	100 ns - 1.2 µsec	10 ns - 120 ns
F (gate)	1 µsec - 12 µsec	10 ns - 120 ns
G (gate)	10 µsec - 120 µsec	10 ns - 120 ns

Figure Captions

Figure 1. Picture of the quad delay gate generator (QDGG) module from the front (left picture) and from the back and side (right picture). One cover is removed to show the details of construction.

Figure 2. Illustration of the front panel and description of the controls and connectors. The eight DIP switches labelled A-H select the delay and gate coarse time ranges (see insert).

Figure 3. a) Picture of the input **ST** (Ch 1), **X** (Ch 2) and **Y** (Ch 3) signals for the operation of mode 1a with D= 80 ns and W=40 ns.

b) The same with both D and W set at their minimum values. The horizontal scale is 20 ns / div.

Figure 4. a) Picture of the **ST** (Ch 1), **SP** (Ch 2), **X** (Ch 3), and **Y** (Ch 4) signals for operation in mode 1b, where the **SP** pulse occurs after the delay time D plus the gate time W. The **SP** signal has NO effect since it occurs after the time D+W.

b) The same as part a) except that the **SP** pulse occurs before the end of the delay time D. The **X** (delay) signal is terminated early and NO **Y** (gate) signal is generated.

c) The same except the **SP** pulse occurs after the delay time D but before the end of the gate time W causing W to be cut short. See **caution** in the text, and note the ~10 ns latency between the leading edge of the **SP** pulse and its effect on the W pulse.

Figure 5. a) Picture of the input **ST** (Ch 1), **SP** (Ch 2), **X** (Ch 3), and **Y** (Ch 4) signals for operation in mode 1c, where the **SP** pulse occurs after the delay time D plus the gate time W. The **SP** signal has NO effect since it occurs after the time D+W.

b) The same as part a) except that the **SP** pulse occurs before the end of the delay time D. In mode 1c, the switch H is "in" so a **Y** (gate) signal of width W is generated off the trailing edge of the **X** (delay) signal.

Figure 6 a) Picture of the input **ST** (Ch 1), **SP** (Ch 2), **X** (Ch 3), and **Y** (Ch 4) signals for operation in mode 2a, where the delay time D is determined by the time difference between the **SP** and **ST** signals. NO **Y** signal is generated.

b) The same as part a) except that this figure depicts mode 2b where the switch H is "in" so a **Y** signal of width W is generated.

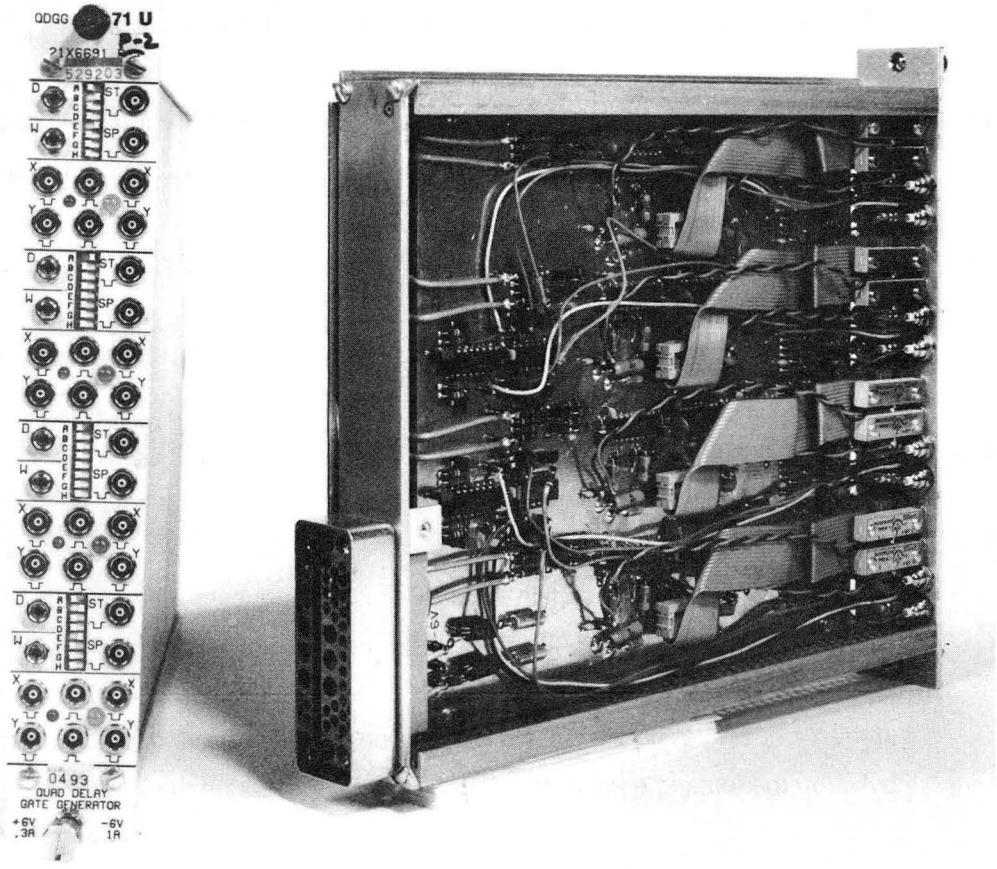

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Figure 1

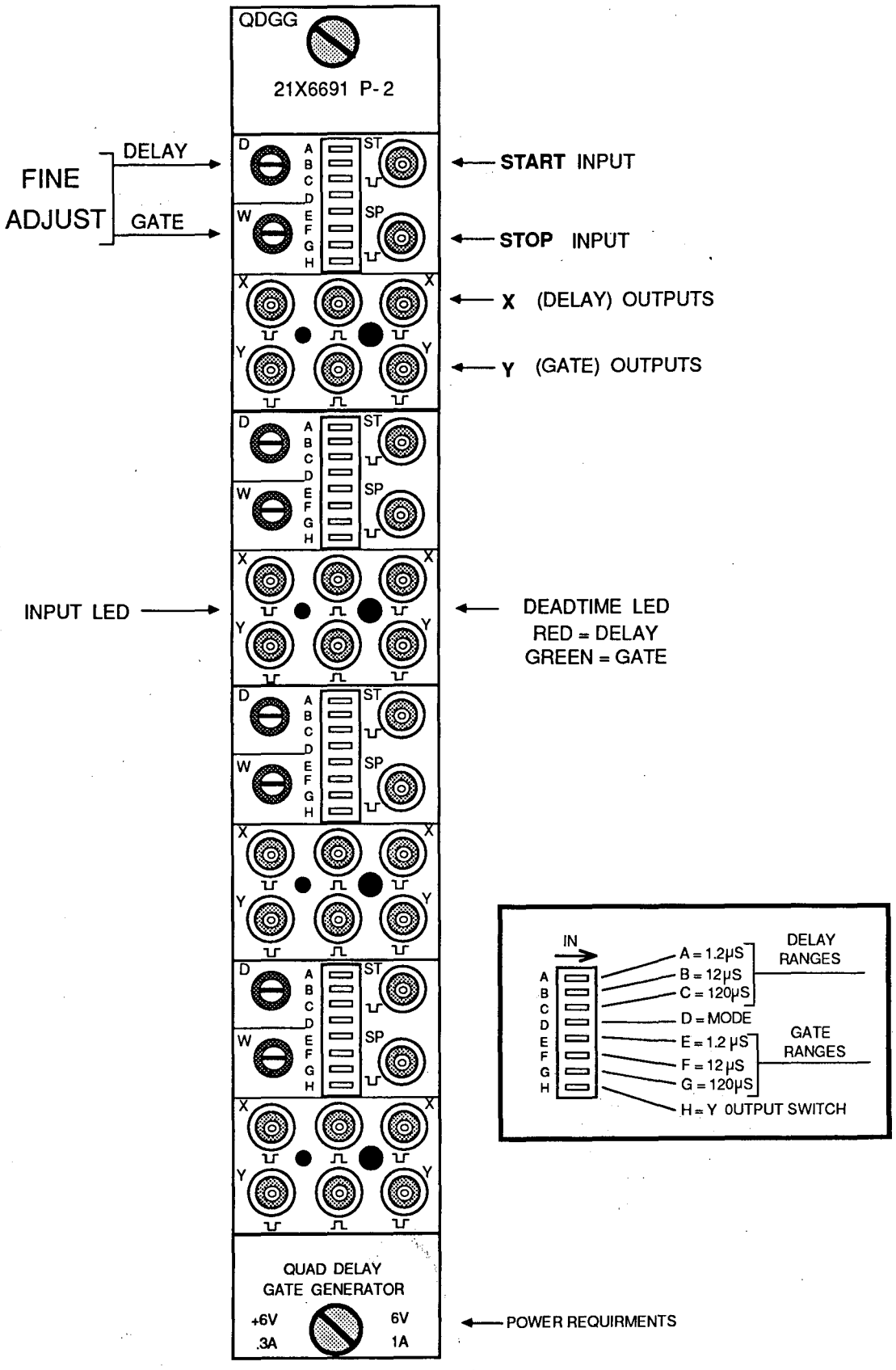
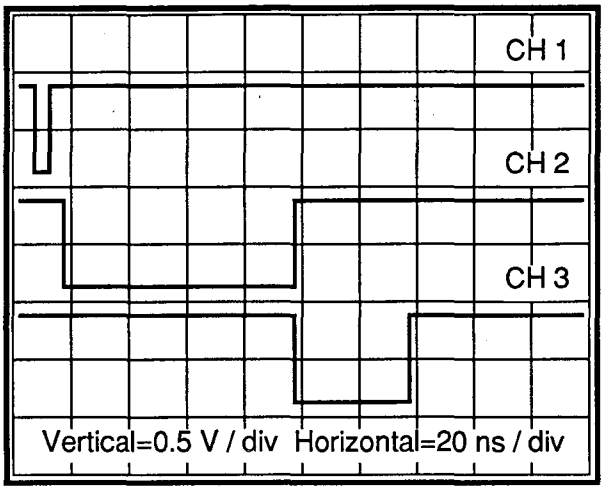

QDGG
21X6691 P-2
FINE ADJUST
DELAY
GATE
START INPUT
STOP INPUT
X (DELAY) OUTPUTS
Y (GATE) OUTPUTS
INPUT LED
DEADTIME LED
RED = DELAY
GREEN = GATE
IN
A = 1.2µS
B = 12µS
C = 120µS
DELAY RANGES
D = MODE
E = 1.2 µS
F = 12µS
G = 120µS
GATE RANGES
H = Y OUTPUT SWITCH
QUAD DELAY
GATE GENERATOR
+6V .3A
6V 1A
POWER REQUIRMENTS

Figure 2

a)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CH 2
CH 3
Vertical=0.5 V / div Horizontal=20 ns / div

b)

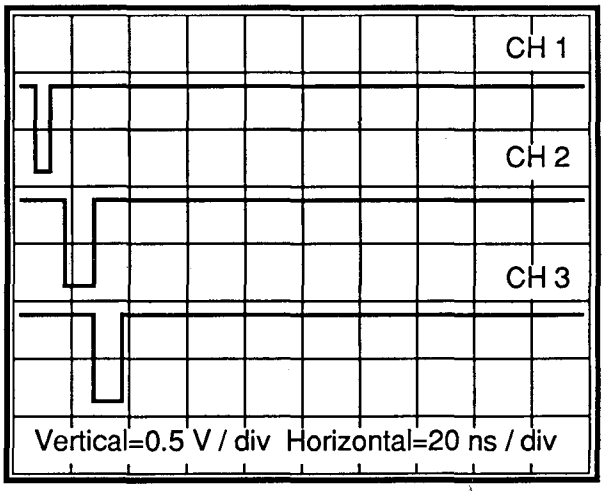
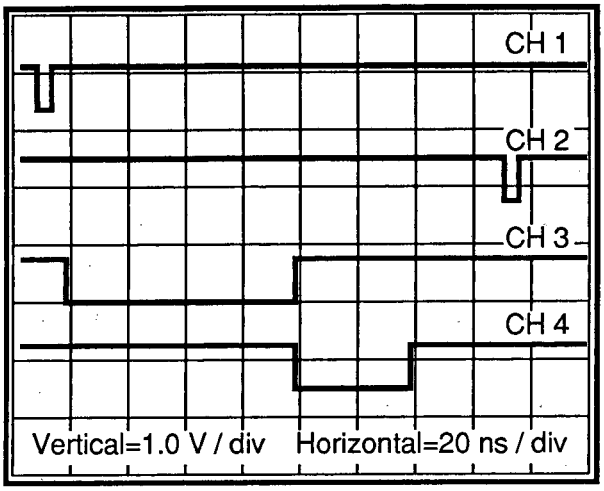

CH 1
CH 2
CH 3
Vertical=0.5 V / div Horizontal=20 ns / div

Figure 3

a)


CH 1
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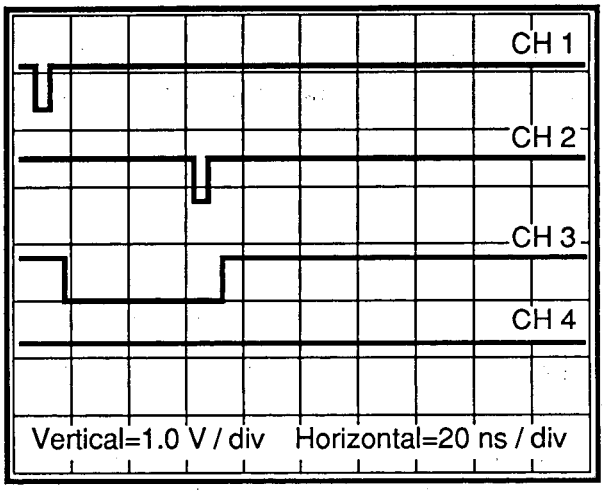
CH 3
CH 4
Vertical=1.0 V / div
Horizontal=20 ns / div

b)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CH 3
CH 4
Vertical=1.0 V / div
Horizontal=20 ns / div

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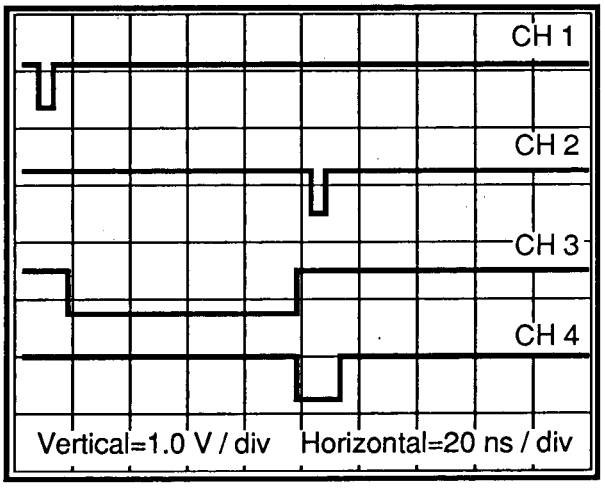
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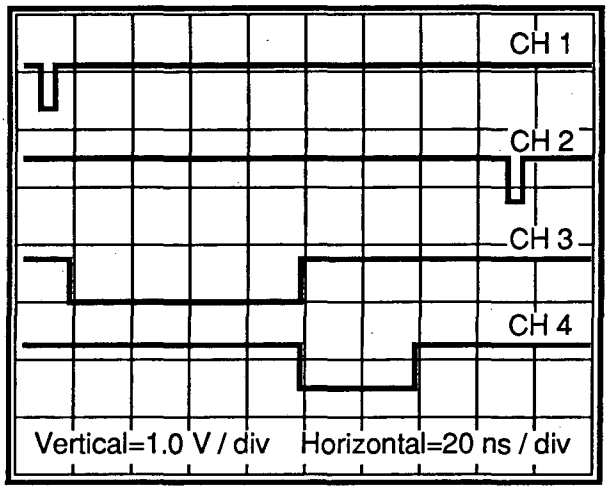
CH 2
CH 3
CH 4
Vertical=1.0 V / div
Horizontal=20 ns / div

Figure 4

a)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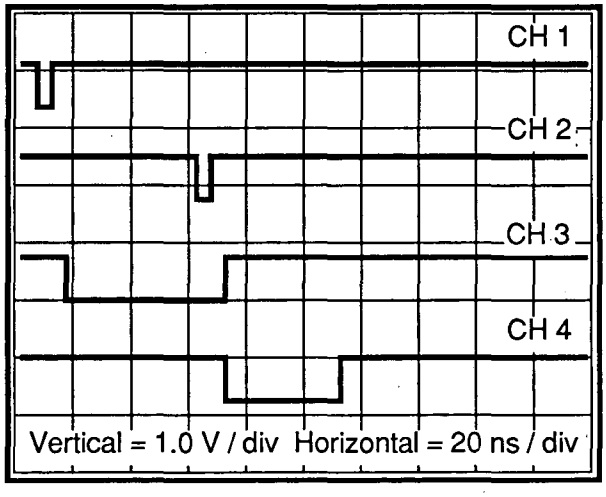
CH 2
CH 3
CH 4
Vertical=1.0 V / div Horizontal=20 ns / div

b)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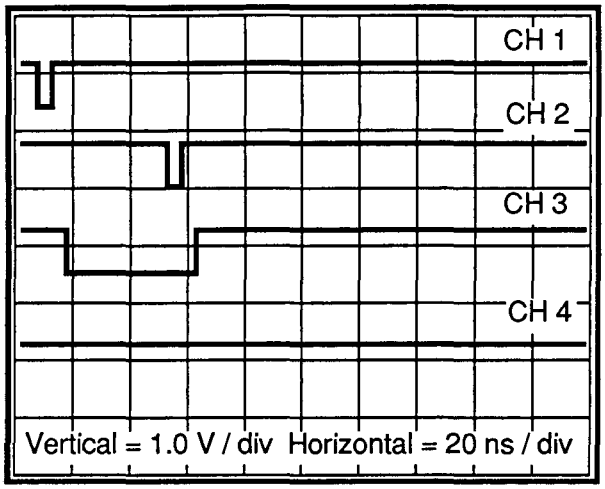
CH 2
CH 3
CH 4
Vertical = 1.0 V / div Horizontal = 20 ns / div

Figure 5

a)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CH 4
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b)

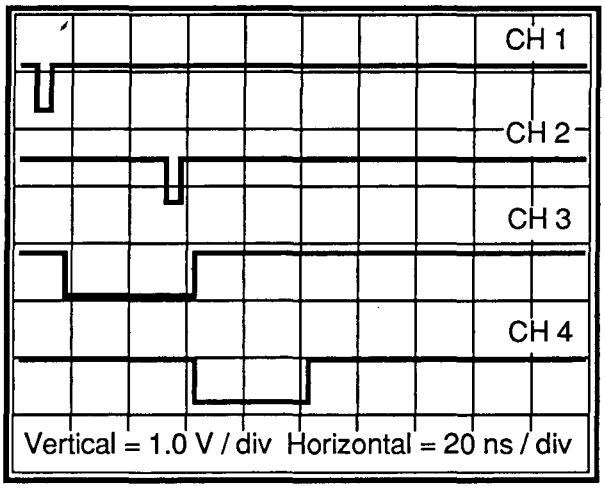
CH 1
CH 2
CH 3
CH 4
Vertical = 1.0 V / div Horizontal = 20 ns / div

Figure 6

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