

On-chip intercalated-graphene inductors for next-generation radio frequency electronics

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On-chip metal inductors that revolutionized radio frequency electronics in the 1990s suffer from an inherent limitation in their scalability in state-of-the-art radio frequency integrated circuits. This is because the inductance density values for conventional metal inductors, which result from magnetic inductance alone, are limited by the laws of electromagnetic induction. Here, we report inductors made of intercalated graphene that uniquely exploit the relatively large kinetic inductance and high conductivity of the material to achieve both small form-factors and high inductance values, a combination that has proved difficult to attain so far. Our two-turn spiral inductors based on bromine-intercalated multilayer graphene exhibit a 1.5-fold higher inductance density, leading to a one-third area reduction, compared to conventional inductors, while providing undiminished Q-factors of up to 12. This purely material-enabled technique provides an attractive solution to the longstanding scaling problem of on-chip inductors and opens an unconventional path for the development of ultra-compact wireless communication systems.

The Internet of Things (IoT) promises unprecedented connectivity between people and 50 billion things by 2020^{1,2}, with a potential economic impact of US\$2.7 trillion to US\$6.2 trillion per year by 2025^{1,3}. This will require a tremendous number of miniaturized wireless connections that are driven by radio frequency (RF) integrated circuits (RF-ICs) that demand scalability, flexibility, high performance and ease of integration. Moreover, the market value of radio frequency identification (RF-ID), which employs electromagnetic fields to automatically identify and track tags attached to objects, is expected to rise to US\$18.68 billion by 2026⁴. Planar on-chip metal inductors (Fig. 1a) are essential passive devices in RF-ICs and can occupy up to 50% of the chip area. They also contribute a major part of the form factor of RF-IDs (see Supplementary Section 1). However, unlike the continuous scaling of transistors and interconnects in IC technology, which was achieved with an increase in performance, progress toward miniaturization of on-chip inductors has remained elusive, mainly due to the fact that large inductor areas, dictated by fundamental electromagnetics, are required to deliver desirable inductance values and performance targets (Fig. 1b; see also Supplementary Section 2).

To achieve continuous size scaling while fulfilling the inductance and performance requirements, improvement in the inductance density is essential, which is defined by inductance per unit area = total inductance (L_{total}) / inductor area, where L_{total} is the sum of the magnetic inductance (L_M) and the kinetic inductance (L_K) (Fig. 1a). Magnetic inductance is the property of an electrical conductor by which a change in current through it, causing a change in the magnetic flux, induces an electromotive force in both the conductor itself (self-inductance) and in any nearby conductors (mutual inductance) that opposes the change. Kinetic inductance is the manifestation of the inertial mass of mobile charge carriers in alternating electric fields as an equivalent series inductance. L_K arises naturally as the inductive impedance per unit length of

the conductor in the Drude model for a.c. electrical conductivity. Hence, the magnetic inductance is determined by the geometrical/structural design of the inductor, while kinetic inductance is purely a material property (see Supplementary Section 3 for more details). Therefore, structural design and materials innovation, that determine L_M and L_K , respectively, are two simultaneous ways to improve the inductance density. As shown in the example in Fig. 1b, a comparable L_K (if it exists) with respect to L_M can significantly improve both the inductance and the quality factor (Q-factor, or Q, the ratio of the inductive reactance to the resistance of an inductor at a given frequency, which is a measure of its efficiency). However, because in conventional metals L_K is negligibly small (because of relatively weak carrier inertia) compared to L_M , almost all studies in the past few decades have been focused on structural improvements to make full use of the magnetic field, such as layout optimization⁵, micro-electromechanical-system fabrication^{6,7}, three-dimensional self-rolled-up⁸ and vertical-stacked^{9,10} architectures, and magnetic cores/dielectrics^{11,12}.

Theories have identified that carbon nanomaterials, including carbon nanotube bundles and multilayer graphene (MLG), can be a very attractive materials-based approach for on-chip inductors^{13–15}, because the large momentum relaxation time (τ) of low-dimensional carbon allotropes could lead to large L_K for certain on-chip inductor sizes, which can be comparable to L_M , thus contributing to high area-efficiency and performance, as well as immunity to the skin effect¹⁶ (a phenomenon that causes the resistance of a metal wire to increase significantly at high frequencies, while decreasing the inductance with the frequency, due to the tendency of a high-frequency alternating current to flow through only the outer layer of a conductor). Using MLG also ensures that the large quantum contact resistance of monolayer graphene can be lowered to acceptable values¹⁶. However, there are two key challenges in using MLG: the much lower conductivity of intrinsic MLG compared to

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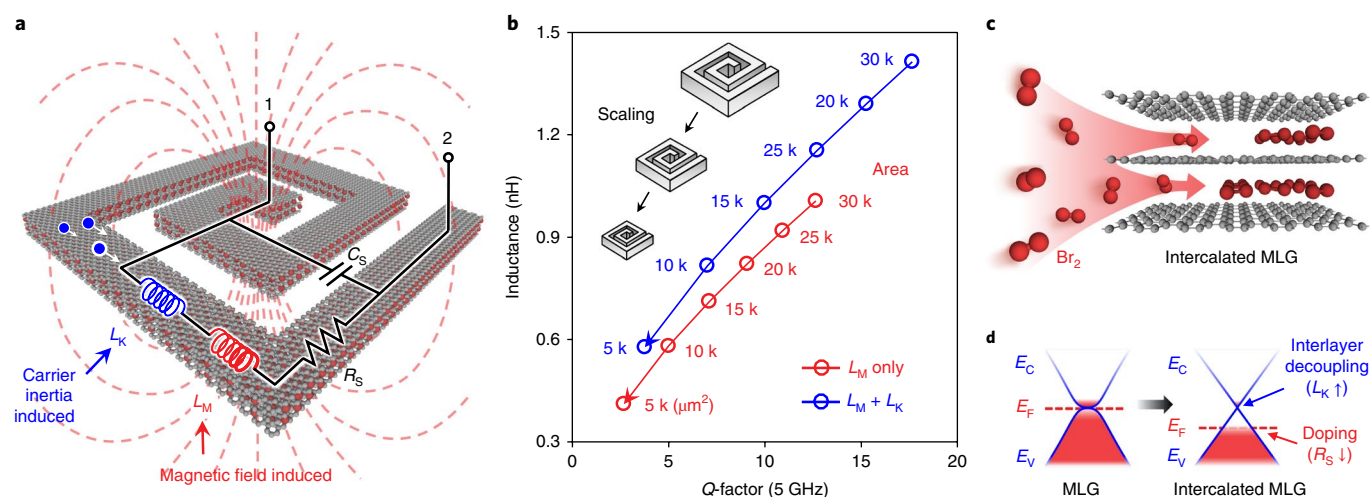


Fig. 1 | Significance of kinetic inductance and concept of intercalated MLG on-chip inductors. **a**, Schematic of a spiral inductor and its simplified equivalent circuit (two-port network). L_M and L_K represent the magnetic and the kinetic inductances, respectively. Red dotted curves represent the time-varying magnetic field, which results in L_M (both self and mutual). Blue dots represent the charge carriers with inertia, which results in L_K . R_S and C_S represent the series resistance and the inter-turn capacitance, respectively. The substrate and its parasitics are not shown. **b**, Simulated total inductance and Q-factor (at 5 GHz) of a two-turn inductor with area ($=$ outer diameter²) scaling, for conventional Cu inductors without L_K (red) and with artificially added L_K (blue). Each parameter other than L_K is assumed to be identical for both cases. In the case with L_K , L_K is assumed to be 50% of the value of L_M , which is shown to be experimentally achievable by intercalated MLG in this work. The corresponding area is marked next to each data point. Insets illustrate how the layout is scaled. See Supplementary Section S4 for further details about **a** and **b**. **c**, Schematic of the bromine (Br_2) intercalated MLG used as the spiral conductor material in this work. **d**, Effects of intercalation on the band structure: shift of the Fermi level by a doping effect that reduces R_S and improves the Q-factor, as well as change of shape (hyperbolic to linear) by an interlayer decoupling effect that increases the momentum relaxation time and thereby increases L_K .

conventional metals results in a significant performance loss—low (≤ 3) Q-factors¹⁷; and the interlayer coupling of MLG reduces the charge carrier inertia and thus L_K (see Supplementary Section 5 for details).

Here, we report an on-chip inductor based on intercalated MLG (Fig. 1a) that overcomes the fundamental scalability challenge exhibited by on-chip inductors, without a loss of performance. This has been achieved by exploiting the high kinetic inductance and high conductivity of intercalated MLG, a concept that introduces a completely new way of designing inductors since their invention nearly 200 years ago. Specifically, bromine intercalation is employed (Fig. 1c), which boosts both the conductivity of MLG (by increasing the carrier density via the doping effect) and L_K (by interlayer decoupling) (Fig. 1d). The technique leads to sufficiently high Q-factors up to 12 in a typical two-turn layout, and up to 1.5-fold higher inductance densities (with plenty of room for further improvement) with respect to copper counterparts with the same layout and Q-factors, which translates to an area reduction of about one-third. Such high-performance and area-efficient spiral intercalated MLG inductors inherently provide the scalability, design flexibility and discreteness required for the next-generation RF-ICs and RF-ID technology needed to realize the potential of the IoT. Moreover, intercalated MLG has been recently demonstrated to address the fundamental current-carrying capacity problem of scaled copper interconnects used in IC applications¹⁸. Hence, our demonstration of intercalated MLG inductors could provide an ‘all-carbon’ back-end-of-line (BEOL) conductor technology for next-generation ICs to provide the ultimate performance and reliability in the smallest form factor possible.

Design and fabrication of intercalated MLG inductors. Our spiral inductor design based on intercalated MLG is shown in Fig. 2a. Intercalated graphene/MLG, or namely graphite intercalation compounds (GICs), have a long research history, and have shown surprising properties^{19,20}. It is worth noting that MLG and graphite are the same material in principle, because of the same lattice

structure and stacking order, although graphite usually has a greater number of layers. However, providing an exact number of layers to differentiate MLG from graphite is impossible. Since the technique demonstrated in this work applies both for MLG and graphite, we use the term MLG to represent both cases in the remainder of the paper. Similarly, we use the term intercalated MLG or intercalated graphene instead of GIC, unless used in the context of the materials science/chemistry glossary. Another reason for using this terminology is that, in our work, the material exhibits graphene-like electrical properties instead of graphite-like properties.

Several candidates as intercalation guests (dopants) have been identified that can improve the conductivity of MLG, such as alkali metals (for example, Li, Na and K), halogens (for example, Cl_2 , Br_2 and ICl) and halides (for example, BF_3 , AsF_5 , $AuCl_3$ and $FeCl_3$)^{18–22}. Among those options, bromine intercalation is favourable due to its low processing temperature, short processing time and deeper diffusion into the intercalation host (MLG), as well as the closer lattice matching of the bromine intercalation layer with that of MLG¹⁹. As illustrated in Fig. 1c, Br_2 molecules can diffuse into the gaps between graphene layers, forming intercalation layers and remaining stable, which induces bands with a high density of states below the Dirac point (and intrinsic Fermi level E_{Fi}) of the graphene layers. These impurity states attract electrons from graphene, generating hole carriers in the valence band of graphene and resulting in p-type doping (see Supplementary Section 5 for ab initio simulations).

To achieve the bromine intercalation, millimetre-sized highly oriented pyrolytic graphite (HOPG) slices were first transferred onto quartz (SiO_2) substrates ($1\text{ cm} \times 1\text{ cm} \times 1\text{ mm}$) at room temperature and then set in a glass tube. After evacuation down to 0.5 Pa, the samples were exposed to Br_2 gas at room temperature for 90 minutes using a two-zone vapour transport method (see Supplementary Section 6 for more details). The cross-sectional scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDX) images of the intercalated samples are shown in Fig. 2b,c, respectively, where dark signals

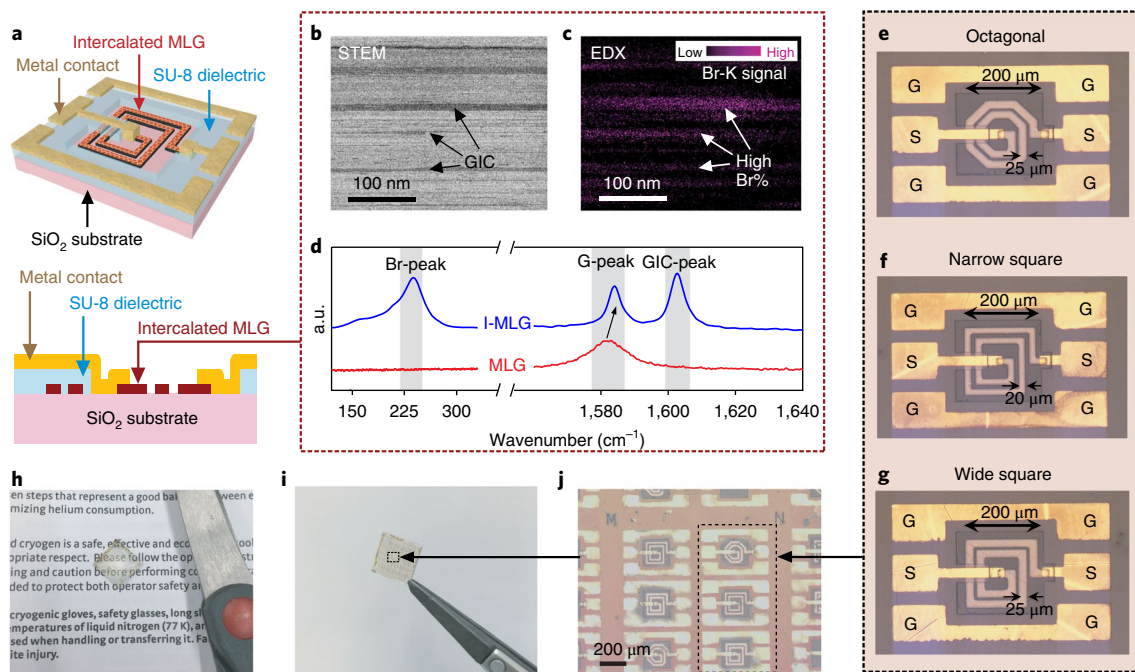


Fig. 2 | Design of bromine-intercalated graphene inductors. **a**, Schematic of the two-turn inductor design: top: perspective view; bottom: cross-sectional view. **b**, The cross-sectional STEM image of the intercalated MLG showing the randomly distributed doping. **c**, EDX mapping image of the bromine-K signal from the same region as in **b**. **d**, Raman spectra before and after Br-intercalation. **e–g**, Optical images of octagonal (**e**), narrow square (**f**) and wide square (**g**) intercalated MLG on-chip inductors. G and S represent the ground line and signal line of the GSG CPWs, respectively. **h, i**, Photos of a fabricated chip with intercalated MLG inductor arrays placed on paper (**h**) and clamped by a tweezer (**i**). **j**, Optical microscope image of an inductor array.

and light signals are alternately stacked, indicating that bromine is intercalated to random regions across the stack of graphene layers, forming a heterogeneous mixture of highly doped MLG and lowly doped MLG. The average thickness increment measured by atomic force microscopy (AFM) is around 6.7% of the original thickness. The average concentration of bromine atoms is about 3%, as confirmed by X-ray spectroscopy (XPS) measurements. Raman spectroscopy (Fig. 2d) confirmed the existence of intercalation (due to appearance of a new Br-peak and a GIC-peak, as well as a shift of the G-peak) and a GIC stage number (number of graphene layers over number of intercalation layers) of about 3 in the highly doped region. According to Hall measurements, intercalated MLG shows five times higher conductivity and carrier density without degrading carrier mobility, with respect to undoped MLG. More details about the various characterizations of bromine-intercalated MLG are provided in Supplementary Section 6.

Subsequently, the intercalated MLG flakes were patterned into spiral inductor coils using photolithography followed by oxygen inductive coupled plasma etching (Fig. 2b). In this work, a set of two-turn layouts with an outer diameter of 200 μm were designed as examples to demonstrate the intercalated MLG technique (Fig. 2e–g). Such a layout works mainly in the relatively high frequency range (10–50 GHz) (see Supplementary Section 7), which is of greater interest in this work for next-generation radio frequency electronics. It is the general trend that almost all wireless applications operate at increasingly higher frequencies as technology scales. This is due to the increase in transistor cut-off frequencies, as well as the need for greater bandwidths. Other than the square-shaped structures simulated in the theoretical works^{13–15}, for comparative study, three slightly different layouts have been designed—octagonal shape (Fig. 2e), narrow square shape (Fig. 2f) and wide square shape (Fig. 2g). The inter-turn distances are 5 μm , 10 μm and 5 μm for the three layouts, respectively. According to the simulations of metal inductors (see Supplementary Section 7), these parameters provide the optimal L_M and C_S , and hence optimal Q -factors for each layout.

Then SU-8 photoresist was spin-coated, patterned and hard baked (180°C) to form a permanent low- k polymer dielectric layer with a thickness of 2 μm and a relative permittivity of 3.1, serving as the isolation layer between the inductor coils and the overlap metal pads. Subsequently, metal contacts and pads (Ni/Au: 10 nm / 2,000 nm) were deposited and patterned. The metal pads are designed as ground–signal–ground (GSG) coplanar waveguide (CPW)²² structures with an intercalated MLG inductor in the signal path for two-port scattering parameter (S-parameter) measurements (Fig. 2e–g). The entire fabrication process is illustrated in Supplementary Section 8. To demonstrate the repeatability and to find the thickness dependence, tens of intercalated MLG inductors with different thicknesses (different series resistances) were fabricated on the same 1 cm \times 1 cm die. Fig. 2h,i shows the entire chip and Fig. 2j shows a micrograph of an intercalated MLG inductor array on the chip.

Characterization of intercalated graphene inductors. Subsequently, S-parameter measurements were performed in the frequency range 100 MHz–67 GHz using an Agilent N5227A Network Analyzer and a microwave probe station equipped with Cascade Infinity GSG-probes with a 150 μm pitch size. To capture the intrinsic properties of the MLG inductors themselves, a standard de-embedding procedure was performed to remove the parasitic effects of the CPW metal pads using dummy (open) structures (GSG CPWs without MLGs on the signal path) fabricated on the same chip, which is sufficient for devices operating below 50 GHz. Details on S-parameter measurements can be found in Supplementary Section 9. Then the inductance L and the Q -factor can be calculated as $L = - (2\pi f \text{imag}(Y_{11}))^{-1}$ and $Q = - \text{imag}(Y_{11}) / \text{real}(Y_{11})$, respectively, where f is the frequency, Y_{11} is the input admittance of Port 1 with Port 2 shorted, converted from S-parameters, and real/imag denotes the real/imaginary part, respectively (see Supplementary Section 9.2 for further discussions).

Comparisons of L and Q between the intrinsic MLG inductors and the intercalated MLG inductors were first performed

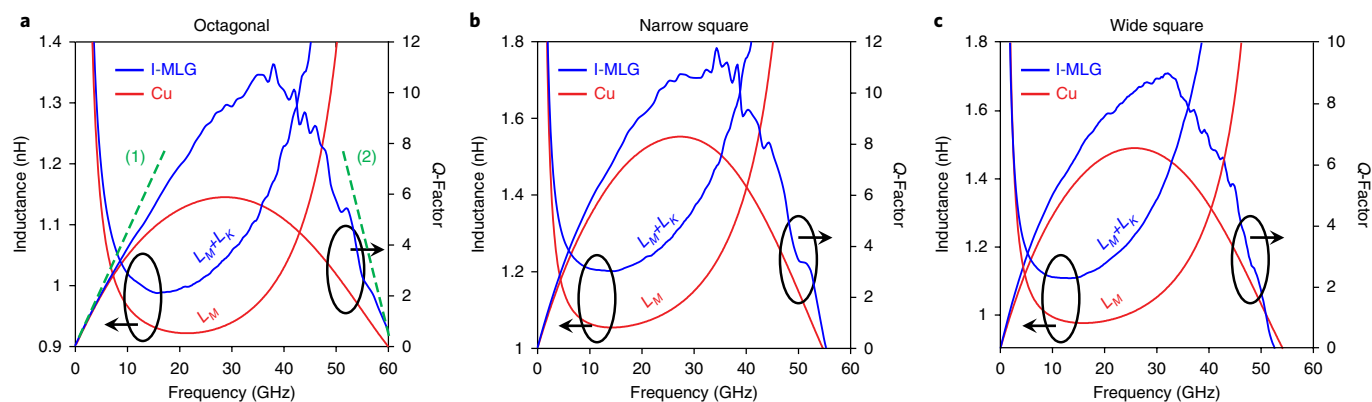


Fig. 3 | Measured inductance and Q-factor versus frequency for intercalated MLG inductors in different layouts. **a–c**, octagonal (**a**), narrow square (**b**) and wide square (**c**) layouts. In each panel, the intercalated MLG (I-MLG) and the Cu inductors compared have the same series resistance, and the same layout and substrate. The series resistances are 14 Ω , 10 Ω and 28 Ω for **a**, **b** and **c**, respectively, since **a**, **b** and **c** have different layouts and spiral thicknesses. Green dashed lines in **a** represent (1) $\omega L/R_s$ upper limit of Q-factor and (2) substrate loss, self-resonance and skin effects at high frequencies. See Supplementary Section 4 for further details about these two lines. The curves for the Cu samples are generated by finite element method after calibration with experiments on some control samples (see Supplementary Section 7 for details).

(see Supplementary Section 10). With bromine intercalation doping, a significant improvement of both L and Q was observed in all three layouts. The improvement of L is mainly due to the band structure engineering—a interlayer decoupling effect from layer separation by intercalation doping, where the energy dispersion of MLG changes from the hyperbolic form to the linear form as in few-layer or monolayer graphene. According to Supplementary Section 5, this band structure engineering can improve the L_K value of MLG. The improvement of Q is a combined effect of both the band structure engineering (improving L_{total}) and the doping effect (increasing carrier density leading to reduced series resistance R_s), since the upper bound of the Q-factor is proportional to L_{total}/R_s .

The measured Q-factor versus frequency for one sample in each layout is plotted in Fig. 3, compared with copper inductors with the same layout and substrate. In many RF circuits, such as voltage-controlled oscillators, the series resistance of the inductors has to be precisely controlled and compensated by a negative resistance provided by complementary-metal-oxide-semiconductor (CMOS) transistors with specified sizes. Hence, the MLG and copper inductors in this work are compared for the same series resistance to emulate identical circuit environments.

It can be seen that all three designs can provide a maximum Q-factor of around 10, which is sufficient for many on-chip inductor applications²³. The maximum Q-factor is about 12 for one of the narrow square inductors with a series resistance of 10 Ω (Fig. 3b). It is obvious that, with the same series resistance, both higher L and higher Q compared to that of copper are achieved by intercalated MLG. Since the value of L_M is almost identical in copper and MLG, primarily due to the same layout design, the source of the increased inductance value in intercalated MLG compared to copper can be attributed only to the kinetic inductance L_K .

The measured inductance (density) versus maximum Q-factor plots for all the intercalated MLG inductors are shown in Fig. 4. Generally, thinner inductors have a higher inductance (due to the slightly lower inter-turn capacitance and much higher L_K) and a lower Q-factor (due to the higher series resistance), while thicker inductors have a higher Q-factor and a lower inductance. Hence, by tuning the spiral thickness, a trade-off between L and Q can be realized (inset in Fig. 4a). Overall, there is no significant difference among the three layout designs in terms of Q-factors, except that the narrow square inductors have a slightly greater scattering in their Q-factors because of the larger doping degradation variation for narrower widths (Fig. 4b).

Compared to copper inductors, it is clear that the same Q-factors can be easily achieved using intercalated MLG. More importantly, for all the three layout designs, the inductance values are always much better than copper when the same Q-factors are achieved. As shown in Fig. 4, without compromising Q-factors, an up to 1.5-fold higher inductance density can be achieved by intercalated MLG inductors. As discussed above, the increased inductance value in MLG compared to copper is contributed by its high kinetic inductance L_K , which is up to 50% of the value of L_M . In other words, in RF circuit designs, the area required to provide the necessary inductance value can be reduced by up to one-third (estimated as required area = required inductance / inductance density). It is worth noting that a more accurate evaluation of area reduction needs to consider other parameters, such as the change of layout (spiral width and length) and the change of operating frequency, which requires significant modelling and experimental efforts beyond the focus of this work.

Conversely, when the same inductance density is achieved by both an intercalated MLG inductor and a copper inductor, the intercalated MLG inductor exhibits a much higher Q-factor. One can also choose specified L – Q points on the blue curves in Fig. 4 to achieve a combination of both higher L and higher Q compared to that of copper, as illustrated by the dotted arrowed lines in Fig. 4b,c. Hence, compared to copper-based inductors, there is a clear advantage of the intercalated MLG inductors in terms of inductance density as well as Q-factors: the high L –high Q combination that could never be achieved simultaneously in a given layout with conventional metals, such as copper, has been achieved with intercalated MLG (see Supplementary Section 11 for more discussion). It is obvious that intercalated MLG on-chip inductors are closer to the top-right ‘desired direction’ illustrated in Fig. 4.

The concentration of bromine in the samples is about 3%, although it has been shown in the literature that bromine concentrations of up to 6% can be achieved experimentally, and could provide a conductivity of $2.9 \times 10^6 \text{ S cm}^{-1}$, which is five times higher than that of copper^{24,25}. On the other hand, as mentioned above, the average intercalation stage in the samples is 3. However, further improvement in both L and Q is expected if stage-1 intercalation can be achieved (see Supplementary Section 5). There are also other intercalation guests that can induce higher and/or more stable doping than that of bromine^{18,19} (see Supplementary Sections 12 and 13 for further discussions). Moreover, the Q-factors can be further increased by improvement of the contact quality¹⁷. Hence, with

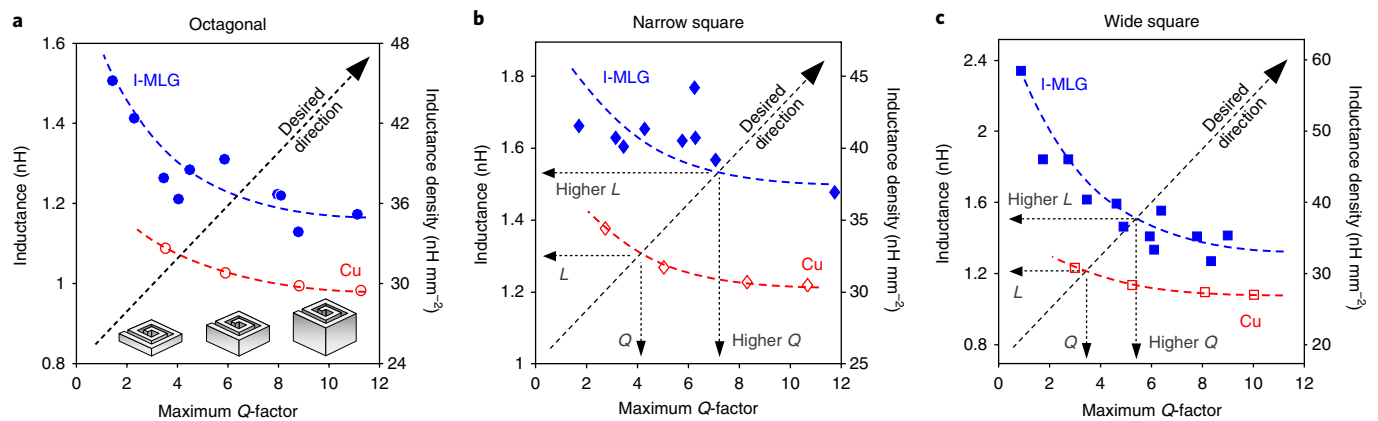


Fig. 4 | Inductance and the corresponding inductance density versus maximum Q -factors of intercalated MLG and copper inductors. a–c, octagonal (a), narrow square (b) and wide square (c) two-turn layouts. Symbols represent data points, and dashed curves are drawn only to guide the eyes. I-MLG represents intercalated MLG. Inset in a indicates that the L - Q trade-off is realized by tuning the spiral thickness. For each device, the inductance (density) is extracted at the frequency where the maximum Q -factor is found (typically around 30 GHz). Cu data are calculated by finite element method and calibrated by experiments (see Supplementary Section 7). Due to the sub-optimal intercalation doping, the conductivity of Br-MLG is still smaller than that of the Cu thin films. Hence, to achieve comparable Q -factors to those of Cu, thicker intercalated MLG films are used to compensate for the lower conductivity. In a–c, the thickness range for Cu is 50–300 nm, while for intercalated MLG, the ranges are approximately 150–1,000 nm in a, 400–1,200 nm in b and 200–1,000 nm in c.

advancements in graphene intercalation technology and contacts, improvements in both the Q -factors and L can be expected.

In conventional metal inductors, reducing the size/area of the spiral reduces the amount of magnetic flux, which is proportional to the ‘surface area’ of the individual spiral segments as well as the area enclosed by each turn of the spiral (see Supplementary Section 3). This reduces the magnetic inductance and can also induce severe ‘size effects’ (such as a quantum confinement that worsens the electronic structure, as well as surface, edge and grain boundary scatterings)²⁵ when the dimensions are scaled down to tens of nanometres. Due to such effects, electrons are less mobile in nano-scale metals, leading to a sharp nonlinear decline in the metal conductivity, and thereby in the Q -factor. Hence, dimension scaling of metal inductors is not sustainable. Remarkably, MLG has no severe size effects when the thickness and width are scaled down to tens of nanometres¹⁸. This is because the unique electronic structure allows electrons/holes to move with minimal resistance in quantum-confined layers, and because of its two-dimensional nature, where the pristine interfaces minimize the roughness and scattering of the surfaces²⁶. On the other hand, the kinetic inductance becomes increasingly dominant (since L_k scales as L_k/N , where N is the number of conducting channels) with thickness and width reduction of MLG (see Supplementary Section 5 for further details). Hence, in the case of any further scaling, MLG can achieve a greater inductance density without degrading the conductivity compared to conventional metals. Such scalability of MLG can be further enhanced by intercalation, and can be highly beneficial for designing ultra-compact and ultra-thin passives, including on-chip inductors and antennas for future wireless communication systems.

Conclusions

We have demonstrated a fundamentally distinct on-chip inductor that can significantly improve the inductance density, and thus area-efficiency, without compromising performance, by exploiting the unique characteristics of intercalated MLG. Using bromine intercalation as an example, we showed that intercalated-MLG-based on-chip inductors can exhibit undiminished Q -factors of up to 12 and an up to 1.5-fold higher inductance density than that of copper inductors with the same footprint, which translates to an inductor area reduction by about one-third. An example of chip-area reduction

is provided in Supplementary Section 14. Moreover, because the technique is a purely materials-based approach, and does not rely solely on the magnetic field, our approach is compatible with various structural design techniques such as multilayer/three-dimensional inductor structures, rolling-up and/or the use of magnetic cores/dielectrics. Hence, it can be used in many state-of-the-art inductors to further improve the performance and form-factors. In addition, the approach is useful for the alleviation of unwanted electromagnetic coupling between neighbouring inductors in scaled RF-IC technologies, because kinetic inductance has no coupling or mutual component. The planar nature of two-dimensional materials and the low-temperature processing enables the BEOL integration with current RF/analog technologies with relative ease (see further discussions in Supplementary Section 15).

Our demonstration highlights the promise of a new working mechanism for on-chip inductors and paves the way for the design and fabrication of graphene-based on-chip inductors for RF/analog-IC applications, providing guidelines for future RF/analog-IC design based on two-dimensional materials, with significant implications for numerous applications in communications, sensing and energy storage/transfer. It also increases the options for designing other on-chip passive components by exploiting a different working mechanism using low-dimensional materials. Combining the superb mechanical and optical properties of two-dimensional materials, our demonstration can also open up new avenues in fabricating the flexible/stretchable/wearable wireless electronics that are needed to realize the emerging ideas of the Internet of Things and Industry 4.0 (Cyber-Physical Systems—the 4th industrial revolution).

Methods

Device Simulation. Numerical simulations of inductors based on conventional metals (copper and silver) were performed for reference and calibration prior to the design and fabrication of intercalated graphene inductors. The simulations were implemented using ANSYS HFSS, a commercial software relying on the finite element method (FEM) to solve Maxwell equations. Considering this full-wave electromagnetic simulation technique, on-chip inductors are modelled as equivalent bulk coils with electrical conductivities incorporating grain-boundary and surface-scattering effects at the micro- and nano-scale for metals²⁷, and conductivities extracted from d.c. measurements for graphene. The conductivities taking into consideration size effects for Cu and Ag are 48.46×10^6 and 50.97×10^6 S m⁻¹, respectively²⁷. Subsequently, full inductor models were built in the software according to the actual physical structures that we fabricated. The

pad structures are designed as a GSG CPW with a graphene inductor test structure in the signal path of a two-port network. Further discussions about the simulation can be found in Supplementary Section 7.

Intercalated graphene preparation. Millimetre-sized HOPG slices were first transferred onto quartz substrates. For Br intercalation, the samples were set in a glass tube. After evacuation down to 0.5 Pa, the samples were exposed to bromine gas at room temperature for 90 min using a two-zone vapour transport method²⁸. The slices were patterned into ribbons or spirals using oxygen inductive coupled plasma etching, the etching selectivity of which is more than 100:1 for MLG:quartz (SiO₂). Further discussions about the entire process can be found in Supplementary Section 6.

Four-probe device fabrication. For four-probe measurement samples, metal contacts and pads (Ni/Au: 40 nm / 760 nm) were deposited by vacuum evaporation and patterned using photolithography. It is worth noting that the Br intercalation process is corrosive, and can remove any metal contacts that are exposed to Br. Hence, metal deposition should be performed after intercalation. Further discussions about the entire process can be found in Supplementary Section 6.

Inductor fabrication. For inductor samples, after patterning of intercalated MLG, SU-8 photoresist was spin-coated, patterned and hard baked to form a permanent low-*k* polymer dielectric layer with a thickness of 2 μm and a dielectric constant of 3.1. Then, metal contacts and pads (Ni/Au: 100 nm / 2,000 nm) were deposited and patterned. The metal pad structures are designed as a GSG CPW with a MLG inductor in the signal path. It is worth noting that to ensure transport of the transverse electromagnetic mode in the CPW, the two GSG ports should be far away from each other. This can also suppress the higher-order modes, which could radiate and affect the results. Further discussions about the entire process can be found in Supplementary Section 8.

Data Availability. The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author Contribution

K.B. conceived the idea and led the research. J.K., X.L. and J.J. performed the modelling and simulations guided by K.B. and J.M. J.K., X.L. and X.X. designed the inductor layouts. J.J., Y.M., K.K., M.K. and K.U. performed the doping process. J.H.C., K.K., M.K. and K.U. performed the Raman, XPS, ultraviolet photoelectron spectroscopy, EDX, STEM and Hall measurements. X.X. and J.J. performed the AFM measurements. J.K., J.J., X.X. and W.L. fabricated the devices and performed electrical measurements. X.L. and J.K. analysed the data. J.K. and K.B. wrote the main paper and the Supplementary Information Sections with input from all other authors.

Competing Interest

The authors declare no competing financial interests.

Additional information

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